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Abstract—**Designing a switched-mode power supply includes the calculation of the loss in all of the different components: inductor, transformer, switches and capacitors. By combining all of the loss calculations, and providing a graphical user interface to the designer, the designer is able to get an understanding of the loss distribution and thereby the influence of each component on the complete design.**

Keywords—dc-dc converter, low-loss, H-bridge, IFBB, SMPS

I. INTRODUCTION (*HEADING 1*)

Renewable energy systems, electrical vehicles and dc microgrids all require flexible and effective reversible dc power flows, making bidirectional dc-dc converters essential [1]–[4]. Often galvanic isolation is a requirement in order to avoid failures propagating through the system. A common way of achieving galvanic isolation is the use of a transformer, which can then also be used to increase the gain of the converter [5]. The plethora of bidirectional dc-dc topologies, and their derivations, can for high voltage gain be narrowed down to two common ones; the dual active bridge (DAB) and the isolated full bridge boost/buck (IFBB) [6], [7]. The IFBB is chosen as the focus of this paper due to a simpler control than the DAB. The simpler control comes at the cost of the IFBB being a hard switching topology, and thereby having higher switching losses than the DAB, which can achieve soft switching. The IFBB can be seen in Figure 1. The IFBB is chosen as an example for a visual approach to designing dc-dc converters because of its inclusion of the common components found in a converter: switches, inductor, capacitors and a transformer. The example program has been written in Python.

II. EASE OF USE

Before designing the dc-dc converter the system specification needs to be set. The system is defined by three of the following four specifications: input voltage, output voltage, input current and output current. Conversation of power will set the last system specification. At this point it would also make sense to choose the switching frequency (f_{sw}) of the converter, as that will influence the rest of the component designs.

The design of a dc-dc converter involves many different choices, including: core shape, core material, and winding strategy for the inductor (and transformer if it is included in the topology), and switches and capacitors. A summary of the needed steps can be seen in Figure 3 as a flowchart.

A. Inductor design

The first component to be designed is the inductor, since it will determine the ripple current in the converter, and thus it has an influence on the switching losses, the losses in the capacitors and the losses in the transformer. Once the inductor has been designed, the resulting ripple current needs
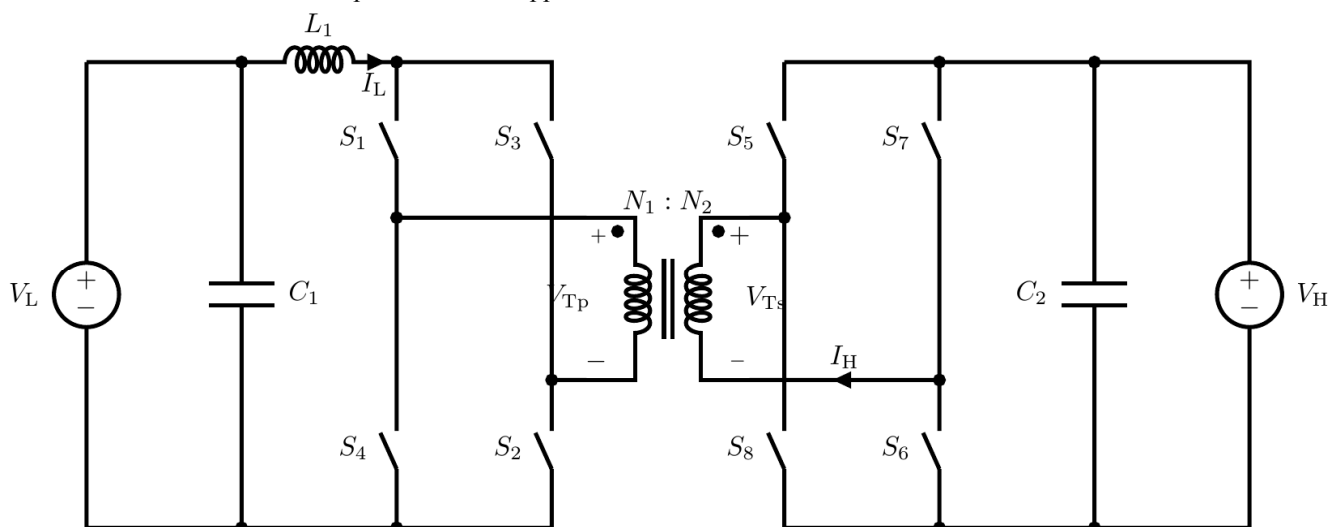

Figure 1: Schematic of the Isolated Full Bridge Boost converter.

to be used for the rest of the component design and choices.

For this example the inductor is chosen to be implemented as a planar inductor. Beside the shape and material of the core, also the number of windings of the inductor has a big influence on the inductance, and by extension the ripple current in the converter. The ripple current (dI) can be calculated from the voltage across the inductor (V_{ind}), the time period of the voltage (D_{ind} and $T_{ind}T$) and the inductance (L) as

$$dI = \frac{V_{ind} \, D_{ind} \, T_{ind}}{L}. \tag{1}$$

The ripple current versus different number of turns are then shown visually in the program as seen in Figure 3. To make it easy to change between different core sizes and core materials, these are also included in the program as a button to click. Along with the ripple caused by the inductor, the losses that are dissipated in the inductor are also interesting, and should be considered at the same time as the ripple current – thus a tradeoff between losses, ripple current, number of turns and the size of the air gap in the core should be chosen. The losses in the inductor can be split into core and winding losses, where the core loss (P_{core}) are determined by the core shape, core material, switching frequency in the inductor (find) and the magnetic flux, as

$$P_{core} = K \, f_{ind}{}^{\alpha} \, B_{pk}{}^{\beta} \, V_e, \tag{2}$$

where K, α, and β are material constants (that can be calculated from the manufactures datasheets), and V_e is the effective volume of the chosen core [8], [9].

For calculating the winding loss ($P_{winding}$), first the dc resistance is found by

$$R_{dc} = \frac{\rho \, l}{w \, t}, \tag{3}$$

where ρ is the resistivity of the material, l is the length of the trace, w is the width of the trace and t is the thickness of the trace. Next the ac resistance (R_{ac}) can be found by [9]
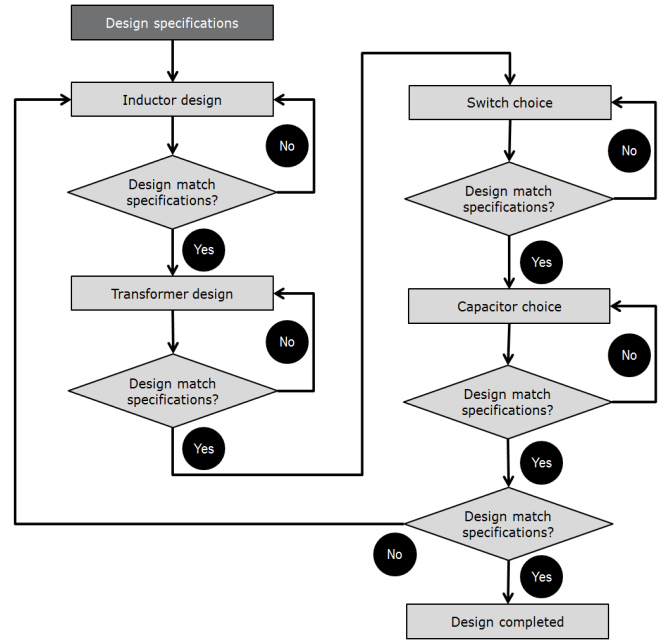

Figure 3: Flowchart showing the design process of a dc-dc converter

$$
\begin{aligned}
R_{ac} &= R_{dc}(2m^2 - 2m + 1) \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)} \\
&\quad - 4m(m-1) \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)},
\end{aligned} \tag{4}
$$

where $\varphi = h/\delta$, and h is the thickness of the copper traces and δ the skin depth of copper at the switching frequency. m is the ratio of magneto-motive force (MMF) to the layer ampere-turns and is given by

$$m = \frac{MMF(h_1)}{MMF(h_1) - MMF(h_0)}, \tag{5}$$

where h_1 and h_0 is representing the two layers of the inductor being analyzed.

Now the loss in the winding can be calculated by multiplying the resistances with the square of the respective dc and ac currents as
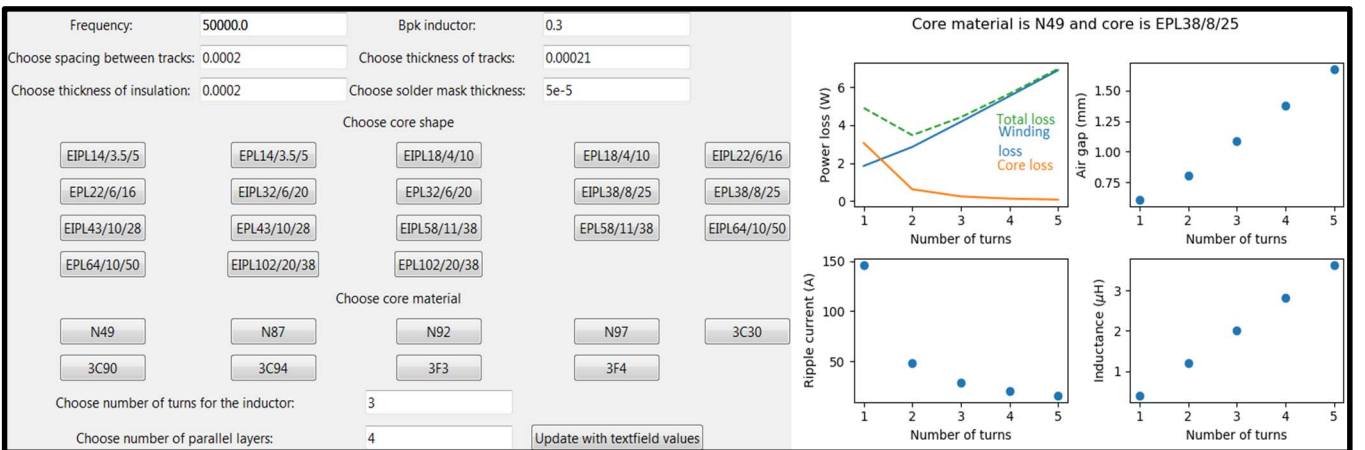

Figure 2: The interface of the inductor choices, along with the results when using it.
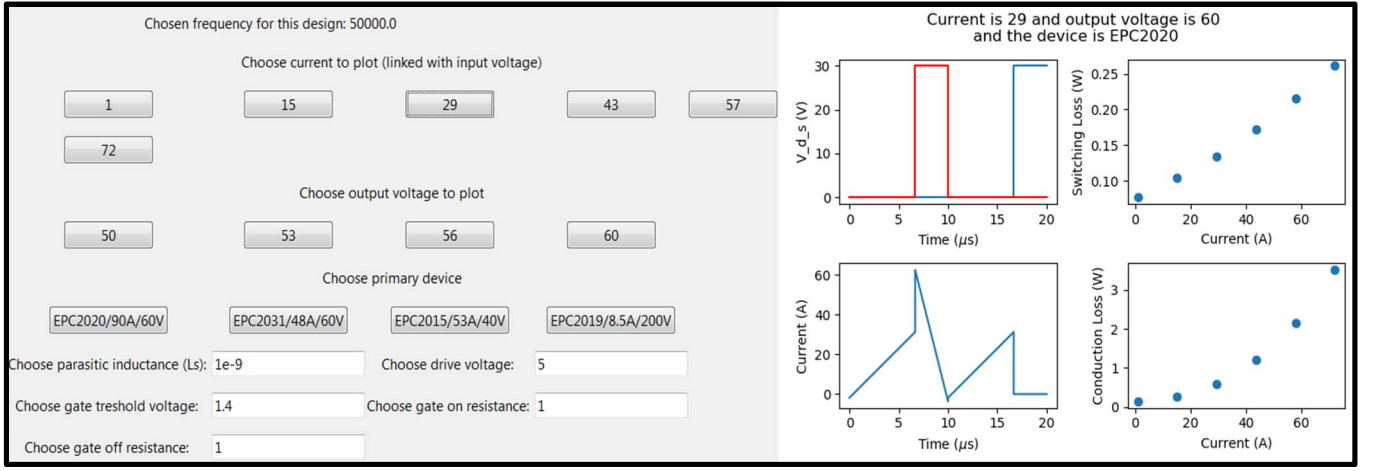
Figure 4: Example of a way to visualize the choice of switching devices.

$$P_{\text{winding}} = R_{\text{dc}}I_{\text{in}}^2 + R_{\text{ac}}\left(\frac{\frac{dI}{2}}{\sqrt{3}}\right). \tag{6}$$

B. Transformer design

The transformer is also made as a planar transformer using a printed circuit board (PCB), and it has the same core shapes and materials available as the inductor. When calculating the loss in the transformer, the interleaving between primary and secondary windings has to be considered [10]. This means that the losses will be changing depending on interleaving strategy, where the simplest approach is to have a complete interleave of primary and secondary layers, which results in $m = 1$. The rest of the loss calculation for the transformer are exactly as for the inductor.

C. Choosing switches

The switches should be chosen so that they are rated for the voltage and current conditions that they are going to experience. This means that an analysis of all waveforms in the converter should be done, and is here plotted in Figure 4 right side, where the top left figure shows the voltages and the lower left graph shows the current.

Table 1: Parameters used in (8), (9), (10) and (11)

Parameter	Description
V_{bus}	Applied voltage across V_{DS} of the transistor
I_{DS}	Current through the transistor
f_{sw}	Switching frequency
Q_{GD}	Gate charge required to leave the plateau
R_{Gon}	Gate resistor for turn on
V_{DR}	Gate drive voltage
V_{pl}	Gate plateau voltage at Q_{GD}
Q_{GS2}	Gate charge required to reach the plateau voltage
R_{CSI}	Resistor equivalent from the common source inductor
V_{th}	Gate threshold voltage
R_{Goff}	Gate resistor for turn off
C_{oss}	Output capacitance

For this design program the choice was made to calculate GaN FETs, and split the losses into conduction and switching. The conduction loss is calculated by using the on resistance of the device ($R_{\text{ds,on}}$) and multiply it by the current through the device squared as

$$P_{conduction} = R_{\text{ds,on}}I^2, \tag{7}$$

The switching loss can be split into four different parts: the switch on loss, the switch off loss, the output capacitance loss and the loss occurring from the capacitance of the switching node, which here will be taking as the output capacitance of the other switch in the half-bridge. The switch on loss is calculated using (9) from [11] and is given as

$$P_{\text{on}} = \frac{V_{\text{bus}}I_{\text{DS}}f_{\text{sw}}}{2}\left(\frac{Q_{\text{GD}}R_{\text{Gon}}}{V_{\text{DR}} - V_{\text{pl}}}\right.$$
$$\left. + \frac{Q_{GS2}(R_{\text{Gon}} + R_{\text{CSI}})}{V_{\text{DR}} - \left(\frac{V_{\text{pl}} + V_{\text{th}}}{2}\right)}\right), \tag{8}$$

and the switch off loss is calculated as

$$P_{\text{off}} = \frac{V_{\text{bus}}I_{\text{DS}}f_{\text{sw}}}{2}\left(\frac{Q_{\text{GD}}R_{\text{Goff}}}{V_{\text{pl}}}\right.$$
$$\left. + \frac{Q_{GS2}(R_{\text{Goff}} + R_{\text{CSI}})}{\left(\frac{V_{\text{pl}} + V_{\text{th}}}{2}\right)}\right). \tag{9}$$

On top of the switching losses there will also be losses in the output capacitor and the switching node capacitance [12]. Both of these losses can be calculated the same way as

$$P_{\text{oss}} = f_{\text{sw}}\int_0^{V_{\text{bus}}} V_{\text{DS}}C_{\text{oss}}dV_{\text{ds}}, \tag{10}$$

and

$$P_{\text{qoss}} = f_{\text{sw}}\int_0^{V_{\text{bus}}} (V_{\text{bus}} - V_{\text{DS}})C_{\text{oss}}dV_{\text{ds}}, \tag{11}$$

where the parameters used in (8), (9), (10) and (11) are explained in Table 1. The parameters are a combination of datasheet values and system values. The loss calculation can
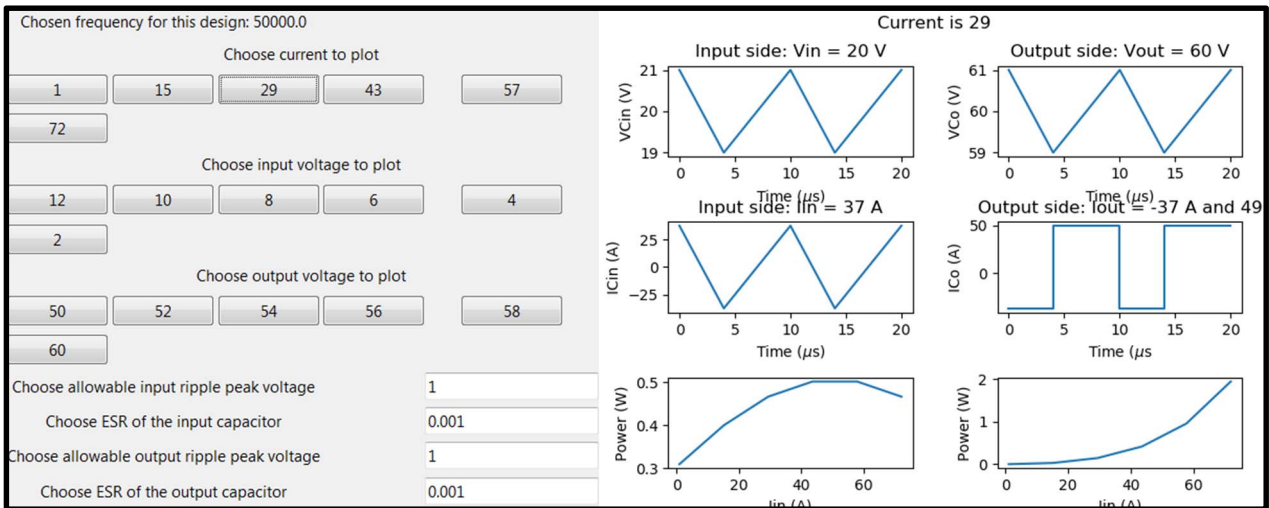
Figure 5: Visualization of the waveforms concerning the capacitors.

be seen in Figure 4 to the right, where the losses has been split in conduction and switching loss.

D. Choosing capacitors

Both the input and output capacitor needs to be chosen so that the voltage ripple caused due to the charging and discharging of the inductor are acceptable, and so that the losses in the capacitor also stays low. The capacitance needed can be calculated based on the triangular waveform of the inductor current seen in Figure 5 middle row to the left. The minimum input capacitance ($C_{in,min}$) can thus be determined based on

$$C_{in,min} = \frac{dI}{16\,f_{sw}dV_{in,pp}}, \tag{12}$$

where $dV_{in,pp}$ is the allowable voltage ripple. For the output capacitor the current waveform is a square, as seen in Figure 5 middle row to the right, resulting in a minimum output capacitance of

$$C_{out,min} = \frac{I_o}{4f_{sw}dV_{out,pp}}, \tag{13}$$

where $dV_{out,pp}$ is the allowable output voltage ripple and I_o is the output current. Figure 5 top graphs shows the voltage ripple with the chosen capacitance.

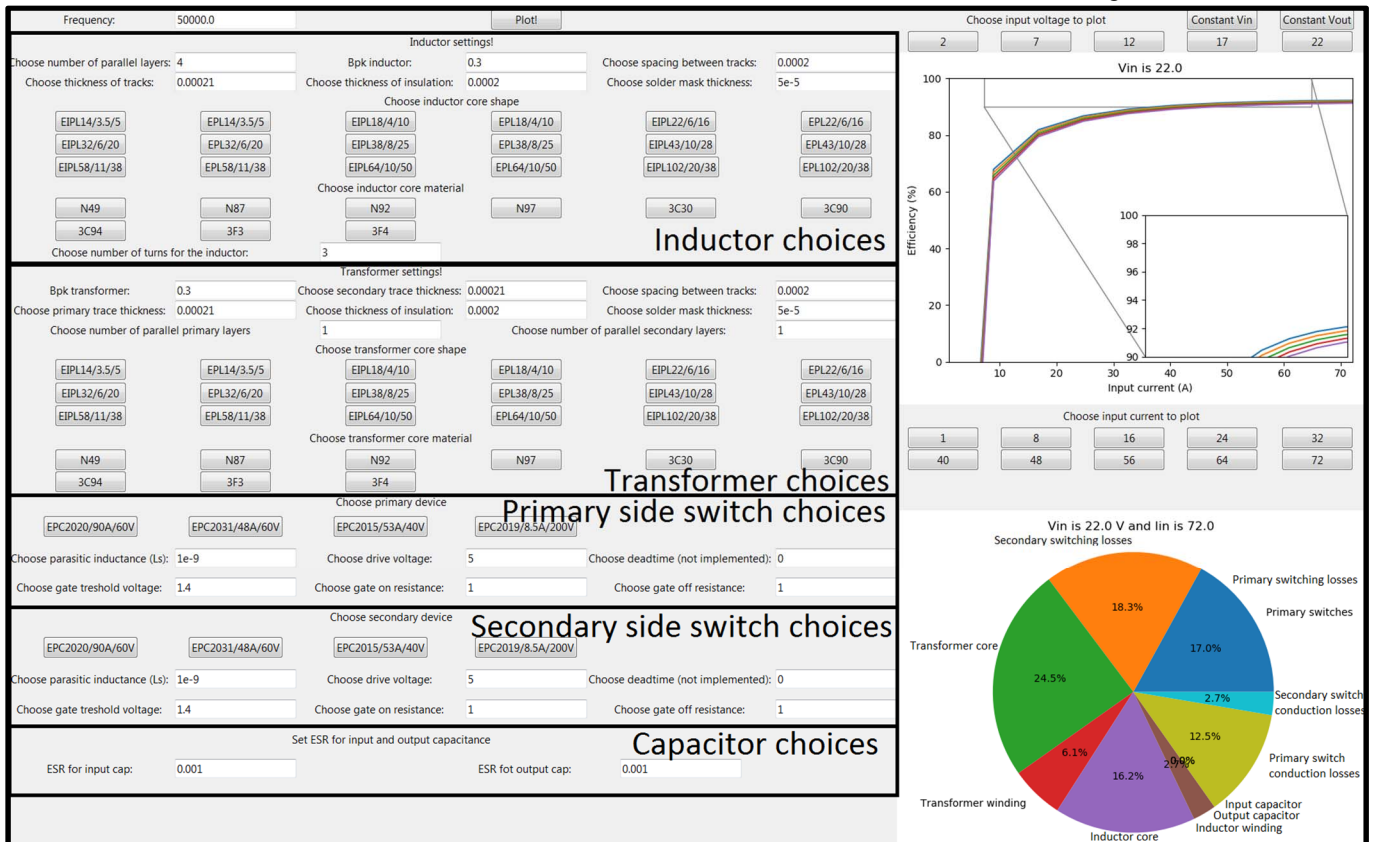To calculate the loss in the capacitors, first the rms

Figure 6: Example view of a picture showing all the choices, complete loss in the dc-dc converter and the break-down of the losses into individual components.

current ($I_{\text{Cin,rms}}$ and $I_{\text{Cout,rms}}$) through them are calculated as

$$I_{\text{Cin,rms}} = \frac{dI}{\sqrt{3}}, \tag{14}$$

and by multiplying with the series resistance (ESR_{Cin}) the loss in the input capacitor is

$$P_{\text{Cin}} = I_{\text{Cin,rms}}{}^2 ESR_{\text{Cin}}. \tag{15}$$

For the output capacitor the rms current is

$$I_{\text{Cout,rms}} = I_o \sqrt{\frac{1 - 2D}{2D - 2}} \tag{16}$$

and the loss is

$$P_{\text{Cout}} = I_{\text{Cout,rms}}{}^2 ESR_{\text{Cin}}. \tag{17}$$

The losses of the capacitor can be seen in Figure 5 bottom graphs.

III. COMPLETE DESIGN

Once all of the individual elements has been added to program, they can be combined in a complete loss picture as shown in Figure 6, where the efficiency is shown along with a breakdown of the different elements contribution to the losses. The loss breakdown can be viewed at different operating condition, giving the means to see what is degrading the efficiency at any operating condition.

With the visual approach two designs can be compared side-by-side as shown in Figure 7, to see which design is performing best, but also to see what the differences between the two designs are.

IV. CONCLUSION

This paper illustrates a way to visualize the design process of a dc-dc converter, so that a better understanding of the different choices / trade-offs of the converter design can be gained. Suggestions on how to visualize each component design are included, and an example of a gathered program that shows all of the choices at once.
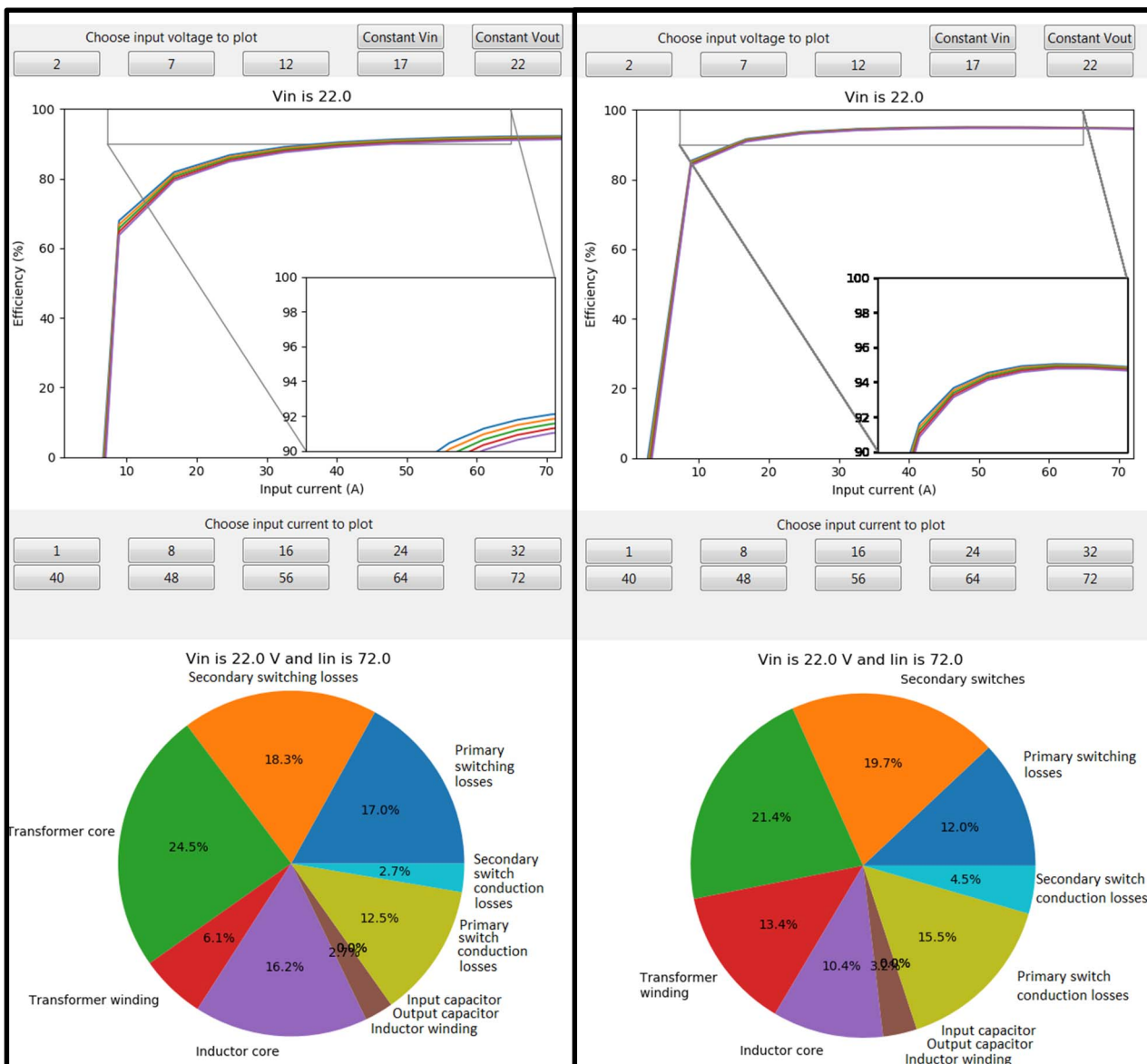
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Figure 7: Comparison between a low efficiency design on the left, and a higher efficiency design on the right.

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