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Keywords

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Abstract

Decreasing size of consumer electronics pushes demands for higher power density and higher efficiency. Increased switching frequency can reduce the size, but generating MHz gate signals is nontrivial, e.g. due to jitter. We show a custom IC containing a low jitter VCO and gate driver, capable of driving MOSFETs at 5-35 MHz.

Introduction

To address the need for smaller consumer electronics, the demand for power converters with higher power density is increasing [1]. The main way to increase power density is to increase switching frequency of the power MOSFETs [2, 3, 4]. This greatly reduces the need for bulky passive components. However, a downside to the increasing power density is the lowered surface area of the power converters.

If a power converter adheres to the IEC 60065:2015 standard [5], its enclosure surface temperature cannot exceed a temperature rise above 60 K. To estimate the maximum radiated and convected power from an enclosure (1) and (2) can be used,

$$P_{radiated} = \sigma \, \varepsilon \, S_a \left(T_a{}^4 - T_{amb}{}^4 \right) \tag{1}$$

$$P_{convected} = 4 \, C_c \, \frac{G \cdot S_a}{L^{0.25}} \, \Delta T^{1.25} \tag{2}$$

where σ is Stefan Boltzmanns constant, ε is the emmissitivity of the material used, S_a is the surface area and T_a and T_{amb} is the surface temperature of enclosure and the ambient temperature, respectively, both given in kelvin. G and L are geometric constants [6]. For a laptop charger enclosed in black plastic with a surface area of $93 \, cm^2$, a commercially available state-of-the-art laptop charger, the maximal radiated and convected power to the air is 4.96 W. Assuming the charger outputs 60 W, the efficiency of the converter has to be above 92.9 %.

Further, with increasing frequency the driving of the MOSFET is a challenge. In the discrete PCB design, many self-oscillating gate drives have been developed, and designed [4, 7]. These utilizes the resonance of the power converter it self, and a high Q inductor, to generate the required gate signal. However, the

use of high Q inductors makes these types of gate drives undesirable of monolithic integration [8]. In this work another approach is used, designing a custom integrated circuit, consisting of a voltage controlled oscillator (VCO) together with a high power gate driver, capable of driving transistors in a frequency range of 5–35 MHz.

One drawback of this type of oscillator, compared to its self-oscillating counterpart, is the susceptibility to noise. In general, any voltage controlled oscillator will be susceptible to noise, often translated to frequency jitter [9, 10]. Jitter is here defined as the standard deviation in seconds, from the average generated time period. Although state-of-the-art VCOs designed for communication purposes have jitter in the 100s of fs [11, 12], the requirement for VCOs in power conversion is much less strict. Many TI integrated controllers, designed for switching frequencies from 150 kHz to 500 kHz, experience jitter from 20–200 ns, corresponding to an effective jitter of 1 % to 3 % of the period [13].

To mitigate the increased switching losses from going up in frequency, topologies utilizing Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) are often used. As these converters benefits from their low switching losses, jitter in the VCO will affect their efficiency. Additionally, other work [14] have shown that jitter, and here more specifically PWM-jitter, can result in efficiency drop of up to 1 percentpoint(pp).

In this work we first present an analysis of frequency jitter effect on a resonant Class E converter, and here after present our taped-out custom integrated VCO and gate driver, as well as the characterization of this.

Class E Analysis

To quantify the effect of jitter on a resonant power converter, an LTSpice simulation was run, of a class E converter (see fig. 1), at 3 different switching frequencies. A class E converter consist of a class E-inverter and -rectifier, generally known from the RF world. It is used for among others wireless power transfer power amplifiers [15, 16]. In fig. 2, the theoretical waveforms of a ZVS class E converter is seen. All three converters where tuned to having as close to both ZVS and ZCS as possible, allowing for a larger time period, where switching can occur - minimizing the possible effect of the jittery gate signal. However, with the class E converter, there is a limited upper frequency where ZCS is possible, depending on the output power, and output capacitance of the chosen MOSFET [17].
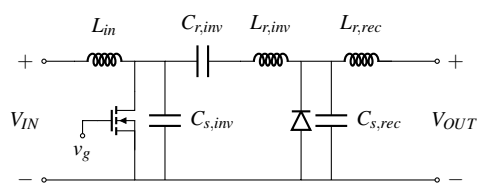

Fig. 1: Class E Converter consisting of a Class E Inverter and Rectifier.
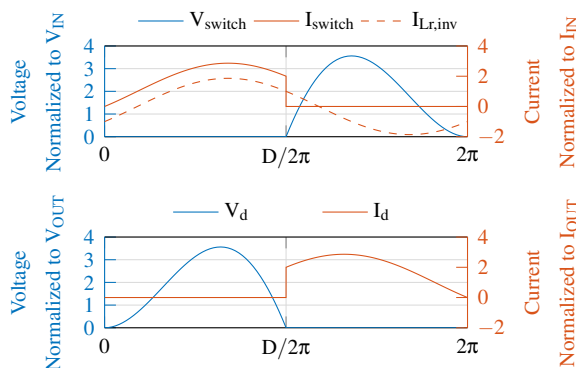

Fig. 2: Operating waveforms of a ZVS Class E Inverter (top) and Rectifier (bottom). Inverter generates a RF sinusoidal current, which is rectified by the diode.

The converter has been tuned for 48 V input voltage and 12 V output voltage, and with an output power of 60 W. Python was used to generate a gate signal, v_g, with a fixed pseudo-random jitter, and then LTSpice simulated the resulting waveforms and efficiency. The MOSFET in the simulation is an EPC2019 GaN-FET from EPC. The inductors is implemented with a series resistance of 5 mΩ. In fig. 3 the general overview of the resulting efficiency is shown.
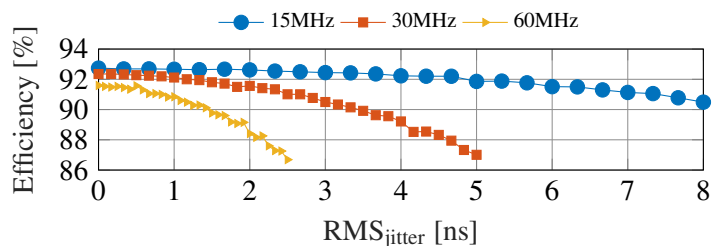
Fig. 3: ZVS and ZCS Class E Converter Simulated Efficiency vs. Jitter at different switching frequencies

The class E converter has another undesired effect of added jitter, and that is that the duty cycle determines the peak voltages of both the MOSFET and the diode. The converter is simulated with fixed duty cycle, however, because the frequency is changing, the resulting effect is equal to a different ON time. Thus, the peak voltages seen on the MOSFET and diode are higher than expected.
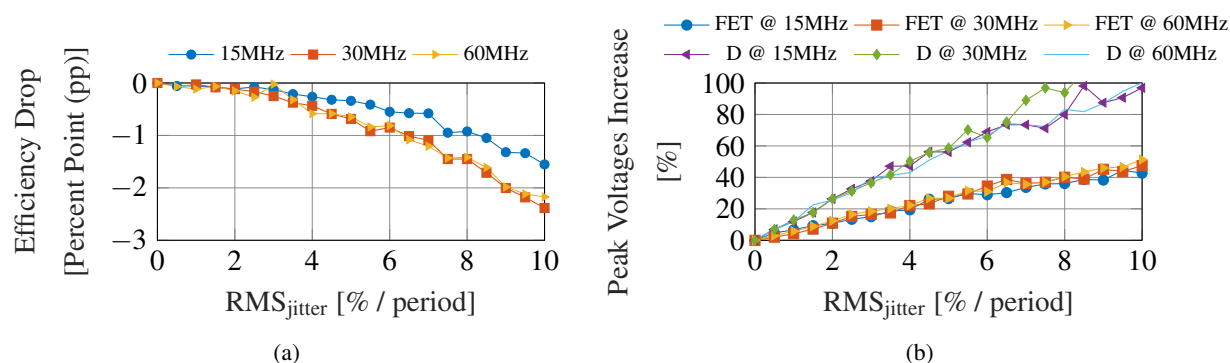

Fig. 4: Simulated Jitter Effect on a Class E converter. (a): The efficiency drop from nominal, normalized to the switching frequency. (b): Peak voltage deviation on the MOSFET and diode.

It is evident that jitter on a gate signal, in a class E converter, does not only affect the efficiency, but also the peak voltages. At 3-5 % jitter the 30 and 60 MHz the efficiency drop is 0.5-1 pp. This is similar to what was found in [14] for a buck converter. Furthermore, the peak voltage on the MOSFET and the diode is almost 30 % and 60 % higher, respectively, at 5 % jitter. This would have to be considered in the component selection.

Voltage Controlled Oscillator

Generate a 15–60 MHz gate signal for a power converter, is as mentioned not a trivial task. Commercially gate drivers capable at these frequencies are scarcely available, and the frequency is generally generated from a signal generator. In this work we have designed a VCO capable of running frequencies from 4–50 MHz. In figure 5a a block diagram of the designed chip is presented. It consist of a VCO, a signal splitter box, which adjust the duty cycle and deadtime between the two channels, and finally the two gate drives, which is implemented as a simple buffer chain.

The VCO is implemented as a current starved inverter ring oscillator, pictured in fig. 5b. The voltage V_{vco} is used to generate two bias voltages, $V_{bias,p}$ and $V_{bias,n}$, that controls the current available to the inverter. The ring oscillator is implemented with an odd numbered inverters, and the current can thus control the frequency that this is then oscillating at. To minimize the achieved jitter, a differential inverter chain could be implemented. However, the singled ended chain is deemed to give acceptably low jitter. The IC was manufactured in a 0.18 μm CMOS process. Fig. 6 shows a photo of the taped out chip.
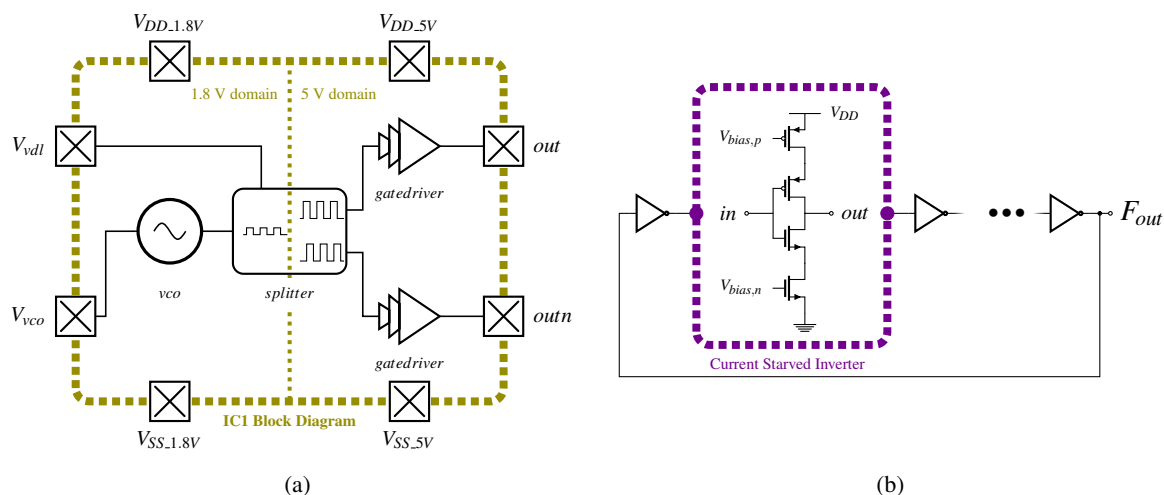
(a)

(b)

Fig. 5: (a): Block diagram of the designed chip. It consist of a voltage controlled oscillator (VCO), a signal splitter, which levelshifts, and a gate driver implemented as a buffer chain (b): Implemented VCO topology

Fig. 6: Photo of Designed Chip

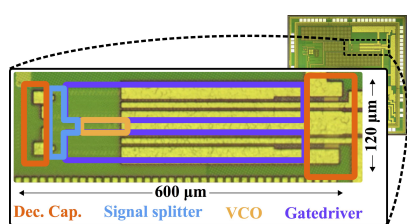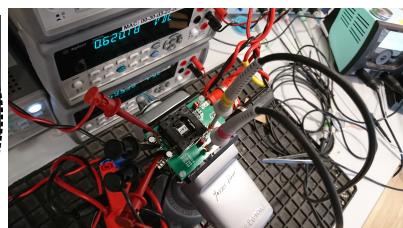Fig. 7: Picture of Measurement setup

Fig. 8: Measured Eyediagram
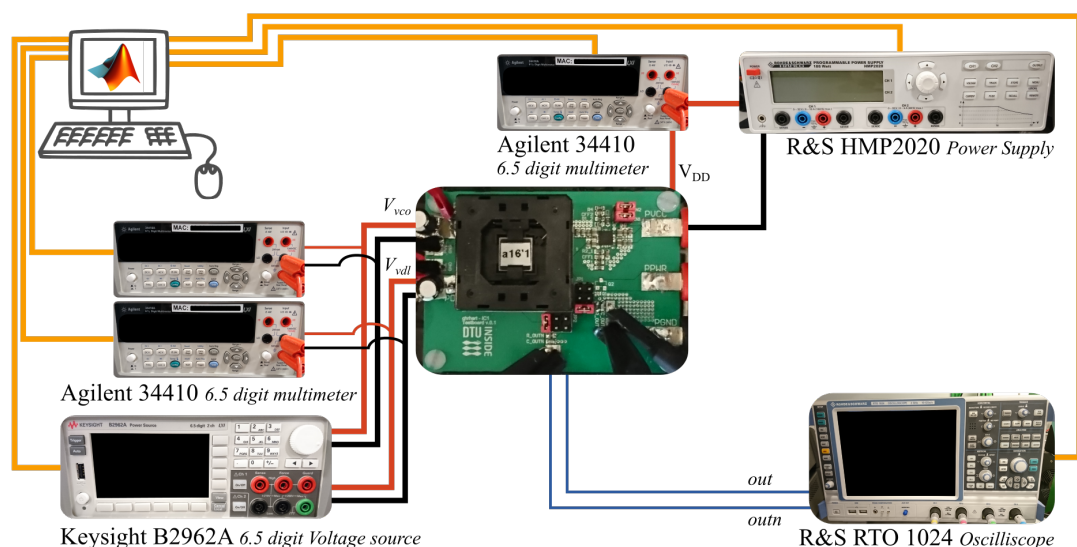
Fig. 9: Block diagram of Automated setup. MATLAB was used to control the instruments.

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An automated setup has been built in the lab. A block diagram of the setup is shown in fig. 9. The frequency and period jitter was measured, across a varying bias voltage. It was measured according to [18], where two adjacent rising edges are measured 1000 times, and their standard deviation is calculated. Jitter follows a Gaussian distribution, and as such the error amounts to $\approx 2.2\,\%$. A screenshot of one of these measurements is shown in fig. 8. This measurement is performed 25 times, with an arbitrary wait in between, and then averaged. The frequency was measured as the average period time. In total 6 ICs were measured. Although their underlying statistical distribution is unknown, their spread is shown to be very low.
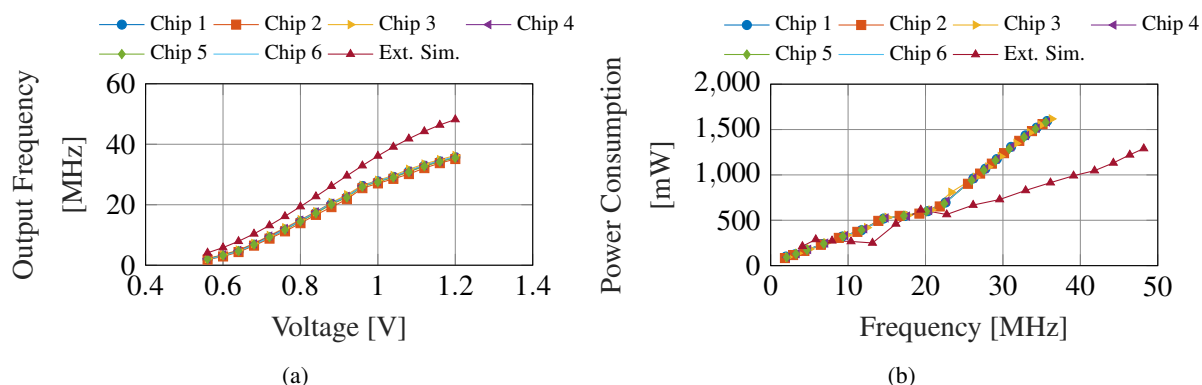

Fig. 10: Results of designed VCO. (a): Generated Frequency at the output. (b): Power Consumption

Fig. 10 shows the voltage to frequency at the output of the IC. The added parasitics of bonding pads and bondwires limits the possible upper frequency, and is the explanation for the larger deviancy in this range. The maximum achievable frequency is $\sim 35\,\text{MHz}$, limited mainly by the bonding wires.
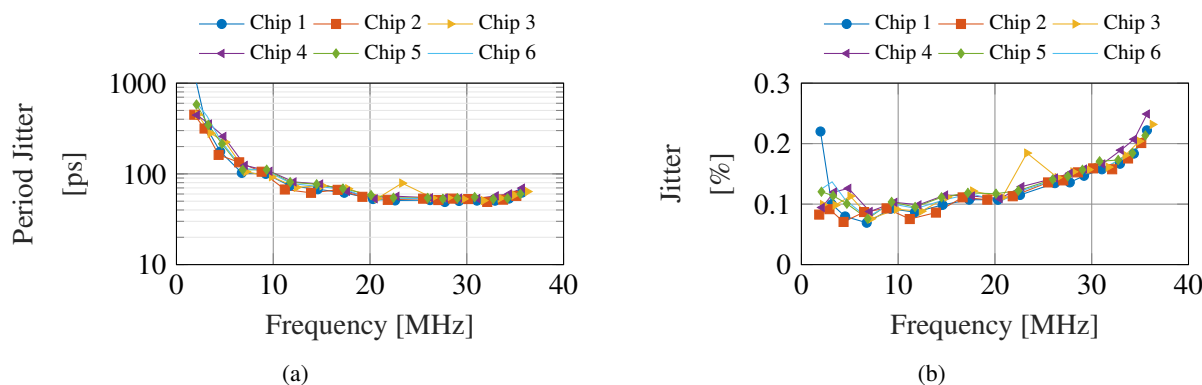

Fig. 11: Jitter of designed VCO. (a): Jitter vs. Output frequency (b): Jitter in percent of period vs. Output Frequency

Fig. 11a and 11b shows the resulting achieved jitter. As discussed, this is far from state-of-the-art jitter performances, but in terms of power electronics is more than capable of driving a power converter to acceptable performances. The jitter is below $0.25\,\%$ of the time period, across the frequency range.

Conclusion

The power density requirements to power converters is currently limited by the efficiency achievable. Pushing the boundary further requires higher efficiency. In order to do so, reducing jitter of gate signals is important. With jitter around $5\,\%$ of the switching frequency, more than $0.5\,\text{pp}$ efficiency is lost in a class E converter. We have designed and measured a voltage controlled oscillator and gate driver capable of pushing the switching frequency of a converter to 5–$35\,\text{MHz}$, with a $\text{RMS}_{\text{jitter}}$ of $<150\,\text{ps}$ corresponding to less than $0.25\,\%$ of a switching period.

References

[1] A. Knott, T. M. Andersen, P. Kamby, J. A. Pedersen, M. Madsen, M. Kovacevic, and M. A. E. Andersen, "Evolution of Very High Frequency Power Supplies," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 386–394, sep 2014.

[2] A. D. Sagneri, "Design of Miniaturized Radio-Frequency DC-DC Power Converters," 2012.

[3] M. Madsen, A. Knott, and M. A. E. Andersen, "Very high frequency half bridge DC/DC converter," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, pp. 1409–1414, 2014.

[4] M. Kovacevic, "Very High Frequency Interleaved Self-Oscillating Resonant SEPIC Converter," *Proceedings of Epe '13-ecce Europe*, 2013.

[5] C. European Committee for Electrotechnical Standardization, "IEC 60065:2015 - Audio, video and similar electronic apparatus - Safety requirements," 2015.

[6] J. Møltoft and L. Rimestad, *Termisk Design*, 1st ed.   DTU, Technical University of Denmark, 2004.

[7] M. Madsen, J. A. Pedersen, A. Knott, and M. A. E. Andersen, "Self-oscillating resonant gate drive for resonant inverters and rectifiers composed solely of passive components," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*.   IEEE, mar 2014, pp. 2029–2035.

[8] J. C. Hertel, Y. Nour, and A. Knott, "Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 526–538, 2018.

[9] A. Hajimiri, S. Limotyrakis, and T. Lee, "Jitter and phase noise in ring oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, jun 1999.

[10] X. Zhang and A. B. Apsel, "A Low-Power, Process-and- Temperature- Compensated Ring Oscillator With Addition-Based Current Source," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 5, pp. 868–878, 2011.

[11] T. Seong, Y. Lee, S. Yoo, and J. Choi, "A -242-dB FOM and -71-dBc reference spur ring-VCO-based ultra-low-jitter switched-loop-filter PLL using a fast phase-error correction technique," in *2017 Symposium on VLSI Circuits*.   IEEE, jun 2017, pp. C186–C187.

[12] J.-m. Kim, J.-s. Lee, S. Kim, T. Kim, H. Park, S.-g. Lee, W. Wkh, S. Dqdo, V. L. V. Dqg, D. Ri, Z. Wxqlqj, U. Lv, V. Lq, W. K. H. Kljk, Q. G. H. Yrowdjh, and F. Rvfloodwru, "LC-VCO in 65nm CMOS," pp. 7–10, 2015.

[13] M. Schurmann, "Not All Jitter is Created Equal: Understanding Jitter in Switching Power Supplies," Tech. Rep., 2015.

[14] C. Yaow-ming, F.-y. Wu, C.-y. Wang, Y.-m. Chen, and C. Yaow-ming, "Converter Efficiency Measurement with PWM Duty Cycle Jitter Department of Electrical Engineering Keywords The PWM Duty Cycle Jitter," pp. 1–8.

[15] P. Niefnecker, M. Simon, S. Salich, and J. Pforr, "Comparison of switching devices for a zero-current switched class E based automotive inductive charging converter system," in *Proceedings - European Conference on Power Electronics and Applications (EPE'17 ECCE-Europe)*.   IEEE, sep 2017, pp. P.1–P.10.

[16] S. Salich, M. Lang, and J. Pforr, "Investigation of the zero-current switched class E converters for automotive wireless power transfer inductive charging applications," in *Proceedings - European Conference on Power Electronics and Applications (EPE'16 ECCE-Europe)*.   IEEE, sep 2016, pp. 1–10.

[17] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, 2nd ed.   Wiley, 2011.

[18] SiTime, "Clock Jitter Definitions and Measurements Method - AN10007," 2014.

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