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Sensitivity Optimization of Wafer Bonded Gravimetric CMUT Sensors

Mathias J. G. Mølgaard, Jesper M. F. Hansen, Mogens H. Jakobsen, and Erik V. Thomsen

Abstract*— Optimization of the mass sensitivity of wafer bonded resonant gravimetric capacitive micromachined ultrasonic transducers (CMUTs) is presented. Gas phase sensors based on resonant gravimetric CMUTs have previously been demonstrated. An important figure of merit of these sensors is the sensitivity which, for typical CMUT geometries, is increased by decreasing the radius of the CMUT cell. This paper investigates how to minimize the radius of CMUT cells fabricated using the wafer bonding process. The design and process parameters affecting the radius of the CMUT and hereby the sensitivity are studied through numerical simulations and atomic force microscopy measurements. An excellent fit was obtained between the simulations and measured profiles with a low relative error of $\leq 5\%$, thus validating the simulation model. Two types of CMUTs are designed and fabricated using the design and process rules determined herein, with experimentally determined mass sensitivities of 0.46 Hz/ag and 0.44 Hz/ag, respectively. The two CMUT devices have cavities made using the local oxidation of silicon (LOCOS) and reactive ion etching (RIE) process. For the LOCOS process, it was found that the smallest radius can be obtained by choosing a Si_3N_4 oxidation mask and lowering the pad SiO_2 thickness, vacuum gap height, and Si bump height. For the RIE process, the vertical dimensions do not influence the horizontal dimensions and consequently, equivalent rules do not exist. [2018-0135]

***Index Terms*— CMUT, sensor, gravimetry, sensitivity, LOCOS.**

I. Introduction

DETECTION of chemical and biological analytes in the gas phase is important in several fields including homeland security, environmental monitoring, and in different branches of industry. Many different types of sensors exist but it has been demonstrated that Capacitive Micromachined Ultrasonic Transducers (CMUTs), used as resonant gravimetric mass sensors, can achieve a low Limit of Detection (LOD) [1] in the ag range [2] and a high mass sensitivity of up to 0.23 Hz/ag [3]. These properties have e.g. been utilized to detect small concentrations of dimethyl methylphosphonate (DMMP) [2] and greenhouse gasses such as CO_2 [4]. Furthermore, the flat and closed surface of the CMUT eases functionalization. Finally, the actuation and readout schemes are typically electrical which enables miniaturization of the sensor system. In conclusion, the CMUT gravimetric sensor has a desirable combination of characteristics. Since the first CMUT was reported in 1994 [5] one of the main applications, for both researchers and companies, has been medical ultrasonic imaging [6]–[9]. Since then CMUTs have also been applied as e.g. biological or chemical sensors, typically based on the resonant gravimetric principle where a small change in the mass of the plate, due to absorbed analytes in the functionalization layer on the plate, results in a resonance frequency shift [4], [10], [11]. A higher mass sensitivity causes a higher resonance frequency shift for the same amount of added mass. The functionalization layer on the plate provides the sensor with a selectivity toward a desired analyte but typically also decreases the mass sensitivity of the sensor as it increases the mass of the oscillating parts.

In general, two fabrication methods have been used for fabricating CMUTs: a process based on sacrificial release and a process based on wafer bonding. The first CMUTs were fabricated using the sacrificial release process [5], that consists of depositing a sacrificial layer, which is selectively etched by an isotropic wet etch, after it has been covered by a plate layer, hereby forming the cavity of the device. In the wafer bonding process, first proposed by Huang *et al.* [12], cavities are defined in an insulating layer on a substrate wafer that is directly bonded to the plate.

In this paper the wafer bonding fabrication method is used where the cavities typically are defined by either one of two processes, namely the Reactive Ion Etch (RIE) process and Local Oxidation of Silicon (LOCOS) process [13]. In the RIE process cavities are dry etched in an insulating layer (typically SiO_2), while in the LOCOS process two consecutive LOCOS steps result in cavities with a central silicon bump. A cross-sectional sketch of half a LOCOS and RIE defined cavity can be seen in Fig. 1, along with all relevant geometrical variables. The characteristic bird's beak structure is also shown in Fig. 1(a). The RIE and LOCOS processes differ on several points: the number of photolithography masks required is one less for the typical RIE process, thus decreasing the process cost and time. For the LOCOS device the vacuum gap height is decoupled from the post SiO_2 height and small gaps can therefore be made while still maintaining a thick post SiO_2, which decreases the parasitic capacitance between the top and bottom electrode. Hence, the electro-mechanical coupling coefficient is generally higher for the LOCOS device compared with a RIE device. Furthermore, the possibility of fabricating small vacuum gaps is beneficial since this causes lower pull-in voltages and the CMUT can hereby be operated at lower DC voltages. The pull-in voltage is the voltage at which the electrostatic

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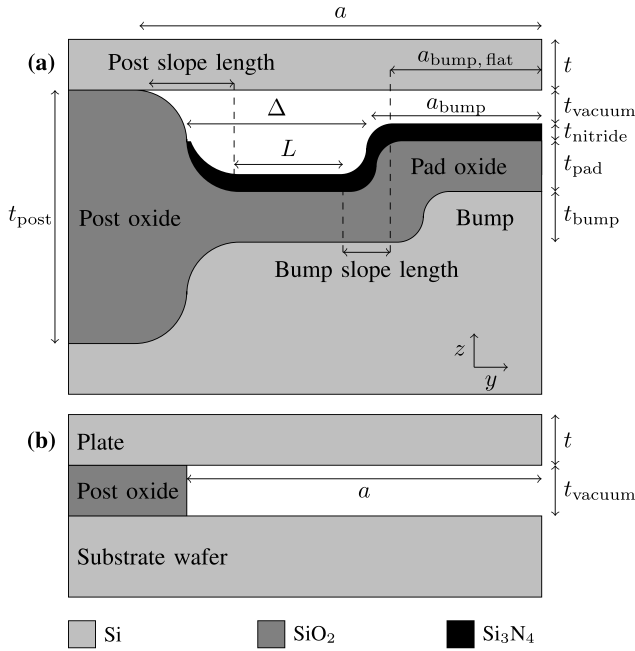

Fig. 1. Cross-sectional sketches of half (a) a LOCOS CMUT cell and (b) a RIE CMUT cell.

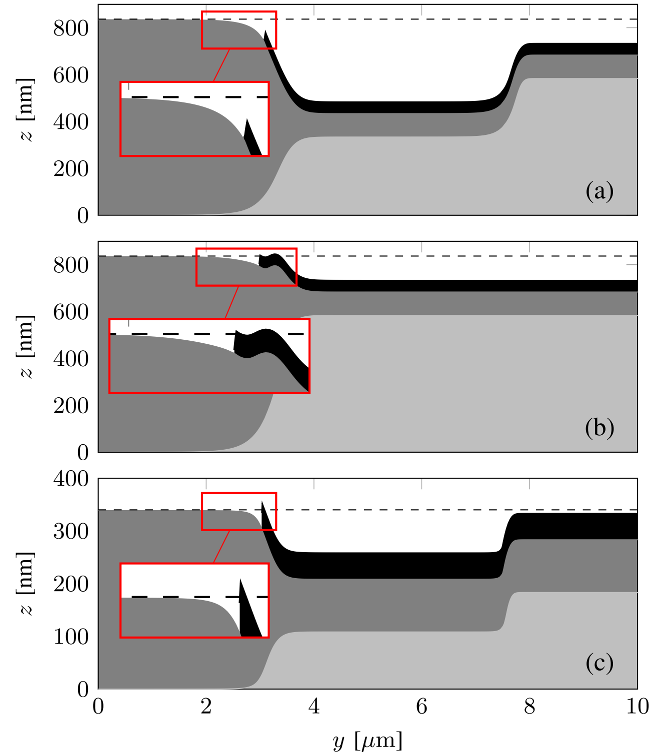

Fig. 2. Simulation results of three different CMUT designs. (a) This design does not inhibit wafer bonding. The designs in (b) and (c) both inhibit wafer bonding since the Si_3N_4 layer protrudes above the post SiO_2 at $y \approx 3\,\mu$m. In (b) the bump is placed too close to the post SiO_2 and in (c) the post SiO_2 is too low.

force, between the top and bottom electrodes, becomes larger than the restoring force from the stiffness of the plate and the plate collapses and touches the bottom of the cavity.

The limit of detection and mass sensitivity are the two most important figures of merit for any resonant gravimetric sensor, which in the ideal case should be as low and as high as possible, respectively. In this article the focus will be on maximizing the mass sensitivity of the CMUT sensor. The CMUT can be modeled as a 1-D linear harmonic oscillator and if the added mass on the plate is small compared with the mass of the plate itself, the sensitivity can be written as [10]:

$$S = \frac{\partial f}{\partial m} = -\frac{1}{2}\frac{f_{\text{res}}}{m_{\text{plate}}} \propto \frac{1}{a^4}, \tag{1}$$

where f_{res} is the resonance frequency, m_{plate} is the mass of the plate and a is the cell radius. For gravimetric gas sensors the sensitivity is often normalized by the plate surface area A:

$$S_{\text{norm}} = \frac{\partial f}{\partial m/A} = -\frac{1}{2}\frac{f_{\text{res}}}{m_{\text{plate}}}A \propto \frac{1}{a^2}. \tag{2}$$

The variable dependencies in Eq. 1 and 2 are found by inserting the symbolic expressions for the resonance frequency and mass of a circular clamped plate. Hence, in order to increase the sensitivity the radius must be decreased. However, a practical lower limit of the radius exists, depending on the plate thickness, where the resonance peak signal approaches the noise floor and the resonance frequency becomes impractically high. Thus, the plates studied in this paper are assumed to have aspect ratios of $a/t \gtrapprox 10$. For LOCOS cavities the smaller radii can become comparable with the lateral width of the bird's beak SiO_2 which in Fig. 1(a) is defined as the 'slope length'. This ultimately limits the radius of the cavity and the sensitivity can hereby be limited by the process parameters that affect the slope length of the bird's beak. The bird's beak structure have previously been studied extensively due to its use as an isolation structure in semiconductor manufacturing [14]–[16], since reduction of the horizontal size has been especially important due to the decrease in device dimensions. However, for small radii ($a < 5\,\mu$m) CMUT cells the more complex geometry has yet to be investigated.

Not all CMUT designs can be fabricated. The main reason being the inability to bond the plate to the cavity wafer. For the RIE process it has previously been shown by Sarioglu *et al.* [17] how oxidation of convex silicon corners can lead to protrusions in the SiO_2 at the corners which can hinder bonding. A study by Christiansen *et al.* [18] showed how the corners of a structured SiO_2 layer are lifted when the wafer is re-oxidized in order to e.g. grow an insulation SiO_2 layer, consequently making bonding impossible. Likewise, some LOCOS designs will hinder bonding but here the problem is slightly different as the solution depends on choosing the right combination of design and process parameters, where for the RIE process the problems are solved by adjusting the process flow. The main challenge, when designing the LOCOS device, from a fabrication point of view, is keeping the Si_3N_4 layer from protruding above the post SiO_2 at the cavity edge, thus inhibiting bonding. Fig. 2 shows three simulated LOCOS devices where (a) is an example of a device that can be fabricated, (b) cannot be fabricated due to the protruding Si_3N_4 layer caused by an overlapping post SiO_2 and silicon bump, either as a result of a bad design choice or misalignment in the lithography step. Finally, in situation (c) the post SiO_2 is too

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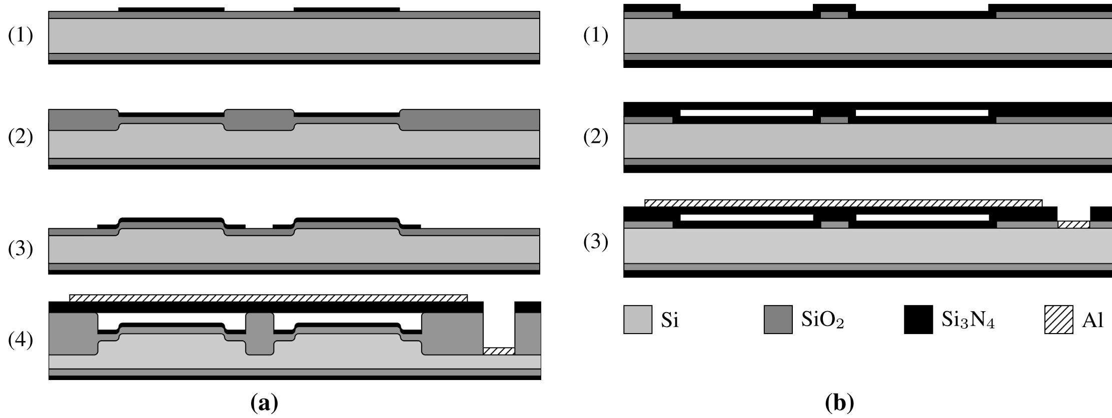

Fig. 3. Process flow of the (a) LOCOS and (b) RIE CMUT. In (a) step (1) a thermal pad SiO_2 layer is grown and subsequently a LPCVD Si_3N_4 layer is deposited and patterned by a RIE etch. In step (2) the LOCOS is performed, forming the Si bumps. Step (3) is a repeat of step (1). Finally, in step (4) the second LOCOS is performed and the cavities are seal under vacuum by fusion bonding a Si_3N_4 layer to the cavity wafer. Openings to the bottom electrode are made and Al is deposited and wet etched. In (b) step (1) a thermal SiO_2 is grown and patterned by a RIE etch. Next a LPCVD Si_3N_4 layer is deposited and the subsequent steps are the same as in the LOCOS process.

TABLE I

TABLE OF TARGET AND MEASURED VALUES FOR THE SEVEN WAFERS FABRICATED FOR THE EXPERIMENTAL VALIDATION OF THE SIMULATION MODEL

Parameter	Wafer number							
	1	2	3	4	5	6	7	Unit
t_{pad} target	0	10	50	100	-	-	-	[nm]
t_{pad} measured	0	10.6	56	99.4	-	-	-	[nm]
Mask SiO_2 thickness target	-	-	-	-	1000	2000	3000	[nm]
Mask SiO_2 thickness measured	-	-	-	-	963	1964	2950	[nm]
t_{bump} target	250	250	250	250	250	250	250	[nm]
t_{bump} measured	244	241	241	241	234	247	260	[nm]
Relative difference between target and measured t_{bump}	2.4	3.6	3.6	3.6	6.4	1.2	4	[%]

low, which e.g. could happen if a very small gap is wanted. The simulation model is discussed and validated later. The failure modes in Fig. 2(b) and (c) can be solved by removing the Si_3N_4 layer in the cavity while protecting the post SiO_2 with an etch mask. This can be done at the expense of additional processing steps and an extra lithography step [19]. However, since minimizing the number of process steps and lithography masks is desirable, this paper investigates LOCOS devices fabricated without removal of the Si_3N_4 layer.

In this paper the design of high mass sensitivity wafer bonded CMUTs is studied by means of AFM and numerical simulations. In addition, LOCOS and RIE CMUTs are fabricated and the feasibility of using a Si_3N_4 mask for both LOCOS steps is demonstrated. Furthermore, it is studied how the choice of oxidation masking material and process parameters influences the LOCOS device and hereby ultimately the minimum radius one can achieve and thus the maximum mass sensitivity. Finally, the experimental sensitivities of the fabricated LOCOS and RIE devices are compared with the theoretical values.

II. METHODS

Standard cleanroom fabrication techniques were used to fabricate LOCOS profiles for experimental verification of the numerical simulation model, as well as LOCOS and RIE CMUT devices.

A. Simulation Model

A numerical simulation model was made using the process simulator ATHENA (Silvaco, Inc., California) where part of the LOCOS process in Fig. 3(a) was simulated. The mesh was optimized so the smallest mesh sizes were centered around the position where the bird's beak is formed. The size of the mesh in the SiO_2 has a maximum vertical length of 5 nm and a maximum horizontal length of 25 nm. These mesh sizes are chosen based on a mesh convergence study.

In the following the fabricated LOCOS structures used to verify the simulation model are described. Specifically, square silicon bumps were fabricated using the LOCOS process following steps (1)-(2) in Fig. 3(a), using both SiO_2 and Si_3N_4 as oxidation mask material. Table I shows an overview of the seven wafers oxidized in the experiment. The pad SiO_2 thickness and thickness of the SiO_2 mask layer were varied resulting in Si bumps of approximately the same height but with differing profiles. The wafers used were (100) oriented single side polished 4″ Si wafers with an electrical resistivity of 1-10 Ωcm. All thermal oxidations for the bump fabrication and simulation were performed in a wet atmosphere at a temperature of 1100 °C. Stoichiometric Si_3N_4 was deposited using a Low Pressure Vapor Deposition (LPCVD), resulting in a 50 nm thick layer on all the wafers with Si_3N_4 masks. Finally, all wafers underwent a LOCOS step with different

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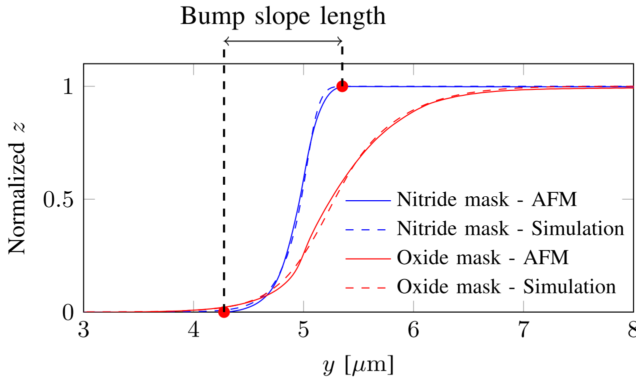

Fig. 4. Silicon bump profiles made using either an SiO_2 mask (thickness: $1\,\mu$m) or a Si_3N_4 mask with a pad SiO_2 thickness of $t_{pad} = 10$ nm. AFM measurements and simulation results are shown together. The distance between the two points, located at the positions where the slope is $< 1\%$, is denoted the slope length.

oxidation durations, in order to reach a bump height of 250 nm. Subsequently, all layers were stripped from the wafer, leaving only the Si surface and the bare silicon bumps were characterized by AFM (Dimension Icon, Bruker). The maximum relative difference between the target and measured Si bump height was found to be 6.4%, which is low enough to allow for a comparison of the profiles.

Fig. 4 shows an example of an experimental and simulated Si bump profile, for bumps fabricated using Si_3N_4 masks and SiO_2 masks. The measured and simulated profiles have been translated relative to each other along the y-axis to the position of minimum relative error. The relative errors between the measured and simulated profiles were found to be $\leq 5\%$. This consistently low error for both the Si_3N_4 and SiO_2 masks demonstrates the validity of the simulation model. Fig. 4 also shows an example of the slope length, shown in Fig. 1, of one of the profiles. The slope length is defined as the horizontal distance between the two points were the slope first becomes $< 1\%$, that is: where the profile becomes flat. The 2D AFM profiles are calculated by taking the mean of the scan lines in the direction orthogonal to the y-plane. The AFM scans consist of 512 scan lines parallel to the y-axis and each scan line is made up of 512 data points. The scan area is a $10\,\mu$m x $10\,\mu$m square and no artifacts were observed due to the relatively slowly varying slope of the profiles. The tilt of the scan is removed by fitting and subtracting a first order polynomial plane from the scan.

B. CMUT Fabrication Processes

In this section the fabrication processes for the LOCOS device (Fig. 3(a)) and RIE device (Fig. 3(b)) are presented. In the original LOCOS process by Park *et al.* [13] the first oxidation mask was a thermally grown SiO_2 layer, while in this process it is a Si_3N_4 layer. The choice of masking material becomes increasingly important as the dimensions of the CMUTs decrease as will be explained in more detail later. We used a Si_3N_4 layer as the plate, thus eliminating the need for a Silicon On Insulator (SOI) wafer, that are both more expensive and not easily attainable for thin (< 200 nm) device layers for 4″ wafers. The silicon substrate wafers have a low electrical resistivity ($< 0.025\,\Omega$cm, (100)) in order to decrease the electrical resistance in the bottom electrode.

In the LOCOS process in Fig. 3(a) step (1) a 10 nm thermal pad SiO_2 layer is grown by dry oxidation at 900 °C and 50 nm Si_3N_4 is deposited by LPCVD. The pad SiO_2 acts as a buffer layer between the tensile stressed Si_3N_4 layer and the silicon surface. Subsequently, the Si_3N_4 layer is patterned by RIE dry etching using an UV photoresist mask. In step (2) the first LOCOS is performed by wet oxidation at 1100 °C to form the Si bumps and afterwards all layers but the silicon are stripped by a buffered HF (BHF) etch and a 160 °C H_3PO_4 etch. Another pad SiO_2 is grown (dry, 900 °C) in step (3) and Si_3N_4 is deposited using LPCVD and wet etched (160 °C, H_3PO_4) using a poly-silicon etching mask. The second LOCOS (wet, 1100 °C) is performed in step (4) hereby forming the cavities. The substrate wafer is bonded, under vacuum, to a silicon wafer with a 137 nm Si_3N_4 layer constituting the plate. The bonded wafer stack is annealed at 1150 °C and the silicon handle wafer is selectively etched by KOH (28 wt%, 80 °C) using the Si_3N_4 plate layer as an etch stop layer. Furthermore, openings to the bottom electrode are dry etched and 100 nm Al is deposited by e-beam deposition and subsequently etched in a solution of $H_2O : H_3PO_4$ (1:2) at room temperature.

In the RIE process in Fig. 3(b) step (1) a thermal 225 nm SiO_2 layer is grown (wet, 1050 °C) and patterned by dry etching, forming cavities. A 27 nm Si_3N_4 layer is deposited using LPCVD, thus covering both sides of the wafer. In step (2) the cavity wafer is bonded to a silicon wafer with a 50 nm Si_3N_4 layer. All subsequent process steps are identical to the steps described for the LOCOS process, except that the Al layer thickness in this case was 50 nm.

The structures are characterized in Section III-B where the dimensions are measured using Scanning Electron Microscopy (SEM) and the mass sensitivity is determined using impedance spectroscopy.

III. RESULTS AND DISCUSSION

The mass sensitivity was in Eq. 1 shown to be dependent on the radius of the CMUT cell, where smaller radii result in higher sensitivities.

The sensitivity of a RIE CMUT is trivial to calculate as the lateral dimensions are not coupled to the vertical dimensions due to the dry etched cavities. That is, no matter the post SiO_2 height the radius will stay the same and consequently so will the sensitivity. The minimum RIE cavity radius is therefore only limited by the minimum feature size of the lithography process.

For the LOCOS device the bird's beak profile results in a coupling between the vertical and lateral dimensions which ultimately limits the radius and hereby the sensitivity. In the following section the parameters influencing the LOCOS profile and thus sensitivity are investigated through AFM measurements and simulations. Furthermore, the limited design space is investigated due to the fabrication limitations exemplified in Fig. 2. Finally, the fabricated CMUT devices are experimentally characterized.

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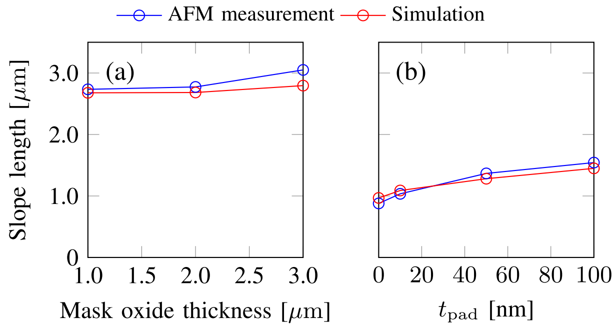

Fig. 5. (a) Slope length as a function of the SiO_2 oxidation mask thickness. (b) Slope length as a function of the pad SiO_2 thickness, under the Si_3N_4 oxidation mask. The simulations and measurements agree with a maximum relative difference of 10 %.

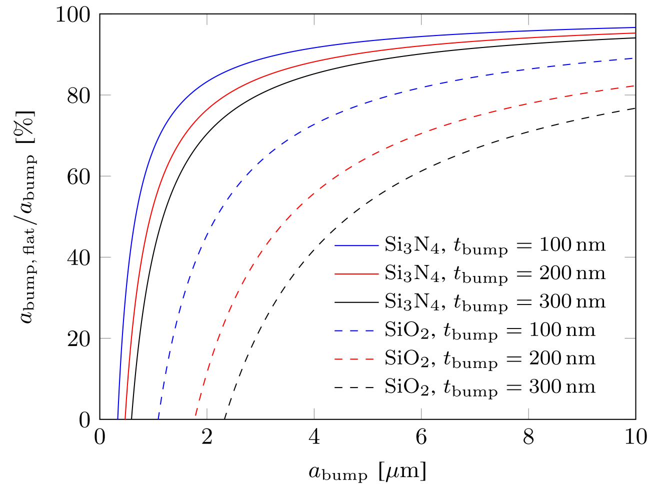

Fig. 6. Simulation results: $a_{bump, flat}$ (see Fig. 1) normalized to a_{bump} as a function of a_{bump} for Si_3N_4 (t_{pad} = 10 nm) and SiO_2 (mask height: 2 μm) as masking material at three bump heights.

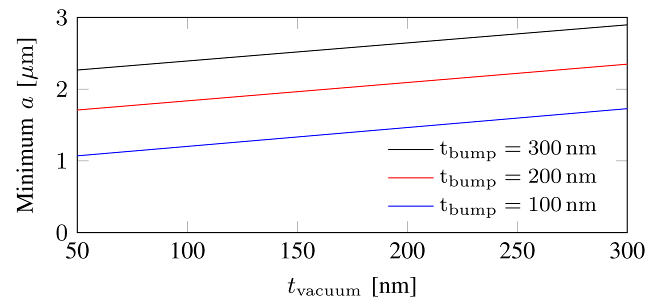

Fig. 7. Minimum cell radius as a function of the vacuum gap height for three bump heights, when $L = 0$ nm and $a_{bump,flat} = 0$ nm.

A. LOCOS Cavity Optimization

To minimize the radius of the LOCOS CMUT cell and the Si bump radius, the slope length (Fig. 1 and 4) should be minimized. Fig. 5 shows that the slope length is approximately 3 times shorter for thin pad oxides ($t_{pad} = 0$ nm to 10 nm) as compared with a SiO_2 mask to 2 times shorter for thicker pad oxides ($t_{pad} = 100$ nm). In addition, Fig. 5(a) shows that the slope length is roughly constant as a function of the thickness of the SiO_2 mask. Whereas, Fig. 5(b) demonstrates an increasing slope length for a thicker pad SiO_2, since the diffusivity of the oxidizing species (O_2 or H_2O) is higher in SiO_2 than Si_3N_4 and a thicker pad SiO_2 layer allows for a higher lateral influx of H_2O under the mask. Likewise, increased lateral diffusion is the cause for the longer slope lengths when SiO_2 is used as the masking material compared with a Si_3N_4 mask. This agrees well with what is found in the literature [14]–[16]. The measured and simulated slope lengths are in agreement with each other, showing a maximum relative error of $\leq$ 10% and demonstrating the same scaling tendencies.

When the radius of the CMUT cell decreases, the radius of the silicon bump must decrease as well and consequently the slope length of the bump will make up an increasing fraction of the total bump radius. As a result, the expected capacitance of the cell is decreased, the expected pull-in voltage is increased and wafer bonding can be rendered impossible if the slope of the bump overlaps too much with the cavity edge, as was the case in Fig. 2(b). Thus, it is important to control the bump slope length and take it into consideration when designing the CMUT. In most cases it is desirable to minimize the slope length, hereby creating the most square-like corners for the bump. Fig. 6 shows the ratio of the flat part of the bump to the bump radius as a function of the bump radius for different oxidation masking materials and bump heights. As the bump radius increases the ratio approaches 100%. The Si_3N_4 mask results in more well defined bumps with square-like corners where a larger fraction of the bump reaches the designed height. Furthermore, higher bumps lead to lower ratios and this difference is relatively larger for the SiO_2 mask. All in all this favors using a Si_3N_4 mask.

When designing bumps with radii in the sub ~ 5 μm range it can therefore be advantageous to use Si_3N_4 as the masking material. In the article by Park *et al.* [13] the masking material for the first LOCOS process was SiO_2 but it was noted that Si_3N_4 could have been used at the cost of additional process steps. Therefore, the choice of LOCOS masking material is a trade-off between tight dimension control and reducing the number of process steps.

What is the minimum radius and hence sensitivity one can achieve with a LOCOS CMUT cell? In order to answer this question two limitations are imposed on the structures: the bump and the post SiO_2 should not overlap, that is $L \geq 0$ nm (see Fig. 1) and the bump should at least reach the designed height in the center, that is $a_{bump,flat} \geq 0$ nm. The minimum radius is obtained when both of these variables are zero. Fig. 7 shows a plot of the minimum radius as a function of the vacuum gap height for three bump heights. As the vacuum gap height is increased the minimum radius increases since the post SiO_2 height increases, thus making the slope length of the post SiO_2 longer. The same effect is seen when the bump height is increased, resulting in larger minimum cavity radii. Eq. 1 shows that these minimum radii given by Fig. 7 for the LOCOS structure, directly determines the maximum sensitivity.

In order to map out the design space for LOCOS cavities, simulations were made where the post SiO_2 height and bump height have been varied. Fig. 8 shows a plot where the contour

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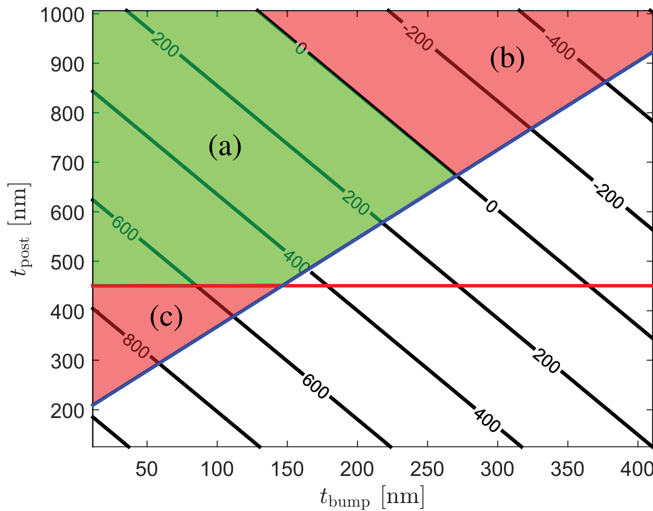

Fig. 8. Contour plot showing the length of the flat region between the cavity and bump L (see Fig. 1) as a function of the SiO_2 post thickness t_{post} and bump height t_{bump}. The red line gives the minimum required post SiO_2 height for successful bonding and the blue line are the points at which the vacuum gap height is 0 nm. The distance between the cavity and bump: $\Delta = 1.5\,\mu$m, bump and cavity Si_3N_4 thickness $t_{nitride} = 50$ nm and bump and cavity pad SiO_2 thicknesses of $t_{pad,\,bump} = 10$ nm and $t_{pad,\,cavity} = 100$ nm, respectively.

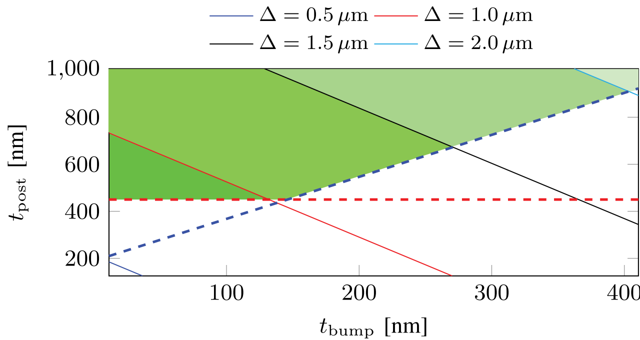

Fig. 9. The solid lines show where $L = 0$ nm and are plotted for different values of Δ as a function of t_{bump} and t_{post}. The red dashed line gives the minimum required post SiO_2 height for successful bonding and the blue dashed line are the points at which the vacuum gap height is 0 nm. Si_3N_4 thickness $t_{nitride} = 50$ nm and bump and cavity pad SiO_2 thicknesses of $t_{pad,\,bump} = 10$ nm and $t_{pad,\,cavity} = 100$ nm, respectively.

lines are the flat distance, L (see Fig. 1), between the bump and the post SiO_2 as a function of t_{post} and t_{bump}. The plot is valid for a specific set of parameters, given in the figure caption, but the overall shape of the plot is general for all LOCOS designs. The parameter Δ is the designed distance on the photolithographic mask between the bump and cavity edge and in this plot it is $\Delta = 1.5\,\mu$m. The three colored regions (a), (b) and (c) correspond to the three situations in Fig. 2. Region (a) is limited by the red line that denotes the minimum post SiO_2 height, the blue line at which the vacuum gap is zero and the $L = 0$-contour line which is the limit where the bump and post SiO_2 start to overlap. Thus, staying inside the green region (a) ensures a LOCOS design that can be successfully fabricated.

Fig. 9 shows that as the bump to cavity edge distance, Δ increases, so does the design space, here shown as green areas. The solid lines are where $L = 0$ nm, here plotted for several values of Δ. The smallest Δs are typically found for small radii cells which are here seen to be the most limited in their design space. Therefore, these design rules are especially important for these smaller radius CMUT cells, which are typical for CMUTs used for sensing, when a high mass sensitivity is wanted.

In conclusion, all variables that affect the LOCOS profile will ultimately affect the sensitivity, capacitance and pull-in voltage. Hence, being able to predict the effect on the final fabricated structure is important. The shortest slope length for the Si bump and post SiO_2 and hereby the smallest cell radii is obtained by using a Si_3N_4 mask with a thin pad SiO_2 (t_{pad}) and choosing a low Si bump height and a small vacuum gap, since this yields the lowest post SiO_2 height. The pad SiO_2 thickness for the first LOCOS step can be made thin as these layers are subsequently stripped. However, the pad SiO_2 thickness for the second LOCOS step is sometimes determined by the requirement for the CMUT cell to prevent electrical breakdown if pull-in occurs. Finally, the design space of LOCOS cavities were investigated and it was shown that for high sensitivity, small radii cavities the design space is limited.

B. CMUT Sensors

Two CMUT devices have been fabricated: a LOCOS and a RIE device, following the process flows in Fig. 3. The design of the LOCOS CMUT utilized the findings above to minimize the slope lengths of the bump and post SiO_2. Namely, using Si_3N_4 as masking material in both LOCOS steps and having a pad SiO_2 thickness of only 10 nm. Furthermore, the vacuum gap is just 65 nm, resulting in a relatively low post SiO_2 height, hereby shortening the post SiO_2 slope length further. The RIE device has an insulation Si_3N_4 layer which both increases the breakdown voltage when in pull-in and prevents potential leakage currents from running during operation. The choice of a Si_3N_4 plate for this device results in a wafer bonding interface between two Si_3N_4 surfaces; two materials that empirically are more difficult to bond than e.g. Si-SiO_2 or Si_3N_4-SiO_2. The bonding strength is increased between the two Si_3N_4 surfaces by oxidizing the Si_3N_4 surfaces at a high temperature in a wet atmosphere, hereby creating a thin layer of oxy-Si_3N_4 [20].

Two SEM cross-sections of the devices can be seen in Fig. 10. Fig. 10(a) shows a RIE cell with a well-defined vertical post SiO_2 cavity edge. Fig. 10(b) shows the LOCOS cell with the central Si bump and (c) is a zoom in on the bird's beak profile at the cavity edge. The Si_3N_4 layer is seen to end well below the bonding surface. The cracked surface is the result of a sputtered Au layer which was applied in order to prevent charge build up during imaging. The dimensions of the two cells are shown in Table II, where the thickness of the Au layer has been subtracted from the measured plate thickness. The Si bump is misaligned relative to the cavity and is therefore not placed completely centered in the cavity which highlights one of the challenges of making the cavities smaller, namely the increasing alignment tolerances. Indeed, if the Si bump is misaligned so much that it overlaps with the post SiO_2, bonding can be hindered which is exemplified

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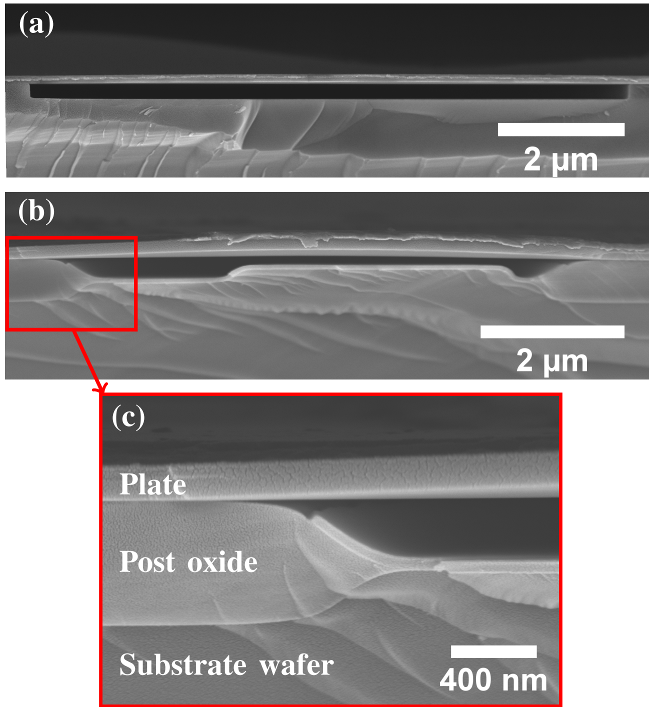

Fig. 10. Scanning electron microscope images of cross-sections of a single CMUT cell for (a) the RIE device, (b) the LOCOS device and (c) zoom in at the bird's beak.

TABLE II

MEASURED DIMENSIONS AND PROPERTIES OF THE LOCOS AND RIE DEVICES

Dimension	**Unit**	**LOCOS**	**RIE**
Plate thickness	[nm]	137	51
Vacuum gap height	[nm]	65	235
Post SiO_2 thickness	[nm]	582	235
Bump height	[nm]	180	-
Pad SiO_2	[nm]	10	-
Cavity Si_3N_4	[nm]	50	27
Plate radius	[μm]	3.75	5.0
Pull-in voltage	[V]	45	91

in Fig. 2(b). Comparing the LOCOS and RIE device it is evident how the sloped part of the LOCOS device makes up a significant part of the total cavity area while the RIE device in unaffected by this.

The sensitivity of the devices can be calculated using Eq. 1 but the sensitivity can also be measured directly by measuring the resonance frequency shift when a known mass is added to the plate. In order for the CMUT to stay in the linear regime the inequality $m_{added} \ll m_{plate}$ must not be violated. The sensitivity was measured by depositing thin (< 10 nm) layers of Au directly on the plate. The resonance frequencies were determined from the position of the resonance peak in the impedance spectra which were measured after each Au deposition. The impedance was measured with an impedance analyzer (E4990A, Keysight) actuating the CMUTs with a 50 mV AC signal while the CMUTs are biased by an external voltage supply (2410 SourceMeter, Keithley) coupled to the CMUT through a bias-T. The pull-in voltage was found for both CMUT devices using this setup and increasing the bias voltage until the resonance peak disappears, see Table II. The added mass was determined by measuring the step height of the Au layer using an AFM and calculating the mass based on the area of the plate and Au density. A plot of the resonance frequency as a function of mass added to the plate is given in Fig. 11 for both the LOCOS and RIE device. The experimental sensitivity is estimated by calculating the slope of the lines in the figure by linear regression. Table III lists the theoretical (Eq. 1) and experimental sensitivities for the two devices. For both the LOCOS and RIE device the experimental sensitivities are lower than the theoretical values which is due to the linearity assumption being broken. Table III states the fraction m_{Au}/m_{plate} for both devices, showing that the assumption is indeed broken. Furthermore, the flexural rigidity and mass of the added Au layer becomes non-negligible compared with that of the plate itself, which also decreases the experimental sensitivity compared with the theoretical one. The relative difference between the theoretical and experimental sensitivity is greater for the RIE device than the LOCOS device since the relative added mass is larger. The decrease in sensitivity between the mass loaded and unloaded case is studied with a simple Finite Element Method (FEM) model and the relative differences for the LOCOS and RIE devices are seen to agree. Nonetheless, both the theoretical and experimental sensitivity values, for both devices, are to the best of our knowledge the highest published for CMUTs.

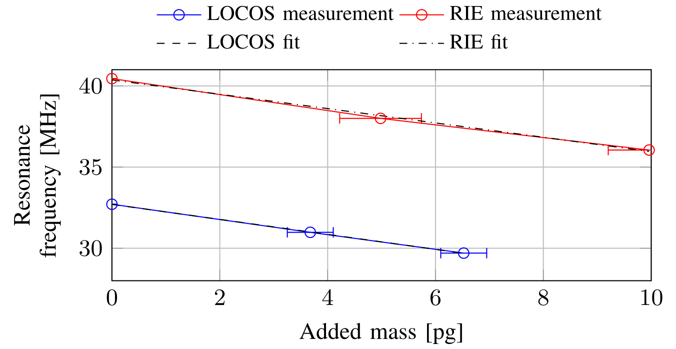

Fig. 11. Resonance frequency as a function of mass added on the plate for the LOCOS and RIE devices. The slopes of the two linear fits are the respective sensitivities. The error bars correspond to an estimated uncertainty of the Au thickness of 0.5 nm from the measurement itself and spatial nonuniformity of the sputtering process.

TABLE III

ABSOLUTE AND NORMALIZED THEORETICAL AND EXPERIMENTAL SENSITIVITIES AND RELATIVE ADDED MASS ON THE LOCOS AND RIE DEVICES. IN ADDITION, S_{theo} AND S_{exp} ARE COMPARED ALONG WITH SENSITIVTIES CALCULATED IN A FEM MODEL

	LOCOS	**RIE**	Unit
S_{theo}	0.74	0.84	Hz/ag
S_{exp}	0.46	0.44	Hz/ag
$S_{theo,\,norm}$	32.7	66.0	$\frac{Hz \cdot \mu m^2}{ag}$
$S_{exp,\,norm}$	20.3	34.6	$\frac{Hz \cdot \mu m^2}{ag}$
m_{Au}/m_{plate}	25	43	%
$1 - S_{exp}/S_{theo}$	38	48	%
$1 - S_{FEM,\,loaded}/S_{FEM,\,unloaded}$	28	48	%

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IV. Conclusion

The minimization of wafer bonded CMUT cells was studied through a numerical process simulation model whose results were compared to AFM measurements of fabricated structures, giving a relative error of $\leq 5\%$. The smallest radius one can achieve using the LOCOS cavities is by using Si_3N_4 as the masking material which result in slope lengths that are 2 to 3 times shorter than using a SiO_2 mask. Further, the pad SiO_2 thickness should be decreased as well as the bump height. Lastly, it was demonstrated how the design space becomes increasingly limited for decreasing cavity dimensions.

CMUT senors were fabricated by the LOCOS and RIE processes and their mass sensitivities were both calculated and measured. The LOCOS CMUT device was designed using the findings from the simulation model while the RIE device was fabricated using Si_3N_4 to Si_3N_4 wafer bonding. The LOCOS and RIE devices both showed a high experimental mass sensitivity of $0.46\,\mathrm{Hz/ag}$ and $0.44\,\mathrm{Hz/ag}$, respectively, which for CMUTs, to our knowledge, are the highest mass sensitivities published.

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