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Published in: Proceedings of The 2018 International Power Electronics Conference

Link to article, DOI: 10.23919/IPEC.2018.8506666

Publication date: 2018

Document Version Peer reviewed version

Link back to DTU Orbit

Citation (APA): Thummala, P., Yelaverthi, D. B., Zane, R., Ouyang, Z., & Andersen, M. A. E. (2018). A 10 MHz GaNFET Based Isolated High Step-Down DC-DC Converter. In Proceedings of The 2018 International Power Electronics Conference (pp. 4066-4073). IEEE. DOI: 10.23919/IPEC.2018.8506666

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A 10 MHz GaNFET Based Isolated High Step-Down DC-DC Converter

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Abstract— This paper presents design of an isolated high-step-down DC-DC converter based on a class-DE power stage, operating at a 10 MHz switching frequency using enhancement mode Gallium Nitride (GaN) transistors. The converter operating principles are discussed, and the power stage design rated for 20 W is presented for a stepdown from 200-300 V to 0-28 V. Commercially available magnetic materials were explored and the high-frequency (HF) resonant inductor and transformer designs using a low-loss Fair-Rite type 67 material are presented. Finite element simulations have been performed to estimate the AC resistances of magnetics at 10 MHz. Experimental results are presented at 12 W, 254 V to 22 V on a laboratory prototype operating at 10 MHz. At 20 W the experimental prototype achieved an efficiency of 85.2%.

Keywords— DC-DC conversion, Gallium Nitride, High frequency, Resonant conversion, Soft switching, Class-DE

I. INTRODUCTION

The motivation to operate at high switching frequency is not just to reduce the size of passive components but also to provide very fast dynamic load response. Most RF communication systems use power amplifiers (PA) to convert low-power signals into larger power RF signals for driving the antenna of a specific transmitter. The majority of PA designs utilize switched-mode pulsewidth-modulating (PWM) converters as the power source to operate RF amplifiers. Envelope tracking PAs use dynamically changing supply voltage to achieve high efficiency for the PA over the full power range. To achieve successful envelope tracking, the power supply must be capable of switching at frequencies greater than 5 MHz, as most modern RF waveforms observe a bandwidth of 1 to 5 MHz [1], [2].

The envelope tracking power supply considered in this paper has to operate with an input voltage range of 200 V to 300 V at 10 MHz switching frequency. Several designs at 10 MHz switching are reported in literature for different applications. A 10-MHz GaN 16 to 34-V boost converter with above 90% efficiency is presented in [3]. A 94% efficient 10-MHz, 100 W buck-boost type DC-DC converter is studied in [4]. A 10 MHz, 10.8-16 V to 0.65-2 V, 2 A multiphase buck converter is implemented in [5]. A 10-MHz, 12 V to 5 V, 5 W buck converter is investigated in [6]. All of these designs are at low operating voltage (few tens of volts).

Traditional hard switching switched-mode power supply (SMPS) topologies are extremely lossy at such high frequencies. This has led to the development of resonant soft-switching converters. With the emergence of Gallium Nitride (GaN) based power switches, power electronic converters tend to be even faster, smaller and more efficient [7]. Resonant converters are often designed in two parts; an inverter converting the DC input voltage to an AC current and a rectifier converting the AC current to a DC output voltage. The two parts are designed individually, but the design of the inverter depends on the input impedance of the rectifier [8], [9].

The most common topologies for the inverter part are based on class E, which could either be a class E, a class EF2 (φ 2), a resonant SEPIC or a resonant boost converter. The choice of the topology is based on the complexity and losses associated with a high side gate drive for operation in the HF range. A class E derived inverter imposes significant voltage stress across the MOSFET. The voltage stress for the class E, the resonant SEPIC and resonant boost is 3.6 times the input voltage with a duty cycle of 50%, and for the class EF2 this stress is reduced to approximately 2.3-3 times. The semiconductor switches in the class DE inverter are directly connected to the input and the voltage across them is limited to the input voltage. The class DE inverter [10]-[12] has two other great advantages over the other topologies. Firstly, it only requires a single inductor. Secondly, due to the lower peak voltage across the MOSFET, the stored energy is approximately ten times lower.

This paper presents a GaN-based and magnetic corebased 10 MHz isolated DC-DC converter using a Class-DE resonant soft-switching power stage. Section II describes the converter design, operation and simulation results. Section III provides the steady state analysis of the converter. Section IV discusses the choice of magnetics at 10 MHz, and the design of inductor and the transformer using Fair-Rite 67 material. Section V provides the experimental results, and Section VI discusses the power loss distribution, followed by the conclusions in Section VII.

II. CONVERTER ANALYSIS AND DESIGN

A class-DE based isolated DC-DC converter is depicted in Fig. 1. The main input power stage consists of switches S_1 and S_2 . Compared to the conventional Class-DE amplifiers, the switches S_3 and S_4 are connected in parallel with the rectifier diodes D_3 and D_4 , to achieve synchronous rectification and also for active rectification to control the output voltage and power. The converter achieves ZVS, zero voltage derivative switching (ZVDS), and ZCS at the turn-on instant. In this converter, the effective impedance of the secondary rectifier is used for designing the series resonant tank components C_r and L_r . A transformer with a turns ratio n:1 is used for providing isolation as well as stepping down the input voltage. The power is transferred from input to output due to the resonance between the resonant tank elements C_r and L_r . Hence, the current flowing through the resonant tank is almost sinusoidal in shape. Based on the fundamental harmonic approximation (FHA), the ac-equivalent circuit of the proposed Class-DE DC-DC converter is shown in Fig. 2.



Fig. 1. Schematic of the Class-DE based isolated synchronous DC-DC converter.



Fig. 2. AC equivalent circuit of the resonant tank based on FHA.

The design equations of the proposed isolated class-DE topology are given below. The AC equivalent load resistance (input resistance of the rectifier) is calculated as [10]

$$R_{ac} = \frac{2R_L n^2}{\pi \left[\pi + \omega R_L C_{\text{oss,sec}}\right]} \,. \tag{1}$$

The RMS voltages on both inverter and rectifier sides of switched-nodes are given by (assuming trapezoidal waveforms) [12]

$$V_{a,rms} = V_{in} \sqrt{\frac{D_{pri} + 1}{3}}$$
, (2)

$$V_{b,rms} = V_{out} n \sqrt{\frac{D_{sec} + 1}{3}} \quad . \tag{3}$$

The reactance of the resonant circuit is calculated as [13]

$$Z_1 = R_{ac} \sqrt{\left(\frac{V_{a,rms}}{V_{b,rms}}\right)^2 - 1} \quad . \tag{4}$$

The resonant tank inductance for a given tank capacitance is given by [14]

$$L_r = \frac{C_r Z_1 \omega + 1}{C_r \omega^2}, \quad \omega = 2\pi f_{sw} \quad . \tag{5}$$

The quality factor of the resonant tank is given by

$$Q = \frac{1}{R_{ac}} \sqrt{\frac{L_r}{C_r}} \quad . \tag{6}$$

In the above equations, R_L is the load resistance, n is the transformer turns ratio, D_{pri} is the duty cycle of the primary GaNFETs, D_{sec} is the duty cycle of the secondary GaNFETs, f_{sw} is the switching frequency, and $C_{oss,sec}$ is the output capacitance of the secondary GaNFETs S_3 and S_4 .

A transformer turns ratio of n = 2.5 is selected to ensure both ZVS of the primary GaNFETs as well as low circulating energy of the resonant tank. An LTspice simulation of the Class-DE converter is performed using the GaNFET models from the manufacturer. On the primary and secondary sides, 650 V devices from GaN Systems (GS66502B) and 40 V GaNFET from EPC (EPC2014C) are used, respectively. The simulation results showing key waveforms are provided in Fig. 3. The primary GaNFETs from GaN Systems are driven with 6 V and the secondary GaNFETs from EPC are driven with 5 V.



Fig. 3. LTSpice simulation results for $V_{in} = 300$ V at $D_{pri} = 18\%$ and $D_{sec}=40\%$. The output power $P_{out} = 20$ W. Power stage design parameters given in Table I are used in the simulation. A phase shift of 22 ns between primary and secondary GaNFETs is used.

TABLE I: POWER STAGE DESIGN			
Variable	Value		
R_{ac}	49.63 Ω		
Z_1	162.2 Ω		
C_r	1 nF		
L_r	2.8 μH		
L_m	2.2 μΗ		
Z_2	36.52 Ω		
Q	1.24		

The design of the converter at 10 MHz for 300 V input and 28 V output at 20 W is summarized in Table I. The magnetic design details are provided in Section IV.

III. STEADY STATE ANALYSIS OF CLASS-DE DC-DC CONVERTER

The fundamental components of the input and output voltages of the resonant tank are given by

$$V_a(t) = \frac{2V_{in}}{\pi} \sin(\omega t) , \qquad (7)$$

$$V_{t1}(t) = \frac{2nV_{out}}{\pi} \sin(\omega t) . \qquad (8)$$

The voltage gain of the resonant tank is given as follows:

$$M = \frac{V_{t1}(t)}{V_{a}(t)} = \frac{nV_{out}}{V_{in}} = \frac{Z_{2}}{Z_{1} + Z_{2}}$$
$$= \frac{k}{\sqrt{\left(1 + k - \frac{1}{f_{n}^{2}}\right)^{2} + Q^{2}k^{2}\left(f_{n} - \frac{1}{f_{n}}\right)^{2}}}, \quad (9)$$
where $k = \frac{L_{m}}{L_{r}}, f_{r} = \frac{1}{2\pi\sqrt{L_{r}C_{r}}}, f_{n} = \frac{f_{sw}}{f_{r}}.$

The voltage gain of the resonant tank M is plotted in Fig. 4 with respect to the normalized frequency and the quality factor for a given constant k. Similarly, the voltage gain of the resonant tank M is plotted with respect to the normalized frequency and the constant k, for a given quality factor, as shown in the Fig. 5. For the converter design specifications described in Section II, k = 0.786, $f_r = 3$ MHz, and $f_n = 3.33$.



Fig. 4. Voltage gain vs. loaded quality factor vs. normalized switching frequency for k = 0.786.

The converter is operating well above the resonance frequency so that current is lagging enough to achieve ZVS for the primary GaN devices. The k-Q analysis of the resonant tank for an LLC series-resonant converter (SRC) is proposed in [15]. The following condition ensures that the converter operates within LLC-SRC region [15]



Fig. 5. Voltage gain vs. constant-*k* vs. normalized switching frequency for Q = 1.24.



Fig. 6. Steady-state waveforms of the proposed resonant DC-DC converter.

$$Q \le \sqrt{\frac{L_r}{L_m}} \le \frac{1}{\sqrt{k}} \ . \tag{10}$$

The steady state waveforms of the proposed DC-DC converter are shown in Fig. 6. The gate drive waveforms of the four primary and secondary GaNFETs, the voltages across the GaNFETs S_2 and S_4 , and the secondary resonant tank current are clearly shown in Fig. 6. The switching frequency of the converter is fixed at 10 MHz.

The output power of the converter is defined as [10], [16]

$$P_{out} = \left(\frac{nI_{pk}\cos\left(\Delta\phi_{s}\right)}{\pi + \omega R_{L}C_{oss,sec}}\right)^{2} R_{L} .$$
(11)

The output current is given by the following expression

$$I_o = \frac{nI_{pk}\cos(\Delta\phi_s)}{\pi + \omega R_L C_{oss,sec}} .$$
(12)

The phase shift $\Delta \phi$ is given by

$$\Delta \phi = \left(\Phi_{P-S} - \Phi_{DTS} \right) - \left(\phi_0 - \Phi_{DTP} \right) , \qquad (13)$$

where I_{pk} is the peak resonant tank current, Φ_{P-S} is the phase-shift between primary GaNFET S_1 (or S_2) and

secondary GaNFET S_3 (or S_4), Φ_{DTS} is the phase corresponding to the dead-time of the secondary side, Φ_{DTP} is the phase corresponding to the dead-time of the primary side, and ϕ_0 is the phase-shift of the resonant current. The output power and voltage can be controlled by varying the phase-shift angle Φ_{P-S} between the primary and secondary GaNFETs. The variations of output voltage and output power with respect to the phase-shift Φ_{P-S} are shown in Fig. 7. The maximum output power occurs at a phase-shift of 15 ns for $V_{in} = 254$ V.



Fig. 7. The variation of output voltage and output power with respect to the phase-shift Φ_{P-S} for $V_{in} = 254$ V, $R_L = 40 \Omega$.

IV. DESIGN AND FEM SIMULATIONS OF MAGNETICS

A. Inductor and Transformer designs

With the emergence of GaN and SiC devices, there has been a significant advancement in semiconductor device switching speed, but magnetics has become a primary limitation constraining miniaturization. By increasing the switching frequency of the converter, the absolute value of capacitance and inductance can be reduced but the actual size reduction at very high frequencies depends on the allowable loss in power density. Appropriate core material and winding structure have to be selected for these high frequencies to reduce the loss and realize the achievable miniaturization. Emerging thin-film magnetic materials are a good choice for frequencies greater than 10 MHz. These materials are typically alloys with Fe, Co and Ni. But these are not commercially available at economical costs [17], [18]. Another limitation is the conductor technology. The performance factor comparisons of magnetic materials at high frequency is reported in [19] @ 500 mW/cc.

There is limited data available on the design of very high frequency power magnetics. Power magnetics have high flux drive. For most of the materials, large signal loss data are not available at above a few MHz. Among the commercially available materials, Ni-Zn ferrites and metal-powder materials, which are developed for RF applications, have very high resistivity and are suitable for the present application. The performance factor for these RF material in range of 1 MHz to 100 MHz are reported in [19] based on the method proposed in [20]. Performance factor is the product of amplitude of flux density (B_{ac}) and frequency (f) and is a measure of power handling capability per unit volume for a given core loss density and is a relevant performance metric when core

loss is the major design constraint (usually true for transformers and resonant inductors), neglecting ac winding loss. Among the above reported materials, Ferroxcube 4F1 [21] and Fair-Rite 67 [22] material were available in planar structures and rest were available in rods and toroidal shapes meant for RF applications. The 67 material also has the highest performance factor at 10 MHz [19].

For both Ferroxcube 4F1 and Fair-Rite 67 material, coreloss is plotted in Fig. 8 from raw data for 10 MHz at 25° C and 100° C (sinusoidal current assumed through the inductor). The core loss density of 67 material is 390 mW/cm³ at 10 MHz, T=100° C for B_{ac} of 10 mT, and is nearly a third of what it is for 4F1. Because of the relatively high thermal coefficient of the 4F1, it is not a good option for fabricating a resonant inductor with low air-gap designs. For the initial prototype, 67 material was chosen as the core option for the above reasons. However, a drawback of the 67 material is that when it is exposed to B_{ac} of greater than 20 mT the material properties irreversibly change and have higher losses than the initial characteristics. Permeability of both the material at 25° C and 100° C is given in Table II. The inductor and transformer prototypes are shown in Fig. 9. The inductor and transformer designs are summarized in Tables III and IV, respectively.



Fig. 8. 4F1 and 67 core loss density comparison at 10 MHz and for different temperatures.

A 4-layer PCB (total thickness is 1.575 mm) with 1 oz. copper thickness is used for practical implementation. To maintain the ease of manufacture and also high repeatability, multi-layered PCBs are used to realize the magnetic winding structures, 6-layer PCB for the inductor with and 8-layer PCB for the transformer. For the inductor, the copper thickness in all layers is 35 µm, and the 3rd and 4th layers are parallel connected. In the transformer, the 5 primary turns are placed in the first 5 layers, the 6th layer in the PCB is kept empty, and the 2 secondary turns are placed in 7th and 8th layers, respectively. Providing an empty 6th layer not only provides isolation between the primary and secondary windings, but it also minimizes the inter-winding capacitance. In Tables III and IV, the measured AC resistance values are used to calculate the winding loss.

TABLE II: 4F1 AND 67 PERMEABILITY WITH TEMPERATURE

Material	Permeability @ T=25° C	Permeability @ T=100° C	
4F1	80	140	
67	40	45	



Fig. 9. A photo of inductor and transformer PCB winding prototypes.

TABLE III: INDUCTOR DESIGN SUMMARY					
Para	meter	Value			
Induc	ctance	2.8 μH			
C	vre	EEQ20, 67 material,			
	sie	Volume= 2.01 cm^3 , Area = 0.6 cm^2			
Overall c	ore height	12.7 mm			
Effective	core length	3.33 cm			
Turns,	Air-gap	5 turns, No Air-gap			
Core loss	@ 20 W	$0.68 \text{ W} (@B_{ac} = 11.2 \text{ mT})$			
0000 1055	@ 12 W	0.46 W (@ $B_{ac} = 9.3 \text{ mT}$)			
Conner loss	@ 20 W	0.16 W (for <i>I</i> _{rms} =0.831 A)			
Copper loss	@ 12 W	0.11 W (for <i>I_{rms}</i> =0.683 A)			
AC resistance	e @ 10 MHz	231 mΩ			
Coppert	thickness	35 μm (in all layers)			
D	מר	6 layer (layers 3 and 4 are paralleled)			
P	Ъ	Total PCB thickness = 1.75 mm			
PCB thickness	between layers	0.254 mm			
{1-2, 3-4	, and 5-6}	0.254 mm			
PCB thickness	between layers	0.38 mm			
{2-3 ai	nd 4-5}	0.58 mm			
TA	ABLE IV: TRANSFO	RMER DESIGN SUMMARY			
Para	ameter	Value			
Transform	nation ratio n	2.5			
Primary magnetizing inductance		2.18 µH			
		EIQ13, 67 material,			
(lore	Volume= 0.28 cm^3 , Area = 0.2 cm^2			
Overall core height		3.95 mm			
Effective core length		1.39 cm			
Turns		5 turns primary,			
Non-interleaved: PPPPPSS		2 turns secondary			
Core loss	@ 20 W	0.055 W (@ $B_{ac} = 8.7 \text{ mT}$)			
Core loss	@ 12 W	0.038 W (@ $B_{ac} = 7.3 \text{ mT}$)			
Connor loss	@ 20 W	0.265 W (for <i>I_{rms}</i> =0.831 A)			
Copper loss	@ 12 W	0.18 W (for <i>I_{rms}</i> =0.683 A)			
AC resistance referred to primary		385 mΩ			
@ 10 MHz					
Copper thickness		$35 \ \mu m$ (in top and bottom layers)			
Соррег	unexiless	17.5 µm (in all middle layers)			
РСВ		8 layers, layer 6 is not used			
		Total PCB thickness = 2 mm			
PCB thickness between layers		0.254 mm			
{1-2, 3-4, 5-6, and 7-8}					
PCB thickness between layers		0.257 mm			
{2-3, 4-5, and 6-7}					

Analytical analysis was done for estimating the AC resistance and optimal copper thickness to minimize the losses in both the transformer and inductor PCB windings. However, a more detailed FEM analysis is required for operation at 10 MHz to improve the design due to the importance of parasitic effects from aspects such as PCB traces and vias.

B. FEM simulations

Maxwell's 3D simulations have been performed to estimate the AC resistance and leakage inductance of magnetics at 10 MHz. The FEA simulation results of the transformer current density and flux density at 10 MHz are shown in Figs. 10(a) and 10(b). The skin depth of copper at 10 MHz is 20.6 μ m. A fine mesh based on inside length selection is used to simulate the eddy current effects in the winding. In the primary and secondary windings, the layer to layer connections are made through the vias with an outer diameter of 0.45 mm and the size of the hole is 0.2 mm. In the transformer 3D simulation model, the vias are placed between 2 layers (layer-to-layer).





Fig. 10. Plots from the 3D Maxwell simulations of EIQ-13 transformer (a) Current density at 10 MHz; (b) Magnetic flux density at 10 MHz. Secondary winding is shorted to obtain the AC resistance and leakage inductance.

The parameters of the transformer are measured using the Agilent 4294A impedance analyzer. The measurement results are shown in Figs. 11-14.



Fig. 11. Measured AC resistance and leakage inductance of the transformer using Agilent 4294A analyzer.

From Fig. 12, the resonance frequency of the transformer is 48.5 MHz, and the primary magnetizing inductance of the transformer at 10 MHz is 2.18μ H as

shown in Fig. 13, which results in a primary transformer self-capacitance of 4.95 pF. The measured interwinding capacitance of the transformer as shown in Fig. 14 is 8.99 pF at 10 MHz. It is obtained by shorting the primary and secondary windings, and measuring the capacitance across the shorted primary and secondary windings.





A comparison of the simulated and measured parameters of the transformer is provided in Table V. The simulated and measured transformer parameters show a close match, with the largest error in the AC resistance. The simulation model of PCB vias can be further improved to match with practical values at 10 MHz switching frequency.

TABLE V: COMPARISON OF SIMULATED AND MEASURED TRANSFORMER PARAMETERS AT 10 MHz

Variable	Simulation	Measurement
Primary magnetizing inductance	2.17 μH	2.18 μH
AC resistance	300 mΩ	385 mΩ
Leakage inductance	188 nH	194 nH
DC resistance	40 mΩ	45 mΩ



Fig. 15. Plots from the 3D simulations of EEQ-20 inductor (a) Current density at 10 MHz; (a) Current density top view at 10 MHz; (c) Magnetic flux density at 10 MHz.

The FEA simulation results of the inductor current density and flux density at 10 MHz are shown in Figs.

15(a), 15(b) and 15(c), respectively. As shown in Fig. 15(b), the current is pushed towards the edges of the winding. In the inductor 3D simulation model, the vias pass through all layers (top-layer to bottom-layer). The measured parameters of the inductor using the impedance analyzer are shown in Fig. 16.



Fig. 16. Measured AC resistance and inductance of the EEQ-20 inductor using Agilent 4294A analyzer.

A comparison of the simulated and measured inductance and AC resistances of the inductor is provided in Table VI. Again, a close match is achieved with the largest error in the AC resistance. The error is primarily due to differences in how the vias are modeled. In the practical implementation of magnetics, the vias are connected from top layer to bottom layer in the PCBs.

TABLE VI: COMPARISON OF SIMULATED AND MEASURED INDUCTOR

PARAMETERS AT 10 MHZ				
Variable	Simulation	Measurement		
Inductance	2.89 µH	2.69 µH		
AC resistance	131 mΩ	231 mΩ		
DC resistance	37.5 mΩ	40 mΩ		

V. EXPERIMENTAL RESULTS

An experimental prototype of the Class-DE based converter is shown in Fig. 17. The resonant converter is operated along a narrow optimized trajectory to guarantee ZVS and ZCS. Inductance and noise coupling in the gate drive loop is critical for operation at high input voltages. For the practical implementation, primary 650 V, 220 m Ω GS66502B GaNFETs with low output capacitance (17 pF) and gate charge (1.7 nC) are used. For synchronous rectification, 40 V, 60 m Ω EPC2014C GaNFETs (C_{oss} = 150 pF, Q_g = 2 nC) are used in the secondary side. A HF diode PMEG6010CEH is used for D_3 and D_4 . The experimental results are provided in Figs. 18 and 19.

High-frequency resonant capacitors from ATC are used for C_r , C_1 and C_2 . A 1000 V, 1 nF capacitor (100C102JW) is used for C_r [23]. A 100 V, 684 nF capacitor (900C684MP) is used for C_1 and C_2 [24]. A digital isolator ADuM210N with common mode transient immunity (CMTI) \geq 100 V/µs is used for isolation. Due to non-availability of commercially available half-bridge gate drivers suitable for 300 V input and 10 MHz operation, and to quickly evaluate the power stage design, a battery powered isolated low-side gate driver LM5114 [25] is used for driving each GaNFET. All gatedrivers for switches S_1 - S_4 have been designed with a negative-bias supply (-2 or -3 V) to prevent false turn-on. Negative bias voltage in switch S_2 can be seen from Fig. 18. Independent gate drive resistors $R_{g,ON}$ (20 Ω) and $R_{g,OFF}$ (3.3 Ω) are used to counter Miller effect on primary side. The inductance and noise coupling in gate drive loop are very critical for operation of converter at 10 MHz. A Virtex-5 FPGA development board is used to generate the required 10 MHz driving signals on both primary and secondary sides.



Fig. 17. An experimental prototype of the Class-DE based converter. The 10 MHz switching power stage is outlined in yellow. The rest of the PCB has connectors to the FPGA board, digital isolators, test points and auxiliary supplies for gate drivers.



Fig. 18. Experimental waveforms for V_{in} =254 V, Phase-shift Φ_{P-S} =25 ns, D_{pri} =18%. CH1: Gate-to-source signal of S_2 [5 V/div]; CH2: Drainto-source waveform of S_2 [50 V/div]; CH3: Output voltage across 40 Ω load [12.5 V/div].



Fig. 19. Experimental waveforms for V_{in} =254 V, Phase-shift Φ_{P-S} =25 ns, D_{pri} =18%. CH1: Resonant tank current [2 A/div] (dark blue); CH2: Resonant tank voltage [50 V/div] (light blue).

VI. POWER LOSS BREAKDOWN

The total loss breakdown for the proposed DC-DC converter at rated power is shown in Fig. 20. The driving loss is the total gate drive loss for both primary and secondary GaNFETs. The device losses include the total forward and reverse conduction loss, and switching loss due to all primary and secondary GaNFETs. The loss due to the power consumption in the auxiliary power supply

is estimated to be 1 W, the loss due to the ESR of the capacitors, and PCB traces are considered as additional conduction losses. The efficiency of the converter at an output power of 20.2 W is 85.27%. The total power loss is 3.49 W. Optimizing the inductor and auxiliary power supply (for powering the gate drivers) designs could further increase the efficiency of the converter. Integrating the transformer and inductor into a single magnetic structure will reduce the overall size of the magnetics. This also reduces the terminations by two and reduces the copper loss due to reduced number of windings. Winding resistance can be reduced by paralleling multiple layers in planar PCB windings. The power stage and magnetic designs can be further investigated by changing the constant-k described in Section III.



Fig. 20. Total loss breakdown for an output power P_{out} =20.2 W.

VII. CONCLUSIONS

In this paper, a high-frequency, high-step down isolated DC-DC converter equipped with the GaN devices is analyzed and designed. The proposed resonant design shapes waveforms to optimize magnetics and achieve low EMI and high efficiency with high power density. The inductor and transformer are designed using commercially available materials to minimize the physical size and core and copper losses when operating at a switching frequency of 10 MHz. The core material Fair-Rite 67 was chosen from many of the commercially available magnetic materials because of its better performance factors and its availability in low-profile planar structures. Maxwell 3D simulations were performed to estimate the AC resistances of the inductor and transformer at 10 MHz. A phase shift angle between the primary and secondary GaNFETs was used to regulate the output voltage and power of the DC-DC converter. A 20 W, 300 V to 28 V laboratory prototype operating at 10 MHz achieved an efficiency of 85.2%.

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