

# Modular Multilevel Converter with Partially Rated Integrated Energy Storage Suitable For Frequency Support and Ancillary Service Provision

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**Abstract**—Grid scale Energy Storage Systems (ESSs) have received significant interest in recent years due to their ability to reduce/defer investment in transmission/distribution networks, as well their ability to act as primary reserve sources and provide emergency support to the transmission system. This paper investigates the dual-purposing of a HVDC-Scale Modular Multilevel Converter (MMC), allowing it to also act as an ESS. This has potential application in primary frequency response provision and other services such as de-coupled power oscillation damping. In the proposed topology a certain percentage of sub-modules (SM) within the MMC have their capacitor interfaced through a DC-DC converter to an Energy Storage Element (ESE), formed of a battery or ultracapacitor. By applying appropriate control, energy can be exchanged from the ESE to the main SM capacitor of each ESE-SM, and from there to either the AC or DC bus. It was found that for some operating points, an injection of circulating current was required to facilitate exchanging energy with the ESE-SMs. Analysis shows that, for instance, an additional power injection to AC or DC terminal of 0.1 p.u. (10%) is possible with only 4% of the SMs replaced by Full-Bridge ESE-SMs, and no additional SMs added.

## I. INTRODUCTION

MULTI megawatt grid-scale Energy Storage Systems (ESS), in particular those using batteries as the storage technology (BESS), have typically been used for asset deferral applications, using bulk energy storage to provide peak load shaving, allowing transmission system upgrades to be delayed [1]–[3]. More recent applications for ESSs have included operational services such as primary and secondary reserve provision, and enhanced frequency response (EFR) [4]–[6]. These services require lower overall energy storage capabilities than the reinforcement deferral applications, and so other ESSs that use storage technologies such as ultracapacitors (UC) have been proposed for these applications [7].

Recent works [8]–[15] have looked at adapting modular converter topologies for ESS applications, with most focus placed on the Cascaded H-Bridge Converter (CHB), and the Modular Multilevel Converter (MMC). Modular converter topologies have the advantage of allowing the energy storage elements (ESEs) to be distributed within each sub-module (SM) of the converter. This allows the DC voltage of each

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ESE to be decoupled from the DC bus voltage, as well as allowing some of the State of Charge (SOC) management to be implemented at a converter control level. The operation of an MMC designed with an uneven distribution of battery ESE-SMs, have been described in [16], [17]. The authors show how the converter can be balanced using circulating currents even with the battery SMs installed in only one phase. An MMC based BESS in which the upper arm of each phase contains SMs with integrated battery storage, and the lower-arm contains UC ESE-SMs is presented in [18]. A delta-connected multilevel E-STATCOM which contains UCs interfaced to each SM capacitor through an interleaved DC-DC converter is described in [7], [19], including industrial-scale experimental prototyping and testing.

This paper will examine the design and operation of a HVDC-scale MMC which in addition to standard AC-DC power conversion capabilities, has integrated energy storage, allowing the AC and DC powers to be de-coupled to an extent. The purpose is to create a secondary function for the converter, without significantly increasing its ratings or comprising its efficiency, allowing it to provide short-term dynamic ancillary services, such as primary frequency reserve response and de-coupled Power Oscillation Damping (POD), in addition to its standard bulk power transfer capability and voltage support services. Modern VSC HVDC converters have available power-ratings that approach 1.8 GW in a single converter station. Most ESSs for frequency support and ancillary services, such as power oscillation damping, would typically require only a small fraction of a HVDC converter station's power capability [20]–[22]. For this reason it is anticipated that the service provision will be at a fraction of the normal power flow and so a design with Partially Rated Storage (PRS) is considered. It is important that the inclusion of the ESS and the ancillary services do not significantly increase the conduction losses during normal AC-DC power conversion but, unlike a standard ESS, the round-trip efficiency of the energy storage itself may not be of prime concern if the primary use is for emergency ancillary service provision.

## II. CONVERTER TOPOLOGY

### A. Topology Introduction

The proposed Partially Rated Storage MMC (PRS-MMC) is illustrated in Fig. 1. Each converter arm contains a mixture of standard Half-Bridge (HB) Sub-Modules (SMs), and Energy Storage Element SMs (ESE-SMs) in which the SM capacitor

is interfaced to an energy source, shown in the diagram as either a battery or UC, through a DC-DC converter. Unlike the solutions presented in [7], [16]–[18], only a portion of SMs within each arm of the proposed topology are formed of ESE-SMs, with the majority of SMs being of the standard half-bridge type. During normal operation of the converter (i.e. no energy being exchanged from the ESEs and the converter acting as a standard HVDC VSC), the DC-DC converters within each ESE-SM are idle and the ESE-SMs function in an identical manner to the other, capacitor-only, SMs within the converter arm. When energy is being exchanged to/from the ESEs, the DC-DC converters within the ESE-SMs exchange power between the ESE and the main SM capacitor and from there this energy is exchanged with either the AC or DC bus. Exchange with the AC or DC bus is set by appropriate choice of the voltage waveform generated by the ESE-SMs, so that the correct amount of power is extracted from the ESEs. The focus of this paper is on determining the fraction of the total SMs present that need to be converted from capacitor-only SMs to ESE-SMs to achieve a given power flow, and on developing methods of controlling the exchange of energy to/from the ESE-SMs.

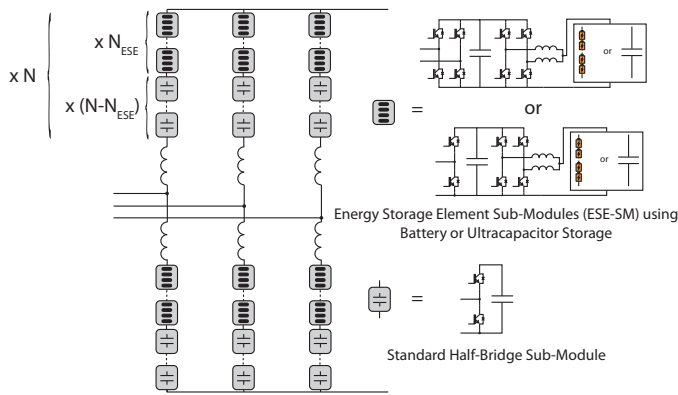


Fig. 1. Modular multilevel converter with partially rated energy storage elements (PRS) showing Energy Storage Element Sub-Modules (ESE-SMs) with both half-bridge and full-bridge topologies, with either batteries or ultracapacitors as the energy source for each ESE-SM.

### B. Analytical Analysis

To operate correctly, MMCs require the average power on the AC and DC sides of the converter to be balanced (neglecting power losses) [23], [24]. This condition results in a net zero energy deviation of the stored energy within the SMs of the converter at the end of each cycle, meaning that the average SM capacitor voltages will not drift over time. In the PRS-MMC, the AC and DC powers can be decoupled, resulting in the overall arm experiencing a non-zero net energy deviation at the end of each cycle. The PRS-MMC can be modelled in a simplified manner as in Fig. 2, with each converter arm being formed of a series combination of two voltage sources, representing the voltage generated by the capacitor-only SMs ( $V_{arm_{cap}}$ ) and the voltage generated by the ESE-SMs ( $V_{ESE}$ ). To ensure the SM capacitors do not suffer a net end-of-cycle deviation in voltage, the net energy

deviation of the capacitor-only portion ( $\Delta E_{arm_{cap}}$ ) of the arm must equal zero, whereas the ESE portion of the arm should have a net energy deviation ( $\Delta E_{ESE}$ ) that matches the desired per-cycle additional exchange of energy.

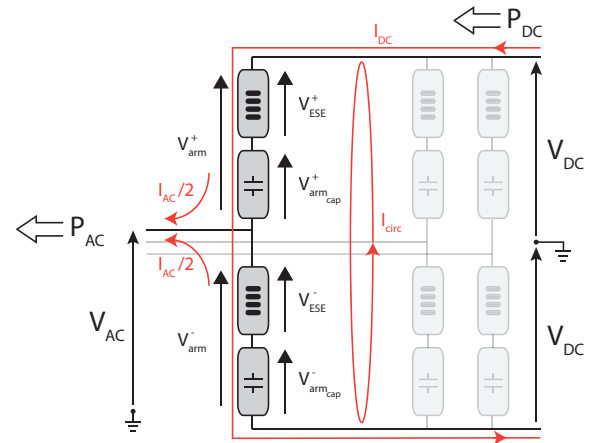
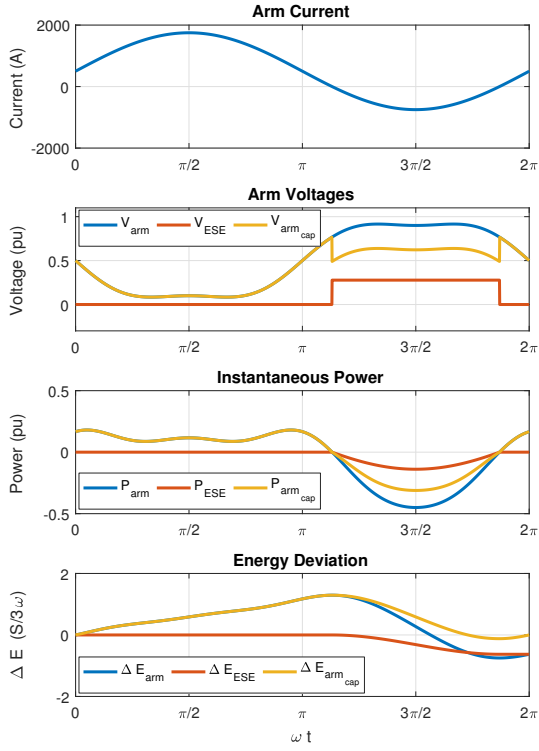


Fig. 2. Electrical model of PRS-MMC showing the voltage source formed by the ESE-SMs and the standard capacitive SMs within each converter arm.

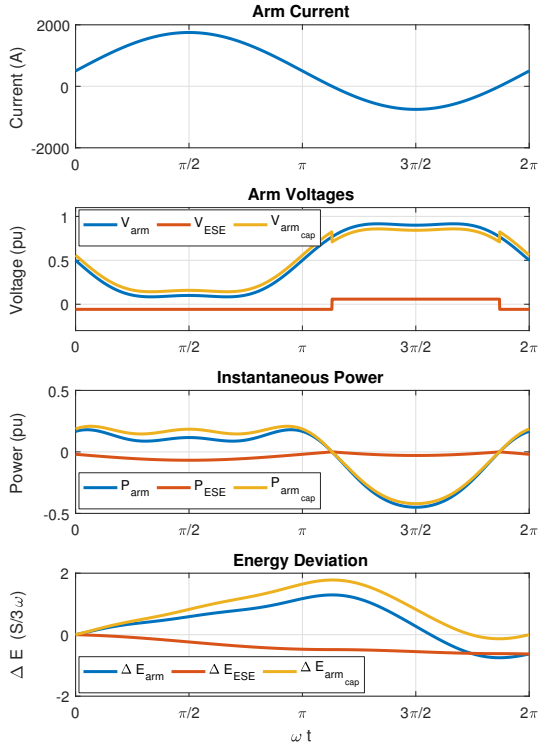
Both HB and FB-SMs are considered for the ESE-SMs and operation of the two types are illustrated in Fig. 3, showing the case where the AC and DC powers have been de-coupled by 0.2 pu. In both cases, the ESE-SMs have been commanded to generate the maximum voltage of which they are capable when this results in a power of the correct polarity being generated. It should be noted that the energy deviations of the ESE-SMs ( $\Delta E_{ESE}$ ) at the end of the cycle and that of the overall arm ( $\Delta E_{arm}$ ) are equal. The end-of-cycle energy deviation of the capacitive portion of the arm ( $\Delta E_{arm_{cap}}$ ) is equal to zero as required. In the HB ESE-SMs case, the ability of the ESE-SMs to generate power of the correct polarity is dependent on the arm current polarity. In contrast, FB ESE-SMs are capable of generating the correct polarity power irrespective of the current polarity. This results in the voltage capability required of the HB ESE-SMs being significantly higher than in the case of the FB HB-ESEs.

An accurate assessment of the fraction of the SMs within each converter arm that needs to be converted to ESE-SMs for a given rated power injection/absorption of storage power ( $P_{ESE}$ ) can not be achieved analytically and will be tackled numerically in a later section. Here, a simplified analysis will be conducted that offers some insights at the expenses of neglecting some constraints. In the simplified analysis, all inductances within the circuit are neglected and the ESE-SMs are assumed to always deploy their full voltage capability when it is possible for them to absorb/generate power of the correct polarity. The capacitor-only portion of the arm must create the correct overall arm voltage taking into account the voltage output of the ESE-SMs. The limit on the total voltage available for the capacitor-only SMs is neglected here but the results will still illustrate the required fraction required to be ESE-SM (expressed as their voltage rating) and the impact of HB and FB ESE-SMs on that fraction.

The current flowing through one of the upper arms of the converter, and assuming any circulating current is well



(a) Half-Bridge ESE-SMs  
 $P_{AC} = 1.2$  (pu)  $P_{DC} = 1$  (pu)



(b) Full-Bridge ESE-SMs  
 $P_{AC} = 1.2$  (pu)  $P_{DC} = 1$  (pu)

Fig. 3. Current, voltage, power and energy deviation waveforms of PRS-MMC Considering operation with HB and FB ESE-SMs. Power and energy deviation given assuming a generator convention.

controlled to zero, can be calculated as in (1) as a function of the converters modulation index ( $m$ ), the DC voltage, and the

AC and DC powers.

$$I_{arm} = \frac{S_{AC}}{3mV_{DC}} \sin(\omega t - \phi) + \frac{P_{DC}}{6V_{DC}} \quad (1)$$

The voltage generated by the overall converter arm, assuming the use of third harmonic injection, can be calculated as:

$$V_{arm}(\omega t) = V_{DC} - mV_{DC} \sin(\omega t) - \frac{mV_{DC}}{6} \sin(3\omega t) \quad (2)$$

The voltage generated by the ESE-SMs as a function of time,  $V_{ESE}(\omega t)$ , will be represented as the product of the minimum required rated voltage of the ESE portion of the converter arm ( $V_{ESE_{min}^{rated}}$ ) and the normalized voltage generated by the ESE-SMs,  $V_{ESE_{norm}}(\omega t)$ .

$$V_{ESE}(\omega t) = V_{ESE_{norm}}(\omega t) \times V_{ESE_{min}^{rated}} \quad (3)$$

FB ESE-SMs are capable of generating a voltage of either polarity and therefore able to create a power flow of the correct direction for either polarity of current flow. The normalized voltage for FB-ESE-SMs is calculated as in (4), where the desired power exchange with the ESE is  $P_{\delta} = S_{AC} \cos(\phi) - P_{DC}$ . In contrast, HB-ESE-SMs can only create the desired power exchange if the current polarity is in the correct direction. The normalized voltage for HB-ESE-SMs is described in (5).

$$V_{ESE_{norm}}(\omega t) = \begin{cases} 1 & \text{if } \text{sgn}(I_{arm}(\omega t)) == \text{sgn}(P_{\delta}) \\ -1 & \text{otherwise} \end{cases} \quad (4)$$

$$V_{ESE_{norm}}(\omega t) = \begin{cases} 1 & \text{if } \text{sgn}(I_{arm}(\omega t)) == \text{sgn}(P_{\delta}) \\ 0 & \text{otherwise} \end{cases} \quad (5)$$

The energy deviation of the overall arm can be calculated as in (6).

$$\Delta E_{arm}(\omega t) = \int_0^{\omega t} V_{arm}(\omega t) I_{arm}(\omega t) d\omega t \quad (6)$$

The energy deviation of the ESE-SMs can then be expressed as in (7).

$$\Delta E_{ESE}(\omega t) = \int_0^{\omega t} V_{ESE_{min}^{rated}} V_{ESE_{norm}}(\omega t) I_{arm}(\omega t) d\omega t \quad (7)$$

To ensure the capacitor-only portion of the arm has a net energy deviation of zero at the end of each cycle, the energy deviation of the ESE-SMs at the end of each cycle must be equal to that of the overall arm (i.e.  $\Delta E_{arm}(2\pi) = \Delta E_{ESE}(2\pi)$ ). The required value of  $V_{ESE_{min}^{rated}}$  can be found by equating (6) and (7) and rearranging to give (8).

$$V_{ESE_{min}^{rated}} = \frac{\int_0^{2\pi} V_{ESE_{norm}}(\omega t) I_{arm}(\omega t) d\omega t}{\int_0^{2\pi} V_{arm}(\omega t) I_{arm}(\omega t) d\omega t} \quad (8)$$

Figure 4 compares the required voltage rating of the ESE-SM portion of the converter arm (indicating the required number of ESE-SMs) as a function of the power

absorbed/generated by the ESE-SMs ( $P_{ESE}$ ) within the PRS-MMC. It can be seen from the upper graphs that the HB ESE-SMs (in blue) require a significantly greater voltage rating than FB ESE-SMs (in red) when supplying power during inverting operation (left hand column) than when they are absorbing power during rectifying operation (right hand column). The analytical method used here does not account for the voltage limitations of the capacitive, standard HB-SM only, portion of the arm. In Fig. 4, it can be seen that in some conditions, the capacitive portion of the arm is required to generate a negative voltage output, which would require bipolar (full-bridge) SMs to be used and in other conditions it is required to generate voltages above 1 and therefore must have its voltage capability uprated. Both of these options are undesirable because they would add conduction losses associated with the extra devices. The next section will revisit the analysis to add constraints on the requested voltage from the standard, capacitor-only SMs.

### III. NUMERICAL ANALYSIS

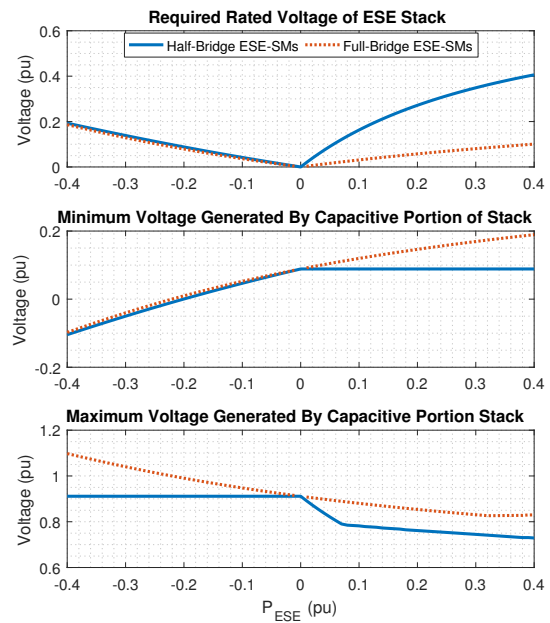
Taking realistic voltage constraints into account for the capacitor-only SMs leads to voltage waveforms for the ESE and standard SM portion of the converter arm that are discontinuous and not amenable to analytical solution. For this reason numerical techniques have been adopted to further investigate the proposed topology. Nonetheless, the previous section indicated something useful which is that the required number of ESE-SMs is significantly reduced if FB ESE-SMs are used. All following results in the paper will therefore assume the use of FB ESE-SMs, and will be combined with standard HB-SMs for the remainder of the converter arm in order not to increase conduction losses.

The voltage limitations that the PRS-MMC must operate under in practice are illustrated in Fig. 5, and can be described generally using (9) and (10), where  $V_{avail_{cap}}^+$  and  $V_{avail_{cap}}^-$  are the positive and negative voltages available from the standard SMs respectively. In the case of the considered PRS-MMC, where the standard SMs are of HB type, the positive available voltage of the standard SMs is given by the sum of their capacitor voltages, while their negative available voltage is zero.

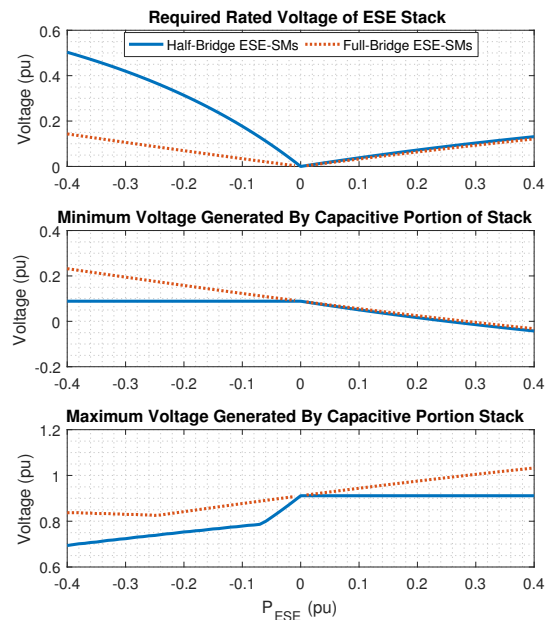
$$V_{avail_{ESE}}^{max}(\omega t) = \min\left(\sum_{n=1}^{N_{ESE}} V_{c_n}, -(V_{avail_{cap}}^- - V_{arm}(\omega t))\right) \quad (9)$$

$$V_{avail_{ESE}}^{min}(\omega t) = \max\left(-\sum_{n=1}^{N_{ESE}} V_{c_n}, -(V_{avail_{cap}}^+ - V_{arm}(\omega t))\right) \quad (10)$$

An example of the positive voltage from the ESE-SMs being limited below the sum ESE-SM capacitor voltage appears in in Fig. 5 from  $t \approx 0.03$  s to  $t \approx 0.08$  s where the output voltage of the ESE-SMs (in yellow) follows the requested overall arm voltage (in blue) rather than adopting its maximum voltage as it does elsewhere where it can to maximize the power transfer of the ESEs. If the proposed scheme was used in a converter topology that includes bipolar SMs as standard, such as the



(a) Inverting Operation,  $P_{DC} = 1$  (pu)  $P_{AC} = P_{DC} + P_{ESE}$



(b) Rectifying Operation  $P_{AC} = -1$  (pu)  $P_{DC} = P_{AC} - P_{ESE}$

Fig. 4. Comparison of the required voltage rating and use for both HB and FB ESE-SMs

Hybrid MMC [25] or Alternate Arm Converter [26], then the negative voltage of the standard SMs could be used to partially compensate for this influence, and potentially reduce the required number of ESE-SMs below what is required in the considered topology.

An example of a constraint on the minimum voltage generated by the ESE-SMs in the PRS-MMC occurs in Fig. 5 from  $t \approx 0.012$  s to  $t \approx 0.018$  s, where the arm voltage approaches the sum SM capacitor voltage of the standard HB-SMs in the overall arm (given by  $V_{avail_{cap}}^+(\omega t) = \sum V_c(\omega t) - \sum_{k=1}^{N_{ESE}} V_{c_k}(\omega t)$ ). During this portion of the cycle generating a negative voltage

would result in the correct sign power being exchanged by the ESE-SMs. Any negative voltage generated by the ESE-SMs must be compensated for by the standard SMs within the arm. As the overall arm voltage approaches  $V_{avail\_cap}^+$  all standard SMs are used to generate a positive output voltage. This initially results in a requirement to limit the negative voltage output of the ESE-SMs. When the overall arm voltage exceeds  $V_{avail\_cap}^+$ , a portion of the ESE-SMs must be utilized to generate a positive voltage, while the others are bypassed, even though this results in the incorrect sign of power being exchanged. A method for deciding which ESE-SMs are selected for which task while accounting for the voltage limits will be described in Section IV.

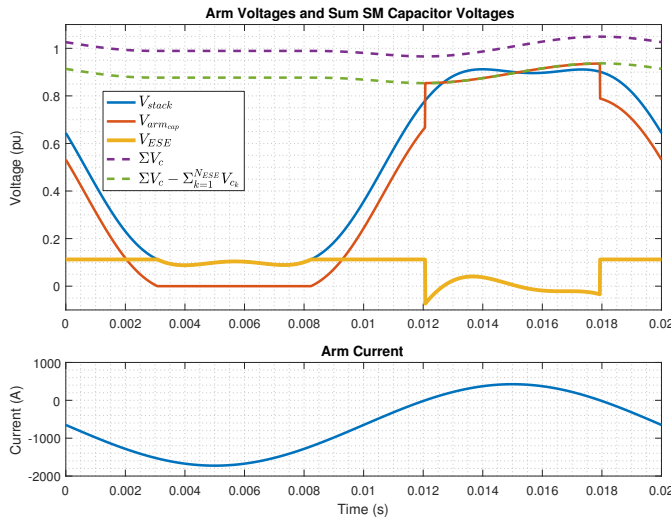


Fig. 5. Illustration of voltage limits within the PRS-MMC when rectifying with additional power flow from the ESE.  $P_{DC} = -1.3$  (pu) and  $P_{AC} = -1$  (pu).

The method used to solve for the minimum required rated voltage of the ESE portion of the arm ( $V_{ESE_{rated}^{min}}$ ) is described by the flowchart in Fig. 6. The AC and DC power references are converted into arm current references and then the voltage drops across the systems inductances (considering both the transformer leakage reactance and arm inductors) are calculated, allowing the voltage generated by the overall converter arm to be calculated. The energy deviation of the overall arm is then calculated numerically as in (6).

The minimum voltage that the ESE-SMs can generate is governed by both the overall arm voltage,  $V_{arm}$ , the time varying sum of SM capacitor voltages,  $\Sigma V_c(\omega t)$ , and the time varying sum ESE-SM capacitor voltage, which is assumed to be negligible in order to simplify the analysis. An investigation into the energy deviation, and resulting impact on voltage deviation and capacitor sizing of the ESE-SMs will be given in Section III-B.  $\Sigma V_c(\omega t)$  is linked to the energy deviation of the capacitive portion of the arm, which is not initially known. An initial estimate of  $\Sigma V_c(\omega t)$  is made using (11), where  $E_{nom}$  is the nominal stored energy within the arm and  $C_{eq}$  is the equivalent capacitance of the arm.

$$\Sigma V_c(\omega t) = \sqrt{2(E_{nom} + \Delta E_{arm\_cap}(\omega t))/C_{eq}} \quad (11)$$

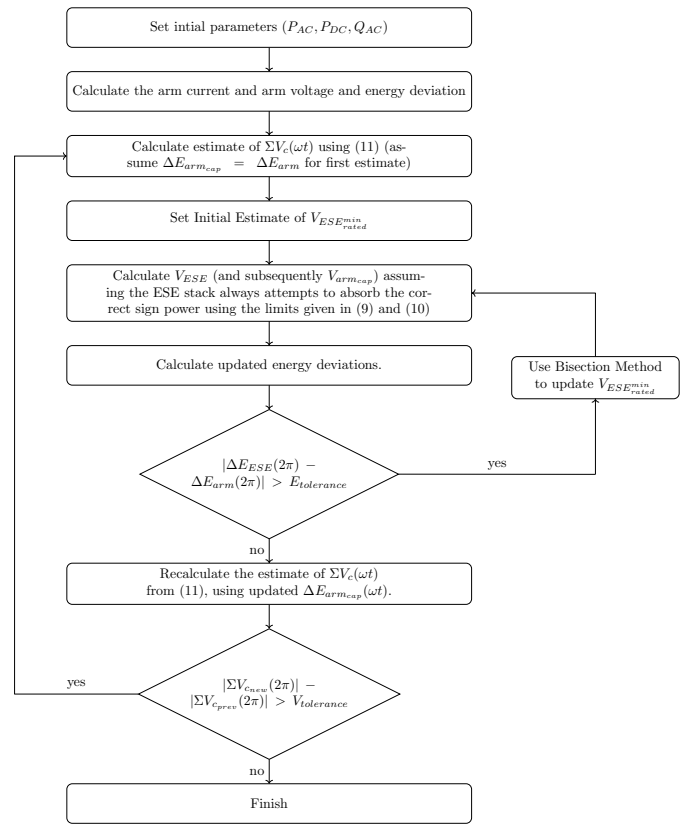
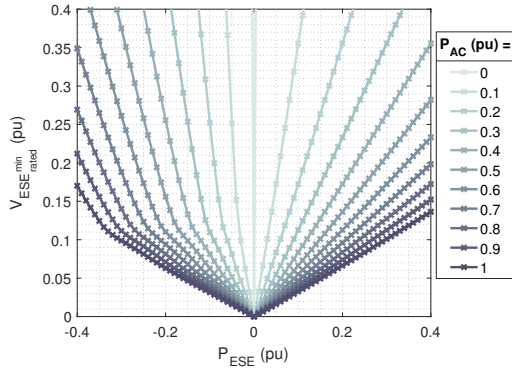


Fig. 6. Flowchart illustrating procedure for numerically solving for the minimum required rated voltage of the ESE portion of the converter arm.

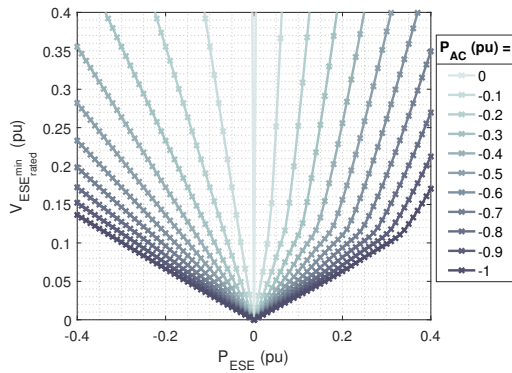
For the initial estimate of the required value of  $V_{ESE_{rated}^{min}}$ ,  $\Delta E_{arm}(\omega t)$  is substituted for the value  $\Delta E_{arm\_cap}(\omega t)$  as this value is initially unknown. The required value of  $V_{ESE_{rated}^{min}}$  is then solved for using the bisection method, so that the energy deviation of the ESE portion of the arm at the end of the electrical cycle is equal to the energy deviation of the overall arm. This ensures that the capacitive portion of the arm has a zero net energy deviation, and hence the capacitor voltages will not have drifted over the cycle. If the difference between the updated and previous sum of SM capacitor voltages at the end of the cycle exceeds a tolerance then the process of solving for  $V_{ESE_{rated}^{min}}$  is repeated with the updated estimate of  $\Sigma V_c(\omega t)$  until the difference in voltage is less than the tolerance.

Using the method of Fig. 6, and the system parameters from Table I, the results shown in Fig. 7 were created, illustrating the required minimum voltage rating of the ESE-SMs for a given rated power of the ESE part of the converter ( $P_{ESE} = P_{AC} - P_{DC}$ ) during both inverting and rectifying operation with variation in the total power being processed by the converter. The values of  $E_{nom}$  and  $C_{eq}$  are calculated assuming the nominal energy of the converter is equivalent to 35 kJ/MVA [27], where the MVA rating is taken as  $S_{base} + |P_{ESE}|$ . For high power throughput ( $\sim 0.7pu$  and above), the required voltage rating of the ESE-SMs (representing the fraction of SMs needing to be ESE) is relatively low but as the power throughput reduces the the required minimum voltage rating is seen to increase significantly. This is because the current magnitude in the converter arm is low and more

voltage is required to maintain the storage power. Further, for cases where the arm current becomes unipolar, the required minimum rated voltage of the ESE-SMs becomes 1.0 pu (i.e., all SMs within the converters need to be of the ESE-SM type), because the capacitor-only portion of the arm cannot achieve zero end-of-cycle energy deviation under this condition. This condition can occur with quite low values of  $P_{ESE}$  if the base power of the converter is low.



(a) Variation in Inverting DC Power  $P_{AC} = P_{DC} + P_{ESE}$



(b) Variation in Rectifying AC Power  $P_{DC} = P_{AC} - P_{ESE}$

Fig. 7. Required minimum rated voltage of the ESE-SMs assuming the use of FB-ESE-SMs with variation in base power.

### A. Operation At Reduced Power Levels

The problem identified in the previous section, namely the significant increase in the required rated voltage of the ESE-SMs for a given  $P_{ESE}$  as the total power being processed by the converter decreases, is a major downside to the proposed topology because the ancillary service provision from the storage needs to be available irrespective of the AC-DC converter's set-point prior to the service but using FB-ESE-SMs in the entire converter arm imposes a significant power loss penalty.

The problem occurs because the decreasing overall arm current magnitude requires an increase in the voltage rating of the ESE-SMs to allow sufficient energy to be exchanged from the ESE-SMs. The proposed solution to this problem is to intentionally inject additional 2nd harmonic circulating current into the converter waveform, which can be used to extract additional power from the ESE-SMs without impacting

the AC or DC current waveforms, or the overall energy balance of the converter. This concept is illustrated in Fig. 8, for the case where the converter is injecting 0.3 pu active power into the AC grid, while the DC side power is set to zero.

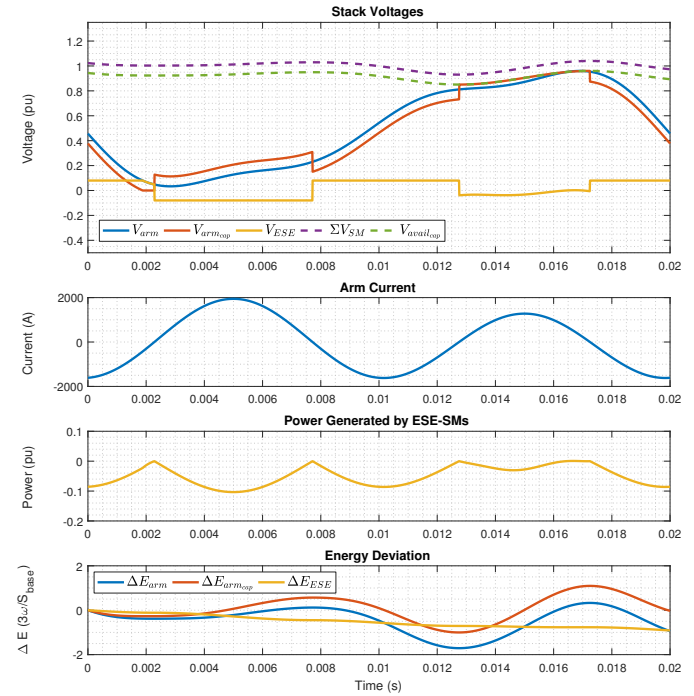


Fig. 8. PRS-MMC operated at  $P_{AC} = 0.3 pu$  and  $P_{DC} = 0 pu$ . The format of the top sub-plot is the same as the top sub-plot in Fig. 5.

It has been found that the phase of the circulating current relative to the fundamental AC component of the arm current has only a very minor impact on the required rated voltage of the ESE-SMs. This is illustrated in Fig. 9 for case where  $P_{ESE}$  is fixed to 0.1 pu, with a fixed magnitude of additional injected circulating current (based upon SM capacitor voltage ripple, or other factors) but this is not considered in this paper.

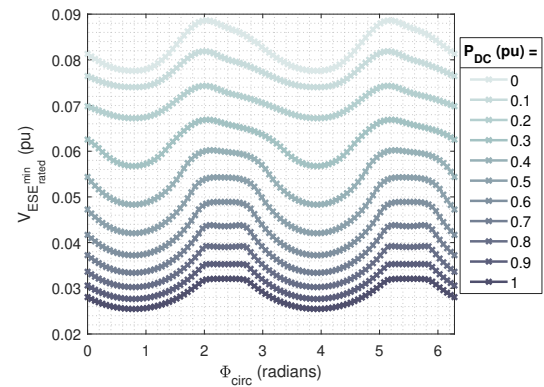


Fig. 9. Required rated voltage of ESE-SM portion of the converter arm with variation in the phase of the additional injected circulating current ( $\Phi_{circ}$ ).  $P_{ESE} = 0.1 pu$   $I_{circ}(\omega t) = 500 \sin(\omega t + \Phi_{circ})$ .

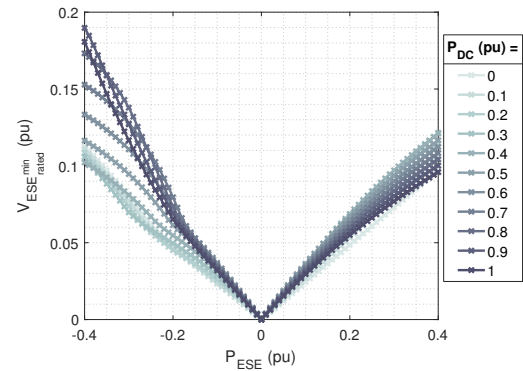
The reduction in the required rated voltage of the ESE achieved with this approach is, naturally, linked to the magnitude of the injected circulating current. The overall efficiency

of the converter when it is providing ancillary services is not considered to be a major concern because it occurs infrequently, therefore, circulating currents that result in arm current magnitudes approaching the continuous peak current rating of the valves are considered acceptable. The proposed circulating current injected into each phase leg ( $k$ ) of the converter is described by (12) where  $ACL$  (arm current limit) is the peak current allowed through the valve.

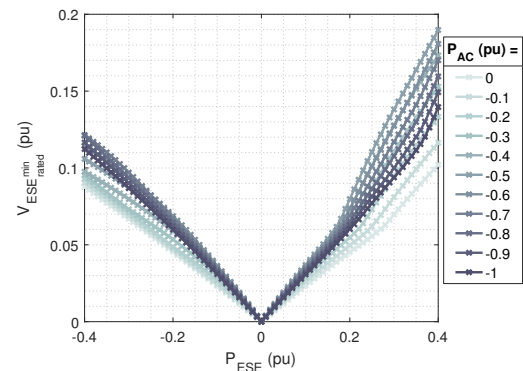
$$I_{circ}^k(\omega t) = \left( ACL - \frac{I_{DC}}{3} - \frac{\hat{I}_{AC}}{2} \right) \left( \frac{|P_{AC} - P_{DC}|}{P_{ESE\ Rated}} \right) \sin \left( 2(\omega t + \phi_k - \phi_{AC} - \frac{\pi}{4}) \right). \quad (12)$$

The analysis method of Fig. 6 was repeated with the added circulating current. For each operating condition employing storage power, the largest possible circulating current is injected subject to the converter arm current limit of  $ACL$ . It was assumed that the converter is rated to provide a fixed  $P_{ESE}$  regardless of its operating point prior to the storage service. The  $ACL$  for each operating point was assumed to be equal to the peak current flowing under the worst case operating conditions for each rating of  $P_{ESE}$  (i.e.,  $P_{AC\ pu} = 1 + |P_{ESE\ pu}|$ ,  $P_{DC\ pu} = 1$ , with zero circulating current). The results from this analysis are shown in Fig. 10. The injection of the circulating current can be seen to significantly reduce the required rated voltage of the ESE-SMs. Now operating points with a low overall power flow have similar requirements to the full rated power case. The results indicate that the minimum of the fraction of SMs that are required to be ESE-SMs is approximately 4% for each 0.1 pu of storage power added, up to  $P_{ESE} \approx 0.2$  pu, where there is an increase in the slope in certain conditions. This increase is due to the influence of the voltage limitations discussed at the start of this section, which become more prominent as  $V_{ESE\ rated}^{min}$  increases.

The peak and RMS current values that result from the proposed circulating current are illustrated in Fig. 11. For brevity results are shown for the case of variation in inverting DC power, with similar results applying to the case of variation in rectifying AC power. The peak arm current value can be seen to be equal at each value of  $P_{ESE}$ , irrespective of the value of  $P_{DC}$ . This reflects the strategy for choosing the magnitude of the circulating current discussed in the previous paragraphs. When the ESE-SMs are generating active power at partially loaded conditions (when circulating current is utilised) the resulting overall RMS arm currents are of similar magnitude to the RMS arm currents at fully loaded conditions (when little or no circulating current is utilised). This indicates that the power-losses and resulting thermal stress on the converter at partially loaded conditions can be expected to be of similar magnitude to that experienced at fully loaded conditions. The highest RMS arm currents occur at partially loaded conditions when the ESE-SMs are absorbing active power. This condition generally results in the minimum required value of  $V_{ESE\ rated}^{min}$  (Fig. 10), which indicates that there is some scope to reduce the required magnitude of the circulating current at this condition, and so reduce the resulting RMS arm current magnitudes.



(a) Half-Bridge MMC - Variation in Inverting DC Power  
 $P_{AC} = P_{DC} + P_{ESE}$



(b) Half-Bridge MMC - Variation in Rectifying AC Power  
 $P_{DC} = P_{AC} - P_{ESE}$

Fig. 10. Required rated voltage of the ESE-SM portion of the converter arm assuming the use of FB-ESE-SMs with variation in base power, with injected circulating current. The value of  $ACL$  for each case is calculated as the peak current resulting from the converter being required to conduct  $P_{AC\ pu} = 1 + |P_{ESE\ pu}|$ ,  $P_{DC\ pu} = 1$ .

### B. Required ESE-SM Capacitor Size

The energy deviation of a converter arm formed of sub-modules is central to determining the required size of the SM capacitor [23]. The average energy deviation per SM in a converter arm is also inversely proportional to the voltage rating of the arm. The ESE-SM and standard SM portions of the converter arms within the PRS-MMC experience different energy deviation waveforms when the ESE-SMs are being utilized, and therefore may require different SM capacitor sizes in order to ensure the same maximum SM capacitor voltage deviation. To investigate this, the ratio of the normalized peak-to-peak energy deviation of the ESE portion of the arm to the normalized peak-to-peak energy deviation of the capacitor-only portion of the arm has been plotted in Fig. 12 for a range of operating points. This ratio indicates the required size of the ESE-SM capacitors relative to the standard SM capacitors. At low values of rated  $P_{ESE}$ , the normalized peak-to-peak energy deviation of the ESE-SMs is seen to be approximately twice that of the standard SMs, with the worst case occurring when the converter is at full rated power. The ratio peaks at a value

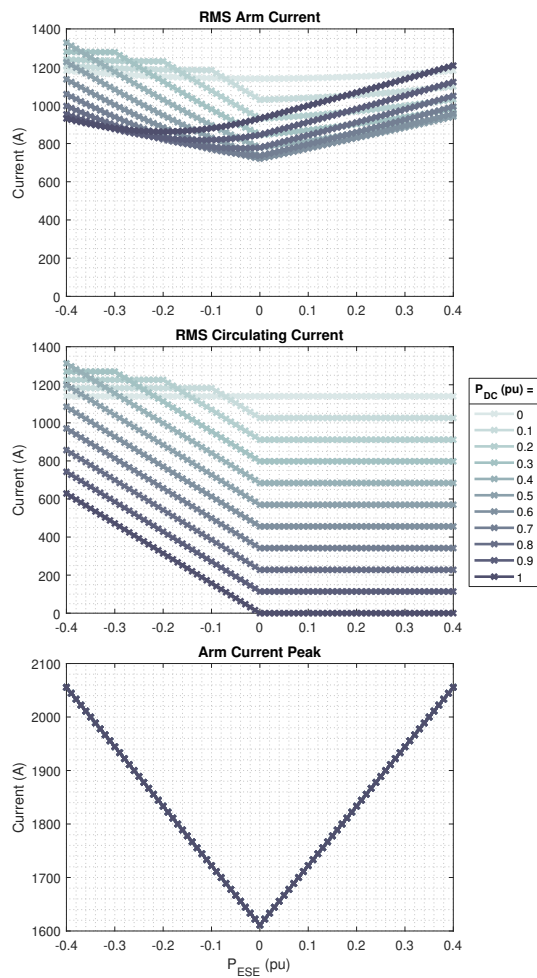


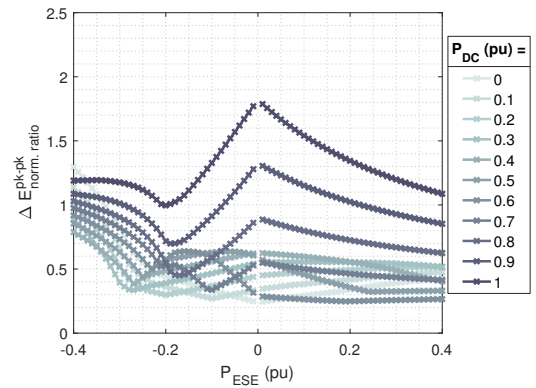
Fig. 11. RMS arm current, RMS circulating current and peak arm current magnitudes in the PRS-MMC assuming the use of FB-ESE-SMs with variation in base power, with injected circulating current. - Variation in Inverting DC Power  $P_{AC} = P_{DC} + P_{ESE}$ .

of around 2.4 when  $P_{ESE}$  is approximately 0.3 pu for the case of delivering additional power to the DC bus during rectifying operation.

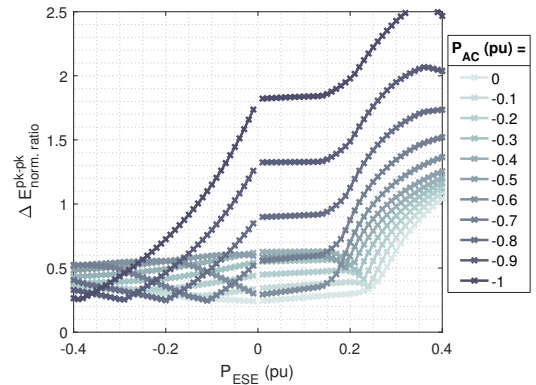
#### IV. CONTROL OF THE CONVERTER

This section describes the proposed control method for the PRS-MMC. The inclusion of the ESE-SMs has been found to not require significant changes to the overall converter control structure, which is shown in Fig. 13, similar to the one presented in [28], which uses full state-feedback based current control. Some changes are required in the current reference generator, which now has separate AC and DC current references which are combined into references for each arm in the converter. A circulating current reference generator is also included based upon (12). The main difference in the controller lies in the low-level control, which translates the voltage references from the current controller into gating signals for each SM, as will now be explained.

Each ESE-SM within the PRS-MMC can be assigned a different active power set-point, the sum of which must equal the difference between the AC and DC side powers. This ability could be used to achieve State of Charge (SoC)



(a) Variation in Inverting DC Power  $P_{AC} = P_{DC} + P_{ESE}$



(b) Variation in Rectifying AC Power  $P_{DC} = P_{AC} - P_{ESE}$

Fig. 12. Ratio of the normalized peak to peak energy deviation of the ESE portion of the converter arm to the normalized peak to peak energy deviation of the capacitive portion of the converter arm.

management of the ESEs. The power reference for each ESE-SM is then translated into a current reference for each ESE-SM's DC-DC converter based upon the measured average SM capacitor voltage. The main challenge in controlling the proposed topology is in ensuring the correct amount of power is exchanged from the ESE-SMs to the AC or DC system while also limiting their capacitor voltage's cycle-by-cycle deviation from their nominal value. It has been found possible to achieve these goals by relying on a voltage balancing algorithm that maintains the ESE-SM capacitor voltages around a tolerance band centered about the nominal voltage. This algorithm is used to control the output states of each of the ESE-SMs, while respecting the voltage limitations of the remainder of the SMs in the converter arm, as discussed in Section III. Once all ESE-SM have been assigned output states the output voltages of the ESE-SMs are summed, and subtracted from the voltage reference received from the current controller ( $V_{ref}$ ) to form the reference for the standard SMs within the arm. The modulation and SM voltage balancing for the standard SMs can then be achieved in a standard manner.

The proposed ESE-SM voltage balancing algorithm (ESE-VBA) is shown by the flowchart in Fig.14 and its operation illustrated in Fig. 15. Each ESE-SM may have differing power set-points, and so the voltage ripple of a ESE-SM may be significantly different from other ESE-SMs within the same arm. To account for this, the ESE-SMs are periodically sorted



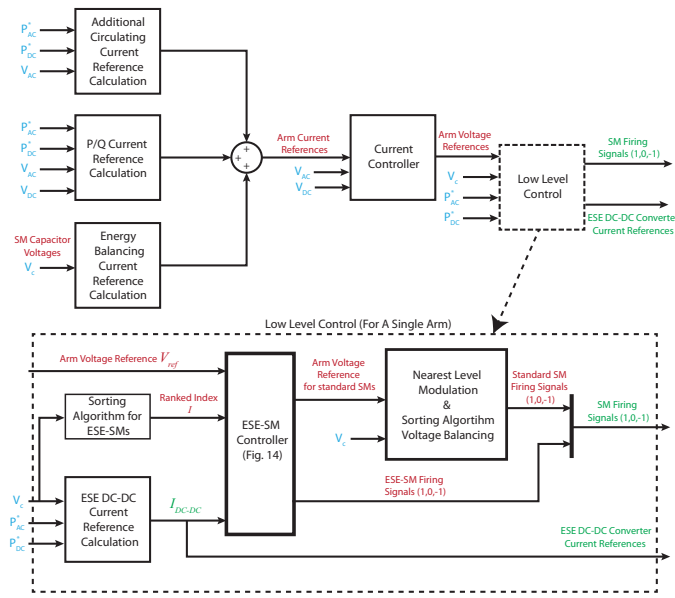


Fig. 13. Overall control scheme and low level control for a single arm within the PRS-MMC

by a ranked index ( $I$ ) based on their absolute deviation from the nominal SM capacitor voltage, rather than their deviation from a mean instantaneous value. A hysteresis band centered around the nominal SM voltage is defined. In order for this controller to function correctly, it has been found that this hysteresis band should be selected so that it is greater than the maximum expected voltage deviation of the ESE-SMs. Each ESE-SM is assigned a command ( $C$ ) to preferentially charge or discharge itself based on whether it has crossed the hysteresis band. This is illustrated in the 2nd and 4th sub-plots of Fig. 15. The rank index ( $I$ ), together with the charging command ( $C$ ), SM capacitor voltages, arm voltage reference from the current controller, measured arm current and the DC-DC converter current references for each ESE-SM are passed to the ESE-SM Voltage Balancing Controller (ESE-VBA). The remaining voltage to be assigned,  $V_{remain}$ , is initially set equal to the reference from the current controller,  $V_{ref}$ , while the available voltage in the arm is set to the sum of all SM capacitor voltages. These values are used to ensure a voltage limitation is not breached. The potential capacitor charging currents for the  $k$ th ESE-SM in the sorted index list are then calculated. These are then ranked based upon the charging command for that ESE-SM. If the sign of the charging command is equal to the sign of the ESE-SMs DC-DC converter's current reference then the zero output voltage is chosen as the preferred state. This has been found to give significantly better performance in terms of keeping SMs within the tolerance band. In addition, in certain operating conditions, all potential charging currents through an ESE-SM can be of the same sign for a portion of the arm current waveform (due to the additional DC current from the ESE DC-DC converter), and so the ESE-VBA cannot always charge the ESE-SMs in the desired direction. This was found to result in some small overshoots in capacitor voltage past the hysteresis band. Selecting the minimum absolute available

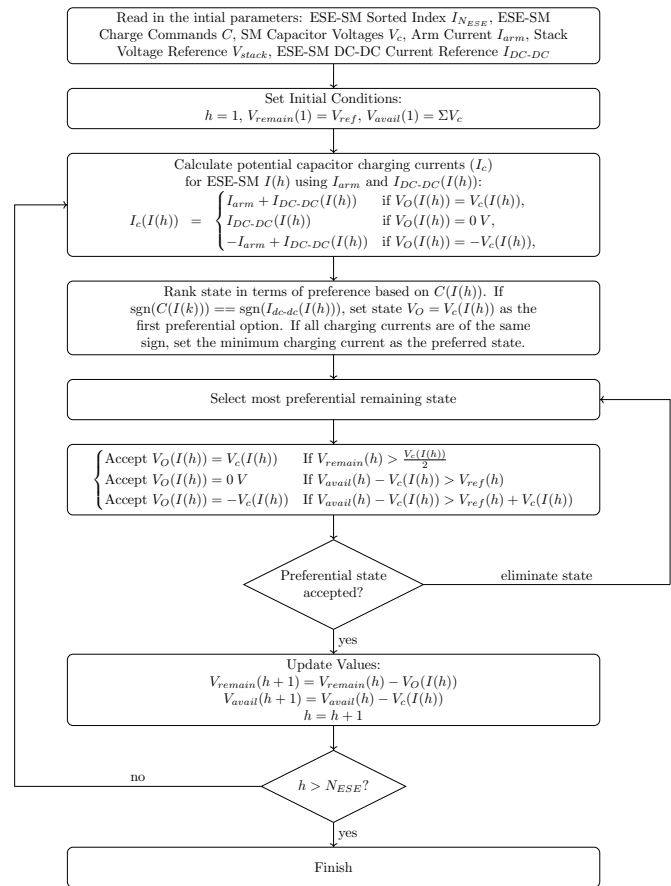


Fig. 14. Flowchart illustrating proposed method for assigning firing states to each ESE-SM within a converter arm within the PRS-MMC.

charging current in these situations was found to be effective in limiting these overshoots past the hysteresis band. The preferred output state is then checked to see if it would result in a voltage limit breach. If the output state for that ESE-SM is not accepted then that state is eliminated from the sorted list of preferred states and the next preferred output state is checked. If the preferred charging state is accepted then  $V_{remain}$  and  $V_{avail}$  are updated and the process incremented to the next ESE-SM in the sorted list. Once all ESE-SMs have been assigned states, the value of  $V_{remain}$  is passed to an additional subsystem which controls the modulation and voltage balancing (in this case using nearest level modulation with sorting algorithm based voltage balancing) of the standard SMs within the arm. The results in Fig. 15 demonstrate stable operation of the converter with the voltages of ESE-SMs being kept within the tolerance band. One ESE-SM in the arm is initially assigned a power reference of opposite sign to the other ESE-SMs, illustrating that the controller is capable of decoupling the power of individual ESE-SMs in order to allow for SoC management, at  $t=0.1$  s, the set-point of the converter is changed and all ESE-SMs are assigned differing power set-points, with now differing voltage ripples being imposed on each ESE-SM capacitor. The capacitor voltages remain well controlled throughout.

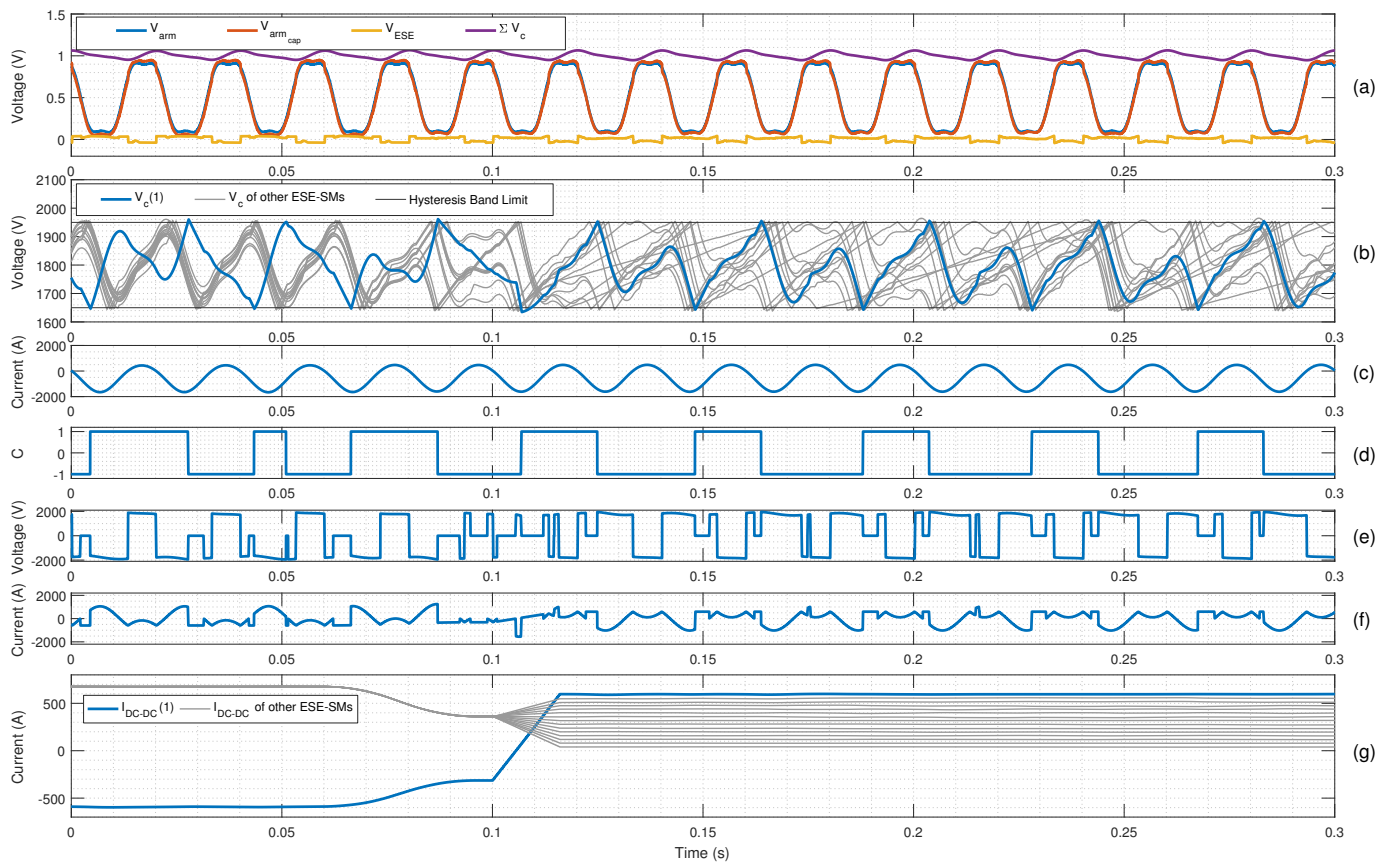


Fig. 15. ESE-SM voltage balancing and assignment system operating, showing details for the upper arm in phase A. ESE-SM power set-points are indicated by their DC-DC converter currents. From Top: (a) Arm voltages. (b) ESE-SM capacitor voltages and hysteresis band. (c) Arm current. (d) Charging command ( $C$ ) for ESE-SM 1. (e) Output voltage ( $V_o$ ) for ESE-SM 1. (f) Capacitor current ( $I_c$ ) for ESE-SM 1. (g) ESE-SM DC-DC currents ( $I_{DC-DC}$ ). Voltage and current waveforms are shown for the upper arm of phase A.

## V. SIMULATION RESULTS

To verify the analysis within the previous sections, a simulation model of the PRS-MMC was implemented in Matlab/Simulink. The DC-DC converters within the ESE-SMs were modeled as current sources connected to the capacitor of each ESE-SM. The specifications of the test converter are given in Table I. The AC and DC systems are modelled as ideal voltage sources. The results in Section III-A indicated 4% of SM should be ESE-SMs for 0.1 pu storage power but 4.5% was used to provide a small headroom for control margin. Using the results in Section III-B, the ESE-SM capacitors were chosen to be twice the size of the capacitors of the capacitor-only SMs.

Simulation results are shown in Fig. 16, showing an artificial test that has been chosen to highlight the ability of the converter to quickly decouple its AC and DC side powers, irrespective of the loading conditions, as would be required if the converter was providing frequency support services or decoupled power oscillation damping. The AC and DC powers are increased through six operating points with decoupling between them provided by the energy extracted from the ESE-SMs. At partially loaded conditions additional circulating current is injected into the arms to enable additional energy to be extracted from the ESE-SMs. The converter achieves good current tracking (Fig. 16(c)) and well-controlled SM voltages

(Fig. 16(d)) notwithstanding the many changes in operating point. The last subplot (Fig. 16(e)) shows the DC-DC current exchanging energy the ESE to the main SM capacitor of one ESE-SM, as well the overall current through the SM capacitor.

TABLE I  
SIMULATION MODEL SPECIFICATION

DC Voltage	$\pm 320$ kV
AC Voltage (L-L RMS)	400 kV
Rated Power	960 MW
Rated Energy Storage Power	96 MW (0.1 pu)
Transformer Leakage Reactance	0.14 pu
Arm Inductor	0.1 pu
Nominal SM Voltage	1800 V
SM Capacitor	9.7 mF
Equivalent Stored Energy	35 kJ/MVA
Total Number of SMs	356
Number of Standard SMs	331
Number of ESE-SMs	15 (~4%)
Controller Frequency	10 kHz
Simulation Time-Step	1 $\mu$ s

## VI. CONCLUSION

A dual-purpose variant of the Modular Multilevel Converter (MMC) has been introduced that incorporates Partially Rated Storage (PRS) to provide additional system services through partially decoupling the AC and DC powers. This is achieved by interfacing a fraction of sub-modules (SMs) within each converter arm through a DC-DC converter to an

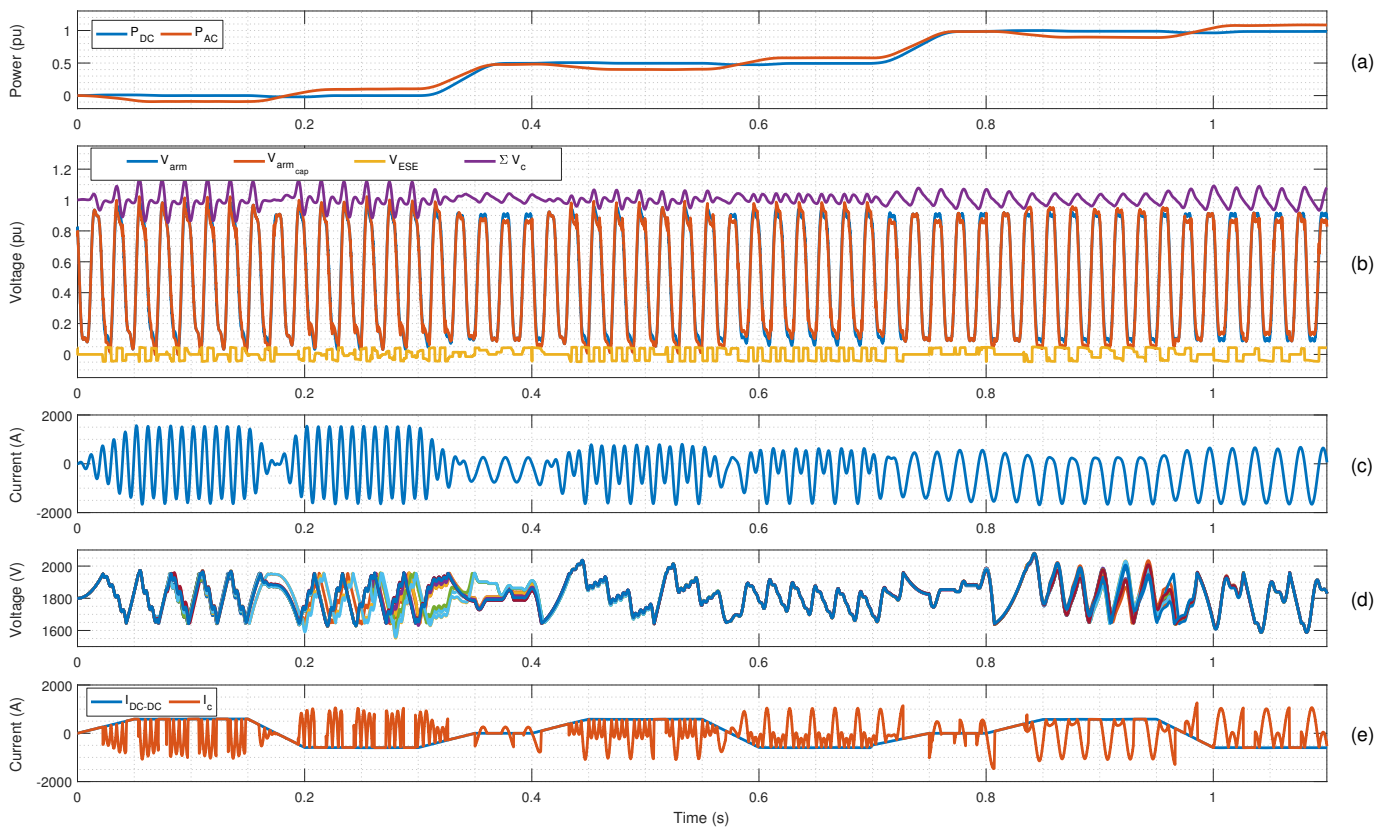


Fig. 16. PRS-MMC operating at several set-points, utilizing circulating currents at partial loading conditions. From top: (a) DC & AC powers. (b) Arm voltages and sum SM capacitor voltage. (c) Arm current. (d) ESE-SM capacitor voltages. (e) Capacitor current ( $I_c$ ) and DC-DC current ( $I_{DC-DC}$ ) of ESE-SM 1 in phase A. Voltage and current waveforms are shown for the upper arm of phase A.

Energy Storage Element (ESE), such as ultra-capacitors or batteries. By controlling the voltage generated by the ESE-SMs, energy can be extracted from the ESEs and directed to either the AC or DC bus. A method has been described for determining the required number of ESE-SMs within the converter which takes into account the voltage limitations of the standard SMs within the converter. Results show that using Full-Bridge (FB) ESE-SMs gives a significant decrease in the required number of ESE-SMs to achieve a given storage power flow. To overcome a problem with large numbers of ESE-SMs being needed at low power throughput, a method of injecting circulating current into the arm current has been devised. When utilised, this circulating current can be expected to cause significant additional losses, and so the proposed topology is not considered suitable for energy arbitrage purposes. The final results show that the required fraction of SMs comprising ESE-SMs is approximately 4% for each 0.1 pu of power required from the energy storage. That 4% of SM incur higher conduction power-loss because they are full-bridges but nonetheless, a dual-purpose MMC with AC-DC power conversion plus storage services for network control is achieved. Achieving rated powers of energy storage that are a significant fraction of the overall nominal rated power is likely to entail additional challenges in the converter design, such as increased peak and RMS currents which can be expected to impact the semiconductor choice and thermal design, and other impacts such as increased SM capacitor sizes due to the

increased ripple imposed. Values up to values of  $P_{ESE} = 0.4$  pu have been given to show the overall trend in results. A controller capable of ensuring the correct amount of energy is exchanged to/from the ESE-SMs has also been detailed. The analytical results and the controller performance have been verified by circuit simulation results. The proposed topology and controller could potentially be extended to other modular converter topologies, such as the Hybrid MMC, Alternate Arm Converter or Cascaded H-Bridge STATCOM. Future work could focus on: optimisation of the circulating current required at partially loaded conditions, more detailed assessment of the impact on the overall converter/sub-module design and cost, and studies examining the potential benefits and application of this type of converter from a power systems perspective.

## REFERENCES

- [1] E. Namor, F. Sossan, R. Cherkaoui, and M. Paolone, "Load leveling and dispatchability of a medium voltage active feeder through battery energy storage systems: Formulation of the control problem and experimental validation," in *2016 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe)*, Oct 2016, pp. 1–6.
- [2] J. Cai, Q. Xu, J. Ye, J. Xue, and X. Xu, "Optimal configuration of battery energy storage system considering comprehensive benefits in power systems," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 2650–2653.
- [3] Y. Ning, X. Li, X. Ma, X. Jia, and D. Hui, "Optimal schedule strategy of battery energy storage systems for peak load shifting based on interior point method," in *2016 12th World Congress on Intelligent Control and Automation (WCICA)*, June 2016, pp. 2285–2288.

- [4] M. Benini, S. Canevese, D. Cirio, and A. Gatti, "Battery energy storage systems for the provision of primary and secondary frequency regulation in Italy," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, June 2016, pp. 1–6.
- [5] F. M. Gonzalez-Longatt and S. M. Alhejaj, "Enabling inertial response in utility-scale battery energy storage system," in *2016 IEEE Innovative Smart Grid Technologies - Asia (ISGT-Asia)*, Nov 2016, pp. 605–610.
- [6] Y. J. Zhang, C. Zhao, W. Tang, and S. H. Low, "Profit maximizing planning and control of battery energy storage systems for primary frequency control," *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1–1, 2016.
- [7] E. Spahic, C. P. S. S. Reddy, M. Pieschel, and R. Alvarez, "Multilevel statcom with power intensive energy storage for dynamic grid stability - frequency and voltage support," in *2015 IEEE Electrical Power and Energy Conference (EPEC)*, Oct 2015, pp. 73–80.
- [8] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3119–3130, Nov 2011.
- [9] C. Qian and M. L. Crow, "A cascaded converter-based statcom with energy storage," in *2002 IEEE Power Engineering Society Winter Meeting, Conference Proceedings (Cat. No.02CH37309)*, vol. 1, 2002, pp. 544–549 vol.1.
- [10] I. Trintis, S. Munk-Nielsen, and R. Teodorescu, "A new modular multilevel converter with integrated energy storage," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, Nov 2011, pp. 1075–1080.
- [11] M. Schroeder, S. Henninger, J. Jaeger, A. Ra?, H. Rubenbauer, and H. Leu, "Integration of batteries into a modular multilevel converter," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–12.
- [12] T. Soong and P. W. Lehn, "Evaluation of emerging modular multilevel converters for bess applications," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2086–2094, Oct 2014.
- [13] M. Vasiladiotis and A. Rufer, "Balancing control actions for cascaded h-bridge converters with integrated battery energy storage," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–10.
- [14] —, "Analysis and control of modular multilevel converters with integrated battery energy storage," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 163–175, Jan 2015.
- [15] N. Kawakami, S. Ota, H. Kon, S. Konno, H. Akagi, H. Kobayashi, and N. Okada, "Development of a 500-kw modular multilevel cascade converter for battery energy storage systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 3902–3910, Nov 2014.
- [16] M. Schroeder, S. Schmitt, S. Henninger, J. Jaeger, H. Rubenbauer, and O. Reimann, "Measurement results of a modular energy storage system unevenly equipped with lithium-ion batteries," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sept 2015, pp. 1–11.
- [17] G. Henke and M. M. Bakran, "Balancing of modular multilevel converters with unbalanced integration of energy storage devices," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–10.
- [18] L. Zhang, Y. Tang, S. Yang, and F. Gao, "A modular multilevel converter-based grid-tied battery-supercapacitor hybrid energy storage system with decoupled power control," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 2964–2971.
- [19] M. John, A. Mertens, L. Baruschka, M. Pieschel, and R. Alvarez, "Design and evaluation of a test rig for full-size grid frequency stabilizer modules with ultracapacitors," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–9.
- [20] T. Smed and G. Andersson, "Utilizing hvdc to damp power oscillations," *IEEE Transactions on Power Delivery*, vol. 8, no. 2, pp. 620–627, Apr 1993.
- [21] D. V. Hertem, O. Gomis-Bellmunt, and J. Liang, *Power system oscillation damping by means of VSC-HVDC systems*. Wiley-IEEE Press, 2016, pp. 528–. [Online]. Available: <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7435166>
- [22] N. T. Trinh, I. Erlich, and S. P. Teeuwssen, "Methods for utilization of mmc-vsc- hvdc for power oscillation damping," in *2014 IEEE PES General Meeting — Conference Exposition*, July 2014, pp. 1–5.
- [23] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *Power Electronics, IET*, vol. 8, no. 3, pp. 350–360, 2015.
- [24] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, Jan 2014.
- [25] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, March 2015.
- [26] M. M. C. Merlin, D. Soto-Sanchez, P. D. Judge, G. Chaffey, P. Clemow, T. C. Green, D. R. Trainer, and K. J. Dyke, "The extended overlap alternate arm converter: A voltage-source converter with dc fault ride-through capability and a compact design," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3898–3910, May 2018.
- [27] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-Level Converters," in *CIGRE, 2010*.
- [28] P. Münch, D. Görges, M. Izák, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Nov. 2010, pp. 150–155.



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