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Wearable electroencephalography for long-term monitoring and diagnostic purposes

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Abstract

Truly Wearable EEG (WEEG) can be considered as the future of ambulatory EEG units, which are the current standard for long-term EEG monitoring. Replacing these short lifetime, bulky units with long-lasting, miniature and wearable devices that can be easily worn by patients will result in more EEG data being collected for extended monitoring periods. This thesis presents three new fabricated systems, in the form of Application Specific Integrated Circuits (ASICs), to aid the diagnosis of epilepsy and sleep disorders by detecting specific clinically important EEG events on the sensor node, while discarding background activity. The power consumption of the WEEG monitoring device incorporating these systems can be reduced since the transmitter, which is the dominating element in terms of power consumption, will only become active based on the output of these systems.

Candidate interictal activity is identified by the developed analog-based interictal spike selection system-on-chip (SoC), using an approximation of the Continuous Wavelet Transform (CWT), as a bandpass filter, and thresholding. The spike selection SoC is fabricated in a 0.35 μm CMOS process and consumes 950 nW. Experimental results reveal that the SoC is able to identify 87% of interictal spikes correctly while only transmitting 45% of the data.

Sections of EEG data containing likely ictal activity are detected by an analog seizure selection SoC using the low complexity line length feature. This SoC is fabricated in a 0.18 μm CMOS technology and consumes 1.14 μW. Based on experimental results, the fabricated SoC is able to correctly detect 83% of seizure episodes while transmitting 52% of the overall EEG data.

A single-channel analog-based sleep spindle detection SoC is developed to aid the diagnosis of sleep disorders by detecting sleep spindles, which are characteristic events of sleep. The system identifies spindle events by monitoring abrupt changes in the input EEG. An approximation of the median frequency calculation, incorporated as part of the system, allows for non-spindle activity incorrectly identified by the system as sleep spindles to be discarded. The sleep spindle detection SoC is fabricated in a 0.18 μm CMOS technology, consuming only 515 nW. The SoC achieves a sensitivity and specificity of 71.5% and 98% respectively.

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List of Publications

The following papers have been published as part of this work.

Journal papers

- S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017.

- S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017.

Peer reviewed conference papers

- S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE International New Circuits and Systems Conference (NEWCAS), Vancouver, Jun. 2016.

- S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, Nov. 2016.

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Declaration of Originality

I hereby confirm that the work presented here is my own, and that appropriate references have been used to denote the work of others.

Saam Iranmanesh

February, 2018.

Copyright Declaration

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Terms and Abbreviations

Term	Meaning
AAR	Adaptive Autoregressive
AASM	American Academy of Sleep Medicine
AdaBoost	Adaptive Boosting Algorithm
ADC	Analogue to Digital Converter
AC	Alternating Current
AED	Anti Epileptic Drug
AEEG	Ambulatory Electroencephalography
ANN	Artificial Neural Network
AP	Average Power
ASIC	Application Specific Integrated Circuit
AUC	Area Under Curve
BPF	Band Pass Filter
CMFB	Common Mode Feed Back
CMFF	Common Mode Feed Forward
CMRR	Common Mode Rejection Ratio
CWT	Continuous Wavelet Transform
DAQ	Data Acquisition
DC	Direct Current
DRL	Driven Right Leg
DSL	DC Servo Loop
DWT	Discrete Wavelet Transform
EDS	Excessive Daytime Sleepiness
EEG	Electroencephalography
ECG	Electrocardiography
ECoG	Electrocordticography
EMD	Empirical-Mode Decomposition
EMG	Electromyography
EOG	Electrooculography

Term	Meaning
ES	Expert System
FDA	Food and Drug Administration
FE	Feature Extraction
FT	Fourier Transform
FFT	Fast Fourier Transform
FN	False Negative
FP	False Positive
GA	Genetic Algorithm
HHT	Hilbert-Huang Transform
HPSG	Home Polysomnography
IA	Instrumentation Amplifier
IBE	International Bureau for Epilepsy
ICMR	Input Common Mode Range
IEC	International Eletrotechnical Commision
IED	Interictal Epileptiform Discharge
IFCN	International Federation of Clinical Neurophysiology
ILAE	International League Against Epilepsy
IQ	Intelligence Quotient
LLS	Linear Least Square
LPF	Low Pass Filter
LSP	Local Signal Processing
MAV	Moving Average
MDD	Major Depressive Disorder
ME	Myoelectric
MIM	Metal–Insulator–Metal
MP	Matching Pursuit
NEO	Nonlinear Energy Operator
NLSVM	Non Linear Support Vector Machine
NEWCAS	International New Circuits and Systems Conference
NREM	Non Rapid Eye Movement
OTA	Operational Transconductance Amplifier
OOS	Output Offset cancelation Scheme
PC	Personal Computer
PCA	Principle Component Analysis

Term	Meaning
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PSG	Polysomnography
PTAT	Proportional To Absolute Temperature
QIR	Quasi Infinite Resistor
REM	Rapid Eye Movement
RFID	Radio Frequency Idetification
SAR	Successive Approximation Register
SC	Switched-Capacitor
SEF	Spectral Edge Frequency
SNR	Signal to Noise Ratio
SoC	System on Chip
STFT	Short Time Fourier Transform
SVM	Support Vector Machine
TEG	Thermo Electric Generator
TEO	Teager Energy Operator
THD	Total Harmonic Distortion
TP	Trur Positive
TN	True Negative
WBAN	Wireless Body Area Network
WEEG	Wearable Electroencephalography

1 Introduction

1.1 Overview

In recent years, there has been growing interest in the use of Wireless Body Area Networks (WBAN) to gather physiological data across the human body for monitoring applications related to healthcare. A conceptual implementation of a network with three tiers is shown in Figure 1.1. Sensor nodes are worn on the body in the first tier to collect physiological signals. These nodes must be of small size, consume little power and incorporate wireless transmission capabilities free from obtrusive wires. In the second tier, a local hub receives the data collected by the sensors. The local hub is a portable device with processing and storage capabilities, and less restrictions in terms of the device size and power consumption, such as a mobile phone or tablet, that is placed within the immediate vicinity of the user. The gathered data is eventually transmitted to a Personal Computer (PC) or a group of computers with high computational power used for data analysis and storage, in the third tier of the network.

In order to be unobtrusive and allow for comfortable movement during routine activities, the sensor should be lightweight and small in size. The physical attributes of the sensor are also particularly important from a privacy standpoint in health monitoring applications, since wearing a larger device may disclose information about the user's health condition [1]. Furthermore, the sensor must consume little power to allow for long-term continuous monitoring without the need for replacement or recharging of the batteries, which can be challenging tasks for untrained users. The constraints imposed on the power consumed by the sensor node are also related to the node size, since a smaller battery with less energy capacity can be used in a miniature sensor.

Development of truly wearable health monitoring systems, that obey the mentioned constraints, with long operating lifetime remains an open challenge due to the power hungry nature of wireless transmitters, which dominate the system power consumption. Integration of intelligent signal processing algorithms into wireless and miniature health monitoring systems will reduce the amount of power required

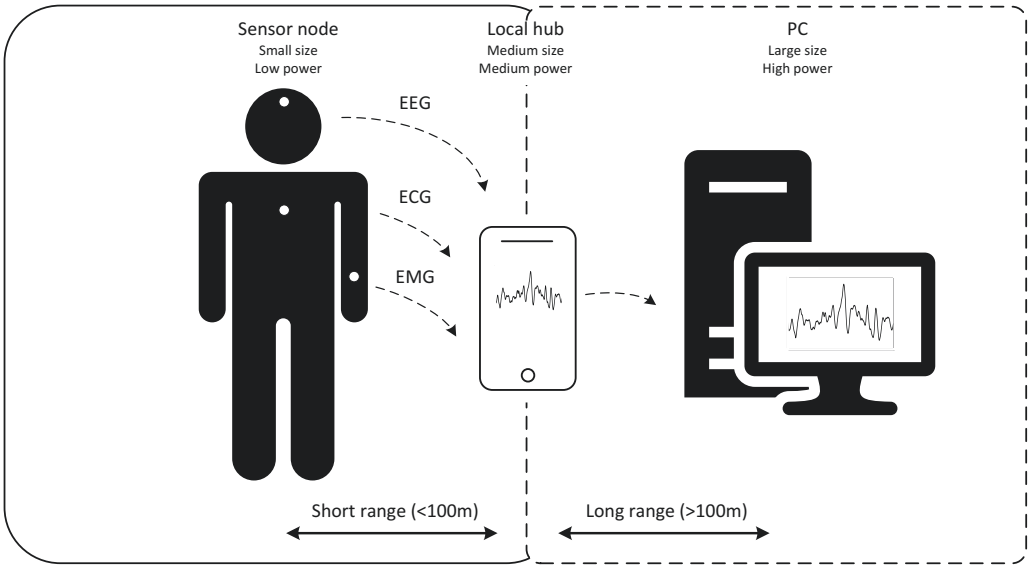

Figure 1.1: *Conceptual implementation of a network consisting of three tiers. In the first tier, miniature sensors are used to gather and transmit physiological data to a local hub, such a mobile phone or portable tablet, in the second tier. Data is then transmitted to a PC, or group of computers, in the third tier for data analysis.*

to transmit physiological data by identifying diagnostically interesting sections of data while discarding background activity. Therefore, the transmitter will only be switched *ON* based on the algorithm detection results. The duration of diagnostically interesting events are generally insignificant compared to the amount of background activity present in data obtained during long monitoring sessions. Thus, significant power savings could be realized using the mentioned approach, resulting in a significant improvement in the battery lifetime of a wearable health monitoring system. In addition, the amount of data presented to the physician for analysis will be reduced as a result of the algorithm operation, resulting in a reduction in the amount of time and resources required for the diagnostic process.

This thesis describes three intelligent signal processing Systems-on-Chip (SoC) for wearable electroencephalography (WEEG) to aid the diagnosis of epilepsy and sleep disorders, which are common neurological diseases with significant negative impact. The diagnostic role of the combination of the presented SoCs is also important considering the comorbidities between epilepsy and sleep disorders [2].

The presented SoCs operate in real-time with low power consumption in or-

der to be truly beneficial in terms of power savings. The motivation, design and experimental results for each system is described in detail.

1.2 Thesis structure

This thesis is organized in four technical chapters. The main contributions of each chapter are summarized below.

Chapter 2 - Wearable EEG: What is it and why is it important?

The main principles of electroencephalography (EEG) and its role in the diagnosis of epilepsy and sleep disorders are discussed in this chapter. The current diagnostic process, which is costly and time consuming for both patients and physicians, is discussed together with the importance of long-term EEG monitoring for increasing diagnostic yield.

The shortcomings of existing ambulatory EEG systems, which are the current standard for long-term EEG monitoring, are discussed as a motivation for the development of long-lasting miniature and wireless EEG systems. A review is presented on the state-of-the-art of individual electronic blocks required to create such EEG systems with reference to the wearability, usability, performance and medical compliance of the overall system. Subsequently, continuous transmission of raw EEG data is recognized as the bottleneck to achieving long-term continuous operation in a wearable EEG system. Local intelligence, in the form of local signal processing, is introduced as a solution to improving the system battery lifetime by reducing the communication cost and amount of data transmitted. This is followed by an analysis of possible approaches to designing intelligent, and application specific, signal processing blocks in wearable EEG systems.

Chapter 3 - A 950 nW interictal spike selection and data reduction System-on-Chip

This chapter presents, for the first time, the design and results for an analog-based data reduction SoC that selects sections of data containing likely interictal epileptiform discharges present within EEG traces and thereby reduces the power consumed by a wearable EEG system. Interictal activity consists of brief events

that occur more frequently than ictal activity in epileptic patients and provide critical information for the clinical diagnosis of epilepsy.

An interictal spike detection algorithm which operates based on the Continuous Wavelet Transform (CWT) at two different scales together with a threshold, is modified in order to create the proposed parallel-processing hardware implementation in the form of a low-power SoC. A novel absolute value comparator circuit, implemented without the use of full-wave rectifier blocks and with low complexity, is also proposed to allow for absolute values of signals to be compared in parallel.

The performance of the data reduction SoC, which has been fabricated in a 0.35 μm CMOS process, is then characterized using a dataset containing 982 interictal events in over 104 hours of data from 18 patients. The SoC consumes 950 nW from a 1.25 V supply and is able to achieve a sensitivity of 87%, while transmitting 45% of the overall EEG data.

Chapter 4 - A 1.14 μW seizure selection and data reduction System-on-Chip

A data reduction SoC to select likely seizures while discarding background EEG activity in wearable EEG systems is presented in this chapter. Seizures are manifested as abnormal activity in EEG traces and may be associated with behavioural changes that affect the patients' quality of life.

By modifying a prototype seizure detection algorithm operating based on extraction and processing of the line length feature to identify seizures, the foundation for the implementation of the low-complexity analog-based data reduction SoC is achieved. An EEG dataset containing over 168 hours of recordings from 21 patients and 34 seizure events is used for testing the system performance. The SoC, which has been fabricated in a 0.18 μm CMOS process, consumes 1.14 μW from a 1.25 V supply and achieves a sensitivity of 83% while only selecting 52% of the EEG data for transmission.

Chapter 5 - A 515 nW sleep spindle detection System-on-Chip

This chapter presents an SoC to automatically detect sleep spindle events from a single channel of scalp EEG signals. Sleep spindles, which are known to play an important role on memory consolidation during sleep, are also of clinical importance since they are characteristic of a number of neurological diseases.

The operation of the proposed SoC, which is fabricated in a 0.18 μm CMOS technology, is influenced by a previously published algorithm, which used the Teager Energy Operator, together with the median frequency, to identify spindle events. A novel TEO circuit operating based on G_mC filters, and a new median frequency comparison circuit which avoids the use of a power hungry Fast Fourier Transform (FFT) implementation, are also presented in order to allow for low-power operation of the SoC. The design process and measurement results have been described in detail.

Experimental results using a dataset containing 538 spindle events in 3 hours of data from 6 patients illustrate that the SoC is able to achieve a sensitivity and specificity of 71.5% and 98% respectively, while only consuming 515 nW from a 1.25 V supply.

Appendix 7 - Optimizing simulation times in systems containing Quasi-Infinite Resistors

A simple method to reduce the amount of simulation time required for time domain simulations of biosignal processing systems is presented. The use cases of the proposed method are not limited to the SoCs presented in the main body of this thesis and can be extended to other systems containing Quasi Infinite Resistors (QIRs) and clocked circuits. The proposed method only requires the addition of an ideal resistor or an ideal switch with a pulse control voltage to the simulation setup.

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2 Wearable EEG: What is it and why is it important?

2.1 Introduction

Studying human brainwaves, which reflect the electrical activity of the brain resulting from the interaction of neurons, is important for the investigation of neurological disorders, motor and cognitive processes, and the underlying functions of the brain. The different types of EEG-based brain sensing technologies are illustrated in Figure 2.1. The electrical activity of the brain can be measured non-invasively using EEG technology, by placing electrodes on the scalp, or invasively using electrodes that are implanted intracranially. Invasive methods can be broadly sub-categorized into Electrocorticography (ECoG) and depth-EEG. In ECoG, signals are obtained by placing electrodes underneath the dura and on the surface of the brain. Depth-EEG recordings, however, are carried out using electrodes that penetrate the brain. Due to the low-pass filtering behaviour of the skull [1], EEG signals acquired invasively have higher spatial resolution, broader bandwidth, higher amplitude and less susceptibility to physiological and enviromental artefacts compared to scalp EEG signals [2]. The mentioned dissimilarities in the characteristics of the signals acquired by non-invasive and invasive EEG monitoring approaches, result in different signal processing requirements for the analysis of data obtained using the two methods.

Invasive EEG recordings are used occasionally during the pre-surgical diagnostic process for patients with drug-resistant epilepsy and, more recently, in closed-loop treatment systems for seizure suppression. However, the surgical procedure required for placing electrodes underneath the skull is not free of complications and adverse effects [3].

This thesis focuses on the use of non-invasive scalp based EEG, hereon referred to as EEG, which is also the most commonly used type of brainwave monitoring. Recorded EEG signals are evaluated as part of the diagnotic process for a number of neurological and psychiatric disorders including epilepsy, sleep disorders,

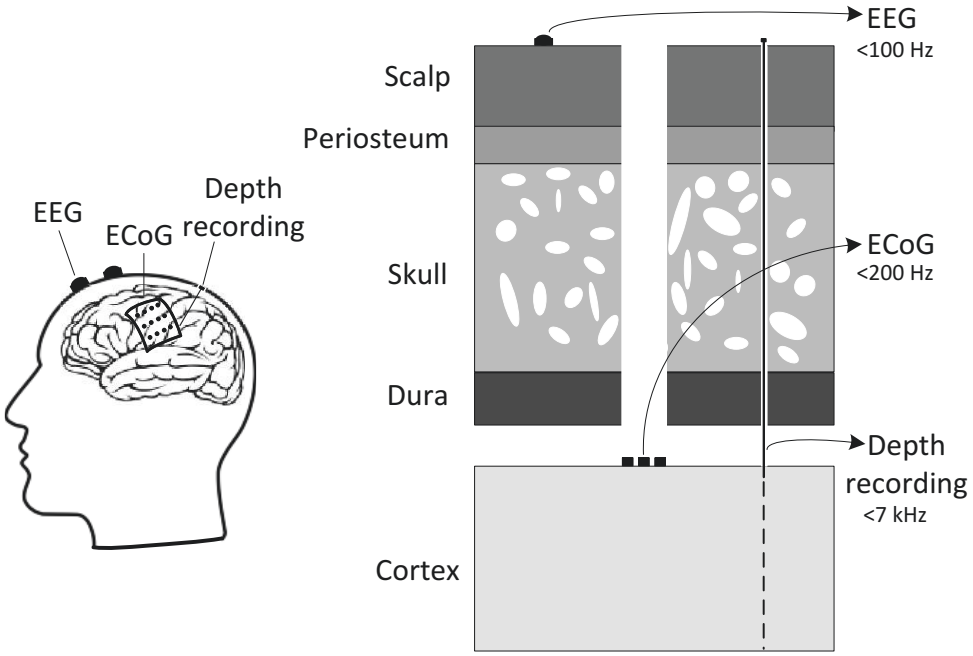


Figure 2.1: *Illustration of non-invasive and invasive brain monitoring techniques.*

dementias, brain tumours and autism [4].

This chapter begins with an overview of EEG and the characteristics of signals obtained using this technology in Section 2.2. The significant role of long-term EEG in the diagnosis of epilepsy, which is also the most common use of EEG, and sleep disorders, that consist of a broad range of disorders, is explained in Section 2.3. This explanation serves as a motivation for the development of a Wearable EEG (WEEG) system. Specific performance and power tradeoffs required for the development of WEEG systems are reviewed in Section 2.4, with reference to existing energy sources, electrode technologies, state-of-the-art data acquisition and transmission circuitry. Establishing the mentioned tradeoffs is essential from a system-design perspective, as it would allow for a lower bound to be derived for the power consumed by a WEEG system while achieving an acceptable level of performance. Section 2.5 provides a description of the different approaches to designing local signal processing nodes and their potential benefits, in terms of data and power reduction, when incorporated as part of a WEEG system for clinical applications.

2.2 EEG technology

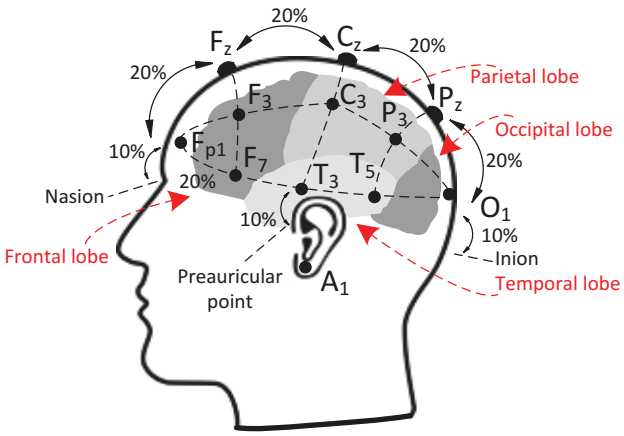
The first use of EEG on a human brain was reported in 1929 by German psychiatrist Hans Berger [5]. Ever since the discovery of EEG, this technology has played a key role in the diagnosis and diagnostic research aspects of brain disorders. Generally, EEG signals are categorized into background activity and transient events, that are relatively shorter in duration. The waveforms sensed by EEG electrodes are low amplitude (less than 150 μV) signals within the $0.5 - 60$ Hz frequency range [6]. This frequency range is further sub-divided into the following four bands:

- Delta: below 4 Hz
- Theta: between 4 to 8 Hz
- Alpha: between 8 to 13 Hz
- Beta: over 13 Hz.

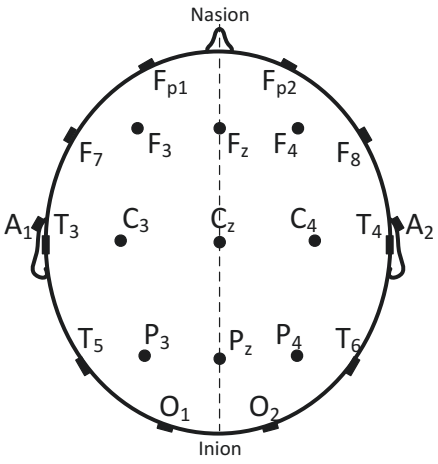
Clinical EEG setups historically include multiple electrodes in order to capture distributed potential changes across the scalp. The differences in head sizes amongst users is taken into account in the international 10-20 standard, which is usually followed for placement of electrodes. Following this standard, electrodes are positioned at fixed distances from the nasion, inion and preauricular points (left and right) in steps of 10% or 20%. An EEG setup following the international 10-20 standard is shown in Figure 2.2, with side view and top view illustrations in Figure 2.2(a) and Figure 2.2(b), respectively. The naming convention used for the electrode locations is based on a letter and number to identify the lobe and hemisphere location.

A simplified version of the setup required for EEG recordings is shown in Figure 2.3. The setup consists of two electrodes, an amplifier and a storage unit, without any assumptions regarding the implementation (analog or digital) of the storage unit. A differential structure is used in the amplifier to reduce the effect of potential common mode interference that may be coupled to the wires connecting the electrodes to the amplifier inputs, while amplifying the difference between the two signals. The following montages are possible, depending on the electrodes chosen as inputs to the amplifier (also known as an EEG channel):

- *Referential montage*: A common reference electrode is used amongst all channels, while the other electrode is used to record the activity of interest on the scalp.



(a)



(b)

Figure 2.2: *The international 10-20 standard for electrode positioning and naming in EEG recordings (based on the work of [7]): (a) Side view; (b) Top view.*

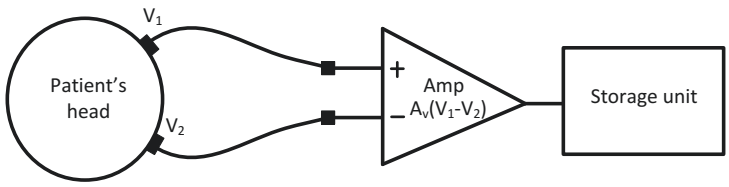


Figure 2.3: *Illustration of a two channel EEG setup consisting of two electrodes, an amplifier and a storage unit.*

- *Bipolar montage*: Each channel consists of a pair of adjacent electrodes, resulting in a series of channels each sharing electrodes with the preceding and following channels.

In the context of EEG interpretation, any electrical activity that does not originate from the brain is considered as an artefact. EEG artefacts can be divided into two main categories of physiological and non-physiological, depending on the source from which they are generated [8].

Physiological artefacts rise from activity inside the body. Artefacts produced by muscle movement, such as chewing and swallowing, can contaminate EEG signals and are characterized by high frequency activity with a power concentration over 15 Hz [9]. Changes in the electric fields around the eyes, resulting from eye movements, can also affect EEG signals. However, the effects of eye movements, such as eye rotation or blinks, are mostly observed in the frontal sites [10]. The work of [8] recommends considering alpha frequency range activity localized to the frontal electrodes as eye movement artefact, unless proven otherwise.

Non-physiological artefacts are generated by external environmental sources or faults in the recording system. The most common environmental artefact results from the alternating current (AC) in the electrical power supply lines. This noise, which is at a frequency of 50 Hz in the UK, can contaminate the EEG signal by coupling to the long wires used to connect the electrodes to the amplifier inputs in conventional recording setups. Movement of these long wires can also introduce noise in the form of low frequency and unusually high amplitude activity. In addition, artefacts may be caused by poor connections or disconnections between the electrodes and the scalp.

A series of standards for digital recording of EEG signals has been proposed by the International Federation of Clinical Neurophysiology (IFCN), in order to

reduce the effect of the mentioned artefacts on the recorded signals to ensure good quality recordings in clinical applications [11]. The standards proposed by IFCN can be summarized as:

- *Number of channels*: The system must record at least 24 channels, preferably 32 channels.
- *Sampling rate*: Minimum sampling frequency of 200 Hz. Higher rates are preferable.
- *Filtering*: A high-pass filter with a cutoff frequency of 0.16 Hz, or less, is required to remove the DC offset voltages caused by electrochemical effects at the electrode-skin interface. The use of an anti-aliasing low-pass filter with a cutoff frequency of 70 Hz and a roll-off of at least 40 dB/decade, prior to sampling, is also recommended. In addition, a notch filter (50 or 60 Hz, depending on the region in which the system is used) should be available to remove power supply noise. This filter is not routinely used in practice.
- *Digitization*: Analog to digital conversion with at least 12 bits and the ability to resolve EEG signals down to 0.5 μV.
- *Impedance levels*: The scalp-electrode impedance must be kept below 5 kΩ throughout the recording process and the amplifier input impedance should be above 100 MΩ.
- *Common mode rejection*: A Common Mode Rejection Ratio (CMRR) of at least 110 dB at the amplifier inputs.
- *Noise*: Less than 1.5 μV_{pp} and 0.5 μV_{rms} of additional noise.
- *Montage*: Recordings should be preformed using the referential montage since other montages can be subsequently reconstructed form this montage.

2.3 The role of EEG in diagnosis

2.3.1 Epilepsy

Epilepsy is a serious and common neurological disease affecting almost 1% of the world population. The known causes of this disease are genetic defects and structural conditions such as stroke, trauma and infection [12]. Epilepsy is characterized by debilitating seizure episodes, resulting from excessive and abnormal firing of

neurons in the brain, that affect the quality of life of patients. The disease affects the ability of patients to work, obtain education and enjoy a social life. Epileptic patients are typically not allowed to drive, which limits their ability to achieve a feeling of independence. The stigma associated with epilepsy can also result in lower self-esteem, depression and anxiety, weakened physical health and lower life satisfaction for sufferers [13]. The adverse effects of epilepsy are not limited to the patients' lifestyle, as the mortality rate is also 2-3 times higher among people with epilepsy than the general population [14]. In adition, there is a very high economic burden associated with epilepsy. A total cost of €20 billion per year is estimated for the 6 million people living with epilepsy in Europe [15], [16].

Despite the large number of sufferers and socio-economic implications of epilepsy, accurate diagnosis of the disease remains challenging with a significant number of sufferers being misdiagnosed. Misdiagnosis rates of 26.1% and 35% were reported in previous studies [17], [18], which were carried out on patients which were already taking anti-epileptic drugs (AEDs), subsequent to being diagnosed with epilepsy. An incorrect diagnosis can have physical, psychological and economical consequences for the patient. Restrictions on driving can result in missed employment opportunities and limit the patients ability to participate in social activities. Adverse physical effects such as neurotoxitiy can occur in misdiagnosed patients which are intolerant to AEDs. A misdiagnosis also implies that the patient is denied a correct diagnosis to the actual condition from which he/she is suffering and this can be life threatening in cases such as cardiac syncope when left untreated [19]. In addition, the misdiagnosis of epilepsy adds a significant financial burden on health services. The annual cost of epilepsy misdiagnosis in England and Wales has been estimated to reach upto £138 million [20]. This figure is only an underestimation, since it includes the total medical and community-based social services costs while excluding the costs incurred as a result of incorrect treatments and lower quality of life.

It is due to such implications of epilepsy that an accurate diagnosis of the disease is essential.

2.3.2 EEG in epilepsy diagnosis

The diagnostic process for epilepsy typically begins after the first seizure event with and urgent referral to a specialist to ensure an accurate and early diagnosis. Epileptic seizures can be mistaken with manifestations of other transient neurological symptoms such as syncope, non-epileptic seizures with psychological causes,

migraines and parasomnias, resulting in an erroneous diagnosis. Seizures can also be provoked by a number of factors including head trauma, metabolic disturbances, sleep deprivation and toxins such as alcohol [21]. Therefore, it is essential for the specialist to take a complete history of the seizure during the initial medical consultation. Information obtained from an eye-witness, if available, can be helpful for the diagnosis since the affected patient may not be able to describe the episode in detail due to unconsciousness. The specialist will obtain details about the time of day at which the seizure occurred, the duration of the seizure, events and initial symptoms leading up to the seizure and the patient's behaviour during and after the seizure. A family history will also be gathered to identify any inheritance patterns. In addition to an EEG test, which is the most important diagnostic tool in epilepsy, further investigations may also be performed to aid the diagnosis by ruling out other conditions that simulate epilepsy include brain imaging, to check for structural abnormalities, electrocardiography (ECG) tests to rule out cardiac conditions in patients with altered consciousness and genetic testing for patients with a strong family history of epilepsy [22].

The specialist will carry out an EEG test as part of the diagnostic process to identify abnormal brainwave patterns that are characteristic of epilepsy, also known as epileptiform activity. The following questions can be answered based on the obtained EEG data:

- *Is epileptiform activity present?* The presence of epileptiform activity helps to differentiate between epileptic and other non-epileptic attacks. In addition, spatial and temporal information of the observed epileptiform activity can aid in classifying seizure type.

- *Where is the epileptogenic zone?* Knowledge about the location of the epileptogenic region can be helpful in identifying the type of epilepsy. If the activity originates from networks within one hemisphere, the epilepsy is considered to be focal, while epileptiform discharges affecting networks in both hemispheres from the beginning are indicative of generalised epilepsy.

A routine EEG test lasts for 20-30 min and is carried out in an inpatient setting in order to capture epileptic EEG data. Epileptic EEG traces can be categorized into two phases of ictal (seizure activity) and interictal (spikes and spike and wave activity occurring between seizures). Seizures occur infrequently in the many patients, with 60-80% of epileptic patients having less than 12 seizures per year [23]. Therefore, due to the short duration of the test, routine EEG is more likely to capture interictal epileptiform discharges (IEDs) occurring in between seizures (also

known as interictal activity). Interictal activity is observed in 98% of patients with epilepsy, while the EEG traces of less than 4% of healthy individuals contain interictal activity [24], [25]. Despite their importance in the clinical diagnosis of epilepsy, interictal discharges are observed in approximately 50% of patients during routine EEG tests. Yield can be increased in routine EEG tests by performing multiple recordings, interpreting both wake and sleep records and utilizing seizure provoking procedures such as photic stimulation, hyperventilation and sleep deprivation. Continuous EEG recording accompanied by video monitoring is considered as the gold standard of EEG monitoring. This type of recording also requires inpatient admission and is carried out continuously over longer durations (24 hours or more). In comparison to routine EEG tests, continuous recording increases the probability of capturing epileptiform activity. However, these long-term EEG tests are not universally available due to the high cost associated with the hospitalization of patients over long periods. In addition, the task of continuous visual analysis and interpretation of the large amount of data acquired during long-term tests is also very time consuming for the specialist. Furthermore, since the test is performed in an isolated hospital setup, patients are removed from their natural environment and therefore not subjected to seizure precipitating stimuli that may be encountered during their daily life.

Alternatively, Ambulatory EEG (AEEG) recordings can be performed in the comfort of the patients home for up to 96 hours, significantly improving the diagnostic yield [26]. The cost of AEEG monitoring over a 24 hour period is estimated to be 51-65% lower than inpatient monitoring over the same duration [27]. However, AEEG devices in their current form have a number of limitations:

- *Weight and volume:* The storage units used to record EEG signals are held in place with a belt that is placed around the patient's waist or neck. These units are bulky, heavy (over 500g) and not comfortable for the patient to carry during everyday activities.

- *Electrodes:* Wet electrodes require skin preparation prior to applying conductive gel that would reduce the impedance between the electrodes and the scalp, thereby ensuring the signals acquired are of good quality. However, the gel is sticky, causing discomfort in the electrode site of the patient's head. Moreover, the gel dries out over time resulting in increased electrode impedance and degraded signal quality, requiring constant attention by medical experts to ensure good contacts

- *Connectivity:* Long wires are used to connect the electrodes to the storage

unit. The patient's movement is limited since any accidental pulling on the wires can result in electrode disconnections and signals not being recorded. Furthermore, moving the wires will reduce signal integrity by introducing atrtefacts that will be superimposed on the recorded signal. Patients are also advised not to remove the connecting belt off the body to avoid the risk of the wires wrapping around the neck causing suffocation, even when in bed, resulting in discomfort.

- *Storage:* Battery lifetime is limited (24 days) due to the power consumption required to store long-term EEG recordings. Approximately 1 GB of data is produced during a 24 hour recording period [28]. Furthermore, patients are often required to visit a specialist clinic regularly throughout the monitoring period to retrieve the recorded data.

- *Reviewing process:* The process of reviewing the recorded EEG signals by a specialist is time consuming, taking approximately 2 hours to review 24 hours of recorded data [29].

There is therefore a clear need for a non-invasive, wireless, light-weight and low-power Wearable EEG (WEEG) unit that could be comfortably worn by the patient for long periods of time.

2.3.3 Sleep studies

It is estimated that over 30% of the population in Europe, 50% in the US and 20% in Japan suffer from one or multiple sleep related problems [30]. The economic implications of sleep disorders are massive, with an annual cost of over €25 billion in Europe alone.

The main categories of sleep disorders include insomnia, sleep related breathing disorders, central disorders of hypersomnolence, circadian rhythm sleep-wake disorders, parasomnias, sleep-related movement disorders and other sleep disorders such as those caused by enviromental factors [31]–[33]. Complaints of sleep onset and maintenance problems despite adequate opportunity and circumstances to sleep, together with reports of significant impairment in daytime functions, are considered as the diagnostic criteria for insomnia. Sleep related breathing disorders are mainly characterized by abnormal ventilation during sleep. Excessive daytime sleepiness (EDS), not caused by disrupted sleep or other sleep disorders, is a characteristic feature of central disorders of hypersomnolence. The main feature of circadian rhythm sleep-wake disorders is the abnormal timing of sleep, resulting in

sleep and wake episodes occurring at inappropriate times. Parasomnias are related to abnormal sleep with behavioural manifestations that occur at the onset of sleep, during sleep or upon awakening, such as sleep terrors, sleep paralysis and sleep related hallucinations. Sleep-related movement disorders cause simple and usually stereotyped movements during sleep, resulting in disturbed sleep.

It can be noted that the negative consequences of sleep disorders are not limited to reduced sleep quality alone, since day time functionality is affected as well. Sleep disorders have major financial implications rising from loss of productivity, work related injuries, motor vehicle accidents and expensive medical costs. Workers with sleep problems have a higher risk of injury during work, by a factor of 1.62, and 13% of work injuries are attributed to sleep problems [34]. Up to 20% of fatal road crashes are caused by someone falling asleep, with an alarming 37% of drivers having reported to have fallen asleep whilst driving at least once [35]. In addition, poor quality of sleep is associated with physical and psychological impairments, with sleep disorders increasing the risk of later occurrence of depression by over twofold [36].

The sleep related parameters required for diagnosis of sleep disorders are extracted during sleep studies using polysomnography (PSG) tests. The main issue associated with diagnosing sleep disorders is the lack of diagnostic sleep clinics, which are required for monitoring patients during the PSG test.

2.3.4 EEG in sleep studies

Human sleep is a dynamic process that can be broadly divided into the two distinct stages of Nonrapid Eye Movement (NREM) and Rapid Eye Movement (REM). The NREM stage is further broken down into three separate stages of N1, N2 and N3. Sleep progresses through the NREM and REM stages in a cyclic manner 4 to 5 times during a full night's sleep, with each cycle lasting about 90 minutes. Extracting information such as duration spent in each sleep stage and the transition between different stages of sleep during sleep studies is used in the diagnostic process in order to confirm the presence of, or differentiate between, different sleep disorders.

Sleep studies are usually carried out in specialized sleep clinics overnight with the help of trained specialists. A PSG setup may include the monitoring of brainwaves using EEG, eye movements through Electrooculography (EOG), heart rhythm via Electrocardiography (ECG) and muscle activity using Electromyography (EMG). Additional sensors may be utilized to monitor breathing related parameters or body movements.

While the number of sensors utilized in sleep studies may vary depending on the type of sleep disorder under investigation, the three common types of neurophysiological sensors used to determine sleep stages are EEG, EOG and EMG. Following the recommendations of the American Academy of Sleep Medicine (AASM) [37], the recording of EEG signals is carried out from 3 to 6 EEG derivations inline with the naming and positioning conventions of the international 10-20 system. Eye movement activity is recorded by placing two electrodes near the left outer canthus and the right outer canthus. Bursts of rapid eye movement, which are seen during the REM stage of sleep, are mostly absent during NREM stages. Rapid eye blinks may also be observed during wakefulness, and replaced with slow eye movements as drowsiness develops. Leg movements and chin EMG are also monitored during full PSG in order to evaluate the presence of periodic limb movement disorder and to help differentiate between the Wake and REM stages and the other stages of sleep, respectively.

The gathered EEG, EOG and EMG signals are stored in a processing unit and segmented into 30 s epochs. Subsequently, a sleep stage is assigned to each epoch, using the following set of rules provided by the AASM [37]:

- *Wake (W):* An epoch is scored as W if more than 50% of the EEG activity can be visually identified as alpha rhythms. Rapid eye blinks, reading eye movements, irregular eye movements associated with chin muscle activity are used to score an epoch as W when visually discernible alpha activity is not present. In addition, an epoch is scored as W if major body movements are present and the preceding or following epoch is also scored as W.

- *Stage 1 of NREM (N1):* An epoch is scored as N1 if alpha rhythm is attenuated (occupying less than 50% of the epoch) and replaced with mixed frequency, low amplitude activity for more than 50% of the epoch. Activity in 4-7 Hz range, vertex sharp waves and slow eye movements are indicative of stage N1 when alpha rhythms are not present.

- *Stage 2 of NREM (N2):* Appearance of sleep spindles and/or K complexes, which are both characteristic events related to sleep, are used to score an epoch as stage N2. Sleep spindles are defined as a train of distinct waves within the 11-16 Hz (most commonly 12-14 Hz) frequency range and a duration of over 0.5 s. A K complex is defined as a negative sharp wave followed by a positive component that is distinguishable from background EEG, with a total duration greater than 0.5 s.

- *Stage 3 of NREM (N3):* If 20% or more of an epoch consists of waves with amplitudes larger than 75 μV_{pp} within the 0.5-2 Hz frequency range, it is scored as N3.

- *REM:* An epoch is scored as REM if low amplitude mixed frequency activity is observed in the EEG, together with rapid eye movements in EOG data and low chin EMG activity.

Sleep studies, when performed in a clinical setting, suffer from a number of limitations. The manual analysis and marking of a full night recording (8 hours) is a laborious task, taking between 2 to 4 hours [38]. Furthermore, full night PSG is expensive and uncomfortable for patients since they are removed from their natural living enviroment, and is associated with very long waiting times. It is estimated that the demand for PSG tests exceeds the supply by a factor of 50 in the UK, with waiting times of up to 2 years upon referral to a sleep clinic [39]. Home PSG (HPSG) has been developed more recently as an alternative to allow for monitoring at the patient's home. A complete HPSG setup consists of the same sensors as clinical PSG, connected to a recording unit which is placed in the proximity of the bed or wrapped around the patient's chest in the form of a belt. In principle, the shortcomings of HPSG systems are fairly similar to those of AEEG systems, used for the monitoring of epilepsy. The bulky recording units and large number of wires connecting the electrodes to the recording unit can cause sleep disruption. In addition, specialist review of the large amount of data stored on the recording device remains an issue in HPSG systems. Although the active operating periods of HPSG systems is tied to the patient's sleep duration, the typical battery lifetime of less than 24 hours in these systems requires regular recharging or battery replacement which can be a burden to the patient and/or medical professionals.

It is therefore evident that minimizing the number of sensors in PSG systems is desirable in terms of comfort and convenience of both patients and medical experts. A lower channel count would also lead to reductions in the overall system size, power consumption and amount of data to be reviewed, all of which result in a better user experience. No significant difference in PSG scoring reliability was observed in the work of [40], when using a single channel of EEG. More recently, the authors of [41] reported the use of a single channel of EEG to detect the REM stage of sleep, thereby obviating the need for additional EMG and EOG sensors. The aforementioned studies illustrate the potential for performing complete sleep scoring using a single channel, light weight, low power and wireless WEEG system that can be comfortably worn by the patient during sleep.

2.4 Wearable EEG

Minimizing size, weight and power consumption while complying with medical regulatory standards, are key features that must be considered in the design of WEEG systems. A miniature device would allow for the patient to move freely and attend to routine activities while being monitoring by the system. This is particularly important in the context of medical diagnosis based on EEG signals, where, by monitoring patients in their own environment, as opposed to a clinical setup, patients can be exposed to stimuli that would provoke the irregular brain activity under investigation. With regards to patient privacy, wearing a bulky ambulatory EEG device can disclose to others that the patient may be suffering from a neurological condition such as epilepsy. A compact and lightweight system, however, can be easily concealed within a hat during daily activities, allowing the patient to keep the medical investigation private.

Low-power operation of the WEEG system is essential in order to achieve long-term monitoring, without interruption, from smaller batteries limited by the mentioned size and weight considerations. Furthermore, extending the battery lifetime of the WEEG system would mitigate the inconvenience and risks associated with recharging or replacement of batteries.

This section presents the state-of-the-art with regards to the energy source, electrode configurations and data acquisition circuitry, while considering the performance requirements of a truly wearable EEG system. Subsequently, the maximum operational lifetime of a WEEG system created using current technologies has been investigated. This is followed by an introduction to the different intelligent local signal processing approaches, which can be incorporated into the WEEG system to improve the device operational lifetime, by reducing the system data rate and communication cost.

2.4.1 Energy sources

A crucial factor that must be considered during the design process of clinical-grade WEEG systems is the type of power source used for the system. In the context of system ergonomics, batteries are a dominating factor in the overall device size and, thus, the use of smaller batteries is desirable in a WEEG system. However, the lower amount of energy available in smaller batteries negatively impacts the system usability by limiting the system operational lifetime and causing inconvenience due to the need for more frequent battery or replacement procedures. Furthermore, the

health and safety consequences associated with battery replacements or recharging operations by untrained users must not be underestimated. A number of battery related scenarios that can lead to a delayed diagnosis and put the patient's safety at risk, based on the risks mentioned in the usability guidelines for medical devices provided by the International Electrotechnical Commission (IEC) [42], are listed in Table 2.1.

Harvesting energy from the environment or the user to achieve a battery-free solution to EEG monitoring has been investigated in the literature. A thermoelectric generator (TEG) was used in [43], to provide up to 2.25 mW of power to a 2 channel EEG system in the form of a headband, based on temperature differences between the user's body and the surrounding environment. The 4 channel EEG system proposed in [44] utilized a more compact TEG (4×4 cm^2), to harvest 60 μW at room temperature, when placed on user's chest. Ultra-high frequency radio frequency identification (RFID) was used to power a single channel EEG system up to a theoretical maximum distance of 2.6 meters in [45]. However, the common drawback of these systems is the non-constant and unreliable supply of energy, rendering them not suitable for use in medical applications.

Alternatively, the battery maintenance issues described earlier can be mitigated by reducing the power consumption of the WEEG system, such that the need for replacement or recharging of batteries is obviated throughout the expected system lifetime. Determining the system lifetime depends on a number of factors that are defined during the verification and validation processes required prior to manufacturing a medical device on a commercial scale, including packaging stability, anticipated material deterioration and availability of spare parts. A system lifetime of 2 years is assumed here, similar to the minimum time period that the manufacturer of a medical device is obliged by the U.S. Food and Drug Administration (FDA) to retain the documentation relating to the device, stated as ([46]):

> *"All records required by this part shall be retained for a period of time equivalent to the design and expected life of the device, but in no case less than 2 years from the date of release for commercial distribution by the manufacturer."*

In order to operate continuously for 2 years from a zinc-air battery providing 246 mWh ([47]), the average power consumed by the system must be less than 14 μW. In a more conservative approach, the authors of [48] aimed for 30 days of continuous operation from a custom made battery with 100 mWh of stored energy, resulting in a system power budget of 140 μW.

Table 2.1: *Battery related hazardous scenarios in medical devices.*

Task	Potential risk
Battery replacement	Late battery replacement (battery depletion)
	Difficult battery replacement for elderly
	Installation of incorrect battery type
	Battery installed with reverse polarity
	Accidental short circuiting of the battery
Battery recharging	Overcharging the battery
	Undercharging the battery
	Forgetting to charge the battery
	Inaccessible mains power socket

2.4.2 Electrodes

Historically, materials used to create EEG electrodes have included gold, sintered silver/silver-chloride (Ag/AgCl), platinum, tin and stainless steel. Among these materials, electrodes made of Ag/AgCl are most widely used due to their very low half cell potential (appearing as a DC voltage of approximately 220 mV [49]) resulting from the unbalanced distribution of anions and cations across the electrolyte-electrode interface, and low drift rate of 121±33 μV/min (calculated over 15 minutes) [50].

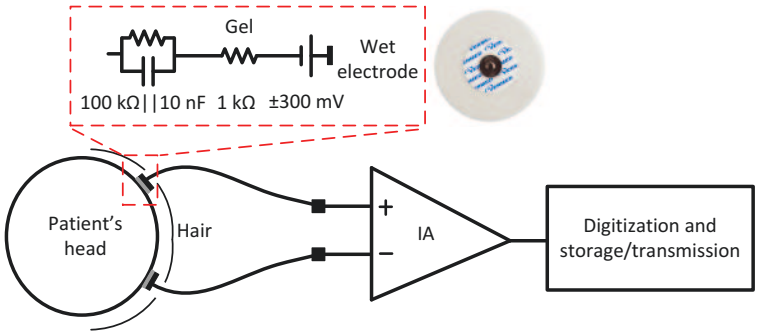
The types of electrodes used for EEG signal acquisition can be categorized as wet and dry electrodes. The electrical model of the electrode-skin interface for different types of electrodes is shown in Figure 2.4. Wet electrodes (Figure 2.4(a)), as the name suggests, require an electrolyte gel to achieve a low electrode-skin contact impedance of up to few kΩ, providing a better connection with the scalp. Nonetheless, one of the main drawbacks of current AEEG devices is the use of wet electrodes. Occasionally, skin abrasion is performed to ensure contact impedance levels below 5 kΩ (required for clinical practice [11]). This procedure increases the risk of infection as the electrodes are likely to come in contact with blood products [51]. Furthermore, the contact impedance increases overtime as the conductive gel dries out, eventually leading to signals not being recorded and requiring new gel to be applied to the scalp. A WEEG device would allow for the transmitted signals to be monitored by medical experts and patients can be asked to visit the specialist clinic when poor quality of electrode connections are observed. However, constant medical attendance of this form is resource intensive, time consuming and

ultimately, inconvenient for both patients and medical experts. The presence of gel is also uncomfortable for patients, often causing irritation, and must be washed off the hair and skin after the monitoring period.

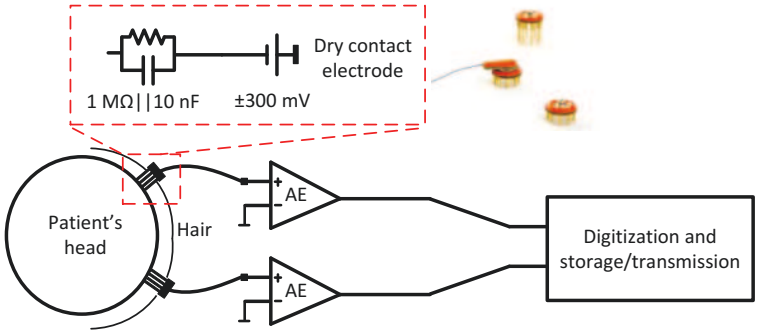
Dry contact electrodes, shown in Figure 2.4(a), alleviate these concerns by eliminating the requirement for conductive gel. Therefore, these electrodes do not require preparation of the patient's scalp which results in reduced setup time and patient comfort. The main disadvantage of dry electrodes is the increase in electrode impedance due to the elimination of the conductive gel. The higher impedance of dry contact electrodes, which is in the range of tens of kΩs up to tens of MΩs [52], results in increased susceptibility to mains noise and interference caused by movement of the lead wires. To overcome the issue of high skin-electrode impedance in dry electrodes, ongoing research is being carried out on the development of active electrodes, which are created by integrating an impedance transformer circuit (i.e. a buffer or an amplifier) onto the electrode structure [53], [57]. The effect of environmental noise on the signal sensed by active electrodes will thus be minimized due to the proximity of the active element and the electrode. Further, the low output impedance of the active element, whether a buffer or amplifier, reduces wire movement artifacts and mains interference picked up by the lead wires.

Dry contact electrodes typically include an array of rigid pins that are designed to pass through the hair and achieve better contact with the scalp, causing discomfort and pain. Therefore, flexible dry contact electrodes which are suitable for long-term EEG monitoring, have been investigated by several researchers. A dry foam-based electrode is proposed in [58], with a skin-electrode impedance of 4 kΩ to 26 kΩ, depending on the amount of hair present in the electrode site. The use of flexible silver-coated polymer bristels instead of conductive pins in order to reduce discomfort by distributing the pressure applied to the skin uniformly, was evaluated in [59]. The electrode achieved an impedance of 80 kΩ when applied to the scalp with low-to-medium pressure. The dry electrode with a multi-pin structure, reported in [60], is made of flexible polyurethane coated with Ag/AgCl and achieves skin-electrode impedance levels of below 150 kΩ.

More recently, dry non-contact electrodes such as the electrode developed by QASAR ([56]), shown in Figure 2.4(c), have been used to acquire bio-potentials through capacitive coupling without touching the surface of the skin. In theory, non-contact electrodes can allow for long-term EEG recordings over a layer of fabric such as a hat worn by the patient, making them appealing from a comfort and usability standpoint due to the explicit gap between the sensor and the skin. However, these electrodes suffer from the following shortcomings, rendering them



(a)



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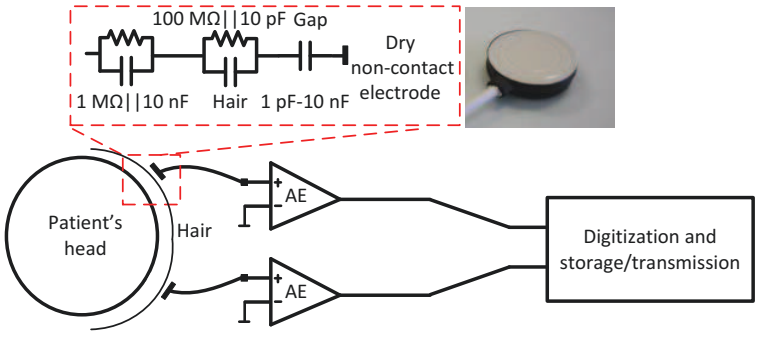


(c)

Figure 2.4: *Electrical models of the electrode-skin interface for different types of electrodes (impedance values taken from [52], [53]): (a) wet Ag/AgCl electrode (electrode image taken from [54]); (b) dry contact electrode (electrode image taken from [55]); (c) dry non-contact electrode (electrode image taken from [56]).*

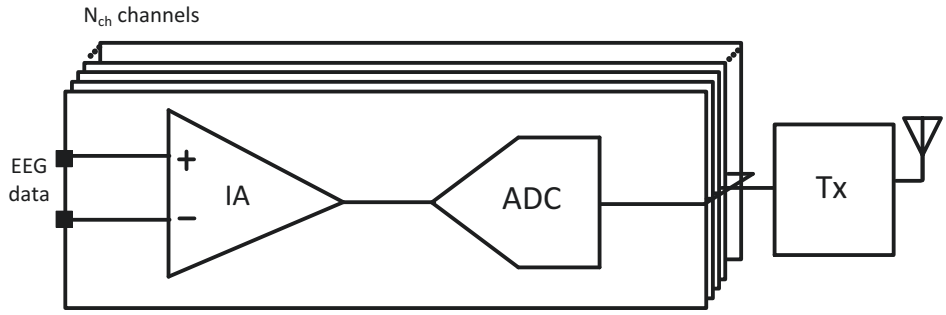


Figure 2.5: *Conceptual implementation of a WEEG system consisting of an IA, ADC and transmitter (Tx).*

unsuitable for clinical EEG applications [52]:

- Increased impedance due to the non-negligible impedance of the insulation layer (i.e. hair or cotton), which is typically in the range of hundreds of MΩs.
- Significant susceptibility to motion artefacts and long recovery times due to the high impedance, capacitively coupled, input node.
- Artefacts resulting from variations in the distance between the electrode and the patient's skin.
- Friction between the insulation layer and the electrode will generate large amplitude artefacts, leading to distortions at the sensitive input node.

2.4.3 Wearable EEG performance considerations

The EEG waves picked up by the electrodes are of low amplitude (<150 μV), with signal energy primarily below 60 Hz. The WEEG system front-end must contain a low noise Instrumentation Amplifier (IA) to scale the collected signals throughout the EEG bandwidth, together with an Analog-to-Digital Converter (ADC) that makes a digitized version of the signal available to the following transmitter module. The conceptual implementation of a WEEG system consisting of an IA, ADC and transmitter is shown in Figure 2.5. The total power consumed by the system can be calculated as

$$P_{\text{sys}} = N_{\text{ch}} P_{\text{IA}} + N_{\text{ch}} P_{\text{ADC}} + P_{\text{t}} \tag{2.1}$$

where P_{IA}, P_{ADC} and P_{t} represent the power consumed by the IA, ADC and wireless transmitter modules, respectively. The number of channels in the system is specified using N_{ch}.

Critical characteristics (e.g. input referred noise and CMRR) must be analyzed together with power consumption, in order to ensure that the tradeoffs involved to achieve lower power operation do not lead to a degraded system performance. In addition to the IFCN guidelines for clinical recording of EEG, a series of requirements for the basic safety and essential performance of EEG systems in medical applications, published by the IEC ([61]) and summarized in Table 2.2, must be noted during the review of front-end circuitry. A series of target specifications, derived based on the two sets of guidelines, have also been included in Table 2.2.

Table 2.2: *WEEG system front-end specifications.*

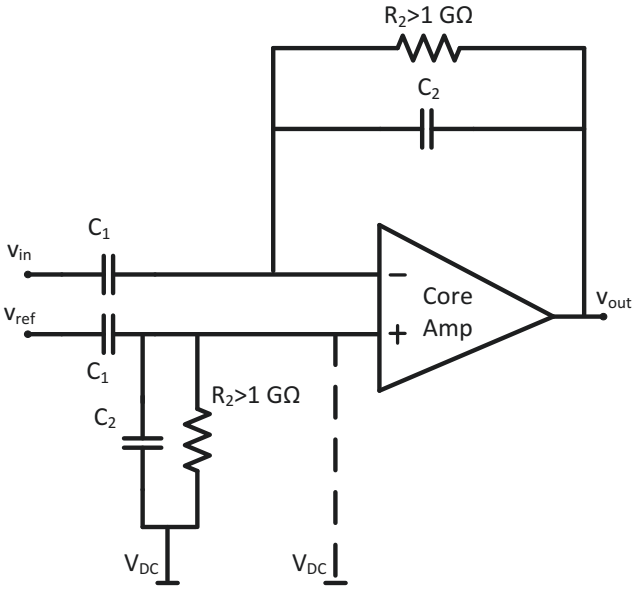
	IFCN [11]	IEC [61]	WEEG specifications
Input impedance	$\geqslant$100 MΩ	-	100 MΩ
Electrode offset tolerance	-	$\pm$300 mV	$\pm$300 mV
Input range	-	0.5 $\mathrm{mV_{pp}}$	1 $\mathrm{mV_{pp}}$
Bandwidth	0.5-100 Hz	0.5-100 Hz	0.5-100 Hz
Input referred noise	6 $\mu\mathrm{V_{pp}}$ (0.91 $\mu\mathrm{V_{rms}}$)	0.5 $\mu\mathrm{V_{rms}}$	0.5 $\mu\mathrm{V_{rms}}$
CMRR	-	$\geqslant$110 dB	110 dB
ADC resolution	$\geqslant$12 bits	-	12 bits
Sampling frequency	$\geqslant$200 Hz	-	200 Hz

The input impedance of the IA must be kept sufficiently large ($\geqslant$100 MΩ) to avoid signal attenuation due to the voltage division formed by the electrode-skin, and IA input, impedances. Furthermore, the combination of low IA input impedance together with the mismatch present between electrode impedances can lead to a degraded CMRR, particularly in the case of high impedance dry electrodes. The IA must tolerate up to $\pm$300 mV of DC offset voltages produced at the electrode-skin interface, which can otherwise result in signal distortion, or even saturation, at the IA output. With regards to IA noise, low-noise operation is essential ($<$1 $\mu\mathrm{V_{rms}}$) to ensure the low frequency and small amplitude EEG signals are not corrupted by noise during amplification. A high CMRR ($\geqslant$100 dB) is desirable to ensure that the effect of common-mode aggressors, namely supply noise (50/60 Hz) and motion artefacts, are minimized. Digitization with 12 bits and a sampling frequency of at least 200 Hz at the IA output, ensures that the entire

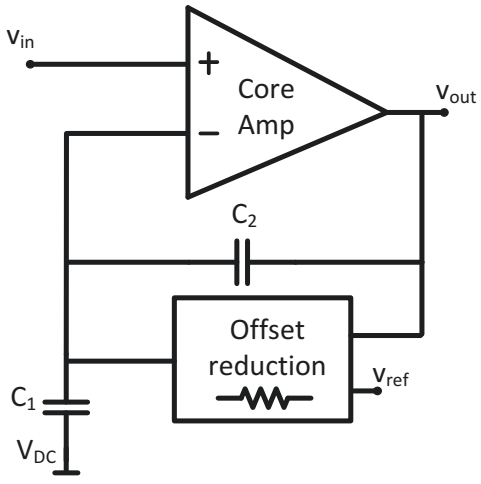
signal range is accommodated by the ADC, while avoiding errors due to aliasing during the sampling process.

The tradeoffs required to meet the mentioned specifications are highly dependent on the IA architecture. With regards to the input configuration, the two common architectures utilized in EEG IAs are shown in Figure 2.6. An AC coupled inverting IA is illustrated in Figure 2.6(a) and used in the works of [62]–[64]. The active electrode of [65] utilizes a similar architecture, with the positive IA input connected directly to a DC common signal, as shown with a dashed line in Figure 2.6(a). A sub-hertz high-pass filtering stage to reject the electrode offset is formed by resistors R_{1-2}, implemented using integrated diode connected pseudo-resistors in [62], together with capacitors C_{1-2}. Pseudo-resistors are an appealing design choice since they are implemented with low complexity, without adding to the power consumed by the IA, while achieving very high resistance in the range tens of GΩs. However, pseudo-resistors suffer from non-linearity for large voltage swings across the device, limiting the input voltage range. Moreover, their effective resistance is highly sensitive to process and temperature variations, leading to variable low frequency behaviour of the IA. A biasing scheme reported in [66] can be used to achieve a pseudo-resistor robust to process variations with a linear range of 600 mV. Alternatively, a robust 150 GΩ resistor implemented using a series-to-parallel charge sharing switched-capacitor (SC) resistor was used for electrode offset rejection in the IA of [64] to achieve rail-to-rail offset rejection.

Capacitively coupled IAs achieve lower input impedance due to the presence of intermediary coupling capacitors (C_1 in Figure 2.6(a)) and complementary impedance boosting circuitry are typically utilized to increase their input impedance. Therefore, Non-inverting IAs are more widely used in active electrodes due to the higher input impedance resulting from the direct coupling of the input to the gates of input transistors in the core amplifier [67]–[69]. A single ended non-inverting IA with capacitive feedback is shown in Figure 2.6(b). Resistors have been used instead of capacitors in [70] to set the IA gain, however, this architectures is less popular due to the noise contribution and power consumption associated with the use of resistors. In Figure 2.6(b), electrode offset is compensated for by the means of a DC-Servo Loop (DSL), in which the low-frequency error at the IA output is sensed by an integrator and a offset correcting voltage is applied to the core amplifier. This architecture achieves up to $\pm$350 mV of offset tolerance at the cost of the added power consumption, and noise, introduced by the DSL. Current feedback DSLs have also been reported in the literature [71], [72], compensating for up to $\pm$50 mV of electrode offset and limited by the maximum correction current



(a)



(b)

Figure 2.6: *Common architectures utilized in the signal amplification stages of EEG systems: (a) AC coupled inverting amplifier; (b) non-inverting IA with capacitive feedback and DSL.*

supplied through the feedback loop.

Large sized input transistors have been used in [62], [63] to minimize the intrinsic flicker ($1/f$) noise and offset of the core amplifier. However, the increased gate area results in added parasitics leading to a reduction in the IA input impedance [53]. The literature reveals that instead, the chopping technique is utilized extensively to improve the IA noise performance. Using this technique [73], the input signal is up-modulated prior to amplification and demodulated back to the original band at the IA output. The flicker noise and offsets introduced by the core amplifier, however, are only up-modulated at the amplifier output and thereby separated from the amplified signal. Performing chopper-modulation prior to the coupling capacitor in AC coupled IAs limits the input impedance, which must be compensated for using input impedance boosting circuitry [74], [75], while enhancing CMRR by modulating mismatches between the coupling capacitors. Furthermore, chopping at this node mitigates the effect of excess noise which is generated when performing modulation at the high impedance virtual ground of the core amplifier [76].

The CMRR of the IA is also improved using the chopping technique, by minimizing the effect of intrinsic offsets resulting from mismatches in the core amplifier. Although specific to active electrodes, the achievable CMRR can be limited by mismatch in electrode impedances and IA gains, since common-mode aggressors are converted into differential-mode noise as a result of these non-idealities. High input impedance active electrodes are key in reducing the effect of electrode mismatches. Chopping between active electrodes to eliminate the effect of gain mismatches is not practical since these electrodes are inevitably placed on individual PCBs and different locations of the scalp. The solutions to top-level CMRR enhancement include the use Driven-Right-Leg (DRL [77]), Common-mode Feedback (CMFB [65]) and Common-mode Feedforward (CMFF [68]) methods. Common-mode gain is reduced in the DRL method by feeding the common-mode signal sensed by the amplifiers back to the patient's body through a separate biasing electrode, effectively improving CMRR resulting from both electrode impedance an gain mismatches. In the CMFB scheme, the IA output common-mode levels are averaged and fed back to the amplifier input, thereby reducing the CMRR degradation due to gain mismatch. Instability issues that may occur due to the feedback loops in DRL and CMFB methods are avoided in the CMFF scheme, in which the input common-mode signal is capacitively coupled to the IA input, via a low output impedance buffer, prior to amplification.

With regards to analogue to digital conversion, low-power ($<1\mu$W) successive-approximation-register (SAR) ADCs are widely used among EEG front-ends due

to their suitability for low sampling rate (up to hundreds of kS/s) and medium resolution (∼12 bits) applications [78]. On the system-level, the actual sampling rate of the ADC is dependent on the positioning of this block with respect to the individual IAs. The ADC is typically placed after the IA and sampled at 0.25-2.5 kHz, exceeding the 200 Hz sampling rate recommended by [11]. Alternatively, the outputs of multiple IAs can been multiplexed to a single ADC operating at a higher sampling rate, optimizing the overall system area ([67], [72], [74], [79]).

The performance of state-of-the-art EEG front-end circuits reported in the literature has been summarized in Table 2.3. Considering the mentioned tradeoffs required to obtain an acceptable performance for a WEEG system, the front-end presented in [64] closely follows the specifications of Table 2.2, while consuming 3.7 μW per channel.

Table 2.4 summarizes the performance of various state-of-the art low-power transceivers. Based on the values of energy used per bit transmitted (e_t) for the commercially available CC2500 [84] and nRF24L01+ [85] transmitters, 40 nJ/bit is taken as a conservative figure, achievable over most wearable environments for short-range communication. A lower bound of 10 nJ/bit has been considered for e_t based on the performance of the Bluetooth low energy CC2640R2F [86] and the recently published works of [87] and [88], which are comparable to the mentioned commercial transmitters in terms of transmitter output power and data rate.

From a system-level perspective, the overall power consumed by the wireless transmitter (P_{t}) is dependent on front-end data rate and is derived as

$$P_{\mathrm{t}} = N_{\mathrm{ch}} f_{\mathrm{s}} R e_{\mathrm{t}} \tag{2.2}$$

where R is the ADC resolution in bits. Based on the mentioned figures for e_t, to continuously transmit 32 channels of EEG data (sampled at 600 Hz with 12 bit resolution inline with [64]) for the diagnosis of epilepsy [11], the transmitter would consume 9.2 mW in the conservative case, and 2.3 mW, if the lower bound for e_t is considered. In the case of a 3 channel WEEG system for diagnosis of sleep related disorders [37], the power consumed by the transmitter is reduced to 863 μW and 216 μW, for the conservative and lower bound figures of e_t, respectively.

The absolute minimum power consumed by the overall WEEG system (P_{WEEG}) can be calculated using Equation 2.2 with 3.7 μW as the front-end power ($P_{\mathrm{IA}} + P_{\mathrm{ADC}}$) together with 2.3 mW and 216 μW for P_{t}, as 2.4 mW and 227 μW for the 32 channel and 3 channel systems respectively. The mentioned figures for P_{WEEG} indicate that the 32 channel system can run for 107 hours (over 4 days) on a typical

Table 2.3: *Performance summary of EEG front-end circuits available in the literature.*

Reference	Year	Supply voltage (V)	Input Impedance (GΩ)	Max. Offset rejection (mV)	Input referred noise (μV_{rms})	CMRR (dB)	ADC	Power per channel (μW)
[62]	2003	5	N/A	N/A	1.6 (DC-30 Hz)	86	No	0.9
[80]	2005	3	N/A	N/A	0.86 (0.3-150 Hz)	117	No	1450
[81]	2006	5	1000	±250	7.49 (0.001-1 kHz)	78	No	7500
[71]	2007	3	N/A	±50	0.41 (0.5-40 Hz)	120	No	60
[72]	2008	3	1	±45	0.59 (0.5-100 Hz)	120	11-bit SAR	25
[63]	2009	1	N/A	N/A	2.5 (0.05-460 Hz)	71.2	12-bit SAR	0.45
[70]	2009	3.3	N/A	Rail-to-rail	2.4 (0.5-100 Hz)	90	16-bit	600
[64]	2010	1	0.7	Rail-to-rail	1.3 (0.5-100 Hz)	60	12-bit SAR	3.7
[82]	2011	3	N/A	N/A	0.9 (0.5-100 Hz)	105	No	1000
[65]	2011	1.8	0.1	Rail-to-rail	1.2 (0.5-100 Hz)	82	No	20
[74]	2013	1.8	0.5	±200	0.91 (0.5-100 Hz)	90	10-bit SAR	8.4
[79]	2013	1.2/3.3	0.235	±300	0.82 (1-100 Hz)	101	12-bit ΣΔ	15000
[67]	2014	1.8	1.2	±250	1.75 (0.5-100 Hz)	84	12-bit SAR	82
[69]	2015	3	0.1	N/A	0.56 (0.5-100 Hz)	64	No	360
[68]	2015	1.8	0.1	±350	0.65 (0.5-100 Hz)	102	12-bit SAR	104.4
[75]	2017	0.2/0.8	0.1	N/A	0.94 (DC-670 Hz)	85	No	0.79
[83]	2017	1.255	1	NA	3.75 (0.5-45.5 Hz)	77.6	No	42

light-weight (0.58 g) hearing-aid battery with an energy capacity of 246 mWh [47], while the operational lifetime of the 3 channel system will be 1051 hours (44 days) from the same battery.

It is therefore clear that the WEEG system power consumption will be dominated by the transmitter, due to the continuous transmission of raw EEG signals. The next section looks at possible solutions for reducing the power consumed by the transmitter, and thereby improving the system operational lifetime, while simultaneously reducing the amount of time required by medical experts to review the transmitted data.

Table 2.4: *Summarized performance summary of state-of-the-art transceivers.*

Reference	Data rate (Mb/s)	Max. Tx power (dBm)	Power consumption (mW)	Energy per bit (nJ/b)
[84]	0.5	1	38.7 (1.8 V)	77.4
[85]	1	0	21.5 (1.9 V)	21.5
[86]	1	5	11 (1.8 V)	11
[87]	0.1	-6	0.89 (1 V)	8.9
[88]	1	-4.4	4.5 (1 V)	4.5

2.5 Local signal processing

The use of signal processing algorithms to support medical diagnosis, based on EEG signals, has been investigated since the 1970s [89]. Historically, the signal processing algorithm would be implemented in the software domain and run on a dedicated processing unit, placed near the patient and connected to the patient through a wired connection. The main aim of using the algorithm would be to assist on the tedious task of identifying clinically relevant events, by automatically detecting the presence or absence of such events in the recorded EEG data. The same approach can be applied to WEEG systems, by continuously transmitting the EEG data acquired by the sensor node to the receiver. The received signals would then be fed to the detection algorithm on the receiving side and results would be presented to medical experts. The computational complexity of the algorithm is not a primary concern in this type of EEG signal processing, due to the high computational power available in receiver-side processing units such as smartphones or desktop computers. However, the continuous data transmission required for this

approach imposes the previously mentioned limitations on the operational lifetime, size and weight of the WEEG system.

In the context of medical diagnosis, a more recent trend is to continuously process the EEG data using a local signal processing (LSP) module, implemented on the sensor node. In this approach, the transmitter would be required to either transmit sections of raw EEG data identified by the LSP block, or transmit the outputs of the LSP block directly, both of which result in a lower data rate and power consumption. The SoCs designed in this thesis operate as LSP modules to aid the diagnosis of epilepsy and sleep disorders. Depending on the end interpreter of the EEG data, LSP stages can be divided into two main categories of data reduction and event detection.

In data reduction, clinical interpretation of the EEG signals is generally performed by a medical expert on the receiving end. The following three methods are commonly used to achieve data reduction ([28], [90]):

- *Reducing the quality of recordings:* The data rate can be reduced by transmitting raw EEG signals with a lower channel count or number of bits.
- *Data compression:* The transmission data rate can be reduced by compressing the raw EEG data using data compression schemes such as compressive sensing [91].
- *Data selection:* The duration of the transmitted data, and thus the data rate, can be reduced by only selecting the clinically interesting sections of EEG data for transmission while rejecting background activity.

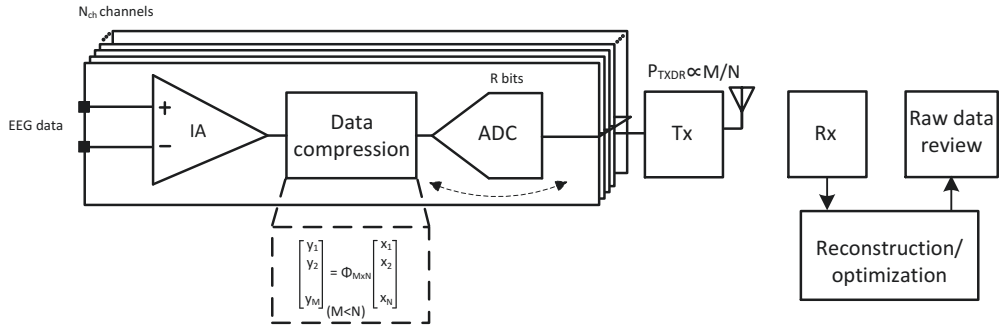
Regardless of the analog or digital nature of the implemented data reduction algorithm, the total power consumed by the WEEG system as a result of incorporating this stage, with no other modifications on the system-level, becomes:

$$P_{\mathrm{WEEG}} = NP_{\mathrm{IA}} + NP_{\mathrm{ADC}} + P_{\mathrm{DR}} + P_{\mathrm{TXDR}} \tag{2.3}$$

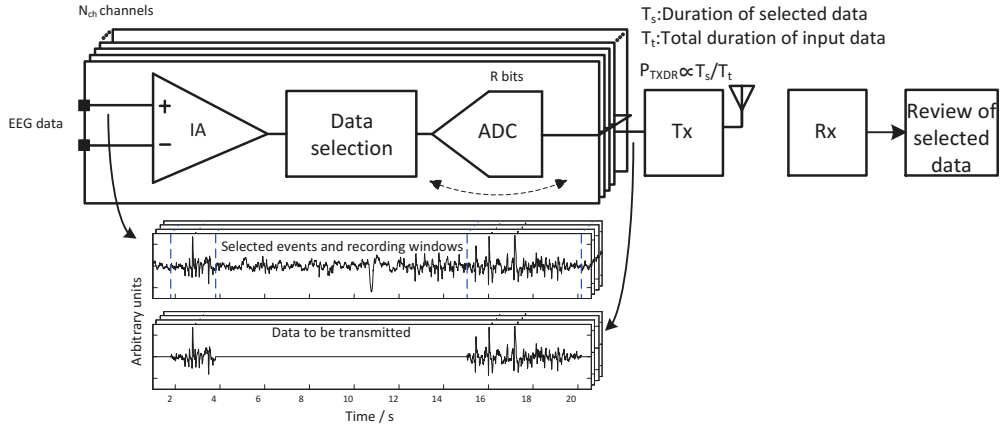
where P_{DR} is the power consumed by the data reduction algorithm and P_{TXDR} is the power consumed by the transmitter as a result of the data reduction factor (C_{DR}) applied, i.e. the fraction of data transmitted, as

$$P_{\mathrm{TXDR}} = C_{\mathrm{DR}} P_{\mathrm{TX}}. \tag{2.4}$$

Based on Equation 2.3 and Equation 2.4, in order for the incorporation of the data reduction stage to be advantageous in terms of reducing the overall WEEG



(a)



(b)

Figure 2.7: *Illustration of data reduction methods: (a) Data compression in the form of compressed sensing; (b) Data selection.*

power, the following inequality must be satisfied:

$$P_{\mathrm{DR}} < (1 - C_{\mathrm{DR}})P_{\mathrm{TX}}. \tag{2.5}$$

Reducing the number of channels or bits can be achieved in WEEG systems without adding any power consuming circuitry to the system ($P_{\mathrm{DR}} = 0$). For example, a 2 channel EEG system was developed in [43] to allow for continuous operation from the power produced by a TEG module. However, since the intention is for medical experts to visually analyse the data when utilizing data reduction schemes, reducing the quality of transmitted signals in this form can negatively impact the

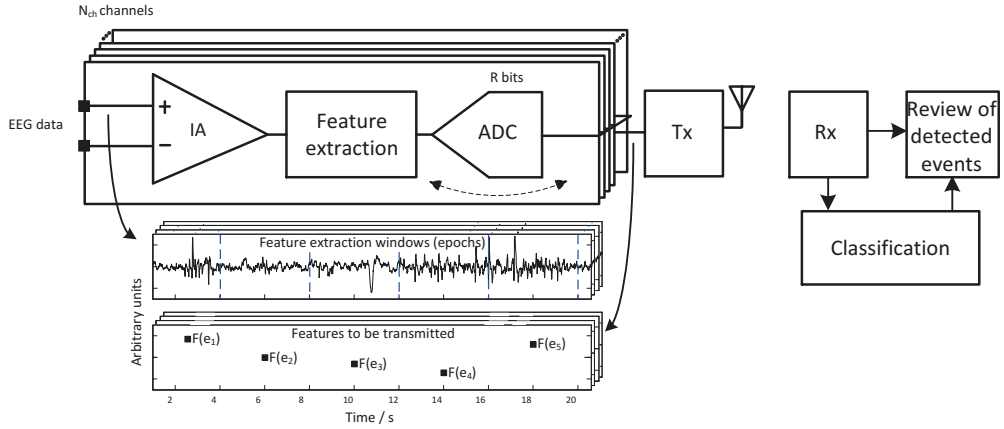
diagnosis due to the loss of clinically important information. Prior knowledge of the signal is utilized in the compressed sensing scheme, which is a lossy data compression scheme, to reduce the effective sampling rate of the acquired EEG signals prior to transmission, with the potential for a low-power hardware implementation (Figure 2.7(a)). However, reducing the reconstructed signal degradation remains an open challenge in this data reduction approach [91]. Furthermore, data compression techniques do not reduce the amount of time required for reviewing the transmitted data or provide decision support, since the entire recording duration is reconstructed at the receiving side and presented to medical experts.

Utilization of the data selection approach allows for the power consumed by the transmitter and analysis time to be reduced simultaneously. Power savings can be achieved since the transmitter is only required to discontinuously transmit sections of raw EEG data, identified by the data selection stage, with a higher probability of clinical significance (see Figure 2.7(b)). Although the amount of data transmitted and analysis time is reduced using this method, the final decision on the clinical significance of the transmitted data is made by the the neurologist and not the algorithm. This form of LSP is used as the foundation for the interictal spike and seizure selection SoCs presented in Chapter 3 and Chapter 4 to aid the diagnosis of epilepsy.

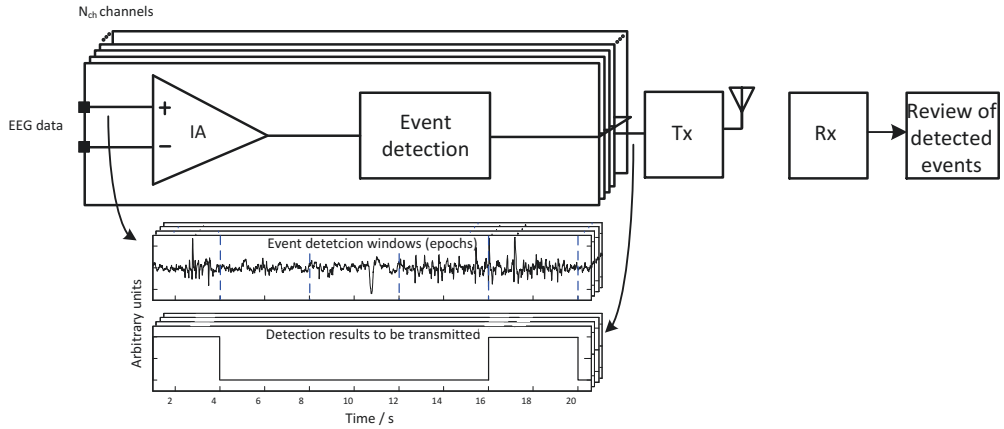
In the event detection approach, the algorithm is ultimately responsible for detection of clinically significant events in the acquired EEG data, as opposed to the medical expert. The two main stages of event detection are feature extraction and classification. Relevant characteristics of raw EEG signals, such as amplitude or power, are extracted by the feature extraction stage and passed to the classification stage for interpretation. An advantage of this form of LSP is that the system data rate can be reduced significantly compared to raw data transmission, since the data rate required to transmit features or detection results are much lower than that of raw EEG signals. With regards to the amount of processing performed on the sensor node, the two common approaches in the literature are:

- *Local feature extraction:* Features are extracted locally on the sensor node and classification is performed on the receiver side. The communication data rate is reduced by transmitting extracted features rather than raw EEG data.

- *Complete event detection:* Feature extraction and classification are performed locally on the sensor node and only classification outputs, which can be represented in fewer bits, are required to be transmitted.



(a)



(b)

Figure 2.8: *Illustration of event detection performed on the sensor node: (a) Local feature extraction; (b) Complete event detection.*

In the case of local feature extraction, shown in Figure 2.8(a), the power budget allocated for on-node processing is dedicated solely to extracting features and classification is performed on the receiving side. The reduction in the communication load is limited by the number and types of extracted features and the time window over which features are calculated. Nonetheless, local feature extraction has been carried out on EEG signals in the literature, mainly in the form of band power extraction, allowing for the transmitted features to be analysed for the presence of neurological diseases ([64], [92]) and sensorimotor functions ([44], [93]).

The number of transmitted bits in complete event detection nodes (Figure 2.8(b)) depends on the target application of the algorithm. For example, the presence or absence of epileptiform activity can be shown using a single bit ([94]–[96]), i.e. a detection as '1' and '0' if no detection occurs, whereas performing complete sleep staging on the sensor node would require the transmission of at least three bits [97]. The sleep spindle detection SoC presented in Chapter 5, designed to aid the diagnosis of sleep disorders, is based on this form of on-node event detection.

Considering a WEEG system incorporating an event detection block with a data rate reduction factor of C_{ED}, implemented in the digital domain, the system power calculations follow the general form of the analysis provided earlier with regards to data reduction, arriving at an upper bound for the power consumed by the event detection (P_{ED}) block as:

$$P_{\mathrm{ED}} < (1 - C_{\mathrm{ED}})P_{\mathrm{TX}}. \tag{2.6}$$

The use of high resolution ADC would be avoided when performing feature extraction in the analog domain, since the outputs of the classification stage, which are digital by nature, can be sent to the transmitter directly. In this case, Equation 2.6 will be modified to:

$$P_{\mathrm{ED}} < (1 - C_{\mathrm{ED}})P_{\mathrm{TX}} + P_{\mathrm{ADC}}. \tag{2.7}$$

Ideally, the power consumed by the data reduction (P_{DR}) and event detection (P_{ED}) blocks should be orders of magnitude lower than the calculated boundaries, in order to allow for the realization of true system-level power savings. This stringent power budget restricts the type of signal processing performed on the sensor to algorithms with low computational complexity.

2.6 Summary

Epilepsy and sleep disorders are serious neurological conditions affecting the daily life of millions of patients globally. The negative aspects of these conditions were

discussed in this chapter, prior to discussing the importance of EEG technology and its role in the diagnosis of these diseases. In order to be diagnosed, patients are often required to be admitted to specialized clinics for an EEG test to be carried out. This process is not only inconvenient and uncomfortable for patients, but also adds a significant financial burden to healthcare services. Ambulatory EEG devices, which were developed with the promise of portable EEG monitoring in the comfort of the patient's home, also have a number of serious shortcomings including their bulkiness and short operating lifetime. Both of these issues are a result of the power consumption of electronic blocks in these devices.

Following a detailed explanation of the potential benefits and shortcomings of conventional EEG monitoring methods, the feasibility of designing a low-power, light-weight and wireless system for long-term EEG monitoring was investigated. The system size and weight are dominated by the battery since larger batteries can store more energy. Thus, a smaller battery can be used by minimizing the power consumed by the electronic components in the wearable EEG system. Subsequent to defining the target power budget available to the system, the state-of-the-art with regards to electrode technologies and electronic blocks required for data acquisition and transmission were reviewed, with emphasis on the system-level tradeoffs required to realize a wearable EEG system suitable for long-term monitoring in clinical applications. It was highlighted that, considering the state-of-the-art of Instrumentation amplifiers (IAs), Analog-to-Digital Converters (ADCs) and wireless transmitters, the total power consumed by a wearable EEG system created using these components and continuously transmitting the acquired EEG signals will be governed by the transmitter, due to the power hungry nature of this block.

Considering the aim of long-term wearable EEG monitoring, different approaches to implementing signal processing algorithms on the sensor node were then discussed. The different types of algorithms were broadly categorized and explained, based on the power savings resulting from the algorithm implementations, and the end interpreter of the gathered EEG signals.

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3 A 950 nW interictal spike selection and data reduction System-on-Chip

The research presented within this chapter is an edited version of research previously published in:

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S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE International New Circuits and Systems Conference (NEWCAS), Vancouver, Jun. 2016, pp. 1-4, © IEEE.

3.1 Introduction

Seizures occur infrequently in many epileptic patients, with the majority of patients having less than 12 seizures a year. Epileptiform activity occurring in-between seizures, also known as interictal activity, occurs more frequently than seizures with 50% of patients with epilepsy presenting interictal discharges in their first routine EEG test.

Analysing sections of data containing interictal activity can help to confirm the diagnosis of epilepsy [1]. In addition, the character and location of interictal EEG helps to localize the epileptogenic region of the brain. Monitoring interictal epileptiform activity is also important in terms of epilepsy management, as the presence of this type of activity indicates a higher risk of seizure recurrence after a first unprovoked seizure [2].

Interictal EEG activity consists of three main forms of patterns, with the following clear descriptions provided by the IFCN ([3]):

- *Spike*: *"A transient, clearly distinguished from background activity, with pointed peak at a conventional paper speed or time scale and a duration from 20 to under 70 ms, i.e. 1/50-1/15 s, approximately. Main component is generally negative relative to other areas. Amplitude varies." [3].*

- *Sharp wave: Similar to the description of spikes, with the difference of duration, which is 70-200 ms for sharp waves (over 1/4-1/5 s approximately).*

- *Spike-and-slow-wave*: *"A pattern consisting of a spike followed by a slow wave." [3], where a slow wave is defined as "Wave with duration longer than alpha waves, i.e. over 1/8 s." [3].*

All mentioned types of interictal epileptiform activity are hereon collectively referred to as spikes.

This chapter presents a low-power scalable data reduction SoC, fabricated in a 0.35 μm CMOS technology, that would continuously select sections of data containing likely interictal activity present within EEG traces. To the best of the author's knowledge, this is the first on-chip implementation of a complete interictal spike selection algorithm and, as a result, a literature review on previously published interictal spike selection SoCs would not be possible. Instead, published interictal activity detection algorithms, implemented in software, have been reviewed in Section 3.2 and their suitability for an on-chip implementation has been accessed. An interictal spike selection algorithm with low complexity which serves as a foundation for the presented SoC, is then described in Section 3.3. This is followed by the architecture of the system together with a detailed explanation of the individual circuits used in the system in Section 3.4. The system front-end and biasing circuits have been presented in Section 3.5, followed by the measured performance results of the fabricated chip, that are presented in Section 3.6.

3.2 Interictal spike detection

Research on software implementations of automated interictal activity detection algorithms has been carried out since the 1970s. The main aim of the published literature has been to reduce the burden of visual EEG analysis for neurologists, while alleviating inter-rater and intra-rater inconsistencies that may occur during manual interpretation [4]. A detailed review on published interictal spike detection algorithms in the literature, up to 2009, was performed in [5].

In [6], a sensitivity of 90% has been considered as an acceptable baseline for the performance of an interictal spike detection algorithm used in clinical diagnosis. Inline with this assumption, the review presented here covers spike detection algorithms published up to 2017 (including the works reviewed in [5]) that achieve a sensitivity above 90%. The detection methods used and reported performance of algorithms achieving this level of sensitivity is summarized in Table 3.1. Due to inconsistencies in the cost metrics reported among automated spike detectors in the literature, the specificity, selectivity and number of false positives per minute (FP/min) corresponding to each of the reviewed publications have been included in Table 3.1. Furthermore, considering the complexity of the algorithms published in the literature, only a brief description of the detection methods used in these algorithms has been presented here and the interested reader is referred to the individual works of Table 3.1 for a detailed explanation of the methods used.

Artificial neural networks (ANNs) are widely used among the works of Table 3.1 to recognize patterns of interictal spikes, with reported sensitivity figures of up to 97%. ANNs are trainable classifiers, and, are particularly useful in cases where large training datasets are available. The training process can be carried out by feeding raw EEG signals as input data to the ANN. This approach was used in the work of [10], which achieved a sensitivity and selectivity of 94% and 93% respectively. Alternatively, the ANN can be trained using pre-extracted EEG features rather than raw EEG data, reducing the data load on the network. The automatic spike detector of [7] achieved a sensitivy of 94.2% and selectivity of 79.1%, by extracting time domain information regarding signal polarity and rate of change in signal amplitude around spike peaks and feeding these features to an ANN. Morphological features, including signal amplitude and half wave durations around spike peaks, were also extracted prior to classification using an ANN in [14], leading to sensitivity, specificity and selectivity figures of 94.1%, 95.8% and 87.5%, respectively. The use of features derived from the wavelet transform, as inputs to the ANN, has been investigated in [8], [9], [11]. The continuous wavelet transform (CWT) was applied to the input signal prior to the ANN in the work of [8], which reported a sensitivity of 90.8% and a specificity of 93.2%. The work of [9] employed the discrete wavelet transform (DWT) and ANN for feature extraction and classification, together with a set of rules mimicing the knowledge and experience of an expert marker (also known as an expert system), which have been applied to the single channel ANN outputs. The expert system is used to produce a final classification result by combining the spatial and temporal information of individual EEG channels with the ANN output, thereby reducing false detections caused by

Table 3.1: *Summarized performance of published interictal spike detection algorithms.*

Reference	Year	Detection method*	Sens. (%)	Spec. (%)	Sel. (%)	FP/min
[7]	1992	Morphological features & ANN	94.2	N/A	79.1	1.5
[8]	1995	CWT & ANN	90.8	93.2	N/A	N/A
[9]	1997	DWT & ANN & ES	97	N/A	89.5	N/A
[10]	1998	ANN	94	N/A	93	N/A
[11]	2002	CWT & ANN & ES	90	N/A	93.6	N/A
[12]	2008	PCA & Template matching	92	N/A	77	N/A
[13]	2008	DWT	91.7	89.3	78.1	N/A
[14]	2009	Morphological features & ANN	94.1	95.8	87.5	N/A
[15]	2011	Morphological features & ANN	90	87	N/A	N/A
[16]	2011	Expert & GA & CWT	96	N/A	88.8	N/A
[17]	2012	Template matching	90	N/A	89.9	N/A
[18]	2013	Template matching	90	N/A	N/A	2.36
[19]	2013	NEO & AdaBoost	94.6	89.6	N/A	N/A
[20]	2014	Template matching & SVM	95	N/A	N/A	0.24-6.6
[21]	2017	Template matching	90	85.9	66.8	N/A

* ANN, artificial neural network; CWT, continuous wavelet transform; DWT, discrete wavelet transform; ES, expert system; PCA, principle component analysis; GA, genetic algorithm; NEO, nonlinear energy operator; AdaBoost, adaptive boosting algorithm.

the presence of artifacts. This approach resulted in overall sensitivity and specificity figures of 97% and 89.5%, respectively, in [9]. A CWT, ANN and expert system were utilized in [11] to achieve sensitivity and selectivity figures of 90% and 93.6%, respectively. Other works have looked at template matching techniques to detect interictal spikes ([12], [17], [18], [20], [21]), achieving sensitivity figures up to 95%. In this approach, classification is performed based on the similarities of potential events with a template, pre-populated with marked interictal spikes during the algorithm training phase. With regards to the computation load, ANNs and template matching systems generally have high computational complexity and are not suitable for hardware implementations with stringent power budgets [22], [23].

Automatic spike detection based on DWT and adaptive thresholding was reported in [13], with a sensitivity of 91.7% and specificity of 89.3%. Although algorithms based on DWT could potentially be more power efficient than those based on extracted time domain features or ANNs, a low power implementation of the DWT reported in [24] (not specific for epilepsy) consumed 26 μW, which is almost double the WEEG system overall power budget of 14 μW, calculated in Chapter 2. More recently, the combination of Genetic algorithms (GA), CWT and thresholding were utilized to identify spikes in the work of [16], which achieved a sensitivity of 96% and selectivity of 88.8%. The GA was used in [16] to find an optimized wavelet basis function based on the morphology of marked interictal spikes present in the training data. However, the large number of GA iterations required to find an optimum solution can be time consuming, resulting in significant delays in the diagnosis.

In addition to the computational complexity of the mentioned works, the complex training process required to achieve an acceptable performance is another shortcoming of the literature reviewed in Table 3.1. The interictal spike detectors of Table 3.1 (except the works of [13] and [16]) rely on large amounts training data in order to accurately identify spikes, with may be costly and difficult to obtain.

3.3 Data selection algorithm

The data reduction algorithm used as a foundation for the spike selection SoC presented in this chapter utilizes the Continuous Wavelet Transform (CWT) to select candidate interictal spikes [6], [25]. The operation of the algorithm implemented in this work is based on the CWT at two different scales together with a threshold, as shown in Figure 3.1. The CWT operation is based around a mother wavelet $\psi(t)$, which extracts signal frequency content at a particular time. The CWT of a signal

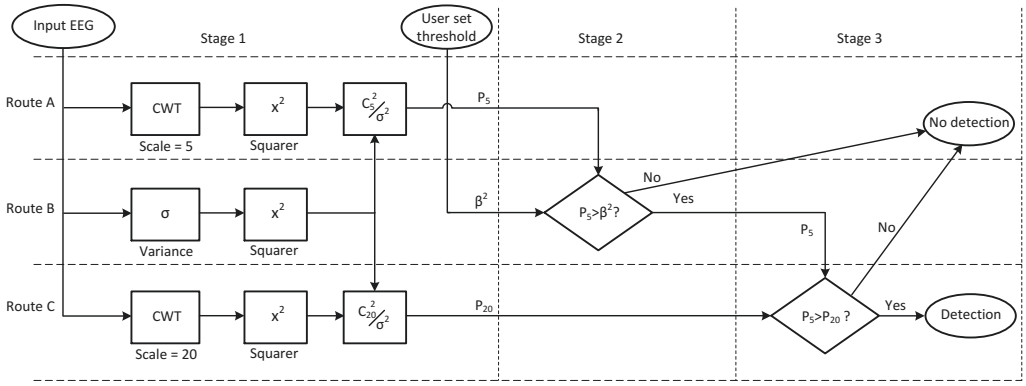


Figure 3.1: *Detailed operation of interictal spike selection algorithm. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

$x(t)$ is given by:

$$W(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t)\psi^* \left(\frac{t-b}{a}\right) dt \tag{3.1}$$

where ψ^* is the complex conjugate of the mother wavelet, a is the analysis scale and b is the time at which the transform is performed. Scales 5 and 20 are used for the CWT and amongst the different choices of mother wavelets available, the Mexican hat mother wavelet (defined as Equation 3.2) has been chosen due to its proven suitability for studying epileptic events [26], [22].

$$\psi(t) = \frac{2}{\pi^{1/4}\sqrt{3}}(1-t^2)e^{-t^2/2} \tag{3.2}$$

After calculating the CWT (Figure 3.1), the normalised wavelet powers are evaluated to account for interpatient and intrapatient changes in EEG amplitude. The EEG signal variance (σ), needed for this, is calculated over pre-defined time intervals. The normalization process allows for a fixed threshold to be used in the algorithm, regardless of the input EEG amplitude.

Possible interictal spikes are identified with the help of thresholding. An event is chosen as a potential interictal spike if the wavelet power at scale 5 (P_5) is greater than a user set threshold ($\beta^2 = \{0.1\text{-}0.9\}$). The wavelet power at scale 20 (P_{20}) is added as a rule to reject artifacts.

The algorithm in the form of Figure 3.1 is, however, not optimised for a hardware implementation that operates in real-time, for two reasons. Firstly, the variance is calculated over blocks of EEG data and should be replaced with a normalising

factor that can be calculated on-the-fly. Furthermore, in practical terms, the CWT is the convolution of the signal $x(t)$ with an impulse response $h(t)$, where $h(t)$ is defined as:

$$h(t) = \frac{1}{\sqrt{a}}\psi\left(\frac{-t}{a}\right) \tag{3.3}$$

Therefore, $\psi(t)$ from Equation 3.2 can be utilized in Equation 3.3, leading to the realization of the Mexican hat CWT using a filter with the following transfer function:

$$H(j\omega) = \pi^{1/4}\sqrt{\frac{8}{3}a^5}\omega^2 e^{-a^2\omega^2/2}. \tag{3.4}$$

Since $\psi(t)$ is centred around $t = 0$ and is non-causal, a hardware implementation with an impulse response derived based on Equation 3.2 will have poles in the right hand complex plane and will be unstable. A stable transfer function approximation that would allow for the CWT to be implemented as a filter can be realized by introducing a time shift (T) in Equation 3.2 [27]. The following transfer function can be derived by accounting for the introduced time shift, and replacing $j\omega$ with s in Equation 3.4, as:

$$H(s) = \frac{-\pi^{1/4}\sqrt{\frac{8}{3}a^5}s^2}{e^{sT-a^2s^2/2}}. \tag{3.5}$$

The exponential term in the denominator of Equation 3.5 can be further approximated using the Maclaurin series of Equation 3.6 ([27]), allowing for the filter transfer function of Equation 3.7, which has a rational and finite transfer function and can be in a filter implementation.

$$e^x = 1 + x + \frac{x^2}{2!} + +\frac{x^3}{3!} + ... \tag{3.6}$$

$$H(s) = \frac{-\pi^{1/4}\sqrt{\frac{8}{3}a^5}s^2}{1 + sT + (\frac{T^2}{2} - \frac{a^2}{2})s^2 + (\frac{T^3}{6} - \frac{Ta^2}{2})s^3 + ...}. \tag{3.7}$$

The introduced time shift would result in a delay in the output of the final filter implementation. This delay must be compensated for, to allow for the real-time operation of the algorithm.

The algorithm, modified to allow for a hardware implementation, has been shown in Figure 3.2 and is partitioned into three main stages (stages 1 to 3) and four routes (routes A to D). A real-time averaging operation is performed in Route A by calculating the input signal envelope with a cutoff frequency of 0.16 Hz. The

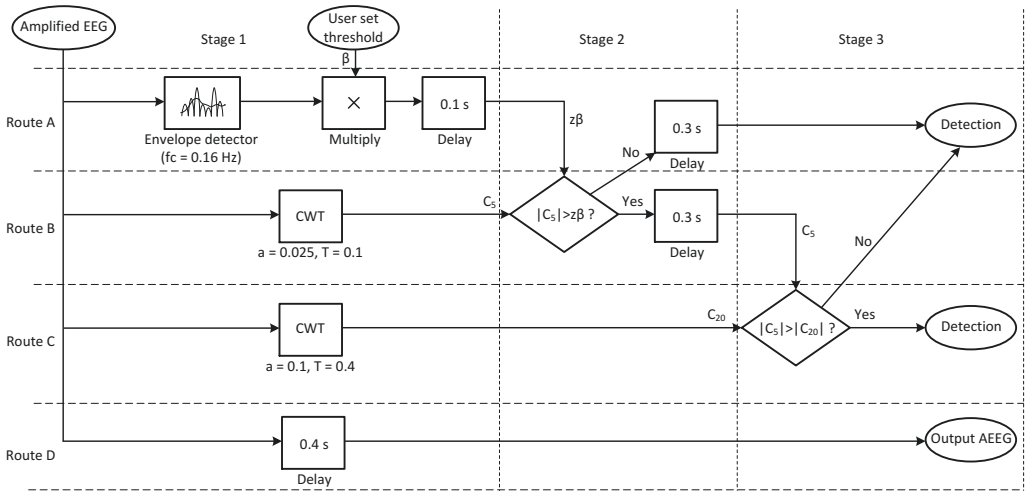


Figure 3.2: *Overview of modified interictal spike selection algorithm for a hardware implementation. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

output of the envelope detector is then multiplied by a user set threshold (β). The multiplication block is subsequently followed by a constant delay of 0.1 s, added to compensate for the delay resulting from the CWT blocks placed in the following routes and the parallel signal processing nature of the algorithm. The normalization performed in route A ensures that the spikes are identified later in the algorithm independent of changes in the EEG signal amplitude occurring between different patients or due to the quality of the electrodes. Routes B and C consist of the CWT approximations (C_5 and C_{20}). C_5 is at scale 0.025 ($T = 0.1$) while C_{20} is at scale 0.1 ($T = 0.4$). Considering the mentioned scales and time shift values, the work of [27] found a 7th order approximation to closely follow the Mexican hat CWT transfer function. Substituting $a = 0.025$, $T = 0.1$ and $a = 0.1$, $T = 0.4$ in a 7th order approximation in the form of Equation 3.7 results in Equation 3.8 and Equation 3.9 as the final transfer functions for C_5 and C_{20}, respectively.

$$H(s) = \frac{-2.15\times10^{-4}s^2}{1.43\times10^{-12}s^7+3.23\times10^{-10}s^6+3.61\times10^{-8}s^5+2.65\times10^{-6}s^4+1.35\times10^{-4}s^3+0.005s^2+0.1s+1}. \tag{3.8}$$

$$H(s) = \frac{-6.88\times10^{-3}s^2}{2.34\times10^{-8}s^7+1.34\times10^{-6}s^6+3.7\times10^{-5}s^5+6.79\times10^{-4}s^4+8.67\times10^{-3}s^3+0.075s^2+0.4s+1}. \quad (3.9)$$

It must be noted that the algorithm has originally been implemented in Matlab and therefore, the analysis scale has been altered based on the sampling frequency of 200 Hz (Matlab scale = Wanted scale(a)×Sampling frequency).

The comparisons of normalised wavelet powers performed in stages 2 and 3 have been replaced with absolute value comparisons ($|C_5| > |z\beta|$ and $|C_5| > |C_{20}|$).

The largest amount of delay present in the algorithm results from the C_{20} wavelet operation ($T = 0.4$) and therefore, two 0.3 s delay blocks have been included in stage 2 to equalize the total amount of delay present within the algorithm routes. The reader should note that the delay blocks have been placed after the comparison stage in Stage 2 as the analog or digital nature of the signals being processed has not been considered in the algorithm description of Figure 3.2.

Finally, Route D delays the raw EEG input signal by 0.4 s so that the correct section of the signal corresponding to the detections are passed to the transmitter.

The algorithm is scalable in that a copy of the algorithm, when implemented in the form of an ASIC (Section 3.4), will be incorporated in each channel of a WEEG unit. Furthermore, taking the union of the detection results of the algorithm copies using a logic OR gate will ensure that a single detection at the output of one of the channels results in the corresponding section of EEG data from all channels to be sent for transmission, as shown in the configuration of Figure 3.3. In response, a set period of the EEG signal before and after the detection will be recorded (the recording window), requiring a buffer memory to store the signal from before the detection for a duration of half the recording window (recording window/2). By using the algorithm, only the signals within the recording window are sent to the transmitter for transmission. Consequently, the overall amount of data to be transmitted is reduced. The algorithm, implemented in software, achieves a sensitivity of 90% for a 50% reduction in transmitted data.

3.4 System architecture

A number of top level specifications must be considered prior to examining the circuit level design strategy.

As previously stated, $CP_{\mathrm{TX}}+NP_{\mathrm{DR}}$ must be smaller than the power consumed by the transmitter in case of no data reduction present. Considering a data reduction

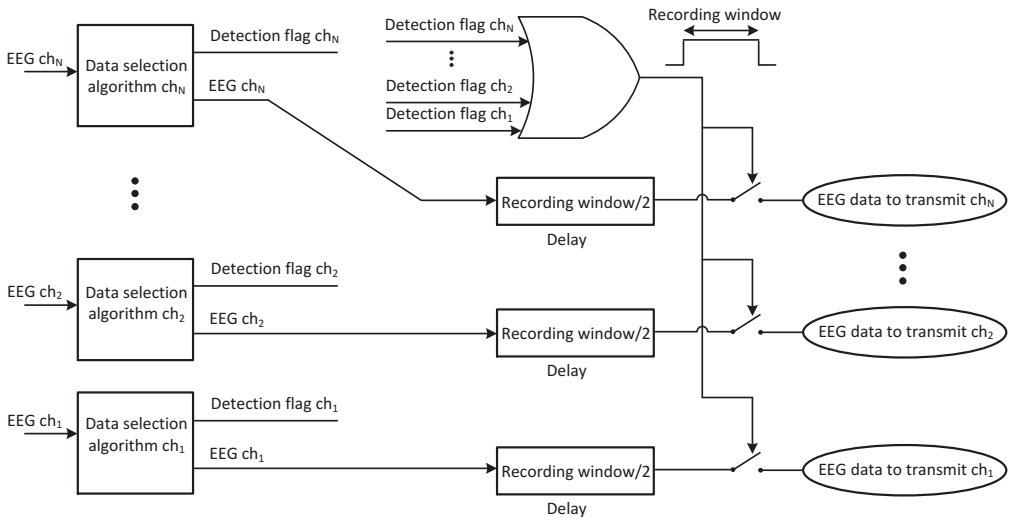


Figure 3.3: *Overview of the configuration required to transmit EEG data from multiple channels in response to a single detection made of any of the algorithm copies.*

(C) of 50%, and P_{TX} of 2.3 mW (lower bound of P_{TX} calculated in Chapter 2), provides a power budget of 1.15 mW for all present data reduction stages. Assuming a channel count of 32 and reserving 50% of the mentioned power budget (575 μW) for buffering data before and after a detection will result in less than 17 μW of power available per channel for implementation of the spike selection system.

A top level block diagram showing the analog-based system architecture has been shown in Figure 3.4. The analog signal processing circuitry have been arranged in Stage 1. This has been followed by Stage 2 in-which comparison operations are performed using two absolute value comparators operating in parallel and in real-time. Stage 3 combines the outputs of the two comparators, using a simple two-input AND gate, to produce a final detection flag output.

3.4.1 Route A

Since full-wave rectifiers effectively calculate the absolute value of a given signal, perfect matching between both polarities is required in a circuit level implementation to maximize accuracy. This often leads to using more complex circuitry that would demand higher power consumption. As a result, a half-wave rectifier has been used within the implemented envelope detector in Route A of Figure 3.4. Signal rectification is performed, as shown in Figure 3.5, using the circuit proposed in [28]. This circuit structure consists of a comparator, and following digital in-

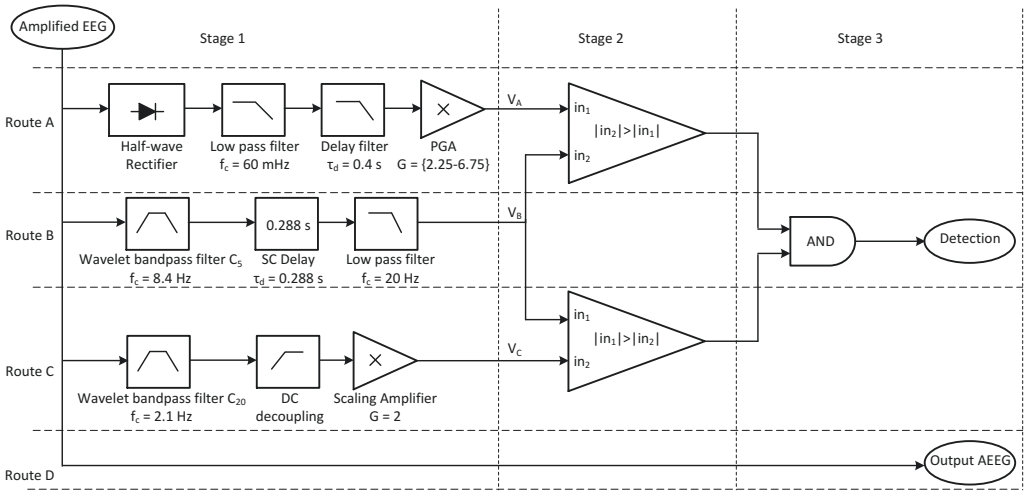


Figure 3.4: *Top level spike selection system architecture. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

verter, that would either select V_{in}, or a DC reference voltage (V_{ref}), to be passed on to the output. The switches, designed as minimum sized NMOS transistors (0.5/0.35 μm), provide a low impedance path to the output while isolating V_{in} and V_{ref} from noise generated by the comparator and digital inverter. The rectifier achieves a dynamic range of 80 dB.

Replacing the full-wave rectifier in the envelope detector with a half-wave rectifier, without supplementary modifications to the system, can result in performance degradation. Half-wave rectifiers only pass the positive sections of the input signal to the output, resulting in signal power loss. Furthermore, extra unwanted frequency components closer to the wanted near-DC terms, will be present at the output due to half-wave rectification [29]. Assuming a single tone sine wave input at frequency f, the corresponding output of the full-wave rectifier will have frequency components including the DC term and even harmonics of the input signal ($2f$, $4f$, ...). The half-wave rectifier output frequency content will, however, contain the DC term and input harmonics including f, requiring a lower cutoff frequency for the subsequent low-pass filter to separate the DC information.

As a result of the above mentioned issues, the cutoff frequency of the low-pass filter following the half-wave rectifier in Figure 3.4 was set to 60 mHz (chosen empirically). An extra gain factor ($\times 2$) was also incorporated into the following programmable gain amplifier by modulating the user-set thresholds to compensate for the signal power loss.

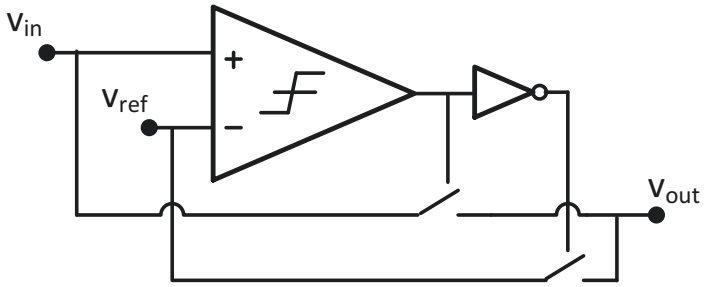


Figure 3.5: *Half-wave rectifier circuit topology. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

The low cutoff frequency (60 mHz) of the low-pass filter is realized by continuously clocking the output of an OTA cell, as proposed in [30]. The filter operation principle is shown in Figure 3.6 and, as can be seen, the OTA output current (I_1) can flow into the output capacitor (C_{int} = 40 pF) only when the switch is closed. Assuming δ as the duty cycle of the clock signal (ϕ), the effective current flowing into C_{int} can be defined as:

$$I_2 = \delta \times I_1. \tag{3.10}$$

The lowpass filter tolerates a maximum input signal amplitude of 140 mV_{pp} and has a dynamic range of 64 dB. A 128 Hz clock signal with a duty cycle of 1% was used to set the filter cutoff frequency to 60 mHz.

The 0.4 s delay block following the filter was created by cascading two first order G_mC lowpass filters. Group delay, which is a measure of the amount of phase distortion seen at the output of a filter as a function of frequency is defined as:

$$\tau_g = -\frac{1}{360} \cdot \frac{d\phi}{df} \tag{3.11}$$

A suitable delay filter must exhibit constant magnitude and a linear phase response with negative slope over the signal bandwidth. Generally, a higher count of poles and zeros in the filter transfer function is required to create large delays for wideband input signals, resulting in more complex circuitry. However, since the input signal to the delay block is significantly band-limited (60 mHz) here, a delay filter with a smaller number of low frequency poles can be utilized to generate the

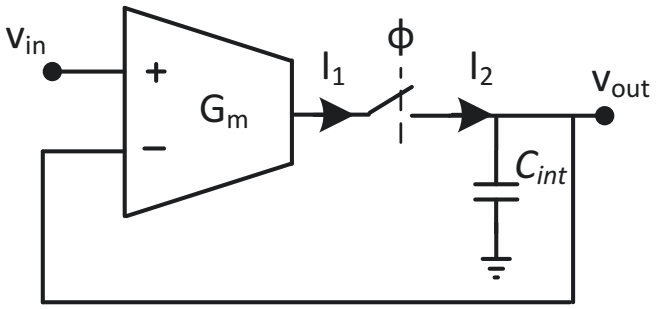
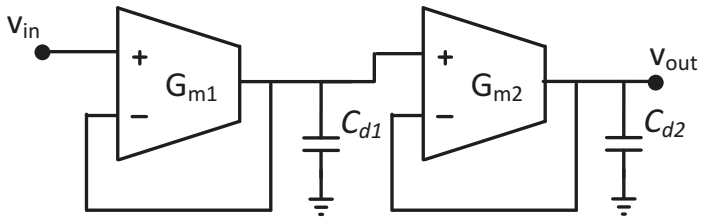


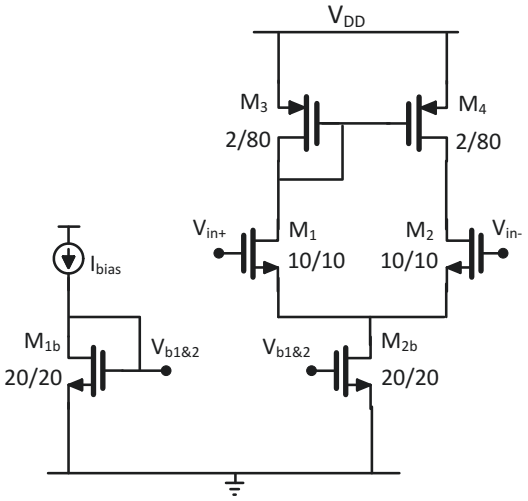
Figure 3.6: *Low pass filter with a cutoff frequency proportional to the duty cycle of the clock signal (ϕ). Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

0.4 s delay. Two G_mC low pass filters were cascaded as shown in Figure 3.7(a) to create an overall delay filter with a nearly constant group delay of 0.4 s with a variation of 0.5 % over the 0 to 60 mHz bandwidth. The two single stage OTAs (G_{m1} − G_{m2}), shown in Figure 3.7(b), are biased with a current (I_{bias}) of 6.5 pA placing all transistors in the deep weak inversion region. The tradeoffs in designing low transconductance OTAs with MOSFET devices biased in the weak inversion region are discussed in detail in previously published literature [31], [32], and therefore not repeated here. Fairly large devices are used in the OTAs to improve matching. The parasitic capacitance introduced by these devices does not distort the delay filter bandwidth, which is much smaller than that of the individual OTAs. Two 20 pF integrated capacitors (C_{d1} and C_{d2}) were used to place the cutoff frequency of the delay filter at 0.5 Hz. This circuit also removes any high frequency artefacts resulting from the clock signal used in the low pass filter preceding the delay filter.

The delay filter topology allows for the distortion introduced by the filter to be minimized, since the inputs to the OTAs used in this circuit closely follow each other for low frequency signals. A Total Harmonic Distortion (THD) of 1.01 % was achieved for an input signal of 140 mV_{pp} at a frequency of 500 mHz and this is reduced to 0.02 % for an input signal with the same amplitude at a frequency of 50 mHz. The inband noise of the delay filter was 25 μVrms and 8.6 μVrms integrated over the 1 mHz to 500 mHz and 1 mHz to 60 mHz bands respectively. Taking the worst case figures for the maximum input signal and integrated noise of 140 mV_{pp}



(a)



(b)

Figure 3.7: *0.4 s G_mC delay filter suitable for processing signals below 60 mHz (a) delay filter structure; (b) OTA circuit topology. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

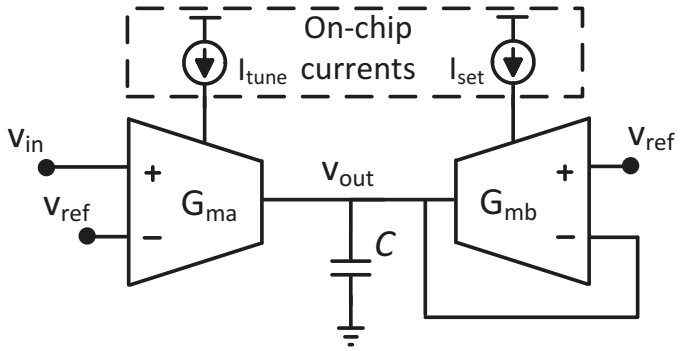


Figure 3.8: *Topology of Programmable Gain Amplifier (PGA). The PGA gain is set by the ratio of currents I_{tune} and I_{set} (I_{tune}/I_{set}). Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

and 25 μVrms results in a dynamic range of 66 dB for the delay filter.

The Programmable Gain Amplifier (PGA) following the delay filter consists of two single stage OTAs ($G_{ma} - G_{mb}$), as shown in Figure 3.8. The gain of the amplifier is set by the ratio of the biasing currents ($I_{\text{tune}}/I_{\text{set}}$). The system architecture must allow for the user to achieve a desired level of system performance, considering the tradeoff between system sensitivity and amount of transmitted data. Therefore, the PGA gain must represent the user set threshold values (β).

The β are multiplied by a factor of 2 to compensate for signal power loss resulting from the half-wave rectifier in Route A (Figure 5.2). Furthermore, an extra factor of 3.56 is incorporated into the new β values to correct for signal amplification resulting from the circuit-level implementation of the CWT (C_5), as will be seen later in Section 3.4.2. Since the values of β^2 originally varied between 0.1 and 0.9, the PGA gain settings must be programmable between 2.25 and 6.75. This is realized by setting the current I_{set} to 5 nA and turning I_{tune} between 11.25 nA and 33.75 nA. After deciding on the specific performance tradeoff between sensitivity and amount of data reduction, the two currents I_{tune} and I_{set} were generated on-chip using a current reference circuit, which has been described later in Section 3.5.

3.4.2 Route B

Considering the 7th order transfer functions derived in Equation 3.8 and Equation 3.9, two bandpass filters with center frequencies of 8.4 Hz and 2.1 Hz can closely approximate the CWT operations in routes B (C_5) and C (C_{20}), respectively. The detailed analysis and design of a 7th order wavelet bandpass filter with a G_mC topology and center frequency of 2.1 Hz (C_{20}), shown in Figure 3.9, has been presented in the work of [33]. Using the same topology, a biasing current of 26.5 pA is used to set the transconductance of the OTA cells in Figure 3.9 (G_{m3}-G_{m11}) to 407 pS, resulting in a center frequency of 8.4 Hz for the bandpass filter. The filter has a dynamic range 43 dB and input referred noise of 51 μV_{rms}, integrated over the 6-10 Hz passband.

The gain of the CWT is dependent on the analysis scale, as seen in the mathematical representation of Equation 3.1. However, the bandpass filter approximation has a center frequency gain of approximately 0 dB, due to the LC ladder implementation. For the case of the C_5 filter, there is a factor of 3.56 attenuation between the center frequency gain of the implemented circuit and the ideal transfer function, together with a 180° phase shift. The negative sign is inconsequential since only the absolute value of the filter output will be used for comparison in stage 2 of the system. However, the factor of 3.56 gain loss must be accounted for in the PGA gain settings of Route A.

The 0.3 s delay block following the C_5 wavelet filter must delay the filter output, which is strongly attenuated around 8.4 Hz, by almost three full cycles. Utilizing a continuous time delay filter to generate the 0.3 s delay is not appealing, since such a filter will require 12 poles. The SC delay circuit of [34] has been modified to be suitable for adaptation in this work. A unity gain buffering stage is added between the C_5 filter and the SC delay circuit to isolate the filter output from the switching transients. The delay circuit operates by cascading multiple delay cells, each consisting of two SC sections controlled by complementary clock signals ϕ_1 and ϕ_2 (see Figure 3.10(a)).

$$d = 2\big(1 - D\big)T \tag{3.12}$$

where T and D are the clock period and duty cycle respectively. The output voltage of the delay cell can be derived as:

$$V_{OUT} = z^{-1}V_{IN} + nU_T \ln\left(\frac{I_{S1}}{I_{S4}}\frac{I_{S3}}{I_{S2}}\right) \tag{3.13}$$

where n is the slope factor, U_T is the thermal voltage and the four I_S terms represent

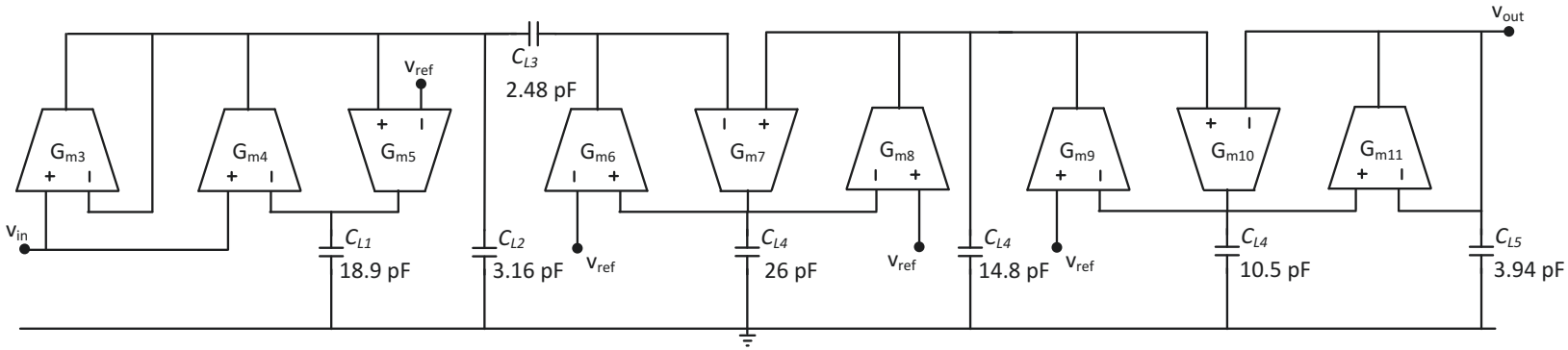


Figure 3.9: *Schematic of 7^{th} order bandpass filter approximating the CWT operation.*

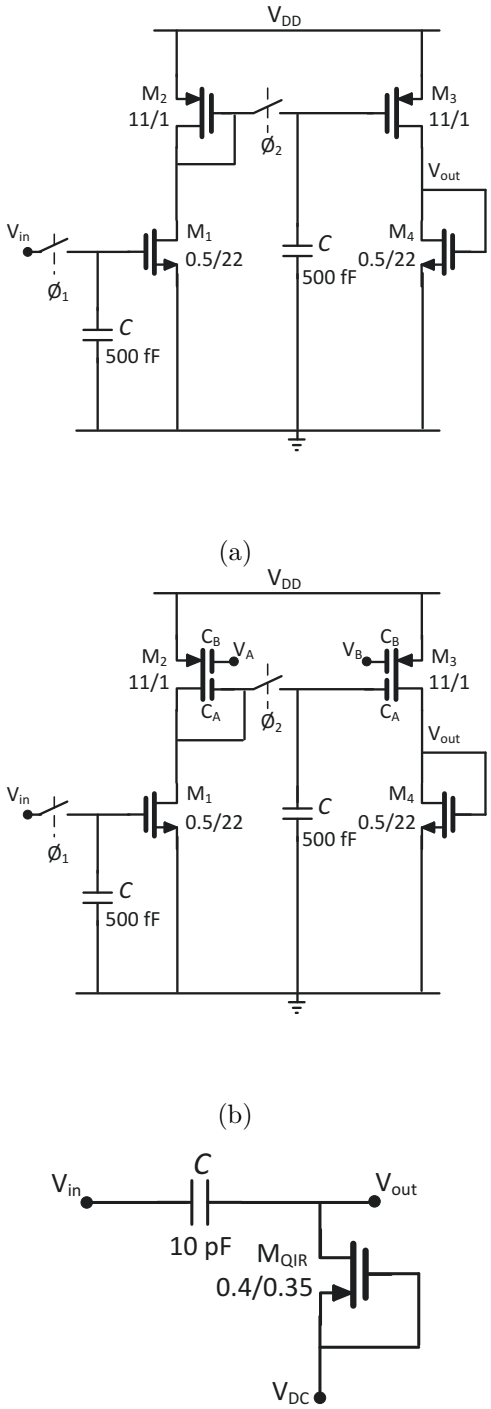


Figure 3.10: *SC delay circuit: (a) circuit architecture of normal delay cell; (b) circuit architecture of offset correction cell presented in [34]; (c) proposed DC blocking section. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

the specific current of transistors M_1 to M_4. As can be seen in Equation 3.13, offset voltages are generated at the output of each cell, due to mismatch between the specific currents of the M_1-M_4 and M_2-M_3 transistor pairs. The compounded effect of these offset voltages will result in signal distortion at the delay circuit output.

The authors of [34] recommend placing an offset correction cell incorporating floating gate transistors, as shown in Figure 3.10(b) within the delay line. The output voltage of the offset correction cell can be derived as

$$V_{OUT} = z^{-1}V_{IN} + nU_T \ln\left(\frac{I_{S1}}{I_{S4}}\frac{I_{S3}}{I_{S2}}\right) + \frac{C_B}{C_T}\left(V_A - V_B\right) \tag{3.14}$$

where C_{T} consists of the sum of the two capacitors, C_{A} and C_{B}, at the inputs of the floating gate PMOS transistors M_2 and M_3, ignoring any parasitic capacitances. Systematic offset from previous cells can be corrected by appropriately adjusting V_A and V_B in Equation 3.14. However, since the final system designed here is intended to be incorporated into each channel of a WEEG system, individual tuning of offset correction cells in each delay circuit may not be a scalable solution. Furthermore, a significant loss of gain (-10.33 dB) has been associated with the offset correction cell in [34]. This is due to the parasitic gate-drain capacitance (C_{GD}) present at the floating gate nodes in the offset correction cells.

An alternative solution for offset correction is to have DC-blocking sections, as shown in Figure 3.10(c), that can be placed intermediately within the delay line to reject the offset voltages. This modification does come at the cost of the added area required by the DC blocking circuitry. Each section is essentially a high pass filter with a sub-Hz corner frequency, created using a 10 pF capacitor and a (0.4 μm/0.35 μm) PMOS transistor acting as a Quasi-Infinite Resistor (M_{QIR}).

In this work, the delay generated by the delay line is 0.288 s (32 cells). A low pass filter (f_c = 20 Hz), placed after the delay line, reduced the distortion resulting from the clock signal frequency component and its harmonics.

3.4.3 Route C

The center frequency of the C_{20} filter, which has a structure identical to the C_5 filter, was set to 2.1 Hz with a biasing current of 6.5 pA. A factor of 2 difference in mid-band gains of the C_5 and C_{20} filters must be present based on the ideal transfer functions. As previously mentioned, the circuit level implementation of the wavelet filters results in a midband gain of 0 dB for both C_5 and C_{20}. The output of the C_{20} filter was scaled to compensate for the difference in gain using a non-inverting amplifier.

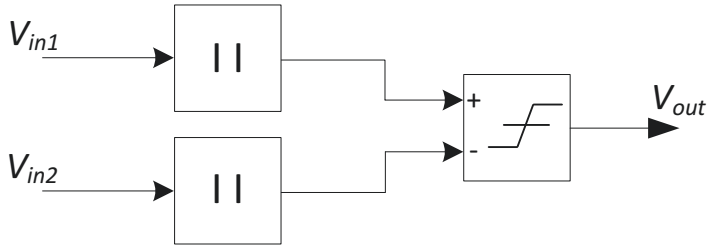


Figure 3.11: *Implementation of an absolute value comparator using two full-wave rectifiers and a conventional comparator. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

3.4.4 Stages 2 and 3

The outputs of the calculations performed in Stage 1 (V_A, V_B and V_C in Figure 3.4) are compared in Stage 2 and a final detection result is produced in Stage 3. Typically, a comparator's functionality is based on comparing the actual value of two signals (i.e. considering the sign in the comparison). However, conventional comparator topologies are suboptimal for the absolute value comparisons required in Stage 2, as they would require full wave rectifiers to be placed at the comparator input. The absolute value comparator proposed in this section would allow for such comparisons to be carried out without the need for additional full-wave rectifiers.

A conceptual implementation of a full-wave rectifier based absolute value comparison is shown in Figure 3.11. It consists of two full-wave rectifiers producing the absolute value of the analog input signals, together with a conventional comparator, which performs the comparison. The full-wave rectifiers employed in this structure require a good matching when processing both polarities of the input signal in order to not distort the signals prior to detection. This is often achieved using complex circuitry leading to higher than necessary power consumption, which may not be an attractive solution in a WEEG system running on a low power budget. On the other hand, the power consumption of comparators is mainly dictated by the system speed requirements. Since the processed bio-signals in biomedical systems, and EEG signals in the case of the WEEG system, are low frequency, it is possible to incorporate slower, low power comparators within the signal chain. Furthermore, a number of low complexity techniques have already been reported and can be used to minimize the non-idealities resulting from comparators which can otherwise impact the overall system resolution [35], [36].

A block diagram implementation of the absolute value comparator without the use of full-wave rectifiers is shown in Figure 3.12(a). It consists of an analog

inverter, two comparators operating in parallel and an XOR gate making a final decision based on the outputs of the two comparators. Signals V_{out1} and V_{out2} refer to the outputs of the two comparators, COMP_1 and COMP_2 respectively, while V_{out} refers to the output of the XOR gate. The main operation of this implementation, based on different input signal levels, is summarized in Table 3.2. As can be seen in Table 3.2, this implementation emulates the correct operation of an absolute value comparator.

Since the two comparators (COMP_1 and COMP_2) perform a decision making operation on the two input signals simultaneously, any delay introduced by the analog inverter circuit should be minimal and nearly constant over the range of input signal frequencies. This would result in higher power consumption in order to push the dominant pole of the inverter towards higher frequencies and reduce the effective group delay. Furthermore, fine matching would be required between the circuit elements in-order to accurately create an inverted version of the input signal.

A modified version of the absolute value comparator is shown in Figure 3.12(b), addressing the above mentioned concerns. In this structure the inverter has been replaced by an addition operation and the input signals have been slightly reconfigured. Table 3.2 can again be used to model the operation of this circuit. The adder circuit has been placed within the two comparators. Therefore, the analog inverter has been eliminated and the group delay of this circuit would not affect the overall performance of the absolute value comparator.

It is possible to implement each of the two comparators (COMP_1 and COMP_2) as dynamic latch circuits in order to achieve low power consumption. However, due to the large input referred offset voltage of the latch, a cascade of three preamplifiers ($\text{A}_{1\text{-}3}$) incorporating the output offset cancellation scheme [35], was added prior to the dynamic latch to reduce the overall input referred offset. The structure of the comparators ($\text{COMP}_{1\text{-}2}$) has been shown in Figure 3.13(a). The clock signals $\phi_{1\text{-}6}$ are generated using the clocking scheme shown in Figure 3.13(b), resulting in a comparison operation every 8 milliseconds. As previously mentioned, this comparison rate is acceptable for use in the interictal spike selection SoC, in which the frequency of input signals to the comparator are extremely low (<20 Hz).

The offset voltage of the preamplifiers is stored and subtracted using the timing signals $\phi_{\ 1\text{-}4}$. Care should be taken in the design in order to reduce the charge injection errors resulting from the switching operation. As a result, all switches were implemented as small size NMOS transistors (0.5/0.35 μm) and all sampling capacitors have a value of 1 pF.

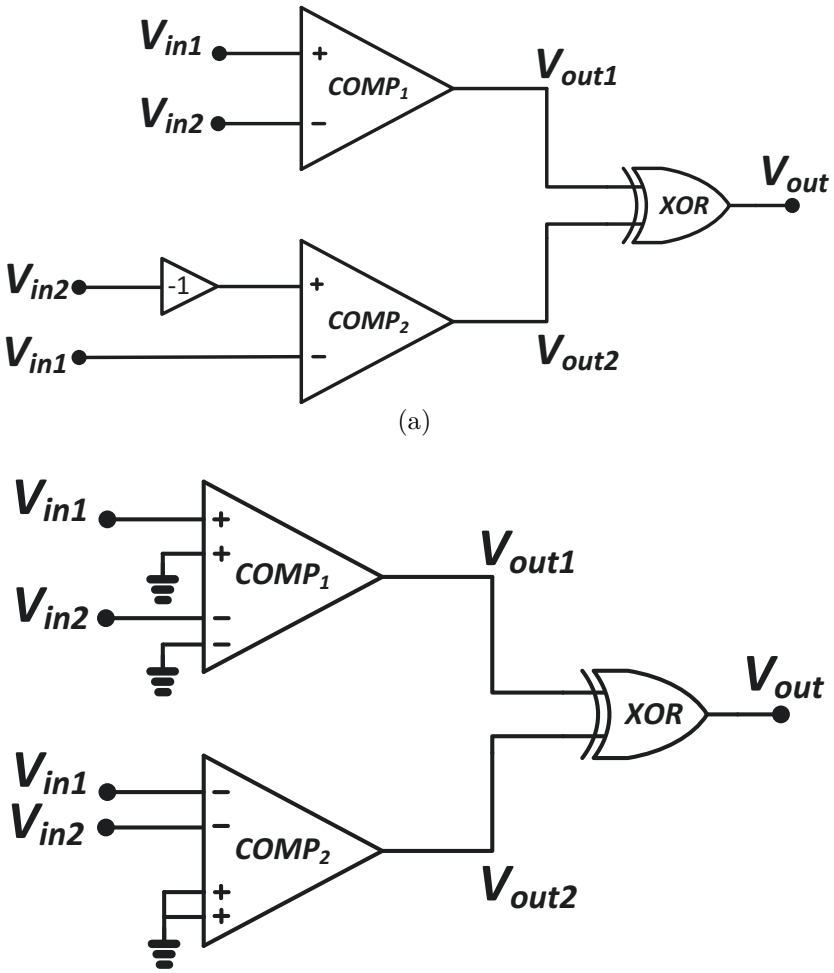
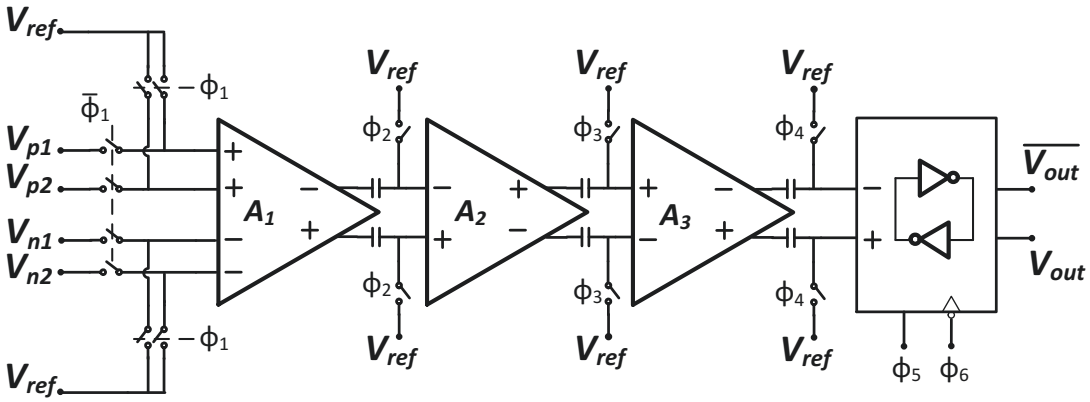
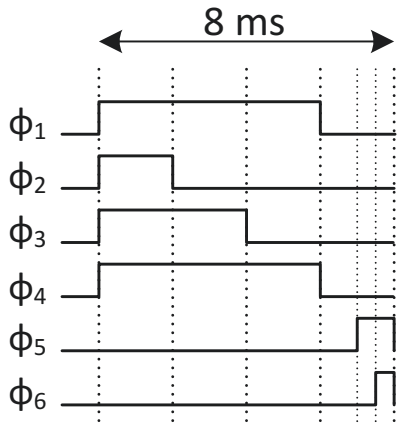


Figure 3.12: *Absolute value comparator: (a) top-level implementation;(b) modified implementation. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*



(a)



(b)

Figure 3.13: *Comparators $COMP_{1\text{-}2}$: (a) circuit schematic; (b) timing diagram for $\phi_{1\text{-}6}$. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

Table 3.2: *Comparator output levels based on different input signals.*

Input signal levels		V_{out1}	V_{out2}	V_{out}
$V_{\text{in1}} > 0$ $V_{\text{in2}} > 0$	$\lvert V_{\text{in1}}\rvert > \lvert V_{\text{in2}}\rvert$	1	0	1
	$\lvert V_{\text{in1}}\rvert < \lvert V_{\text{in2}}\rvert$	0	0	0
$V_{\text{in1}} > 0$ $V_{\text{in2}} < 0$	$\lvert V_{\text{in1}}\rvert > \lvert V_{\text{in2}}\rvert$	1	0	1
	$\lvert V_{\text{in1}}\rvert < \lvert V_{\text{in2}}\rvert$	1	1	0
$V_{\text{in1}} < 0$ $V_{\text{in2}} > 0$	$\lvert V_{\text{in1}}\rvert > \lvert V_{\text{in2}}\rvert$	0	1	1
	$\lvert V_{\text{in1}}\rvert < \lvert V_{\text{in2}}\rvert$	0	0	0
$V_{\text{in1}} < 0$ $V_{\text{in2}} < 0$	$\lvert V_{\text{in1}}\rvert > \lvert V_{\text{in2}}\rvert$	0	1	1
	$\lvert V_{\text{in1}}\rvert < \lvert V_{\text{in2}}\rvert$	1	1	0

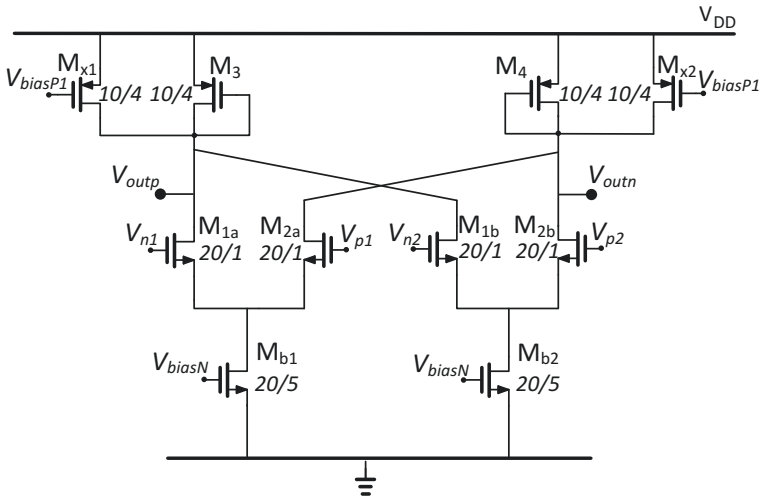


Figure 3.14: *Circuit-level structure of multiple input preamplifier A_1. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

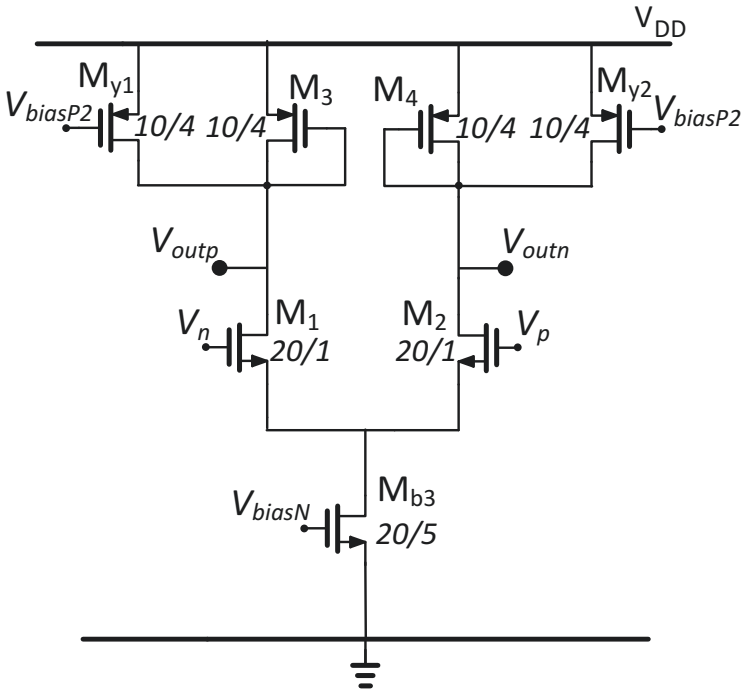


Figure 3.15: *Circuit-level structure of preamplifiers A_2 and A_3. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

The circuit diagrams of the pre-amplifiers ($A_{1\text{-}3}$), are shown in Figure 3.14 and Figure 3.15. The first preamplifier A_1, shown in Figure 3.14, is based on a multiple input OTA structure. Since offset cancellation is achieved by the means of an open loop operation, as seen earlier in Figure 3.13, a high gain in the preamplifiers could lead to saturation at the output nodes. Therefore, a diode connected load was chosen for the preamplifiers in order to provide a relatively low gain, that is defined by the ratio of the input and load transistor transconductances (g_{m1}/g_{m3}). Due the low power consumption and relaxed speed requirements here, the preamplifiers were designed to operate in the weak inversion region with small biasing currents. The diode connected loads by themselves would provide a gain that would be too small (<1). Unlike the strong inversion operation region, changing the device sizes would not change the effective transconductance of the input and load transistors, when biased in weak inversion region. Therefore, two current injecting transistors (M_{x1} and M_{x2}) have been connected to the drains of the diode connected load transistors. The current through the injecting transistors would account for a portion of the total current passing through the main biasing transistors (M_{b1} and M_{b2}) and would result in the input transistors having a larger value of transconductance compared

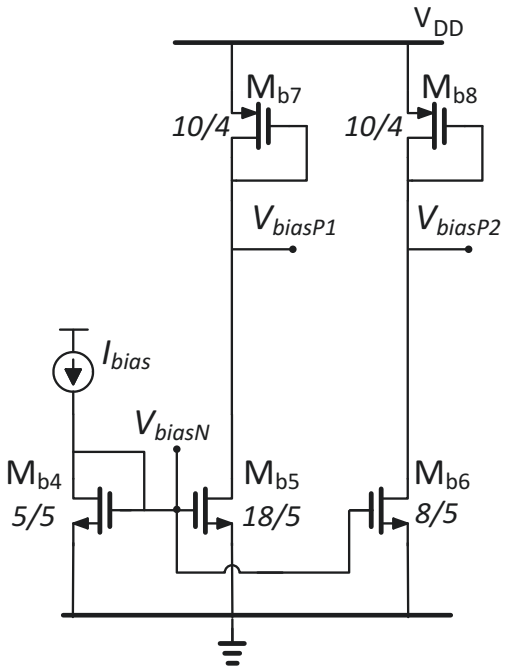


Figure 3.16: *Current scaling circuit used in the absolute value comparator. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

to the diode connected load transistors ($g_{m1} > g_{m3}$).

The second and third preamplifiers ($A_{2\text{-}3}$) have the same structure and are shown in Figure 3.15. This structure is also similar to the first preamplifier, with the difference of having a single set of input transistors. The biasing voltages V_{biasN}, V_{biasP1} and V_{biasP2} are used to bias the main biasing transistors ($M_{b1\text{-}3}$) and the current injecting transistors in A_1 ($M_{x1\text{-}2}$) and $A_{2\text{-}3}$ ($M_{y1\text{-}2}$) respectively. The voltages are created using the current scaling circuit shown in Figure 3.16. It must be noted that the current scaling transistors M_{b5} and M_{b6} have not been sized equally. The DC current passing through each of the load transistors (M_3 and M_4) in A_1, is twice the current passing through the load transistors (M_3 and M_4) in $A_{2\text{-}3}$ under nominal conditions and therefore, M_{b5} has been sized with a larger aspect ratio to provide a larger portion of the overall current in A_1 and increase the gain.

The topolopgy of the dynamic latch is based on the circuit proposed in the work of [37], and has been shown in Figure 3.17. The output of the latch would be valid for a certain amount of time prior to becoming non-valid (reset-phase). Therefore, two inverters followed by a D-flipflop have also been added at the outputs of the dynamic latch in order to sample the output of this circuit at the rising edge of

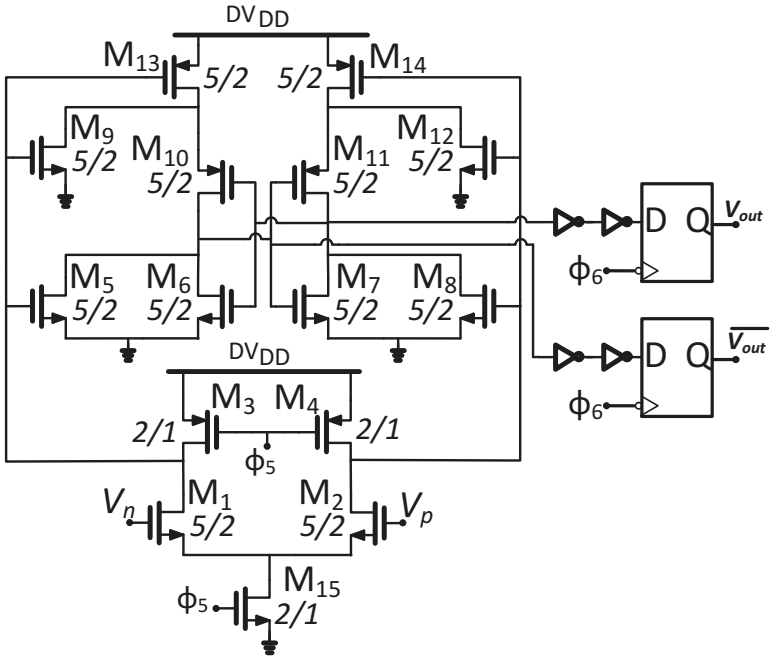


Figure 3.17: *Dyanmic latch and following sampling D-flipflops. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

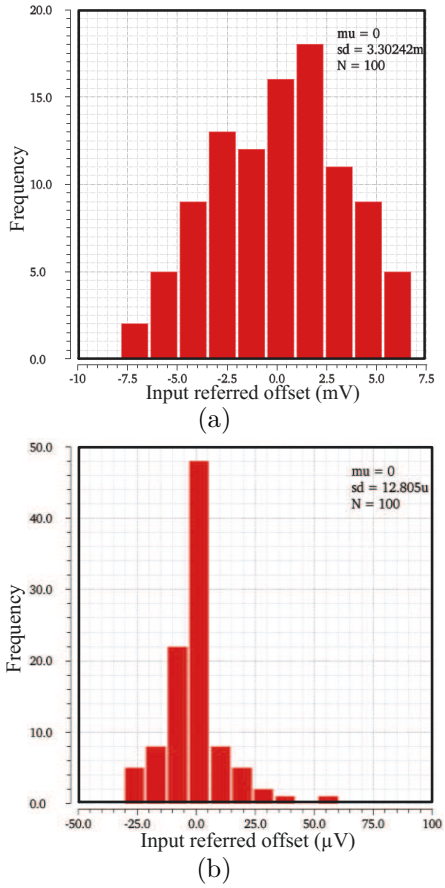


Figure 3.18: *Input referred offset voltage of: (a) dynamic latch; (b) preamplifiers and dynamic latch. Figure reprinted from: S. Iranmanesh, G. Raikos, Z. Jiang and E. Rodriguez-Villegas, "CMOS implementation of a low power absolute value comparator circuit," in IEEE NEWCAS, Vancouver, Jun. 2016, pp. 1-4, © IEEE.*

ϕ_6.

The main biasing current of the preamplifiers (I_{bias} in Figure 3.16) is set to 2.5 nA, resulting in a gain of almost 6 for each of the preamplifiers and a bandwidth of 33 kHz, which is much larger than the input signal bandwidth.

The input referred offset voltages of the dynamic latch and the structure consisting of the preamplifiers and the latch (previously shown in Figure 3.13(a)) were found by running 100 runs of Monte-Carlo simulations with a slow input ramp signal. The Monte-Carlo simulation results are shown in Figure 3.18. As can be seen in Figure 3.18(a), the dynamic latch alone has an input referred offset with a standard deviation (SD) of 3.3 mV. As shown in Figure 3.18(b), this value is reduced to 12.8 μV when employing the preamplifiers together with the offset cancellation scheme prior to the latch.

The nominal current consumption of the preamplifiers and the averaged current consumption of the digital circuitry were 112.7 nA and 0.3 nA, respectively. The absolute comparator therefore consumed 113 nA of current overall, from the 1.25 V supply voltage.

Two instances of the presented absolute value comparator are used in Stage 2 of the interictal spike selection system to compare $|C_5|$ with $|z\beta|$ and $|C_{20}|$. The output of the AND gate in stage 3 represents the detection flag and will only turn to 'VDD' when interictal activity is detected by the system (i.e. $|C_5| > |z\beta|$ and $|C_5| > |C_{20}|$).

3.5 System front end and biasing

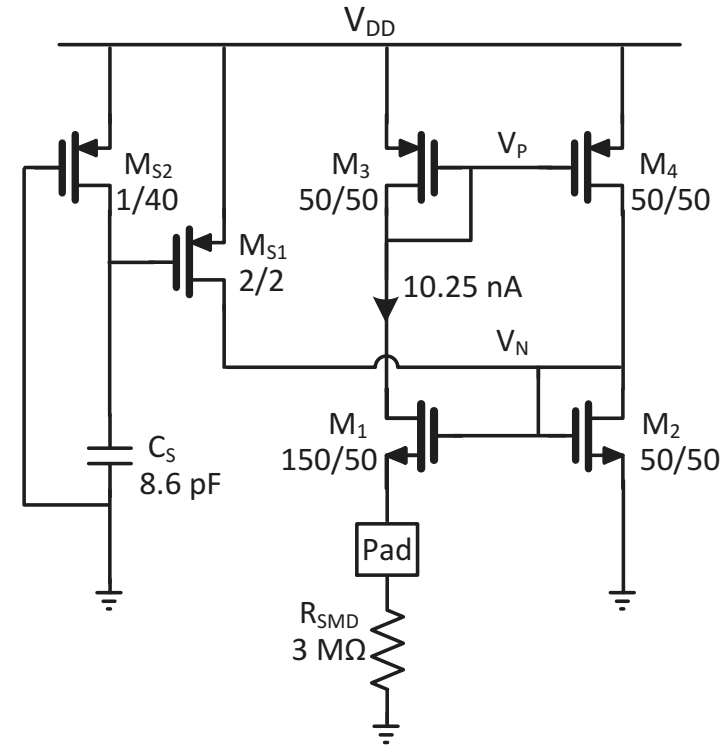
The IA was designed based on the topology of [38], achieving a mid-band gain of 39 dB and input referred noise of 2.7 μV_{rms} (integrated over 0.5-100 Hz).

The currents required by the system were generated using a main current reference circuit, shown in Figure 3.19(a), and on-chip current scaling circuitry. The current reference circuit generates a 10.25 nA reference current using an off-chip 3 MΩ surface mount resistor. The circuit obtains a correct operating point at startup with the help of the current injected by transistors M_{S1} and M_{S2}. The use of traditional current scaling circuitry to create the pA currents is not practical due to the large aspect ratio spread required. For instance, an aspect ratio spread of ∼1600 will be required to generate the 6.5 pA biasing current required by the C_{20} filter, from the reference current. Therefore, the $R-2R$ current splitting method reported in [39], [40] (shown in Figure 3.19(b)) has been adapted in 6 stages to produce the pA currents from a scaled down version of the reference current. In each stage, the R-2R ladder like structure consisting of one M_R and two M_{2R} devices would split the current in half. A fairly large sized diode connected device (M_n) has been used at the bottom of each stage to allow for the current to be copied by the circuits while minimizing mismatch.

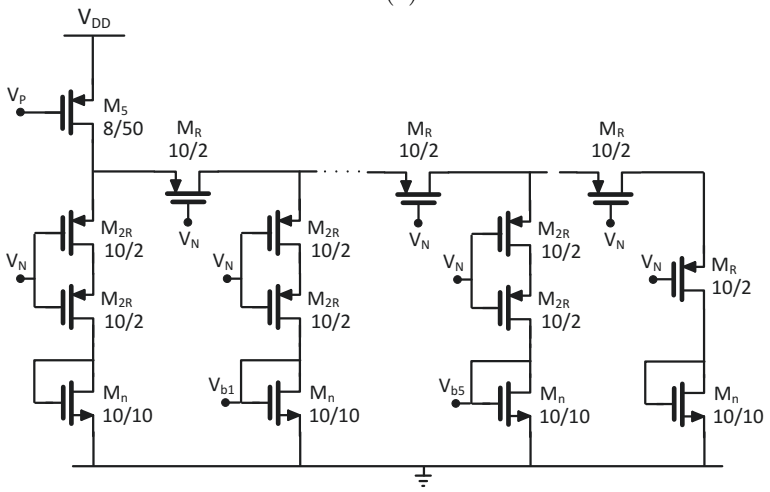
3.6 Experimental Results

3.6.1 Chip fabrication

The spike selection SoC was fabricated using a 0.35 μm AMS, 2 poly, 4 metal CMOS process. The capacitance values mentioned previously in this chapter were achieved on-chip using poly-poly capacitors. A micrograph of the fabricated chip



(a)



(b)

Figure 3.19: *Current reference: (a) core and startup circuitry; (b) splitter circuit. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

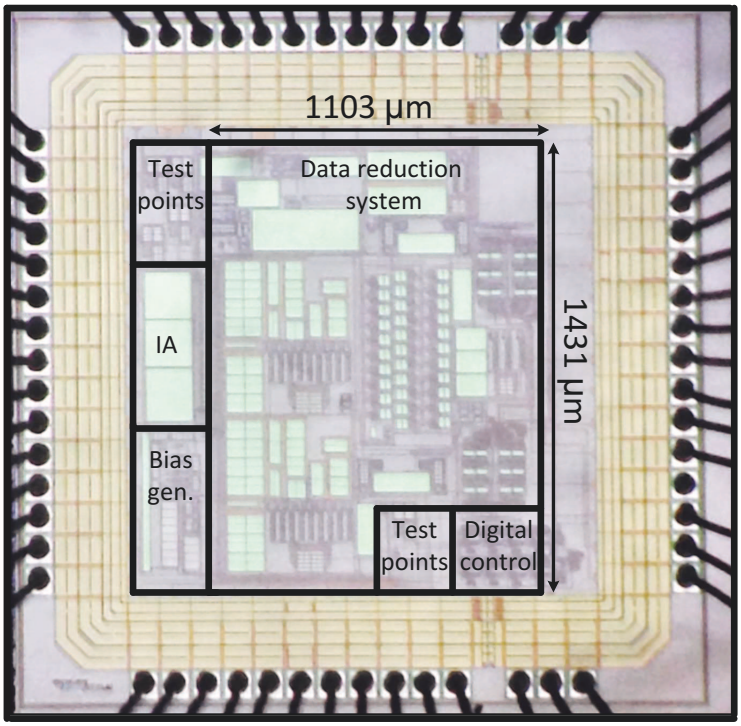


Figure 3.20: *Micrograph of fabricated chip. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

is shown in Figure 3.20. The active area consumed by the interictal spike selection system is 1.57 mm^2.

The digital portion of the system was restricted to the right side of the chip and the chip padring was partitioned into two separate parts in order to isolate the sensitive analog circuitry from the noisy digital sections.

3.6.2 Test setup and measurements

Input signals to the chip were generated by a National Instruments USB-6259 data acquisition (DAQ) board, and the same device was used to collect the detection flag output together with analog intermediate testpoint signals V_A, V_B and V_C in Figure 5.2. The data acquisition board presents a significant load to the outputs of the circuits within the system, which generally have a weak driving capability. Therefore, analog buffering circuitry consuming 8 μA from a separate 2 V supply was implemented on-chip between the testpoints and output pads. A digital buffering stage was also placed after the detection flag output.

Table 3.3: *Summary of data used for testing the interictal spike selection system performance.*

Patient	Age	Gender	Type of recording	Marked interictal events	Recording duration	$T_{spike}(\%)$
0	Unknown	Unknown	fMRI/EEG	644	00:36:55	14.5
1	24	Male	Long term monitoring	49	03:58:15	0.2
2	47	Female	AEEG	7	02:00:11	0.04
3	33	Female	AEEG	52	06:00:33	0.12
4	51	Unknown	AEEG	12	04:00:22	0.04
5	23	Female	AEEG	11	04:00:22	0.04
6	44	Female	Routine EEG	0	00:46:19	0
7	43	Male	Routine EEG	2	00:18:30	0.09
8	46	Male	AEEG	26	02:00:11	0.18
9	45	Male	Long term monitoring	30	04:00:22	0.1
10	23	Female	AEEG	45	04:00:22	0.15
11	53	Female	AEEG	8	02:00:11	0.05
12	27	Female	Long term monitoring	0	02:00:11	0
13	21	Female	AEEG	12	02:00:12	0.08
15	33	Unknown	Routine EEG	1	00:10:53	0.07
19	Unknown	Unknown	AEEG	28	22:57:05	0.01
20	Unknown	Unknown	AEEG	15	22:06:23	0.01
21	Unknown	Unknown	AEEG	40	21:05:43	0.02
Total	-	-	-	982	104:03:00	0.13

The dataset used for testing the chip performance contained 982 interictal events in over 4 days of data from 18 patients. Table 4.1 summarizes the dataset details per patient together with the number of marked events and total duration of events normalized by the recording duration (T_{spike}). Marking of the interictal events was performed by an expert from the UK National Hospital for Neurology and Neurosurgery. Since the duration of individual spikes was not available as part of the database documentation, a spike duration of 0.5 s (accounting for different forms of interictal activity) was assumed for the calculation of T_{spike}. The number of channels present in all recordings were not equal and therefore the 10 channels F7, F8, Fp1, Fp2, O1, O2, T3, T4, T5 and T6, which were common to all recordings, were selected to be processed by the chip.

An illustration of the system behaviour with 45 s of EEG signal containing an interictal event at the 10 s time mark is shown in Figure 3.21. The EEG trace was obtained from the data file belonging to channel F7 of patient 1. Measured outputs of the three intermediate testpoints V_{A}, V_{B} and V_{C}, which are the outputs of the calculations performed in Stage 1 of the system, are shown in Figure 3.22, Figure 3.23 and Figure 3.24, respectively, and follow the broad shape of the simulated results. As seen in Figure 3.25, the state of the detection flag signal changes twice from 'low' to 'high' around the 9.6 s time mark since the condition for an interictal event to be detected by the system (i.e. $|V_{\text{B}}| > |V_{\text{A}}|$ and $|V_{\text{B}}| > |V_{\text{C}}|$) has been satisfied.

The total noise contributed by the interictal spike selection system integrated over the algorithm operating band (referred to the IA input) was 1.5 μV_{rms}. System noise is dominated by thermal noise components and only 1% of the total noise is attributed to flicker noise.

The system performance was evaluated using the sensitivity and percentage of data transmitted indices, to allow for direct comparison with the work of [6]. The sensitivity is the percentage of events that are correctly identified by the system and is calculated as:

$$\text{Sensitivity} = \frac{TP}{TP + FN} \times 100\%. \tag{3.15}$$

In order to allow for direct comparison of the fabricated system performance with [6], an event detected by the system was deemed a True Positive (TP) if detected within a 2 s window of an expert marked event. Marked events left undetected by the system were considered as False Negatives (FN). The percentage of data transmitted was calculated assuming a 5 s window of EEG data stored for

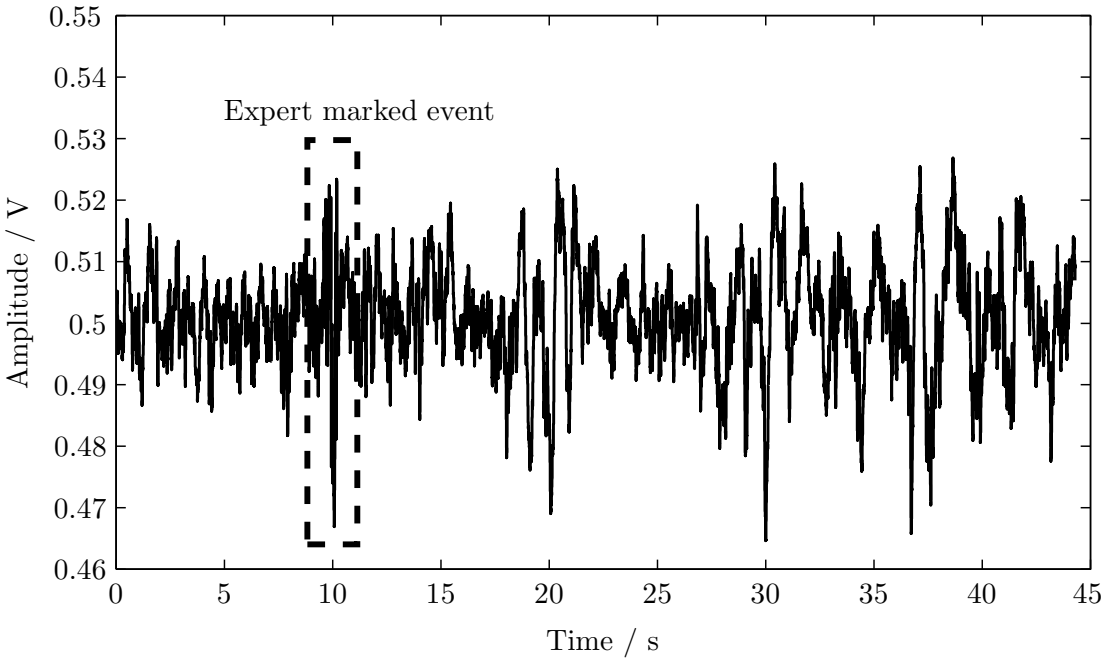


Figure 3.21: *A 45 s section of input EEG data processed by the system. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

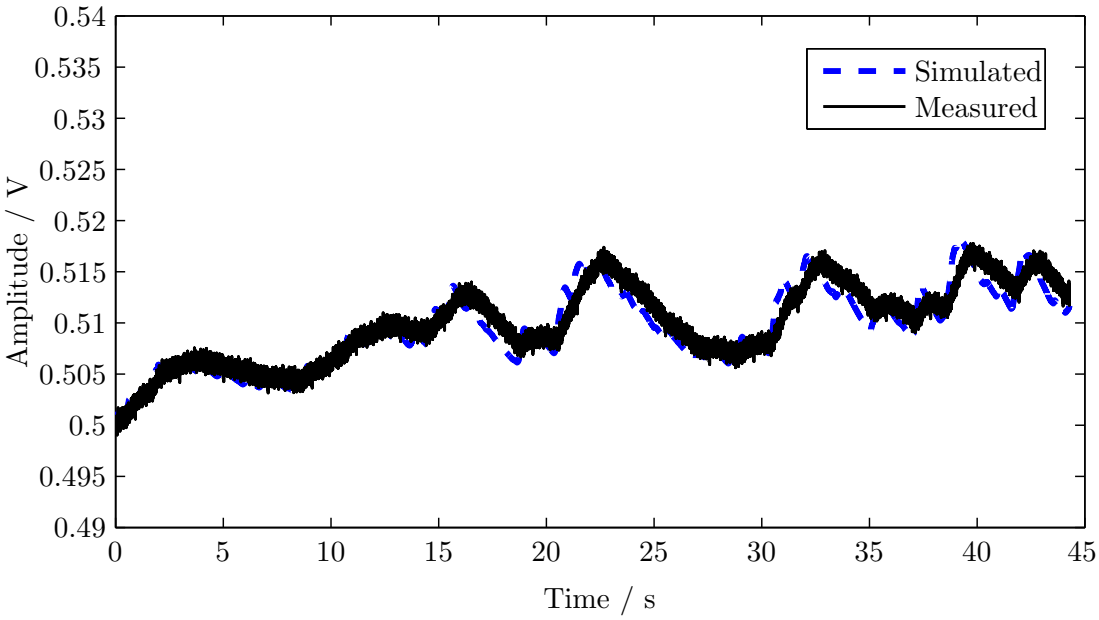


Figure 3.22: *Output of route A (V_A) in response to the input EEG trace. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

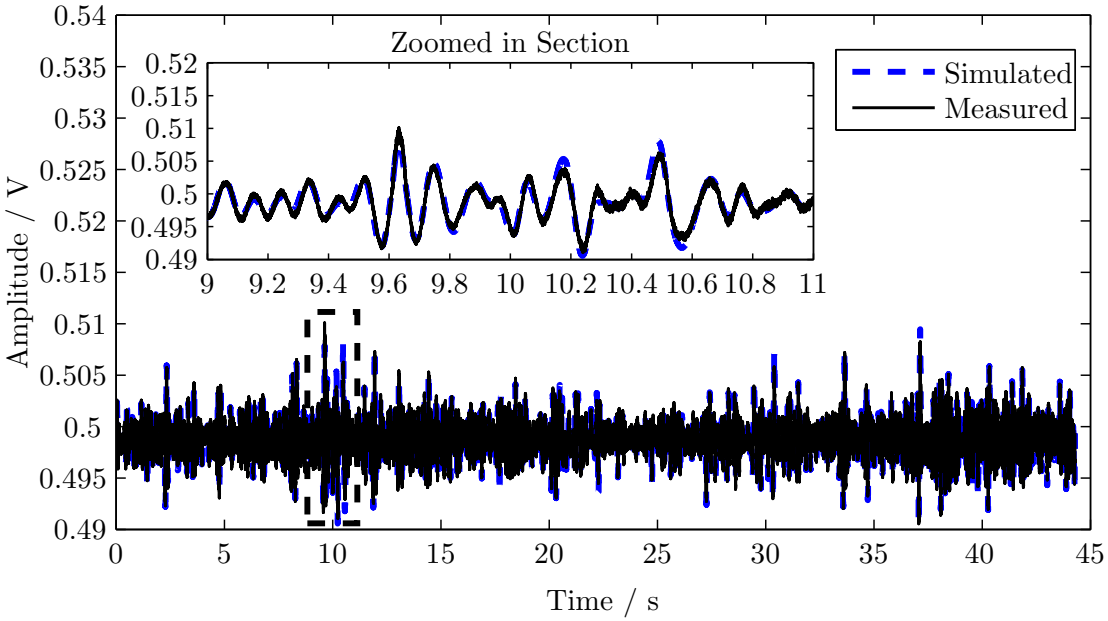


Figure 3.23: *Output of route B (V_B) in response to the input EEG trace. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

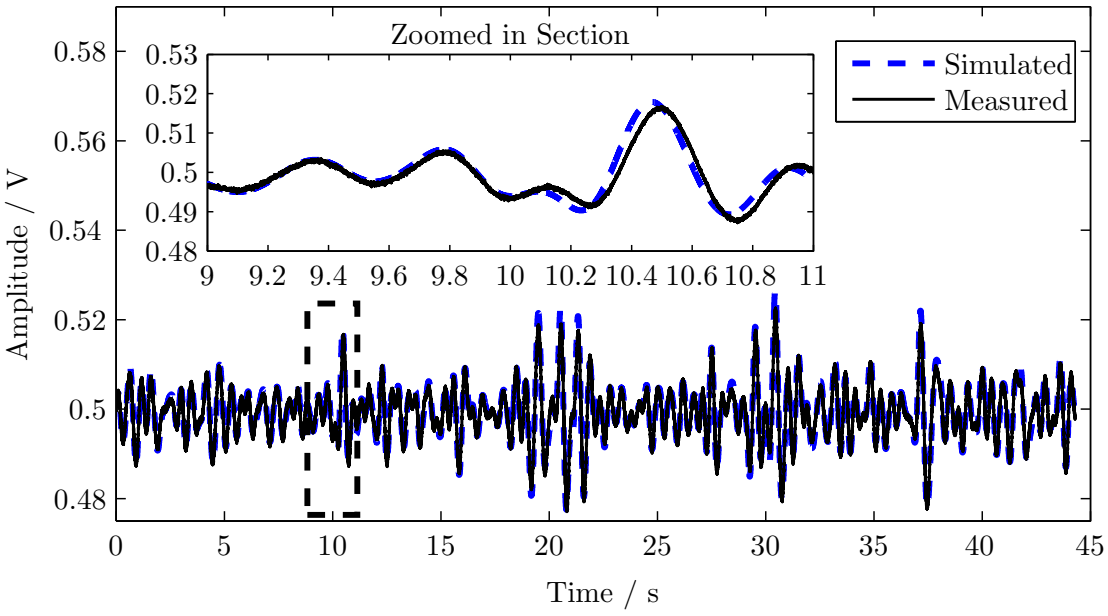


Figure 3.24: *Output of route C (V_C) in response to the input EEG trace. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

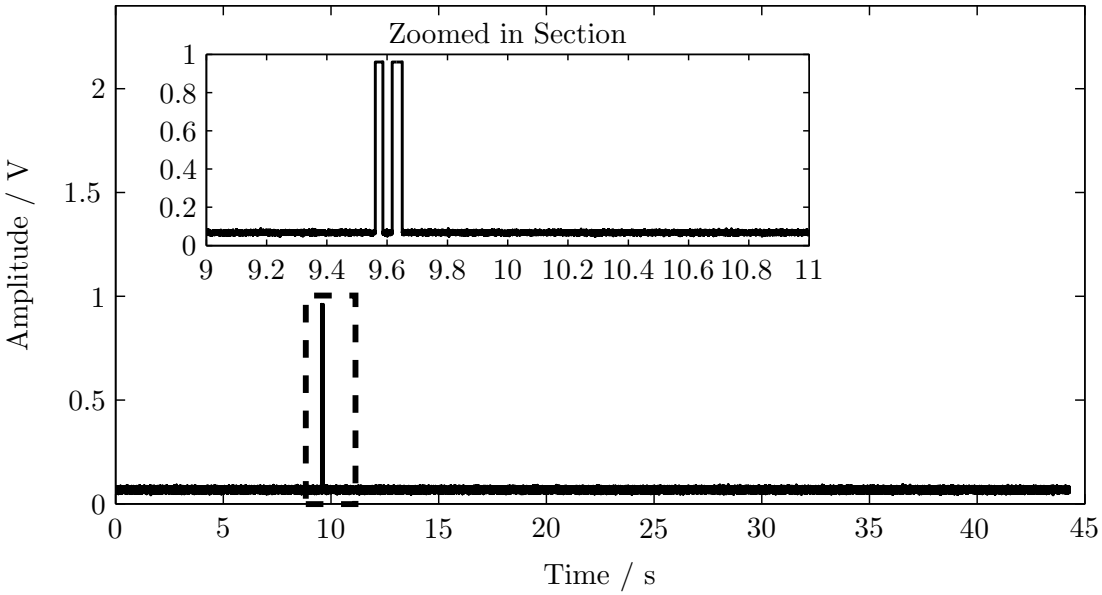


Figure 3.25: *System decision flag output in response to the input EEG trace. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

transmission in response to a detected event. Higher sensitivity together with a lower percentage of data transmitted would indicate better system performance.

The sensitivity and percentage of transmitted data tradeoff curve is generated as in Figure 4.18, based on the individual gain settings of the PGA. A set of four tuning currents ($I_{tune} = \{16\text{ nA}, 23\text{ nA}, 28\text{ nA}, 31.9\text{ nA}\}$) have been used to produce the desired PGA gains while keeping the testing process across the entire database tractable. The spike selection system achieves a sensitivity of 87.17% for a percentage of data transmitted of 44.65%, as seen in Figure 4.18. The area under the curve (AUC) is calculated to quantify the overall system performance and is found to be 0.774, a difference of 5.2% compared to the AUC of 0.816 achieved for the mathematical implementation of the spike selection algorithm.

The system performance has been summarized in Table 3.4. The system consumes 760 nA from a supply voltage of 1.25 V, resulting in a power consumption figure of 950 nW. The power consumed by the IA and current generation circuitry has been excluded from this figure, since as mentioned in Section 3.4, power savings are achieved using the reported system by reducing the power consumed by the transmitter. Therefore, the benefits of the data selection SoC are independent of the power consumed by the IA. Furthermore, the WEEG unit would utilize one instance of the current generator to bias all copies of the system, regardless of the channel count. The power consumed by the spike selection system is only 5.6% of

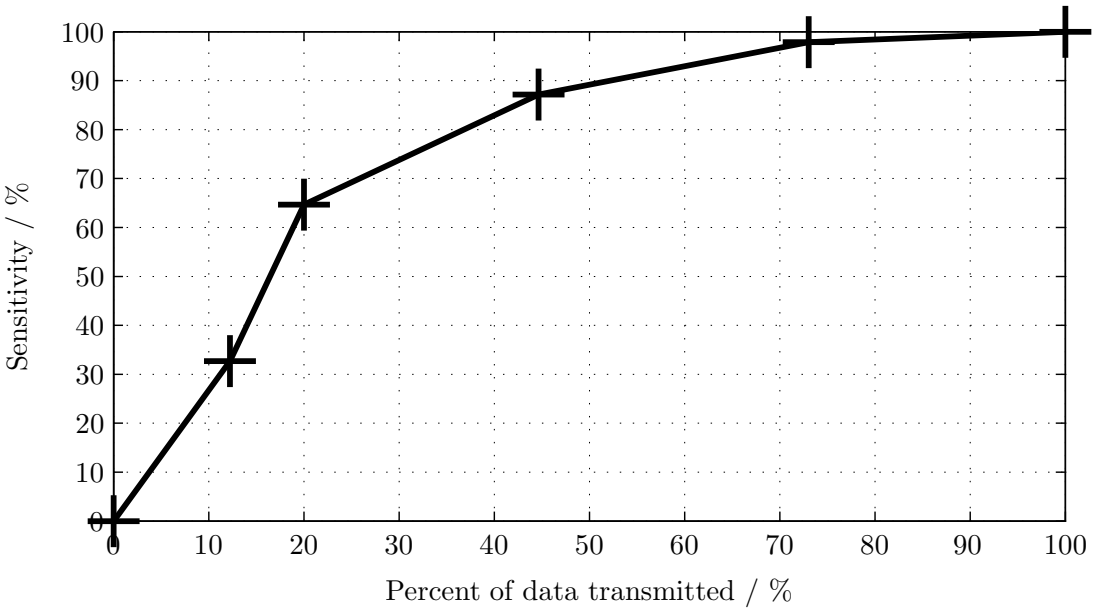


Figure 3.26: *System performance trade-off curve showing the tradeoff between sensitivity and amount of transmitted data. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "A 950 nW Analog-Based Data Reduction Chip for Wearable EEG Systems in Epilepsy," IEEE Journal of Solid-State Circuits, vol. 52, no. 9, pp. 2362-2373, 2017, © IEEE.*

the available power budget of 17 μW, calculated in Section 3.4.

The benefits of the data reduction stage in terms of power savings have been illustrated in Table 3.5, by comparing power figures for a 32 channel conventional wireless EEG unit (with no data reduction) and a WEEG system with the same number of channels utilizing the data reduction system proposed here. It has been assumed that both units have 32 channels consisting of an array of IAs, ADCs and a transmitter, with the only difference of an array of data reduction blocks providing 50% data reduction (C = 0.5), utilized in the WEEG system. Power figures for the data reduction stages are based on the power consumed by the interictal spike selection system (950 nW), and assuming 32 channels. The power numbers for the IA and ADC arrays are taken from the low-power implementations of [41] and [42], respectively, while the transmitter is assumed to be the commercially available CC2640R2F [43]. It can be noted that the presence of the data reduction stage in the WEEG system allows for 46% reduction in the overall system power consumption in comparison to a conventional wireless device created from the same IA array, ADC array and transmitter.

Table 3.4: *Summary of interictal spike selection system performance.*

CMOS Process	0.35 μm	
Area	1.57 mm^2	
Supply Voltage	1.25 V	
Sensitivity	87%	
Percentage of data transmitted	45%	
Current consumption (nA)	Envelope detector	76.5
	Delay filter	0.02
	PGA (I_{tune} = 23 nA)	54
	Wavelet filter (C_5)	0.24
	SC delay	360
	Low-pass filter (f_c = 20 Hz)	0.3
	Wavelet filter (C_{20})	0.06
	Scaling amplifier	30
	Absolute value comparator	113.5 (×2)
	Digital circuitry	11
	Total	760

Table 3.5: *Power comparison of conventional wireless EEG (no data reduction) and WEEG incorporating data reduction stage.*

	Wireless EEG	Wearable EEG ($C = 0.5$)
IA array [41]	112 μW	112 μW
ADCs (12b, 500 S/s) [42]	6.4 μW	6.4 μW
Data reduction array	-	30.4 μW
Transmitter [43] Active: 192Kbps×11nJ/b	2112 μW	2112 μW×0.5
Total	2230.4 μW	1204.8 μW

3.7 Discussion

Interictal activity is more frequent than ictal activity, with 50% of epileptic patients presenting interictal discharges in their first EEG session. Furthermore, interictal discharges can provide useful information for the clinical diagnosis of epilepsy, such as seizure type and the likelihood of recurrence. Thus, long-term EEG recordings containing interictal activity are sought after by the medical community to increase the diagnostic yield.

Developing truly wearable EEG monitoring devices with long operating lifetimes to allow for patients to be monitored at the comfort of their natural environment remains an open challenge due to the power hungry nature of wireless transmitters, which dominate the device power consumption. This chapter presented, for the first time, the design and results for a low power scalable data reduction system that would benefit the realization of truly wearable EEG devices for the monitoring of epilepsy. The system reduces the amount of EEG data to be transmitted by selecting sections of data that are likely to contain interictal events for transmission, while rejecting background activity. Furthermore, as a result of the data reduction performed by the system, the amount of data presented to the neurologists is also reduced, reducing the amount of time required for the diagnosis process.

A sensitivity figure of 87% is achieved by the system for a data reduction of 55%. In order to reflect real world data acquisition conditions, no effort has been made to select artefact free sections of the database during the testing process.

A number of system-level approximations were carried out to allow for the original algorithm, which was implemented in the software domain, to be mapped to an on-chip hardware implementation. Modifications performed in the three main processing routes (Routes A, B and C) to maintain the parallel processing nature of the algorithm in hardware were discussed in detail. A novel absolute value comparator, also presented as part of this chapter, was used to compare the absolute values of the signals processed by the analog circuitry in the system, without the need for a full-wave rectification stage. Full-wave rectifiers require good matching when processing both polarities of input signals in order to not distort the signals prior to the comparison operation. The comparator circuit consumes 142 nW and has an input referred offset voltage of 12.8 μV. The use of the absolute value comparator circuit can be extended to processing other low-frequency biosignals in low-power applications where the use of full-wave rectifiers is not desirable.

The spike selection system was fabricated using a 0.35 μm CMOS process (with an active area of 1.57 mm^2 occupied by the system). The analog-based design

approach results on the system power consumption of 950 nW to be negligible compared to the power consumed by the transmitter in the case of continuous transmission, allowing for the operating lifetime of a wearable EEG device to be significantly extended.

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4 A 1.14 μW seizure selection and data reduction System-on-Chip

4.1 Introduction

Based on the definition proposed by the International League Against Epilepsy (ILAE) and the International Bureau for Epilepsy (IBE), epileptic seizures are transient episodes occuring with signs and symptoms resulting from excessive or synchronous discharge of neurons in the brain [1]. Clinical seizures are primarily detected using EEG and are associated with different degrees of behavioural manifestations and changes in the patient's emotional, consciousness and cognition states, depending on factors such as the location of seizure onset, seizure propagation patterns and brain maturity. In 2010, seizures were classified into 13 categories by the ILAE, with different symptoms and morphologies [2].

Determination of behavioural seizures depends on how closely the patient is observed and interacted with. On the other hand, observing seizure patterns in the patient's EEG traces is dependent on the quality of the EEG monitoring setup. In [3], EEG seizures have been defined as events present on the EEG, independent of possible behavioural manifestations. Rhythmic EEG activity patterns with varying frequency and amplitude are generally seen during seizures. The fundumental frequency of this activity has been noted to be between DC and 28 Hz in [4]. Based on the work of [5], however, analysing low frequency signal information below 10 Hz is sufficient for seizure identification. With regards to duration of the event, seizures typically last from 3 s to more than a minute [3].

This chapter presents a low-power and scalable EEG seizure selection SoC, fabricated in a 0.18 μm CMOS process, targeting the diagnostic aspect of epilepsy. Reviewing raw and relevant EEG data is important for neurologists during the diagnostic process in order to provide an accurate diagnosis. The presented SoC, which operates based on the data reduction concept, reduces the amount of data to be transmitted by a WEEG device by continuously selecting sections of EEG data containing candidate seizure activity. Therefore, the transmitter will only be

required to transmit the selected data sections, resulting in significant reductions in the overall power consumed by the WEEG device. This approach simultaneously reduces the amount of time required by neurologists to review the transmitted EEG data, without replacing their role in the diagnostic process.

A number of seizure detection SoCs focusing on real-time treatment and symptom alleviation or automatic diary generation by counting the number of occurred seizures, as opposed to selecting sections of data containing candidate seizures to aid the diagnosis which is carried out here, have been reported in the literature and reviewed in Section 4.2. A description of the data selection algorithm used as a foundation for the developed SoC, is presented in Section 4.3. This is followed by Section 4.4, in which the data selection system architecture together with the circuits blocks used in the system have been presented. The front-end and control circuitry are discussed in Section 4.5. Subsequently, measurement and performance results of the fabricated chip are discussed in detail in Section 4.6.

4.2 Seizure detection

In the context of epilepsy monitoring, a number of recently reported SoCs, focusing on seizure control rather than diagnosis, targeted a reduction on the communication cost by detecting seizures locally. A reduction of 14× in the system power consumption was achieved in the work of [6]. This system transmits feature-vectors extracted based on spectral decomposition using a filter bank, rather than transmitting raw EEG signals, and seizure detection was performed in the software domain using the extracted features. The seizure detection system of [7] is designed based on counters that detect high frequency activity while consuming 1.5 μW/channel. This system uses parameters that must be tuned specifically to each patient, achieving sensitivity and specificity figures of 100% and a detection delay of 13.5 s. Detection delay (latency) is an important performance metric of systems that perform seizure detection locally and are intended to be used in conjunction with real time seizure suppression. The detection delay must be minimized to allow for timely closed-loop control of seizures. A seizure detector utilizing signal entropy and frequency spectrum based feature extraction together with a Linear Least Square (LLS) classifier was reported in [8]. The SoC requires patient-specific training and achieves power consumption, detection delay and accuracy figures of 162.31 μW/channel, 0.8 s and 92%, respectively. Feature Extraction (FE) is carried out in the seizure detection SoC of [9] by deriving the spectral energy distribution of the input signal prior to the classification stage. The SoC utilizes a Non-Linear

Support Vector Machine (NLSVM) classifier to perform patient-specific seizure classification, while consuming 19.6 μW/channel (FE + classification) and achieving a sensitivity, specificity and detection delay of 95.1%, 99% and 2 s, respectively.

With regards to the seizure detection systems proposed in [6]–[9], it must be noted that these systems focus on real-time treatment of epilepsy through closed-loop instantaneous seizure suppression. As such, patient-specific approaches can be utilized in these works since patients requiring such systems have already been diagnosed with epilepsy and therefore the gathered EEG data, which is known to contain seizure activity, can be used for training the seizure detection algorithms.

The patient-specific seizure detection system of [10] focused on seizure counting and the monitoring aspect of epilepsy. Seizure events are detected in this system by deriving the input signal energy in different frequency bands and using a lookup table. During the patient-specific training phase, the system is run continuously for each patient, gathering raw EEG signals that must be reviewed manually by a neurologist until at least one seizure event is identified. A probability lookup table for each value of signal energy is subsequently generated, based on the data collected in the training phase, and used to match the measured energy values with the probability of seizure occurrence. The seizure detector consumes 0.45 μW/channel, while detecting 98.5% of seizures with a specificity of 85%. The detection delay is not a concern in the SoC of [10], since the system aim is to count the number of seizures, and as such is it sufficient to detect seizure occurrence once at any time throughout the seizure duration. Nonetheless, the detection delay of the system was found to be 9.1 s. Seizure counting systems can be used to form automatic seizure diaries, allowing for neurologists to monitor the frequency of seizure occurrence. In addition, the generated diary can be used to support the expert decision on the effectiveness of antiepileptic drugs (AEDs) [11].

In order to be suitable for incorporation as part of a WEEG system intended to aid the diagnosis of epilepsy, the seizure selection algorithm must ideally select the entire duration of every candidate seizure while operating with a stringent power budget. Furthermore, the use of patient-specific data to train the algorithm will not be practical since such data would not be readily available prior to diagnosis, requiring additional EEG monitoring sessions to acquire sufficient training data before using the algorithm. In addition to delaying the diagnosis, the mentioned training process would be resource intensive due to the need for manual review of the gathered raw EEG signals by a neurologist, to identify potential seizure episodes.

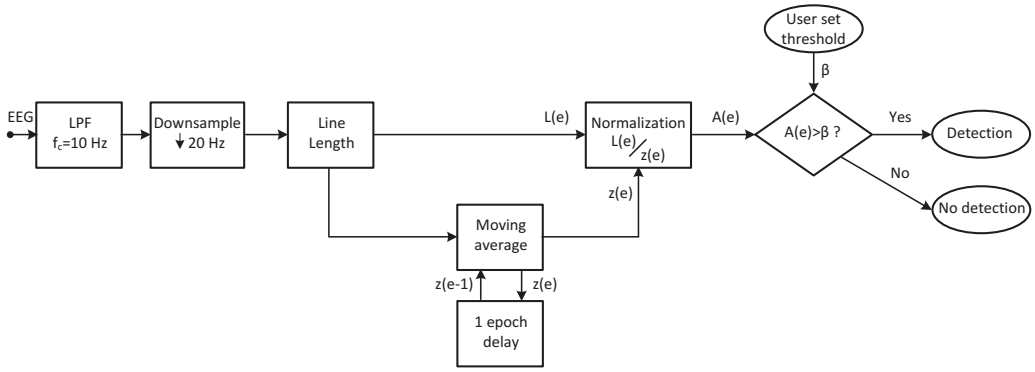


Figure 4.1: *Overview of the seizure selection algorithm operation.*

4.3 Algorithm architecture

The data selection SoC presented in this chapter utilizes the algorithm proposed in [12], which is based on extraction and processing of the line length feature to identify likely seizures, as a foundation. An overview of the algorithm operation is shown in Figure 4.1.

The EEG input to each channel of the algorithm is initially high-pass filtered with a cutoff frequency of 0.16 Hz, to remove the DC offsets produced at the electrode-skin interface. Since analysing the signal information below 10 Hz is sufficient for seizure identification, a 10 Hz third order low-pass filter is used to strongly attenuate the signal frequency components above 10 Hz, allowing for the algorithm data rate to be reduced by downsampling the EEG signal while avoiding distortion resulting from aliasing. Subsequently, the low-pass filtered signal is downsampled to 20 Hz, using a decimation block.

The downsampled signal, split into 2 s non-overlapping epochs, is used for feature calculation. The suitability of 65 features consisting of time domain features and features derived based on the DWT, CWT and Fourier Transform (FT), in terms of seizure selection performance and computational complexity, was evaluated in the work of [13]. Considering both the sensitivity-specificity tradeoff and the relative complexity, the features achieving the best performance were reported as the DWT based relative power and line length. With regards to the power consumed by a hardware implementation of the feature extraction stage, a power figure of 26 μW was reported for the low-power DWT engine proposed in [14], rendering the DWT based feature extraction method unsuitable for use in a diagnostic WEEG system with a power budget of 14 μW (see Chapter 2).

The line length is defined as the sum of distances across successive samples ([15]), calculated over each epoch as

$$L(e) = \sum_{k=1}^{S} |x(k-1) - x(k)| \tag{4.1}$$

where e is the epoch number being processed and $L(e)$, x, k and S are the line length calculated within the epoch, downsampled signal, sample number and total number of samples in the epoch, respectively.

Signal normalization is performed in the next stage of the algorithm to correct for broad changes in signal amplitude among different patients and intrapatient EEG variations, e.g. differences in the amplitude of signals picked up at different locations of the head. This will allow for a fixed detection threshold to be used later in the algorithm, regardless of the EEG signal amplitude. Considering line length as the feature to be normalized, the effectiveness of five normalization techniques calculated based on the median decaying memory, mean memory, standard deviation memory, peak detector and input signal range detector was investigated in [16], in terms of aiding seizure selection. The median decaying memory was found to provide normalization while enhancing the differentiation between seizure activity and background EEG [16]. The median decaying memory is derived as

$$z(e) = (1-\lambda) \times \text{median}\{L(e-1)...L(e-B_1)\} + \lambda \times z(e-1) \tag{4.2}$$

where $z(e)$ represents the estimated background activity calculated for the current epoch. The number of epochs used in the median calculation (searching window) is B_1 and λ is a decay constant which controls the effect of previously calculated values of z on the current calculation.

A start-up time of 2 min was chosen for the algorithm in the work of [12] to allow for the background estimate $z(e)$ to reach the same range of values as $L(e)$, during which the median is derived using all available epochs and $\lambda = 0.92$. The value of λ is increased to 0.99 after the initial 2 min period to reduce the effect of erroneous values of the median calculation likely caused by seizure events. The normalization estimate is calculated over a 120 s period and therefore $B_1 = 60$ for 2 s epochs.

Hardware implementations of median filters, not specifically designed for processing EEG signals, have been previously reported in the literature and proven to be power hungry. A 3 input median filter (not specific to EEG processing) was proposed in [17], consuming 14 mW. The more recent work of [18] reports a 9 input

median circuit consuming 1.25 mW. Since in Equation 4.2, the median operation is performed on the input signal and its time-shifted copies, the required delay elements (60 in the case of Equation 4.2) would only add to the hardware implementation complexity and power consumption. Due to the limited power budget of the data selection algorithm hardware implementation, a moving average filter was used to estimate the background activity instead of the median decaying memory. The moving average (MAV) is calculated as:

$$MAV(e) = \frac{1}{B_2} \sum_{i=0}^{B_2-1} L(e-i) \tag{4.3}$$

where B_2 is the window length of the filter and was set to 60, similar to B_1 in the median decaying memory calculation of Equation 4.2. For $B_2 \gg 1$, the moving average of Equation 4.3 can be approximated in the less computationally expensive recursive form, that is used here to estimate the backgroud activity ($z(e)$) as in Equation 4.4 [19].

$$z(e) = \frac{B_2 - 1}{B_2} \times z(e-1) + \frac{L(e)}{B_2}. \tag{4.4}$$

It should be noted that Equation 4.4 is specific to processing discrete time signals. Considering the epoch duration of 2 s ($f_s = 500$ mHz), the transfer function of the moving average corresponds to a single-pole recursive low pass filter with a cutoff frequency (f_c) of 1.3 mHz calculated using Equation 4.5, allowing for a continuous time analog domain approximation which was used in the hardware implementation shown later in Section 4.4.

$$f_c = \frac{-f_s}{2\pi} \ln\left(\frac{B_2 - 1}{B_2}\right). \tag{4.5}$$

The normalization stage is completed by dividing the output of the line length calculation by the background estimate as:

$$A(e) = L(e)/z(e). \tag{4.6}$$

A detection flag for the channel being analysed (represented by $DF_n(e)$ in Figure 5.1) will be set to '1' if the normalized feature $A(e)$ is greater than a user set threshold (β). The value of β can be tuned by a neurologist to achieve a desired level of performance, based on the tradeoff between the system sensitivity and the amount of transmitted data.

Candidate seizure events are selected using a multichannel approach as shown

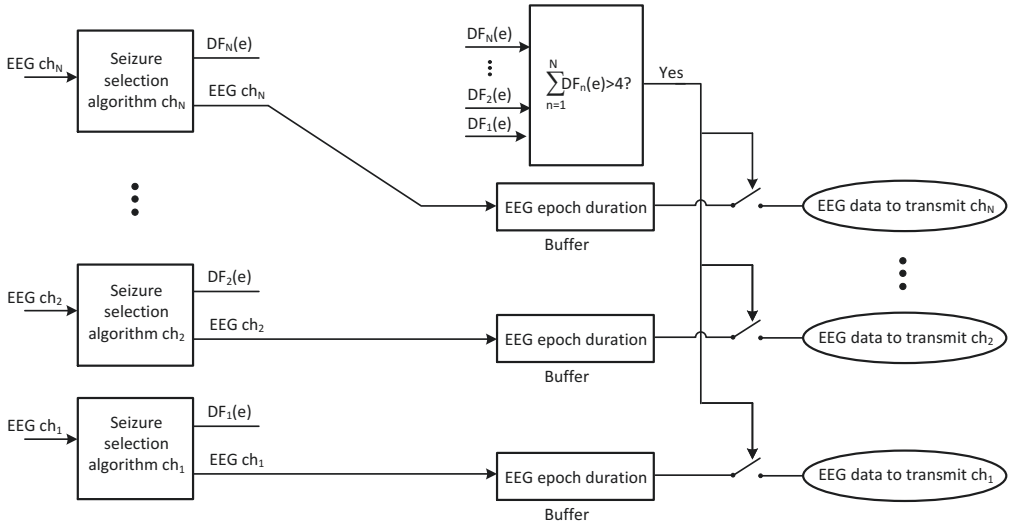


Figure 4.2: *Multi-channel seizure selection operation. Candidate data sections are transmitted if a detection is reported by more than 4 channels of the seizure selection algorithm.*

in Figure 4.2. A buffering stage stores the EEG for the duration of the epoch to compensate for the feature extraction process in the seizure selection algorithm. A section of EEG data is selected for containing likely seizure activity only if the number of channels with a detection of '1' is higher than a threshold of 4 (chosen empirically in [12]).

4.4 System architecture

The seizure selection system performs data reduction in the form of data selection, similar to the spike selection system presented in Chapter 3. Thus, top-level calculations of the seizure selection power budget are equivalent to the those carried out for the spike selection system in Chapter 3. A 32 channel WEEG system ([20]) with P_{TX} of 2.3 mW and a data reduction (C) of 50% will have 1.15 mW available to all stages of the algorithm hardware implementation. Assuming 50% of this power budget to be reserved for buffering the EEG data for the duration of an epoch, less than 17 μW of power will be available to each channel of the algorithm hardware implementation.

The system level implementation of the algorithm is shown in Figure 4.3. An initial low-pass filtering stage strongly attenuates the signal frequency components above 10 Hz to ensure that the signal can be subsequently sampled during the

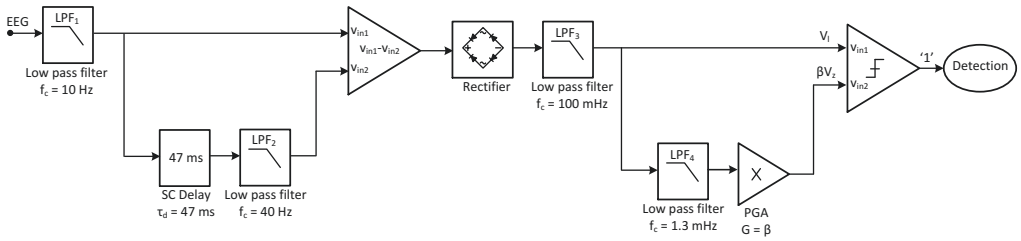


Figure 4.3: *System-level implementation of the data reduction algorithm*

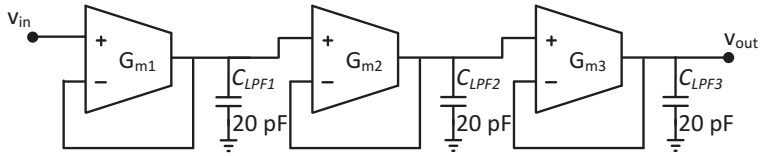
line length feature calculation at a reasonable sampling rate. The filter, shown in Figure 4.4(a), is created by cascading three first order G_mC low-pass filters with cutoff frequencies of 21 Hz, achieved using a biasing current of 200 pA for each filter OTA (see Figure 4.4(b)) and integrated capacitance of 20 pF for $C_{\text{LPF1-2}}$. The filter noise, referred to the circuit input and integrated over the 1 mHz to 10 Hz band, is 25.3 μV_{rms}. The THD at the filter output remains below 1% for input signal amplitudes less than 160 mV_{pp}. Considering 160 mV_{pp} as the input linear range, the filter dynamic range is found to be 76 dB.

The line length equation of Equation 4.1 is implemented by subtracting the original signal from a delayed copy of itself, followed by a rectifier and integrator. The delay element has been taken from the work of [21] and ported to a 0.18 μm CMOS process. The circuit operates by cascading six delay cells each consisting of two SC stages (shown in Figure 4.5) and controlled by complementary clock signals ϕ_1 and ϕ_2. The amount of delay introduced by each cell is calculated as

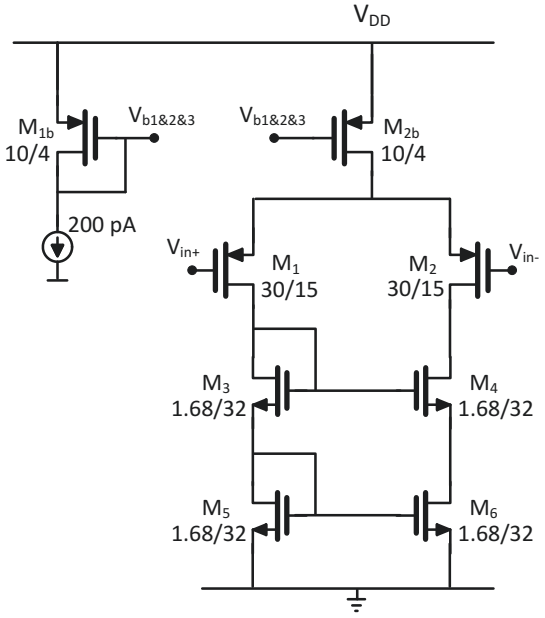
$$d = 2\big(1 - D\big)T \tag{4.7}$$

where D and T are the clock signal duty cycle and period respectively. The clock frequency was set to 128 Hz, resulting in an overall delay of 47 ms produced by the six cascaded delay cells (50% duty cycle). A single stage G_mC low-pass filter with a cutoff frequency of 40 Hz, placed after the delay circuit, effectively attenuates the distortion resulting from the clock signal frequency component and its harmonics.

The topology of the subtractor circuit is shown in Figure 4.6(a) and the core OTA used in this circuit is shown in Figure 4.6(b). As shown in Figure 4.6(a), the subtractor circuit utilizes quasi-infinite resistors (M_{Q1-Q2}) and capacitors (C_{1-2}), which form a high pass filter stage with a cutoff frequency of 20 mHz, to block the DC offset resulting from the previous circuitry. The circuit was designed to have a gain (-C_1/C_2) of -1. The negative sign is of no consequence since the subtractor



(a)



(b)

Figure 4.4: *Low-pass filter created by cascading three first order G_mC stages: (a) Top-level structure; (b) OTA circuit schematic.*

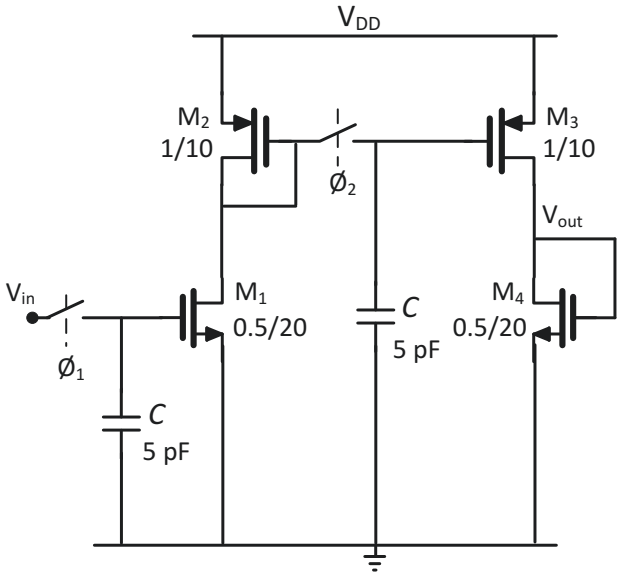
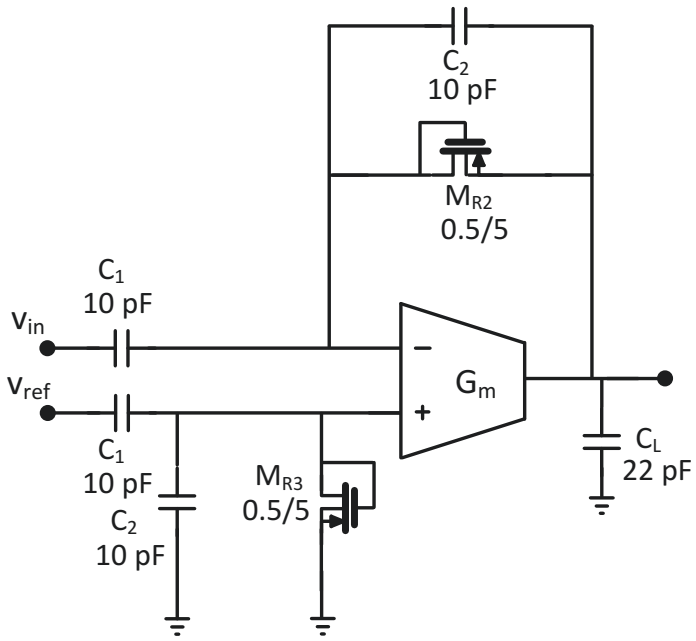


Figure 4.5: *Single stage of SC circuit used in the delay line*

output is subsequently passed through a full-wave rectifier. Using a capacitance value of 10 pF for both C_1 and C_2, unity gain is achieved within the 20 mHz to 500 Hz passband as seen in the simulated Bode magnitude response of the subtractor circuit, shown in Figure 4.7. The biasing current of the OTA was set to 12.5 nA and cascoded load devices ($M_3 - M_6$) were used to maintain the DC operating point. A PMOS input stage was used in the subtractor OTA (Figure 4.6(b)) to reduce the effect of low frequency noise on the subtractor output. Considering the bandlimited input to the subtractor, the input referred noise of this circuit, integrated over the 20 mHz to 10 Hz frequency range, was 33 μV_{rms}. With regards to the subtractor linear range, the circuit maintains a THD below 1% for input signal amplitudes less than 330 mV_{pp} in the 20 mHz to 10 Hz band.

The top-level architecture of the full-wave signal rectification stage was influenced by the concept proposed in [22], in which comparison results of the input signal (V_{in}) against a DC reference voltage (V_{ref}) is used to discriminate between the positive and negative signal polarities (see Figure 4.8). A low impedance path is provided to the outputs (V_{out1} and V_{out2}) of the non-inverting and inverting amplifiers (A_1 and A_2) upon selection based on the comparator output, through the switches (S_1 and S_2) which were implemented using minimum sized NMOS devices. The comparator, shown in Figure 4.8(b), is designed based on the architecture proposed



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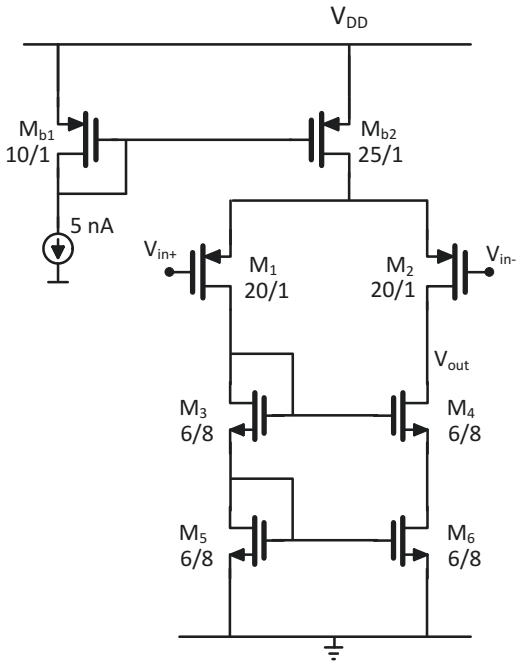


(b)

Figure 4.6: *Subtractor circuit to subtract the low-filtered input signal from a delayed copy of itself: (a) subtractor top-level design; (b) OTA circuit schematic.*

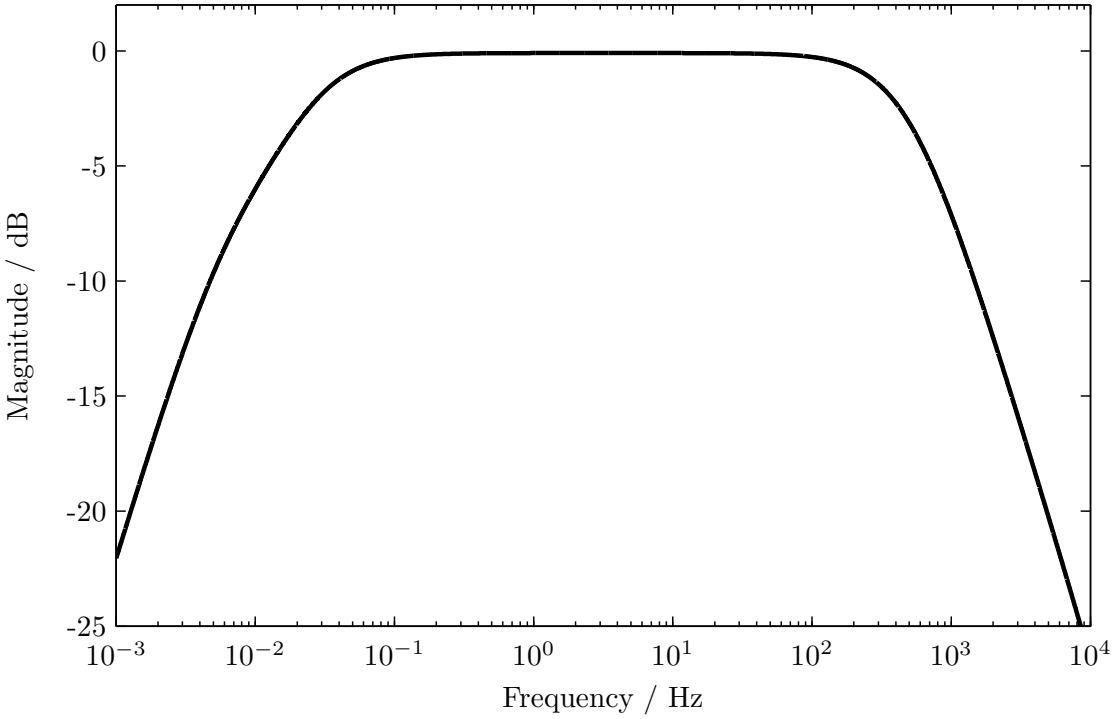
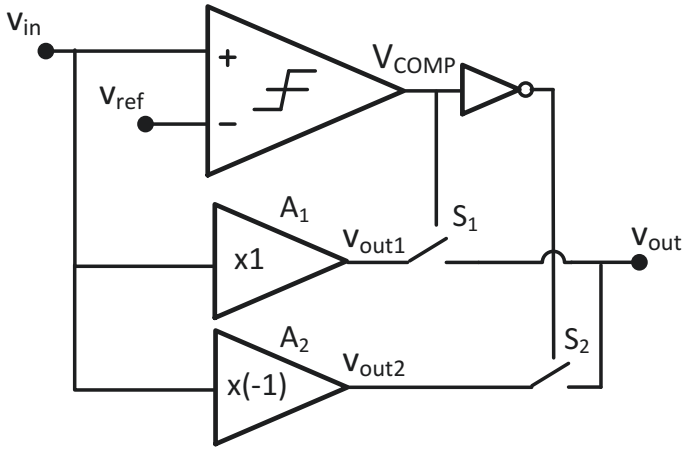


Figure 4.7: *Simulated frequency response of the subtractor circuit.*

in [23] and consists of a chain of three open-loop amplifiers (A_{rec1}, A_{rec2} and A_{rec3}). Two DC-blocking stages, created using two QIR devices (M_{R4} and M_{R5}) and 10 pF capacitors C_1 and C_2, are used to remove offset voltages at the outputs of A_{rec1} and A_{rec2}. Signals at the outputs of the three amplifiers will be injected on to the reference node, which will be connected to the reference inputs of all three amplifiers in the case of a direct connection between these nodes and the main reference voltage V_{ref}, potentially resulting in instability. This concern is alleviated by isolating the main reference voltage from the negative inputs to the amplifiers using the buffering stages A_{buff1} and A_{buff2}. The two amplifiers A_1 and A_2 were implemented using the two OTA pairs G_{m3}-G_{m4} an G_{m5}-G_{m6}, respectively, where all OTAs are identical. The circuit-level implementation of these OTAs is based on the schematic shown earlier in Figure 4.4(b), with a biasing current of 3 nA. The inputs to G_{m3} and G_{m5} were configured such that two versions of the input signal, scaled by factors of 1 and -1, are made available to the outputs V_{out1} and V_{out2}, simultaneously.

The input-output transfer function is derived by applying a 10 Hz sine wave input with amplitudes between 1 μV_{pk} and 200 mV_{pk} (2 μV_{pp} and 400 mV_{pp}) and calculating the average value of the rectified AC output ($\overline{V_{\text{out}}}$) [24], as shown in Figure 4.9. The ideal output response to the same input signal range, plotted



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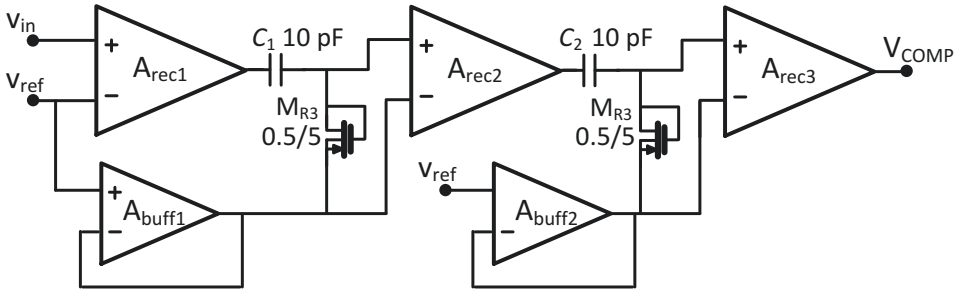

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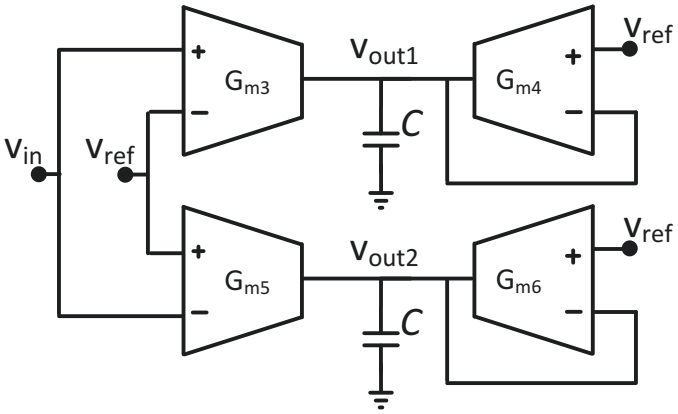


(c)

Figure 4.8: *Full-wave rectifier circuit: (a) Top-level topology; (b) Comparator architecture; (c) Inverting and non-inverting amplifiers used to pass the input signal to the output based on the comparator output.*

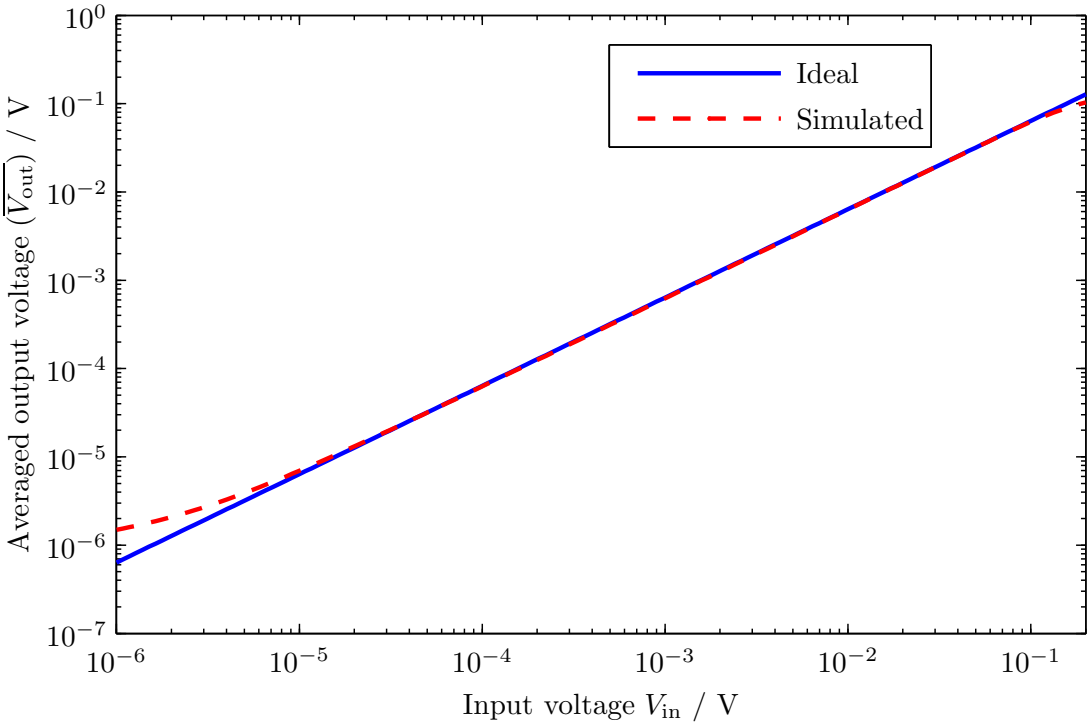


Figure 4.9: *Rectifier input-output transfer function simulated for inputs in the range of 1 μV_{pk} and 200 mV_{pk}.*

in the same figure, has a constant gradient of 0.636 ($\frac{2}{\pi}$). The gradient of the simulated circuit response deviates less than 5% from this value for the input range of 8 μV_{pp} to 166 mV_{pp}. The maximum input signal acceptable by the rectifier is taken as 166 mV_{pp}, corresponding to an averaged output voltage of 52 mV. The integrated output noise of the rectifier over the 1 mHz to 100 mHz band (inline with the bandwidth of the following low-pass filter), simulated using the periodic noise analysis (pnoise) tool in Cadence with an input at 10 Hz, was 35.2 μV_{rms}.

The low-pass filter following the rectifier, shown in Figure 4.10, effectively integrates the rectified signal to approximate the line length behaviour. The circuit is taken directly from the work of [25] and ported to a 0.18 μm CMOS process to be used here. The clocked switch used at the output node of the filter OTA controls the amount of current flowing into the integration capacitor (C_{int}) allowing for the OTA transconductance, and consequently the filter cutoff frequency, to be proportional to the clock signal duty cycle [25]. The effective current flowing into C_{int} can be defined as:

$$I_2 = \delta \times I_1 \tag{4.8}$$

where δ is the duty cycle of the clock signal (ϕ). The clock frequency has was to 128 Hz with a duty cycle of 4% to achieve a filter cutoff frequency of 100 mHz.

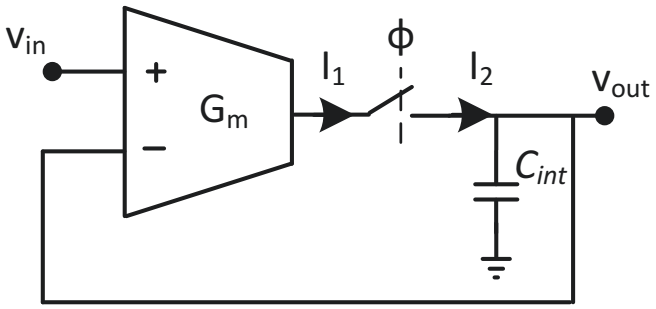


Figure 4.10: *Architecture of the low pass filter with a cutoff frequency proportional to the clock signal duty cycle.*

The moving average approximation of Equation 4.4 is suitable for a discrete time implementation. Considering a continuous time implementation, the transfer function of the moving average filter results in a filter with a cut off frequency of 1.3 mHz (see Equation 4.5). The low-pass filter of Figure 4.10 ([25]), was also used here to approximate the moving average filter using a 128 Hz clock with a duty cycle of 0.5%.

A Programmable Gain Amplifier (PGA) behaving as a multiplier is utilized to apply the user-set threshold values (β) to the background estimate. The PGA consists of two OTAs ($G_{m1} - G_{m2}$) as shown in Figure 4.11. The gain of the amplifier represents the user set threshold values and is set by the ratio of the two biasing currents ($I_{\text{tune}}/I_{\text{set}}$). The PGA gain is realized by setting I_{set} to 10 nA and varying I_{tune} to achieve a desired system performance after deciding on the specific tradeoff between sensitivity and amount of data reduction.

A comparator detects the time periods for which the line length output V_L is greater than the modulated background estimate (βV_Z). The comparator architecture, shown in Figure 5.6, includes three pre-amplification stages ($A_1 - A_3$) followed by a dynamic latch, taken from [26], and a D-flipflop. The preamplifiers are used together with offset sampling switches and offset storage capacitors to implement an output offset cancellation scheme (OOS) in order to reduce the effect of the comparator offset [27]. Current injecting devices (M_{i1}-M_{i2}) were used to increase the transconductance of the input transistors compared to the diode connected load transistors. The tail transistor M_b was biased to draw a current of 800 pA, 600 pA of which was supplied by the current injecting transistors, resulting in a

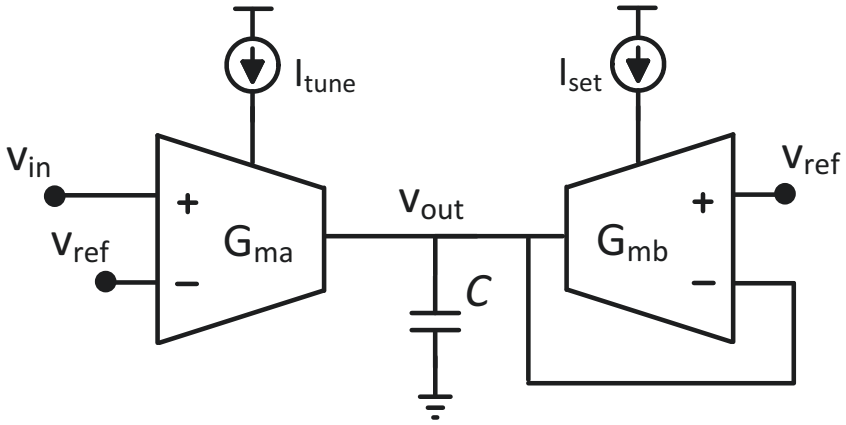


Figure 4.11: *Topology of the programmable gain amplifier. The amplifier gain is equal to the user set threshold (β) and is set by the ratio of the two currents I_{tune} and I_{set}.*

moderate gain (g_{m1}/g_{m3}) of 5.5 for each of the pre-amplifiers. Offset sampling and storage sections in the comparator circuit were realized using 0.5μm/0.3μm NMOS devices and 606 fF sampling capacitors. In 100 runs of Monte-Carlo simulations, shown in Figure 4.12, using an input ramp signal, the input referred offset of the comparator was found to be 24.3 μV.

The comparator output was sampled in 2 s intervals to create the effect of non-overlapping epochs inline with the epoch duration of the seizure selection algorithm (see Section 4.3).

4.5 System front end and control circuitry

The IA, which is designed based on the topology reported in [28], achieved a mid-band gain of 37 dB and input referred noise of 4 μV_{rms} integrated from 0.5-100 Hz. A current generation circuit was used to draw a reference current of 366 nA from the 1.25 V power supply. The IA and current reference circuits were designed by colleagues at Imperial College London. The currents required by the circuits in the seizure selection system were generated using scaled copies of the reference current. An 8b counter circuit using JK flip-flops followed by D flip-flops and combinational digital logic was used to scale-down a 32.6 KHz clock provided by

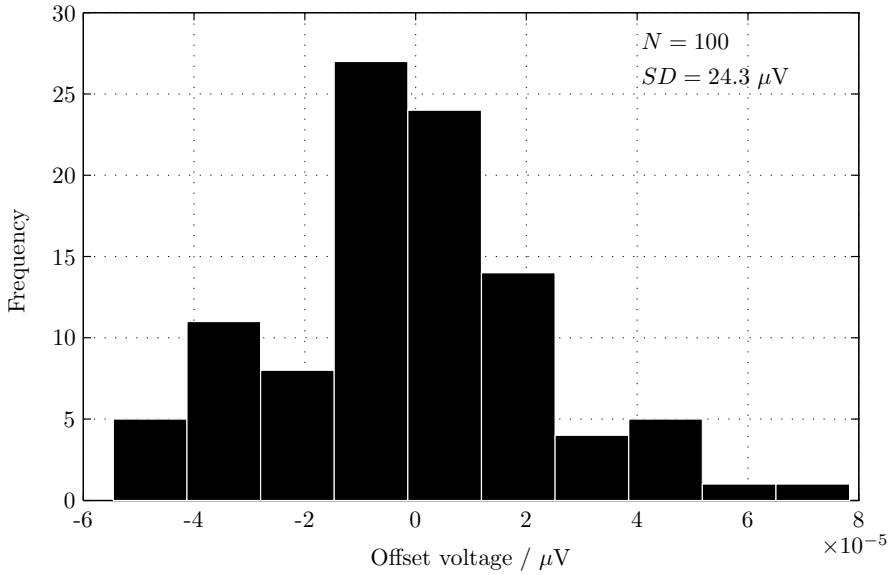


Figure 4.12: *Histogram of comparator input offset voltage.*

an off-chip oscillator and to generate the low duty cycle pulses required for the circuits in the system.

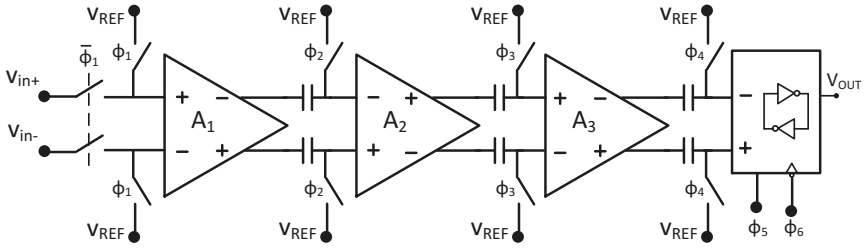
4.6 Fabrication and testing

4.6.1 Chip fabrication

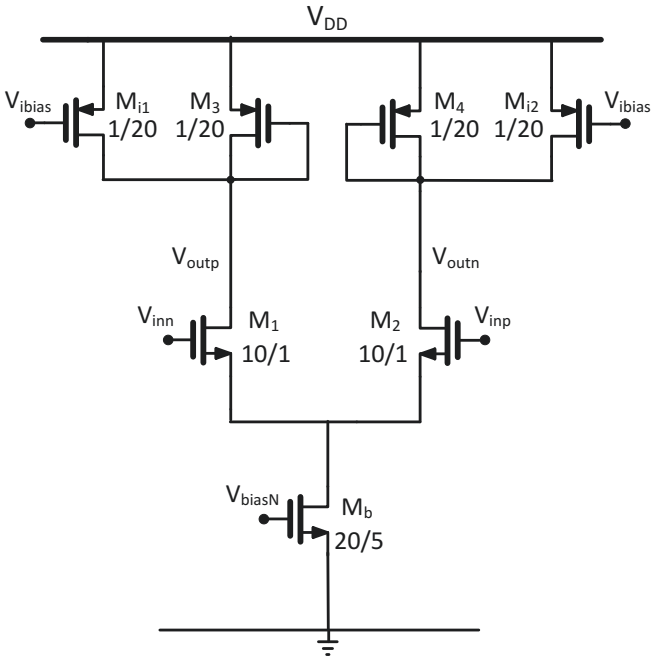
The seizure selection SoC was fabricated in a 0.18 μm, triple well 6 metal AMS CMOS technology. The chip padring was split into two separate padrings, in order to isolate sensitive analog circuitry from the noisy digital stages. The capacitance values mentioned in this chapter were achieved on-chip using Metal–Insulator–Metal (MIM) capacitors. The chip micrograph is shown in Figure 4.14 and the active area consumed by the seizure selection system is 1.48 mm^2.

4.6.2 Experimental results

A National Instruments NI USB-6259 data acquisition board (DAQ) has been used to feed the input signals to the chip and to gather the output results and intermediate test-points. The DAQ board introduces a highly capacitive load of 100 pF to its analog input signals and the implemented circuits generally have a low driving ability, not suitable for driving this off-chip load. Single stage analog buffer circuits with a biasing current of 40 μA, provided through separate 1.8 V



(a)



(b)

Figure 4.13: *Comparator producing the system output detection flag: (a) top-level architecture; (b) preamplifier schematic.*

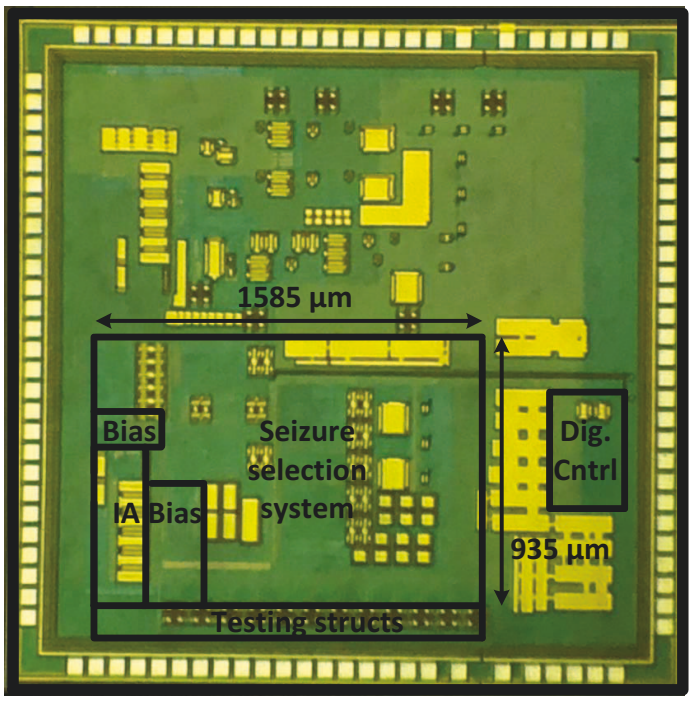


Figure 4.14: *Micograph of fabricated chip showing the seizure selection system with an active area of 1.48 mm^2.*

supply and ground pads, were placed on-chip after the analog test-points for testing purposes. A digital buffer was also placed after the decision flag output in order to maintain the integrity of the system detection results during the measurement process.

The EEG dataset used for the testing the system performance contained over 168 h of recordings from 21 patients and 34 marked seizure events from the UK National Hospital for Neurology and Neurosurgery, Freiburg University Hospital (Germany) and Katholieke Universiteit Leuven (Belgium) [29], [30]. A summary of the dataset is provided in Table 4.1 together with the number of events per patient and the percentage of data occupied by seizure activity (T_{seizure}). The 16 channels used for testing the system performance were chosen as the channels common to all recordings in the dataset, and are: C3, C4, CZ, F3, F4, FZ, F7, F8, FP1, FP2, O1, O2, T3, T4, T5, and T6.

A 700 s trace of EEG data from patient 5 (channel C3), shown in Figure 4.15, includes a marked seizure event (from 341 s to 416 s time marks) and is utilized to illustrate the system behaviour. The modelled and measured line length signal (V_L) and background estimate output (V_Z) in response to the input data trace is presented in Figure 4.16(a) and Figure 4.16(b), respectively. It can be seen that

Table 4.1: *Data used for testing the data reduction system performance.*

Patient	**Age at test**	**Gender**	**Marked seizure events**	**Seizure duration (s)**	**Recording duration**	$T_{seizure}$*(%)*
1	53	Female	1	118	02:20:50	1.39
2	33	Female	3	293	34:02:07	0.23
3	56	Female	7	827	66:59:38	0.34
4	41	Female	5	2029	19:54:17	2.83
5	35	Male	1	75	10:45:20	0.19
6	35	Male	1	102	12:04:50	0.23
7	60	Male	1	45	03:23:44	0.36
8	33	Male	1	97	04:08:57	0.64
9	23	Female	1	38	01:08:00	0.93
10	34	Male	0	0	02:00:11	0
11	Unknown	Male	0	0	04:00:22	0
12	22	Female	1	94	00:49:59	3.13
13	35	Female	6	109	00:31:55	5.69
14	46	Female	1	148	00:06:12	39.78
15	Unknown	Unknown	3	98	00:26:42	6.11
16	Unknown	Female	2	85	00:21:39	6.54
17	47	Female	0	0	02:00:11	0
18	45	Female	0	0	00:46:19	0
19	43	Male	0	0	00:15:15	0
10	47	Male	0	0	02:00:11	0
21	28	Female	0	0	02:00:11	0
Total	-	-	34	4158	168:57:31	0.68

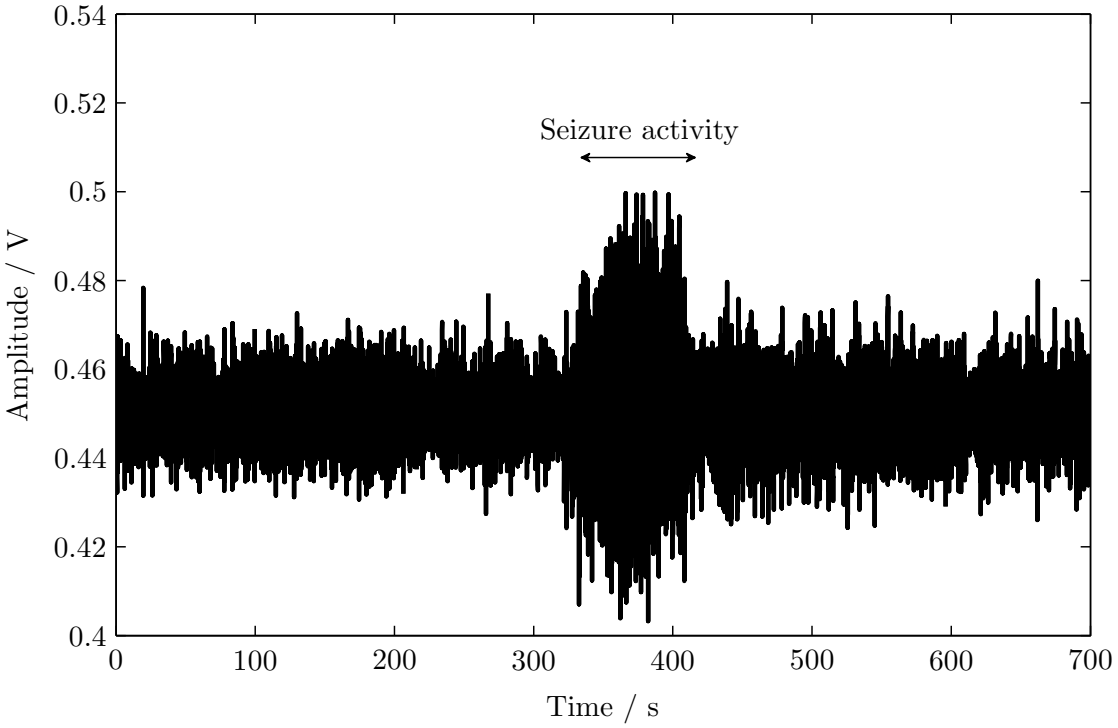


Figure 4.15: *A 700 s section of EEG containing a seizure event with a duration of 75 s (from 341 s to 416 s time marks).*

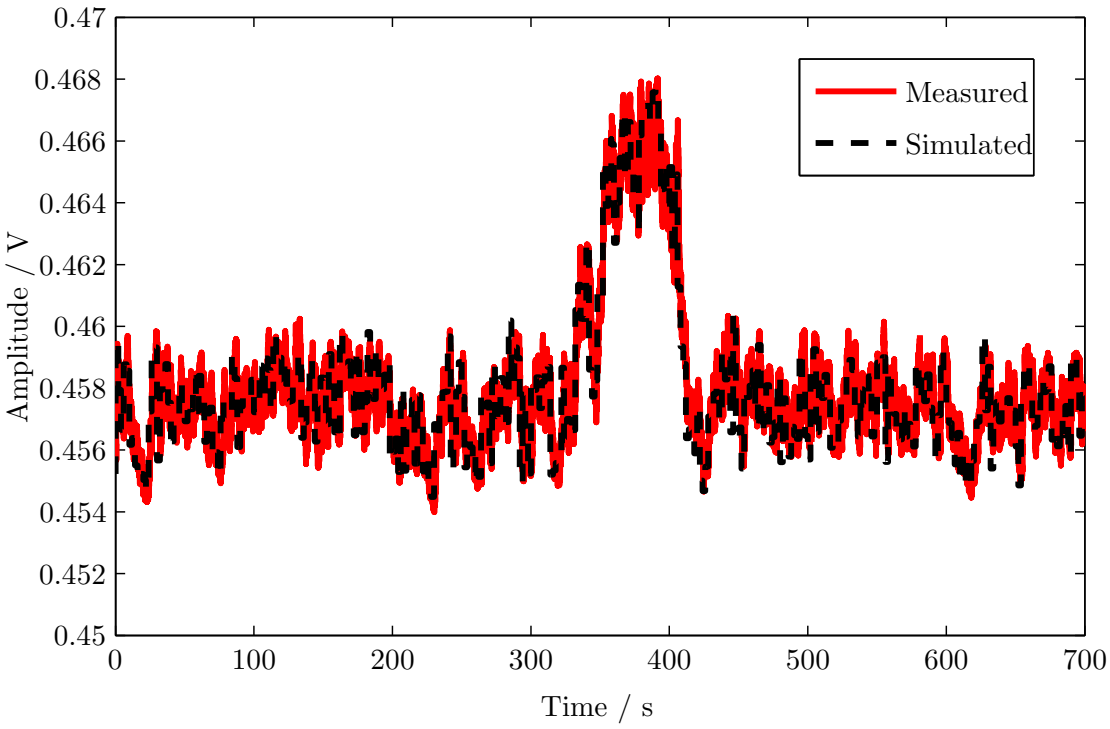
the measured signals (shown with a solid line) are inline with the shape of the modelled (shown with a dashed line) results. The system detection flag output (V_{DF}) is also shown in Figure 4.17.

The indices used to report the system performance are sensitivty and percentage of data transmitted. In order to distinguish between the number of seizure events correctly identified by the system and the number of identified seizure epochs, two variants of sensitivity have been used in this work which are event sensitivity and epoch sensitivity. Event sensitivity is calculated as:

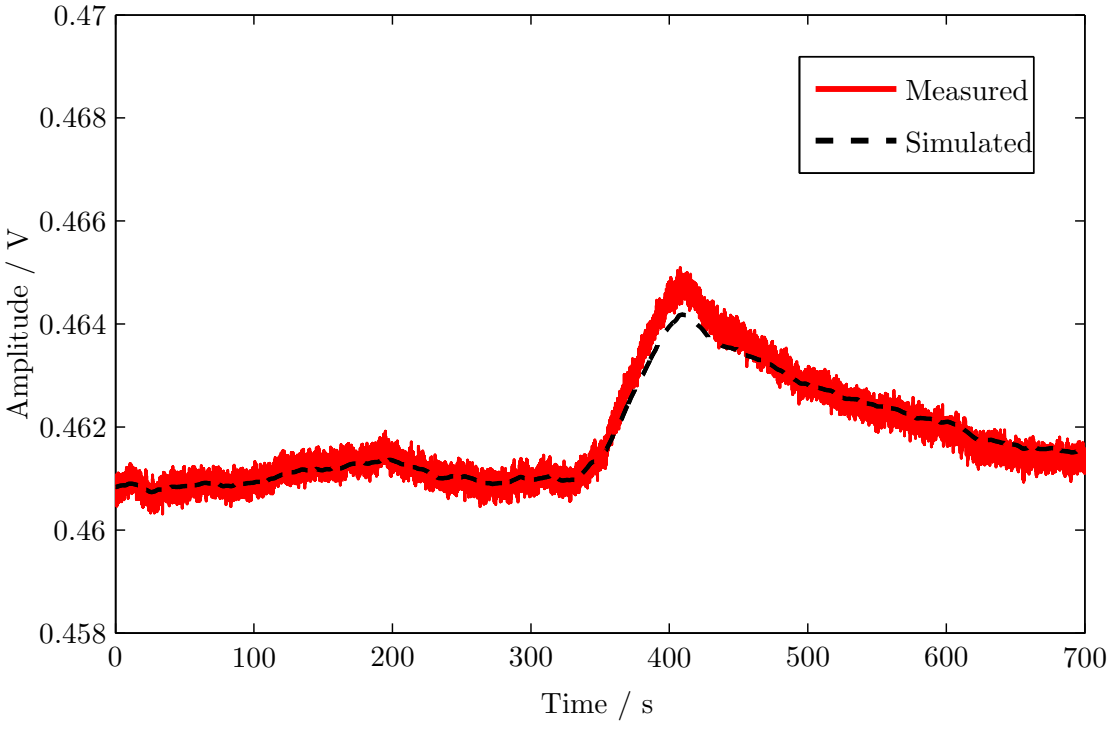
$$\text{Event Sensitivity} = \frac{TP_{ev}}{TP_{ev} + FN_{ev}} \times 100\% \tag{4.9}$$

where TP_{ev} is the number of True Positives (TP) and is equal to the number of correctly identified seizure events. The number of seizure events that have not been identified by the system are counted as False Negatives FN_{ev}. The calculation of epoch sensitivity followed the general form of Equation 4.9, as:

$$\text{Epoch Sensitivity} = \frac{TP_{ep}}{TP_{ep} + FN_{ep}} \times 100\% \tag{4.10}$$



(a)



(b)

Figure 4.16: *System outputs in response to the input EEG trace: (a) Line length calculation (V_L); (b) Output of moving average approximation (V_Z).*

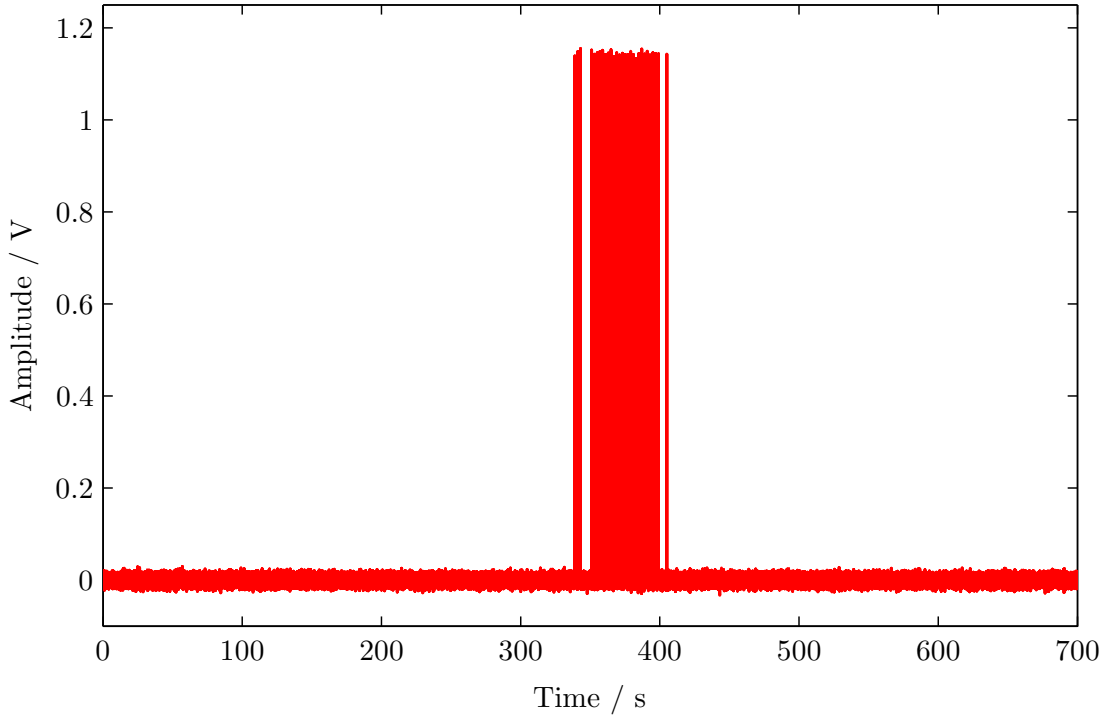


Figure 4.17: *System detection flag output in response to 75 s of input EEG.*

where TP_{ep} and FN_{ep} are the number of correctly detected seizure epochs and incorrectly rejected seizure epochs, respectively.

Considering the 75 s seizure event present in the input EEG trace of Figure 4.15, and the epoch duration of 2 s used in the seizure selection system, a single detection by the system during any of the 37 epochs will result in an event sensitivity of 100%. However, to achieve an epoch sensitivity of 100%, the system must correctly identify all present epochs as seizure epochs resulting in 37 detections. Considering the input trace of Figure 4.15 alone, the detection flag output of Figure 4.17 indicates that the presented seizure selection system was able to identify the seizure event (event sensitivty of 100%), while correctly detecting 29 out of the 37 seizure epochs present, resulting in an epoch sensitivity of 78.3%.

When testing the system performance on data obtained from patients during long recording periods, where the duration of seizure events is insignificant compared to the total duration of the recordings, the percentage of data transmitted was very close to 1 − specificity. System specificity was derived using Equation 5.10 where TN_{ep} and FP_{ep} are the number of correctly rejected non-seizure epochs (True Negatives) and the number of incorrectly detected non-seizure epochs (False Positives), respectively.

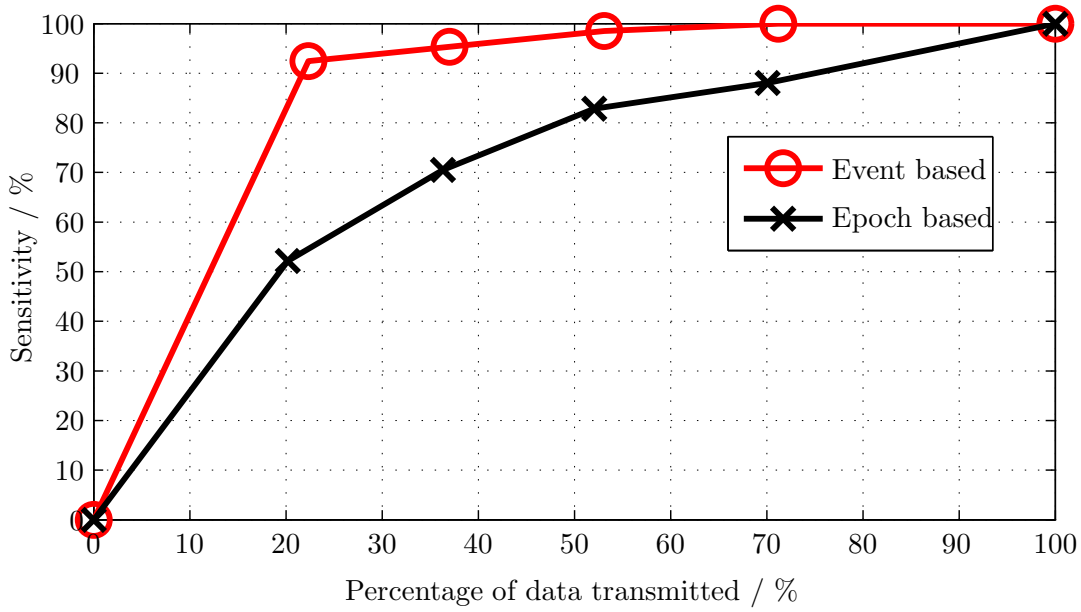


Figure 4.18: *System performance tradeoff curve.*

$$\text{Specificity} = \frac{TN_{ep}}{TN_{ep} + FP_{ep}} \times 100\% \tag{4.11}$$

In order to keep the duration of the measurement process across the dataset of Table 4.1 reasonable, the values of the sensitivity and percentage of data transmitted indices were calculated and averaged across all epochs using four threshold (β) values of 0.9, 1.1, 1.3 and 1.5. The system performance tradeoff curve is shown in Figure 4.18. It can be seen that the system was able to achieve an epoch sensitivity of 82.8% and an event sensitivity of 98.5% for a percentage of data transmitted of 52.5%. In comparison, for the same percentage of data transmitted, the mathematical model of the data reduction algorithm achieved an event sensitivity of 100% and epoch sensitivity of 85%. The difference in the results is due to the mathematical approximations carried out in the original algorithm in order to aid the analog implementation.

The performance metrics must be considered in the context of the system aim, namely data reduction and power savings for a WEEG system for the long-term monitoring and diagnosis of epilepsy. It is expected that performance results achieved for the system event sensitivity will be higher than that of epoch sensitivity, since it is easier to detect a single seizure event as opposed to detecting all seizure epochs present in the input EEG data. Event sensitivity is an essential metric for real-time treatment systems that require a seizure event to be detected to allow for focal treatment and prevent seizure progression. This metric is also

Table 4.2: *System performance summary.*

CMOS Process	0.18 μm	
Area	1.48 mm^2	
Supply Voltage	1.25 V	
Sensitivity	83%	
Fraction of data transmitted	52%	
Current consumption (nA)	LPF_1	2
	SC delay line	622
	LPF_2	5
	Subtractor	32
	Rectifier	172
	LPF_3	5
	LPF_4	5
	PGA ($\beta = 1.1$)	56
	Comparator	5.5
	Digital circuitry	5
	Total	910

useful in the context of seizure counting systems, where the presence of a seizure event will be noted in the automatically generated diary once an event is detected. However, epoch sensitivity is an essential metric for seizure selection systems since the aim is not only to identify seizure occurrence, but also to correctly identify sections of data containing candidate seizure activity. A higher number for this metric would indicate that a larger percentage of interesting EEG data has been successfully selected for transmission, which will lead to increased accuracy in the diagnosis.

Furthermore, higher sensitivity and specificity can be achieved using signal processing chains with higher complexity. However this will be achieved at the the cost of increased power consumption for the system hardware implementation and ultimately the WEEG unit.

A summary of the seizure selection SoC performance is shown in Table 4.2. The fabricated chip consumed 910 nA from a 1.25 V supply resulting in a power consumption figure of 1.14 μW, which is only 6.7% of the available power budget of 17 μW per channel calculated for the hardware implementation of the algorithm in Section 4.4. In addition, the power consumed by the presented analog-based

Table 4.3: *Power comparison of conventional wireless EEG (no data reduction) and WEEG incorporating seizure selection stage.*

	Wireless EEG	Wearable EEG ($C = 0.5$)
IA array [6]	112 μW	112 μW
ADCs (12b, 500 S/s) [32]	6.4 μW	6.4 μW
Data reduction array	-	36.48 μW
Transmitter [33] Active: 192Kbps×11nJ/b	2112 μW	2112 μW×0.5
Total	2230.4 μW	1210.88 μW
Operational time	110.29 hours	203.15 hours

SoC was smaller than the power figure of 23 μW consumed by the digital ASIC implementation of the same seizure selection algorithm of Section 4.4 [31], by a factor of 20×.

The potential power savings realized by incorporating the presented seizure selection system as part of a WEEG unit, in comparison to a wireless EEG unit with no data reduction, are illustrated in Table 4.3. It has been assumed that both units incorporate 32 channels consisting of an array of IAs, ADCs and a transmitter. The power figures for the IA and ADC are taken from the works [6] and [32], which are implemented in 0.18 μm CMOS process, as 3.5 μW and 200 nW respectively. An energy per bit transmitted value of 11nJ/b is used to calculate the power consumed by the transmitter, based on the performance of the commercially available CC2640R2F module [33]. The data reduction provided by the seizure selection system incorporated in the WEEG system is assumed to be 50% ($C = 0.5$). The total power consumption figures calculated in Table 4.3 demonstrate that the power consumed by the device can be reduced by 45.7% when utilizing the seizure selection system as part of the WEEG device, in comparison to a wireless device consisting of the same components except the data reduction stage. With regards to operational lifetime from a miniature battery, such as the battery of [34], with an energy capacity of 246 mWh, the WEEG device operation time is extended to over 8 days as a result of the mentioned data reduction, in comparison to the conventional wireless device which can run continuously for over 4 days.

Based on the power figures presented in Table 4.3, it can be noted that the power

overhead of the seizure selection system is negligible compared to the overall power consumed by the other components in the WEEG device. Therefore, the achieved power savings can also be capitalized on by introducing additional discriminatory features that can be mapped to hardware implementations with low complexity into the presented system in order to improve the system performance in terms of sensitivity and data reduction.

4.7 Discussion

The majority of epileptic patients experience less than 12 seizure episodes a year and, despite their importance for clinical diagnosis, seizure events are less likely to be captured during routine EEG tests. This chapter presented the design and experimental results for a low-power seizure selection system that would benefit the realization of truly WEEG devices to aid epilepsy diagnosis by operating continuously for over 8 days. Significant power savings can be achieved by using the system, since only sections of EEG data containing likely seizure activity are selected for transmission. In addition, the amount of data presented to the neurologists can be reduced as a result of the data reduction performed by the system, resulting in less time required for the diagnosis process.

Rather than using a patient-specific approach to identify different types of seizures, the presented system relies on the line length feature, implemented using an analog delay element, subtractor, full-wave rectifier and integrator, to discriminate between seizures and background activity. The complex median operation used in the algorithm of [12] was replaced with a moving average filter in the system presented here, allowing for a low-power continuous time approximation using a single stage low-pass filter. An analog-based design approach allows for the seizure selection system to operate with a power consumption figure 20 times less than the power consumed by the digital ASIC implementation of the same algorithm.

The seizure selection system was fabricated using a 0.18 μm CMOS process. The system consumed 1.14 μW and was able to correctly identify 83% of seizure epochs while achieving a data reduction of 48%.

The power consumed by the seizure selection system could potentially be reduced even further by optimizing the delay circuit used in the line length calculation. Referring back to Table 4.2, it can be noted that the delay circuit power consumption accounts for almost 68% of the total system power. Although not verified here, future work could look at utilizing high-threshold transistors (available in the CMOS process used for the chip fabrication) in the delay circuit design to optimize the

power consumed by this circuit. Nonetheless, the power figure achieved by the fabricated seizure selection system is only 6.7% less than the power budget calculated for the system in this chapter.

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5 A 515 nW sleep spindle detection System-on-Chip

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5.1 Introduction

Human sleep is a dynamic process that can be divided into the two distinct states of Nonrapid Eye Movement (NREM) and Rapid Eye Movement (REM). The NREM stage consists of three separate stages (N1, N2 and N3). Sleep spindles are micro-events within the sleep EEG and are considered as the hallmark of the N2 sleep stage. Identiying these events would allow for marking the begining and continuation of the N2 stage of sleep. Sleep spindles are also known to play an important role in memory consolidation during sleep [1].

Ongoing research on sleep spindles suggests that the importance of these events is not limited to the study of sleep. Sleep spindles are also of clinical importance, as active research indicates that changes in spindle density and frequency are observed in a range of clinical disorders such as epilepsy, sleep disorders (e.g. sleep walking and sleep terrors), schizophrenia, autism, mental retardation and neurodegenerative diseases [2]. The study of [3] found a decrease in sleep spindle activity in youth with Major Depressive Disorder (MDD) and those at high risk for the illness. A number of studies have shown that sleep spindles may be an indicator of intellectual ability. A thorough review of these studies was carried out in [4], ultimately suggesting a curvilinear relationship between sleep spindles and learning potential, where individuals with a high number of sleep spindles can have a low or high IQ. The more recent study of [5] found the association of sleep spindles with

intellectual performance to be prominent in females.

The number of spindles observed during an all-night sleep recording is typically in the range of 200 to a 1000 [6]. According to the American Academy of Sleep Medicine (AASM) manual for scoring of sleep and sleep associated events [7], sleep spindles are trains of distinct waves with a frequency in the range of 11-16 Hz (most commonly 12-14 Hz) and a duration larger than 0.5 seconds. Spindle frequency bounds that are both wider and narrower than the frequency range defined by the AASM, including the 11.5-15 Hz, 11.5-16 Hz, 11-15 Hz, 11-16 Hz, 10.5-16 Hz and 10-16 Hz bands, have been previously proposed in the literature for the purpose of spindle detection [8]. It can also be noted that no recommendations regarding the amplitude of sleep spindles has been proposed by the AASM. Although it would be difficult to realize universal bounds for the amplitude of spindle activity, previous works have attempted to use lower voltage thresholds between 8 μV and 25 μV for spindle detection [8].

This chapter presents an ultralow-power SoC, fabricated in a 0.18 μm CMOS technology, to detect sleep spindles using a single channel of EEG. The presented system could be used either on its own in the form of a WEEG solution, to allow for the long-term monitoring of sleep and aid the diagnosis of sleep disorders by reporting the frequency of spindles during sleep; or as part of a different SoC in combination with other reported low complexity algorithms incorporating further detection of additional sleep, or disease related features. To the best of the author's knowledge, this is the first implementation of a sleep spindle detection algorithm in the form of an ASIC. A literature review on spindle detection algorithms implemented in the software domain, is presented in Section 5.2. A number of discrete hardware based spindle detection systems, implemented using off-the-shelf components, have previously been reported in the literature and these have been included in the literature review of Section 5.2. This is followed by an explanation of the mathematical characteristics of the sleep spindle detection algorithm which utilizes the Teager Energy Operator (TEO) together with the Spectral Edge Frequency - 50% (SEF50) to detect spindle events and is used as a foundation for the SoC presented in this chapter, in Section 5.3. Subsequently, the system architecture together with individual sub-blocks and circuits implemented in the system, have been explained in detail in Section 5.4. The measured performance results of the fabricated chip are presented in Section 5.5.

5.2 Sleep spindle detection

Traditionally, sleep spindles have been identified in sleep clinics by inspection of EEG traces by a specialist. This is very laborious and financially costly. Therefore, it would be useful to have a system for automatic detection of sleep spindles, without the requirement for human intervention. Furthermore, a hardware implementation of a low complexity automatic detection system may prove to be appealing since the system, as a whole, could be used to avoid the costly and time consuming setup required for clinical recordings of spindles.

Feature extraction was carried out in the algorithm of [9] by utilizing the Short Time Fourier Transform (STFT), prior to using Artificial Neural Networks (ANNs) and Support Vector Machines (SVMs) for sleep spindle classification. The algorithm performance was reported as an average accuracy of 88.7% and 95.4% for the ANN and SVM based classifiers, respectively. The work of [10] also used an ANN and SVM to independently classify features obtained using the Adaptive Autoregressive (AAR) method, reporting sensitivity figures of 89.1% and 94.6% for ANN and SVM classifiers, respectively. Classification of spindle events in bandpass filtered EEG was carried out in [11] using an ANN and without feature extraction. The sensitivity and specificity figures achieved by the network are in the range of 79.2% to 87.5% and 88.4% to 97.3%, respectively.

A four stage spindle detection approach was proposed in the work of [12]. An initial search for EEG zones containing candidate spindles (analysis zones) is carried out in the first stage based on Average Power (AP) calculation and thresholding in the frequency domain. The resulting analysis zones are used in the second stage, where Empirical-Mode Decomposition (EMD), FFT and Hilbert-Huang transform (HHT) are applied together with amplitude, frequency and duration criteria to select candidate spindles. Candidate events from the second stage are filtered and validated using morphological and frequency information in the third stage and mimicking expert analysis in the final stage. The algorithm achieves sensitivity and specificity figures of 88.2% and 89.7% respectively.

Signal content is limited to the spindle frequency range, using a bandpass filter, in the initial stage of the algorithm proposed in [13]. The filtered signal is then subjected to adaptive thresholding, using the statistical properties of the signal, and timing criteria to detect candidate spindles. The FFT is used in a parallel path to ensure that the maximum signal frequency is within a predefined band. A detection is reported by the algorithm in response to a candidate spindle being chosen by both paths. The algorithm performance was characterized as a sensitivity

of 78.44% and a specificity of 88.62%.

Matching pursuit (MP) was used in the work of [14], which reported sensitivity and specificity of 80.6%. A method for individual adjustment of amplitude and frequency criteria of spindle analysis was proposed in [15], achieving sensitivity and selectivity of 92.9% and 41.5% respectively. The normalized amplitude of STFT at 12 Hz, Discrete Wavelet Transform (DWT), Teager Energy Operator (TEO) and harmonic decomposition were used in the work of [16] to identify spindle events, yielding a sensitivity and specificity of 96.17% and 95.54% respectively.

Spindle detection using the FFT and spindle amplitude analysis yielded the best performance, with sensitivity and specificity of 70% and 98.6% respectively, amongst the four detection methods developed and compared in [6]. A fusion of two spindle detectors were used in the work of [17] to identify spindles based on bandpass filtering the input signal, time varying thresholding and power features. The algorithm obtains mean sensitivity and specificity figures of 84.6% and 95.3% respectively. The amplitude-frequency spindle distribution was modelled in the algorithm of [8]. Subsequently, spindles are detected when their amplitude-frequency features are within a certain interval of the the model. The algorithm was subjected to two seperate datasets for adults and children, achieving sensitivity and specificity pairs of $(78.5\%, 94.2\%)$ and (75.1%,96.7%), for the two datasets respectively.

Spindles were detected in [18] using the synchrosqueezing transform, which is a recently developed time-frequency signal analysis tool designed for signal decomposition into components with time-varying oscillatory features with robustness to the input signal errors. Using this method, the algorithm achieved sensitivity and specificity figures of 96.5% and 98.1%.

A summary of the mentioned literature is shown in Table 5.1. It can be noted that in general, a good level of performance is achieved with sensitivity and specificity figures larger than 78% and 80%, respectively. However, a direct comparison between the performance results is difficult due to the different datasets used for testing algorithm performance in the literature [19], [8]. Furthermore, none of the mentioned literature commented on the complexity of the implemented algorithms in the context of a hardware implementation with a stringent power budget imposed by a small sized battery. This is expected, as the main trend followed in the literature on spindle detection software is to improve on algorithm accuracy with the assumption that the algorithm will eventually run on a computing unit with no restrictions on power consumption (e.g. desktop computers available in sleep clinics).

Discrete hardware based approaches for spindle detection have also been intro-

Table 5.1: *Summary of literature review on sleep spindle detection algorithms.*

Reference	Year	Detection method	Sens. (%)	Spec. (%)	Sel. (%)
[9]	2002	STFT & ANN		Accuracy (AAN): 88.7	
		STFT & SVM		Accuracy (SVM): 95.4	
[10]	2004	AAR & ANN	89.1	N/A	N/A
		AAR & SVM	94.6	N/A	N/A
[11]	2005	Filtering & ANN	79.2-87.5	88.4-97.3	N/A
[13]	2006	Filtering & Threshold & FFT	78.44	88.62	N/A
[14]	2006	MP	80.6	80.6	N/A
[6]	2007	FFT & Amplitude analysis	70	98.6	N/A
[15]	2009	Individual adjustment	92.9		41.5
[16]	2009	STFT & DWT & TEO	96.17	95.54	N/A
[12]	2010	EMD & FFT & HHT	88.2	89.7	N/A
[17]	2012	Filtering & Threshold & Power features	84.6	95.32	N/A
[8]	2013	Amplitude-frequency distribution	(Adult dataset) 78.5	94.2	N/A
			(Child dataset) 75.1	96.7	N/A
[18]	2015	Synchrosqueezing Transform	96.5	98.1	N/A

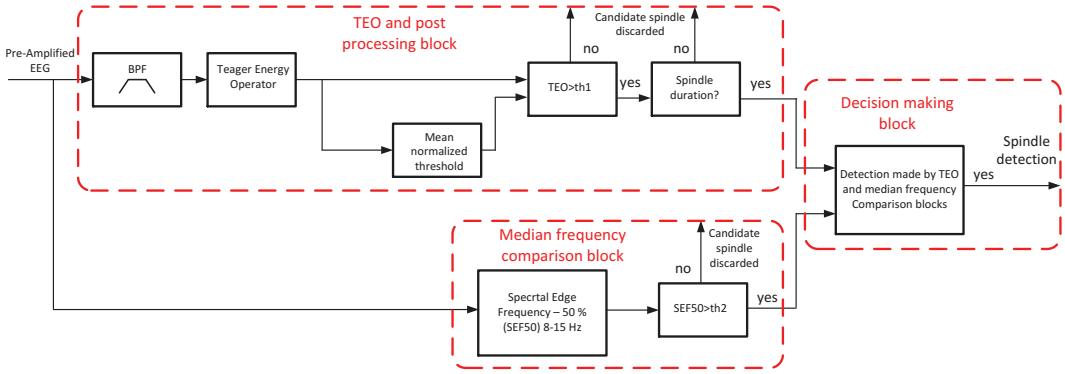


Figure 5.1: *Operational overview of the sleep spindle detection algorithm. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

duced by [20], [21] and [22]. They all use low complexity algorithms implemented using off-the-shelf components. Out of these, the only system that had power consumption as a target was the one in [22]. This system was based on the low complexity line-length feature, and implemented on a TI MSP40 microcontroller. The reported power consumption was 56.7 μW, achieving sensitivity and specificity values of 83.6% and 87.9% respectively.

5.3 Sleep spindle detection algorithm

The sleep spindle detection algorithm previously reported in [23] serves as a foundation for the SoC presented later in this chapter. The algorithm only requires a single channel of EEG input to identify spindles using the TEO and Spectral Edge Frequency (SEF). An overview of the algorithm operation is shown in Figure 5.1. The algorithm has been partitioned into three separate sub-sections here to aid the explanation of individual circuits presented in Section 5.4. These sub-sections are named as 'TEO and post processing block', 'median frequency comparison block' and 'decision making block'.

The single channel EEG input signal is initially amplified and filtered using a front-end amplification stage with highpass and lowpass cutoff frequencies of 0.3 Hz and 1 KHz, respectively. This input signal is then fed to a second-order bandpass filter with lower and upper cutoff frequencies of 11 Hz and 16 Hz, as shown in Figure 5.1. This filter is used to attenuate frequency content out of the spindle

frequency range.

Subsequently, a TEO stage estimates the instantaneous signal energy. The TEO ([24]) is a useful tool in highlighting sudden changes in signal levels. Since the input signal to the TEO is already within the spindle frequency range, a rise in signal energy levels will be seen at the output of this stage in response to spindle activity. The output of the TEO stage is segmented into epochs with a duration of 250 ms and an overlap of 50%. Candidate spindle events are identified in the following thresholding stage. The mean value of the TEO signal over the previous 60 epochs is calculated and the threshold is defined as 2.19 times this mean value. This multiplication factor was chosen empirically in [23]. Therefore, an epoch would be considered as a candidate spindle at any given time section by the algorithm if all samples in that epoch are greater than the running mean of the previous 60 epochs by a factor of 2.19. The calculation of the threshold in this form would allow for a fixed multiplication factor to be used to identify candidate spindles, regardless of the amplitude of the input EEG signal.

In the following stage of the algorithm, timing constraints in the form of minimum and maximum spindle duration are applied to the spindle under investigation. If the duration of the candidate spindle was found to be greater than 3 seconds or less than 500 ms, the candidate is discarded and not subject to any further analysis.

The next stage of the algorithm consists of the calculation of Spectral Edge Frequency - 50 % (SEF50), also known as the median frequency (f_{med}). The spectral edge frequency at 50% is defined as the frequency below which 50% of the signal energy is present. This stage will only be activated if the candidate spindle obeys the mentioned timing constraints. The SEF50 is analyzed in the 8-15 Hz frequency range to cover the spindle frequency range and alpha activity. As a result, this stage is highly specific and reduces the number of false detections by removing non-spindle sections of EEG, that may have been chosen as candidate spindles incorrectly, and alpha rhythms that may have been incorrectly detected by the previous stages of the algorithm. The SEF50 is obtained using a 512-point FFT operation in [23].

5.4 System architecture

A system-level design of the algorithm is shown in Figure 5.2 and partitioned using similar names for the sub-sections as used in the previous section.

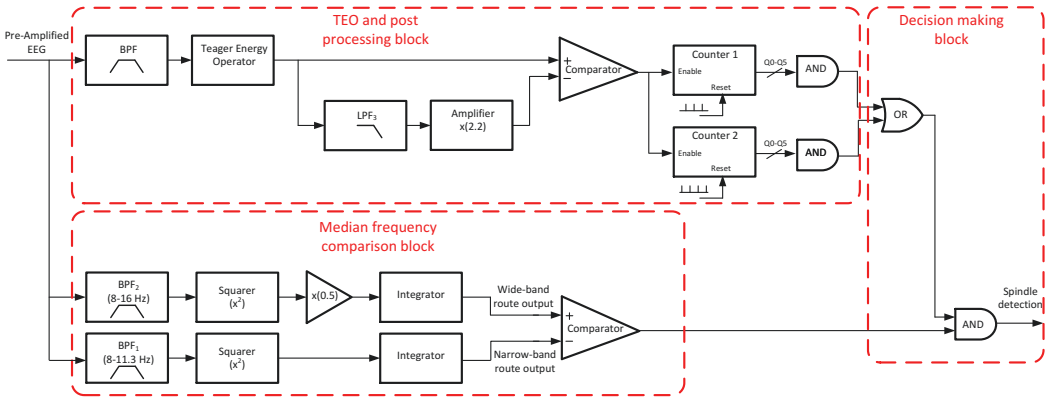


Figure 5.2: *Proposed system architecture. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

5.4.1 TEO And post-processing block

The Teager energy operator (TEO) is a non-linear time domain operator used to estimate the instantaneous energy of a signal. The TEO is defined in continuous and discrete time forms as Equation 5.1a and Equation 5.1b respectively [24].

$$\Psi[x(t)] = \left(\frac{dx(t)}{dt}\right)^2 - x(t)\frac{d^2x(t)}{dt^2} \tag{5.1a}$$

$$\Psi[x(n)] = x^2(n) - x(n-1)x(n+1) \tag{5.1b}$$

Analog circuit-level implementations of the TEO have mostly been based on continuous time derivations using high-pass filtering stages as differentiators, multiplier blocks and summing circuitry [25], [26]. In the case of using a high pass filter to approximate an ideal differentiator, the filter has to be designed to have a corner frequency much larger than the input signal bandwidth. This results in an attenuating effect on the input signal and a reduced Signal-to-Noise Ratio (SNR) at the filter output. Because of this, equation Equation 5.1b was chosen in this work instead. A block diagram of the TEO circuit is shown in Figure 5.3. Similar to the approach in [27], each of the delay elements in Equation 5.1b was modelled using a low pass filter (LPF_1 and LPF_2 in Figure 5.3). The low pass filters were created by cascading two first order GmC low pass filters with cutoff frequencies of 65 Hz, achieved by setting a biasing current of 250 pA for each of the filter OTAs together with an integrating capacitor (C) of 8.5 pF. An added advantage of using

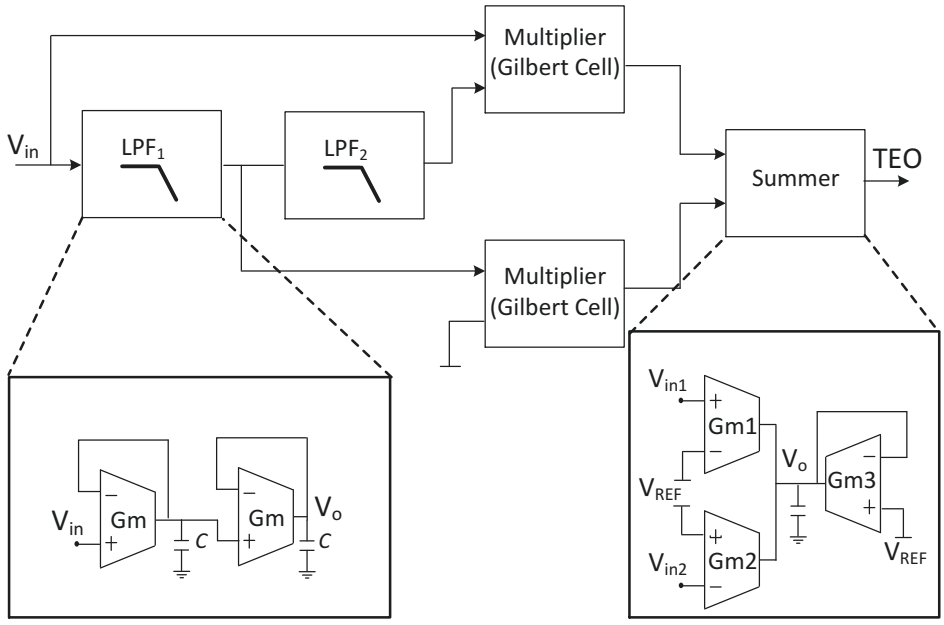


Figure 5.3: *Block diagram of the Teager energy operator. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

this approach is that the low-pass filter attenuates the high frequency components remaining on the signal at the input of the TEO circuit.

Furthermore, since the input signal to the TEO circuit is fairly band-limited (11-16 Hz) to the sleep spindle frequency range, the low pass filter nearly constant group delay of 4 ms with a 1% variation across the mentioned bandwidth is acceptable.

The multipliers in Figure 5.3 were implemented using the standard Gilbert cell topology biased with a 10 nA current source. Figure 5.4 shows the multiplier schematic together with the following Operational Transconductance Amplifier (OTA). The inputs to the multiplier were AC coupled using 10 pF capacitors (C_1 and C_2) and (0.5 μm/0.5 μm) PMOS transistors (M_{R1} and M_{R2}) acting as Quasi Infinite Resistors (QIR). This stage removes any DC offsets created by the low pass filters prior to the multiplication. The PMOS input stage within the Gilbert cell multiplier helps to reduce the low frequency noise on top of the already attenuated output signal of this circuit. Due to the low current operation of the multiplier, a cascoded load ($M_8 - M_{11}$) was used in order to maintain the DC operating point. The summing circuit is the final processing stage of the TEO calculator and it consisted of three single stage OTAs ($G_{m1} - G_{m3}$).

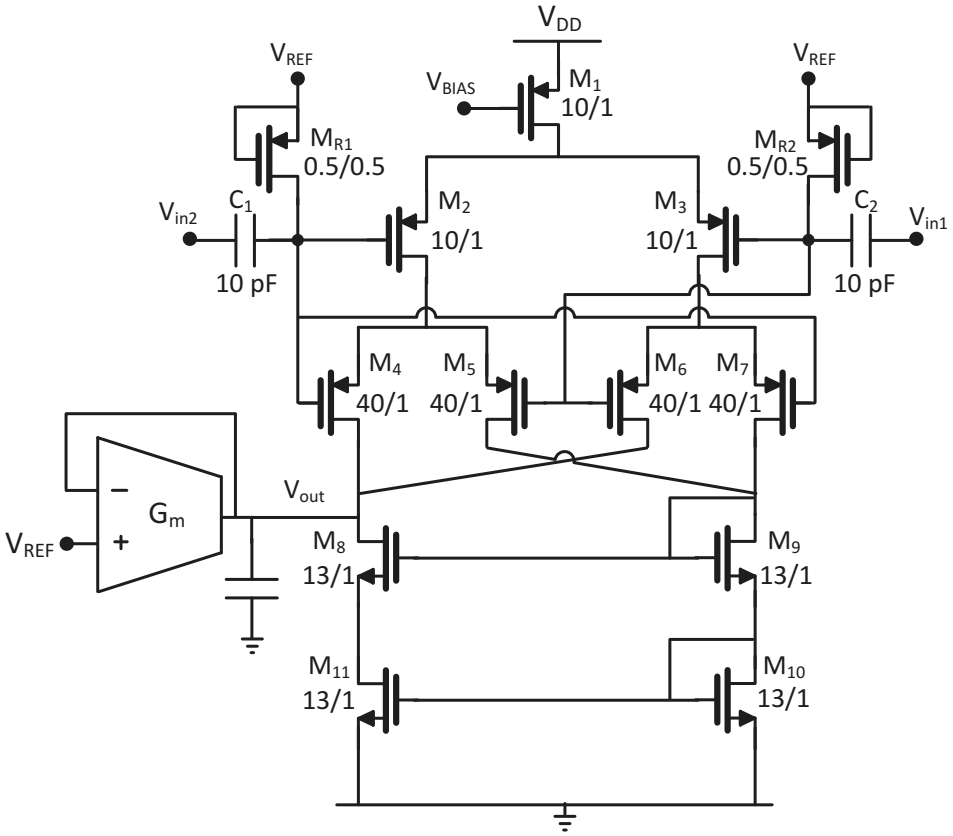


Figure 5.4: *Design of the Gilbert cell multiplier together with following OTA in this work. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

The running average in the original algorithm shown in Figure 5.1 was approximated with an analog low pass filter with a cutoff frequency of 5 mHz for the purpose of this work. The cutoff frequency of the low pass filter was set based on the clocking of a transconductor output and was proportional to the clock signal (ϕ) duty cycle. As can be seen in the filter schematic of Figure 5.5, the transconductor output current (I_1) can only flow into the capacitor when the switch is closed. Assuming the clock duty cycle to be δ, the effective current flowing into the capacitor (I_2) is defined using Equation 5.2 [28].

$$I_2 = \delta \times I_1 \tag{5.2}$$

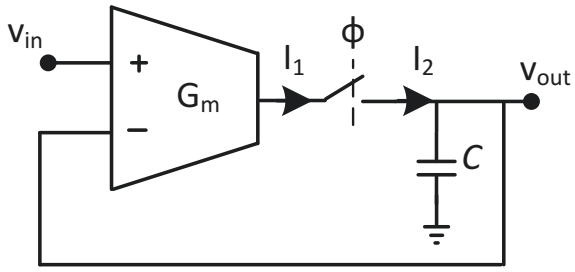


Figure 5.5: *Low pass filter adopted from [28]. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

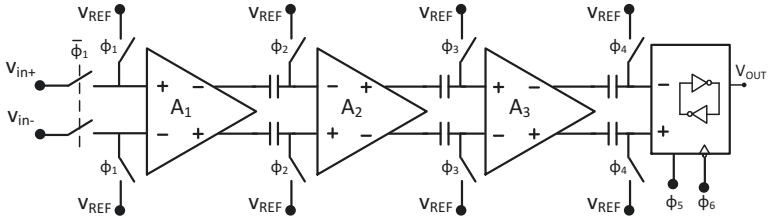


Figure 5.6: *Comparator schematic. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

A 256 Hz clock signal with a duty cycle of 1.8%, generated by the control circuitry, was used to set the filter cutoff frequency. The clock frequency proved to be high enough to avoid aliasing at the output of the TEO calculator.

Two non-inverting amplifiers placed after the lowpass filter and the TEO calculator output help to scale the outputs while isolating the two mentioned routes from the switching inputs of the comparator (Figure 5.2). The comparator effectively detects the time periods for which the TEO output is greater than the amplified version of the low pass filtered signal. As can be seen in Figure 5.6, the comparator utilizes an Output Offset Cancellation scheme (OOS), implemented with three pre-amplifiers ($A_1 - A_3$) [29].

Two six bit digital counters clocked at a rate of 256 Hz follow the comparator

as shown in Figure 5.2. By connecting the comparator output to the counter '*ENABLE*' pins, together with a reset pulse occurring at 250 ms intervals, the counter output detects epochs in which the TEO calculator output is larger than the amplified low pass filter output for the entire duration of the epoch. A delay of 125 ms was added between the two reset pulse signals to effectively create 250 ms long epochs with 50 % overlap between consecutive epochs, inline with the operation of the original algorithm.

5.4.2 Median frequency comparison block

The Median Frequency (f_{med}) is defined as the frequency component at which the signal power spectrum is split into two equal halves [30]. In the case of a bandlimited signal with lower and upper frequency limits of f_l and f_h respectively, f_{med} should satisfy the following equation:

$$\int_{f_l}^{f_{med}} P(f)df = \int_{f_{med}}^{f_h} P(f)df = \frac{1}{2}\int_{f_l}^{f_h} P(f)df \tag{5.3}$$

Traditionally, on-chip implementations of the Median Frequency calculator have used digital computations on the signal spectrum by utilizing a Fast Fourier Transform (FFT) [31]. Using the FFT to calculate the median frequency is the most accurate method and the calculated values using it are considered as a benchmark for other implementations to be compared against. However, the main drawback of this method in terms of the implemented circuit is the power hungry nature of the FFT. For example, the 512-point FFT engine utilized in the recently reported sleep staging SoC of [32] consumes 299 μW and would clearly dominate the power consumed by all blocks described previously and used in the system presented in this chapter. Low power consuming analog FFTs have been proposed recently [33], however, as currents are scaled down in order to reduce the power consumption, component matching will become an issue in such implementations.

Another proposed analog approach is based on changing the cutoff frequency of a voltage controlled filter and having a feedback loop through which the input signal power content below and above the filter cutoff frequency are compared. The filter cutoff frequency is then re-adjusted to mirror the changes in the Median Frequency. Due to the direct relationship between the filter cutoff frequency and the median frequency, this method has been very popular in analysing myoelectric (ME) signals to detect ME spectral shifts resulting from muscle fatigue [34], [35].

The large power requirements of the mentioned methods made them unsuitable

for use in this implementation. Furthermore, the error associated with calculation of the median frequency in all previous works was generally larger than the entire bandwidth available for operation here, resulting in new design requirements with stringent specifications.

As previously mentioned, the median frequency of the signal over the duration of an epoch was compared to a pre-set threshold (f_{th}) in the proposed system, to reject falsely detected spindles. Since the value of f_{th} was known to be 10.7 Hz, it would be sufficient to determine whether f_{med} was larger than the threshold value f_{th} at any point, rather than calculating the instantaneous value of f_{med}. Theoretically, the equation below can be derived from Equation 5.3 for the case of $f_{med} \geqslant f_{th}$:

$$\int_{f_l}^{f_{th}} P(f)df + \int_{f_{th}}^{f_{med}} P(f)df = \frac{1}{2}\int_{f_l}^{f_h} P(f)df \tag{5.4}$$

Therefore, the following will hold true if $f_{med} \geqslant f_{th}$:

$$\int_{f_l}^{f_{th}} P(f)df \leqslant \frac{1}{2}\int_{f_l}^{f_h} P(f)df \tag{5.5}$$

Since the two integrals on both sides of Equation 5.5 represent the signal power of the $f_l - f_{th}$ and $f_l - f_h$ bands respectively, it is possible to estimate the signal power within each of the mentioned bands using a combination of a bandpass filter, squarer and an integrator as shown in Figure 5.7. The input signal is initially passed through the bandpass filters in the top and bottom routes which limit the input signal frequency content to the $f_l - f_{th}$ and $f_l - f_h$ bands respectively. The power of the signals in both routes is then calculated using the squarer circuits. The output of the squarer signal in the bottom route is then multiplied by a factor of 0.5, inline with the right hand side of Equation 5.5. The following integrators provide an average of the signal powers. A following comparator will subsequently compare the outputs of the two routes and determine if a spindle has been correctly detected ($f_{med} \geqslant f_{th}$) or if the detected spindle should be rejected ($f_{med} < f_{th}$).

A second order structure was chosen for the filters in this work due to the reduced complexity of the circuit-level implementation. Furthermore, the larger group delay associated with higher order filters would have resulted in delayed outputs which is not attractive considering the short epoch duration (250 ms) in this work. The value of f_{th} was also modified to 11.3 Hz to compensate for the signal power loss at the filter cutoff points.

The median frequency comparison circuit was initially modelled in Matlab and tested using data made available by the DREAMS sleep spindle database of Uni-

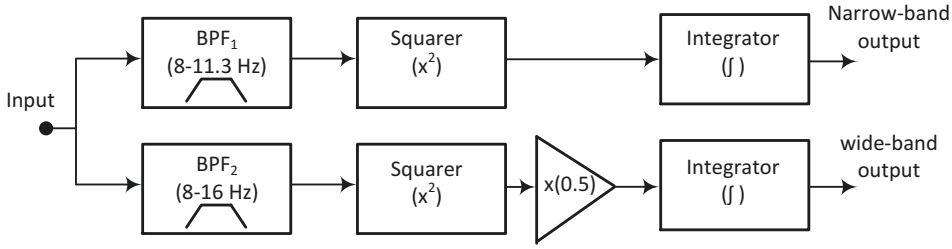


Figure 5.7: *Median frequency detector block diagram. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

versity of MONS - TCTS laboratory and Universite Libre de Bruxelles - CHU de Charleroi Sleep laboratory [36]. Six 30-minute EEG excerpts belonging to six subjects were used. The EEG data was segmented into 250 ms long epochs. The median frequency of each epoch was computed by an FFT and further compared to f_{th}. The results, for each epoch, were compared against the results of the proposed model. The proposed model achieves an overall accuracy of 82.5%. This value was obtained by dividing the number of epochs that match, in terms of the detection result, by the total number of epochs available in the data.

The bandpass filters used here were designed based on the work reported in [37]. The top-level schematic of the second order bandpass filters (BPF_1 and BPF_2) is shown in Figure 5.8. Both OTAs G_{m1} and G_{m2} were identical in terms of their circuit level implementation, which is shown in Figure 5.9(a).

If values of C_1 and C_3 are chosen to be much larger than C_2, the bandpass filter transfer function can be defined as:

$$H(s) = -\frac{\frac{C_1}{C_2}\frac{G_{m1}}{G_{m2}}}{\beta} \cdot \frac{1 - \frac{s}{w_0\beta}}{\frac{s}{w_0} + \frac{\frac{C_3}{C_2}+\frac{G_{m1}}{G_{m2}}}{\beta} + \frac{w_0}{s}} \tag{5.6}$$

where the filter center frequency (w_0) and β are defined using Equation 5.7 and Equation 5.8 respectively:

$$w_0 = \frac{G_{m1}}{\beta C_2} \tag{5.7}$$

$$\beta = \sqrt{\frac{G_{m1}}{G_{m2}}\frac{C_1}{C_2}\frac{C_3}{C_2}} \tag{5.8}$$

Since both OTAs operate in the weak-inversion region, their respective transconductance is proportional to their biasing currents. Therefore, a current scaling

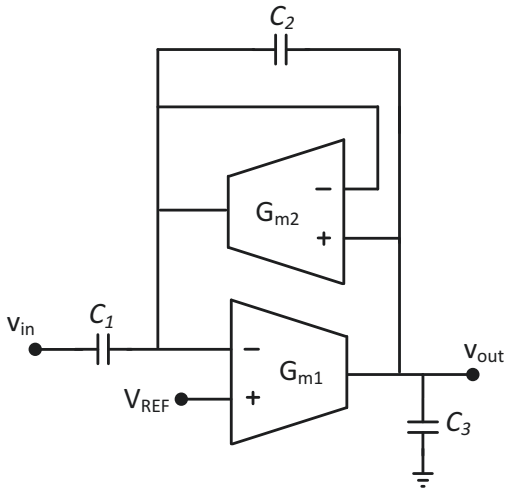


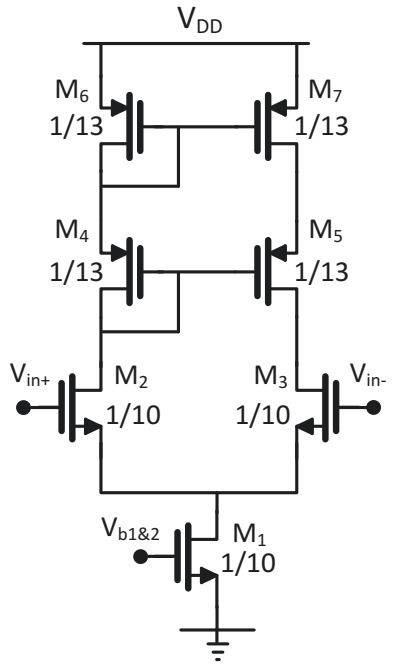
Figure 5.8: *Circuit-level implementation of median frequency detector bandpass filters. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

circuit, shown in Figure 5.9(b) was utilized to create the biasing currents for G_{m1} and G_{m2} (G_{m1} having a biasing current 2.5 larger than that of G_{m2}).

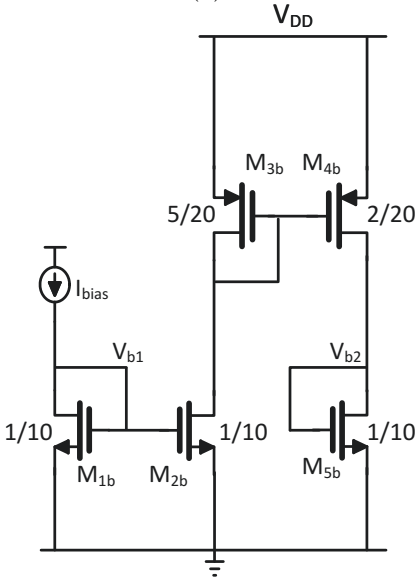
Biasing currents (I_{bias}) of 40 pA and 70 pA were chosen for BPF_1 and BPF_2 respectively. The capacitor values were predistorted during the layout process to compensate for the parasitic capacitors associated to the transistors within the two OTAs as well as the tie down diodes required by the design rules of the process used. Hence, the final values of C_1, C_2 and C_3 were chosen as 11 pF/6.5 pF, 800 fF/800 fF and 2.5 pF/10 pF for BPF_1/BPF_2.

As can be seen in Equation 5.6, the filter mid-band gain is dependent on the ratio of the circuit capacitors and transconductances, i.e $\frac{C_1}{C_2}$, $\frac{C_3}{C_2}$ and $\frac{g_{m1}}{g_{m2}}$. As mentioned above, different capacitor ratios were used to implement the two bandpass filters and this results in different mid-band gains for the two filters, as shown in the measurement results of Section 5.5.2. Therefore, two non-inverting amplifiers were placed after the two filters in order to scale the outputs to reach the same mid-band gain. A factor of (-1) is also present in the filter mid-band gain as seen in Equation 5.6, however, this will not affect the system performance due to the squaring operation of the Gilbert cells following the filters.

A Gilbert cell multiplier equivalent to the one shown in Figure 5.4 was used here again as a squarer circuit, with both inputs shorted together. As shown in



(a)



(b)

Figure 5.9: *Structure of OTA and biasing circuitry: (a) OTA circuit design; (b) current scaling circuitry. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

Figure 5.7, the output of the squarer in the bottom route should be attenuated by a factor of 2 to satisfy the right hand side of Equation 5.3. The approach chosen here is to instead amplify the squarer output in the top route by a factor of two using the non-inverting amplifier placed after the multiplier, since at this point the signal amplitude has already been weakened by the squaring operation.

A lossy integrator implemented as a single stage GmC filter with a time constant of 160 ms was used to provide a running average of the squared signals in both routes.

Finally, a comparator identical to one shown in Figure 5.6 was used to compare the outputs of the upper and bottom routes of the median frequency comparison circuit.

5.4.3 Decision making block

As the final stage of the system, the decision making block combines the results of the TEO processing stage and the median frequency comparison stage, to detect sleep spindles available in the subject EEG traces. The outputs of the two counters in the TEO processing stage are initially fed to an OR gate. The output of the mentioned OR gate is then combined with the outputs of the median frequency comparison circuit by using an AND gate. Finally, outputs of the AND gate which are 'high' represent epochs which contain part of a sleep spindle.

Timing constraints required by the system were maintained in the system back-end. During this stage, which is implemented in Matlab, events detected by the system with durations shorter than 0.5s (3 consecutive epochs) or longer than 3s (23 consecutive epochs), were discarded.

5.4.4 Biasing and clock generation circuitry

The on-chip IA achieved a mid-band gain of 37 dB and input referred noise of 4 μV_{rms} integrated from 0.5-100 Hz. Current branching circuitry was used to draw a 10 nA current from a main current reference, operating from the 1.25 V main power supply. The IA and main current reference circuits were designed by colleagues at Imperial College London.

An 8b counter circuit using JK flip-flops followed by D flip-flops and combinational digital logic was used to scale-down a 32.6 KHz clock provided by an off-chip oscillator and to generate the low duty cycle pulses required for the circuits in the system.

5.5 Fabrication and testing

5.5.1 Layout and fabrication

The chip was fabricated in a 0.18 μm, triple well, 6 metal AMS CMOS process. All on-chip capacitors larger than 1 pF were implemented using dense dual-MIM capacitors available in the process in order to reduce the overall chip area. By splitting the chip padring into two seperate padrings, the analog and digital portions of the chip were set apart to isolate the sensitive analog circuitry from the noisy digital signals. The analog and digital connections to the pads were restricted to the left/bottom side and the bottom/right sides. The chip micrograph is shown in Figure 5.10. The overall system occupied 1.63 mm^2.

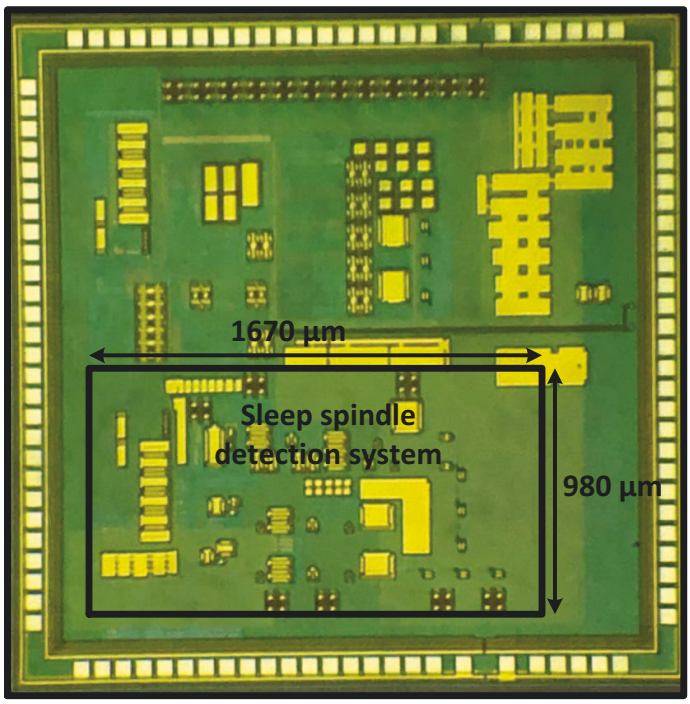


Figure 5.10: *Micrograph of the fabricated chip.*

5.5.2 Test setup and measurements

A National Instruments USB-6259 data acquisition (DAQ) board was used to generate the input signals to the system and to collect the output results from the decision making block together with the analog intermediate testpoint signals within the system. Due to the low current consuming nature and weak driving capability of the circuits within the system, buffering stages were required to drive the 15

pF load present at the data acquisition board inputs. Hence, analog single stage buffering stages consuming 1 μA from a seperate 1.8 V supply were implemented on-chip and placed between the testpoints and the output pads. Digital buffers were implemented and placed after the decision making block outputs.

Six 30-minute long EEG traces belonging to six subjects from the DREAMS database [36] were used to validate the system accuracy. Reference markings from two different experts were also provided together with the database. Similar to [23], the union of the two reference markings was used as the reference marking in this work for system performance evaluation purposes. Artefacts were present in the test database and no effort was made to select artefact free sections of the database during the testing process.

Matlab was also used to feed the inputs to the chip through the DAQ board and to store the output signals collected by the board.

The signals in the database were sampled at different sampling frequencies and all signals were resampled to have a uniform sampling rate of 256 Hz.

The integrated noise at the input of the system was 70 μV_{rms}. The contribution of the sleep spindle detection system to the equivalent input noise of the full EEG system (including an EEG amplifier) will be reduced as a function of the gain chosen for the amplifier stage. Hence, by considering a typical amplifier gain of 100 and noise performance of state-of-the-art EEG amplifiers such as [38] and [39], the minimum input signal that the full system would be able to process that would be in the order of 1 μV_{rms}.

A 30 s long section of the EEG input signal fed to the system is shown in Figure 5.11. Measured and Matlab simulation outputs of the TEO circuit corresponding to the EEG input are shown in Figure 5.12.

The measured frequency responses of the 8 Hz to 11.3 Hz and 8 Hz to 16 Hz bandpass filters used in the median frequency comparison circuit are shown in Figure 5.13. As can be seen, a difference of 13 dB is present between the mid-band gains of the two filters and this was corrected for using the non-inverting amplifiers described earlier. The effect of a zero present in the transfer function of both filters on the measured frequency response can also be seen in Figure 5.13, resulting from the filter topology chosen in this work [37]. This was proven not to affect the performance due to the integrator following the filters which significantly attenuates the higher frequency content present in the system at this point.

Subsequently, the outputs of the two filters resulting from the mentioned input EEG signal are shown in Figure 5.14 and Figure 5.15, respectively.

The final system output is shown in Figure 5.16. It can be seen that a false

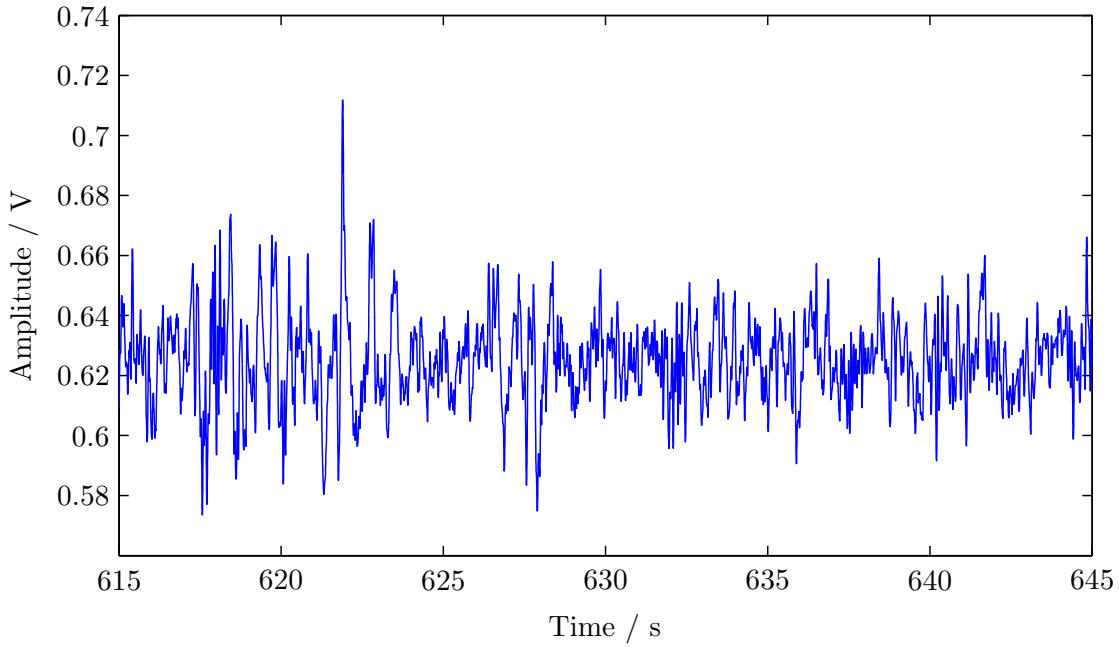


Figure 5.11: *A 30 s section of the system EEG input. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

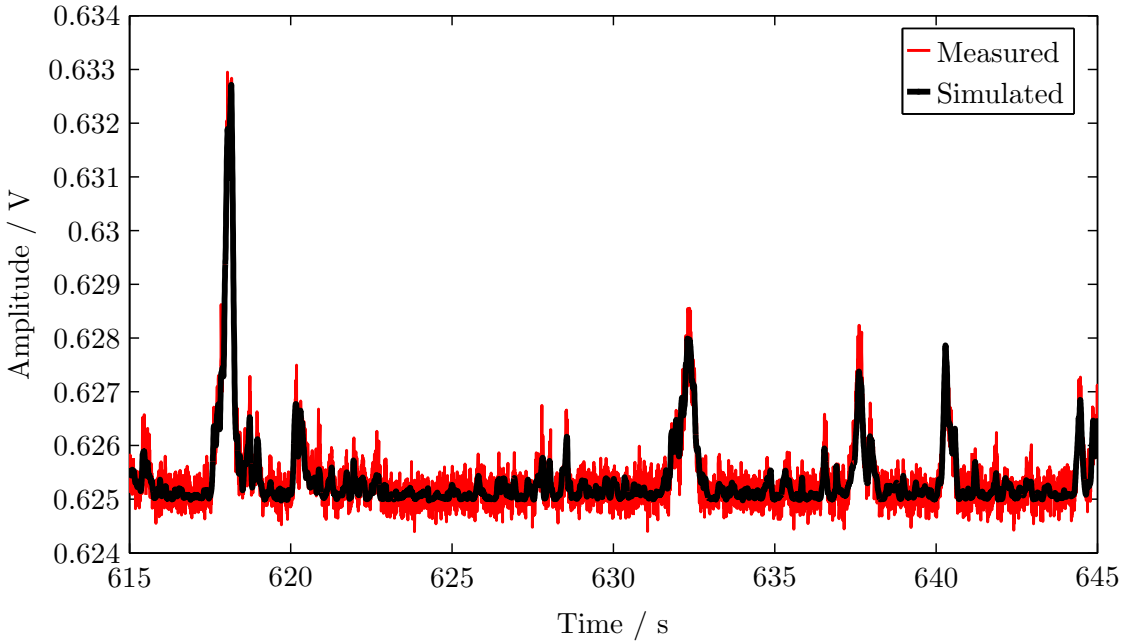


Figure 5.12: *Simulated and measured outputs of the TEO circuit corresponding to the EEG input signal. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

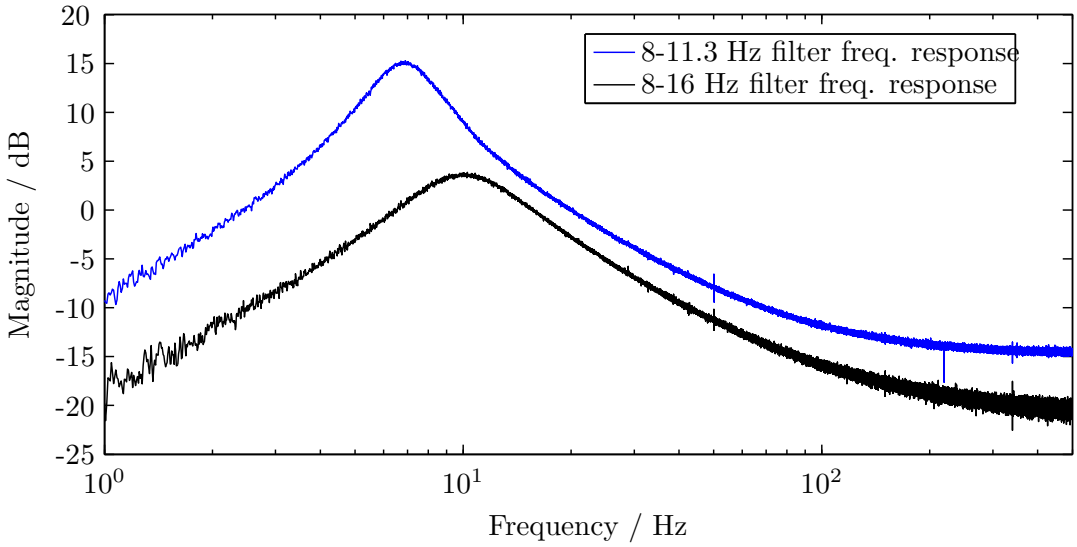


Figure 5.13: *Measured frequency response of the 8 Hz to 11.3 Hz and 8 Hz to 16 Hz bandpass filters used in the median frequency comparison circuit. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

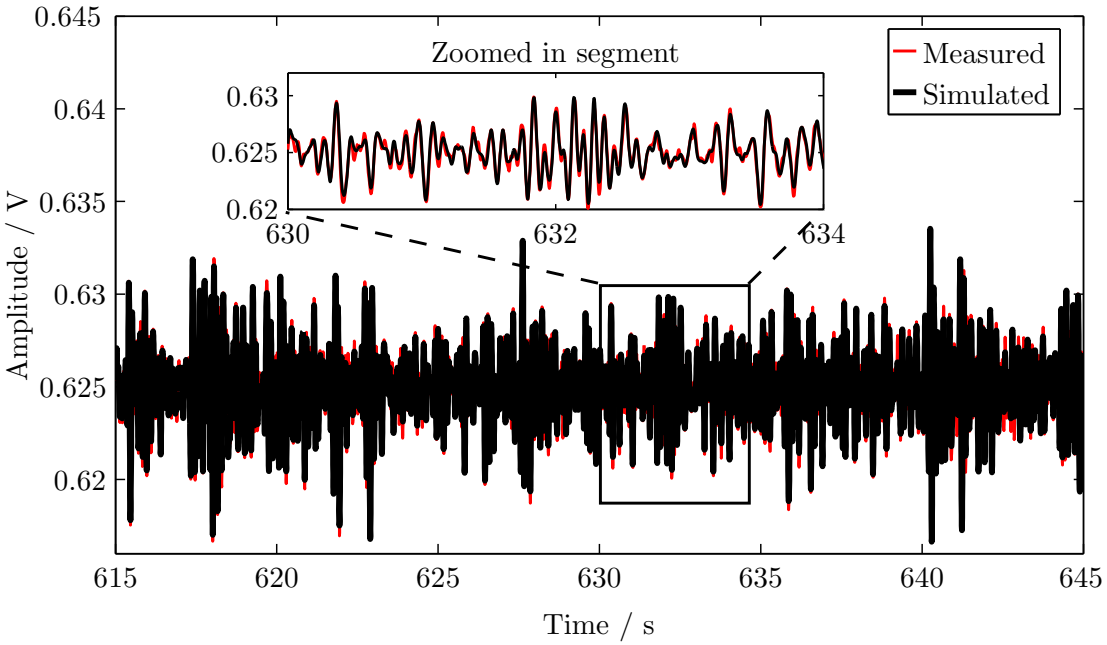


Figure 5.14: *Simulated and measured outputs of the 8 Hz to 11.3 Hz bandpass filter used in the median frequency comparison circuit. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

Table 5.2: *Summary of system detection results.*

		Matlab simulation results of [23]			Measurement results of this work		
Subject	**Total spindles**	**True Positives**	**Sensitivity (%)**	**Specificity (%)**	**True Positives**	**Sensitivity (%)**	**Specificity (%)**
1	134	111	82.8	96.7	105	78.3	98.1
2	77	58	75.3	98.3	51	66	98.6
3	44	39	88.6	97.7	32	72.7	99.1
4	63	38	60.3	97.8	21	33	98.7
5	103	87	84.5	97.1	82	79.6	97.5
6	117	99	84.6	98.1	92	80.7	98.2

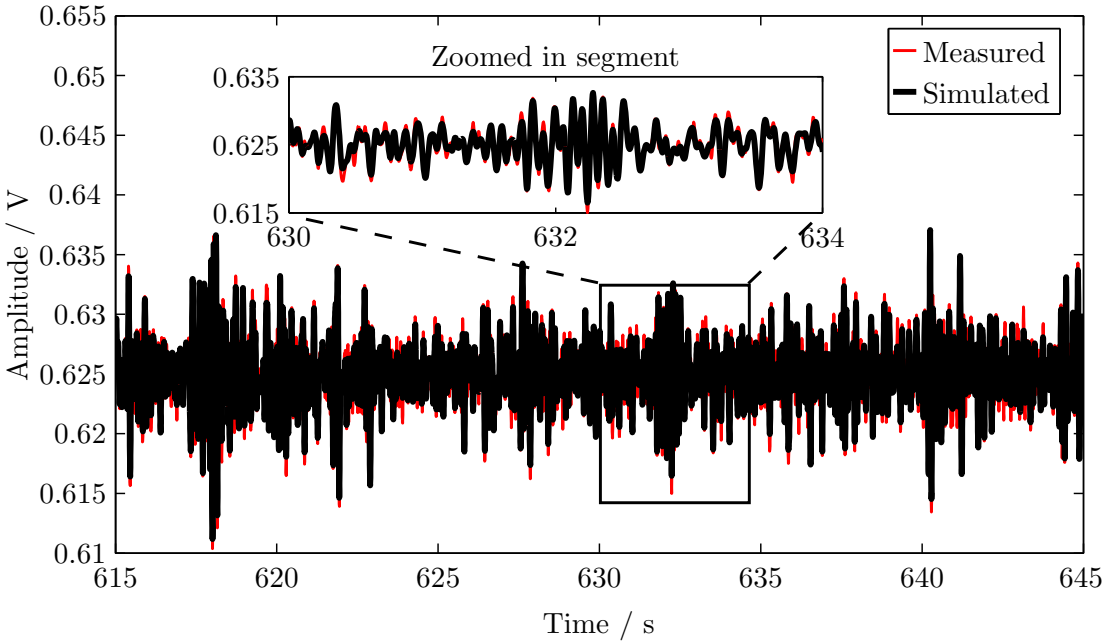


Figure 5.15: *Simulated and measured outputs of the 8 Hz to 16 Hz bandpass filter used in the median frequency comparison circuit. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

detection by the system at the 641 s time mark is effectively eliminated by the median frequency comparison circuit.

The system performance was further evaluated by calculating the sensitivity and specificity values using Equation 5.9 and Equation 5.10, respectively.

$$Sensitivity = \frac{TP}{TP + FN} \tag{5.9}$$

$$Specificity = \frac{TN}{TN + FP} \tag{5.10}$$

A spindle detected by the system is marked as a True Positive (TP) if it overlaps at any point with an expert marked spindle, and marked as a False Positive (FP) if this condition is not satisfied. Spindles not detected by the system are considered False Negatives (FN), while True Negative (TN) values were calculated using Equation 5.11, which is based on the general assessment method reported in [19].

$$TN = \frac{\text{Total duration of record}}{\text{Average detected spindle duration}} - TP - FP - FN \tag{5.11}$$

During the pre-fabrication testing of the system performance with respect to

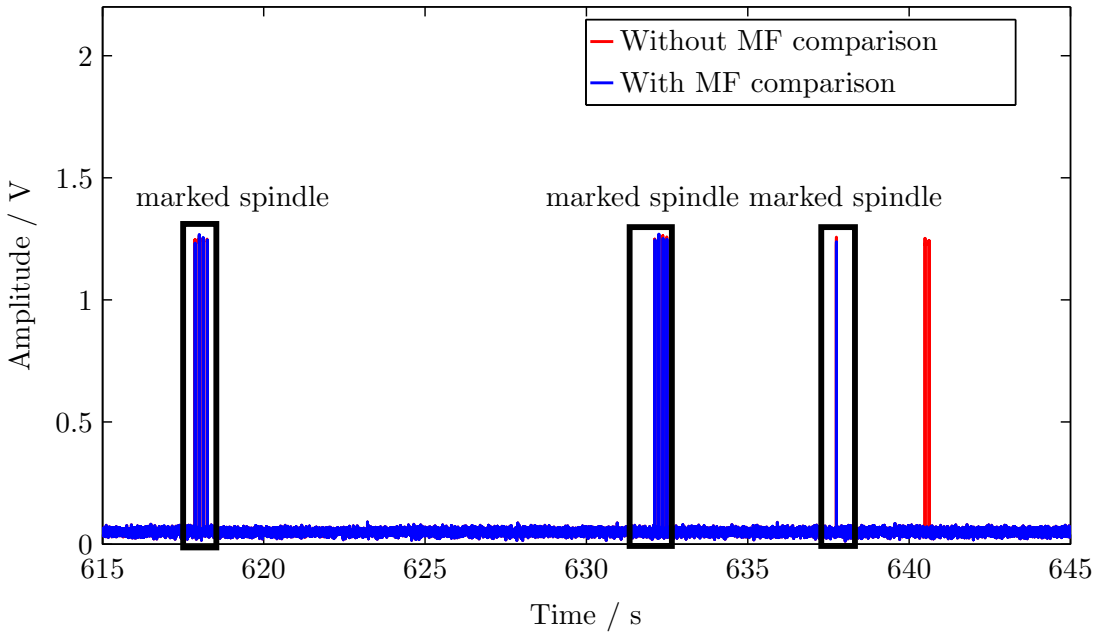


Figure 5.16: *System outputs with and without using the median frequency comparison circuit. Figure reprinted from: S. Iranmanesh and E. Rodriguez-Villegas, "An Ultralow-Power Sleep Spindle Detection System on Chip," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 4, pp. 858-866, 2017, © IEEE.*

process and mismatch variations using the test database, the worse cases of system sensitivity and specificity were found to be 67% and 91.5% respectively. A careful layout design process was carried out to ensure robust performance. However, even though it is not necessary, it is worth noting that should it be needed the transconductors could be tuned through their tail current.

The fabricated system detection results corresponding to the test database EEG inputs are summarized in Table 5.2, including the total positive values together with sensitivity and specificity values individually for each of the six subjects. As mentioned previously, the same test database was fed to the ideal system which was modelled in Matlab and simulated. The simulation results are also included in the table for comparison. Out of the total number of 535 spindles present in the database, 383 spindles were correctly detected by the system. As can be seen in Table 5.2, the sensitivity of the system was degraded in the case of subject number four. Comparison of the marked events with the hypnogram, provided with the database, verifies that 31 of the 63 marked spindles in this record belong to the Wake stage as opposed to the NREM stages. The fabricated system incorectly detected 3 out of the 31 spindles in the Wake stage while the Matlab model detected

Table 5.3: *Summary of system performance.*

CMOS Process		0.18 μm	
Area		1.63 mm^2	
Supply Voltage		1.25 V	
Sensitivity		71.5%	
Specificity		98%	
Current consumption (nA)	TEO and post processing block	BPF	0.22
		$LPF_{1\text{-}2}$ ($\times$2)	1
		Multiplier ($\times$2)	88
		Summer	86
		Amplifier	3.5
		LPF_3	3
		Comparator (static)	4.5
	Median frequency comparison block	BPF_1	0.11
		BPF_2	0.2
		Scaling amplifier	35.6
		Squarer ($\times$2)	88
		Amplifier ($\times$2)	93
		Integrator ($\times$2)	0.04
		Comparator (static)	4.5
	Digital circuitry (averaged)		4
	Total		412

14 of such events. The other TP detections made by both the fabricated system and the matlab model are part of the NREM stages.

The system achieved an overall sensitivity and specificity of 71.5% and 98% as opposed to 80.3% and 97.6%, which is achieved by the ideal Matlab model reported in [23]. A summary of system performance including a breakdown of the total power consumed by the hardware blocks is shown in Table 5.3. The system consumed an averaged current of 412 nA from a 1.25 V power supply which translates to a power consumption of 515 nW.

5.6 Discussion

This chapter presented the design and results for a prototype low power consuming SoC to automatically detect sleep spindles using EEG input signals. The system is partitioned into three separate blocks, i.e., the TEO and post-processing block, median frequency comparison block and the decision making block. A novel TEO calculating circuit operating based on lowpass filters to replace delay elements and a median frequency comparison circuit using bandpass filters, multipliers and integrators were introduced. The design process of the TEO and median frequency comparison circuits, required in order to make them suitable for a low power system solution, were explained in detail. Measurement results verified that the overall system achieved a sensitivity and specificity of 71.5% and 98% respectively, which is very close to the original performance of the ideal algorithm. The chip was fabricated using a 0.18 μm AMS CMOS process. Due to the analog customized implementation in this work, extremely low levels of power consumption could be achieved. The entire system consumed 515 nW from a 1.25 V power supply.

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6 Conclusions

6.1 Contributions

This thesis discussed the design and experimental results of three separate SoCs fabricated in CMOS technology to locally identify clinically significant events that are characteristic of epilepsy and sleep. The operational lifetime of a wearable EEG monitoring device operating from a miniature battery and incorporating these SoCs would be increased since the transmitter, which is the dominating component in terms of power consumption, would only become active based on the output of these SoCs and would therefore operate at a reduced data rate. This reduction in the WEEG system data rate, and ultimately power consumption, is a direct result of the efficient signal processing that is carried out within the presented SoCs, with a negligible power overhead to the WEEG system.

Chapter 2 presented a review on the current clinical EEG monitoring with regards to the diagnosis of epilepsy and sleep disorders, while highlighting the benefits of long-term monitoring for the diagnostic process. A wireless, light weight and low-power WEEG device compliant with regulatory standards of medical devices was envisioned as an optimum solution for long-term EEG monitoring of patients. A detailed literature review on the state-of-the-art of the individual components to develop such a device revealed that developing a truly WEEG monitoring devices with a long operating lifetime remains an open challenge. This is due to the power hungry nature of wireless transmitters, which dominate the device power consumption. Power savings, and therefore a longer operational time, can be achieved on a system-level by incorporation of a Local Signal Processing (LSP) module as part of the WEEG device. The power savings are due to the reduction in the device data rate as a result of the processing carried out by the LSP. Emphasis was put on the stringent power budget available to the LSP module, as the power consumed by this block must be much lower than the WEEG device in order to be truly beneficial in terms of power savings. Different types of LSP modules were also explained and their potential benefits and shortcomings for clinical applications were discussed.

The importance of monitoring interictal activity and the software based ap-

proaches to identify this form of activity were reviewed in Chapter 3. The detailed design and experimental results of an SoC that identifies interictal spikes were discussed. A previously published interictal spike selection algorithm implemented as a mathematical model in software, was used as a foundation for the developed SoC. All approximations required on the system-level to allow for an efficient analog implementation of the algorithm in the form of an SoC were explained. Further, the design of individual circuits required to achieve a sub-μW level of power consumption while maintaining the system accuracy in identifying interictal activity, was explained. A novel low-power absolute value comparator consuming 142 nW was also proposed and developed, in a 0.35 μm CMOS process, in order to satisfy the computational requirements of the SoC. However, the use case of this circuit, which is self-sufficient and does not require additional rectification circuitry, is not limited to processing EEG signals and can be extended to other low-bandwidth system with low power budgets, in which the use of additional full-wave rectifiers is not desired.

The performance of the interictal spike detection SoC, fabricated in a 0.35 μm CMOS technology, was tested on a database containing 982 interictal events marked by a medical expert. The SoC achieved a sensitivity of 87% for a percentage of data transmitted of 45%. The power consumed by the SoC was 950 nW.

Chapter 4 focussed on the design and experimental results of an analog-based seizure selection SoC. The SoC can aid the diagnosis of epilepsy since by only transmitting sections of data containing likely seizure activity, significant data reductions can be achieved. Moreover, the amount of time required for neurologists to review the transmitted data could be reduced. The SoC used a previously published seizure detection algorithm as a foundation. Modifications carried out at the system-level included the replacement of median calculation, which would be power hungry in hardware, with a moving average operation which was then approximated using a low-power analog filter. The design of individual circuits required for the low-power operation of the system was explained in detail. The performance of the SoC, fabricated in a 0.18 μm CMOS process, was characterized using a database containing 34 seizure events. The SoC consumed 1.14 μW and was able to achieve a sensitivity of 83% for a percentage of data transmitted of 52%.

The design and experimental results of a sleep spindle detection SoC were described in Chapter 5. The SoC used a previously published algorithm, implemented as a mathematical model in Matlab, as a foundation. A number of approximations carried out to allow for the low-power operation of the SoC were explained. As

part of the SoC design process, a novel TEO calculating circuit operating based on low-pass filters to replace delay elements and a median frequency comparison circuit using bandpass filters, multipliers and integrators, as opposed to the power hungry FFT operation, were introduced. The SoC was fabricated in a 0.18 μm CMOS process and experimental results using a publicly available EEG database containing sleep spindles, revealed overall sensitivity and specificity figures of 71.5% and 98% for the SoC. The power consumed by the SoC was 515 nW.

The SoC could be used on its own to report the frequency of sleep spindles. Furthermore, due to the very low level of power consumption achieved, the SoC could be used as part of a sleep staging SoC to increase the accuracy of the staging operation, with practically no added power overhead. In addition to its use case in sleep monitoring applications, the SoC could be used to aid researchers looking at gathering more data on sleep spindles, considering the active research carried out on the clinical significance of sleep spindles in other diseases.

6.2 Further work

Future work can look at adding other discriminatory features which can be implemented in hardware with low complexity, to the developed SoCs in order to improve their performance with regards to detection accuracy. In the case of the interictal spike and seizure SoCs specifically, less than 1% of the databases used for testing consisted of epileptic EEG activity, while the systems achieved a sensitivity above 80% when selecting almost 50% of the available EEG data for transmission. It is worth noting that this does not jeopardize the diagnosis as it is the neurologist who eventually decides on the clinical significance of the transmitted data. However, it is conceivable that improving on the data reduction provided by the SoCs by addition of other features with low complexity, while maintaining the same level of sensitivity, will be beneficial in terms of power savings for the WEEG system. A similar approach could be used to improve the sensitivity of the sleep spindle detection SoC presented in Chapter 5. More than 50% of power in both mentioned systems is consumed by the SC delay circuit and the possibility of optimizing the power of this block could be investigated in the future.

Future work could also look at combining the presented SoCs. The interictal spike and seizure selection SoCs could be combined in order to provide a complete solution to the monitoring of epilepsy. The sleep spindle SoC could be used together with other algorithms that identify other stages of sleep, to form a complete sleep staging system. Ultimately, all three SoCs can be combined to be used throughout

the 24 hours of a day for extended periods of time. Future research can be carried out on the possibility of implementing a WEEG system with a high channel count utilizing the interictal spike and seizure selection SoCs, to aid the diagnosis of epilepsy, while incorporating the sleep spindle detection SoC in a single channel of the system to mark the presence of sleep spindles. This will be especially useful when considering the comorbidity between epilepsy and sleep disorders.

7 Optimizing simulation times in systems containing Quasi-Infinite Resistors

The research presented within this chapter is an edited version of research previously published in:

S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.

7.1 Introduction

Recently, much effort has been placed in developing systems for recording [1] and/or on-chip processing of bio-signals [2], in real time. As shown in Figure 7.1, these systems generally consist of an amplifier at the front-end, followed by an ADC and if required for transmission, a transmitter. Signal processing chains may also be incorporated into the system to reduce the amount of data that needs to be transmitted, resulting in an overall reduction in the system power consumption. In the design phase of such systems, time-domain system-level simulations are required by the designer to verify the correct operation of the system. Bio-signals are typically low frequency signals and hence long time-domain simulations are needed for the designer to monitor a tangible amount of simulated results in order to verify accurate system operation. Simulations quickly become extremely time consuming when signals with higher frequencies, such as high speed clock signals, are also present in the system. Examples of this are biomedical systems which incorporate Switch Capacitor (SC) circuits operating with higher frequency clocks to create filters, delay lines, etc. The SC circuits would normally operate with clocks at frequencies at least an order of magnitude higher than the input signal

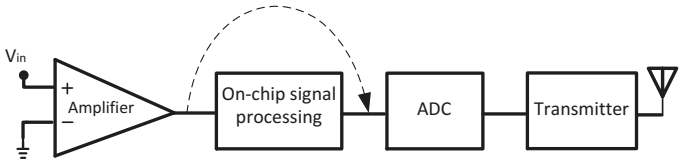


Figure 7.1: *Conceptual implementation of system for bio-signal recording/processing. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

bandwidth in order to reduce the amount of mean square error produced by sampling the continuous time signal. The simulator would therefore choose smaller time steps to accommodate the faster clock signal, resulting in much longer simulation times. Furthermore, Quasi-Infinite Resistor (QIR) elements have recently been widely used in creating circuits to reject DC offsets in biomedical systems [3]. When properly biased, QIRs would create extremely large incremental resistances (typically in the GΩ-TΩ range). This would allow for QIRs to be used together with smaller capacitors, implementable on-chip, to filter DC offsets either at the system frontend or at any point within the signal processing chain [4]. For example, SC circuits would generally, if not compensated for, be associated with an offset voltage at their respective output as a result of charge injection associated with non-ideal CMOS switches, and therefore, a DC blocking stage may be placed right after such circuits in order to shift the common mode voltage into the Input Common Mode Range (ICMR) of the subsequent circuitry. A simple DC blocking circuit created using a capacitor and a gate-source shorted PMOS transistor, acting as the QIR has been shown in Figure 7.2.

Time domain simulations of the overall system will become challenging and time consuming once the DC blocking circuits consisting of the QIR are placed in a system that also contains switching circuitry. One of the main issues in terms of simulation time would be the long initial settling time required for the output of the DC blocking circuit to settle at the required voltage (V_{DC} in Figure 7.2).

Numerical methods that help reduce the overall simulation time in systems incorporating both clocks operating at high frequencies and low frequency input signals have previously been reported [5], and extended versions of these methods have been incorporated in todays simulation tools. However, these methods are most beneficial for systems in which the high frequency components are orders of mag-

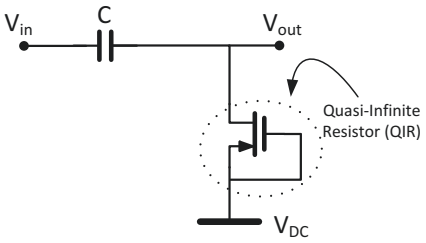


Figure 7.2: *QIR and Capacitor forming single stage DC-blocking circuit. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

nitude larger than the signal being processed in terms of frequency, as a result of the computational overhead required.

A simple simulation method is introduced here to eliminate the startup and settling time required for the output voltage of DC blocking circuits that use QIRs to settle to the required voltage levels. This method would be mostly beneficial in systems that also contain switched circuits (high frequency components) and would significantly reduce the time required for simulations. The proposed simulation method has been explained in detail in Section 7.2. This is followed by an example scenario and simulation setup in Section 7.3. The simulation results have been described in Section 7.4.

7.2 Proposed implementation strategy

The time domain simulation of an SC circuit would simulate the normal circuit behaviour with the clocks operating and therefore, an amount of time would be required for the output of the SC circuit to stabilize around a periodically varying operating point [6]. If placed after the SC circuit, the output of the DC blocking circuit consisting of the QIR and the capacitor will also follow this change in voltage level and therefore an added amount of time would be required to allow the circuit output voltage to retune and settle at a predefined value (V_{DC} in Figure 7.2). Due to the nonlinear nature of QIRs, the conventional settling time analysis could not be performed on such circuits. Assuming the output of the SC circuit to stabilize around a DC voltage (V_{stab}), for $V_{DC} - V_{stab}$ larger than about twice the thermal voltage, the effect of leakage currents is negligible and the output voltage (V_{out}) would move towards V_{DC} more rapidly. As the difference of the two voltage levels

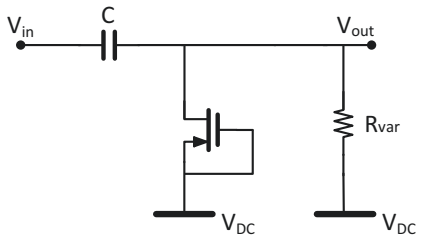


Figure 7.3: *Ideal resistor placed in parallel with the QIR for time domain simulations. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

(V_{DC} and V_{stab}) is reduced, leakage currents would dominate and even more time is required for the output of the DC blocking circuit to settle to a voltage close to V_{DC} [7]. When considering the effect of the switching clock signals present, the mentioned settling time would translate to very long simulation times.

The proposed solution is to place an 'ideal' variable resistor (R_{var}) in parallel to the QIR, as shown in Figure 7.3. The resistor would be switched between 'high resistance' and 'low resistance' modes. The value of R_{var} would initially be set to the 'high resistance' mode having an extremely large value at the start of the time-domain simulation, resulting in the circuit behavior to be dominated by the QIR element. Once the input voltage (V_{in}) reaches the steady state voltage (V_{stab}), the value of R_{var} would be switched to an extremely small value ('low resistance' mode). This would ensure that the overall circuit settling time is dominated by the low resistance path and would allow for V_{out} to rapidly reach a voltage very close to the pre-defined value of V_{DC}. This would be followed by switching the value of R_{var} back to the 'high resistance' mode, resulting in the circuit returning to its normal operation.

It should be noted that R_{var} could also be modeled as an ideal switch together with a pulsed voltage source. In this case, the switch *ON* and *OFF* states would model the 'low resistance' and 'high resistance' modes respectively.

7.3 Simulation setup

An appropriate test setup has to be selected in order to validate the efficiency of the simulation method proposed in Section 7.2. The setup should incorporate

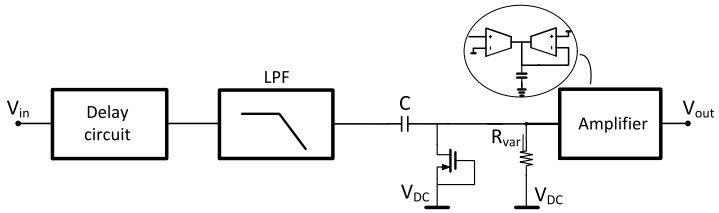


Figure 7.4: *Example scenario of an analog bio-signal processing chain. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

both higher frequency components and circuits with large time constants, as is the case in many biomedical systems. A small section of a biomedical system will be used as an example scenario. This sub-system, shown in Figure 7.4, could be potentially used to delay and amplify a bio-signal using analog circuitry. The mentioned sub-system has been implemented in Cadence enviroment using a 0.18 μm CMOS technology. The aim of this section is to illustrate the amount of time required for the simulator to simulate the settling time required for the output of the amplifier (V_{out}) to settle at a voltage close to V_{DC}, with and without using the proposed simulation method.

The delay circuit, adapted from [8], consists of ten cascaded single SC delay cells (see Figure 7.5). Each delay cell would delay the input signal by a clock period by providing linear phase behavior and therefore, using a 100 Hz clock, the ten cascaded SC delay cells would delay the input signal by 100 ms.

The delay circuit is followed by a low pass filter (LPF), to reduce the distortion introduced by the clock signal and its harmonics, without adding phase non-linearity to the already delayed signal. As seen in Figure 7.4, a DC-blocking circuit was also added prior to the amplifier. This circuit consists of a capacitor (C = 20 pF) and a gate-source connected high threshold voltage PMOS transistor with W/L of 0.5 μm/5 μm as the QIR, resulting in a very low high pass corner frequency (nearly 30 mHz).

The DC-blocking circuit was used to reject offset voltages at the output of the low pass filter that would be created by the delay circuit or the low pass filter itself. As a result, the DC-blocking circuit would ensure that the input to the amplifier is eventually conditioned around V_{DC}.

The amplifier in this test setup was chosen to amplify and integrate the input signal using an OTA based structure. The gain of this circuit was set to nearly

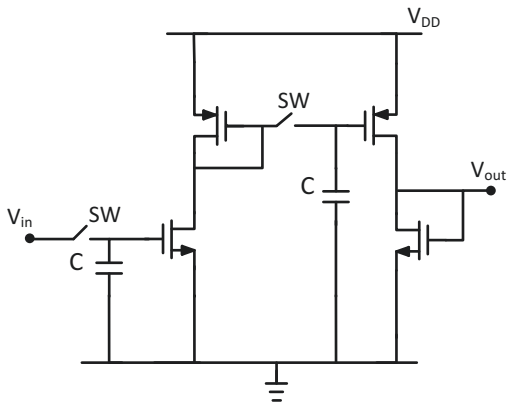


Figure 7.5: *Single delay element. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

compensate for the gain loss resulting from the SC delay circuit.

The author believes this example test setup to be a useful case scenario and the time required for simulating this sub-system without using the proposed simulation method to only be an underestimation of the amount of time required to simulate a complete biomedical system, for the following reasons: First, the mentioned delay circuit operates based on a 100 Hz clock while other clocked circuits that may be present in biomedical systems, such as ADCs, generally operate with higher sampling rates. The simulator would therefore take smaller time steps to accurately calculate the signal levels and more time would be required for the simulation to end. Also, the reader should note that although the bio-signals are generally low bandwidth signals, the SC circuits in biomedical systems would generally not run at rates lower than the mentioned 100 Hz since the sampling rates of such circuits should be at least 2x larger than input signal bandwidth.

Furthermore, as mentioned in [7], the use of an AC signal superimposed on a DC input signal would allow for larger peak currents through the DC-blocking circuit and therefore, the input signal used in this test setup only helped to speed up the settling time of the DC-blocking circuit in the case of not using the proposed simulation method.

7.4 Simulation results

Time domain simulations of the sub-system mentioned in the previous section were executed in the Cadence (IC6.1.5) Spectre environment run on an Intel Xeon 3.30 GHz processor. For illustration purposes V_{DC} was set to 500 mV, and a 10 mVpp 5 Hz AC signal on top of a 500 mV DC signal has been chosen as input to the sub-system. This input signal is in-line with typical low frequency small amplitude (pre-amplified) bio-potentials. In order for the simulator to find the initial operating points of all nodes within the sub-system, an initial short transient simulation should be run while all clock signals are set to the constant value of 'Vdd' and the input signal is slowly ramped from 'Gnd' to the 500 mV DC voltage [9]. The 'rampup' option of the transient analysis in Spectre environment was used to perform this initial simulation. The outputs of this simulation, which are the operating points of all the nodes within the sub-system, are saved and used in the following simulation.

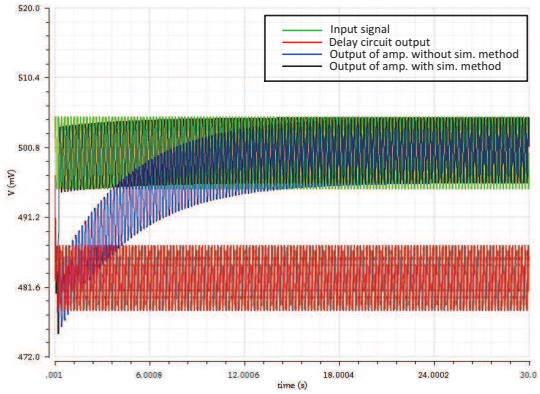
Using the saved operating points, a second transient simulation (30 seconds long) was run with the clocks switching between 'Gnd' and 'Vdd' voltage levels. Rather than using an ideal switch as the ideal resistor as previously mentioned, the 'dynamic parameter' option in Spectre transient analysis was utilized to change the value of the ideal resistor R_{var}. This option would allow for parameter value, time mark pairs to be entered at the beginning of the simulation resulting in dynamic changes in parameter values during the time domain simulation. The value and time mark pairs chosen for R_{var} are shown in Table 7.1.

Table 7.1: *R_{var} value and time mark pairs.*

R_{var} values	Time mark
500 TΩ	0
0.01 Ω	250 ms
500 TΩ	300 ms

The results of the time domain simulations have been shown in Figure 7.6(a). R_{var} is initially set to 500 TΩ ('high resistance' mode), allowing for the QIR transistor to dominate in terms of circuit behaviour. This would result in the output of the DC-blocking circuit to follow the change in the output of the LPF circuit which would finally stabilize at V_{stab}, which is 482 mV (see Figure 7.6(b)), as a result of the switching clocks.

The value of R_{var} is then changed to 0.01 Ω ('low resistance' mode) at the 250



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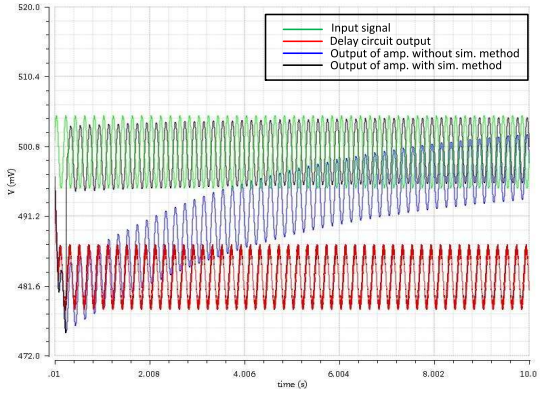

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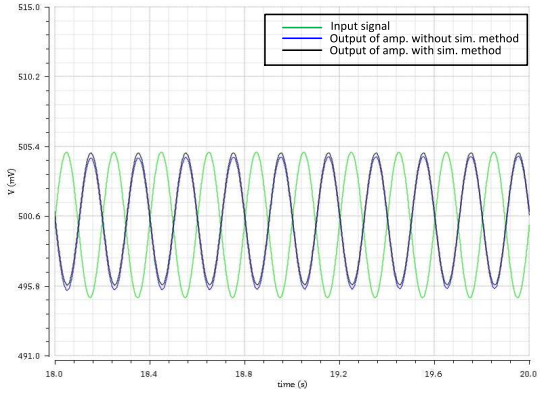

(c)

Figure 7.6: *Time domain simulation of the sub-system with and without using the proposed simulation method: (a) Complete results; (b) Zoomed in results showing time 0 to 10 s; (c) Zoomed in results showing 18 s to 20 s. Figure reprinted from: S. Iranmanesh, M. Eid and E. Rodriguez-Villegas, "Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors," IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, November 2016, © IEEE.*

Table 7.2: *Summarized simulation results.*

Simulation setup	Time required
Using sim. method	25 s
Without using sim. method	2489 s

ms time mark, allowing for the output of the DC-blocking circuit to rapidly reach V_{DC} (500 mV). At the 300 ms time mark, the value of R_{var} is toggled back to 500 TΩ and kept in the 'high resistance' mode, until the end of the simulation is reached. The limitation on the value of R_{var} is that it should be high enough during the 'high resistance' mode as to not affect the circuit normal behaviour (e.g. the circuit frequency response).

As can be seen in Figure 7.6(b), the amplifier output voltage stabilizes around $V_{DC} = 500$ mV before the 300 ms time mark when the proposed simulation method is used. It takes 25 seconds for the simulator to simulate the mentioned 300 ms of the circuit time domain behaviour. However, when the simulation method is not used, the full simulation time length of 30 seconds is required for the output of the amplifier to stabilize near $V_{DC} = 500$ mV, and this would take 2489 seconds (41 minutes) to finish. A zoomed-in version of the simulated results between the 18 s and 20 s time marks (Figure 7.6(c)), proves that the presence of the ideal resistor R_{var} in the simulation setup has not disrupted the normal circuit behavior. As can be seen in Figure 7.6(c), the amplifier output in the case of not using the proposed method has started to closely follow the output in the case of using the simulation method. It would take the full simulation time for the outputs in the two cases to become indistinguishable, with a Root Mean Square Error (RMSE) of 1 μV calculated over the 28 s to 30 s time marks.

7.5 Discussion

This appendix described a simple simulation method to reduce the amount of simulation time required for time domain simulations of biomedical systems containing QIRs and switching circuits. By using the proposed method, only an ideal resistor or an ideal switch with a pulse control voltage would be required to be added to the simulation setup. An example sub-system containing a SC delay circuit, low pass filter, DC blocking circuit and OTA based amplifier was implemented to verify the efficiency of the proposed simulation method, and reasons for the suitability of the

example case were discussed. The time required for a 30 second long time domain simulation of the example subsystem was reduced by two orders of magnitude when using the proposed sub-system as opposed to when the method was not used.

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