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Titre : Dedicated Design Of Experiments and Experimental Diagnostic Tools for Accurate Reliability Investigations on AlGaN/GaN High Electron Mobility Transistors (HEMTs)

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It is the end of the Acknowledgement, and here I wish you courage if you dare to continue to the next pages.

Serge KARBOYAN
Toulouse, France
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Titre : « Développement de Procédures de Caractérisation et d'Analyse Dédiées à l'Etude de la Fiabilité des Transistors à Haute Mobilité Electronique AlGaN/GaN (HEMTs) »

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Le développement intensif et rapide des dispositifs HEMT à base de nitrure de gallium a été largement favorisé par les qualités intrinsèques du matériau pour proposer des performances élevées (haute puissance, haute fréquence…) et pour autoriser un fonctionnement en environnement extrêmement sévère (fluctuations thermiques, brouillage, tenues aux radiations ionisantes…) par rapport aux technologies concurrentes plus traditionnelles (Si, GaAs…). À ce jour, les dispositifs HEMTs AlGaN/GaN sont considérés comme une alternative prometteuse pour remplacer la technologie GaAs, et se positionnent comme d'excellents candidats pour des applications d'électronique de puissance, pour les applications TVSAT, des stations de base terrestres et des systèmes radar à large bande de fréquence (bande L à W), et pour les applications civiles et militaires. Cependant, il reste à lever certains verrous concernant des problèmes de fiabilité de ces dispositifs, qui affectent la durée de vie élevée attendue ; l'amélioration de la robustesse de ces technologies reste une phase critique à étudier malgré les progrès déjà réalisés. Plusieurs paramètres de fabrication affectent la fiabilité, tels que la passivation de la surface, le plateau de champ, le procédé de dépôt de la grille. Il est bien connu que l'étude de la fiabilité est complexe et ne pourra jamais être totalement accomplie, cependant les limites escomptées pour une exploitation raisonnable des filières GaN laissent entrevoir la possibilité de réels progrès dans ce domaine pour assoir le positionnement de ces technologies vis à vis des solutions concurrentes. Ce manuscrit de thèse présente les outils de diagnostic et les procédures de mesures associées développés pour mieux comprendre les mécanismes de dégradation sous-jacents de ces dispositifs. Les mesures électriques DC et pulsées à différentes températures sont présentées en premier lieu. Pour obtenir des informations au niveau microscopique sur la fluctuation des porteurs et des défauts dans les zones actives et passives du dispositif, des mesures de bruit basse fréquence sont effectuées sur les courant de grille et de drain sous différentes configurations : la diode seule (drain en l'air) et le transistor en régime saturé. Une technique électro-optique, l'OBIRCh (Optical Beam Induced Resistance Change technique), est aussi appliquée sur les mêmes composants : cette technique apporte d'autres informations quant à l'intégrité du composant (fluctuations de courant), et vient corroborer nos hypothèses sur l'activation de mécanismes piezoélectriques dans les zones fortement polarisées du composant.

Toutes ces techniques non-destructives permettent des analyses croisées. Un modèle original de la diode Schottky a été établi pour tenir compte de certains défauts d'homogénéité à l'intérieur du contact de grille à l'interface entre la diode Schottky et la couche semi-conductrice supérieure. D'autres résultats originaux ont été trouvés à partir des mesures de bruit basse

fréquence concernant la localisation des défauts actifs et leur évolution suite à l'application d'un stress électrique et thermique (HTRB, HTOL, …). Les analyses électriques (pulsées et transitoires) des phénomènes de retard à la commande (grille ou drain) sont partiellement corrélées aux analyses du bruit basse fréquences des courant de grille et de drain pour identifier les mécanismes sous-jacents de dégradations. Dernièrement, une ébauche de plan d'expérience (DOE) est proposée dans le cadre de notre travail, qui complètera celui mis en œuvre dans le cadre du projet ANR REAGAN impliquant tous les partenaires : des règles et des procédures expérimentales sont identifiées pour s'assurer que les données expérimentales sont fiables (i.e. reflètent statistiquement le comportement réel du dispositif).

Title: « Dedicated Design Of Experiments and Experimental Diagnostic Tools for Accurate Reliability Investigations on AlGaN/GaN High Electron Mobility Transistors (HEMTs) »

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Intensive and rapid development of GaN-based HEMT devices has been largely promoted by their extreme attraction and intrinsic capabilities for proposing high performances (high power and PAE, high frequency, moderate HF noise…) and for operating under different extreme conditions and harsh environment (thermal fluctuations, jamming, ionizing radiations…) over more traditional competitive technologies (Si, GaAs). More than ever, AlGaN/GaN HEMTs are considered as promising technology to replace the GaAs, and an excellent candidate for power electronics applications, for TVSAT applications, terrestrial base stations and radar transceivers operating over large frequency band (from L to W-band) for both civil and military applications. However, some remaining problems concerning the reliability of the devices affect the expected elevated lifetime, and the improvement of the robustness of these technologies stay a questionable phase to study despite the progress already made. Several fabrication parameters could impact the reliability such as surface passivation, field plate, gate deposition process (presence of spontaneous and piezoelectrical effects). It is well known that the reliability background is complex and will never be completely accomplished, but the margin between expected theoretical lifetime and results already obtained motivates efforts to give for an improved level of reliability. The following manuscript presents diagnostic tools and associated measurement procedures to better understand the underlying degradation mechanisms of such devices. Electrical DC and pulsed measurements at different temperatures are presented first. To get more microscopic information about the carrier flow and the defects in the active and passive areas of the device, low frequency noise measurements on the gate and drain currents are investigated under open drain (Schottky diode) and when the transistor is biased in saturated region. An electro-optical technique is also applied, called OBIRCh (Optical Beam Induced Resistance Change technique), on the same devices: this technique brings other expertise about the device integrity (current fluctuations).

All these non-destructive techniques are cross-correlated. Original Schottky diode models have been established to account for some inhomogeneities within the gate contact at the interface between the Schottky diode and the upper semiconductor layer. Some other original results have been found from Low Frequency Noise measurements concerning the location of the active defects, and their evolution after the application of thermal and electrical stresses (HTRB & HTOL). The electrical (pulsed and transient) analyses of lag effects are correlated to the harmonic low frequency analysis of the current spectral densities to identify the root trapping mechanisms. Lastly, a first Design of Experiment (DOE) is proposed in conjunction with our work, and also within the ANR REAGAN project involving all the partners: experimental rules and procedures are identified to ensure that the experimental data are reliable (i.e. reflect the actual behavior of the device, with statistical assessment).

CONTENTS

GENERAL INTRODUCTION

The needs for high power amplification at high frequencies are increasing for both military and civil applications. For military applications, they are focused on RADAR and communication systems, and for civil applications the market is competing for the most reliable and powerful wireless telecommunications and base stations. At last, the space applications (civil or military) are also concerned for the fabrication of satellites, base stations and radar systems for GPS tracking, meteorological applications, etc. All these applications require high power levels, high linearity and high frequencies for enhanced data rates. Thus, these requested features have led to the study of wide bandgap technologies and more precisely the Gallium Nitride (GaN).

The deep studies on the GaN technology restarted in the 90s. The semiconductor was considered very interesting due to its wide bandgap (to reach high voltages and high carrier densities), high saturation velocity of the carriers (to reach high current values at high frequencies), high breakdown voltages and excellent thermal management (allowing the semiconductor to evacuate the maximum calories more efficiently than the conventional GaAs). These properties give the Field Effects Transistors (FETs) robustness and performance required for applications at high power and high frequencies. Consequently, the high electron mobility transistors AlGaN/GaN fabricated within the GaN technology showed the same qualities added to this the high electron mobility in the 2DEG. However, with all these qualifications, the GaN-based HEMTs still suffer of reliability issues and need more investigations and failure analysis to stand as alternative solution for GaAs and Si technologies.

The work presented in this thesis is performed at LAAS – CNRS in Toulouse, France and is a part of ReAGaN - ANR project assembling six partners (UMS, IMS, TRT, LEPMI and SERMA) and the DGA French DoD (Department of Defense). The project addresses the reliability of the GaN technology in its industrialization phase. Its main objective is the development of advanced electro-optical and physical characterisation techniques dedicated to wide bandgap semiconductor technologies. For the first time, new analysis techniques are developed and their results are correlated leading to the identification and characterisation of nano-structural defects and physical mechanisms taking place in GaN technologies and potentially responsible for degradation.

Assuming the project and since this work is a part of it, hence this manuscript is organized around two main complementary axes.

The first axe consists of developing several original characterization procedures for the evaluation of AlGaN/GaN HEMTs. To do this, different set of multi-physical efficient experimental tools are established to get information about the main parameters leading to the degradation of the devices. Thus, the best experimental sets and methods are determined paying attention to the work environment of each technique; this represents a challenging program because of the high level of complexity since it comes to GaN technologies (electro-mechanico-thermal interactions, experimentally evidenced but rarely or hardly modeled). The characterisation techniques presented in this manuscript are the DC and pulsed measurements versus temperature, the low frequency noise characterizations, the EBIC and OBIRCh electro-optical techniques and the I-DLTS.

The second axe consists of measuring, characterizing, and analyzing the results carried on several sets of virgin and stressed AlGaN/GaN HEMT structures. The differences in these structures are present in the gate width and length, the number of gate fingers, the impact of the field plate, the leaky property, the stresses, etc. Thus, it can be seen that the main area of this study is focused on the "gate structure". As a large number of set of devices have been investigated a rigorous classification is needed (technological declination, stress type, etc.). The device procurement from UMS (our manufacturer) is decided in accordance with the priorities of the project and the needed steps to identify the main issues to better understand the failure mechanisms. Destructive and non-destructive techniques are applied on the transistors; the following work presents only non-destructive techniques and their reproducible results.

When the two axes are completely achieved and understood, here it comes on two main conclusions: support to the process validation and the definition of innovative GaN analysis toolbox. The first concerns a feedback to the manufacturer on the failure analysis of part coming directly from the reliability test ongoing at UMS; as well as the new decisions made on the fabrication process to improve the reliability (MTTF) and the terms of use of the devices to expand their market. The second conclusion is to define a relevant failure analysis methodology for the GaN-based technologies developed by UMS. At the end, strengths and drawbacks of each characterization technique, electrical or physical, investigated in the project are examined as a function of each failure mode.

Chapter I:

GALLIUM NITRIDE (GAN) AND ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS (HEMTS): DEVICES AND RELIABILITY

I.1 Introduction

Wide bandgap semiconductors (SC) and more precisely Gallium Nitride (GaN) technology differs from existing Silicium (Si) and Gallium Arsenide (GaAs), since it presents qualities for high power, high temperature and high frequency applications, with high breakdown voltages and improved thermal management. This technology has attracted a lot of attention for both, civil and military applications and stands as promising candidate to replace the traditional Si and GaAs technologies for power modules but also for high frequency robust receivers. Hence, considering the high potential of such GaN technologies, many efforts have been given to develop devices for high power, high frequency and robust applications.

However, in spite of all the qualities of these materials, reliability assessment of these technologies is not mastered yet. Some industrial processes have been qualified, but it is well accepted that the ultimate limits of these technologies have not been reached yet. Moreover, it is also of great interest to understand the root causes limiting the reliability to develop devices and to push up the performances of GaN technologies, and thus to broaden their market. The impact of benefiting of high power transistors concerns the last stage power, but also the power added efficiency of the power module, and thus the DC power saving and thermal management.

The chapter is organized as follows. In the next section, a short overview on the history, the economic and market relevancies of this technology are presented. Section 2 discusses the wide bandgap semiconductors and their properties: the bandgap, the mobility and the breakdown voltage. The AlGaN/GaN high electron mobility transistors (HEMTs) are presented in section 4, highlighting on the capacity of the transistor for high power and high temperature applications in comparison with

competitive solid states technologies (Si and GaAs). The piezoelectrical and spontaneous polarizations as well as the thermal management at the device and circuit level are presented next, followed by the reliability study cases according to different stresses. Since the reliability is the concern of the present work, the next two sections highlight mainly on the reliability study and the degradation mechanisms that limit the optimal operating conditions of a device. Section 9 sets the conclusions drawn from this overview on the GaN and AlGaN/GaN HEMTs.

I.2 History, economic and market relevancies

I.2.1 History

The first Gallium Nitride (GaN) crystal is fabricated and studied by Johnson *et al.* [1] in 1932 and its first applications appeared afterward in 1971 by the demonstrator of the electroluminescent diode Pankove *et al.* [2]. In 1986, Amano *et al*. [3] developed another GaN layer grown with MOCVD technique on sapphire substrate with better optical and electrical properties. Then the motivations to study the GaN material have been started by the same team, that in 1989 developed p-type conductive GaN layer [4].

As for the transistor, the first HEMT demonstrator was developed in the late 70s by a researcher called Takashi Mimura working in Fujitsu laboratories [5]. The transistors were based on AlGaAs/GaAs grown on Si, GaAs or InP substrates. In 1980 the first publication on GaAs HEMT appeared. **Figure I-1** extracted from [5] presents the first Mimura's sketch of the energy band diagram explaining the operating principles of the first HEMT.

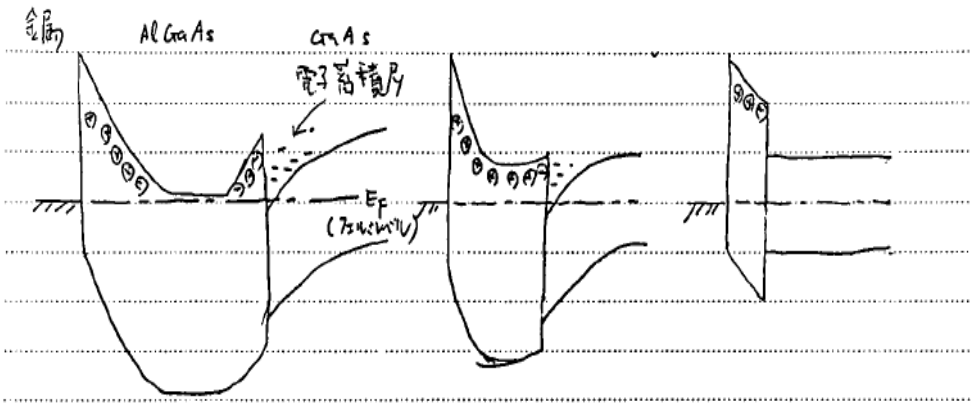


Figure I-1. Sketch of the energy band diagrams explaining the operating principles of the first HEMTs by Mimura [5].

In order to target high power amplification and high frequency applications, in the 90s GaN based HEMTs were found to be an interesting alternative as a promising technology. These devices were grown on Sapphire, Si or SiC and even GaN epitaxies. They were first reported by M. Khan *et al*. in 1991 [6] with 9% of Al and the structure displayed a peak mobility of 1980 $cm^2V^{-1}s^{-1}$ at 77K. Between 1994 and 1997, with advancements of studies on the GaN material quality and on the heterostructure design of the transistor the first AlGaN/GaN HEMTs feature a high potential for

microwave electronics and an interesting solution for civil and military applications. The United States of America, Japan and Europe are the first to invest on this technology.

I.2.2 Economic and market relevancies

GaN technologies allow saving large amount of energy with the emergence of low consumption lightning system, based on high quantum yield LED. This will become a standard in car and public light for electronic purposes. The use of re-configurable system will limit also the electrical consumption of telecommunication systems and base station, through relaxed thermal budget and higher electrical yield.

Figure I-2 illustrates the gain of energy when using GaN technologies in UMTS base station. Moreover, the consumption of amplifier and cooling system represents 60% of the total consumption of a full rack. Fujitsu has recently published an example of narrow band transmitter for Wi-Max application based on GaN technology and using a pre-distorsion function to optimise the yield [7]. The module presents tremendous electrical yield and size characteristics which illustrate the saving energy foreseen with such technology.

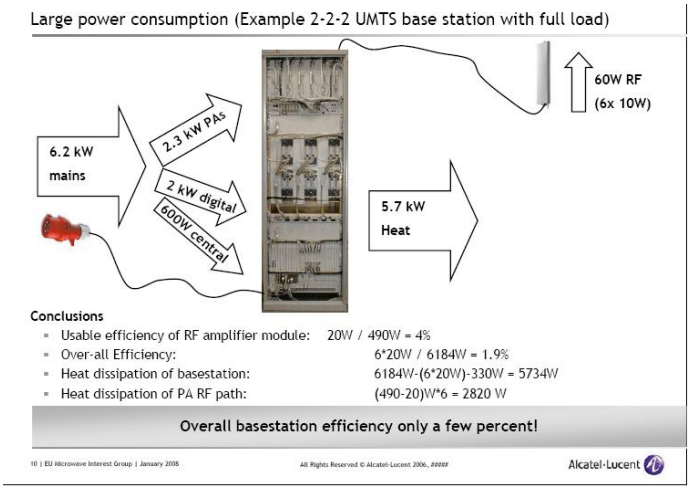


Figure I-2. Actual base station electrical consumption – Alcatel-Lucent source.

The improvement of electrical yield associated with a better linearity will have a direct impact on the energy consumption but also will relax the thermal management constraint at power supply level. Also, the use of high operation voltage reduces resistive losses in wire reducing size and save weight and material use.

European situation and stake on the GaN technologies development

In Europe, Germany benefits of the early massive investment from the minister of defence and of industry in technological research institute in cooperation with industry in the field of defence (EADS) and telecommunication (Infineon, NXP). These efforts have been concentrated at IAF (Fraunhofer-Institute for Applied Solid-State Physics, Freiburg), for defence applications and at FBH (Ferdinand Braun Institut für Höchstfrequenztechnik) at Berlin for RF applications.

The most important R&D effort in UK takes place at QinetiQ. Nevertheless, since the buyout of Filtronics by RFMD, the transfer of technology from QinetiQ is difficult to foresee without a strong

effort from the government. Main development in Italy are centralised in Selex and mainly oriented on high frequency applications. Like their PHEMT GaAs processes, GaN development will stay captive for military and space application, for terrestrial base station – TVSAT applications, etc.

A significant effort has been made by the European Defence Agency (EDA) and the Department of Defence (DoD) of leader countries through the Korrigan project which involved 7 European nations through research laboratories, institutes and industries including UMS. The main objective of this project is to set a common technological basement involving experimental foundry.

In France, the Ministry of Defence has supported the development of GaN HEMT via the industrial laboratory Alcatel-Thales III-V Lab., which is in charge of the upfront and prospective scientific development benefiting to UMS. Also, the ANR in coordination with the Ministry of Defence, the Ministry of Research and the CNES, has also initiated various R&D activities covering material development, reliability or the evaluation of basic functions (ANDRO, CARDYNAL projects for device characterisation and demonstrations)

UMS (a Thales-EADS joint venture) has initiated transfer activities of GaN technologies by optimising key process step on its industrial manufacturing tool. These developments are made in cooperation with III-V Lab and IAF in Germany. The main targeted applications are defence, space, and telecom (in particular the RF power transistor for the new generation of base stations).

This transfer activity is now supported by 5 years German-French MOD program (GaNTA) and by ESA (GREAT2). The objective of these programs is the industrialisation of GaN processes at UMS. The qualification of the first GaN process for RF-defence and telecommunications applications is planned for mid-2010.

UMS is currently developing two technologies:

- A Power bar technology GH50 based on 0.5µm gate length transistor. The GH50 technology is dedicated to cover high power applications (>100W power bar in S/C band) up to 10GHz.
- A Monolithic Microwave Integrated Circuit (MMIC) technology GH25 based on 0.25µm gate length transistor and including passive components. GH25 technology aims to cover high frequency and wide band applications up to 18GHz.

Both technologies are built from GaN on SiC substrate for its high thermal properties.

The technologies will be updated generation by generation to reflect all the technology steps up over time, following a continual improvement approach.

These international programs include evaluation and qualification activities. The following work in this manuscript is supported by ReAGaN ANR project that aim to develop basic knowledge of the reliability of UMS GaN processes during its industrialisation phase.

Even if other projects, as GaNTA and GREAT2, are mainly focused on the feasibility of demonstrators by these breaking technologies, reliability considerations are also investigated. For its part, ReAGaN intends to develop innovative tools and adequate methodology dedicated for GaN technologies. Also, to complete the industrial strategy, results from ReAGaN will benefit to product development for example in the project ATTITUDE 4G (ANR Verso).

Results from previous projects like Korrigan (EDA), ESA – AO1-3916/01/NL/CK, ANDRO (RNRT), CARDYNAL (ANR) where most of the ReAGaN partners were involved, will fully benefit to the present project.

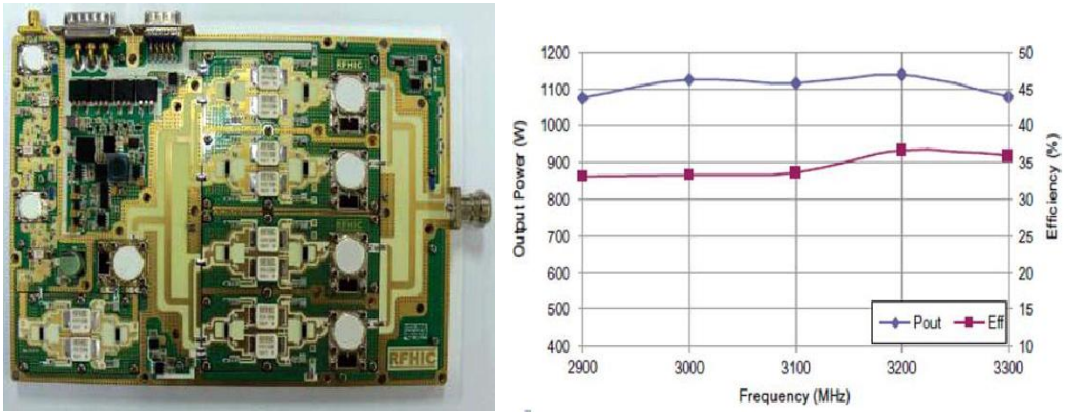
The ReAGaN project is an original and innovative research program dealing with the deep understanding of parasitic effects and degradation mechanisms of GaN technology as it proposes the combined use of physical observations of nanometric defects and macroscopic opto-electrical characterisation on material and devices.

The outcomes of the project allow speed–up the time to market of the European industrial leader in GaN technology. It participates to the competitiveness of European industry in the field of telecom applications by defining standard methodology dedicated to such technology.

I.2.3 Applications

Since GaN HEMTs offer an abilities for high voltage and high temperature operation. This allows them to be targeted by industrial, defense, medical and commercial applications. Next are proposed some few realizations of GaN based amplifiers featuring high performances:

- Kwack *et al*. [9] reported the design and manufacture of GaN based highly integrated S-band Solid State Power Amplifier delivering a very high power of 1 kW in the frequency range of 2900 to 3300 MHz and a typical PAE of 34%. **Figure I-3** shows the practical implementation and the measured output power and efficiency of 1kW S-band PA. The low weight and good efficiency make this SSPA very attractive for radar applications.



(a) (b)

Figure I-3. Practical implementation (a) and measured output power and total line up efficiency (b) of 1 kW Sband GaN HEMT PA. [9]

- Fujitsu developed high efficiency GaN HEMT power amplifier for W-CDMA base station applications with a characteristics of 174 W output power with 63 V operation [10]
- Saito *et al*. from Toshiba R&D center reported on the fabrication of current collapseless high voltage (480V/2A) GaN HEMT by using dual field plate structure and back side field plate (on the conductive substrate). Boost converter circuit is also fabricated with an output power of 54 W, high PAE of 92.7% and high switching frequency of 1 MHz [11].

- The HF highest output power of AlGaN/GaN HEMTs on Si and SiC substrates is 12.88 W/mm and 30.6 W/mm at f=2.14 GHz and f=8 GHz respectively, this results are demonstrated by Hoshi *et al.* [12] and Wu *et al.* [13] respectively.

The advantages of GaN HEMT amplifiers are synthesized in **Table I-1**.

Physical property	Advantage of HEMT	Advantage of amplifier
High breakdown voltage	High voltage operation High load impedance Good linearity	Easy harmonic processing (higher efficiency) Low matching loss Simplified voltage conversion
High heat conductivity	High temperature operation	Small, lightweight cooling system
High current density	High power operation Small chip size	Small, lightweight amplifier

Table I-1. Advantages of a GaN HEMT amplifier. [10]

I.3 Wide bandgap semiconductors: electrical parameters

The wide bandgap semiconductors and more specifically the III-N composites like GaN and AlN are excellent candidates for high power and high frequency devices. They present properties for high thermal conductivity, high breakdown field and high velocity of free carriers. These technologies present alternative solutions to meet the needs for the fabrication of high power devices.

Table I-2 resumes the main physical and electrical parameters for different materials. The main parameters qualifying a technology are detailed afterward.

Technology	Si	GaAs	4H-SiC	InP	GaN	AlN	Diamond
E_g (eV)	1.12	1.43	3.26	1.3	3.39	6.2	5.45
n_i (cm^{-3})	1.5×10^{10}	1.79×10^{6}	8.2×10^{9}	-	1.9×10^{10}	1×10^{31}	1.6×10^{27}
ε_r	11.8	12.5	10	12.5	9	8.4	5.5
μ_n ($cm^2V^{-1}.s^{-1}$)	1350	8500	750	5400	1500	1100	1900
E_c (10^6 Vcm^{-1})	0.3	0.4	3	0.5	3.4	-	5.6
V_{sat}($.10^7$ $cm.s^{-1}$)	1	2	2	1	2.5	2	2.7
T_{max} (°C)	300	300	600	150	700	-	-

Table I-2. Electrical parameters of different technologies used for the fabrication of electronic devices [14] [15] [16].

I.3.1 Bandgap

The bandgap (E_G) is the gap between the lower energy of the conduction band (E_C) and the higher energy of the valence band (E_V). It is the energy necessary for an electron to reach from E_V to E_C. The high power capability of the GaN technology is mainly related to its wide bandgap of 3.4 eV in comparison with Si and GaAs (**Table I-2**).

The HEMT is then formed by associating high and low bandgap-s to form the Two Dimensional Electron Gas (2DEG) at the interface. The concentration of the carriers in the 2DEG is 10 times larger than that of Si: this leads to a large drain current and hence to an improved amplification.

The bandgap is temperature dependent as it decreases when the temperature increases because the material expands; Eq. 1 shows the dependence of the bandgap from the temperature [15]:

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T+\beta} \qquad (1)$$

Where T is the temperature in Kelvin and α and β are constant coefficients equal to 7.7×10^{-4} eV.K^{-1} and 600 K respectively. The bandgap of the AlGaN barrier lowers (as well as the breakdown voltage) of 0.1 eV when the temperature increases from 298K to 523K.

I.3.2 Surface mobility

In some words, it is related to the free carrier transportation in the SC, any modification in the crystal lattice causes a change in the mobility. **Figure I-4** extracted from [17] compares the calculated temperature dependencies of the electron mobility in bulk GaN and GaAs with and without accounting for the impurity scattering. From this figure, it can be concluded that the electron mobility in bulk GaN is less sensitive to ionized impurity scattering than that in GaAs.

For high frequency applications, a high mobility and high saturation velocity are required. The mobility in the GaN (and SiC) being smaller than that in GaAs, hence this stands as a disadvantage for the fabrication of devices (such as HEMTs) for high mobility applications. However, these values of mobility in GaN are sufficient for transistors specifically designed for high power operation.

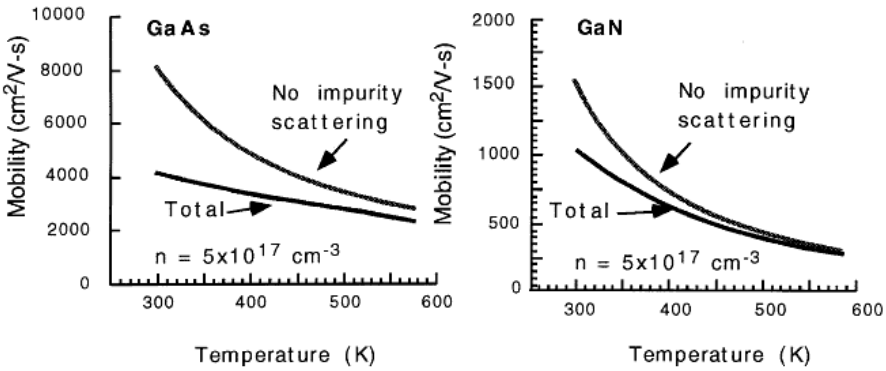


Figure I-4. Calculated temperature dependencies of the electron mobility in GaAs and GaN with and without accounting for the impurity scattering [17].

I.3.3 Breakdown voltage

The breakdown of any device is usually caused by impact ionization. Moreover, the measurement of the breakdown voltage for normally-on devices is very difficult due to the high powers that they can resist and to excessive self-heating. Thus, the breakdown voltage measured under normally-off configuration will be the relevant parameter.

Figure I-5 - extracted from [17] - shows the computed velocity-electrical-field characteristics of GaN and GaAs at different temperatures. It can be concluded that GaN devices are less sensitive to temperature, able to sustain self-heating and suitable for high temperature applications. Hence, from all these characteristics, this figure highlights the ability of GaN versus GaAs for high power and high temperature applications. Considering that Si and GaAs HEMTs represent today's conventional devices in the market, GaN HEMTs on SiC (Si, also even if less developed but still on the roadmaps for some developers such as Nitronex and Triquint) are expected to be the next generation power devices. Because GaN-HEMTs on Si are still suffering from low breakdown voltages (for example the breakdown voltage of 600V is observed on an HEMT with a 2 µm epitaxial layer on Si substrates, while for the same thickness 1.9 kV has been extracted on a SiC substrate). Some solutions are still under study to improve the device breakdown voltage like increasing the buffer thickness as proposed in [18] where 1.8 kV has been observed or doping the buffer with Fe or C [18]: these parameters are essentially important considering switching applications (switches, class E, F … amplifiers). However, for RF applications, the improvement on the junction temperature (reduction) and on the power added efficiency (PAE increase) represents the real challenges for the GaN technologies.

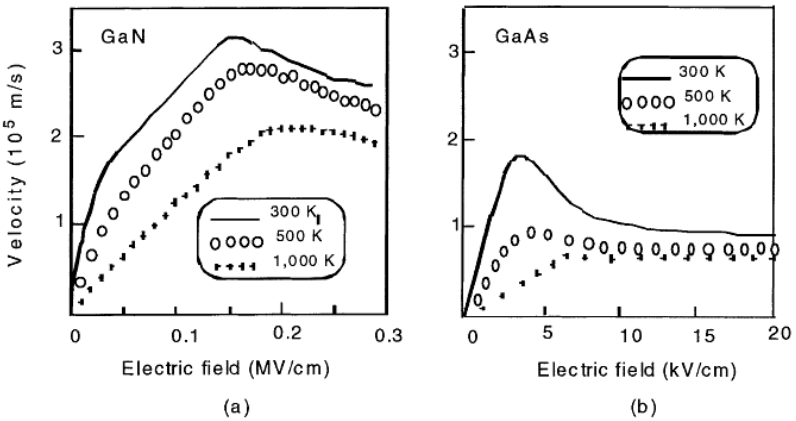


Figure I-5. Velocity electrical-field characteristics of GaN (a) and GaAs (b) at different temperatures. (a) is after [19]. (b) is computed using the Monte Carlo calculation's fit reported in [20] for the following values of the low field mobility: 7000 $cm^2.V^{-1}s^{-1}$ at 300K, 3000 $cm^2.V^{-1}s^{-1}$ at 500K and 1100 $cm^2.V^{-1}s^{-1}$ at 1000K.

I.3.4 Figure of merits for power modules

A figure of merit is necessary to evaluate the potential of a material with the intended application. Several figures of merits exist [39] [40] [41]:

- Johnson's figure of merit (JM) for high frequency devices

$$JM = \left(\frac{E_c v_{sat}}{\pi}\right)^2 \quad (2)$$

- Keye's figure of merit (KM) when considering thermal limits

$$KM = k_T \left(\frac{c v_{sat}}{4\pi\varepsilon}\right)^{1/2} \quad (3)$$

- Baliga's figure of merit (BM) for power commutation

$$BM = \varepsilon \mu E_c^3 \quad (4)$$

- Baliga's figure of merit (BHFM) for fast power commutation

$$BHFM = \mu E_c^2 \quad (5)$$

The different figures of merit are presented in **Table I-3** for different technologies and normalized versus Silicium's figure of merit. From this table if we consider the JM or the BHFM that are figures of merit for high frequency and high power respectively, we notice that the wide bandgap semiconductors in bold are the best for high frequency and high power applications.

	Si	GaAs	**4H-SiC**	**GaN**	**AlN**	**Diamond**
JM	1	7.1	**180**	**760**	**5120**	**2540**
KM	1	0.45	4.6	1.6	21	32.1
BM	1	15.6	130	650	31700	4110
BHFM	1	10.8	**22.9**	**77.8**	**1100**	**470**

Table I-3. Normalized figures of merit of important semiconductors for high-voltage power devices. [39] [40] [41]

For high frequency applications, some other figure of merits are more prone to make comparison between technologies, such as the transition frequency f_t, the maximum oscillation frequency f_{max} and also the power added efficiency η_{PAE} for power modules.

I.4 HEMT devices

I.4.1 General information

High Electron Mobility Transistors (HEMTs) using AlGaN/GaN heterojunction also known as Modulation-doped FET (MODFET) or Heterojunction FET (HFET), are devices featuring a junction between two different bandgap regions; one undoped (GaN) and the other lightly doped (or also non-intentionally doped, the AlGaN layer). **Figure I-6** shows a schematic illustration of the transistor.

The transistor can be developed using two techniques: the MetalOrganic Chemical Vapor Deposition (MOCVD) technique and Molecular Beam Epitaxy (MBE) techniques.

As for the fabrication of the device, due to lattice mismatch between GaN and the substrate (Si, SiC, GaN or Al_2O_3) several layers are added on the Si substrate before introducing the GaN layer. **Table I-4** presents the thermal conductivity and the lattice mismatches between the GaN and many substrates: it can be noticed that a GaN substrate matches the best but the conductivity stands better for a SiC substrate. The very low thermal conductivity of the sapphire substrate prevents it to be used for high power applications although its low cost, hence the Si stand as compromising candidate due to its better thermal conductivity and low cost in comparison with SiC (as well as the possible compatibility with Si technologies for digital command). Etchings in the AlGaN layer are performed for the Ohmic contacts necessary for source and drain terminals. The Schottky contact and the gate access are the first parameters to investigate when studying the gate control and

leakage conduction mechanisms. The gate voltage modulates the channel conduction. In this work, normally-on transistors are presented.

Substrate	Thermal conductivity ($Wcm^{-1}K^{-1}$)	Lattice mismatch (%)
Si	1.5	17
SiC	4.9	4
GaN	1.7	0
Al_2O_3	0.5	14

Table I-4. Thermal conductivity and lattice mismatch of different substrates

The characteristics of such devices for high power applications are the maximum drain–source current I_{max} and the transconductance gain g_m given below:

$$I_{max} = qn_{s0}v_s \qquad (6)$$

$$g_m \approx \frac{qn_{s0}\mu/L_G}{\sqrt{1+\left[\frac{\theta n_{s0}\mu(d+\Delta d)}{\varepsilon_d v_s L_G}\right]^2}} \qquad (7)$$

as well as the transition frequency (f_T) and the maximum oscillation frequency frequencies (f_{max}):

$$f_T = \frac{g_m}{2\pi(C_{GS}+C_{GD})} \qquad (8)$$

$$f_{max} = \frac{f_T}{\sqrt{4[1+(R_S+R_G)g_0]+2\left(\frac{C_{GD}}{C_{GS}}\right)\left[\frac{C_{GD}}{C_{GS}}+g_m\left(R_S+\frac{1}{g_0}\right)\right]}} \qquad (9)$$

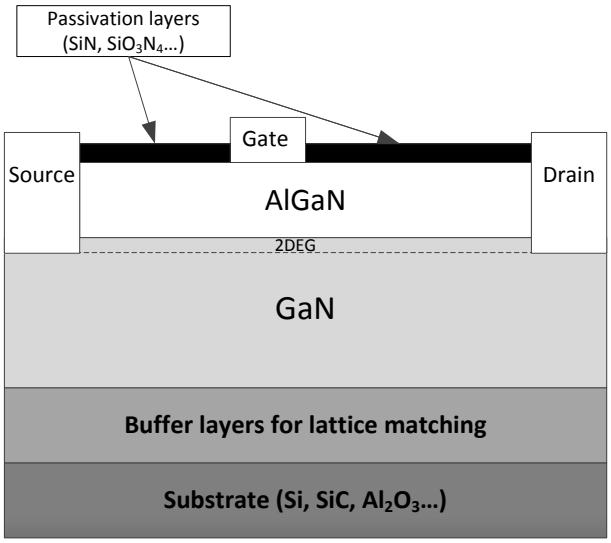


Figure I-6. Schematic cross section of the AlGaN/GaN HEMTs under test.

Figure I-7 [21] shows the commercialization roadmap of GaN HEMTs for several applications in the different frequency ranges. Since 2005, commercialized power amplifiers for wireless base stations exist. The expectations highlight on wireless mobile networks to move up to 4G mobile technologies and then to go deeper for millimeter wave communications.

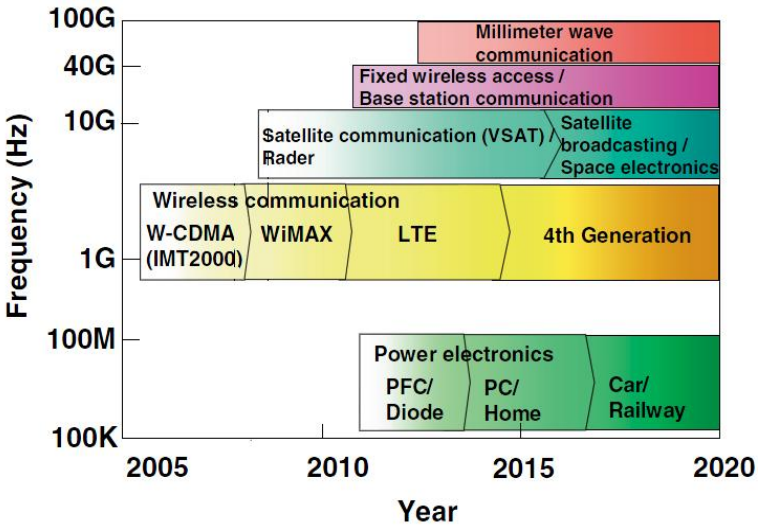


Figure I-7. Commercialization roadmap of GaN HEMTs for several applications in different frequency ranges. [21]

I.4.2 GaN versus GaAs and InP power HEMTs

The GaN based devices are the upcoming alternative solution for Si, GaAs and InP based high frequency power HEMTs. Thus, it is of great importance to compare between HEMTs based on these technologies knowing the fact that Si and GaAs-based devices became commercial long time ago, contrarily to GaN and InP HEMTs that are still between laboratory and market products; these latter still suffer of lack of reliability (GaN) or high cost of production (InP, GaN), hence they need more investigations before emerging completely the market.

Based on the results presented in **Table I-5**:

- The high breakdown voltages and excellent thermal conductivities allow a device to behave at high efficiency characteristics at full power. Consequently, the thermal conductivities of GaN are up to 2 $W.cm^{-1}K^{-1}$ versus 0.46 $W.cm^{-1}K^{-1}$ for GaAs.
- InP HEMTs provide the highest f_T and f_{max} due to high v_s so they are only used at high frequencies due to the high cost of production.
- Moreover, due to its wide bandgap, the GaN based HEMTs can reach higher intrinsic temperatures (up to 700°C) and are less sensitive to temperature variations than the GaAs (T_{max}=300°C). So, GaN devices can operate with less cooling in complicated structures and are suitable for high temperature applications more than the GaAs devices.

Device	Heterojunction	μ ($cm^2V^{-1}.s^{-1}$)	K_{300K} ($W.cm^{-1}.K^{-1}$)	V_{br} (V)	f_T (GHz)	f_{max} (GHz)
GaN HEMT	$Al_{0.3}Ga_{0.7}N/GaN$	1180	2	40	65	180
GaAs PHEMT	$Al_{0.3}Ga_{0.7}S/GaAs$	8500	0.46	7	130	250
InP HEMT	$Al_{0.5}In_{0.5}As/In_{0.6}Ga_{0.4}S$	13000	-	5	290	480

Table I-5. Typical values of parameters in various power HEMTs. [22]

Moreover, **Figure I-8** shows the power and frequency ranges of different technologies and semiconductors present today in the market. It can be seen, that GaN HEMTs reach high powers (≅ 1kW) at high frequencies (≅ 100GHz), contrarily to GaAs and Si-based devices.

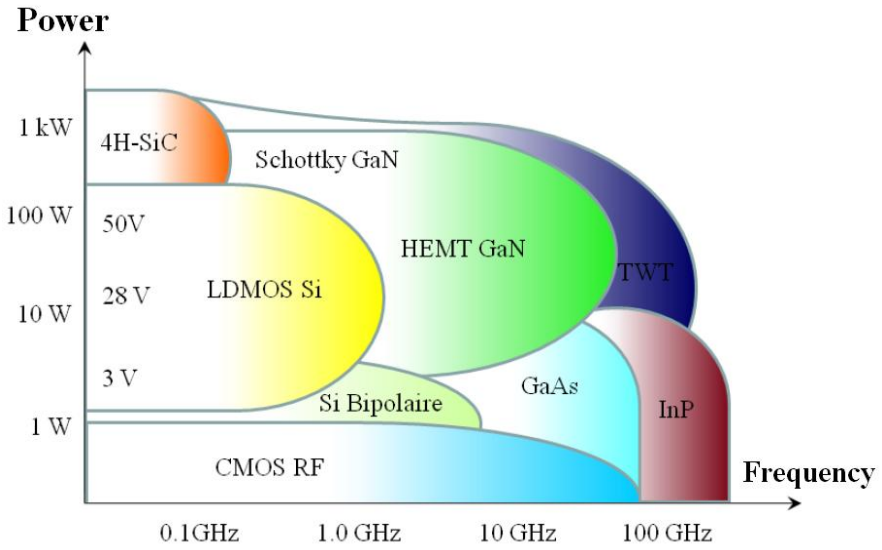


Figure I-8. Power versus frequency ranges of different semiconductor materials. [23]

I.4.3 Gate access: Schottky contact and gate current carrier transport

I.4.3.a Schottky contacts

The carrier transport control is a concern; and for reliable devices, the Schottky and Ohmic contacts must be controlled rigorously and mainly during the fabrication of the device.

The purpose of the Schottky contact is to create a space charge region that modulates the carriers in the channel, and to stand as a barrier that prevents from a high leakage current of the gate. Hence, this contact has an important impact on the reliability and its degradation affects the device operation. Thus, a poor Schottky contact presents high gate leakage current conduction mechanisms. The I_G-V_{GS} measurements of a transistor bring information about the leakage level (I_G=0A for ideal conditions). The well-known Schottky barriers are usually made by deposition of different transition metals such as: Ni/Au, Ni/Ti/Au and Pt/Au. The effects of temperature are a first parameter to consider to metal diffusion, also called “gate sinking”. Several studies showed that slight metal diffusion of the barrier height made with WSiN/Au and Ir/Au was observed at 500°C during a stress of 120 hours whereas Schottky contacts made with Pt/Ni degraded under the same experimental conditions [24] [25] [26].

I.4.3.b Gate current carrier transport

Several models are proposed in the literature for carrier transport across contacts and interfaces, Padovani and Stratton [27] first evoked on the transport mechanism in 1966 (and most of the papers and models in the literature afterward were based on their considerations). They distinguished three different conduction mechanisms of the gate current: the Thermoionic Emission (TE), the Thermoionic Field Emission (TFE) and the Field Emission (FE) (**Figure I-9** and **Figure I-10**). These three

mechanisms are observed under forward and reverse gate-to-source biasing conditions. The analysis of the current-voltage characteristics reveals the existence of each emission. In their paper, the experimental results are performed on GaAs and Si diodes showing good agreement with the theory. The forward and reverse gate current-voltage characteristics bring information on the emission type in Schottky barriers as follows:

Forward current-voltage characteristic

The electrons tunnel directly from the conduction band of the semiconductor into the metal. At low temperatures, the electrons tunnel from the bottom of the conduction band that represents the only contribution to the current. At an intermediate temperature range, the electrons tunnel at an energy E_m above the conduction band smaller than the energy E_b of the top of the barrier. At higher temperatures, the TE dominates and the electrons are emitted over the top of the barrier [27]. These emissions are illustrated in **Figure I-9**.

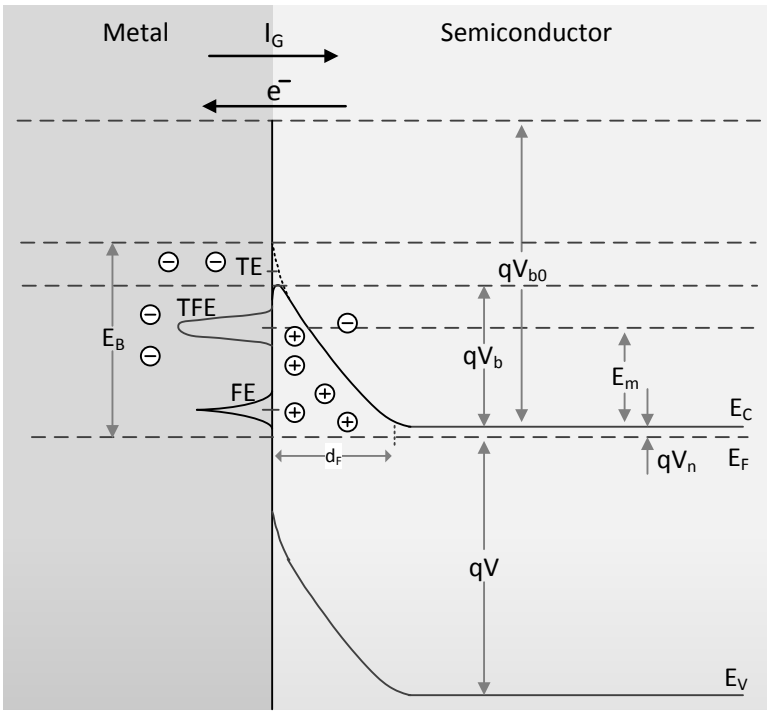


Figure I-9. Electron potential energy diagram of a forward biased Schottky barrier. TE, TFE and FE present the emission types and the distribution density probability of each type is shown in the figure. [27]

Reverse current-voltage characteristic

The reverse bias applied to the gate access increases the field in the junction and thus increases the probability for an electron to tunnel from the metal into the semiconductor. Similarly, under reverse conduction mechanisms the FE and TFE are also the dominant parameters. At low temperatures, most of the electrons originate from the Fermi level of the metal. At intermediate temperature range, the conduction occurs between the Fermi level of the metal and the top of the barrier (E_B) at an energy level E_m. According to Padovani and Stratton [27], under reverse conduction

mechanisms, there is no consideration of higher temperatures where the conduction is controlled by reduction of the barrier height by image force correction that is more important under reverse biasing conditions and presented in Eq. 6; the effective barrier height calculated from the traditional current voltage expression will include the image force lowering [28]. **Figure I-10** illustrates the electron potential energy diagram of a reverse biased Schottky barrier.

$$\Delta\varphi = \sqrt{\frac{qE}{4\pi\varepsilon_S}} \qquad (10)$$

where E is the electric field at the metal-semiconductor interface and q is the electron charge.

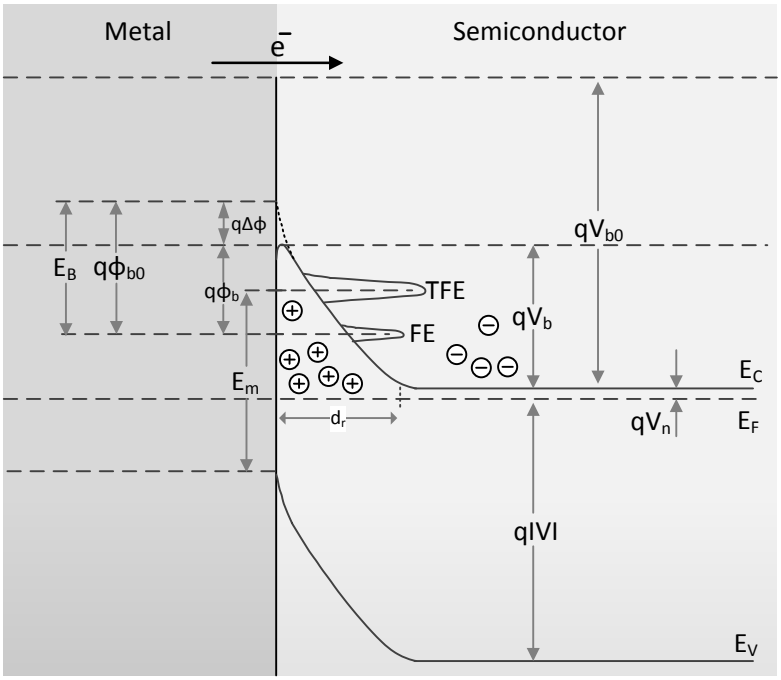


Figure I-10. Electron potential energy diagram of a reverse biased Schottky barrier. [27]

In the present document, the study is focused on the forward conduction mechanisms and on the reverse conduction mechanisms, even if more attention is given to the exploitation of forward biasing conditions.

The tunneling electrons can accumulate and conduct along the surface of the SC near the gate, creating a virtual gate effect and increasing the gate length. As the tunneling proceeds, an I_{GD} leakage current is also established between the gate and the drain terminals. The tunneling electrons can go also deeper into the SC (deeper in the AlGaN layer) to reach the 2DEG conducting channel [29], and here the gate access loses the control of the drain current rate in the channel. Solutions are used to reduce the tunneling electrons through the barrier: the reduction of the leakage current can be obtained by adding a field plate (that lowers the maximum voltage into local zones of the device, near the gate edges) as well as by using an efficient passivation layer. A model is presented in the literature to reduce the tunneling leakage current. [30]

Figure I-11 extracted from [29] shows the electron tunneling leakage from the gate electrode and its possible current paths. According to Trew et al. *"the electrons that tunnel from the gate electrode can [29]:*

- *Accumulate on the surface of the semiconductor next to the gate.*
- *Conduct along the surface by a trap-to-trap hopping mechanism creating a gate-to-drain leakage current.*
- *Possibly travel through the AlGaN layer to the two-dimensional electron gas (2DEG) conducting channel."*

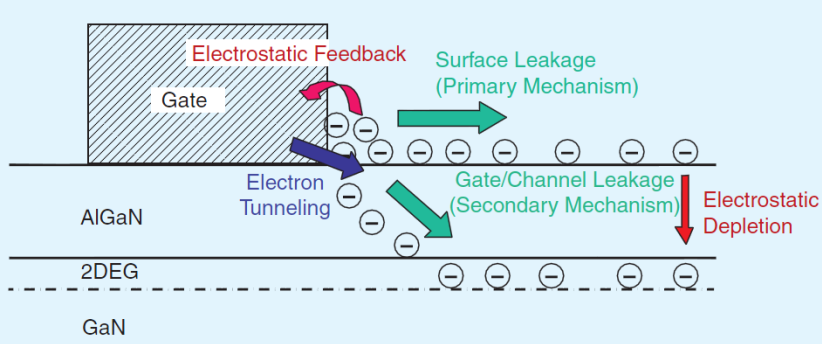


Figure I-11. Electron tunneling leakage from the gate electrode and possible current paths.[29]

I.4.4 Drain and source accesses: Ohmic contacts

As for the Ohmic contacts, Ti/Al alloys are usually used for the fabrication of drain and source Ohmic contacts. Since the Aluminium presents risks for cracks and oxidations, other alloys of transition metals are also studied such as Ti/Au, Ni/Au, Pt/Au, Ir/Au and Nb/Au for more robust Ohmic contacts. Some contacts made by deposition of Ti/WSiN/Au has shown stability at 800°C for 20 minutes and classic contacts such as Ti/Al/Ni/Au with WSiN barrier has shown stability at 500°C for 120 hours. [24] [26]

The drain current carrier transport is also important to be controlled at the drain and source Ohmic contacts that govern the drain current. Moreover, the interface AlGaN/GaN where the carrier flows is also a concern and the roughness of this interface and the dislocations generated from the substrate may create trapping/detrapping effects. The contact resistors of the source (R_S) and the drain (R_D) accesses may reduce the current and hence the power in the channel. In the Ohmic region, the drain current is linear versus V_{DS} following the well know Ohm's law with a resistance equivalent to the sum of the drain and source resistors, as well as the channel resistance ($R_{eq}=R_D+R_S+R_{Ch}$). The saturation of the current appears between 5 and 10 $kVcm^{-1}$.

I.5 GaN technology: a matter of electro-mechanico-thermal management

I.5.1 Piezoelectric and spontaneous polarizations

I.5.1.a Piezoelectric polarization

The GaN technology and all other III-N nitrides such as AlN and InN suffer of large piezoelectrical and spontaneous polarization effects at heterointerfaces [22], under the gate in the AlGaN layer and also in the GaN buffer layer. The piezoelectric effects appear when the layer is submitted to stresses that change the symmetric characteristic of the crystal (due to mechanical stresses).

The generation of piezoelectric strain can lead to the creation of defects that can act as traps for electron transport. GaN and AlN show strongly pronounced piezoelectric effects and because of the Wurtzite properties of GaN and AlGaN structures, the crystal growth is in the c-axis direction, all these considerations affect directly the electric field in the direction perpendicular to the AlGaN/GaN heterointerface. According to Ambacher *et al*. [31] in Wurtzite structure AlGaN/GaN HEMTs, the piezoelectric polarization of the strained top layer is more than five times larger as compared to AlGaAs/GaAs structures. This may lead to a significant increase of the sheet carrier concentration at the interface. The increase of charges can generate trapping-detrapping processes and lag effects in the device. The piezoelectric polarization in the $Al_xGa_{1-x}N$ is given by:

$$P_{pzAlGaN} = \varepsilon_{GaN} F_{GaN} - \varepsilon_{AlGaN} F_{AlGaN} \qquad (11)$$

where ε_{GaN} and ε_{AlGaN} are the dielectric constants, and F_{GaN} and F_{AlGaN} are the interface values of the electric field in GaN and AlGaN layers respectively and P_{AlGaN} is the piezoelectric polarization in the AlGaN layer. In Wurtzite structures, P_{AlGaN} can be expresses in terms of the AlGaN piezoelectric coefficients e_{31} and e_{33} given by:

$$P_{pzAlGaN} = \pm 2 \left(e_{31} - \frac{e_{33} c_{13}}{c_{33}} \right) u_{xx} \qquad (12)$$

where c_{31} and c_{33} are the AlGaN elastic constants and u_{xx} is the strain component in the interface plane. If the dislocations do not relax the strain, then the strain component is given by:

$$u_{xx} = \frac{a_{GaN}}{a_{AlGaN}} - 1 \qquad (13)$$

For an AlGaN/GaN heterojunction, the non-linear dependence of the piezoelectric polarization on the alloy can be approximated by the following quadratic equation [32]:

$$P_{pz\ Al_xGa_{1-x}N/GaN}(x) = -0.0525x + 0.0282x(1-x)\ C/m^2 \qquad (14)$$

I.5.1.b Spontaneous polarization

Due to the Wurtzite structure along which epitaxial films and AlGaN/GaN heterostructures are grown, the spontaneous polarization is in the c-axis of the crystal following the equation:

$$\overrightarrow{P_{sp}} = P_{sp}\vec{z} \qquad (15)$$

They mainly exist in the GaN layer where the effect is generated from the nitride to the gallium, noted P_{sp} and given by the Aluminium concentration as follows:

$$P_{spAl_xGa_{1-x}N}(x) = -0.052x - 0.029\ C/m^2 \qquad (16)$$

It is noticed that the P_{sp} in the GaN layer is equal to -0.029 C/m².

The spontaneous polarization is independent of the electric field and of the stress, and it is due to the polar bond between the gallium and the nitride. When the non-ideality of the structure increases the spontaneous polarization increases.

Table I-6 synthesizes the calculated piezoelectrical and spontaneous polarisation constants for different III-N technologies and **Figure I-12** shows the piezoelectrical and spontaneous polarizations for an AlGaN/GaN alloy. The polarizations are in the reverse directions to the c-axis (0001) structure and due to lattice mismatch between the GaN and the AlGaN, another piezoelectric polarization could be established at the AlGaN/GaN interface. For a flat interface, the fix carrier density is given by [32]:

$$\sigma_{interface}(x) = P_{SP\ GaN} - \left(P_{sp\ Al_xGa_{1-x}N} + P_{pz\ Al_xGa_{1-x}N}\right) \quad (17)$$

	AlN	GaN	InN
e31 (Cm-²)	-0.58	-0.49	-0.57
e33 (Cm-²)	1.55	0.73	0.97

Table I-6. Pizoelectrical and spontaneous polarization constant for different III-N technologies [33].

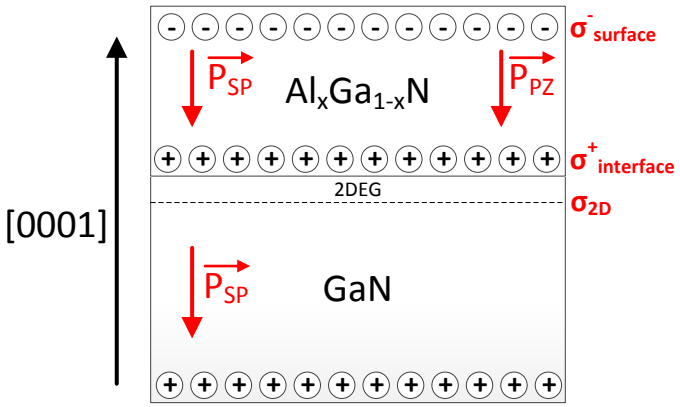


Figure I-12. Example of Piezoelectrical and spontaneous polarization in the AlGaN and the GaN layers (N ended).

Equations (18), (19) and (20) show the relation between the piezoelectric and spontaneous polarizations with the threshold voltage, the carrier density and the drain current respectively:

$$V_{th} = \frac{\phi_B - \Delta E_c}{q} - \frac{\sigma_{p1} - \sigma_{p2}}{C_1} + \frac{C_2 \phi_B}{C_1 q} \quad (18)$$

$$\boldsymbol{n_s = \frac{\varepsilon_1}{q(d+\Delta d)} (V_{GS} - V_{th} - V(l))} \quad \textbf{(19)}$$

$$\boldsymbol{I_{DS} = W_G q v_{sat} n_s} \quad \textbf{(20)}$$

where $\boldsymbol{\sigma}_{P1}$ and $\boldsymbol{\sigma}_{P2}$ are the strain tensors, C1 and C2 are the elastic constants and d is the thickness of the layer [28]. Moreover, these polarizations could also affect the sheet resistance of the AlGaN and GaN layers. Equation (21) shows the relation between the mobility (affected by the carrier density) and the sheet resistance:

$$R_{sh} = \frac{1}{q\mu_e N_D (W_{ch} - W_d)} \quad (21)$$

where $\boldsymbol{\mu}_e$ is the electron mobility, W_{ch} is the thickness of the active channel and W_d is the thickness of the depletion layer. The impact of the polarization on these parameters will also change the carrier

density in the channel (as it depends on V_{th}) and the subsequent drain value I_{DS}. Taking into account these effects for evaluating the evolutions of the I_{DS}-V_{GS} or g_m-V_{GS} plots is then necessary.

I.5.2 Thermal management

The operating channel temperature is one of the main device reliability indicators for AlGaN/GaN HEMTs. Therefore, it is of great importance to determine the channel conductivity and the maximum operating temperature for transistors dissipating large amount of thermal energy [34].

The channel temperature of a device is modeled by its thermal resistance for packaged transistors. Prejs *et al*. [34] developed a dual-mannered model for thermal resistance determination by using of Infrared microscopy and finite element analysis from which θ_{jc} (junction to case thermal resistance) can be calculated using the following equation:

$$\theta_{jc} = \frac{T_j(channel\ temperature) - T_c(case\ temperature)}{Dissipated\ power} \qquad (22)$$

And in its simplest form can be presented as the sum of a series of component resistance as shown below:

$$\theta_{jc} = \theta_{die} + \theta_{die\ attach} + \theta_{package} \qquad (23)$$

Using these values in a casual way to determine thermal resistance in scenarios other than how they were measured will lead to erroneous results [34]. Moreover, according to the complexity of the packaging and die design (multifinger power die), the model of the thermal resistance can be much more complex since every element in the system is contributing to the overall heat flow (multi stage serial resistors cells). The conventional thermal management technique is presented in **Figure I-13** extracted from [35] and shows the main elements that contribute to the heat flow. According to Laskar *et al.* [35] the heat spreads from the device channel, vertically through the layers.

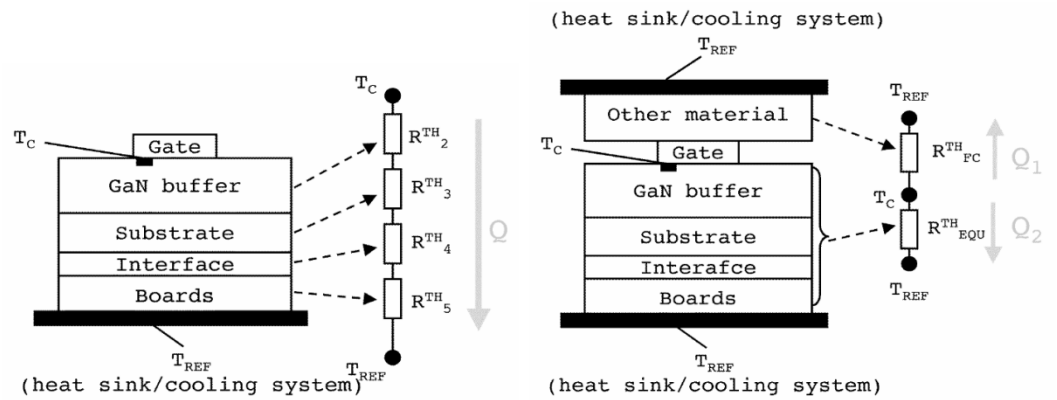


Figure I-13. Conventional and flip-chip representations of the channel temperature. [35]

In a conventional configuration the channel temperature can be approximated by [35]:

$$T_C = Q \sum R_i^{TH} + T_{REF} \qquad (24)$$

And, in a flip-chip configuration, it can be approximated by [35]:

$$T_C = Q_1 R_{FC}^{TH} + T_{REF} = Q_2 R_{EQU}^{TH} + T_{REF} \qquad (25)$$

where R_i^{TH} is the thermal resistance associated to each layer, T_{REF} is the reference temperature fixed by the environment or a cooling system, T_C is the channel temperature, and Q_i represents the heat flow from the device channel to the reference temperature [35]. This representation does not account for the dynamic time of heating establishment in the different layers (thermal capacitances). This will be discussed in chapters 2 and 3 related to the measurements experimental setups and to the interpretation of pulsed transient, low frequency noise, and packaged devices measurements.

Under high power conditions, thermal effects induce a drop in the carrier mobility, and thus reduction of device performances, as well as its reliability and lifetime. According to Laskar *et al.* [35], a lot of parameters impact the transistor channel temperature such as the substrate thickness, as well as the device geometrical parameters (number of fingers, gate pitch…) and the PAE in circuit design because it controls the total power to dissipate in the device when designing the power amplifiers (PA).

Figure I-14 shows the channel temperature versus the power density of 3 different HEMTs (GaAs on Si, GaN on Si and GaN on SiC). It is noticeable that GaN on SiC HEMTs provide the best channel temperature even at high power densities in comparison with GaAs on Si and GaN on Si HEMTs.

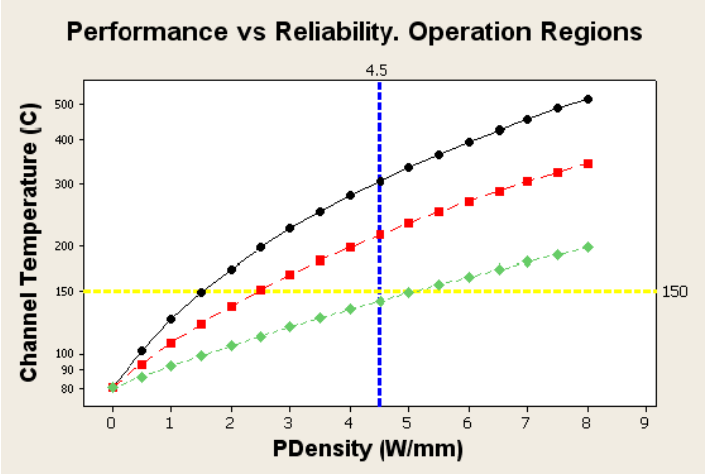


Figure I-14. Channel temperature versus power density of three different HEMTs: GaAs on Si (in black), GaN on Si (in red) and GaN on SiC (in green). [36]

I.6 Stresses

I.6.1 Arrhenius accelerated lifetime testing

Since a product lifetime is very long under normal operating conditions, therefore it is of great interest to develop accelerated life tests. Under these conditions, an artificial stress can be performed on devices that accelerate their time to failure. Arrhenius reported in 1887 about a lifetime testing based on Eq. 26 [29]:

$$R(T) = Aexp\left(-\frac{E_a}{kT}\right) \quad (26)$$

where R is the reaction rate, T is the temperature, A is a constant, E_a is an activation energy and k is Boltzmann's constant. The equation shows that the product lifetime is proportional to the inverse of

the reaction rate. Each life test yield to a failure rate λ as expressed in Eq. 27 showing the relationship between failure rate and the Khi^2 distribution:

$$\lambda = \frac{\chi^2}{2.TDH.AF,} \qquad (27)$$

where TDH is the "Total Device Hours" of the test and AF is an acceleration factor, both of them can be expressed as follows:

$$TDH = N \times H \qquad (28)$$

and

$$AF = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{op}} - \frac{1}{T_{stress}}\right)\right] \qquad (29)$$

where N is the number of units being tested, H is the hours they are subjected to the test, T_{op} is the operating temperature and T_{stress} is the elevated stress temperature used in the accelerated life test. The lifetime of a device is determined as a function of the stress parameter (temperature). Each activation energy is the parameter that provides the information on each failure mechanism on the device by solving a sequence of equation-tests performed at two different temperatures following these equations:

For the first temperature T1: $\ln(t_{f1}) = C + \frac{E_a}{kT_1}$ (30)

For the second temperature T2: $\ln(t_{f2}) = C + \frac{E_a}{kT_2}$ (31)

The activation energy can be written as: $E_a = [k\frac{\ln(t_{f1}) - \ln(t_{f2})}{\frac{1}{T_1} - \frac{1}{T_2}}]$ (32)

where t_{f1} and t_{f2} are the time to failure at T_1 and T_2 corresponding temperatures respectively [7]. This is valuable if considering a single failure with activation energy E_a. Then the temperature range of the study (and then the time to degradation) must be chosen to evidence realistic failure modes for a given set of applications (other techniques can be used, as proposed in the next chapter, to extract activation energies). Indeed, at least 3 temperatures are needed to assess for the accelerated dependence of the degradation (to reveal the linear trend related to the mathematical expression), and to extract the related activation energy. Moreover, the temperature range should not be too much elevated, as different activation energies can be evidenced in comparison with the activation energy that should be revealed by the investigation at lower temperatures (in spite of a longer time until the degradation occurs).

I.6.2 DC stresses

For lifetime testing, other types of stresses may be also applied such as the DC stresses. They are also temperature dependent stresses where the resultant parameter is also activation energy. We distinguish three types of DC stresses usually used for lifetime testing.

I.6.2.a High Temperature Reverse Bias (HTRB) stress

Where the device is biased under "off-state" conditions with high V_{DS} (closer to $V_{DS\,max}$) and with pinched-off channel ($V_{GS}<V_{th}$). The high junction temperature is followed by high temperature on the device. The junction temperature can be extracted using the following stress condition's equation:

$$T_j = T_a + R_{th} \times P_R \qquad (33)$$

where T_j is the junction temperature, T_a is the room temperature, R_{th} is the thermal resistance of the junction at room temperature and P_R is the dissipated power on the gate access ($P_R=|V_{GS}|\times I_G$ usually low enough to be considered as null). This stress intends to validate the robustness of the Schottky contact under high electric field. The biasing conditions are: V_{DS}=50V, V_{GS}=-7V (deeply pinched off) at 175°C. If after several hours (usually 2000 hours) no drift of the Schottky contact and of the DC parameters of the device are reported, then the test is considered as successful [37].

I.6.2.b High Temperature Operating Life (HTOL) stress

This stress is performed at room temperature and the thermal stresses are exhibited through high drain-to-source voltages (V_{DS}) at V_{GS}=0V (open channel). The junction temperature varies following the current rate in the channel. During this stress, the DC and RF characterizations are performed after 48h, 96h, 192h, 450h, 1000h, 2000h, 3000h, etc. The failure mechanism is related to the drain current run-away which consists in a loss of the drain current control as illustrated in **Figure I-15** (extracted from [37]).

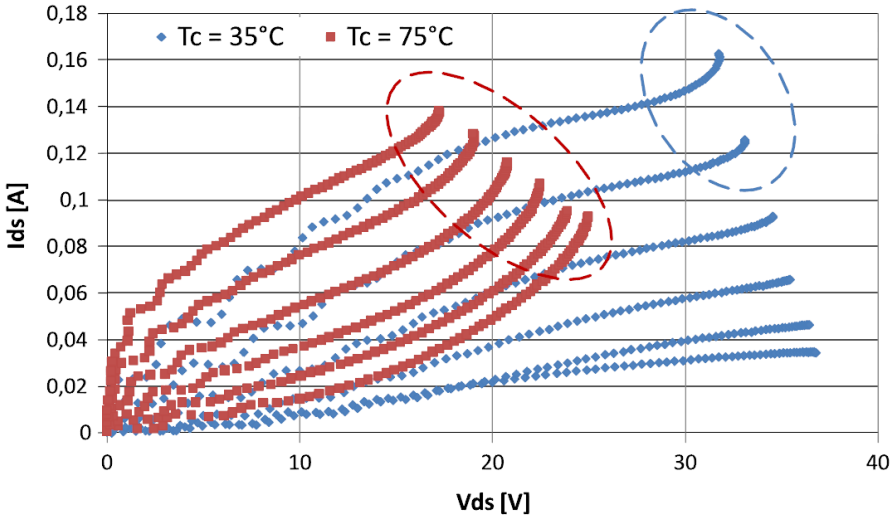


Figure I-15. Output characteristics measured by means of a curve tracer at different temperatures for a device exhibiting a runaway mechanism (ellipse area). [37]

I.6.2.c IDQ stress

This stress is also applied at room temperature at constant I_{DS} with an average value of V_{DS} where the gate-to-source voltage (V_{GS}) is dependent of the drain current needed to apply the stress. The result is an average junction temperature. Less degradation can be observed within the IDQ stress in comparison with HTRB and HTOL stresses.

Table I-7 - extracted from [37] - presents an example of qualification test plan of UMS (our manufacturer) that consists of a set of ageing tests and it covers environmental tests, Safe Operating Area definition, including recommended Operating Rating (OR) and Absolute Maximum Rating (AMR) as well as the assessment of wear-out mechanisms [37].

Test	DUT	Conditions	Test type	Duration
Storage	Wafer	250, 300°C	Diffusion	2000 h
TC	RIC	-65, +125°C	CTE	500 cycles
THB	RIC	85°C, 85%	Humidity	1000 h
DCSST	DEC	50V + n × 5V	AMR	1st failure
RFSST	DEC	50V + n × 5V, PAE_{max}+N × 1 dBm	AMR	1^{st} failure
HTRB	DEC	100V, -7V, 175°C	Schottky	2000 h
HTOL	DEC	50V, 3 temp	Wear out	70% failure
DCLT-1	DEC	50V, 250°C	MTTF	>2000 h
DCLT-2	RIC	50V, 200°C	MTTF	2000 h
RFLT-1	DEC	50V, PAE_{max}	MTTF	2000 h
RFLT-2	RIC	50V, PAE_{max}	MTTF	1000 h
VSWR	RIC	50V, |3|,|5|,|10|	Robustness	All phases

Table I-7. GH50-10 qualification test plan. [37]

I.6.2.d Step stress

The step stress is a non-thermal stress (performed at room temperature) where the parameters inducing the stress are the voltage, current or RF power variations. The purpose of this stress is to identify the Absolute Maximum Rating (AMR) [37]. This type of stress can be performed monotonically with a recovery time. **Figure I-16** extracted from [38] shows examples of devices degrading rapidly or gradually during step-stressing action. An example of step stress test is proposed in **Figure I-17** from [37] by our manufacturer UMS [8], on a devices stepping the compression level as PAE_{max}, PAE_{max+1} dBm and PAE_{max+2} dBm. After each compression cycle, V_{DS} is increased by a step of 5V starting from 50V. Failures occurred at the step V_{DS}=60V and PAE_{max+2} dBm (as shown in **Figure I-17**). Hence, the AMR of this technology is fixed today at V_{DS}=60V and PAE_{max+1} dBm. Nevertheless failures occurred for conditions where the device was not sufficiently matched, and they are attributed to an excessive induced junction temperature [37].

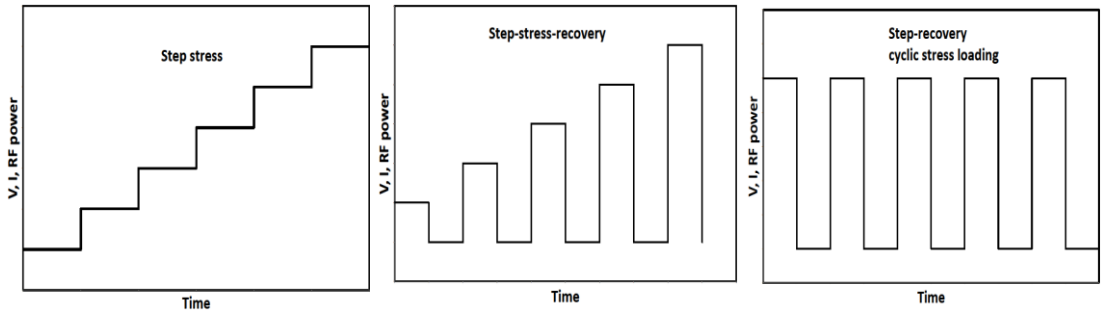


Figure I-16. Examples of typical time dependence of stressing protocols [38] (stresses performed to control jamming (electronic warfare) or radar overshooting).

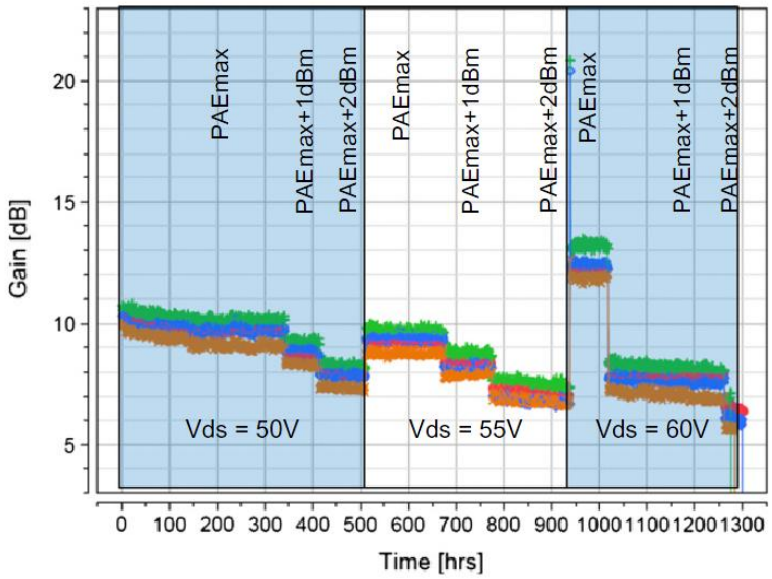


Figure I-17. RF gain monitored during RFSST test. Pin is set such as the device was operating at the maximum PAE, PAEmax+1 dBm and PAEmax+2 dBm. Starting from V_{DS}=50V, after each compression cycle, the V_{DS} is step up by 5V. [37]

I.7 Reliability of GaN devices

In the first stages of GaN reliability studies, researches have been driven using the same procedures and roadmaps for GaAs technologies. However, till the middle of 2005, lots of peculiar degradation behavior could not be interpreted using established theories. Then, GaN technologies have been considered in a much more realistic context considering all the potential effects and their interactions. But everything was to be developed (experimental tools for destructive and non-destructive analysis to be matched, theories to be gathered, etc.). This stands as the starting point for the ReAGaN project, involving different partners with specific expertise in the many areas of interest.

We distinguish two types of failures: Catastrophic (destructive or permanent degradation) and recoverable degradation.

Moreover, the Mean Time To Failure (MTTF) in any device is important reliability indicator. It is carried out on *n* devices that fail at several operating times t_n. The Mean Time To Failure is given by Eq. 34 [42]:

$$MTTF = \frac{t_1+t_2+t_3+\cdots+t_n}{n} \qquad (34)$$

The experimental techniques to determine the MTTF are more rigorous and give accurate information rather than the theoretical techniques. Great values of 10^7h of MTTF have been reported at junction temperature below 200°C, with activation energies ranging from 0.18 to 2 eV, but without taking into account the high electric field and current when determining the device lifetime. **Table I-8** [43] synthesizes the MTTF of GaN HEMTs from different manufacturers. As for our manufacturer (UMS), **Figure I-18** (extracted from [37]) shows the Arrhenius plot of devices submitted to an HTOL stress test. A MTTF of 3×10^7 hours is observed for a junction temperature of 175°C with associated

activation energy of 1.82 eV. These results demonstrate the high reliability level of this technology [37], even if some specific phenomena can still be extracted to enhance the overall reliability.

Manufacturer	Substrate	Gate length (L_G in µm)	Junction temperature (T_j in °C)	Mean Time To Failure (MTTF in hours)
Triquint	Si (111)	0.25	200	10^7
			225	10^6
Cree	4H-SiC	0.4	225	5.10^6
		1	175	10^9
			225	10^7
RFMD	4H-SiC	0.5 – 1	200	2.10^7
Nitronex	Si	0.5 – 1	160	10^7
			180	10^6
			200	10^5
Fujitsu	SiC	0.3	200	10^6
		0.8	200	10^7
UMS	SiC	0.25 and 0.5	200	10^6
M/A-COMSiC	-	-	200	10^6
NXP	SiC	-	-	10^6

Table I-8. MTTF of GaN HEMTs from different manufacturers. [43]

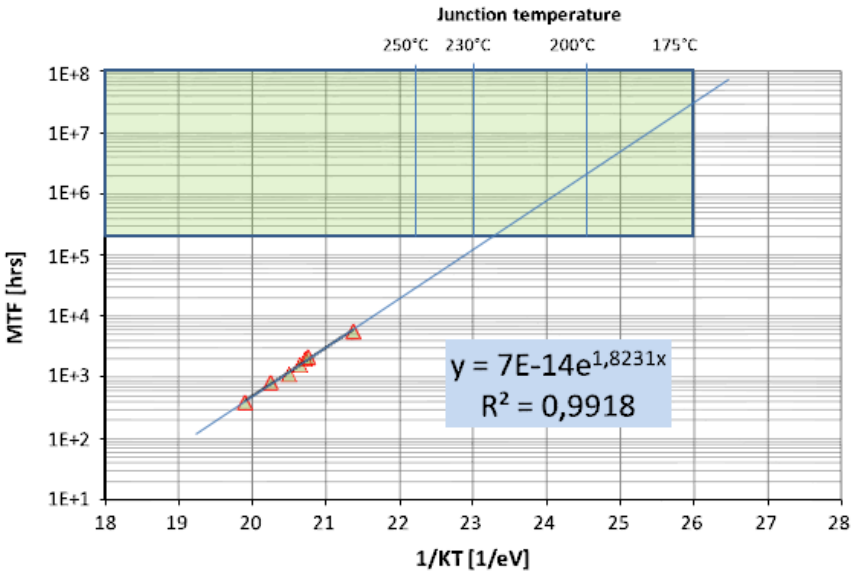


Figure I-18. MTTF versus temperature. HTOL test performed at V_{DS}=50V and I_{DS}=100 mA/mm. [37]

According to Schroder, the failure rate is sometimes represented by the bathtub curve as shown in **Figure I-19** [42]. Known as Infant Mortality, during the early life, the failure rate is high and they can be eliminated by burn-in. The next region corresponds to the useful life of the device showing a constant failure rate. At the end, the failure rate increases due to Wearout mechanisms.

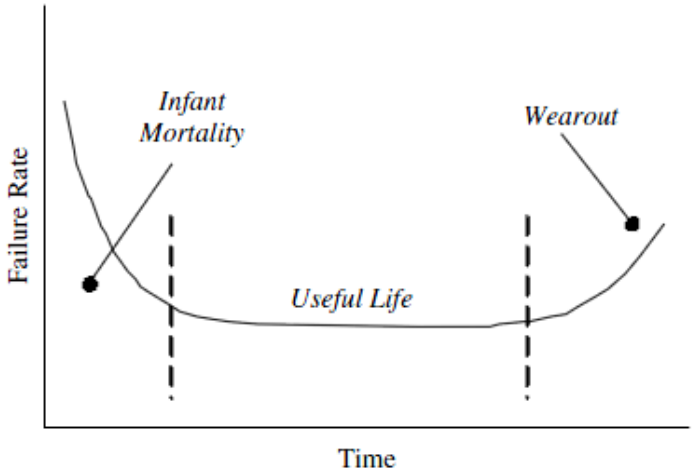


Figure I-19. Reliability bathtub curve showing early, intermediate and final failure. [42]

Various failure mechanisms can reduce the reliability and the MTTF such as the small distance between the channel and the gate (for high transconductance), this may cause surface effects. Also, surface damages caused by wet etching are employed to reduce R_{DS}. The high electric field at the drain end of the gate (for high power amplification and hence high drain voltages). Other failure mechanisms also may contribute such as piezoelectric effects, hot electrons trapping in the GaN buffer layer or on the surface (main cause of for gate and drain lag), metal-semiconductor interface and AlGaN/GaN heterointerface inhomogeneities, mechanical stress, humidity may cause corrosion... Some of these failure mechanisms are discussed in the next paragraph. Moreover, some reliability issues are technological, during the fabrication process, and could be controlled or replaced: the use of Ga-faced buffer is better than N-faced buffer for higher 2DEG concentration; the replacement of Pt-based Schottky contacts by WSiN-based contacts can stand as a beneficial solution for high temperature applications (>300°C) to avoid “gate sinking” [22], but this solution is not yet developed by the GaN industry; Moreover, WSiN contacts can generate leakage paths [40].

Failure analyses are carried out in many stages. The first step is usually the visual inspection of the devices and the electrical characterization. Then, to locate the defects, the optical techniques are essential like electron beams (for example the EBIC technique), optical beams (for example the OBIRCh technique), emission microscopy, deep level traps analysis (for example C-DLTS and I-DLTS), etc. Since, all these techniques are non-destructive; noise characterization and electrical analysis versus temperature variations performed next are also of great importance as they reveal the electrical (macro or micro) signature induced by defects before and after the stress period(s).

There is always a reliability study even for commercial devices, hence it is well known that the reliability process is very complex, as well as it is difficult to announce a completely reliable device, and thus the reliability can be never completely understood. Several complex and robust experimental procedures and original characterization techniques (starting with non-destructive techniques then destructive ones) are required to set “reliable” information under the adequate operating conditions of the device, and the subsequent lifetime.

I.8 Degradation mechanisms and reliability concerns

We distinguish two types of failures: Catastrophic failures and monotonic degradation. **Figure I-20** illustrates the interconnection between electrical, thermal and mechanical behaviors. The figure shows the multiple interactions: electrical, mechanical and thermal. All these phenomena are forward, reverse and complementary to each other showing how tricky can be the interconnected phenomena and the resulting degradation under operating mode of the device. The transport mechanism and the carrier distribution induce a thermal effect on the layers and create a mechanical distortion due to the electric field. This mechanical distortion can also be result from a self-heating of the device under test. Moreover, the strain and the thermal transport induce piezoelectric and thermal effects that lead to the generation of traps and defects on the drain current. These electro-thermo-mechanical interconnections are complicated, and their mastering is not really essential to optimize a technology at T_0. However, when it comes to the control of the performance's evolution of a device (during or after the application of a stress), it is essential to control these interactions in order to provide more robust and reliable technology.

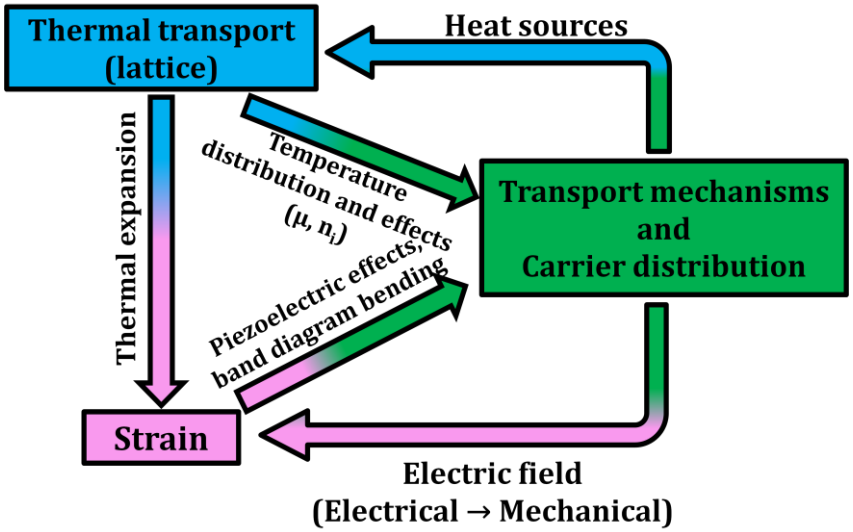


Figure I-20. Interconnection between electrical, thermal and mechanical behaviors [43].

I.8.1 Electromigration (EM)

Electromigration (EM) failures are evidenced by an increase in the line resistance, by a line becoming short or open circuit or by an adjacent lines becoming short-circuited. The voids can be observed at one end of a line and hillocks at the other end as illustrated in **Figure I-21** (extracted from [42]). Their size, of approximately 100 nm, depends on the processing stage. Because of these voids, the line is considered under mechanical stress due to thermal and lattice mismatch. Passivating such lines increases the EM resistance, by introducing additional stress. Cracks are formed as shown in **Figure I-22** [42] by heavy lines leading to an open circuit and the metal diffusion occurs primarily through vacancies.

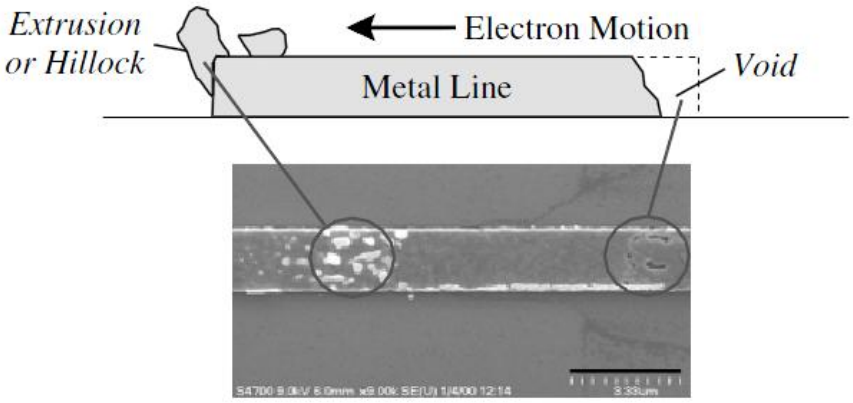


Figure I-21. Void and hillock formation in an Ag line stressed with J=23 MA/cm² at T=160°C. [42]

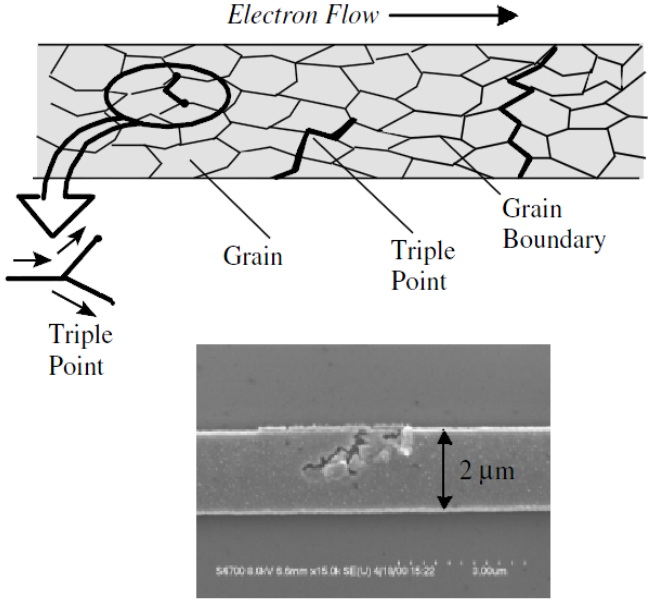


Figure I-22. Schematic of a polycrystalline line containing grains, grain boundaries and triple points. The SEM micrograph shows a propagating crack. [42]

Today's most dominant metal failure mechanism is the contact EM, but depending on the type of the contact. **Figure I-23(a)** [42] shows two Al lines connected by a tungsten (W) plug. Since the migration in the W plug is negligible, the electrons flowing from M2 to M1 will develop a void under the W plug in the M1 metal [42]. **Figure I-23(b)** [44] and **Figure I-23(c)** [45] show examples of contact EM.

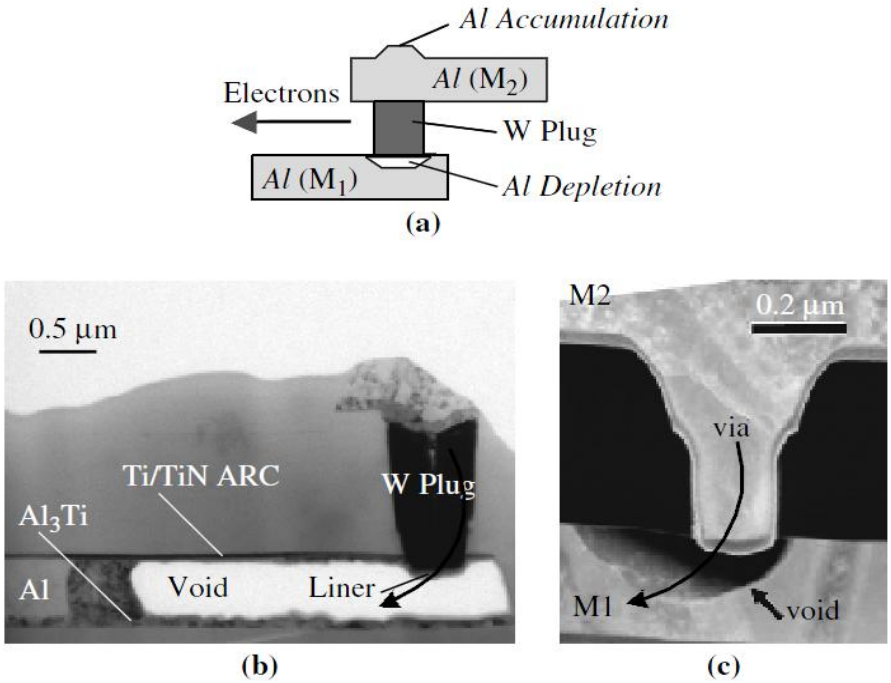


Figure I-23. Contact electromigration (a) schematic showing void development under the W plug with electrons flowing from M2 to M1 [42]; TEM cross-sections showing the void in (b) Al [44] and (c) Cu [45] lines. The arrows indicate the electron flow.

After testing metal lines at different temperatures for a given current density, a log-normal distribution is required to study the EM failure data. The MTTF is then plotted versus 1/T (for example **Figure I-24**) and the activation energy is extracted.

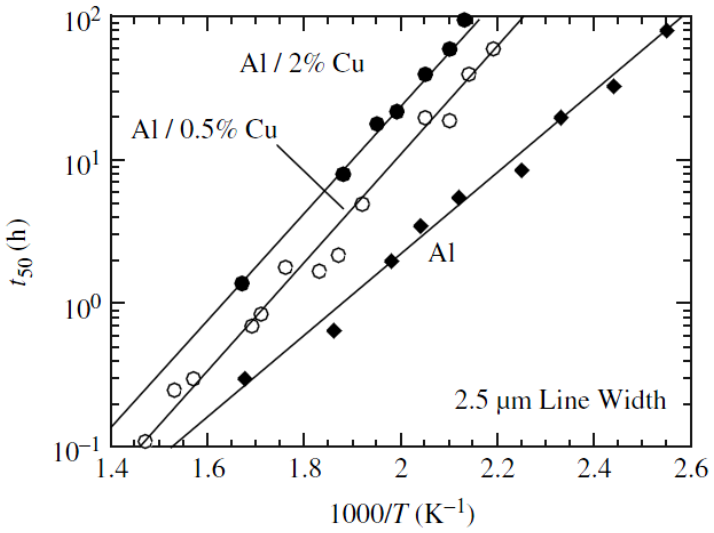


Figure I-24. Activation energy determination of electromigration data. [42]

I.8.2 Piezoelectrical degradation

The high electric fields applied between source and drain terminals and gate and drain terminals are the origin of the mechanical stress that may lead to the presence of piezoelectrical effects. V_{DS} creates piezoelectrical effects in the AlGaN layer. Moreover, AlGaN and GaN layers are intrinsically piezoelectric layers; this may result of significant tensile strains even with absence of any electric field. Moreover, these strains can change considering the thermal variations during the fabrications

processes of the devices. Gate and drain currents degradations occurs at V_{DG}>20V [38] [46] [47]. This critical voltage presents the maximum voltage before the degradation of the device.

The critical voltage varies from V_{DG}=15V to V_{DG}=30V, this variation is attributed to changes in the fabrication process (Al content, layers thickness…) [48] [49]. The piezoelectrical degradation depends of the Al concentration in the layers, thus for our devices from UMS, this concentration being very low leads to higher critical voltages than 30V.

Chowdhury *et al.* [50] studied TEM cross section on 20 AlGaN/GaN HEMTs to evidence the inverse piezoelectric effects at three different junction temperatures of 250°C, 285°C and 320°C. TEM analyses reveal that virgin devices did not show any type of defects. In the other hand, 18 stressed devices showed several types of degradations:

- Pit-like defects are observed in the AlGaN under the drain located 10 nm distant from the surface of the SC (**Figure I-25(a)**).
- Crack shaped defects are also observed for a stress time of 6h at a channel temperature of 320°C (**Figure I-25(b)** and **Figure I-26**).
- Gate metal diffusion of around 2nm is noticed into the defect crack in the SC (**Figure I-25(c)**).

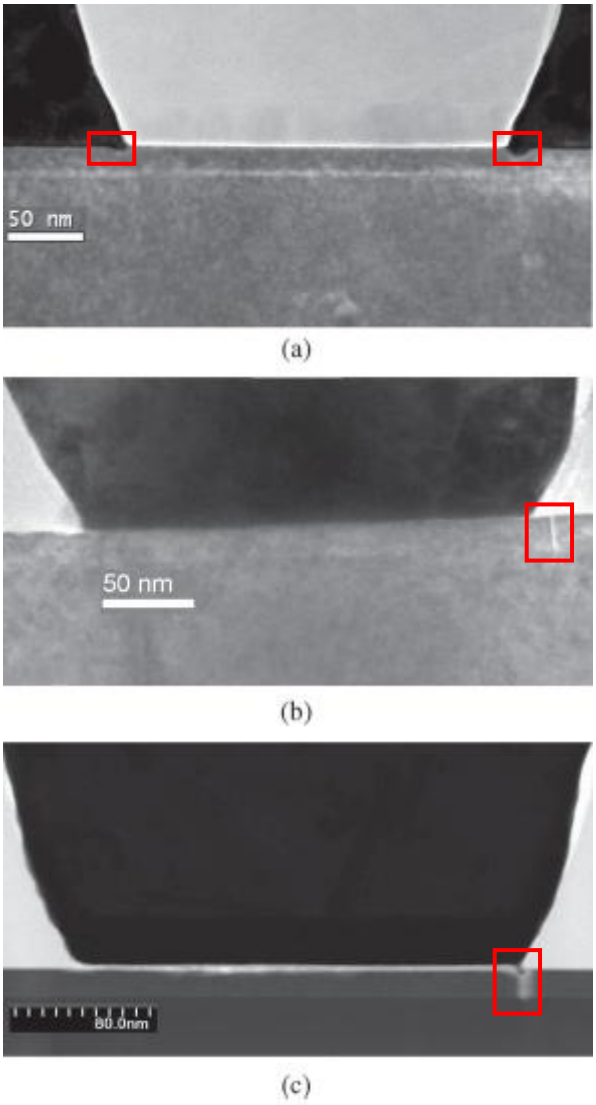


Figure I-25. Three examples of stressed devices showing the semiconductor (below the horizontal interface) and he gate metal. [50]
(a) Formation of pits on both source- and drain-side edges of the gate
(b) Formation of a crack
(c) Severe case of degradation where the gate metal (Pt) has diffused into the formed crack.

Non-uniform strain could also be detected due to SiN passivation. Mastro *et al.* [51] have reported simulation results of non-uniform strain due to SiN passivation where PECVD SiN_x films tend to become compressive on the AlGaN. To reduce the compressive stress, some solutions were proposed such as running the PECVD process at relatively high pressure (≤2 Torr). According to Mastro *et al*. [51] the gate length and the magnitude of the strain due to passivation process are inversely proportional (important result for high power passivated devices with small dimensions).

I.8.3 Hot carriers and trapping/detrapping effects

Hot carriers (electrons or holes) are energetic carriers dependent from the temperature and the energy where they are related through the expression E=kT [42]. Mostly, the hot carriers are located on the surface or in the substrate:

I.8.3.a Surface traps

Passivation of the surface is the well-known first solution to reduce surface traps. The surface is usually passivated with Silicium Nitride (SiN) but other passivation layers are also available such as SiO_2, Al_2O_3, Gd_2O_3, AlN and GaN (**Figure I-26**).

Device with and without Si_3N_4 passivation layers are studied in [52], the results show an activation energy of 1.43eV for the unpassivated device. Also, more pronounced gate lag effects are observed on unpassivated devices in comparison with SiN passivated devices [53]. However, gate lag effects could exist on passivated devices after being stressed under high electric field conditions [54] [55].

I.8.3.b Substrate traps

Substrate traps or self-backgating traps or drain lag are activated in the GaN buffer layer between the source and the drain due to the application of V_{DS} voltages. The crystal impurities or defects (under high electric field) generate trap states that can be recombined with carriers from the 2DEG, or can change the intrinsic voltage between gate and source (and thus modify the carrier density in the 2DEG). These traps affect the drain current. Without electric field, the electrons cross the barrier of the substrate into the channel where they are trapped by donor states. Other electrons are then released by the free donor states. Hence, the number of the captured electrons is equal to the number of trapped electrons. The electrons are then injected from the channel into the substrate where they are trapped by ionized states. The upper part of the GaN layer closer to the channel is then negatively charged, thus a positively charged region appears at the channel-substrate interface for equilibrium. The charged area in the substrate is then considered as virtual gate (**Figure I-26**) modulating the carriers in the channel (self-backgating). [56] [57]

I.8.4 Metallurgical degradation and interface inhomogeneities

The metallurgical degradation mechanisms are related to high temperature conditions. It is mainly observed on the sinking of the Schottky and Ohmic contacts (**Figure I-25(c)** and **Figure I-26**). As for the Schottky contacts, it is well known as “gate sinking”. These degradations result a modification of the pinch-off voltage, a reduction of the drain current and trapping-detrapping effects on the surface and in the AlGaN layer. These also lead to HF degradations and consequently to the destruction of the device and the breakdown of the gate contact. As for the AlGaN/GaN heterointerface and the metal-semiconductor interface inhomogeneities, there are experimental and theoretical techniques to track and control them. In the present work, the Schottky barrier height inhomogeneities are discussed.

I.8.5 Electrostatic Discharge (ESD)

Electrostatic discharge is the transient discharge of static charge due to human handling, contact with equipment, automated test or handling systems [42]. The device is charged during transport or contact with that highly charged surface or material and it remains charged until contacting the ground; then the device is discharged through it pins. According to Schroder [42], the three ESD

mechanism models are the Human Body Model (HBM), the Machine Model (MM) and the Charged Device Model (CDM). HBM and MM are quiet similar since they are different forms of the same discharge mechanism and different from CDM ESD type.

This paragraph evoked the degradation mechanisms of AlGaN/GaN HEMTs under stress or high electric field conditions. Many factors such as elevated temperatures, high electric field are shown that create sudden and/or permanent degradations. **Figure I-26** shows a schematic cross section of the devices under test with the main degradation mechanisms and their localization in the body of the device. Several failure analysis characterization techniques exist to understand the underlying mechanisms of the device degradation such as: the EMission MIcroscopy (EMMI), InfraRed Thermography (IRT), Optical Beam Induced Resistance Change (OBIRCh), Low Frequency Noise (LFN), etc. The next chapters focus on the failure analysis techniques performed on our devices and the associated results.

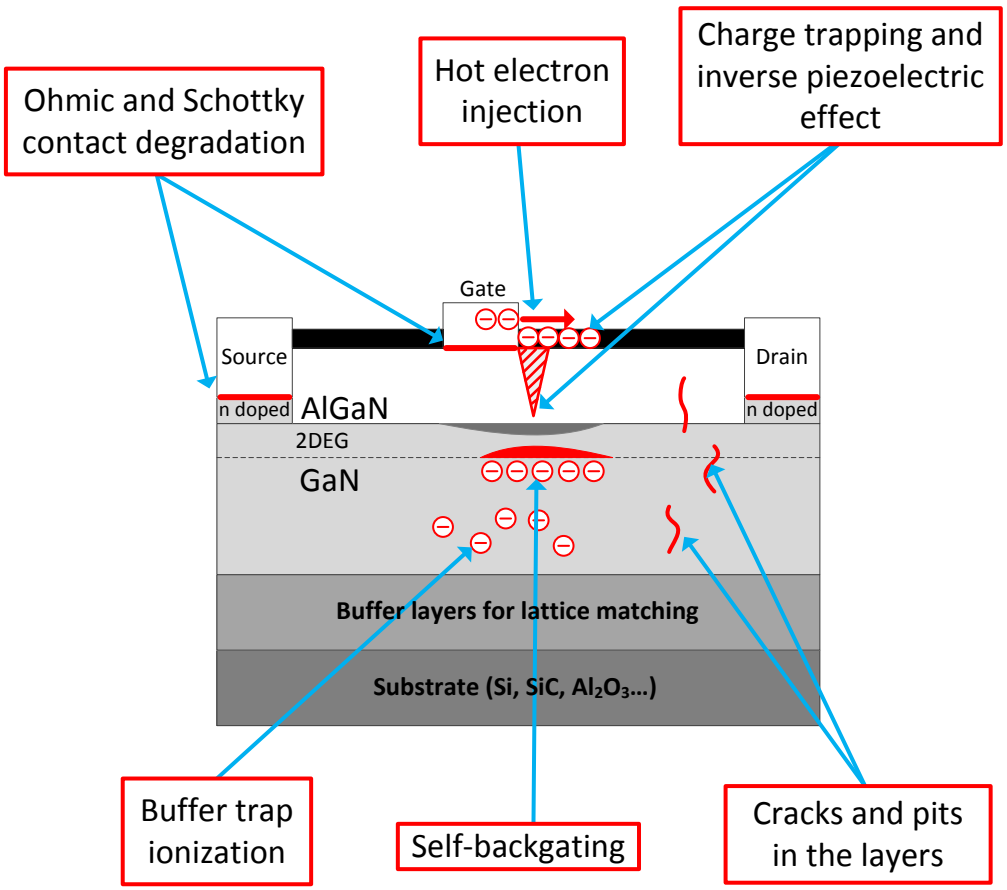


Figure I-26. Localization of the degradation mechanisms in AlGaN/GaN HEMTs

I.9 Conclusions

AlGaN/GaN HEMTs are enlarging their application area but they still need a reliability improvement to address new markets or to reach high level of reliability states. This chapter presents an overview of the GaN based HEMTs, that under intense research is showing promising results for

high power, high frequency and high temperature applications in comparison with competitive solid state technologies. These qualities set the GaN HEMTs as alternative solution for high power applications below the C band, in the X band and above; hence, more efficiency can be observed in the GaN based power amplifiers than the GaAs, with promising results for long term operations.

With all these qualities stated above, it is important to highlight on the fact that these technology is not yet completely mature. The degradation mechanisms (presented in the last part of the chapter) are the main study cases for these devices. Several degradation mechanisms limit its operation conditions like the electromigration, the hot carriers, the piezoelectrical degradation, etc. These mechanisms creating defects in the device can be optically observed as well as electrically. The correlation between these two types of detections is very difficult, since the electrically activated defect and the defect observed using optical techniques could not be the same. Hence, reliability issues are still a questionable parameter. Sudden and permanent degradation mechanisms stand as limiting candidate for this technology to dominate the market and shift in device performance. The following manuscript, in the next chapters, discusses investigation techniques to point out the main underlying mechanisms of degradation.

I.10 References

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Chapter II:

DESIGN OF EXPERIMENTS AND CHARACTERIZATION PROCEDURES FOR PHYSICAL AND ELECTRICAL ANALYSIS AT THE DEVICE SCALE

II.1 Introduction

As the reliability study of GaN HEMT devices is the heart of the project related to this thesis document, the objectives are twofold:

The partners have to propose a set of different multi-physics efficient experimental tools to get information about the main parameters leading to the degradation of the devices.

The consortium has to confront the different set of measurements, with the goal of defining a design of experiment on these technologies, but also for their following declinations.

The design of experiment (DOE) consists in systematically and efficiently experiment on a process for determining the principal degradation cause. Then the next step is to find solutions to solve the reliability problems, as well as avoiding the creation of new ones; there will always have degradation mechanisms, but then the boundaries using conditions of these technologies will be extended. The roadmap of the project related to this work has been first defined at the project submission stage, and more or less regularly refined according to the study cases that priority must be given to or according to the efficiency of new sets of experiments that have been experienced on these technologies. Then the most important variables in the degradation process and their interaction will be identified. The best experimental sets and methods will be determined to get those parameters. This represents a challenging program because of the high level of complexity when it comes to GaN technologies (electro-mechanico-thermal interactions, experimentally evidenced but rarely or hardly modeled).

Next are described the ReAGaN project we have been involved in, and the partners contribution to the project. Then the experimental tools developed or used within the project by LAAS partner are presented. The results issued from the measurements are exploited in chapter 3: in this last chapter, a first DOE at this state of progress of the project is proposed.

II.2 ReAGaN project: description, scientific and technical objectives

This thesis is carried out as part of the ReAGaN project (Reliability Analysis of GaN Devices) [1] funded by the ANR (*Agence National de la Recherche*) [2] and in collaboration with six partners from France and with the French DoD:

- United Monolithic Semiconductors (UMS) from Villebon sur Yvette, France.
- Thales Research and Technology (TRT) from Palaiseau, France.
- IMS - CNRS from Talence, France.
- LEPMI from Saint-Martin d'Heres, France.
- Serma technologies from Grenoble, France.
- LAAS - CNRS from Toulouse, France.

Even if not officially identified as a partner of the ReAGaN project, the *Délégation Générale de l'Armement* (*DGA*, French DoD) from Rennes, France is also involved in the project. Their contribution to the project helps to ensure the success of the proposed strategy with providing a special knowledge about the different ongoing and finalized projects as well as keeping an overall view on the GaN French and European development roadmap.

The project addresses the reliability of the GaN technology in its industrialisation phase (UMS foundry). The introduction of GaN technologies into market required highly reliable devices associated with high performances. Both aspects meant a deep understanding of the physical and electrical behaviour of the device.

The main objective of the project is the development of advanced electro-optical and physical characterisation techniques dedicated to wide bandgap semiconductor technologies. For the first time, new analysis techniques are developed and their results are correlated leading to the identification and characterisation of nano-structural defects and physical mechanisms taking place in GaN technologies and potentially responsible for degradation.

The complementarities between techniques are demonstrated as a proof of the existing interaction between electrical transport properties, light characteristic and material atomic structure. From concept or laboratories expertise, some techniques like TEM-CBED, RAMAN analysis, UV microscopy… demonstrate applications at industrial level. Then efficient electrical and physical analysis tool boxes are a major outcome of the project.

As the stake, techniques are developed in parallel of the GaN technologies maturation and of the needs at UMS. While the techniques development are fed by devices from reliability life tests and from different processing options, by technological information, and by technical objectives (bottleneck), analysis undertaken along the project produce results with two main objectives described in **Figure II-1**.

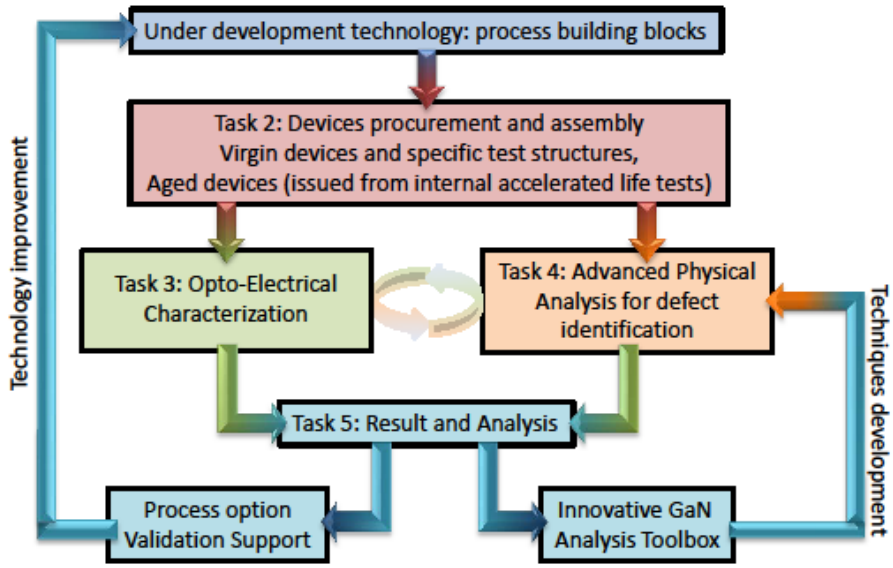


Figure II-1. Schematic illustration showing the structure of the project and the tasks. [1]

The failure analysis aims through the identification of failure root cause at supporting the determination and characterisation of degradation mechanisms of the GH50 technologies under development at UMS (cf. Chapter 1 for failure analysis).

The comparative analysis of different processing steps provides important and pertinent information to support the step-up of the GH50 technology from one generation to the next one.

This ambitious project aims to support European GaN process industrialization at UMS by developing failure analysis tool and methodology dedicated to such technology. This project focuses on the study of parasitic effects and degradation mechanisms affecting GaN technologies. It aims to reduce the time to market of these technologies by building fundamental knowledge for GaN technology improvement.

The project structure presented in **Figure II-1** is directly correlated to the development, evaluation and qualification of two GaN processes developed at UMS and supported by various international programs as previously mentioned (Chapter 1). Then it is divided into five tasks as follows:

- Task 1: Project Management
- Task 2: Devices procurement and assembly
- Task 3: Opto-electrical characterization
- Task 4: Advanced physical analysis for defect identification
- Task 5: Result analysis: support to process option validation and definition of innovative GaN analysis toolbox.

The **1st task** is dedicated to the project management and involves all the partners. Task 1 is regularly discussed (every 6 months during progress meetings) according to the obtained results and to the objectives to be reached (additional measurements under specific conditions).

The **2nd task** consists in providing both specific virgin structures, and packaged reference and aged devices, to partners for both opto-electrical analysis and physical analysis.

The **3rd task** is focused on an exhaustive characterisation of parasitic physical phenomena by means of complementary electrical and opto-electrical techniques to identify the degradation modes of the different technology variants under investigation. These studies are split between LAAS and IMS partners for electrical and noise analysis, each responsible for a specific set of measurements. A close interaction is maintained between the two laboratories, and preliminary DC-pulsed measurements have been determined on the same devices to calibrate the electrical workbenches (and to ensure the cross analysis for the study). The optical analyses are performed by TRT III-V lab. The management of the studies (device procurement and exchange between partners) depends on the exploitation of the research results and of the hypothesis to evaluate. A reactive feedback is expected for the success of this task, as an input for the next steps of the project.

Electrical characterisation (IMS and LAAS)

An extensive DC electrical characterisation is performed on reference devices to analyse the dispersion of the I-V characteristics as well as on the sets of aged devices.

DC and pulsed I(V) measurements are carried out. For instance, the pulsed measurements allow to evidence and to study the physical origin of the drop of the drain current which can be related to trap effects located either under the gate (gate lag) or in the gate-drain spacing (drain lag), or at the interface layers below the 2DEG channel. The trapping phenomena involve in particular a drop of the microwave power and of the device efficiency compared to the expected values.

Thermal analysis and optical characterization versus bias and temperature (TRT)

Information on the device temperature is crucial since it affects their performance and reliability. Although electrical methods can be used to estimate the device temperature, only a spatially averaged temperature over the entire device is determined. IR thermography is used for temperature cartography in the active area of the device and hot spot localisation. To get the required spatial resolution, Raman analysis is undertaken for the determination of the maximum junction temperature.

Concerning the opto-electrical measurements, we focus on emission microscopy technique and electrical characterisation under monochromatic illumination. In this project, the visible-near IR domain is investigated for the characterization of the Schottky contact and of the passivation layers.

Time domain characterization versus temperature (LAAS and IMS)

The purpose of this task is the characterisation of electrical anomalies occurring in GaN HEMTs. The parasitic effects are electrical anomalies which penalize the initial potential performances of the devices. The physical origin of these effects is directly associated with the intrinsic structure of the device and/or with anomalies induced by the technological process.

Lag effects are studied versus time rise, fall settling measurements on the gate and drain terminals. Temperature is also used as a variable parameter to assess the dependence of these phenomena on the carrier conduction mode.

RF measurements are performed at different input power levels: small signal parameters are related to the behaviour of the device for linear applications. The dispersion of the low frequency transconductance $g_m(f)$ versus frequency and of the output conductance $g_d(f)$ as well as drain current transients measurements are studied to complete the interpretations from pulsed electrical measurements. These frequency dispersions effects can also be related to trapping-detrapping processes also visible by low frequency noise measurements on a different range of frequency (from 1 Hz to 1 MHz for low frequency noise characterization; from 100kHz to 4 GHz [or 40 GHz using two Vector Network Analysers] for S-parameters and frequency dispersion). Moreover, a DLTS measurement allows tracking deep traps and providing directly their activation energy and capture cross section to correlate with LFN results.

Low frequency noise (LFN) measurements are carried out to characterize the fabrication processes as the LF noise reflects the transport properties of carriers and is also very sensitive to the presence of crystal defects in active layers and semiconductor interfaces. Consequently, it will be useful to evaluate the maturity of the GaN technologies under test. Cross comparisons between different processes can also be helpful to discriminate the technological key parameters impacting the reliability improvement of the HEMT devices.

While LF drain current noise is essentially used to evidence defects on the carrier's path between drain and source (Ohmic contact resistances, 2DEG channel, bulk layers and interfaces, passivation efficiency, etc.), LF gate current noise reflects fluctuations of leakage current's carrier properties from/to the gate terminal. These two noises can be more or less partially correlated when gate leakage currents are very elevated [3], or not correlated for improved technological processes (i.e. mastered level of leakage current). Drain LFN measurements allows to track the evolution of the drain to source defects during the application of a stress (impact of the biasing, temperature, RF signal or also modification induced by the gate terminal Schottky deterioration), while gate LFN is used to provide information about the defects on the gate terminal (that tunes the command of the device) and about the possible evolution and consequence of these defects after a stress period.

This study is conducted on AlGaN/GaN HEMTs with different gate geometries and includes:

Low frequency drain current noise measurements in Ohmic and saturated regions. Ohmic region: the extraction of the Hooge parameter from experimental data allows comparing the technologies under test with other GaN HEMT technologies [4]. Saturated region: the noise sources contributors (1/f, generation-recombination centers) are tracked versus different biasing V_{DS}, V_{DG} and V_{GS} conditions to determine the location/nature of the defects [5].

Low frequency gate current noise measurements are performed on the diode (under open drain configuration) and on the transistor (under saturated biasing conditions). This study is one of the key-points of the project as the gate related phenomena are expected to be first order parameters leading the degradation mechanisms.

The **4th task** is dedicated to the physical analysis of specific structures (reference and aged HEMTs).

Defect localisation and characterisation (SERMA, LEPMI and TRT)

LEPMI uses RS and Raman imaging to examine aged and failed devices. Any difference in the observed signals is related to the presence of structural defects in the aged samples.

SERMA proposed destructive physical analysis like standard TEM. When the defect localisation has been performed by TRT, the standard TEM analysis implemented by SERMA includes structural and/or chemical analysis.

We have gathered in **Table II-1** a presentation of non destructive techniques, and their use for getting information on the degradation mode or its mechanism (concerning tasks 3 and 4). The significant techniques are compiled and included inside the innovative GaN analysis toolbox of Task 5.

Defect signatures	Non-destructive techniques	
	Task 3	Task 4
• Leakage current	• Electrical measurements (pulsed I-V-T)	• Hot spot localization by II/thermal mapping
• Self-heating effect	• Evolution of traps (Low Frequency Noise)	• Thermal mapping
• Schottky diode degradation	• Electrical characterisation versus temperature • Low frequency noise measurements on gate current	• Visible to Near IR • Emission microscopy
• Passivation defects	• Low frequency noise, transient I-V-T, DLTS	• Visible to Near IR emission microscopy • UHF Scanning acoustic microscopy
• High electric field localization • Hot carrier degradation		• UV emission microscopy and pulsed I-V
• Crystallographic defect		• Raman Imaging – low frequency noise

Table II-1. Defects signatures and associated techniques from tasks 3 and 4

From **Table II-1**, it can be noticed that most of the techniques from task 4 can also be correlated to techniques developed in task 3; but the expected results should reveal different trends as electrical and LF noise measurements only evidence active defects (i.e. defects that impact the carriers and /or the control of the device) while Raman or near IR emission spectroscopy provide an exhaustive mapping of the defects (some should be 'enabled', some are 'disabled' as they do not play a role in the device running mode). Lastly, if 'blind' electrical measurements are not easily exploitable because any spatial information is directly proposed, Raman and near IR emission spectroscopy propose a visual repartition of defects (statistical value of the defects, time evolution after the application of a stress). These techniques, even if not easy to cross, offer a chance to access to the deep underlying mechanisms responsible of the degradation of the devices.

The **5th task** review and correlate the analysis of results obtained from Tasks 3 and 4. It supports the optimization of technological processing bricks thanks to the results on manufacturing options performed by electrical and physical failure analysis experiments where failure modes and root causes are identified.

Its second objective is the definition of an adequate tool box for the improvement of the process and reliability of GaN technologies. The efficiency of this methodology is established as a large set of innovative electrical and physical techniques are investigated to face the difficulties encountered when failure root cause has to be linked to electrical failure mechanisms.

All the tasks presented above are subject to confidentiality to the project and cannot be developed more than that.

II.3 Experimental procedures developed in LAAS and dedicated to the reliability analysis

Firstly, as the set of devices under test are provided by UMS and successively sent to other partners, a quick control of the device integrity must be performed. This control consists of understanding the datasheet sent from our manufacturer (UMS) and in a visual verification of the devices. Then electrical measurements (DC) confirm the state of the transistors (output characteristics). Sometimes, these two controls are also performed at different moments of the characterization (for instance, between two LFN measurements campaigns a verification is important to check if any change occurred or not). For example, two sets of GH50 GaN devices issued from two different wafers have been tested at LAAS and IMS laboratories. Devices with single gate finger are measured presenting different interconnection patterns between the gate and the pad as shown in **Figure II-2**. This difference was provided in a datasheet by UMS when we received the devices and it allows organizing the measurements between those two types of transistors.

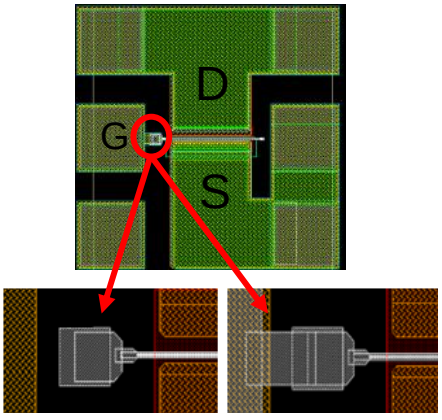
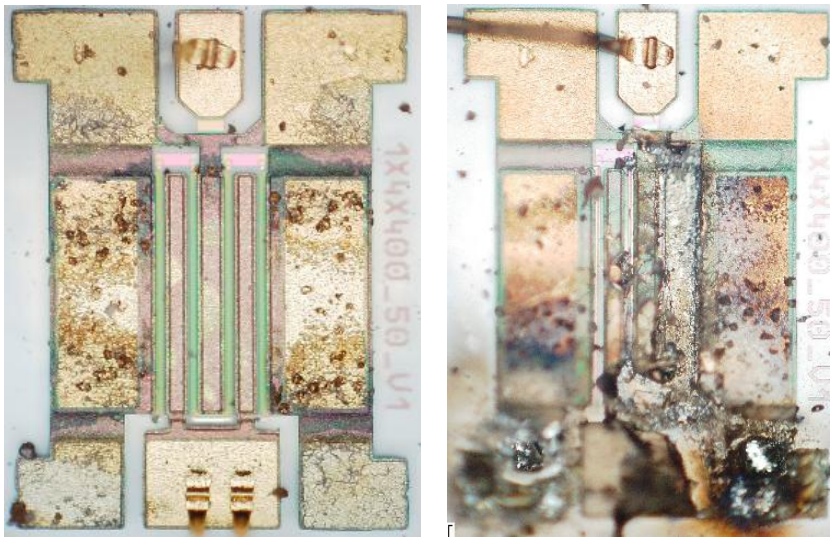


Figure II-2. GH50 AlGaN/GaN HEMTs with single gate finger. 2 types of devices are tested:
(a) Devices without interconnection between the gate and the pad.
(b) Devices with interconnection between the gate and the pad.

The second set of devices, also measured, features 4 gate fingers (4×400µm×0.5µm) and divided into 2 types: Non-leaky (NL) and leaky (L) devices, where the non-leaky devices are also measured

before and after application of HTOL (High Temperature Operating Life) stress for 10^4 hours at V_{DS}=50V and I_{DS} = 160mA (100mA/mm) @ 25°C. The preliminary test on the devices is – as usual – their visual observation in order to check the state of the device before the application of any biases (V_{GS} and/or V_{DS}). **Figure II-3** shows devices from the GH50 technology with 4 gate fingers: **Figure II-3(a)** (resp. **3(b)**) presents a functional (resp. failed) device after their visual observations. In brief, this first control allows to check if the technical specifications of UMS are (visually) in agreement with the received devices (cf. files of data and state, - test set details) and to avoid any misunderstanding concerning a possible error in their classification. Then electrical tests can be performed as detailed below.



(a) (b)

Figure II-3. Optical observation of GH50 AlGaN/GaN HEMTs (4*400µm*0.5µm).
(a) Functional device.
(b) Failed device.

II.3.1 Electrical DC and pulsed characterization (versus temperature)

The electrical characterization procedure is the easiest experimental bench and the most commonly available by most of the partners. The measurements are of two types (DC and pulsed). This technique provides a prior information about the self-heating of the device when we measure the drain current (I_D) versus V_{DS} and V_{GS}.

Furthermore, the gate current provides also important information about the gate leakage level and its conduction mechanisms.

In the present work, all the measurements are performed using Agilent 4156C precision semiconductor parameter analyzer.

II.3.1.a Gate current study

The quality of the Schottky barrier contact is only revealed by the measurements of the gate current (I_G) versus V_{GS} and V_{DS}. The Richardson plot brings information on the physical and electrical parameters of the Schottky diode such as the saturation current (I_S), the ideality factor (n), the Schottky barrier height (ϕ_B), the effective Richardson constant (A*) and the effective mass (m*).

The gate terminal can be biased under forward and reverse gate voltages. In this work, the Schottky parameters are studied under forward biasing conditions whereas the low frequency noise measurements are performed under both forward and reverse biasing conditions. Both studies and results are detailed in the next chapter.

In order to extract the physical parameters, a sweep in temperature is required when measuring the gate current (I_G) versus the gate-to-source voltage (V_{GS}). The equation of the current can be expressed as follows [6]:

$$I_G = I_S \left[exp\left(\frac{q(V_{GS} - I_G R_S)}{nkT} \right) - 1 \right] \qquad (1)$$

$$\text{and} \qquad I_S = S \times A^* \times T^2 exp\left(-\frac{q\varphi_B}{kT} \right) \qquad (2)$$

where I_S is the saturation current (in Ampere), R_S is the series resistance (in Ohm), S is the surface (in cm²), A* is the effective Richardson constant (in $A.cm^{-2}K^{-2}$), n is the ideality factor, k is Boltzmann's constant (in $m^2kg.s^{-2}K^{-1}$), T is the temperature (in K) and ϕ_B is the Schottky barrier height (in eV). **Figure II-4** shows an example of the static I_G-V_{GS} measurements versus temperature; the red arrows indicate the temperature increase.

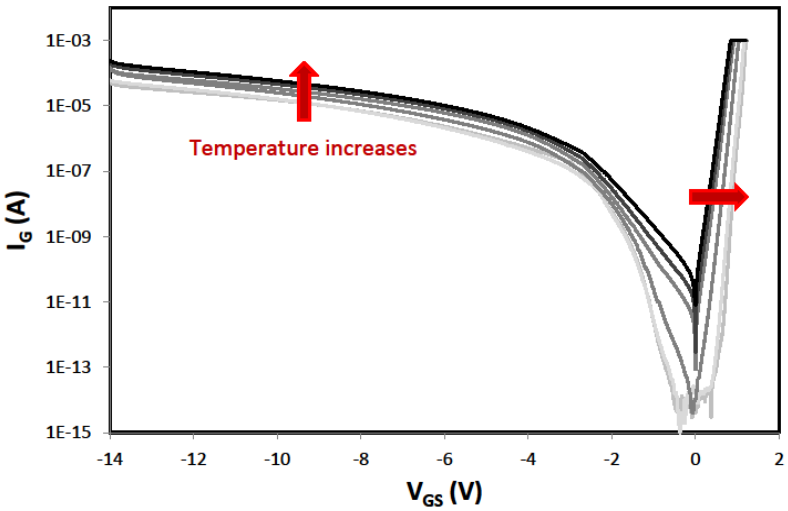


Figure II-4. Static $I_G(V_{GS})$ characteristics versus temperature featuring the current variations when the temperature increases (100K-400K).

The temperature sweep is performed on the "Cryoprober PMV200" from SUSS Microtec (**Figure II-5**). Depending on the necessary resolution, the DUT can be monitored with an Optem or Navitar microscope with color CCD camera. The probe system, as well as the device under test, is affected by static electricity: Agilent 4156C, so that the system should be installed in an area where the floor covering does not generate a static charge, or so the static can be discharged through static mats [7]. While mounting the devices into the Cryoprober, test measurements are carried out and should be identical to the measurements outside the Cryoprober at room temperature. The following test is performed before every measurement campaign.

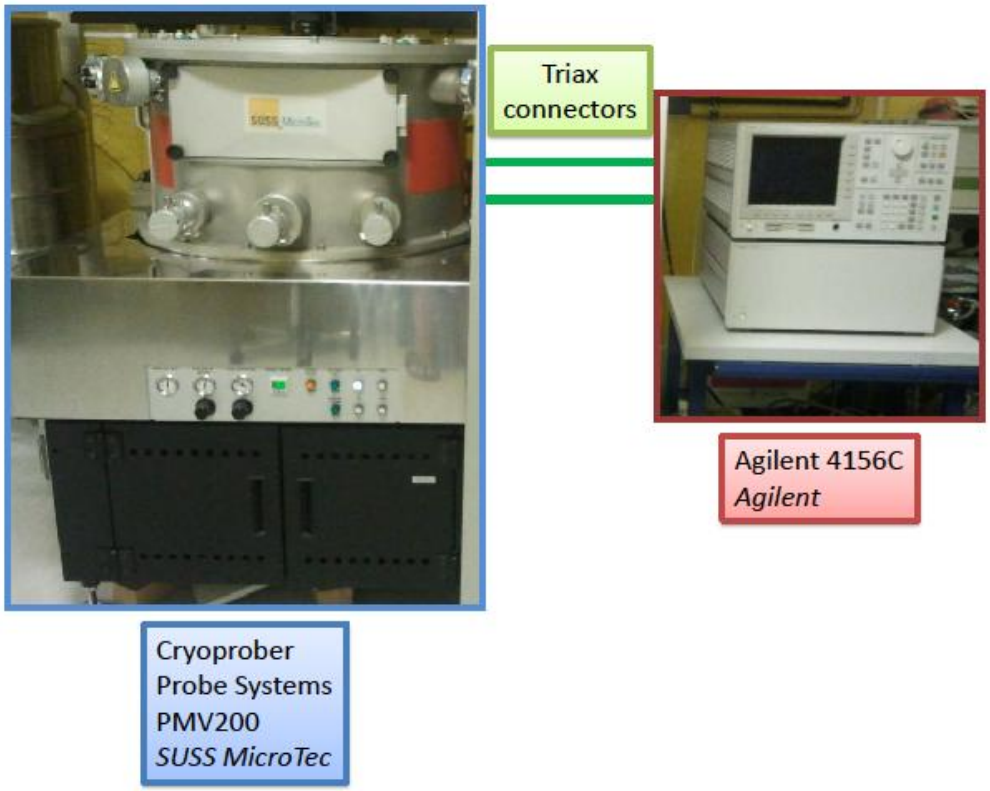
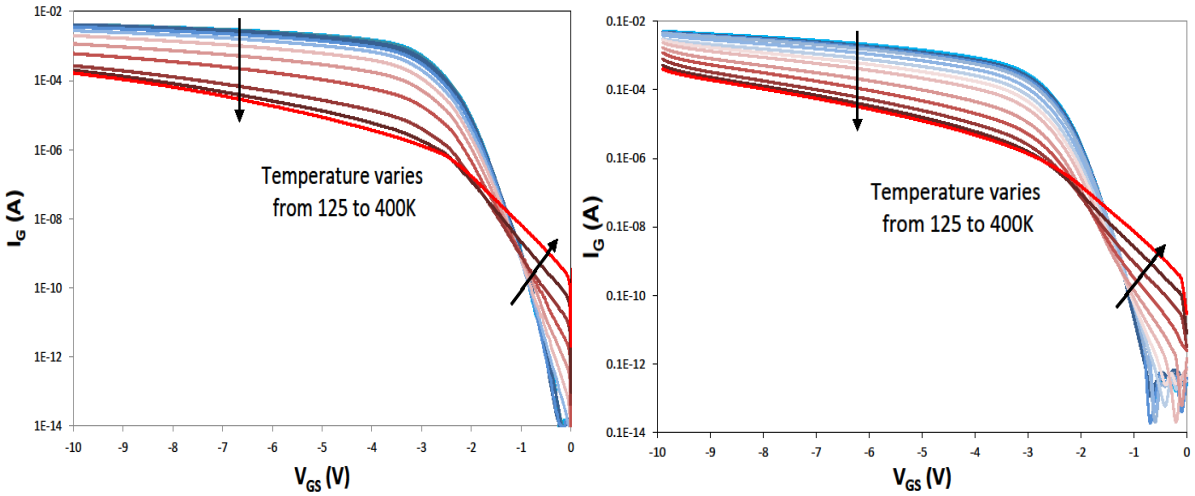


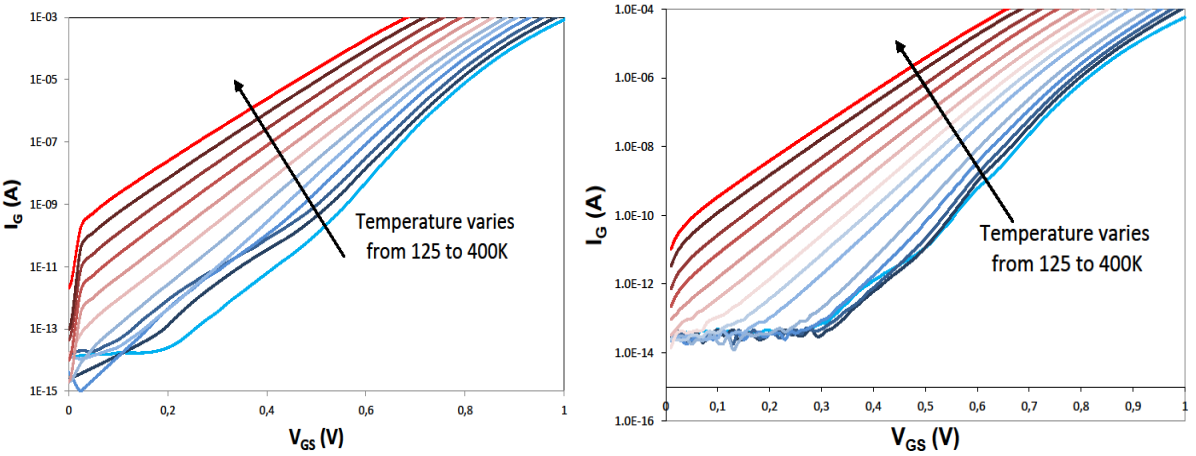
Figure II-5. Picture of the Cryoprober PMV200 (on the left) and of Agilent 4156C (on the right) used for thermal DC and pulsed characterizations of packaged and on-wafer AlGaN/GaN devices (stressed and virgin devices).

To validate the thermal crossed analysis between LAAS and IMS (performed on two different sets of devices), one reference device has been measured by the two laboratories under the same conditions (measurements performed at V_{GS} biasing from -10 to 1V (open drain) with temperature ranging from 125K to 400K. The results of the reverse and forward biases are shown in **Figure II-6** and **Figure II-7** respectively. It can be noticed that a good agreement is obtained and only the measurement floor (resolution) differs between these two sets of graphs. Some differences can however be observed for the low temperature ranges under forward biasing conditions, but these temperature ranges are usually out of range for the interpretations as it will be proposed in our model for the Schottky diode (cf. chapter 3).



(a) (b)

Figure II-6. Reverse I_G-V_{GS} measurements of GH50 AlGaN/GaN HEMTs (4*400µm*0.5µm).
(a) Measurements performed at LAAS-CNRS, Toulouse.
(b) Measurements performed at IMS, Bordeaux.



(a) (b)

Figure II-7. Forward I_G-V_{GS} measurements of GH50 AlGaN/GaN HEMTs (4*400µm*0.5µm).
(a) Measurements performed at LAAS-CNRS, Toulouse.
(b) Measurements performed at IMS, Bordeaux.

II.3.1.b Drain current study

- Static output characteristics $I_D(V_{DS}, V_{GS})$

The current is measured while a sweep in V_{DS} at constant V_{GS} is performed. Two main regions are distinguished in the $I_D(V_{DS}, V_{GS})$ measurements: the Ohmic region and the saturated region as shown in **Figure II-8**. As for the Ohmic region, the device behaves like a resistance and the R_{on} parameter can be extracted. The FETs are devices operating mainly under Ohmic region for controlled resistance applications. On the other hand, the saturated region is when the channel resistance is very high and the current cannot be affected by the variations of V_{DS}. Devices operating under saturated region are mainly used for the design of amplifiers.

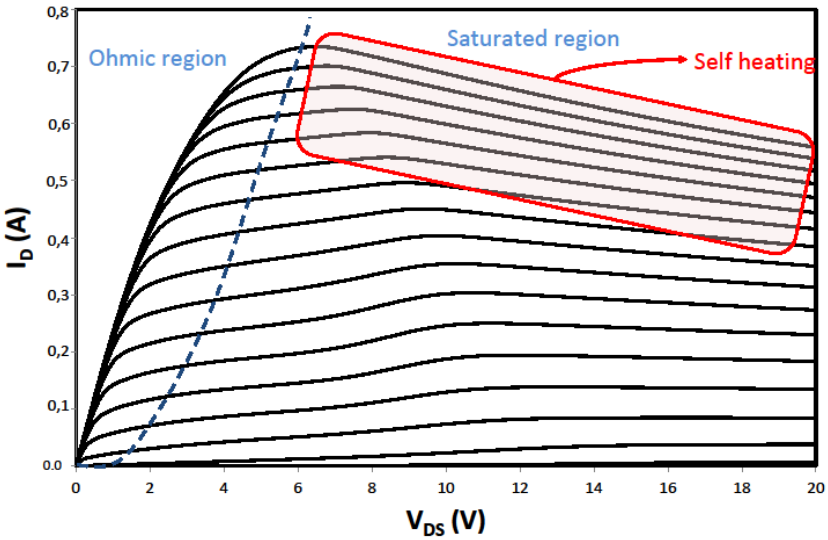


Figure II-8. Static $I_D(V_{DS}, V_{GS})$ output characteristics featuring the Ohmic and saturated regions, the knee voltage and the self-heating.

Pulsed measurements allows to determine the thermal contribution to the I_{DS} current drop, and allows to extract some lag effects according to the application of a drain to source voltage (drain lag) or to the application of gate to source voltage (gate lag). These lag effects are closely bind to the technological process, and accurate methods have been developed to identify where the active zones responsible of this lag are located [8, 9].

- Static $I_D(V_{GS})$

The $I_D(V_{GS})$ characteristics allow to extract the threshold voltage (V_{th}) as shown in **Figure II-9**. This parameter can be extracted using the tangent method, by plotting a tangent on the characteristic, the intersection point between the tangent and the x'x axis (V_{GS}) will be the threshold voltage.

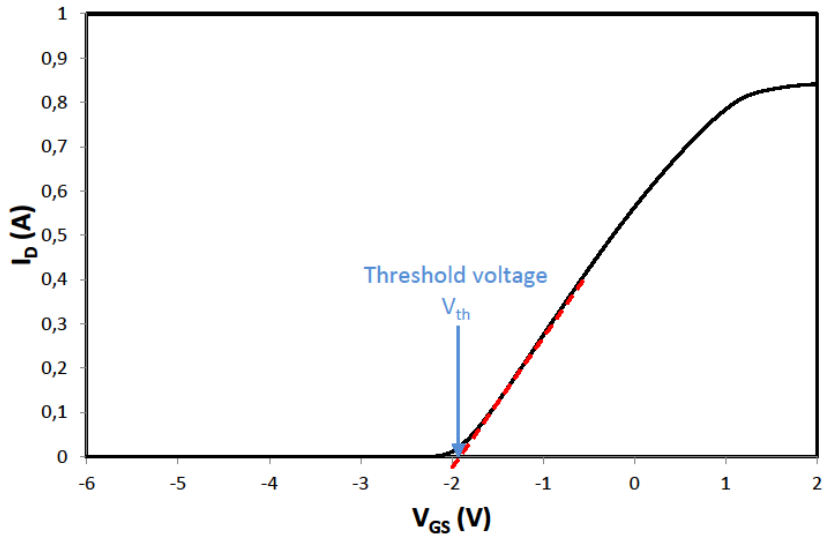


Figure II-9. Static $I_D(V_{GS})$ characteristic featuring the tangent method to extract the threshold voltage.

An accurate method can be used by exploiting LFN measurements [43], but this later is time consuming and must only be used when accurate appreciation is needed on this parameter knowledge (as shown in **Table II-2**). It consists in using the following mathematical expression:

$$V_{th} = \varphi_B - \frac{\Delta E_C}{q} - \frac{qNd}{q\varepsilon} \qquad (3)$$

Where ϕ_B is the barrier height, ΔE_C is the discontinuity in the conduction band, q is the electron charge and d and ε are the thickness and the permittivity of the AlGaN barrier layer. Moreover, these measurements allow extracting the small signal transconductance g_m at a given bias point (V_{GS0}, V_{DS0}).

Table II-2– extracted from [10] – shows the calculated values of V_T using two methods (LFN method and DC measurements) and on different substrates (Si and SiC). The differences on Si (3%) and SiC (6%) substrates are negligible.

	V_T (V) using LFN method	V_T (V) using DC measurements
Si	-3,4 V	-3,5 V
SiC	-4,7 V	-5,0 V

Table II-2. Extraction of the V_T voltage using electrical characteristics and LFN measurements. [10]

II.3.2 Pulsed time-domain measurements

Two different sets of measurements have been developed to discriminate between the evolutions of the drain current versus initial DC conditions (magnitude sensitivity of the lag effect, time evolution of the drain current). A procedure has been proposed to discriminate between possible simultaneous effects (thermal+drain lag and/or gate lag) [11]: for that purpose, it is possible to apply initial conditions where no thermal effects are dissipated (I_{DS}xV_{DS}=0 W), and investigate on specific lag effects (once with I_{DS}=0V, i.e. V_{GS}<$V_{pinchoff}$ for gate-lag effects, and once with V_{DS}=0V for drain-lag effects). An illustration of the time evolutions according to a step change in V_{DS} (drain-lag) is given in **Figure II-10**.

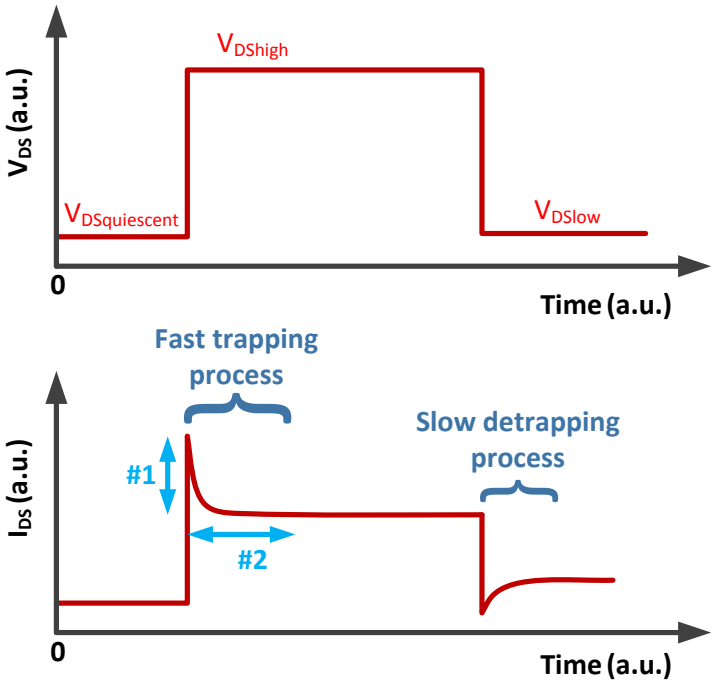


Figure II-10. Time dependence of the drain current I_{DS} versus the step variations of V_{DS}.

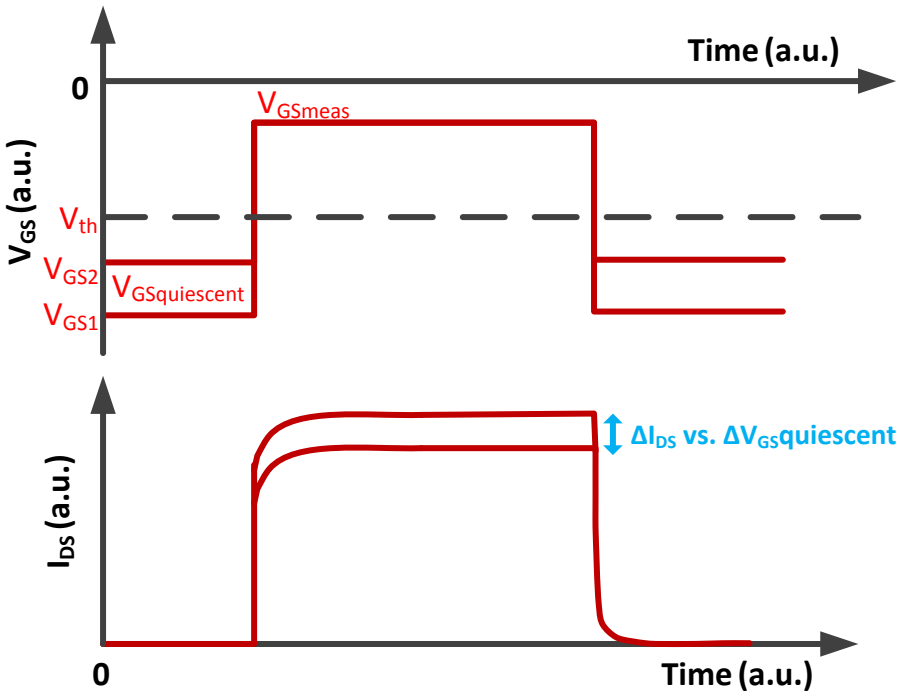


Figure II-11. Time dependence of the drain current I_{DS} versus the step variations of V_{GS}.

In this figure, #1 is the magnitude-evolution of I_{DS} versus initial quiescent conditions and can be investigated using short-pulse measurements (pulse duration t=0.1µs, no significant decrease on I_{DS}) [8, 12]. The time-evolution represented by #2 can be modeled using an analytical expression of the decrease of the drain current. The drain-lag effects are attributed to deep traps located beneath the channel; these traps create a space charge area that disturbs the pinching of the device by self-backgating mechanism (explained in the 1st chapter). The same procedure can be proposed for the drain current evolution versus V_{GS} (**Figure II-11**).

II.3.3 Low frequency noise measurement

A noise is a random fluctuation of a current or a voltage: different noise sources can contribute to the overall noise power spectral density. The noise can be expressed as a function of the current or voltage or power spectral densities. Therefore, the autocorrelation function of x(t) can be introduced as follows:

$$R_x(\tau) = \overline{x(t)x(t+\tau)} \qquad (4)$$

The spectral density of the x signal is defined as:

$$S(f) = 2\int_0^{+\infty} \overline{x(t)x(t+\tau)}\, cos2\pi f\tau\, d\tau \qquad (5)$$

The spectral density is two times the Fourier transformer of the autocorrelation function. The value of S(f) allows to extract the mean quadratic value of the signal between two frequencies f1 and f2 by:

$$\overline{i^2(t)} = \int_{f_1}^{f_2} S_i(f)\, df \qquad (6)$$

Hence, for small frequency ranges, it can be expressed as follows:

$$\overline{\imath^2(t)} = S_i(f).\Delta f \qquad (7)$$

II.3.3.a Noise sources involved in GaN HEMTs

Figure II-12 shows the noise equivalent circuit of the AlGaN/GaN HEMTs. Two main noise measurements can be performed on the device: the drain noise measured on the drain terminal and includes I_{RD}, I_{ch} and I_{RS} noise sources and the gate noise measurements carried out on the gate terminal, includes I_{GS} and I_{GD} noise sources. When the Schottky contact is of very good quality, the measurements of the gate noise are very sensitive due to the non-leaky behavior of the device.

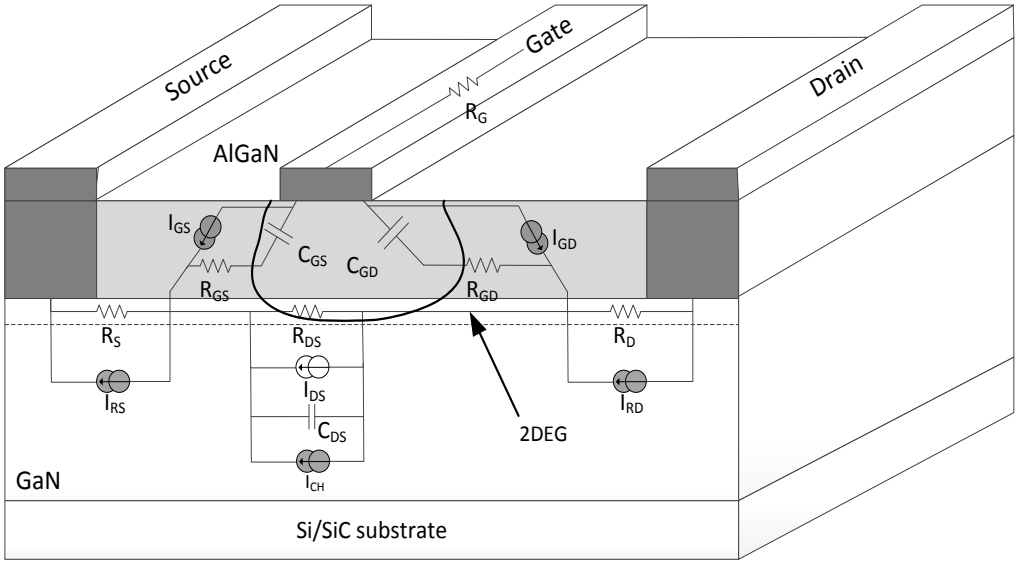


Figure II-12. Schematic illustration of the Low Noise equivalent circuit for the AlGaN/GaN HEMTs.

These noise sources can be interconnected in pairs by a coefficient called correlation coefficient. It can be evaluated by a post-treatment measurement of cross spectrum between the two given noise sources. If the coefficient is zero, then the two noise sources do not have any common origin and are considered as non-correlated. If the coefficient is one (upper limit), then the two noise sources are totally correlated and originate from the same phenomena. Some noise sources can be only partially correlated when the correlation coefficient is between 0 and 1.

The analysis of the measurements is very sensitive due to the variety of noise sources and their origins. Moreover, the device only features two external terminals to access to the noise information (added to this, the ground terminal); the overall noise spectral density can be the manifestation of several different noise sources, weighted according to their location in the device. The analysis of the noise spectral density requires an accurate mastering of the experimental workbench to avoid any misunderstanding about the measured noise contributors (device under test or measurement environment) and also a rigorous method or procedure to access to the singular contributors (noise source origin and location). The different noise contributions can be represented as proposed in **Figure II-13**; the interpretation of the noise spectral density on each gate and drain terminals

requires excellent background information on the likely present noise sources in a structure. Therefore, the extrinsic models proposed in the literature and shown in the **Figure II-13** cover different possibilities to measure the noise. It can be concluded from this figure that the parallel representation is convenient to represent the gate and source current fluctuations on the extrinsic terminals of our devices. However, if a partition is needed, only a voltage representation can allow separating the serial contributions into the device (from drain to source for example in **Figure II-12**, with serial contributions of the source and drain contact resistances, and of the channel (if the correlation coefficient is considered to be zero)

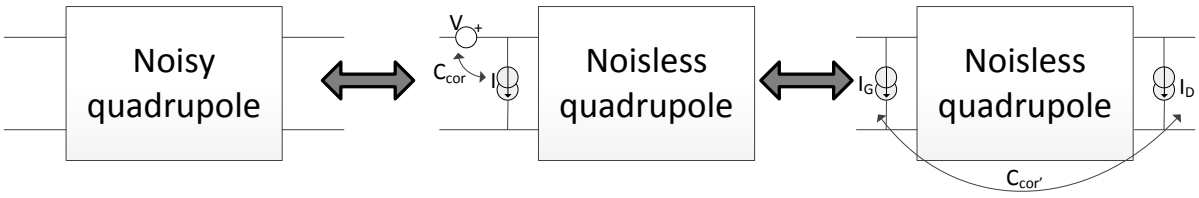


Figure II-13. Schematic illustration of the low frequency noise in quadruple.
(a) Noisy quadruple.
(b) Serial presentation.
(c) Parallel presentation (adopted model in the present work).

II.3.3.b Different noise sources

- Thermal noise: it originates from the spontaneous current or voltage fluctuations on a resistance. Thus, it is only resistance and temperature dependent and can be expressed as follows [13, 14]:

$$S_{V_{(T)}} = 4kTR \qquad (8)$$

$$\text{or } S_{I_{(T)}} = 4kT/R \qquad (9)$$

where k is Boltzmann's constant, T is the temperature and R is the resistance value. The noise measured in a frequency range Δf across a resistance is presented by the following noise spectral densities equations [13]:

$$\overline{v^2} = 4kTR\,\Delta f \qquad (10)$$

$$\text{and } \overline{i^2} = (4kT/R)\Delta f \qquad (11)$$

The thermal noise is found to be present in any resistor that shows dissipation when a current is passed through it [13].

- Shot noise: The origin of this noise is mainly related to the carrier fluctuations associated to an injection like that of the carriers crossing a potential barrier. Near the heterojunction of the HEMT device, the electrons flow on all over the heterojunction without crossing the barrier (lateral transport of the carriers in the 2DEG). Hence, the shot noise is negligible and does not exist on the drain current. However, near the Schottky contact, the leakage current tunnels through the barrier and generates a shot noise. Random generation leads to fluctuation around the average current value as follows [13]:

$S_I = 2qI$, and consequently on the gate current $S_{I_G} = 2qI_G$

- Generation-recombination noise: According to Hooge [46] the number of free electrons in the conduction band may fluctuate because of generation and recombination processes between the band and the traps. This noise source is characterized by its Lorentzian form due to trapping-detrapping effects in the semiconductor and can be expressed as:

$$S_{I_{(GR)}} = \frac{K}{1+\left(\frac{f}{f_c}\right)^2} \qquad (12)$$

where K is magnitude and f_c is the cutoff frequency associated to the relaxation time of the involved trap.

- Random Telegraph Signal (RTS) noise: known also as Random Telegraph Noise (RTN), burst noise or popcorn noise. This noise shows random switching of the current between two different states: high and low (as shown in **Figure II-14** [15]). The signal amplitude is presented versus the time variation and the RTN is characterized by three parameters: the up-time (t_u), the down-time (t_{do}) and the amplitude ΔI_D. As its name suggests, the time between switching processes is random. Moreover, the time necessary for switching between two processes is much shorter than the time interval during which the system remains in one state.

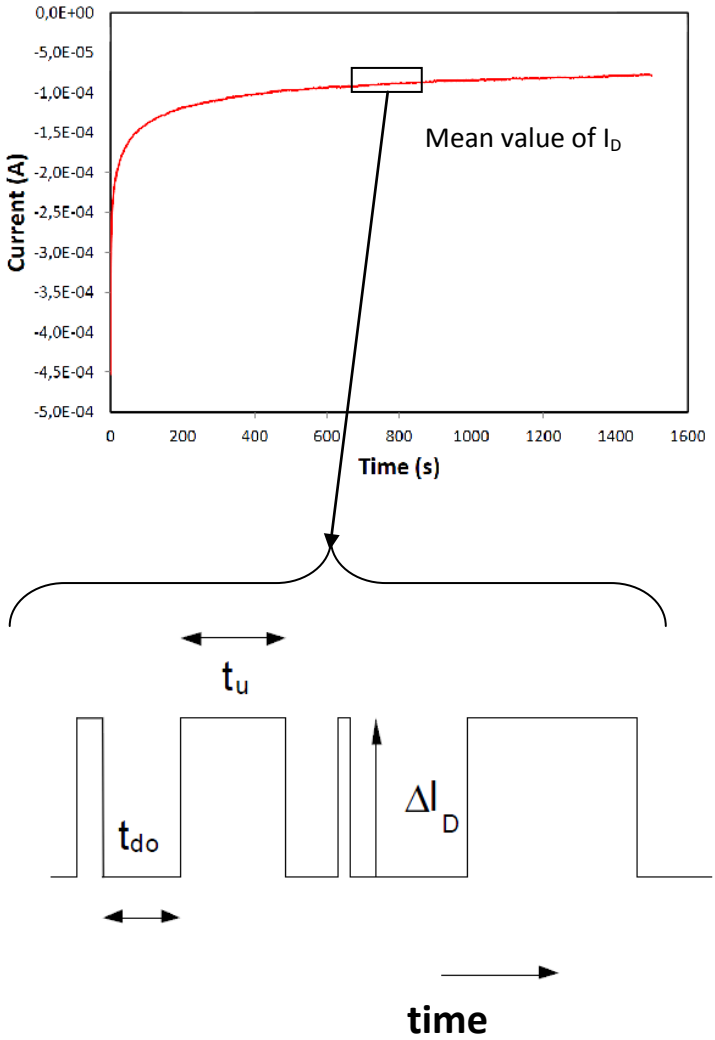


Figure II-14. Schematic representation of a two-level Random Telegraph Signal, showing its main parameters. [15]

In the 80s the RTN was studied in the time domain or in the frequency domain by applying a Fourier transform of the amplitude versus time signal [24] [25] [26]. The corresponding noise is a Lorentzian described in **Figure II-15** and Eq. 13 [15]:

$$S_{I_{(RTN)}} = \frac{2(\Delta I_D)^2 \tau_0}{4+(\omega\tau_0)^2} \qquad (13)$$

With ΔI_D the RTS amplitude, τ_0 the characteristic time constant and $\omega=2\pi f$ gives the radial frequency.

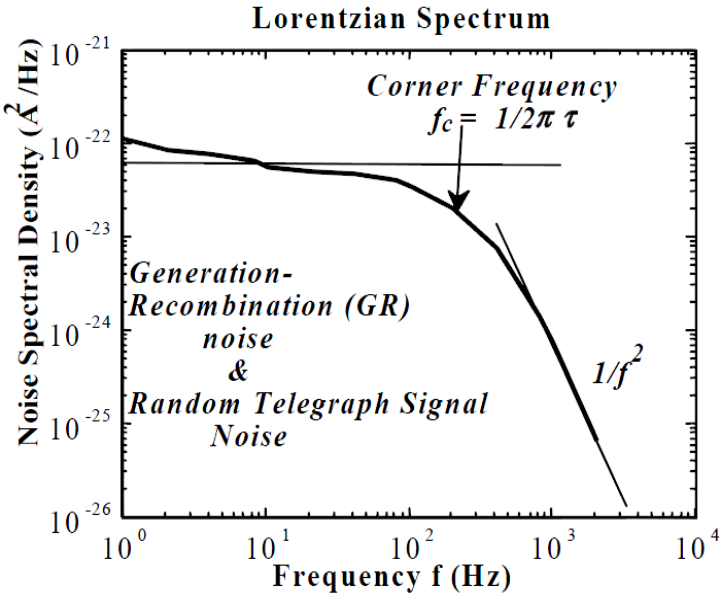


Figure II-15. Lorentzian noise spectrum associated with a RT signal. A similar type of spectrum is also obtained from generation-recombination (GR) noise in a large transistors produced by an ensemble of traps with the same energy level and capture cross sections [15].

The RTS noise is usually caused by number fluctuations that affect the conductivity (σ=nqμ) and result in a current change. The amplitude of the fluctuation is dependent of the carrier fluctuations (ΔR/R=ΔN/N).

- 1/f noise: This noise is characterized by a spectral density inversely proportional to the frequency. Thus, it is mainly observed in the low frequencies and its origin is always been controversial (fluctuation of the carriers mobility or fluctuation of the carriers number).

  - McWhorter explained this noise as a continuum of generation-recombination (GR) mechanisms. Its mathematical equation is defined as follows:

$$S_I = \frac{q\mu}{L^2}\,\frac{n_t f_t(1-f_t)}{n\times\ln\left(\frac{\tau_1}{\tau_2}f\right)}IV \qquad (14)$$

where $$f_t = \frac{1}{1+B\times exp\left(\frac{E_t-E_f}{kT}\right)} \qquad (15)$$

and $$n = N_c exp\left(\frac{E_f-E_c}{kT}\right) \qquad (16)$$

Where E_t is the energy of the involved GR center level, E_f is the Fermi level, E_c is the conduction band energy, n is the density of the free carriers and n_t is density of a GR center.

  - for Hooge, this noise is related to the fluctuation of the carriers mobility with a power spectral density proportional to the frequency and defined as:

$$\frac{S_I}{I^2} = \left\langle\left(\frac{\Delta R}{R}\right)^2\right\rangle = \frac{\alpha_H}{N}\times\frac{\Delta f}{f} \qquad (17)$$

where α_H is the Hooge parameter and N is the number of free carriers.

The study of the electric noise, mainly in the low frequencies (below 1 MHz) gives information about physical mechanisms in the body of the device. Indeed, **Figure II-16** shows an example of the measured noise spectrum with the different noise sources that can be found in GaN HEMTs. The analytical reconstitution of an LFN spectrum is presented in **Figure II-17** and can be carried out using the following equation:

$$S_{I_{(Total)}} = 2qI + \frac{4kT}{R} + \frac{B}{f^{\gamma}} + \sum_{i=1}^{n} \frac{K_i}{1+\left(\frac{f}{f_{ci}}\right)^2} \qquad (18)$$

where B is the LFN noise level, γ is the frequency index, K_i and f_{ci} are the magnitude and the cut-off frequency of the involved GR center "i".

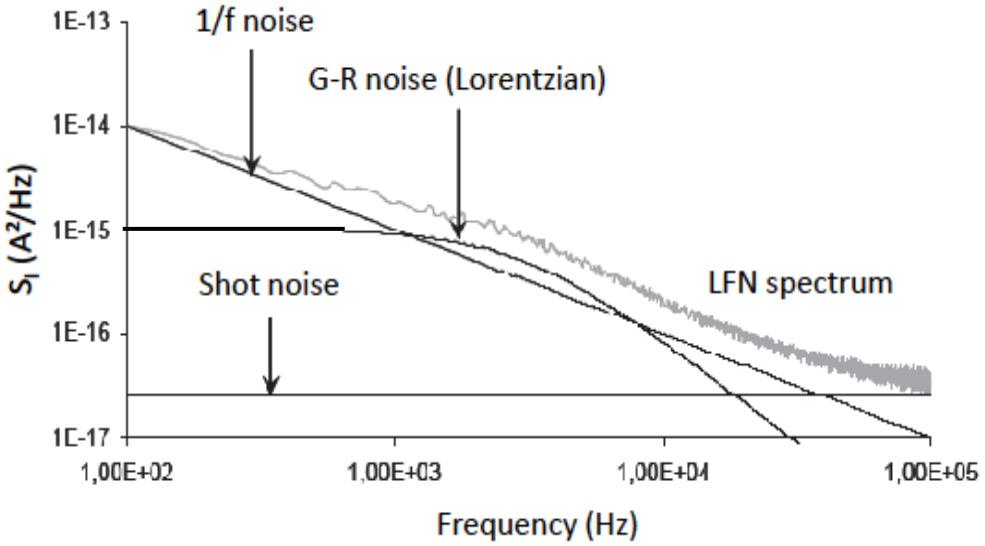


Figure II-16. Example of GaN HEMT LFN spectrum featuring the contributing noise sources [10]

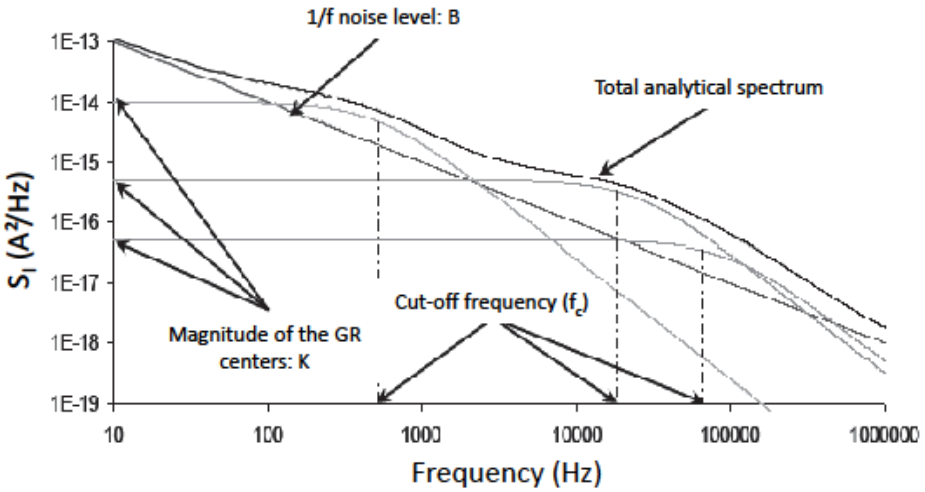


Figure II-17. Analytical reconstitution of the LFN spectrum [10]

II.3.3.c Adjustment of the measurement bench [16]

The measurement bench was developed by Laurent Bary during his thesis in 2001 [17, 18]. It consists of gate and drain biasing circuits as well as transimpedance amplifiers connected to the device. However, the measurement of the drain current noise is not accurate with the present system associating the drain biasing circuit and the transimpedance amplifier (**Figure II-18**) and mainly in the higher frequencies (when f>10 kHz) as shown in **Figure II-19**; thus there was a necessity to replace it by a new biasing circuit and a voltage amplifier for several reasons:

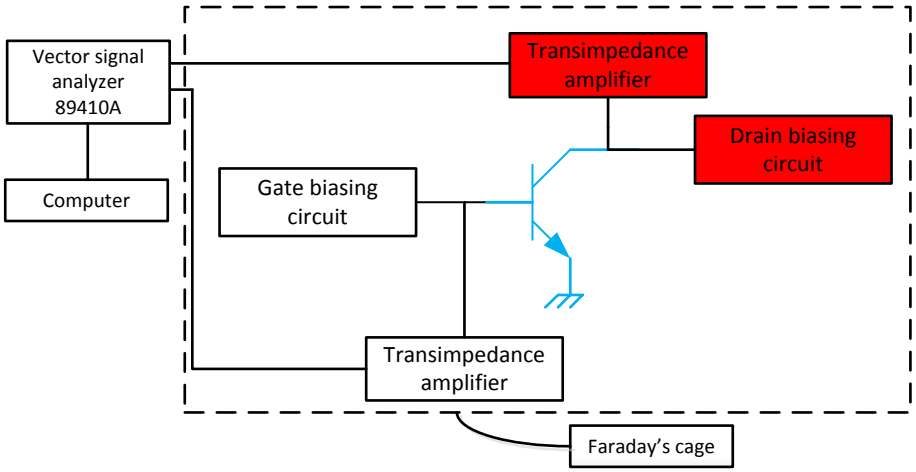


Figure II-18. Gate and drain current low frequency noise measurement bench featuring in red the adjusted parts of the bench.

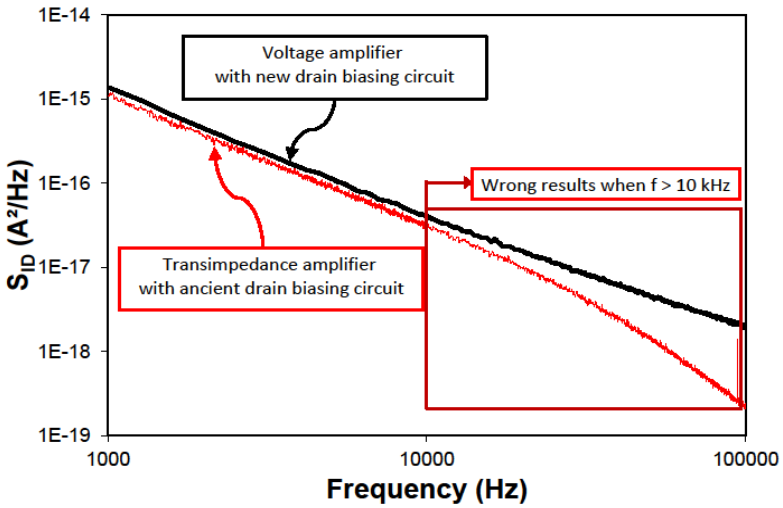


Figure II-19. Drain current LFN measurements with transimpedance amplifier and old drain biasing circuit (in red) and voltage amplifier and new drain biasing circuit featuring the wrong results with the transimpedance amplifier at frequencies above 10 kHz.

- The noise level: For a transistor exhibiting 500mA of drain current and biased with a battery of 24V, we need a biasing resistor R_B of 30 Ohms. Hence, a $R_{eq}=R_{DS}//R_B$ of approximately 30 Ohms is observed at the input of the transimpedance amplifier. The voltage noise of the amplifier will mask all other noise sources because:

$$\frac{\overline{e_t^2}}{R_{eq}^2} = \frac{10^{-17}}{30^2} \approx 10^{-20}\ A^2/Hz$$

This value corresponds to the noise floor limit. Hence, it is not possible to calibrate or verify the bench with low resistance values (the biasing circuit) instead of the transistor. For instance, the current noise of a 100 Ohms resistor is $1.6.10^{-22}$ A²/Hz representing only 1% of the voltage noise of the amplifier.

This reason concerns the biasing circuit more than the amplifiers, so it can be observed even if using a voltage amplifier (or any kind of other amplifiers since it is independent of the amplifier itself). Thus, the drain biasing circuit is replaced by a high power 10 laps potentiometer varying from 0 Ohms to 750 Ohms.

- Gain measurement: the gain measurement must be performed under realistic conditions, i.e. when the device is biased. To measure the gain of the system, we connect a white noise (WN) source at the input of the transimpedance amplifier as shown in **Figure II-20**.

$$\text{At the output: } V_{s(WN)} = i_{WN} \times \frac{R_{eq}}{R_{eq}+R_{in}} \times G_t \qquad (19)$$

where R_{eq} is $R_{DS}//R_B$, R_{in} is the real part of Z_{in} (**Figure II-20** and **Figure II-21**) and G_t is the gain of the transimpedance amplifier.

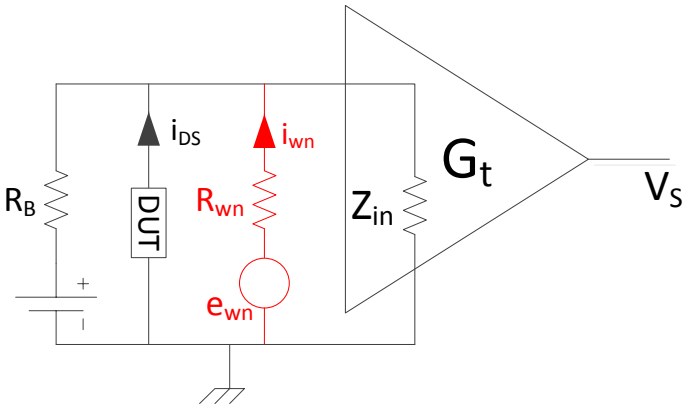


Figure II-20. Gain measurement circuit when the device is biased.

For an amplitude of -20 dBm (10^{-5}W) of the white noise source, the white noise voltage delivered is around $V_{WN}^2=10^{-3}$ V². Hence, the noise voltage at 100 kHz is in the order of $S_{VWN}=10^{-8}$ V^2Hz^{-1}.

Then, the current noise for a white noise resistor of 2 kOhms will be:

$$S_{i_{WN}} = \frac{S_{v_{WN}}}{R_{WN}^2} \ @\ R_{WN} = 2\ k\Omega \qquad (20)$$

$$\Rightarrow \quad S_{i_{WN}} = 2.5.10^{-15}\ A^2/Hz \qquad (21)$$

$10^{-15}A^2Hz^{-1}$ presents the maximum value to avoid saturating the amplifier at G= 10^6 VA^{-1} (respectively 10^{-13} A^2Hz^{-1} maximum at 10^5 VA^{-1} gain condition). A necessary precondition of $S_{iWN} >> S_{iDS}$ is then established. The gain cannot be measured when $S_{iDS} > 10^{-15}$ A^2Hz^{-1} in some part of the spectrum (i.e. in the lower frequency band near 1 Hz). For instance, with our devices and in the

low frequencies S_{iDS} is around 10^{-13} A^2Hz^{-1}. Thus, the measured coherence is different than 1 and the gain cannot be measured.

- Input impedance: The input impedance (Z_{in}) of the tranismpedance amplifiers is frequency dependent (as shown in **Figure II-21**). At the output, the measured voltage is gain and input current dependent (**Figure II-22** and Eq. 22):

$$i_{input} = \frac{i_{DUT}}{Z_{DUT}+Z_{in}} Z_{DUT} \quad (22)$$

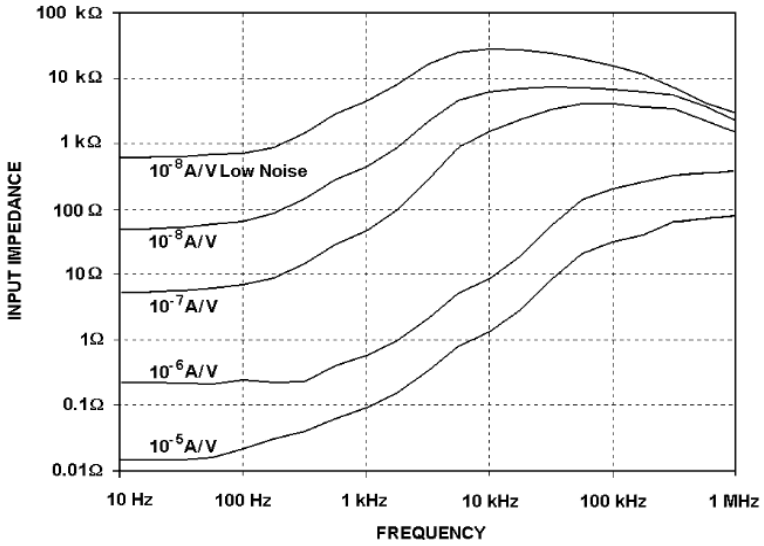


Figure II-21. The input impedance of the transimpedance amplifier and its variations versus frequency. [19]

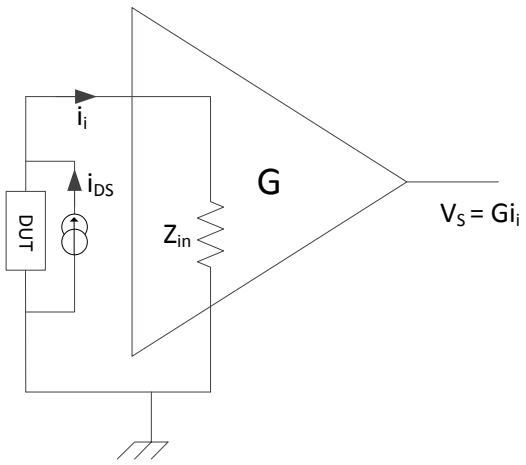


Figure II-22. Impact of Z_{in} on the Low frequency noise measurement.

When the device under test shows impedances (Z_{dut}) close to Z_{in}; two problems can generate: first, since Z_{in} is frequency dependent, the noise measurement will be influenced by the variations of Z_{in} with the frequency. Second, the noise of Z_{in} will mask the noise of the device under test. In comparison with voltage amplifiers, the $Z_{in\text{-}voltageAmp}$ is independent of the frequency and has a constant value of 10 MOhms.

It can be concluded from all the reasons above that the measurement of S_{iDS} is only possible when the two following conditions are respected:

$$S_{I_{DS}} \gg \left\{ \frac{\overline{e_a^2}}{R_{eq}^2} + \frac{2Re\left[\overline{e_a i_a^*}\right]}{R_{eq}} \right\} and$$

$$S_{I_{DS}} << 10^{-15} A^2/Hz \ \ for\ any\ frequency$$

Since these two conditions are not fulfilled on our devices, hence it is necessary to process the drain current noise measurements with a voltage amplifier instead of a transimpedance amplifier, and to replace the drain biasing circuit with another one compatible with the voltage amplifier.

Moreover, the stability of the bias is controlled and it is noticed from the evolution of the current versus time that 10 to 15 min waiting time is required to stabilize each bias condition of the device (long term memory effects and thermal stability, cf. chapter 3). **Figure II-23** shows measurement performed without waiting the bias stabilization of the device, it can be seen from this figure how the spectra are not superimposed as the device state (and noise sources related to this biasing condition) evolves during the first minutes of the characterization (for each of the 3 frequency bands). Moreover, **Figure II-24** shows the drain current evolution versus time, illustrating the waiting time necessary to reach a stable state of the device.

As the LFN test-bench is sensitive to different environmental and device-related phenomena, reference measurements are needed. These reference measurements are performed at the beginning of each measurement campaign on different reference samples, and are also at the beginning and at the end of each measurement day to assess the stability of the workbench and the validity of the data to be processed. Then it is possible to evaluate the statistical meaning of our measurements (measurement uncertainty). Hence, the differences noticed from the set of measured spectra can be analyzed and interpreted.

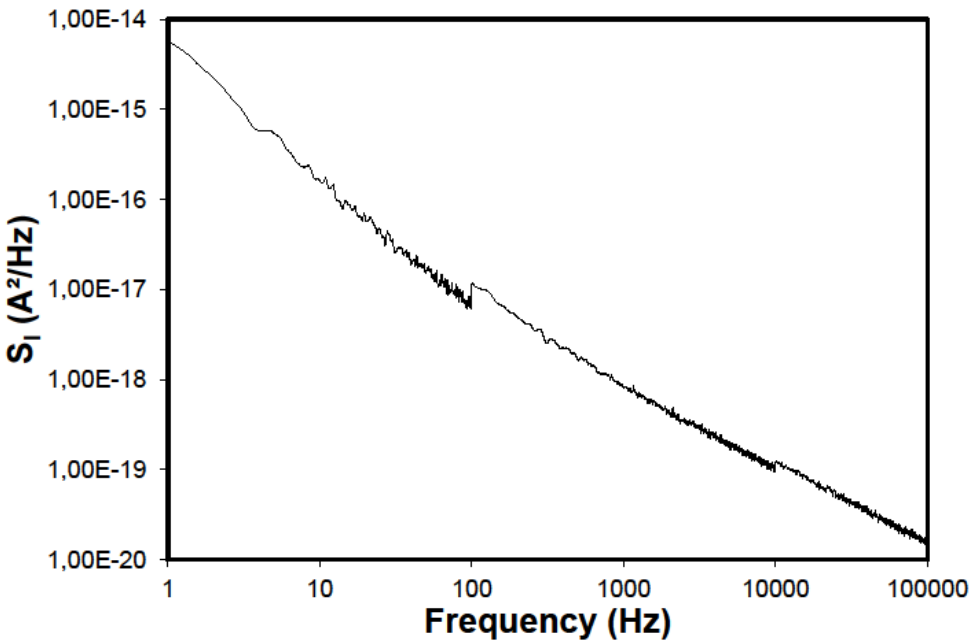


Figure II-23. Illustration of LFN measurements performed without the waiting time necessary for stability.

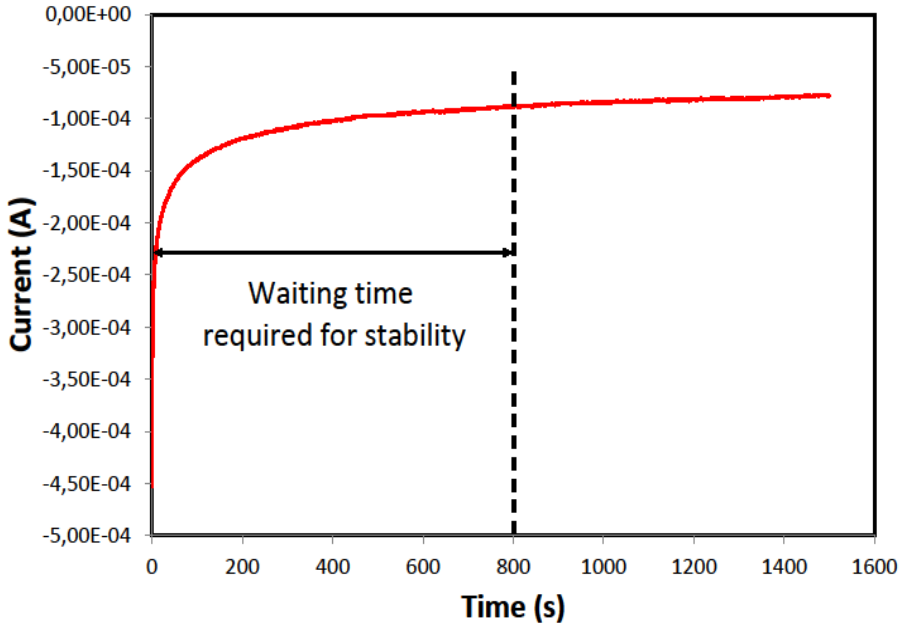


Figure II-24. Current versus time showing the waiting time required for the stability of the bias point (here is an example of the gate current).

The measurement bench of the low frequency noise is presented in **Figure II-25** and consists of gate and drain biasing circuits at each terminal of the device. Voltage and transimpedance amplifiers are connected in order to measure the gate and drain current noise spectral densities respectively. All these elements are located in a shielded room to reduce interference with the external environment. The amplifiers are then connected to HP89410 vector signal analyzer, and to a computer program to monitor and collect and correct the data. The measurements are performed at room temperature and in the frequency range from 1 Hz to 100 kHz.

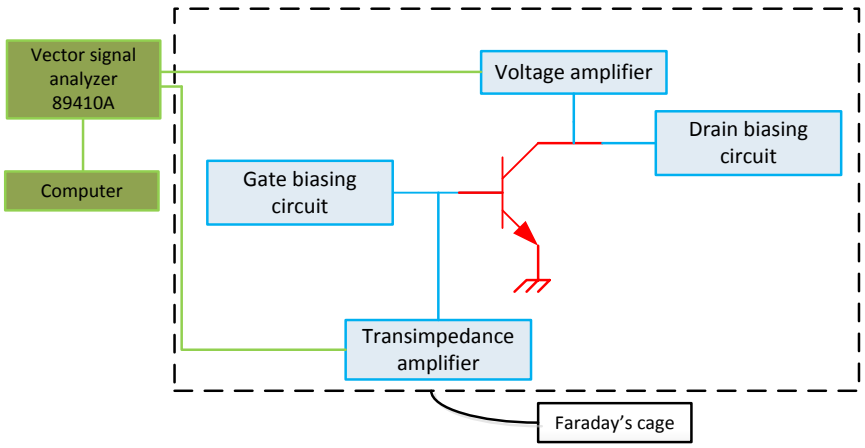


Figure II-25. Gate and drain current low frequency noise measurement bench.

II.3.4 Deep level Transient Spectroscopy (DLTS) technique

II.3.4.a Definition

The non-homogeneity of the crystal of a semiconductor creates energy levels in the bandgap that are the origin of deep centers (defects). These defects are due to dislocations or even created during the etching process. When these defects are near the conduction or the valence band, they are called n or p type impurities. However, when they are in the body of the bandgap, they are called deep traps. Their proximity to the conduction and to the valence band allows them to interact with the carriers that are present in both bands. Thus, they present the same characteristics as the generation-recombination centers. These interactions are shown in the **Figure II-26** where the centers act like a GR center in (a) and (b) or like a trap in (c) and (d). The emission and capture processes are dependent of the emission ($e_{n,p}$) and capture ($c_{n,p}$) rates.

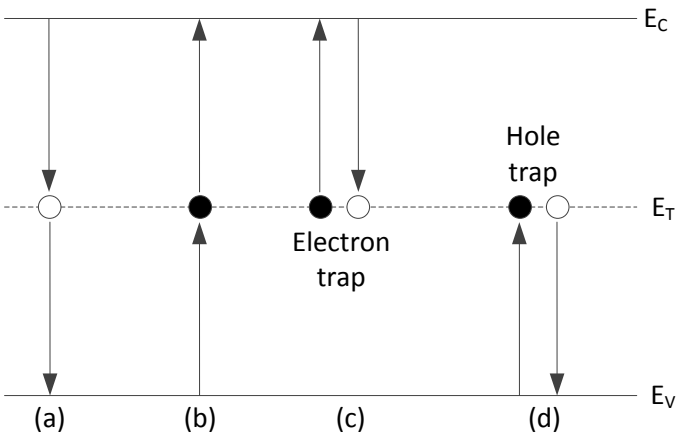


Figure II-26. Illustration of the interaction between the deep centers and the carriers.
(a) Electron capture and hole emission.
(b) Electron emission and hole capture.
(c) Electron trap.
(d) Hole trap.

II.3.4.b Emission and capture processes of deep centers

The capture rate can be written as:

$$c_n = \sigma_n n V_{thn} \qquad (23)$$

$$c_p = \sigma_p p V_{thp} \qquad (24)$$

Where $\boldsymbol{\sigma}_n$ and $\boldsymbol{\sigma}_p$ are the capture cross sections, V_{thn} and V_{thp} are respectively the thermal velocities in the semiconductor of the electron and of the hole expressed as follows:

$$V_{thn} = \left(\frac{3kT}{m_e^*}\right)^{1/2} \qquad (25)$$

$$V_{thp} = \left(\frac{3kT}{m_p^*}\right)^{1/2} \qquad (26)$$

And n and p are the hole and electron concentrations respectively, expressed as follows:

$$n = N_c exp\left(-\frac{E_c - E_F}{kT}\right) \quad (27)$$

$$p = N_c exp\left(-\frac{E_F - E_V}{kT}\right) \quad (28)$$

The capture rate allows characterizing the deep centers. The trap behaves like electron trap when $c_n >> c_p$, as a hole trap when $c_n << c_p$ and as a GR center when $c_n = c_p$. The capture cross sections $\boldsymbol{\sigma}_n$ and $\boldsymbol{\sigma}_p$ represents the surface where the free carriers can be captured. When the surface increases, the GR process's probability increases.

As for the emission, the rates can be expressed as follows:

$$e_n = K_n T^2 exp\left(-\frac{E_c - E_T}{kT}\right) \quad (29)$$

$$e_p = K_p T^2 exp\left(-\frac{E_V - E_T}{kT}\right) \quad (30)$$

where K_n and K_p are constants equal to $4\left(\frac{3}{2}\right)^{1/2} \pi^{3/2} \left(\frac{k}{n,p}\right)^2 \sigma_{n,p} m^*_{e,p}$ and $m_{e,p}$ is the effective mass of the electrons and the holes.

The emission rate is temperature dependent. It is experimentally possible to evidence the intrinsic characteristics of the center, like the activation energy E_a and the emission cross section (independent of T).

II.3.4.c Principle of DLTS

The DLTS technique is used for the detection of traps and defects in crystals [20]. It consists of applying a current pulse on a device and observes the transient response using capacitor or current based systems. Several approaches exist for the study of these deep centers; in the following work, we studied the I-DLTS and we limit our explanations to C-DLTS and I-DLTS methods:

- The C-DLTS: this system is commonly used due to the proportionality of the capacity with the derivative of the carrier numbers, thus more sensitive to the carrier flow.
- The I-DLTS: less accurate from the C-DLTS but allows overcoming all the series resistances that may disturb using the capacitor based system.

As for the FETs, the gate structure has an important impact. The capacity based technique is complex due to the small dimensions of the gate access leading to inaccurate results when measuring the capacity.

The results are presented by positive and negative peaks known as the DLTS signals (in Ampere) as a function of the temperature. The sign and the magnitude of the peaks indicate the nature of the trap and its concentration. Moreover, information on the trap cross section and its activation energy can also be extracted from the measurements. The experimental bench used in LAAS is exploited by Francois Olivier.

II.3.5 OBIRCh: an electro-optical technique

The technique was proposed and developed by Nikawa and Tozaki in 1993 [21]. It consists of detecting defects and current paths in metal lines [22] as well as high resistance areas at the bottom of the vias [23]. The OBIRCH system (and not the method) has the ability to detect thermal property anomalies, DC current path anomalies, thermoelectric power anomalies and Schottky barrier anomalies [24].

II.3.5.a Laser stimulation technique

The OBIRCh is a laser stimulation technique applied on electrically and optically accessible samples with a wavelength of 1.34 µm and can also be used in the visible and near infrared (200 to 1700 µm). The packaged devices will be open from the front or from the rear. The technique allows detecting resistive defects mainly in the Back End Of Line (BEOL): resistive short-circuit, abnormal current path, oxide breakdown… The technique is applied on devices under their static behavior when a constant voltage bias is applied and the current is measured. In general, the goal is to determine where the failure is physically located. More specifically, the laser stimulation allows localizing defects leading to the self-heating of the device under biased conditions or not and under specific operating condition.

II.3.5.b Description of the technique

The OBIRCh measurements are performed at University of Rouen, France, under the supervision of Professor Olivier Latry and with the assistance of Dominique Carisetti from TRT. We used Phemos 1000 and the operating mode is described in KP5-334 [25] and Instruction d'utilisation du microscope à émission du Phemos 1000 [26] by Hamamatsu.

The principle of the OBIRCh technique consists of biasing the device, then measuring the current before and during laser irradiation. The laser irradiation can be performed from the front and from the back sides (as shown in **Figure II-27**). In the present work, only the frontside characterization has been performed (no need of specific samples).

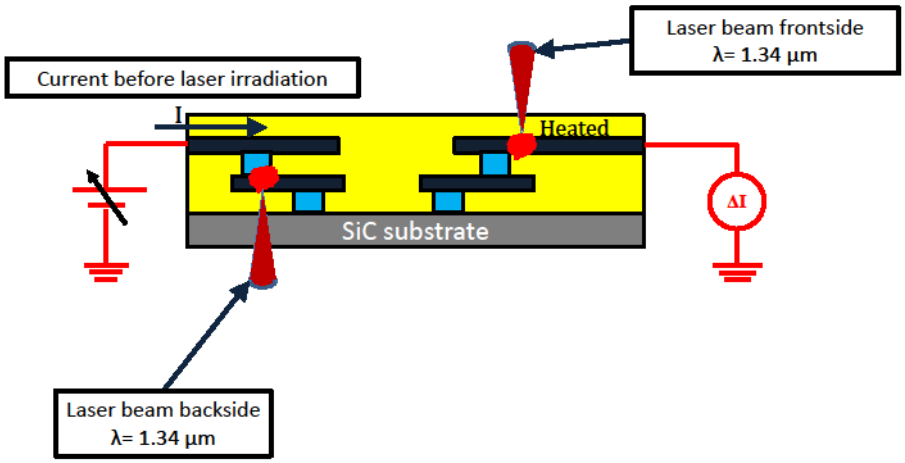


Figure II-27. Illustration showing the principle of OBIRCh technique and the both sides of the laser irradiation.

An amplifier is connected on the output to amplify the measured current. The current fluctuations are then related to the resistivity variations (at constant voltage) within the following equation [29]:

$$\Delta I = -\frac{\Delta R}{R^2} V \qquad (31)$$

The resistivity fluctuations are related to the temperature fluctuations after heating with the laser, through α that is a Temperature Coefficient of Resistance (in K^{-1}) of the material being heated:

$$\frac{\Delta R}{R} = \alpha_{TCR} \times \Delta T \qquad (32)$$

The sign of α indicates whether the detected defect is in the metal or in the semiconductor, **Figure II-28** synthesizes the defect detection dependence with α.

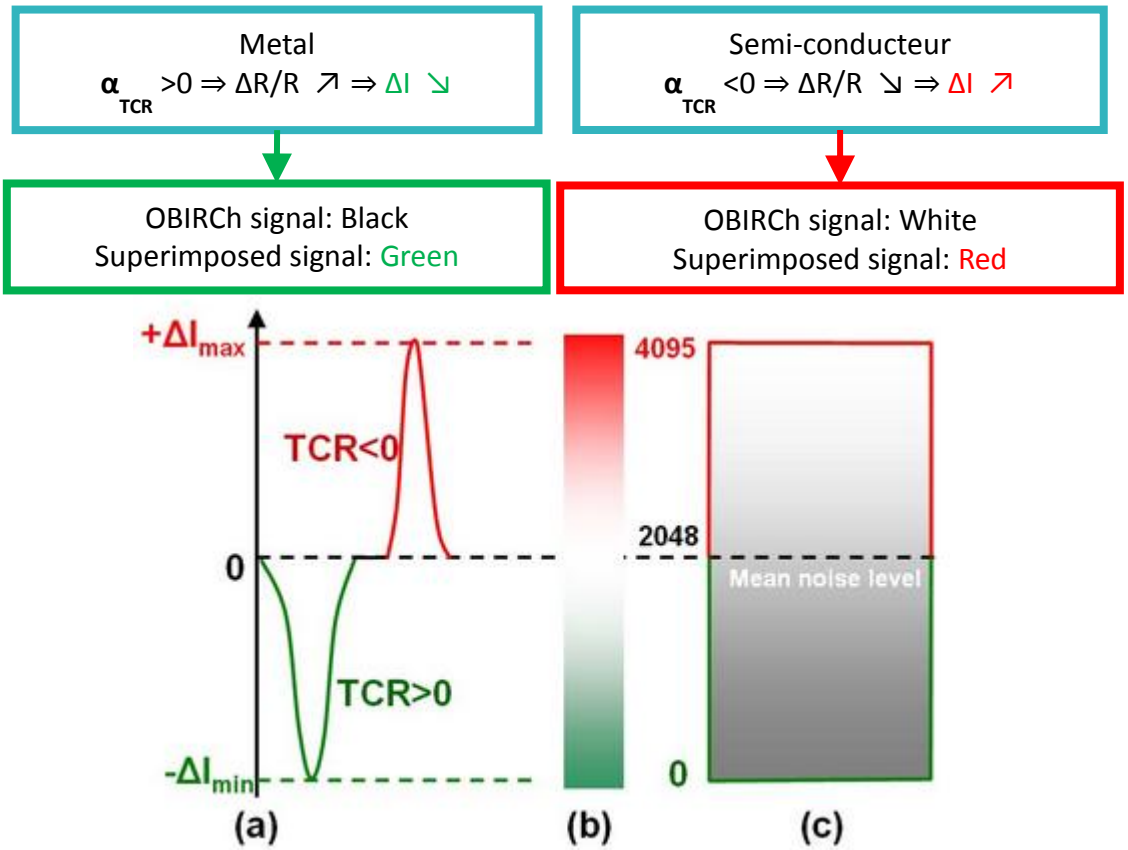


Figure II-28. Defect detection. [27]
(a) Current variation.
(b) Superimposed colors.
(c) Coded IR-OBIRCh signal.

Moreover, according to Sanchez *et al* [28]., the resistance variation is not only affected by α but also by δ that presented the modification of the spatial dimensions and the Eq. 32 becomes:

$$\frac{\Delta R}{R} = (\alpha_{TCR} - 2\delta_r) \times \Delta T \qquad (33)$$

This second term has a tiny effect on the resistance variation and it can be neglected in most cases.

Table II-3 shows a comparison between three different and usually used failure analysis techniques. It can be easily judged the importance of the IR-OBIRCh system compared to the emission microscope (EMMI) and to the liquid crystal method (LCM) techniques. The EMMI technique is a light emission microscope (LEM) technique to detect deep traps and recombination effects and the LCM technique consists of introducing a liquid on the surface called Cholesteric liquid.

	IR-OBIRCH system	Emission microscope (EMMI)	Liquid Crystal Method (LCM)
Detectable anomalous phenomena	• Thermal property anomalies • DC-current path anomalies • Thermoelectric power anomalies • Schottky barrier anomalies ***	Slight light emission **	Hot spots **
Type of material	Metal or semiconductor ***	Semiconductor only ***	
Microscope	Co-focal laser scanning microscope ⇒ better spatial resolution ***	Conventional optical microscope **	Conventional optical microscope ⇒ Liquid crystal deposited on a chip surface degrades the spatial resolution *
Sensitivity	1µA at 1V and 1µW **	Most sensitive (1nA) ***	The worst (several ten µW) *
Backside observation	Very few limitations ***	Only longer wavelength light among emitted light **	Impossible *
Necessity of preprocessing	Mirror polishing is required when observing from the backside ***	Mirror polishing and usually a thinning of a wafer or a chip is required when observing from the backside *	Liquid crystal deposition is required **
Flexibility of electrical-state setting by test vectors	Only a static is possible **	Both dynamic and static settings are possible ***	Both dynamic and static settings are possible ***

Table II-3. Comparison with conventional failure analysis methods and ranking of each technique for each characteristic as follows (inputs compiled from [24]):
Best : ***
Intermediate : **
Worst : *

II.3.5.c Implementation

Two types of devices are tested by the OBIRCh technique:

- On wafer devices, are placed directly on the chuck. The electric contacts are made with probes hold on the station on each side of the chuck.
- Packaged devices: are deposited directly on the chuck in their proper socket.

The CCD camera can take physical photos of the devices under test. The Phemos 1000 for laboratories is usually accompanied with a laser source of 1.34µm wavelength and 100mW max that radiates the surface of the device.

The suitable lenses for OBIRCh are 5x, 20x, 50x and 100x, each with its own numerical aperture. The highest sensitivity at high magnification is obtained with the 50x that is specially adjusted to the 1,34 µm laser.

The measurements are performed at room temperature, and at 223K for the CCD camera controlled by the software. The maximum voltage/current are 10V/100mA under commonly using conditions and 70V/2A with “high current probe head”.

II.4 Conclusions

The chapter synthesizes the experimental tools developed for the study of the reliability of GaN devices. The first part includes the management of the ReAGaN project with all the partners and their contributions.

A detailed description of our laboratory contribution is presented next, highlighting on each experimental tool and procedure necessary for the study of the AlGaN/GaN HEMTs. Current and temperature stabilities are of main importance for the LFN and DC versus temperature techniques. The test-benches are verified before each characterization campaign and the last result carried out in the previous campaign is repeated for more accuracy; moreover, this back-up test brings additional information on the device evolution (if occurred) during the previous measurement campaign.

Figure II-29 illustrates the time and frequency range of the experimental tools and stress workbenches. It can be seen that each experimental technique presents its own frequency/time range; hence the device should not evolve during the characterization campaign for better extraction of the activated defects. The initial and final observations of the gate and drain currents should be in the same order, any modification requires a restart in the characterization campaign. For more rigorous study, the visual observation and the DC measurements are always performed between two different characterization techniques (even when an exchange of devices between partners happens).

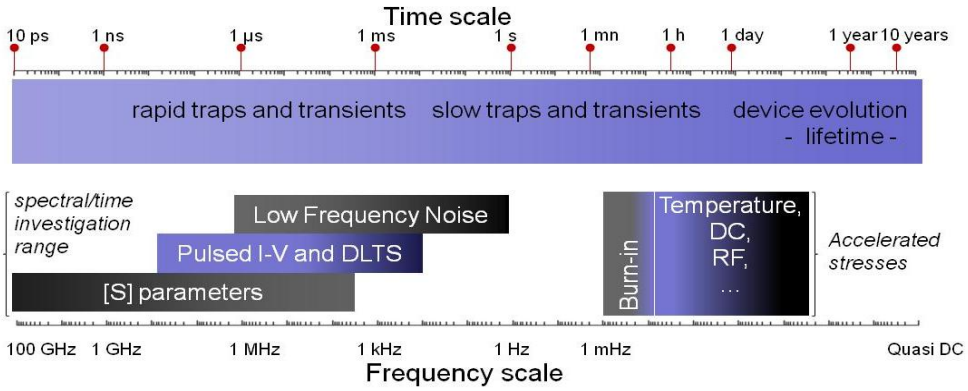


Figure II-29. Graphic representing the time/frequency staggering for LFN, electrical I-V and [S] parameters (investigation range), and stress induced time range. Measurements must be non-invasive versus stress. [30]

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Chapter III:

RELIABILITY STUDY CASES

III.1 Introduction

This chapter presents investigations issued on AlGaN/GaN HEMTs by making use of the different experimental techniques presented in the previous chapter (Chapter 2-II). As a large number of set of devices have been investigated, a rigorous classification is needed (technological declination, stress type and state of the device before characterization if concerned, type of measurements to perform). After a quick visual inspection (microscope) of the devices, DC characterizations are performed (output characteristics, leakage current): this is mandatory to set the biasing conditions where the device must/can be measured. Hence, when the static information about the device is provided, all the other characterization techniques can be performed independently from the sequence, since they are all considered as non-destructive techniques for the devices under test, and as we expect them not to stress the device (cf. chapter 2: LFN measurements performed as first and last measurement on a reference device and on a reference biasing point of the measured device after the characterization campaign). For instance, the LFN measurements can precede the OBIRCh characterizations and inversely: LFN measurements are considered as accurate indicative of a microscopic state of the device as they concern noise sources measurements. The noise source stability is much more sensitive than a reproducible electrical trace.

Thus, as stated in the conclusion of the previous chapter, the device procurement has been decided in accordance with the priorities of the project and the needed steps to identify the main issues to better understand the root causes of failures mechanisms: study cases have been sorted out by UMS as the technological leader of the consortium, with the partners' approval. As long as the results are presented, discussions will highlight on the impact of the experimental technique and the physical mechanisms brought out from the study. Correlation between experimental techniques and degradation mechanisms on the AlGaN/GaN HEMTs are also discussed as well as comparison between GH50 stressed and virgin devices. For the study on the GH50 process, two approaches were undertaken: while the next called **Declination_S** concerns on wafer small dimension devices (mono-

finger), the **Declination_L** is related to the commercial declination of the devices (large dimension multi-fingers device, packaged). The two processes are identical, except for the source field-plate (FP) that is not realized on **Declination_S** set of devices. Then, **Table III-1** summarizes the goals and measurement possibilities over the two GH50 declinations. Comparison between declination-S and declination-L must be carefully weighted as the devices, even if realized according to the same process and set of masks, are not from the same wafer and can be sensitive to dispersion effects (according to the placement within the wafer) and to some technological uncertainties (technological reproducibility). However, in the next paragraphs, we will assess some of the technological parameters such as the barrier height for devices from the two declinations (and also from declination-S, with and without field-plate).

GH50 process name Main differences	Measurements possibilities
Declination_S Mono-finger, on wafer devices 1x100µm. With and without Field-Plate (FP). Stress type: HTOL.	**Laser based techniques** • No field plate: improved accuracy for spot location and intensity (no edge effects) **Electrical measurements:** • Check if techniques and parameters (barrier height, lag effects, etc.) are more or less pronounced for large or small devices (correlate with laser techniques and Low Frequency Noise measurements) • Check if the device scaling or Field plate affect technological parameters **Low Frequency Noise characterization** • Small devices: comparison of defects versus large devices (LFN → 1/f contribution is increased for small devices) • Evolution of GR centers before/after stress period
Declination_L Multi-fingers, packaged devices 4x400µm. Source Field-plate. Virgin, leaky and non-leaky devices. Stressed, leaky devices Stress type: HTOL	**Laser based techniques** • Less sensitive because of the field plate for front-side measurements. Possibility to perform back side measurements with dedicated packaging **Electrical measurements** • Large characterization for lag effects, thermal effects for stressed and virgin devices **Low Frequency Noise characterization** • Evolution of GR centers on virgin and aged devices for different type of stresses

Table III-1. Goals and measurements possibilities over **Declination_S** and **Declination_L** GH50 technologies.

III.2 GH50 Declination_S: on wafer devices

III.2.1 Devices under test and study roadmap

The **Declination_S** as stated previously are fabricated at United Monolithic Semicondcutors (UMS) [1]. They are grown on SiC substrate and feature 18% of Al content in the high bandgap layer. The surface is SiN passivated and the Schottky contact is formed by deposition of Ni/Pt/Au transition

metals. They are research level devices featuring single gate finger with a width of 100 µm and a length of 0.5µm (1×100µm×0.5µm) as shown in **Figure III-1**. Two declinations are proposed for these devices (next referenced as #A and #B) featuring extrinsic difference at the interconnections between the gate finger and the gate pad; this difference can be observed on the mask view of the devices presented in **Figure III-2**. Furthermore, #A devices are divided into two types (with and without field plate devices) in order to highlight on the impact of the field plate structure in such devices.

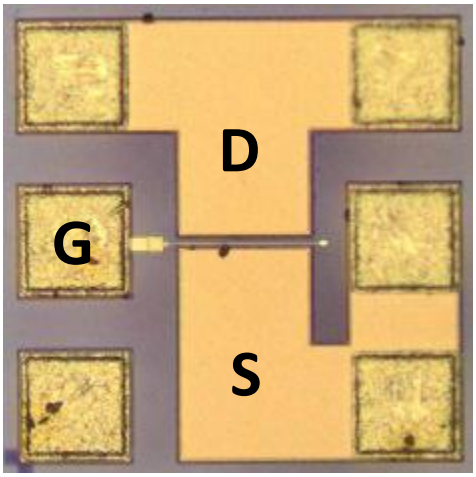
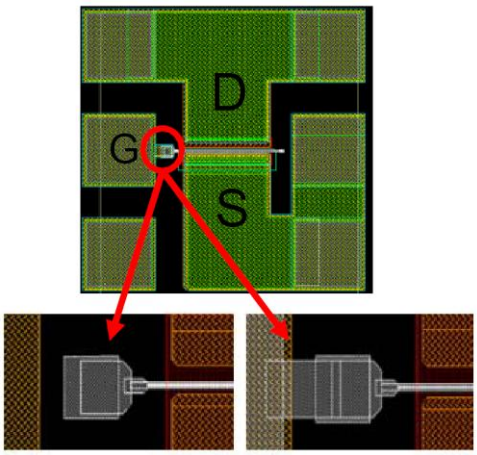


Figure III-1. Top view of Declination_S devices under test.



Device #A Device #B

Figure III-2. Mast top view of the devices under test.
Device #A: without the interconnection between the gate and the pad.
Device #B: with the interconnection between the gate and the pad.

The study on these devices is focused on their gate current conduction mechanisms, as this point is considered as the major phenomena to investigate concerning the reliability of GaN HEMT devices. Under forward gate biasing conditions, DC I_G-V_{GS} measurements versus temperature are performed in order to study the Schottky barrier height. Whereas under reverse biasing conditions, gate LFN measurements are performed on the Schottky diode (open drain configuration) and on the transistor (biased at V_{DS}=8V): these conditions are chosen to discriminate between the activated noise sources under these two configurations (diode alone / transistor), and to propose reliable interpretations about the origin of the activated defects after the application of a stress OBIRCh measurements are

also performed under reverse biases. Furthermore, EBIC results from the DGA are presented to correlate with our results and to validate the proposed electrical technique.

The main difference between the two types of devices is observed on their reverse gate leakage current where #A devices show a higher leakage current than #B devices (two decades and more, cf. **Figure III-3**). Due to these very low leakage currents and to the resolution of our LFN bench, the gate LFN measurements cannot be performed on #B devices. Hence, #A devices with and without field plate are studied. Moreover, devices with field plate cannot be measured by the OBIRCh technique, thus #B devices and #A devices with field plate are not fully characterized.

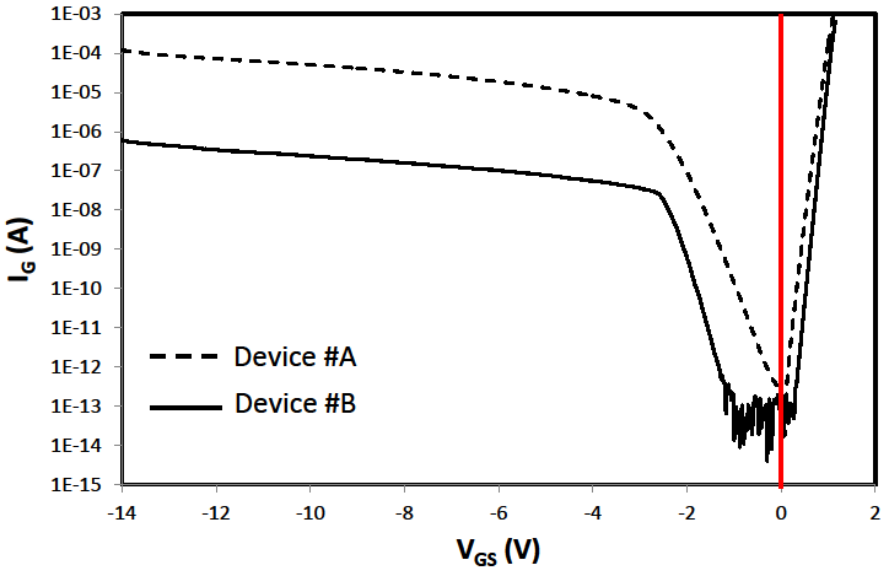


Figure III-3. DC I_G-V_{GS} measurements on #A and #B devices, featuring a difference of two decades on their reverse gate leakage current.

However, the wafer has been totally characterized at ambient (electrical measurements), and no significant difference has been sorted out between devices with/without field plate. For reasons of clarity and consistency, the study on Humbolt_18 wafer will be focused on #A devices without field plate (electrical, Low frequency noise, OBIRCh).

III.2.2 Electrical characterization versus temperature

On wafer DC I_G-V_{GS} in the temperature range of 100k to 400k are performed using Agilent 4156C and a Cryoprober. The study presented next are illustrated for a given device from each type but is statistically relevant and representative (the results are similar on 6 devices from #A and 5 devices from #B). **Figure III-4** shows the forward I_G-V_{GS} characteristics of the Schottky diode for devices #A and #B. The physical parameters are first extracted according to Eqs. 1 and 2 [3].

$$I_G = I_s exp\left(\frac{qV_{GS}}{nkT}\right) \quad (1)$$

$$\text{with } I_S = SA^*T^2\, exp\left(-\frac{q\phi_B}{kT}\right) \quad (2)$$

where I_S is the saturation current, q is the electron charge, n is the ideality factor, k is Boltzmann constant, T is the temperature, S is the effective area of the diode, A* is the effective Richardson constant found to be 32 $AK^{-2}cm^{-2}$ from A*=0.266A (according to Eq. 3 where A=120 $AK^{-2}cm^{-2}$ and $m^*=0.266m_0$ is the effective mass) for the AlGaN and ϕ_B is the Schottky barrier height [3].

$$A^* = \frac{m^*}{m_0} A \qquad (3)$$

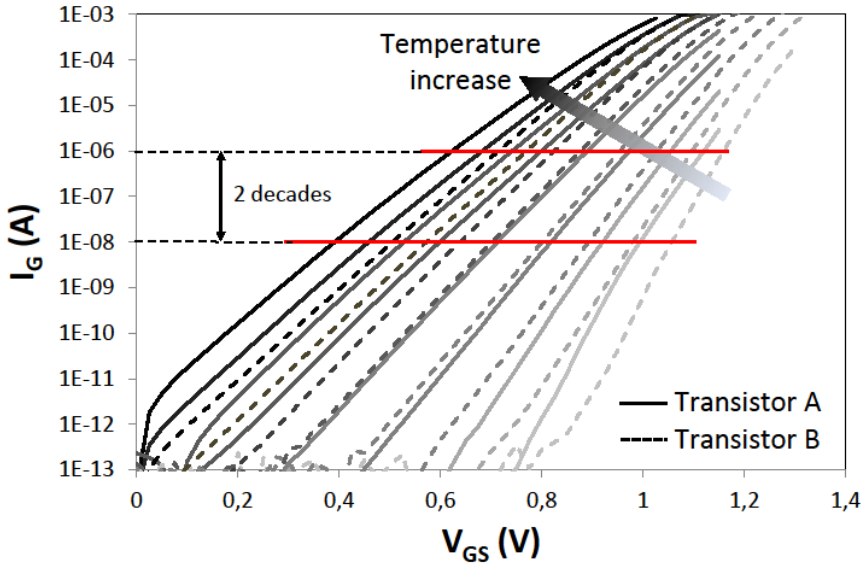


Figure III-4. Forward gate current-voltage (I_G-V_{GS}) characteristics of AlGaN/GaN HEMTs, open drain configuration versus temperature ranging from 100K to 400K.

The Schottky parameters or the electrical parameters of the Schottky diode are the ideality factor and the Schottky barrier height and their dependences with the temperature variations:

III.2.2.a Electrical parameters extraction

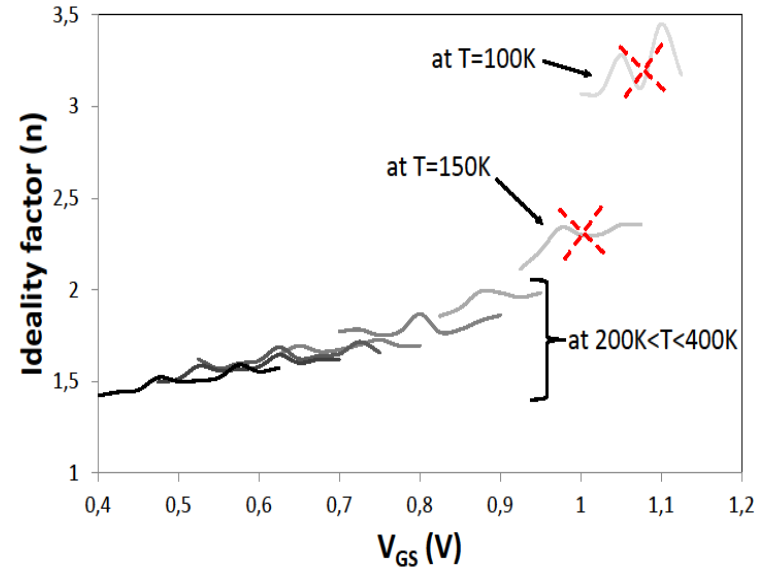
III.2.2.a.1 Ideality factor dependence of forward bias

Figure III-4 displays a constant current region [4] where the I-V-T characteristics can be fitted (10^{-8}A – 10^{-6}A). If these measurements feature a linear relation for all the temperatures (100K to 400K), a variation appears when studying the ideality factor variations versus V_{GS} using the following equation:

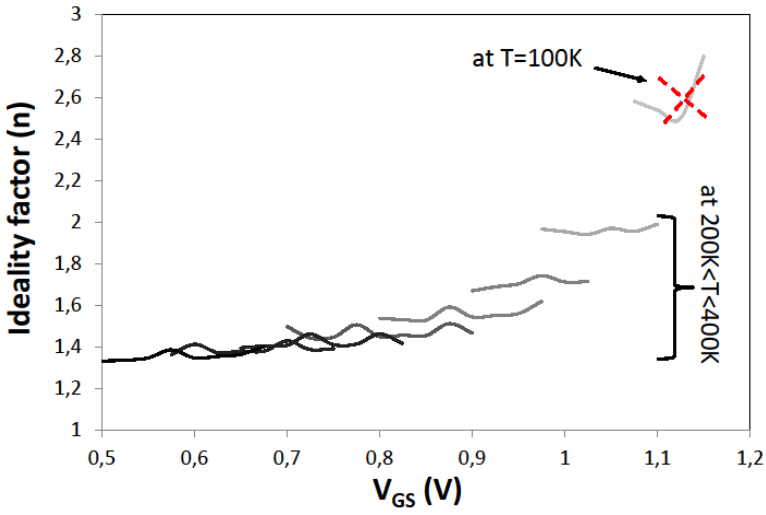
$$n = \frac{q}{kT}\left[\frac{dV}{dln(I/I_S)}\right] \qquad (4)$$

Therefore, to choose and validate the linear segments for fitting the diode characteristics, it is essential to observe the ideality factor variations versus the applied bias V_{GS} for all the temperatures: *n* must show a quasi-constant value versus V_{GS} as presented in **Figure III-5(a)** and **5(b)** (respectively for the devices #A and #B). The large variation of the ideality factor at 100K and 150K for #A devices has no physical sense and these temperatures are thus excluded from the study proposed in the next paragraphs (idem for #B at 100K). Hence, the best fitting and analysis of the data are in the temperature range of 200K-400K for #A and 150K-400K for #B. The same procedure has been tested

for a current range of 5 decades, displaying higher non-linear deviations on the ideality factor (and a reduced accuracy on the extracted parameters): thus, reducing the current range (here taken at 2 decades) improves the accuracy of the extraction method.



(a) Device #A



(b) Device #B

Figure III-5. Ideality factor (n) versus forward bias (V_{GS}) for devices #A and #B within a constant current range of two decades, and for different temperatures. The red deletions indicate which measurements have to be excluded from the study (100K to 150K for device #A and at 100K for device #B), based on the results of the next method (feedback).

III.2.2.a.2 Ideality factor and Schottky barrier height dependences of the temperature

The first electrical/physical parameters highlighting on the Schottky barrier homogeneity are the ideality factor and the Schottky barrier height (SBH). By combining Eqs. 1 and 2 and plotting Eq. 5, it is possible to extract the temperature dependency of n and ϕ_B in **Figure III-6**.

$$ln\left(\frac{I}{SA^{*}T^{2}}\right) = f(V) \qquad (5)$$

A marginal decrease of the Schottky barrier height (SBH) and a marginal increase of the ideality factor are observed in the lower temperature range, in comparison with the higher temperature range. These variations are early indicators of deviation from the conventional Richardson behavior: the assumption of homogeneous Schottky barrier could be wrong. According to Werner *et al.* [5], these variations can be attributed to interface states at the thin oxide between the metal and the semiconductor, extra current caused by tunneling through the barrier, generation-recombination current within the space charge region and edge related currents.

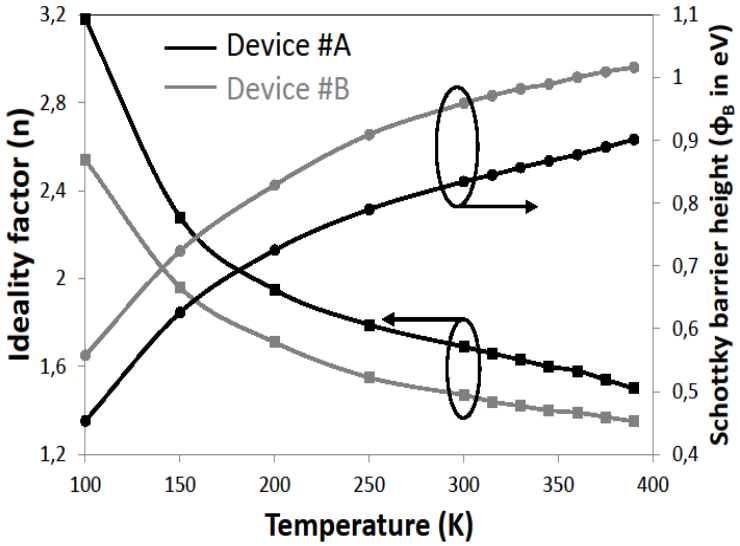


Figure III-6. Temperature dependence of the ideality factor (n) and Schottky barrier height for devices #A and #B (with black and grey plots respectively).

The SBH becomes smaller as the ideality factor increases [6] [7]. This phenomenon is represented in **Figure III-7**. Plotting ϕ_B versus n allows to extract the barrier heights for an ideal study case (considering n=1) of the Schottky diode. The extracted values of the SBH at n=1 are 1.1eV for #A, and 1.2eV for #B.

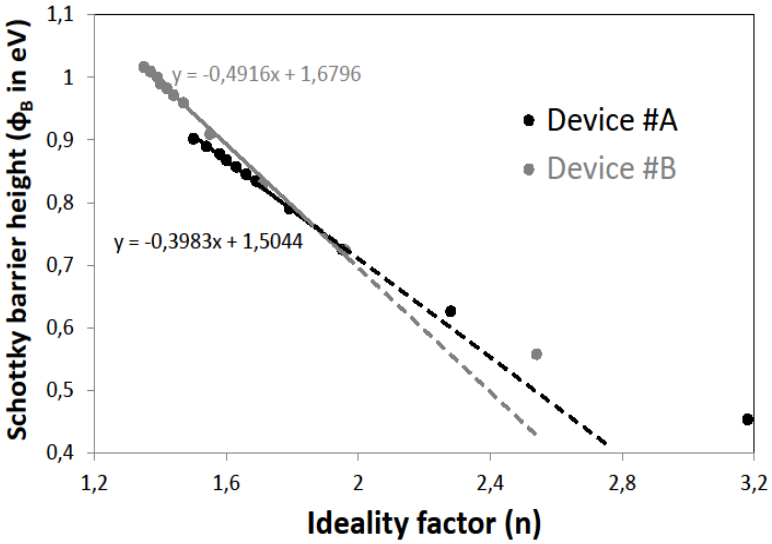


Figure III-7. Schottky barrier height versus ideality factor for devices #A and #B (black and grey plots resp.) featuring the equations of the trends for each device.

III.2.2.b Potential fluctuation model application

The model proposed by Werner and Guttler in [5] is designed to analyze the transport properties and the roughness at the interface between the metal and the semiconductor. It is an analytical model and does not require any computer simulation. A Gaussian distribution with a standard deviation is presented in Eq. 6 [5]:

$$P(\Phi_B) = \frac{1}{\sigma_S\sqrt{2\pi}} \exp\left[-\frac{(\overline{\Phi_B}-\Phi_B)^2}{2\sigma_S^2}\right] \qquad (6)$$

By using Eqs. 1 and 6, we obtain [5]:

$$\Phi_B(T) = \overline{\Phi_B} - \frac{\sigma_S^2}{2kT/q} \qquad (7)$$

where $\overline{\phi_B}$ is the mean barrier height, and $\boldsymbol{\sigma}_S$ is the standard deviation that represents the barrier inhomogeneities (the lower the standard deviation, the better the barrier height homogeneity). By using Eq. 7 and by plotting Φ_B versus 1/T (**Figure III-8**), the negative slope and the y-intercept allows extracting $\boldsymbol{\sigma}_S$ and $\overline{\phi_B}$. **Table III-2** synthesizes the extracted values for the two types of transistor's configurations #A and #B. **Figure III-8** also illustrates the barrier inhomogeneity for both devices; in case of homogeneous barrier, the plot of the SBH versus 1/T should exhibit an horizontal trend parallel to the x-axis, featuring a constant value of Φ_B, which is not the case for these two types of diodes.

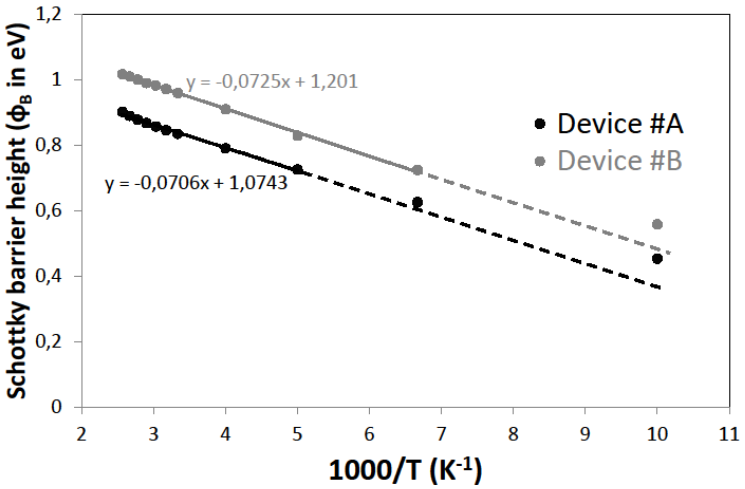


Figure III-8. Schottky barrier height calculated from I-V-T measurements versus 1/T for devices #A and #B (in black and grey plots resp.).

Schottky barrier height anomalies evidenced by Richardson constant values

The constant SBH and the effective Richardson constant can be extracted using Eq. 8 as presented below:

$$ln\left(\frac{I_S}{T^2}\right) = ln(SA^*) - \frac{q\Phi_B}{kT} \qquad (8)$$

The plot of $\ln(I_S/T^2)$ versus 1/T from Eq. 8 (as shown in **Figure III-9** with filled squares) must correspond to a straight line where the slope and the y-intercept are used to extract ϕ_B and A* respectively.

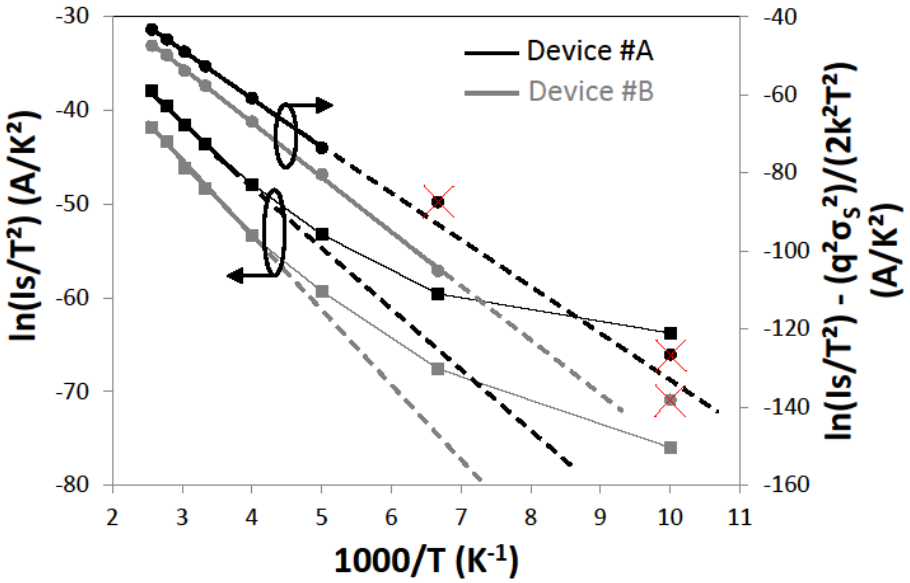


Figure III-9. Conventional and modified Richardson plots of AlGaN/GaN HEMTs:
- Conventional Richardson plots with the y-axis on the left.
- Modified Richardson plots with Werner's model using the y-axis on the right.

Device #A: black lines and dots.
Device #B: grey lines and dots.

The Richardson plot should exhibit linearity in the whole temperature range, but it is noticeable that the linear portion is reduced between 250K and 400K (non-linearity at low temperatures). By fitting the plots, a ϕ_B and an A* of 0.6 eV and 2.8×10^{-3} $AK^{-2}cm^{-2}$ for transistor #A and 0.7 eV and 1.3×10^{-3} $AK^{-2}cm^{-2}$ for transistor #B are extracted. Deviation in Richardson plots leads to a strong deviation in A*, thus the M-SC interface is considered as inhomogeneous. According to Werner and Guttler's model [5], the SBH in Eq. 8 should be replaced by its value in Eq. 7:

$$ln\left(\frac{I_S}{T^2}\right) = ln(SA^*) - \frac{q\overline{\Phi_B}}{kT} + \frac{q^2\sigma_S^2}{2k^2T^2} \qquad (9)$$

The Richardson plot modified by Werner's model can be written as follows:

$$ln\left(\frac{I_S}{T^2} - \frac{q^2\sigma_S^2}{2k^2T^2}\right) = f\left(\frac{1}{T}\right) \qquad (10)$$

and shown in **Figure III-9** with filled circles.

Table III-2 synthesizes the Schottky diode parameters extracted from the conventional Richardson method and from the modified Richardson plot using Werner's model. The temperature range is reduced according to the non-constant values of the ideality factor versus V_{GS} for some temperatures (cf. **Figure III-5**). The new values obtained for A* from our experiments are in close agreement with the theoretical value (32 $A.K^{-2}cm^{-2}$). The small difference keeps the effective Richardson constant as a questionable parameter! But according to Horvath [8], this is due to the real effective mass that is not always equal to the theoretical value (m*=0.266m0) calculated at the pure

thermoionic emission [3]. Hence, the A* value obtained from I-V-T measurements could be affected by the lateral inhomogeneities of the barrier. The new values of m* are also presented in **Table III-1**.

$$A^* = \frac{4\pi q m^* k^2}{h^3} \qquad (11)$$

where h is Planck's constant.

Figure III-10 shows a summary of the Werner's model applied on Richardson's equations. The sequence is completely explained featuring in grey Richardson's method, in grey-red arrow the transition from a method to another, and in red Richardson and Werner's methods.

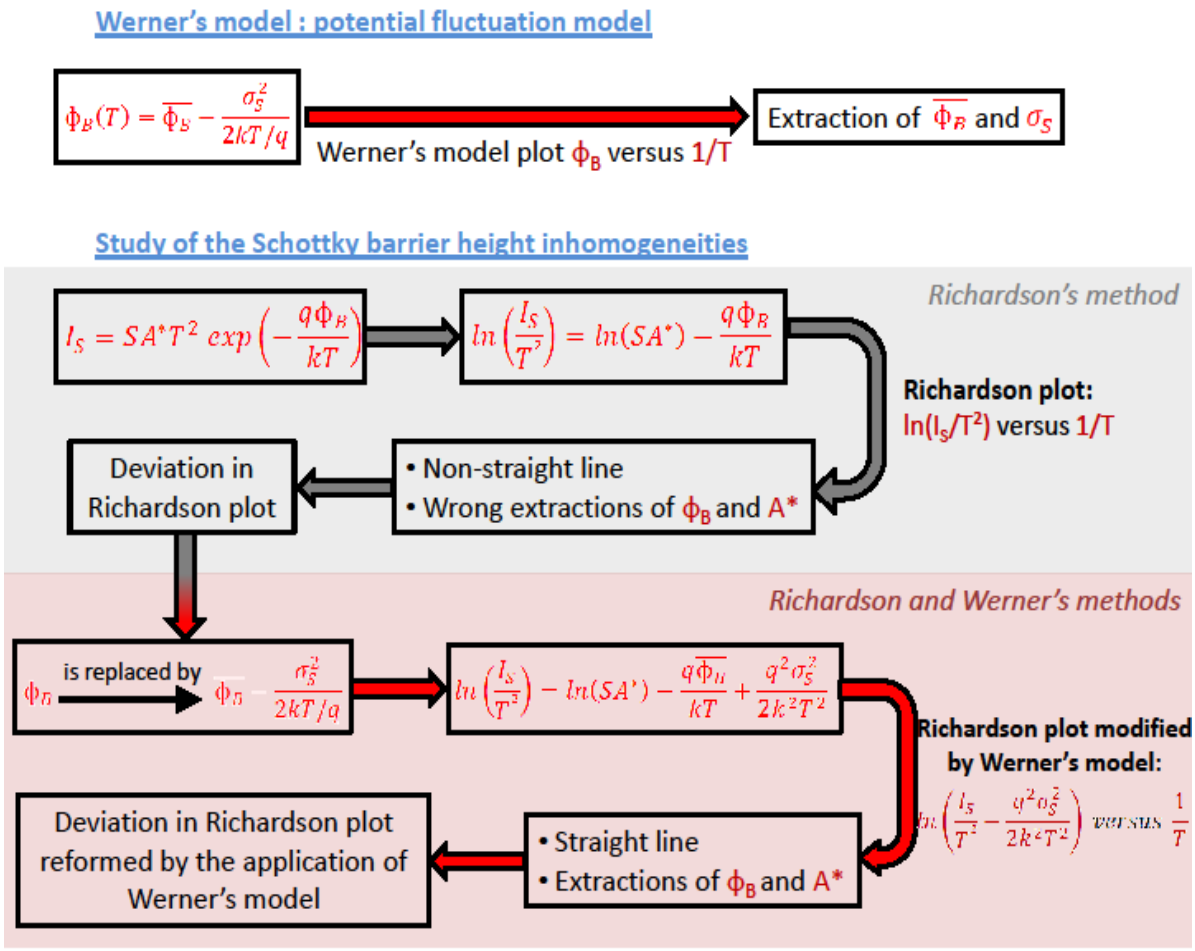


Figure III-10. Summary of Richardson and Werner model's sequence.

Electrical parameters	Device #A	Device #B
Results of the conventional Richardson method		
T range (K)	250 to 400K	250 to 400K
ϕ_B (eV)	0.6	0.7
A* ($AK^{-2}cm^{-2}$)	2.8×10^{-3}	1.3×10^{-3}
Results of our modified Richardson method by Werner's model		
T range (K)	200 to 400K	150 to 400K
$\overline{\phi_B}$ (eV)	1.1	1.2
σ_S (meV)	111	113
A* ($AK^{-2}cm^{-2}$)	29.8	42
m* (kg)	$0.25m_0$	$0.35m_0$

Table III-2. Physical and Electrical parameters of AlGaN/GaN HEMTs.

The transistors – in spite of the extrinsic difference on the gate pad connection mode – show the same behavior. Hence, the defects are localized under the gate, and the pad connection has no influence on the technological parameters (as expected), even if a difference is found on the electrical leakage signatures between the investigated devices: computed physical parameters A* and m* are very close to theoretical values.

The proposed technique represents an accurate method for extracting the technological parameters of the Schottky barrier (cf. deviation with conventional method, featuring a unrealistic Φ_B=0.6 eV barrier height). However, the amount of measurements at different temperatures and the data processing is time consuming. An exhaustive work on this proposed method is developed on **Declination_L** structures (impact of the initial conditions on the extracted values of σ_S and $\overline{\phi_B}$, impact of the '2 decades' zone, reverse analysis of the method, etc.), and results are cross analyzed between virgin and stressed devices.

III.2.3 Gate LFN characterization

The LFN measurements are largely used to track defects in semiconductor devices. These measurements are related to the carriers, and thus depend on the conduction path of the carriers. The evolution of the noise sources with application of a stress can also give information about the origin of the failure. The measurements are performed under two configurations: the Schottky diode is measured at open drain, and the transistor is investigated in the saturated region (at V_{DS}=8V). Furthermore, to remind what was stated previously, only #A devices are measured due to the resolution of the measurement bench that cannot measure low gate noise current values (below 10^{-21} A^2Hz^{-1}) such as for the low leakage current values of #B devices.

Figure III-11 shows DC current-voltage measurements of the Schottky diode (open drain) and of the transistor when V_{DS} is biased from 0 to 8V. Diode with shorted drain has also been measured and features the same trend as with open drain (with a slight increase on I_G). The study focuses on the

two extreme I_G plots extracted from our measurements (the diode alone and the transistor biased at V_{DS}=8V).

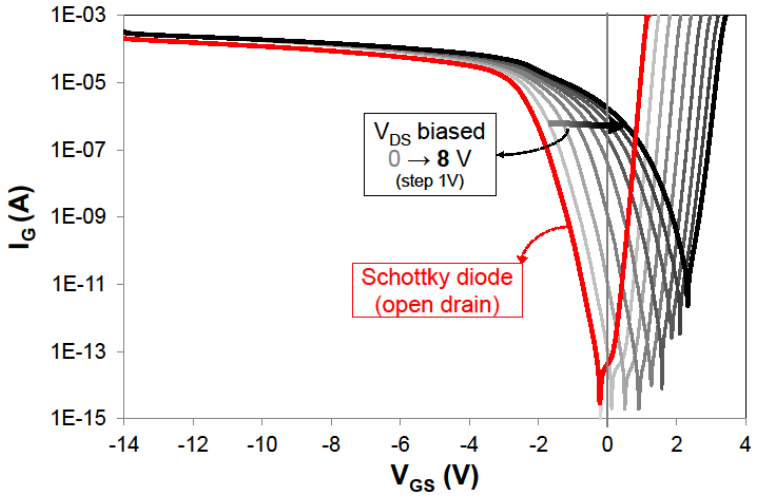


Figure III-11. DC I_G-V_{GS} gate characteristics of the Schottky diode (red solid line) and of the transistor biased from V_{DS}=0V to 8V with ΔV_{DS}=1V (grey to black characteristics).

It can be seen that the I_G-V_{GS} trends shifts towards positive V_{GS} values when the drain to gate voltage increases. The signature of the leakage current evolves for these different biasing conditions.

The measurements on the diode and on the transistor (biased at V_{DS}=8V) are performed at reverse V_{GS} values of -2V, -3V, -5V, -7V and -9V. The evolution of the gate current LFN spectra is given in **Figure III-12** for the different biases: **Figure III-12(a)** presents the measurements performed on the Schottky diode (open drain) whereas **Figure III-12(b)** illustrates the measurements on the transistor (drain biased at V_{DS}=8V). The gate noise level is sensitive to V_{GS} as I_G varies, even if the S_{IG} spectra evolution is different under these two configurations (3 decades for the diode, and 1 decade for the transistor over 7V shift on V_{GS}). **Table III-3** synthesizes the gate current values for the different V_{GS} biases under each configuration.

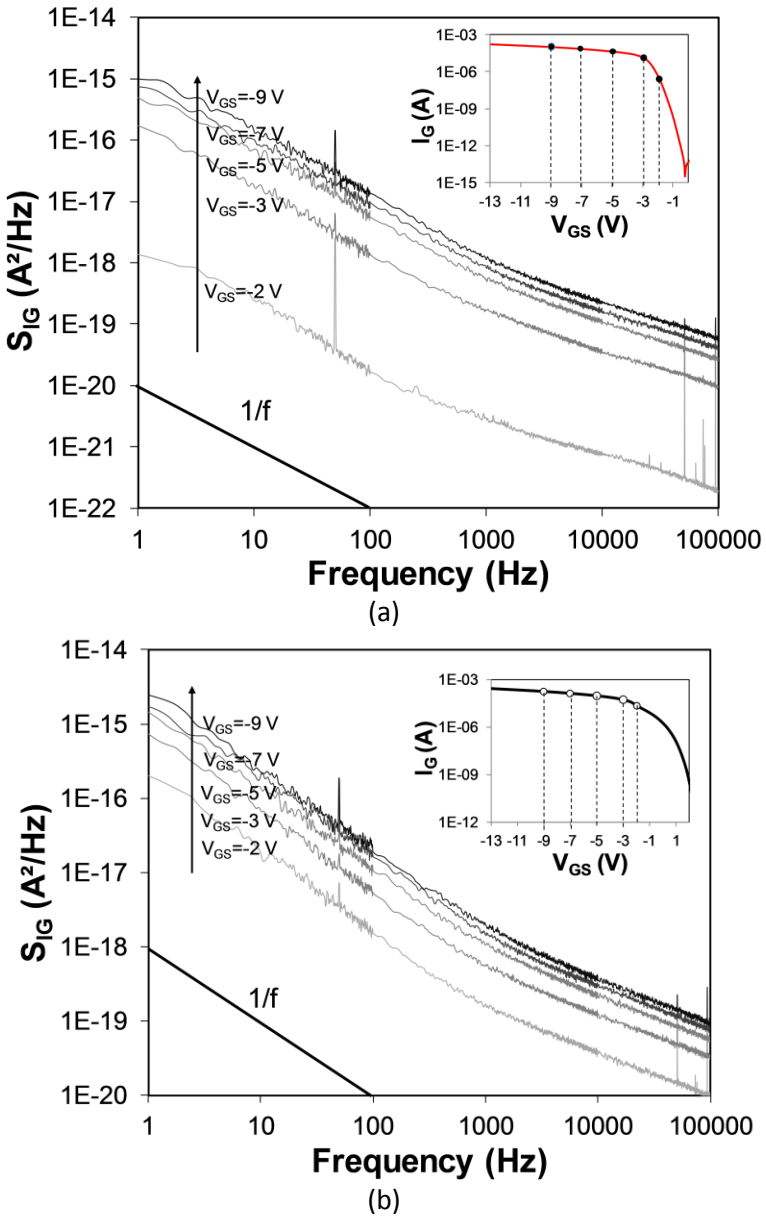


Figure III-12. Gate noise current spectral density of the AlGaN/GaN HEMT (a) of the Schottky diode (open drain) and (b) of the transistor biased in the saturation region at V_{DS}=8V. Insets: reverse gate I_G-V_{GS} characteristics featuring gate biases where S_{IG} LFN measurements are carried out.

V_{GS} (V)	**-2**	**-3**	**-5**	**-7**	**-9**
I_G (Schottky diode) (µA)	0.4	12	33	51	61
I_G (Schottky diode) (µA/mm)	**4**	**120**	**330**	**510**	**610**
I_G (Transistor at V_{DS}=8V) (µA)	17	41	68	86	106
I_G (Transistor at V_{DS}=8V) (µA/mm)	**170**	**410**	**680**	**860**	**1060**

Table III-3. Gate current values (raw and normalized values/gate width).

The measurements exhibit a 1/f trend superimposed with many generation-recombination centers: a robust analytical procedure has been developed [12] to accurately extract each noise contributors (the extraction accuracy depends on the relative weight of each noise source to the total spectra). Then the 1/f noise source can be distinguished from the many GR centers, as far as its contribution has a valuable weight to the overall S_{IG} spectra; her, up to 15 GR centers are needed to fit the S_{IG} spectra, and it is then delicate to track the magnitude and the frequency evolution of each

GR center versus V_{GS}. The raw values are then extracted at 100 Hz as presented in **Figure III-13**. An I_G power law of 1.35±0.1 is found for the diode and for the transistor.

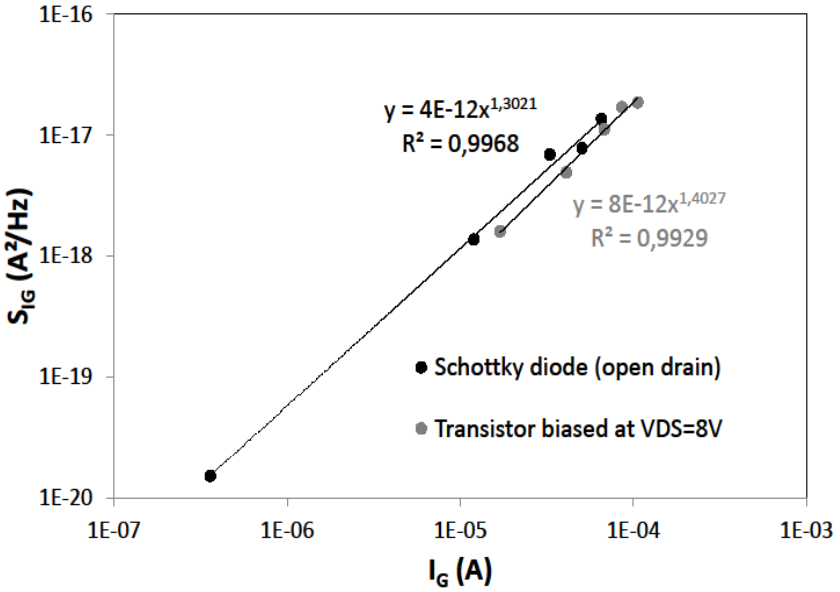


Figure III-13. Gate current noise versus gate current for the Schottky diode (-9V≤V_{GS}≤-2V, black plots) and for the transistor (V_{DS}=8V, 9V≤V_{GS}≤-2V, grey plots).

Since it is found that the S_{IG} spectra depends on a power law of $I_G^{1.3}$, thus the gate current spectral density can be normalized as $S_{IG}/I_G^{1.3}$ as shown in **Figure III-14**. The identical signature observed for the diode (-9V≤V_{GS}≤-5V) and for the transistor (-9V≤V_{GS}≤-2V) can be imputed to the same noise sources, and thus to the same path for the electrons within gate to source (or drain) accesses (same signature, even for the GR centers above 1 kHz). The leakage current responsible for I_G is of the same nature for the diode (under high reverse biases) and for the transistor (regardless the gate bias and at V_{DS}=8V). Moreover, as the presented device has a field-plate structure, devices without field-plate have also been measured and have shown the same current law of $I_G^{1.3}$ dependency for the diode and for the transistor under the same biasing conditions. Hence, the field plate did not show any impact on the gate LFN measurements.

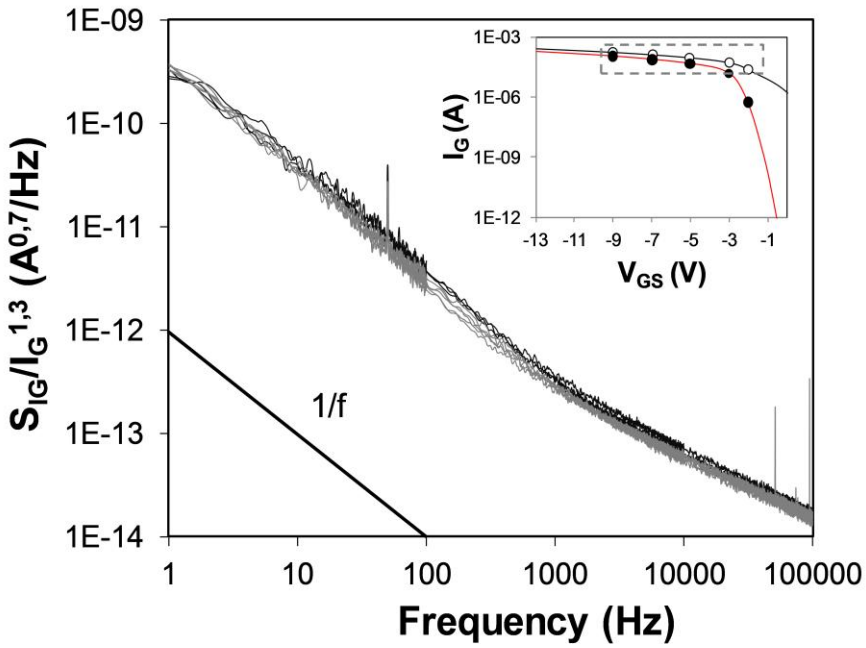


Figure III-14. Normalized gate noise current spectral density $S_{IG}/I_G^{1.3}$ for the Schottky diode (-9V≤V_{GS}≤-5V, black plots) under high reverse bias, and for the transistor (V_{DS}=8V, 9V≤V_{GS}≤-2V, grey plots).

A study has been performed on the dependence of the gate low frequency noise versus the leakage current for the reverse and forward biasing of the Schottky diode (both for the diode alone and for the transistor). It is found that the defects have specific current laws dependency considering the biasing condition (thus revealing noise mechanisms of different nature, with different impact considering the biasing operating mode). This part of the work will not be presented in this document, even if available in the reports of REAGAN project.

For these devices, V_{GS}=-3V stands as knee value between two (or more) conductions mechanisms: the noise spectra S_{IG} of the Schottky diode measured between -3V≤V_{GS}≤0 do not fit the $I_G^{1.3}$ power law anymore: other mechanisms are engaged leading to a change on the gate current origin. In this biasing zone, the GR centers and the 1/f noise of S_{IG} spectra are featuring non monotonic behavior, revealing a change in the path of the carriers or in the conduction mode through the gate (also confirmed by the fit of I_G-V_{GS} versus analytical models) [13]. According to Zhang *et al*. [14], a leakage current model could be extracted, explaining the contribution of each mechanism. Next, is presented the analytical approach of the model but it is not applied on our devices yet; a modeling has been tested using models without satisfactory results. Studies are still ongoing to develop a model able to fit each part of the I_G-V_{GS} curves for a wide range of temperature. This model is also studied on the DC I_G-V_{GS} measurements versus temperature where the low temperatures present a different conduction mechanism than the higher temperatures to that under forward biasing conditions where the tunneling is the dominant source of the current flow. The current density is given by the Fowler-Nordheim tunneling expression [14]:

$$J = AE_b^2 \exp\left(-\frac{B}{E_b}\right) \qquad (12)$$

$$A = \frac{q^2\left(\frac{m_e}{m_n^*}\right)}{8\pi h \phi_B} = 1.54 \times 10^{-6} \frac{\left(\frac{m_e}{m_n^*}\right)}{\phi_B} \quad \left(\frac{A}{V^2}\right) \tag{13}$$

$$B = \frac{8\pi\sqrt{2\left(\frac{m_e}{m_n^*}\right)(q\phi_B)^3}}{3qh} = 6.83 \times 10^7 \sqrt{2\left(\frac{m_e}{m_n^*}\right)(q\phi_B)^3} \quad \left(\frac{V}{cm}\right) \tag{14}$$

where E_b is the electric field in the semiconductor barrier, q is the electron charge, me is the free-electron mass, m_n* is the conduction band effective mass in the semiconductor, h is Planck's constant and ϕ_B is the effective barrier height at the Schottky contact. By plotting J/E_b^2 versus $1/E_b$ in the low temperature (below 150K for example), the y-intercept and the slope allows extracting A and B (hence the barrier height). Eq. 12 shows the slope is independence of the temperature and the superposition of the plots will confirm this theoretical equation. At higher temperatures, Frenkel-Pool emission refers to electric field enhanced thermal emission from a trap state into a continuum of electronic states; the current densities associated with the Frenkel-Pool emission are given below [14]:

$$J = CE_b \exp\left[-\frac{q\left(\phi_t - \sqrt{\frac{qE_b}{\pi\varepsilon_0\varepsilon_s}}\right)}{kT}\right] \tag{15}$$

where Eb is the electric field in the semiconductor barrier at the M-SC interface, ϕt is the barrier height for the electron emission from the trap state, εs is the relative dielectric permittivity at high frequency, T is the temperature, ε0 is the permittivity of free space, and k is Boltzmann's constant. Log(J/Eb) is the relevant parameter for the Frenkel-Pool emission, hence Eq. 15 becomes:

$$log\left(\frac{J}{E_b}\right) = \frac{q}{kT}\sqrt{\frac{qE_b}{\pi\varepsilon_0\varepsilon_s}} - \frac{q\phi_t}{kT} + logC = m(T)\sqrt{E_b} + b(T) \tag{16}$$

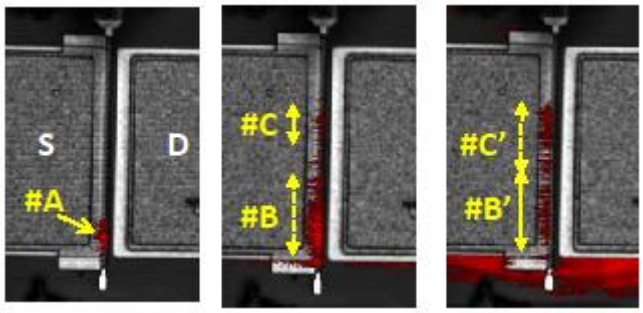
where $m(T) = \frac{q}{kT}\sqrt{\frac{qE_b}{\pi\varepsilon_0\varepsilon_s}}$ and $b(T) = -\frac{q\phi_t}{kT} + logC$

m(T) and b(T) functions can be plotted versus 1/T. These plots allow extracting the relative dielectric constant εS and the emission barrier height ϕt for the diode under study.

Thus, it can be concluded that under reverse biasing conditions, the two processes governing the reverse gate leakage current conduction mechanisms are the Fowler-Nordheim and Frenkel-Pool emissions.

III.2.4 OBIRCh results on Declination_S devices

As stated previously, the OBIRCh measurements reveal resistivity fluctuations in the active irradiated area using a laser beam that induces thermal changes in the device. The wavelength of the laser used in this study is 1.34µm. An increase in the current is revealed by the presence of red spots in the irradiated area of the device [15] [16]. These spots highlight the zones where the current passes. Results of OBIRCh method on AlGaN/GaN HEMTs are presented in **Figure III-15**. These measurements have been performed by Dominique Carisetti (TRT), according to the biasing conditions used for the LFN measurements.



(a) V_{GS}=-3V (b) V_{GS}=-5V (c) V_{GS}=-9V

Figure III-15. OBIRCh measurements between gate and source regions of the transistor: the Schottky diode is biased at V_{GS}=-3, -5 and -9V.

Figure III-15 features only red spots, and so only resistivity fluctuations are identified in the semiconductor layers. A spot revealing a very local current path at the end of the gate width can be observed in **Figure III-15(a)** (#A for V_{GS}=-3V, also visible at -4V). This spot is spread at V_{GS}=-5V (#B) and another one appears closer to the end of the gate toward the gate pad in the upper part of the picture (#C). As for V_{GS}=-9V and when the gate current increases, #B spreads homogeneously and #C conduction zone increases (see #B' and #C' in **Figure III-15(c)**) [13].

Figure III-15 is a schematic illustration of the HEMT under study representing where the gate leakage current flows. The location where OBIRCh measurements are carried out is indicated with red spots. Wg is the gate width **Figure III-15** wherein the laser beam irradiates. From our measurements, it can be assumed that:

- The current path (surface, vertical, or lateral leakage mechanisms) occurs in the same regions for the two configurations (between G-S for the diode or between G-S and G-D for the transistor).
- Moreover, whatever the gate current value (under the proposed V_{GS} ranges), and both for the diode and for the transistor, the noise spectral density evolves with an $I_G^{1.3}$ current law (the noise contributors are the same). These signatures can be partially correlated with the presence of very local current paths revealed by OBIRCh technique.

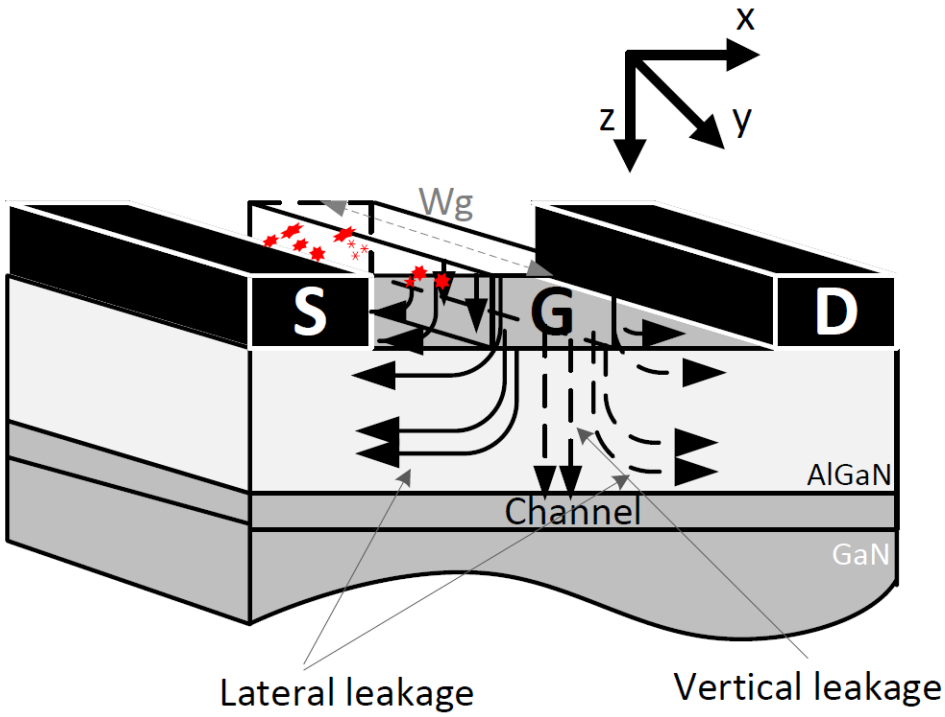


Figure III-16. Illustration of the HEMT AlGaN/GaN structure representing the vertical and lateral gate leakage current paths for the Schottky diode (solid lines) and for the transistors (gate-source diode solid lines and gate-drain diode dashed lines). The red spots illustrate the presence of very local current paths detected by OBIRCh technique.

III.2.5 Mechanical and piezoelectrical stresses in the devices

This part of interpretation of the work has been proposed to the project community, and closely discussed with Michel Mermoux (LEPMI). It is assumed that the LFN measurements of defects as well as the OBIRCh spot locations can be the manifestation of piezoelectric effects along the gate width at first order when the electrical field evolves with V_{GS}. Strong indications are found that generation of piezoelectric strain under the gate edge might be the cause of performance degradation of the GaN based transistors. Generation of piezoelectric strain can lead to the creation of defects that can act as traps for electron transport [17] [18]. Under bias, this additional strain will superimpose on the mechanical stresses already present in the device. Those stresses - developed in materials - are due to multiple physical phenomena including lattice mismatch, differences in the coefficient of thermal expansion (CTE), and residual (mostly process-induced) stresses. These residual stresses develop as a consequence of the processing schemes used during device fabrication. Thus, it seems of importance to measure, or at least estimate, the different sources of stresses in order to further refine both the capability and overall device lifetime. Of course, full quantification and analysis of the stress distribution require investigation of each of the contributions that give rise to the total load placed on the device.

Because of the wurtzite properties of the GaN and AlGaN structures, an applied voltage, i.e. an electric field, results in the so-called converse piezoelectric effect generating strain in the device. Strain (ε_i) in a device generated by an applied electric field (E_k) can be expressed as [19]:

$$\varepsilon_i = S_{ij}\sigma_j + d_{ik}E_k \qquad (17)$$

where σ_j is the stress tensor, S_{ij} are the elastic compliance tensor components and d_{ik} are the piezoelectric moduli with i, j = 1 to 6 = xx, yy, zz, yz, zx, xy and k = 1 to 3 = x, y, z. Here, the z axis is along the normal to the device surface, i.e. along the c-axis of the wurtzite structure, the x axis points from the device source to the drain contact parallel to the device surface, the y axis is chosen along the gate contact width to form a right-handed coordinate system (**Figure III-16**). In the wurtzite crystal structure, there are only three independent non-zero coefficients in the piezoelectric moduli dij (d_{31}, d_{33} and d_{15}) and five independent non-zero coefficients in the elastic compliance tensor components Sij (S_{11}, S_{12}, S_{13}, S_{33} and S_{44}). Therefore, the strain can be written using Eq. 17 as:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} S_{11}\sigma_{xx} + S_{12}\sigma_{yy} + S_{13}\sigma_{zz} + d_{31}E_z \\ S_{12}\sigma_{xx} + S_{11}\sigma_{yy} + S_{13}\sigma_{zz} + d_{31}E_z \\ S_{13}\sigma_{xx} + S_{13}\sigma_{yy} + S_{33}\sigma_{zz} + d_{33}E_z \\ S_{44}\sigma_{yz} + d_{15}E_y \\ S_{44}\sigma_{zx} + d_{15}E_x \\ 2(S_{11} - S_{12})\sigma_{xy} \end{pmatrix} \quad (18)$$

From Eq. 18, it can be seen that the vertical component of the electric field E_z will affect the principle strain components while the horizontal E_x field component in the device will generate a shear component in the *zx*-plane.

The extent of the coupling between pure mechanical strain the electric field-induced one will depend in part on the Al mole fraction and the electric field in the layers. The complete problem is quite complicated to solve, and this is beyond the scope of the present work, but orders of magnitude can be considered. Strains in similar devices were evaluated with Raman spectroscopy. Small frequency shifts of particular phonon modes, the non-polar E2 mode in particular, are related to strain or stress via phonon deformation potentials, and the peak positions exhibit a linear shift with stress or strain. Using acquisition conditions similar to those described in [20] [21], a visible excitation wavelength in particular, the whole GaN layer is probed, but the thin AlGaN layer is not seen. Two main sources of mechanical stress could be identified: local micro-strains due to the presence of dislocations in the GaN layer, and a rather high tensile strain in the source-gate (source-drain) area which is most probably induced by the Ohmic contacts and by the application of a voltage in the gate-source (gate-drain) zone. This tensile strain leads to a downshift of the E2 line of about 0.4 cm^{-1}, translating a more or less uniaxial stress of about 300 MPa in the active area of the device.

A few studies were devoted to the estimation of the stress in the GaN layer induced by the reverse piezoelectric effect, with the aid of Raman spectroscopy [20] [21]. In all cases, upshifts of the GaN E2 mode of about 0.3 - 0.4 cm^{-1} are reported for applied V_{DS} voltages of about 40-50V. Moreover, the magnitude of the experimentally obtained stress was always about ten times higher than that estimated from simulations [20]. Thus, the effects of the piezoelectric and the pure mechanical stresses may be of similar amplitudes, but of opposite signs. Moreover, under strong bias, we can expect a strong E_x component of the electric field, of the order of some $MVcm^{-1}$. Clearly, this component will contribute to induce strong shear strains, which will add up to those induced by purely mechanical effects, in particular in the vicinity of all geometrical singularities, in particular along the edges of the Schottky and Ohmic contacts. These shear stresses, often neglected, can be

strong enough to induce dislocation gliding, or even to create new defects, for example, pits and cracks as shown in reference [18].

As the electrical and low frequency noise measurements have shown reversible signatures, it can be assumed that the strain is elastic, and the defects are released when the bias returns to low $\|V_{GS}\|$ values. However, for long period stresses such as HTRB (High Thermal Reverse Bias), the micro-strains due to dislocation could evolve to a permanent degradation mode. This last point has been evidenced on other stressed structures but is not discussed in the present work.

III.2.6 EBIC results on Declination_S devices

The objective of this section is to introduce the EBIC technique developed at DGA/IS since 2011. The results obtained on **Declination_S** devices are also presented simultaneously taking into account electrical characterization, defect localization and physical analysis.

III.2.6.a EBIC technique

EBIC was introduced in 1970's as a useful scanning electron microscope (SEM) technique for semiconductors which allows the direct observation of charge depletion regions and electrically active defects like dislocations, leakage or local breakdown [23]. It is also used for the measurement of the minority carrier diffusion length.

The electron hole pairs generated in the beam interaction volume of a semiconductor during SEM inspection by the primary electron beam can be separated if the device exhibits a p-n junction or a Schottky junction. The internal field inside the depletion layer will drift the electron and the holes in an opposite direction. Thus, an EBIC signal is generated and measured by connecting the 2 diode electrodes to a specific current amplifier designed for operating with very small currents induced by the sample. As the output of the current amplifier is used as the imaging signal, the EBIC signal can be mapped to provide information by the images contrast thanks to spatial variations in the internal electrical field. So, abnormal local recombinations lead to dark spots (like dislocations) and local extra emissions to bright spots. Generally, to appreciate the junction quality, the EBIC signal homogeneity is evaluated: a big spot will localize a big defect.

A Design of Experiments (DoE) has been made to select the most relevant parameters for a good EBIC image: acceleration voltage, beam current (around 400pA), number of pixels (generally 2048 x2048), pixel dwell time (40µs), gain/sensitivity (10^3/10^6) of the amplifier. The acceleration voltage of the primary electron gun is one of the most important parameter to adjust depending on the Device under test topology and construction. It must be high enough to allow the electron penetration through the top layers of the device (passivation, gate metallization) up to the interest area, which is the charge depletion zone of the Schottky diode. But the acceleration voltage must not be too high because of a possible EBIC saturation (blooming) which is detrimental to good defect localization.

III.2.6.b EBIC results on Declination_S devices

Complete EBIC experiments are made on **Declination_S** devices without field plate for which a large number of transistors are observed in order to get statistical correlation between EBIC signatures and gate leakage current levels. The devices under test are not those used for electrical characterization and low frequency noise measurements. A trend is observed only on a few cases with large leakage current: the more the intensity of EBIC signal is (or the number of EBIC spots along the gate), the more the leakage gate current is (**Figure III-18**). The second conclusion is related to the heterogeneity of these EBIC gate signatures as shown in **Figure III-17** that is related to few nanovoids inside the gate metallurgy for the most important EBIC spots. The gate metallurgy is indeed investigated using TEM and HAADF STEM conjugated to EDX analysis. Classical cross sections and longitudinal views are achieved showing that nanovoids develop from the Ni/GaN interface and confine within the Nickel barrier layer (**Figure III-19(a)** and **19(b)**).

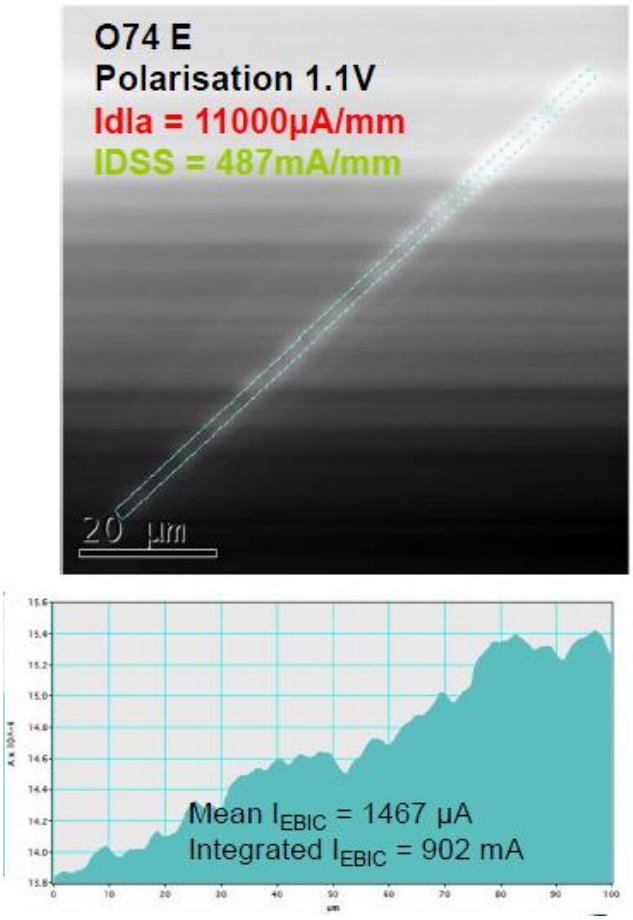


Figure III-17. Inhomogenous EBIC signature.

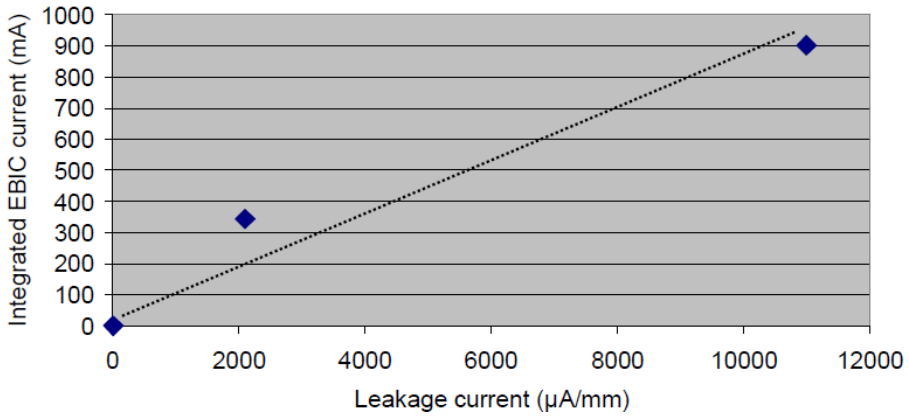


Figure III-18. Example of correlation between large gate leakage current variation and EBIC signature.

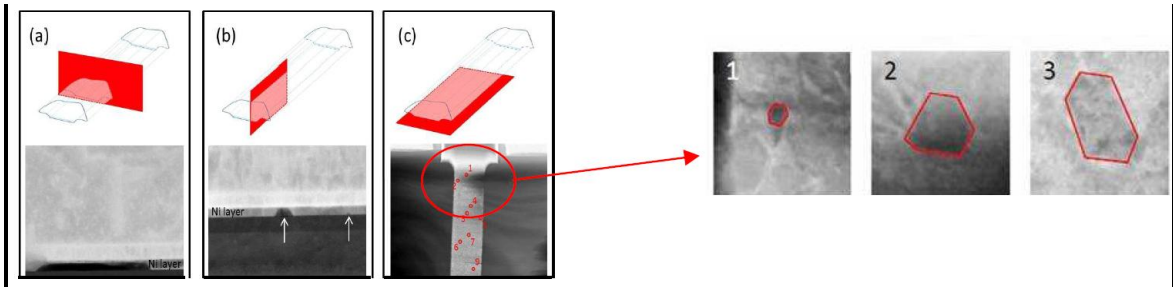


Figure III-19. (a) cross section, (b) longitudinal and (c) plane view of HAADF STEM images showing nanovoids developing within the Ni barrier layer which revealed only on the leakiest devices.

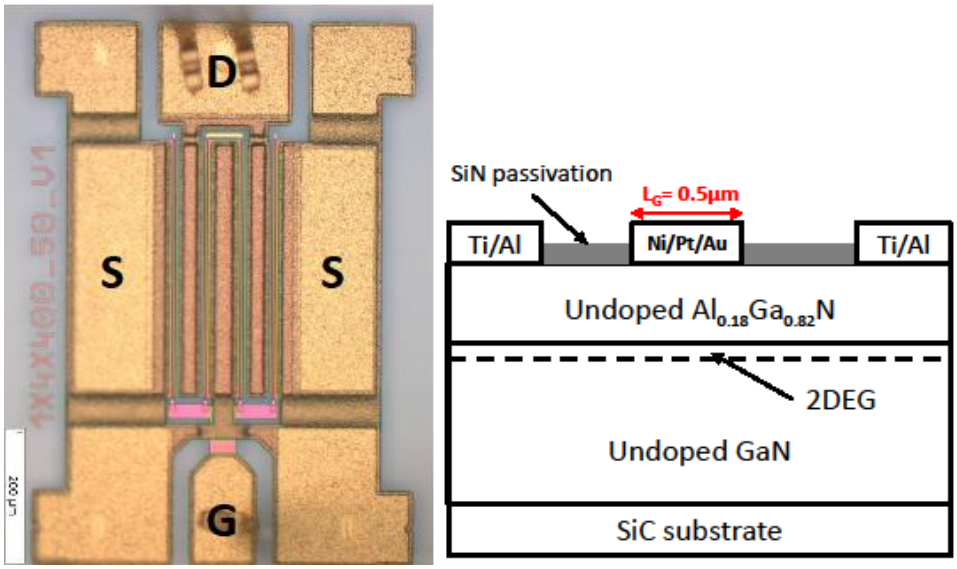
A new method for plane view extraction of the Ni layer is also developed by SERMA Technologies under ReAGaN ANR project. In particular, it has been identified from this plane view dark regions exhibiting grain boundary-like shapes with dimensions varying from 10 nm to 100 nm (**Figure III-19(c)**). EDX spectra (not shown) performed in these dark regions confirm Ni-free composition thus unambiguously demonstrating the presence of nanovoids within the Ni barrier. In opposition to previous cross section and longitudinal views, the plane view allows retrieving spatial distribution and surface density of voids within the Ni layer as well.

It can be assumed that nanovoids reduce the barrier height and are the preferential sites for trapping effects just inside the semiconductor near to the interface, so RF instabilities and reliability concerns.

III.3 GH50 Declination_L: packaged devices

III.3.1 Devices under test

The **Declination_L** devices present the same fabrication process as the **Declination_S** devices. The difference between both technologies is that the **Declination_L** are not research level devices and they are from the commercial declinations of UMS. Moreover, these devices are packaged and present have 4 gate fingers with a width of 400µm and a length of 0.5µm (4×400µ×0.5µm), thus bigger devices, and thus feature higher power and higher drain current. **Figure III-20** shows a picture of these transistors featuring the 4 gate fingers. Two declinations are proposed for these devices #NL ('non leaky') and #L ('leaky') featuring difference at their gate leakage current level; this difference can be observed on the gate current measurements proposed next. Furthermore, the #NL devices are submitted to an HTOL stress of 10000 hours at V_{DS}=50V, I_{DS}=160mA (100mA/mm) at 25°C. **Table III-4** synthesizes all the set of devices received to the date from UMS with their conditions. The studies are still ongoing on Nanowatt_311_GH50 and Picowatt_B_GH25 sets.



(a) (b)

Figure III-20. AlGaN/GaN HEMTs under test.
(a) Top view of the device under test (4 gate fingers).
(b) Tranversal schematic illustration of the mono-finger device.

Lot nickname	Technology	Dimensions	Devices	Substrate	Stress type
Declination_S	GH50	1x100µmx0.5µm	On wafer	SiC	HTOL
Declination_L	GH50	4x400µmx0.5µm	Packaged EGIDE	SiC	Unstressed
Nanowatt_311	GH50	4x400µmx0.5µm	Packaged EGIDE	SiC	HTOL
Picowatt_B	GH25	-	Packaged EGIDE	SiC	Unstressed

Table III-4. Devices under test by LAAS – CNRS during ReAGaN ANR project. [1]

III.3.2 Electrical characterization versus temperature

The electrical characterisation versus temperature on these devices was quite complicated since they are not on wafer, and they are packaged devices. Hence, this difference required some replacements on the Cryoprober. **Figure III-21** shows a top view picture of the Cryoprober station's

chuck when the devices were connected. The thermal paste is inserted under the device and under the package for better thermal conduction. The measurements are performed using the same biasing conditions as for Humblodt_18 devices.

Figure III-21. Top view picture of the chuck of the Cryoprober station where the **Declination_L** devices are connected in two different configurations:
(a) Open drain configuration for the study of the Schottky diode (present work).
(b) Drain biased: where the drain access is connected (saturated behavior study, future work).

The I_G-V_{GS} measurements shown in **Figure III-22** are performed on the devices under open drain configuration and when the temperature varies from 100K to 400K. Two devices are tested featuring high and low gate leakage currents: #NL with an I_G of 265 µAmm^{-1} and #L with an I_G of 855 µAmm^{-1} at V_{DS}=50V and V_{GS}=-7V.

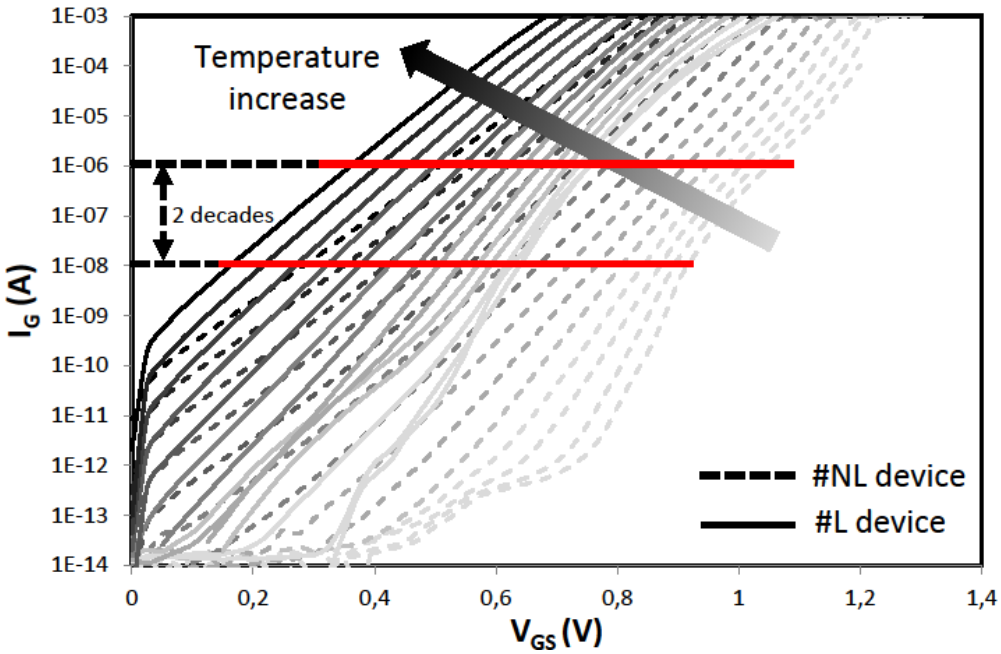


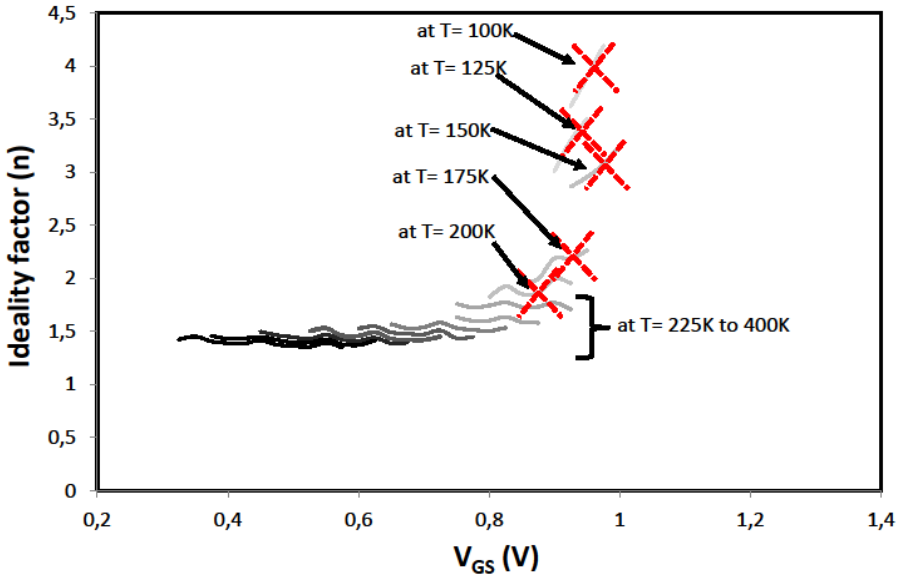
Figure III-22. Forward gate current-voltage characteristics of AlGaN/GaN HEMTs, open drain configuration versus temperature ranging from 100K to 400K.

The study presented next is identical to that detailed for **Declination_S** devices in the previous section.

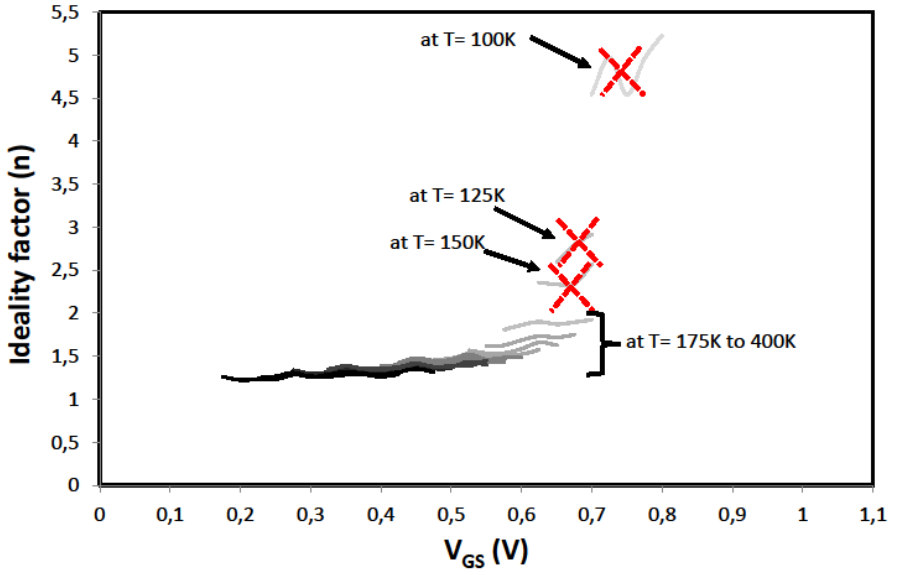
III.3.2.a Electrical parameters extraction

III.3.2.a.1 Ideality factor dependence of forward bias

The study is performed on a constant current range of two decades (10^{-8}A to 10^{-6}A) where the I-V-T characterisitics can be fitted. The ideality factor (n) variations versus the applied voltage (V_{GS}) must show a quasi-constant value of n when V_{GS} varies. **Figure III-23** shows these variations for the non-leaky (#NL in **Figure III-23(a)**) and for the leaky (#L in **Figure III-23(b)**). The large variation of the ideality factor at 100K to 200K for #NL have no physical sense and are excluded from the study (also at 100K, 125K and 150K for #L) presented in the next paragraphs. Hence, the best fitting and analysis of the data are in the temperature ranges of 225K-400K for #NL and 175K-400K for #L.



(a) Device #NL



(b) Device #L

Figure III-23. Ideality factor (n) versus forward bias (V_{GS}) for devices #NL and #L within a constant current range of two decades. The red deletions indicate which measurements have to be excluded from the study.

III.3.2.a.2 Ideality factor and Schottky barrier height dependence of the temperature

The electrical parameters (the SBH and the ideality factor) are also extracted following the Eqs. 1 and 2 and presented in **Figure III-24** and **Figure III-25**. An increase in the SBH and a decrease in the ideality factor are observed when the temperature increases. These variations stand as early indicators of barrier inhomogeneities.

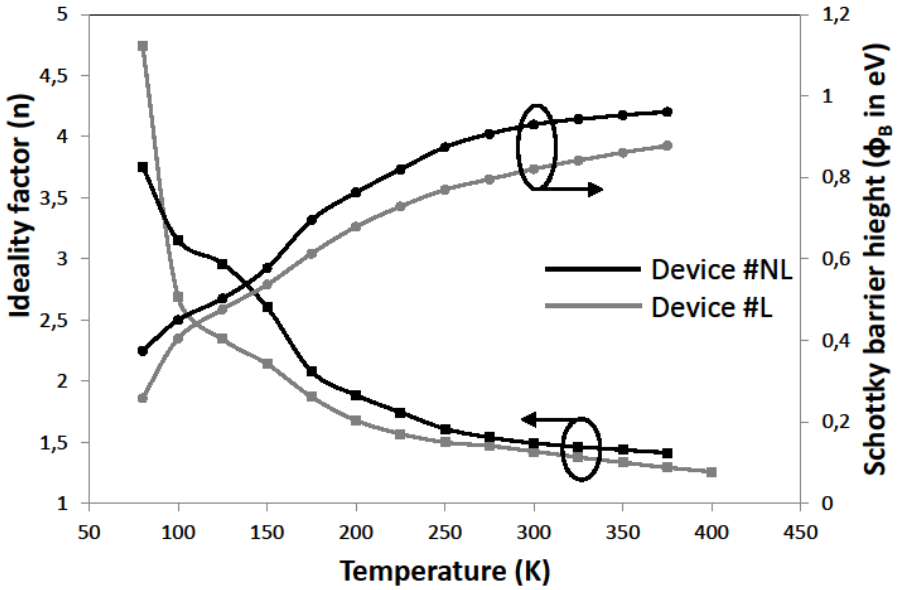


Figure III-24. Temperature dependence of the ideality factor (n) and Schottky barrier height for devices #NL and #L (with black and grey plots respectively).

Similarly to the **Declination_S** devices, the SBH of the **Declination_L** devices becomes smaller as the ideality factor increases. This phenomenon is represented in **Figure III-25**. Plotting ϕ_B versus n allows to extract the barrier heights for an ideal study case (considering n=1) of the Schottky diode. The extracted values of the SBH at n=1 are 1.13eV for #NL, and 1eV for #L.

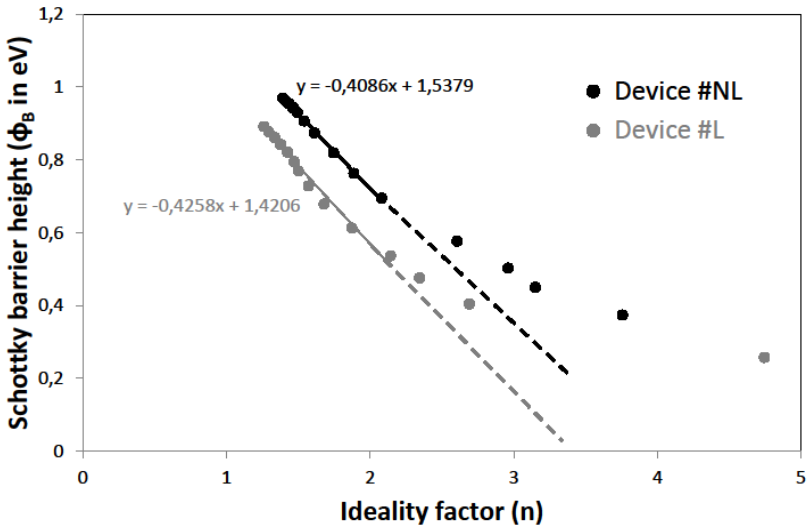


Figure III-25. Schottky barrier height versus ideality factor for devices #NL and #L (black and grey plots resp.) featuring the equations of the trends for each device.

III.3.2.b Potential fluctuation model application

The application of the model explained in the previous paragraph for the **Declination_S** devices is synthesized in **Figure III-26** since it is the same procedure followed for **Declination_L** devices [5]:

- The potential fluctuation plot allows extracting the mean value of the barrier height and the standard deviation (**Figure III-27**).

- The grey part of the figure explains the invalidity of the Richardson model and the necessity to integrate Werner's model to extract the values of the Schottky barrier height and effective Richardson constant in good agreement with the theoretical values (**Figure III-28**).
- The red part of the figure shows the correct method to extract the barrier height and the effective Richardson constant and this can be performed only by combining the Werner's model in Richardson's one (**Figure III-28**).

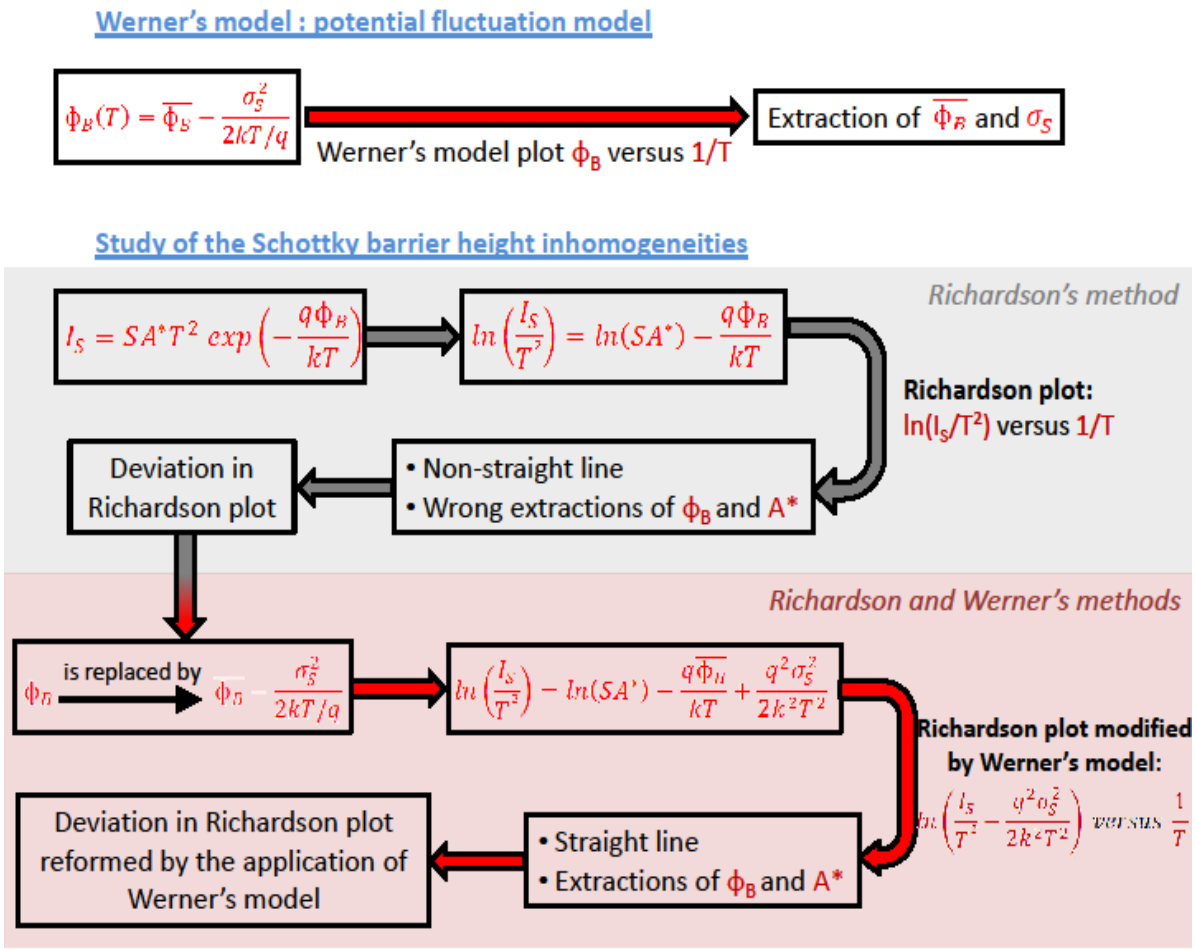


Figure III-26. Summary of Richardson and Werner model's sequence.

The extracted parameters are presented in **Table III-5**: It can be noticed how the SBH is higher for the non-leaky device in comparison with the leaky device. The effective Richardson constant is closer to the theoretical value (32 $AK^{-2}cm^{-2}$) for #NL (29 $AK^{-2}cm^{-2}$) than for #L (23 $AK^{-2}cm^{-2}$) devices. All these physical parameters confirm the leaky nature of #L and the impact of the barrier height with the gate conduction mechanisms. Moreover, the standard deviation seems to increase with the leakage current for the two virgin devices. This should confirm that the leakage current level is higher when the density of inhomogeneities increases (higher σ_s value of +10meV for the virgin leaky device).

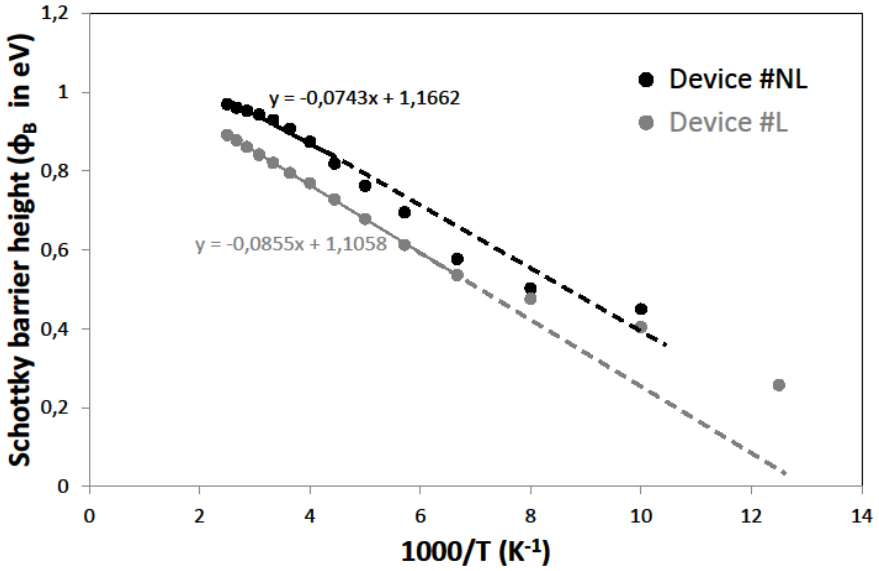


Figure III-27. Schottky barrier height calculated from I-V-T measurements versus 1/T for devices #NL and #L (in black and grey plots resp.).

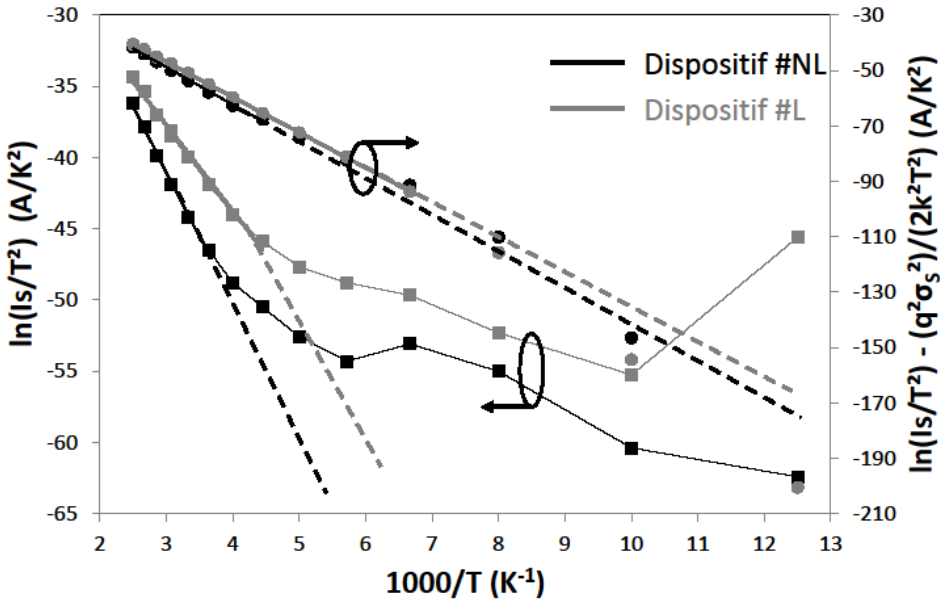


Figure III-28. Conventional and modified Richardson plots of AlGaN/GaN HEMTs.

- Conventional Richardson plots with the y-axis on the left.
- Modified Richardson plots by Werner's model with the y-axis on the right.

Device #NL: black lines and dots.
Device #L: grey lines and dots.

Electrical parameters	Device #NL	Device #L
Results of the conventional Richardson method		
T range (K)	225 to 400K	225 to 400K
ϕ_B (eV)	0.65	0.52
A* ($AK^{-2}cm^{-2}$)	1.33×10^{-3}	3.8×10^{-4}
Results of the modified Richardson method by Werner's model		
T range (K)	225 to 400K	175 to 400K
$\overline{\phi_B}$ (eV)	1.2	1.1
σS (meV)	113	121
A* ($AK^{-2}cm^{-2}$)	29	23
m* (kg)	$0.24m_0$	$0.2m_0$

Table III-5. Physical and Electrical parameters of AlGaN/GaN HEMTs from **Declination_L** device's set.

The study of the Schottky barrier height homogeneity is also performed on the non-leaky stressed devices. **Table III-6** synthesizes the results obtained on the same current range (10^{-8}A to 10^{-6}A) on three non-leaky stressed devices by HTOL stress during 10000 hours (#NL_S1, #NL_S2 and #NL_S3). The mean barrier height is in close agreement with the unstressed device and with the theoretical values. It can be concluded that the HTOL stress has no impact on the mean Schottky barrier height. However, the standard deviation for these stressed (non-leaky) devices does not follow the previous trend between leaky and non-leaky virgin devices. Here, a linear trend for the 3 stressed devices show a decrease on the standard deviation (better homogeneity) when the leakage current increases: then the correlation between the leakage current level and the inhomogeneity of the Schottky barrier height does not apply on stressed devices. Moreover the meanings of the Richardson constant and of the effective mass still have to be investigated in future works.

Electrical parameters	Device #NL_S1	Device #NL_S2	Device #NL_S3
Results of the conventional Richardson method			
T range (K)	250 to 400K	300 to 400K	250 to 400K
ϕ_B (eV)	0.57	0.58	0.58
A* ($AK^{-2}cm^{-2}$)	1.06×10^{-4}	5.84×10^{-4}	1.21×10^{-4}
Results of the modified Richardson method by Werner's model			
T range (K)	175 to 400K	150 to 400K	150 to 400K
Leakage current (µA/mm) (at V_{GS}=-9V and T=300K)	12.8	7.2	3.7
$\overline{\phi_B}$ (eV)	1.2	1.3	1.27
σ_S (meV)	123	146	135
A* ($AK^{-2}cm^{-2}$)	31	30	37
m* (kg)	$0.25m_0$	$0.25m_0$	$0.31m_0$

Table III-6. Physical and Electrical parameters of AlGaN/GaN HEMTs from **Declination_L** stressed device's set.

Moreover, **Figure III-29** shows the I_G-V_{GS} measurements between 10^{-8}A to 10^{-6}A at 250K, 300K and 400K for #NL_S1, #NL_S2 and #NL_S3 devices. It can be noticed that the standard deviation

presented in **Table III-6** for the three devices decreases when the gate leakage current increases: the defects at the M-SC interface decrease when more current is flowing. Then it can be supposed that the leakage mechanisms cannot be related to the defects revealed by the proposed method. However, this method stands as a good indicator of the quality of the Schottky contact and can be exploited to check the process maturity of this technological step.

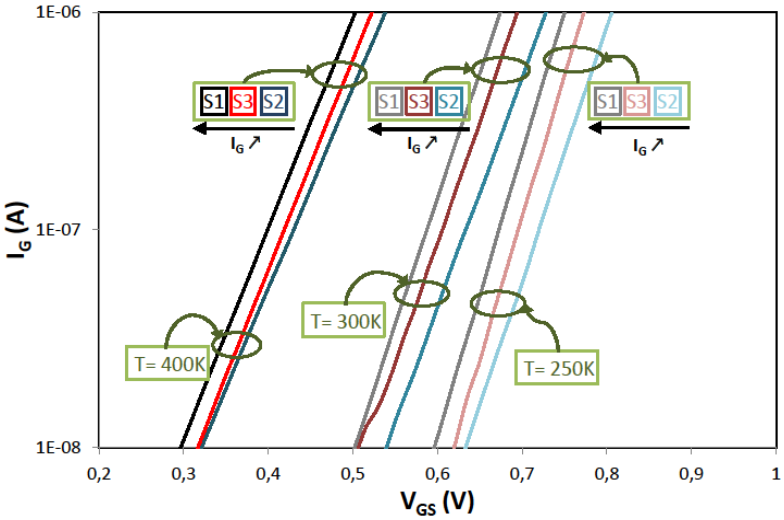


Figure III-29. DC I_G-V_{GS} measurements between 10^{-8}A to 10^{-6}A at 250K, 300K and 400K for #NL_S1, #NL_S2 and #NL_S3 devices.

III.3.2.c Study of different current ranges

Only a single current range is presented in the previous paragraphs. However, this paragraph presents results on different current ranges of two decades on #NL and #L devices. **Figure III-30** shows the I_G-V_{GS} measurements of #NL and #L devices featuring the three current ranges studied: R1 (10^{-11}A to 10^{-9}A), R2 (10^{-9}A to 10^{-7}A) and R3 (10^{-7}A to 10^{-5}A).

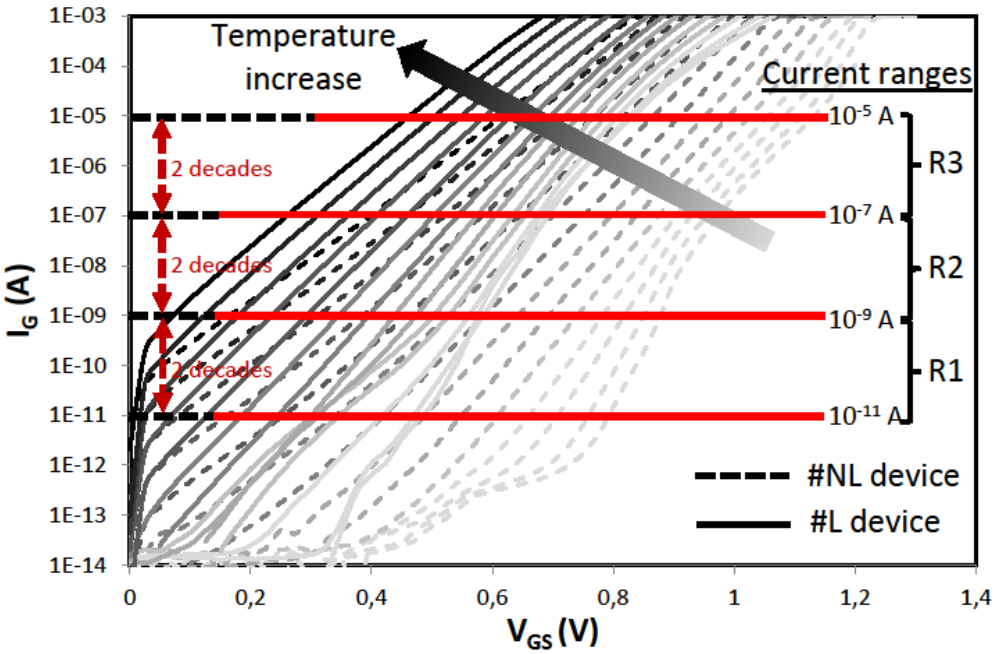


Figure III-30. Forward gate current-voltage characteristics of AlGaN/GaN HEMTs, open drain configuration versus temperature featuring the three current ranges (R1:10^{-11}A to 10^{-9}A, R2:10^{-9}A to 10^{-7}A and R3:10^{-7}A to 10^{-5}A) where the SBH homogeneity is studied.

Table III-7 and **Table III-8** synthesize the results obtained on these three current ranges (R1, R2 and R3) for #NL and #L devices respectively. The mean barrier height, the effective Richardson constant and the effective mass are closer to the theoretical values for the non-leaky device more than for the leaky device, regardless of the chosen current ranges R1, R2 and R3. Moreover, the differences observed for these parameters (comparing each device alone versus the current range R1 R2 or R3) are not significant; However when the current increases their variation ($I_{R1}<I_{R2}<I_{R3}$) is non-monotonic. Hence, the barrier homogeneity does not depend of the current flow, in accordance with the previous conclusion about inhomogeneities and leakage current values.

Electrical parameters	Device #NL_R1	Device #NL_R2	Device #NL_R3
Results of the conventional Richardson method			
T range (K)	300 to 400K	300 to 400K	300 to 400K
Φ_B (eV)	0.74	0.78	0.85
A* ($AK^{-2}cm^{-2}$)	6.95×10^{-2}	1.4×10^{-1}	6.85×10^{-1}
Results of the modified Richardson method by Werner's model			
T range (K)	225 to 400K	175 to 400K	250 to 400K
$\overline{\Phi_B}$ (eV)	1.1	1.2	1.14
σ_S (meV)	102	116	104
A* ($AK^{-2}cm^{-2}$)	34	31.3	32.5
m* (kg)	$0.28m_0$	$0.26m_0$	$0.27m_0$

Table III-7. Physical and Electrical parameters of the #NL devices in three different current ranges R1 (10^{-11}A to 10^{-9}A), R2 (10^{-9}A to 10^{-7}A) and R3 (10^{-7}A to 10^{-5}A).

Electrical parameters	Device #L_R1	Device #L_R2	Device #L_R3
Results of the conventional Richardson method			
T range (K)	300 to 400K	300 to 400K	300 to 400K
Φ_B (eV)	0.6	0.61	0.62
A* ($AK^{-2}cm^{-2}$)	4.53×10^{-3}	7.56×10^{-3}	1.57×10^{-2}
Results of the modified Richardson method by Werner's model			
T range (K)	250 to 350K	250 to 400K	175 to 400K
$\overline{\Phi_B}$ (eV)	1.13	1.1	1.11
σ_S (meV)	124	120	124
A* ($AK^{-2}cm^{-2}$)	39.3	33.2	35.3
m* (kg)	$0.32m_0$	$0.28m_0$	$0.29m_0$

Table III-8. Physical and Electrical parameters of the #L devices in three different current ranges R1 (10^{-11}A to 10^{-9}A), R2 (10^{-9}A to 10^{-7}A) and R3 (10^{-7}A to 10^{-5}A).

III.3.2.d Accuracy of Richardson-Werner's model

As can be seen from the previous paragraphs, the applied model on our devices needs the knowledge of an effective Richardson constant value that is injected in Eq. 2; it is expected to find the same value when the Richardson model is applied, which is not the case. Thus, there is a necessity to apply Werner's model on Richardson's equation to find a value of A* in close agreement with the well-known theoretical value (32 $Acm^{-2}K^{-2}$).

However, for the accuracy of our extraction tool, a test is performed by injecting two different values of A* (lower value 20 $Acm^{-2}K^{-2}$ and upper value 40 $Acm^{-2}K^{-2}$, largely out of the uncertainty limits of the real value, worst cases analysis) in Eq. 2 and by applying Werner's model on Richardson's equation. **Table III-9** shows a comparison of the results obtained on the non-leaky device for the three A* values in the current range of 10^{-9}A to 10^{-7}A. The results indicate the accuracy of the model (Werner - Richardson): the extracted values of A* (19.1 $Acm^{-2}K^{-2}$, 31.3 $Acm^{-2}K^{-2}$ and 40.8 $Acm^{-2}K^{-2}$) are in close agreement with the injected values (20 $Acm^{-2}K^{-2}$, 32 $Acm^{-2}K^{-2}$ and 40 $Acm^{-2}K^{-2}$) with a negligible difference. Independently from the initial value injected on A*, the mean barrier height and the standard deviation are not affected from the variation of the Richardson constant. The only parameter affected is the effective mass, and this is obvious because of its dependence of A* through Eq. 11. Thus it can be concluded that the proposed method for extracting the Schottky barrier height and the standard deviation are robust versus the initial needed conditions.

Electrical parameters	A* = 20 $Acm^{-2}K^{-2}$	A* = 32 $Acm^{-2}K^{-2}$ (Al content of 18%)	A* = 40 $Acm^{-2}K^{-2}$
$\overline{\Phi_B}$ (eV)	1.14	**1.17**	1.16
σ_S (meV)	114	**116**	106
A* ($A.K^{-2}cm^{-2}$)	19.1	**31.3**	40.8
dA* (%)	-4.5	**-2.19**	-1.5
m* (kg)	$0.16m_0$	**$0.26m_0$**	$0.33m_0$
dm*	-4.2	**-1.9**	-1.5

Table III-9. Physical and Electrical parameters of the #NL devices in three different current ranges R1 (10^{-11}A to 10^{-9}A), R2 (10^{-9}A to 10^{-7}A) and R3 (10^{-7}A to 10^{-5}A).

Works are still ongoing on this extraction technique to understand the correlation between leakage current level, barrier height (mean value), standard deviation. Moreover, the deviation between initial parameter's instruction (Richardson constant and effective mass) and the extracted corresponding values must also be investigated to assess the representativity of these parameters. This part of the study will be conducted by another Ph. D candidate.

III.3.3 Pulsed time-domain measurements

The two different techniques developed to discriminate between the evolutions of the drain current versus initial DC conditions were described and presented in the previous chapter (reported below in **Figure III-31** and **Figure III-32**). Only non-leaky devices are measured due to the non-availability of leaky devices during that period of time of the project. The drain current is studied versus V_{DS} and V_{GS}. Afterward, by plotting the drain current versus time in a logarithmic presentation, it is possible to extract different time constants related to electrical initial conditions or to thermal conditions (#2 trapping process in **Figure III-31**). A procedure has been developed to discriminate between electrical and thermal effects, even if it is difficult to take account for the thermal effects as the involved time constants can range on a wide time scale (according to the different 'package-device-material' behavior).

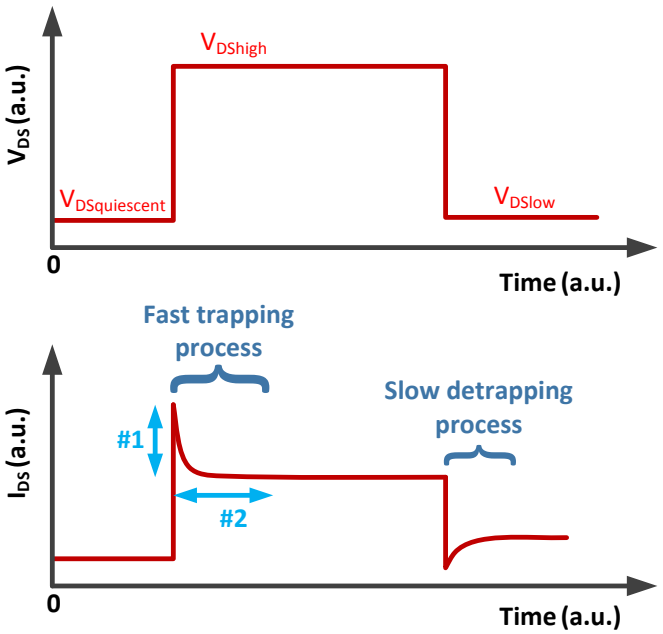


Figure III-31. Time dependence of the drain current I_{DS} versus the step variations of V_{DS}.

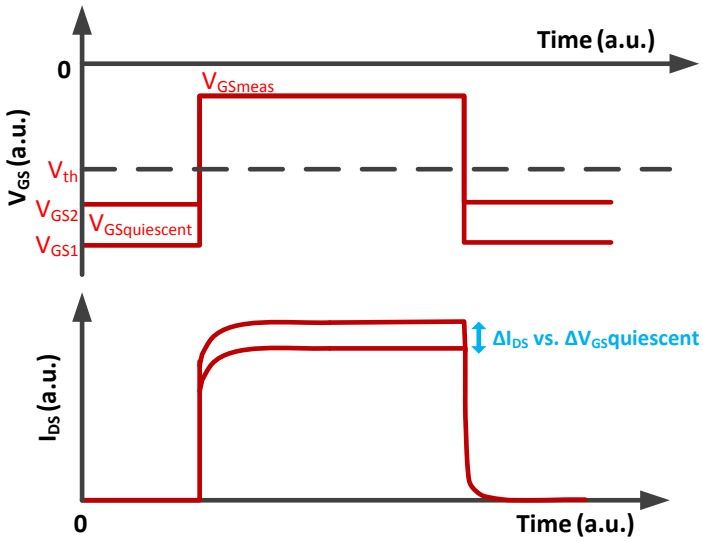


Figure III-32. Time dependence of the drain current I_{DS} versus the step variations of V_{GS}.

As illustrated in **Figure III-33**, five time constants can be used to fit the time dependence of I_{DS} (Involving up to 8 parameters). It is obvious that a logarithmic representation of the drain current evolution differs from that a linear representation as shown in **Figure III-31**. The measurements are performed at V_{DS}=10V (with initial V_{DS}=0V) and V_{GS}=-2V.

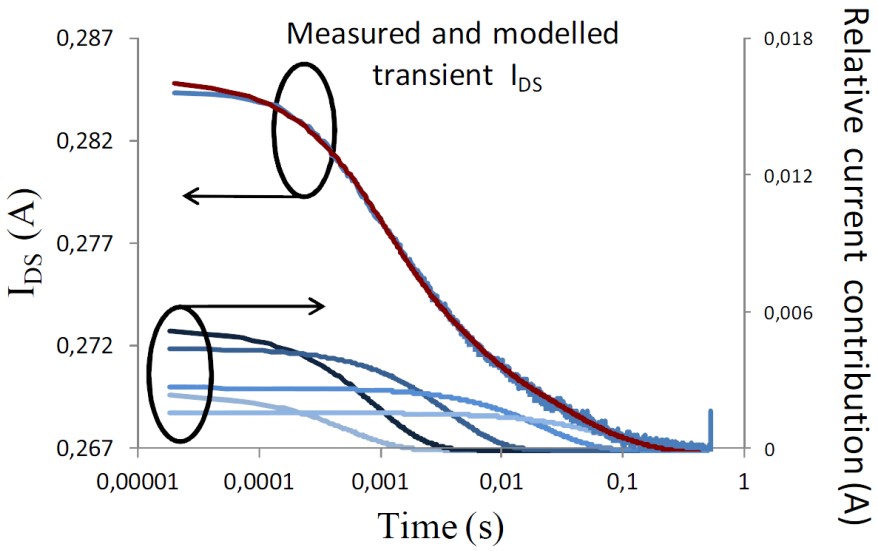


Figure III-33. I_{DS} logarithmic dependence with time, involving 5 exponential functions with time constant in the range of 10µs up to the second. Measurement performed on a virgin non-leaky device at V_{DS}=10V, V_{GS}=-2V ($V_{DS\_quiescent}$=0V).

This time dependence gives a dynamic overview of the different manifestations of the drain current variations versus V_{GS} and V_{DS}. This work has been done during the Master degree of Thierry Noutsa [25], and presented in [24].

It can be noticed from **Figure III-33** that the pulse duration of the gate or drain voltage sources for the lag characterization can be settled at τ=0.1µs to avoid any fluctuation of the drain current with time. A period (T=1ms to 100ms) long enough must be chosen to recover the initial state (no thermal effects, initial traps configuration before measurement) [26] [24].

III.3.4 Gate and drain LFN characterization

Gate and drain LFN measurements are performed on the **Declination_L** devices under different biasing conditions. This section focuses on the gate current LFN measurements followed by the drain current LFN measurements.

III.3.4.a Gate LFN characterization

The gate access of the HEMT devices is now investigated on transistors from the industrial process. Even if the technology is identical to that of the **Declination_S** wafer, some variations exists such as the size of the devices, involving a fundamental change in the noise sources magnitude (1/f and GR centers). As the gate remains a critical key point concerning the reliability of the devices, this characterization must be accurately developed (gate conduction mechanisms are usually pointed out to be the main limiting parameter leading to failures in AlGaN/GaN HEMTs). The LFN characterizations on the gate current are performed on the diode (open drain configuration) and on the transistor (in saturated region at V_{DS}=8V) similarly to the measurements carried out on **Declination_S** devices.

DC current voltage measurements are performed at room temperature using Agilent 4156C. **Figure III-34** shows the I_G-V_{GS} characteristics of the Schottky diode (open drain) and of the transistor when V_{DS} is biased from 0 to 8V. A similar trend to that of the Schottky diode is obtained when the device is shorted at the drain access (with a slight increase on I_G as the leakage path is also available between gate and drain). This study focuses on the two extreme I_G plots extracted from our measurements (the diode alone and the transistor mode at V_{DS}=8V). A difference in the gate leakage current is observed between #NL and #L devices.

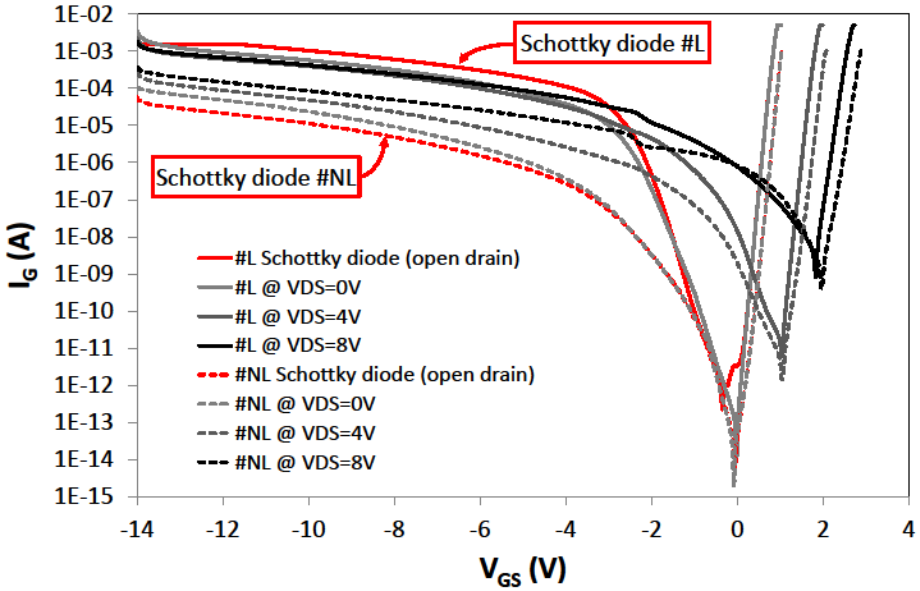
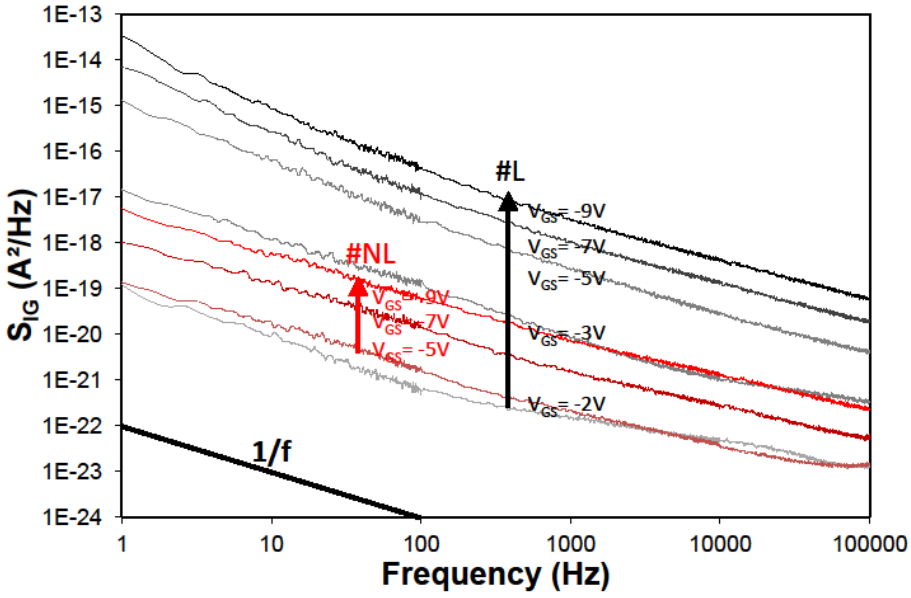
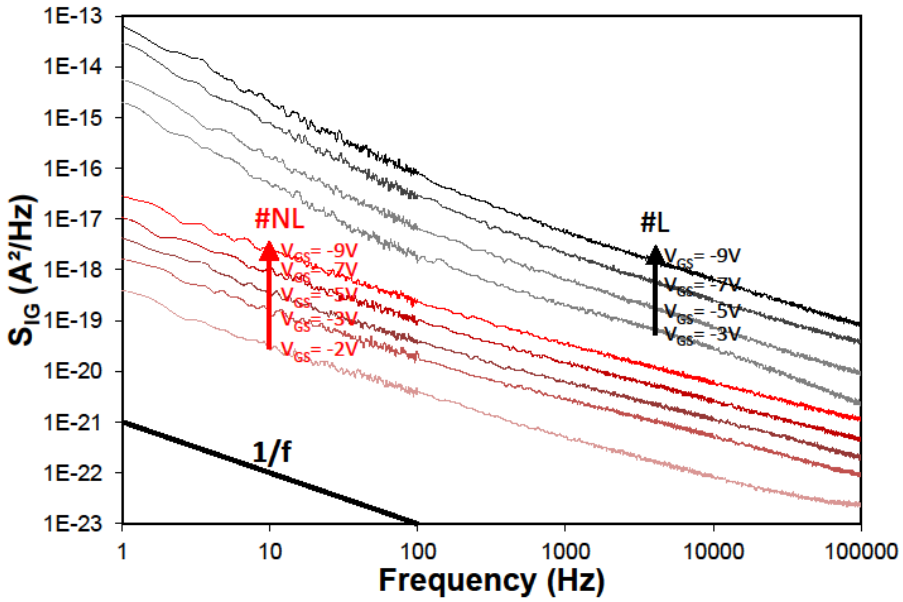


Figure III-34. DC I_G-V_{GS} gate characteristics of #NL and #L devices.
Red curves (dashed and solid lines): the Schottky diode
Grey to black: the transistor biased at V_{DS}=0V, 4V and 8V.

The gate noise current measurements performed on #NL and #L are presented in **Figure III-35** as follows: **Figure III-35(a)** and **35(b)** show the measurements carried out on the Schottky diodes and on the transistor at V_{DS}=8V respectively for #NL and #L.



(a)



(b)

Figure III-35. Gate noise current spectral density of the AlGaN/GaN HEMTs.
(a) Of the Schottky diodes (open drain).
(b) Of the transistors biased in the saturation region at V_{DS}=8V.

The non-leaky device #NL features almost the same scattering of the spectra than for #L when considering the common biasing range (approximately 2 decades). However, it is found that a difference of more than four decades is noticeable between the gate noise current densities of #NL and #L: this is relevant with the difference found on DC leakage currents from **Figure III-34** (more than 2 decades at V_{GS}=-2V, -3V, -5V). Moreover, the noise evolution of the non-leaky device follows a 1/f behavior while #L spectra are mainly composed by numerous generation-recombination (GR) centers (mainly in the lower frequency band), that mask the 1/f noise source. At first, this reveals a large number of traps and defects directly related to the degradation of the leakage current for #L device.

These traps can be the precursors of failure degradation modes when the devices are stressed. **Table III-10** synthesizes the gate current values from the LFN measurements extracted at different biases under each configuration for #NL and #L.

	V_{GS} (V)	-2	-3	-5	-7	-9
#NL (Non-leaky device)	I_G (Schottky diode) (µA)	-	-	0.64	2.8	7.4
	I_G (Schottky diode) (µA/mm)	**-**	**-**	**0.4**	**1.75**	**4.6**
	I_G (Transistor at V_{DS}=8V) (µA)	1.12	4	8	14	23.5
	I_G (Transistor at V_{DS}=8V) (µA/mm)	**0.7**	**2.5**	**5**	**8.8**	**14.7**
#L (Leaky device)	I_G (Schottky diode) (µA)	0.25	7.1	37	97	210
	I_G (Schottky diode) (µA/mm)	**0.16**	**4.4**	**23.1**	**61**	**131.2**
	I_G (Transistor at V_{DS}=8V) (µA)	-	36.5	80	160	300
	I_G (Transistor at V_{DS}=8V) (µA/mm)	**-**	**23**	**50**	**100**	**188**

Table III-10. Gate Current Values

The results reveal the strong difference on the gate access between the two devices: the current leakage kinetic is also of different nature between #NL and #L as the electrons are neither subjected to the same mechanism nor following the same conduction path (leakage current between gate and source). From the raw values taken at a frequency of 100 Hz, the evolution of the magnitude of a generation-recombination (GR) center is extracted for every bias. **Figure III-36** shows the dependence of the gate current noise spectral density (S_{IG}) when the gate current (I_G) varies. I_G power laws of 1.35±0.1 and 1.7±0.1 are found for the diode and for the transistor for the non-leaky device (#NL) and leaky (#L) devices respectively.

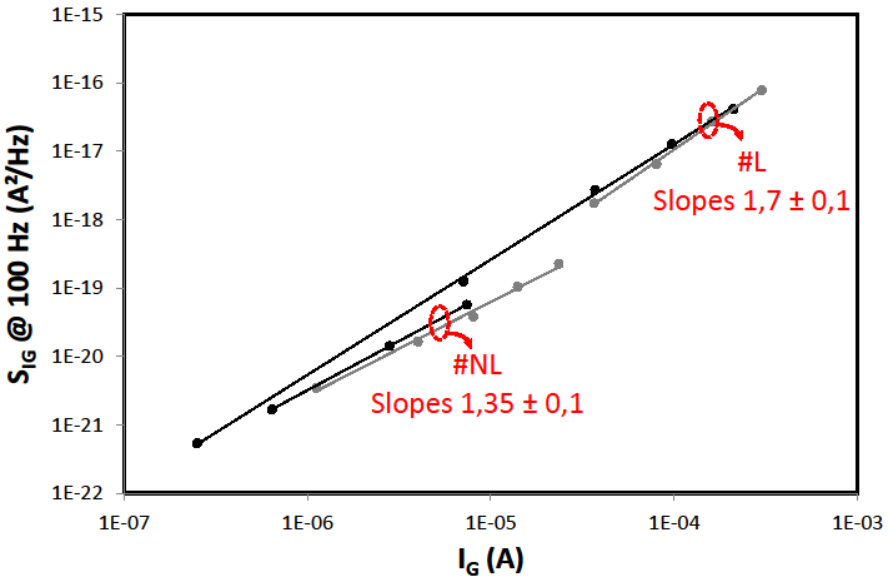


Figure III-36. Gate current noise spectral density (SI_G) at 100Hz versus gate current (I_G) for the Schottky diode (-9V≤V_{GS}≤-2V, black plots) and for the transistor (V_{DS}=8V, -9V≤V_{GS}≤-2V, grey plots).

Figure III-37 shows the gate current spectral density S_{IG} normalized as S_{IG}/I_G^x with x=1.3 and x=1.7 for #NL and #L devices respectively corresponding to $I_G^{1.3}$ and $I_G^{1.7}$ respective power laws as presented in **Figure III-36**. This identical signature observed for the diode (-9V≤V_{GS}≤-5V) and for the transistor (-9V≤V_{GS}≤-2V) can be imputed to the same noise sources, and to the same path where the electrons flow from the gate to the source and from the gate to the drain accesses as mentioned previously for

the **Declination_S** devices in the previous section [13]. The leakage current responsible for I_G is of the same nature for the diode (under high reverse biases) and for the transistor (regardless the gate bias and at V_{DS}=8V) [10].

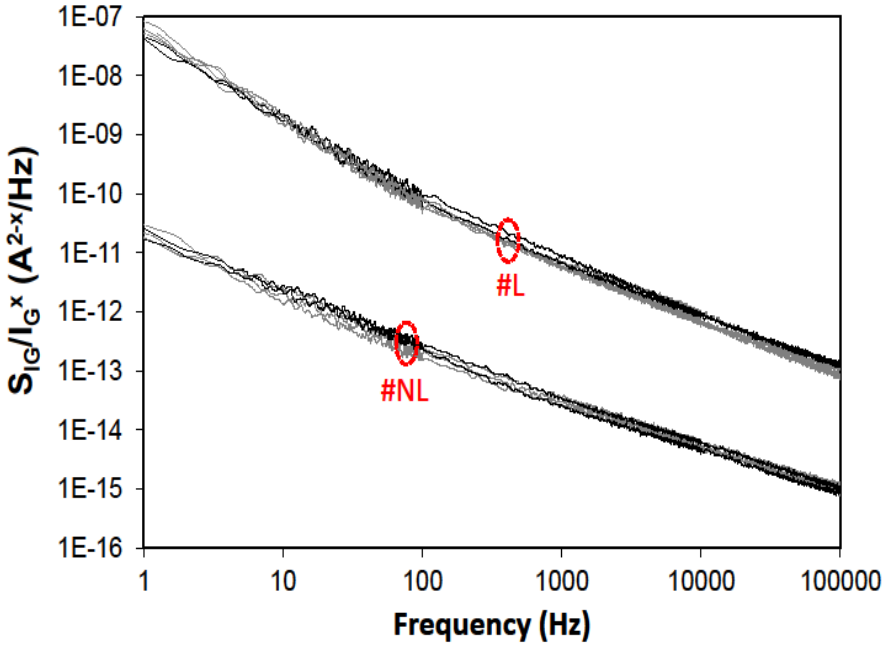


Figure III-37. Normalized gate current noise spectral density for the Schottky diode under high reverse biases (-9V≤V_{GS}≤-5V, black plots), and for the transistor (-9V≤V_{GS}≤-2V, grey plots).
(a) Normalized gate current noise spectral density $S_{IG}/I_G^{x=1.3}$ for #NL devices.
(b) Normalized gate current noise spectral density $S_{IG}/I_G^{x=1.7}$ for #NL devices.

III.3.4.b Discussion on the gate LFN characterization of Declination_S and Declination_L devices

The study presented above proves the needs to control and study the gate access performances through its technological structure. This section is devoted to the comparison between small size research level devices (**Declination_S**) with large size commercial level devices with field-plate (**Declination_L**). **Figure III-38** shows the dependence of the gate current noise spectral density (S_{IG}) when the gate current (I_G) varies for the **Declination_S** (#A) and **Declination_L** (#NL and #L) devices. It can be noticed that #A and #NL share the same current law of I_G1.3 and different than that observed for the leaky device (#L) of 1.7.

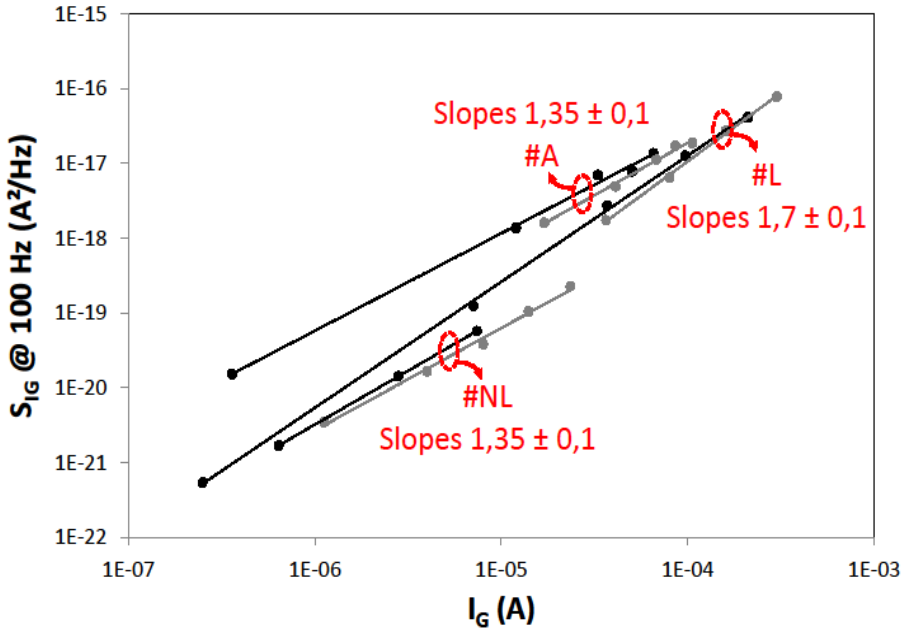


Figure III-38. Gate current noise spectral density (S_{IG}) at 100Hz versus gate current (I_G) for the Schottky diode (-9V≤V_{GS}≤-2V, black plots) and for the transistor (V_{DS}=8V, -9V≤V_{GS}≤-2V, grey plots) for #A, #NL and #L devices.

Figure III-39 superimposes these LFN dependences versus frequency. Low leakage #NL large size devices and low leakage #A small size devices share the same power law over the whole frequency range, whereas another type of leakage is involved in leaky #L large devices. Consequently, the devices driven under high reverse bias conditions will be sensitive to different leakage mechanisms and thus to different degradation modes under the application of stresses such as HTRB (high thermal reverse bias) stress for example. However, even if sharing the same power law, the spectra differs from #A structures to #NL devices. Firstly, the large size of the device lowers the LFN spectral density as expected because of the 1/f contribution that decreases with the size of the device. Moreover, different GR centers appear (visible in the high frequency range of #A), attributed to long term memory effects. This result also corroborates with the transient measurement; featuring time constants up to some seconds.

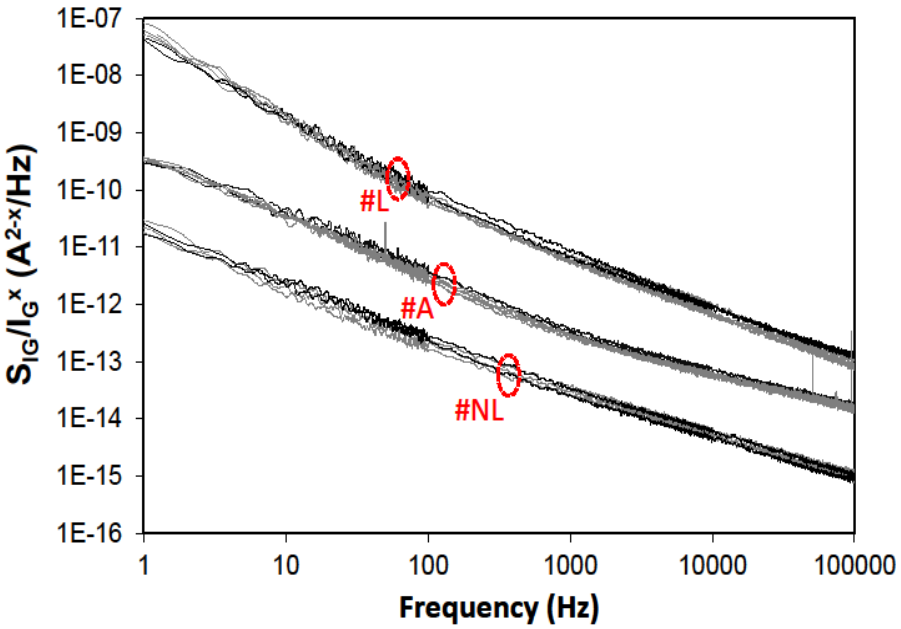


Figure III-39. Normalized gate current noise spectral density for the Schottky diode under high reverse biases (-9V≤V_{GS}≤-5V, black plots), and for the transistor (-9V≤V_{GS}≤-2V, grey plots).
(a) Normalized gate current noise spectral density $S_{IG}/I_G^{x=1.3}$ for #NL devices.
(b) Normalized gate current noise spectral density $S_{IG}/I_G^{x=1.7}$ for #A and #NL devices.

As the gate Schottky terminal controls the carrier's flowing in the channel between source and drain, the gate stability and the mastering of the conduction mechanisms are of prime importance to assess the reliability of a technology. However, the drain noise current spectral densities are also of prime interest as they are used to size the electronic modules such as (controlled) oscillators and mixers. The mastering and the stability of these spectra ensure an equipment to fulfill its specifications during the expected life time. Results of LFN spectra on the drain terminal are presented in the next section.

III.3.4.c Drain LFN characterization

The drain current and drain LFN spectra are the first parameters to consider for non-linear applications such as VCO, mixer, etc., the study of S_{ID} can be used to design low noise non-linear circuits.

Figure III-40 illustrates the $I_D(V_{DS})$ DC measurements. The difference noticed on the drain currents of #NL and #L remains small (about 10%) in comparison with their gate currents, but it is important to take it into account. Thus, no significant difference is noticed between #NL and #L on their drain current (DC and pulsed measurements), and it could be easily assumed that #NL and #L could be independently used for a given application if only the drain current was considered.

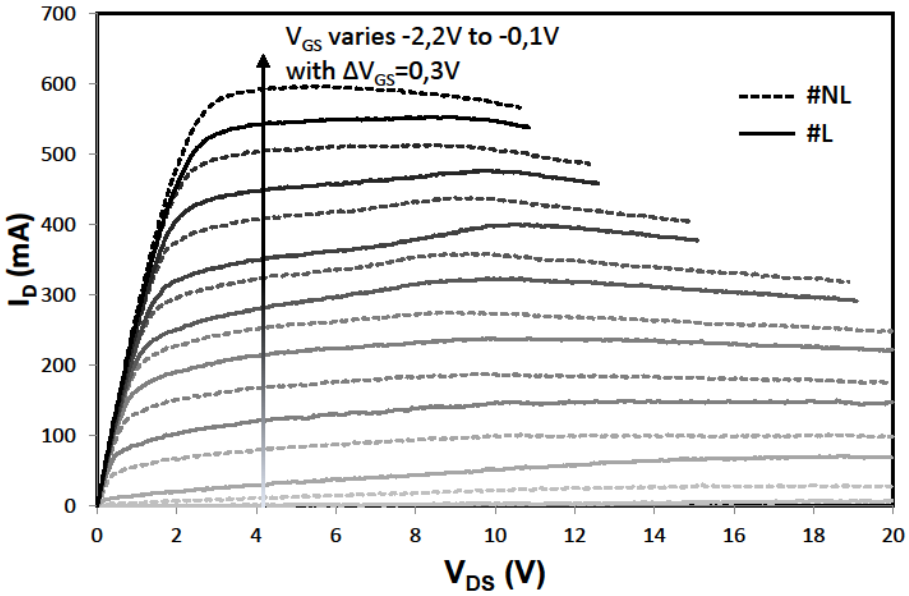


Figure III-40. DC output characteristics of #NL and #L devices when V_{GS} varies from -2.2 to -0.1V with a step of 0.3V.
The dashed and solid lines correspond to #NL and #L respectively.

Figure III-41 shows the drain current noise measurements normalized versus the drain current (S_{ID}/I_D) for #NL and #L at constant V_{GS} and when V_{DS} varies (V_{GS}=-1.3V, V_{DS}=5V) and (V_{GS}=-1.3V, V_{DS}=8V). From the gate current noise measurements, it is noticeable that more GR centers are masking the 1/f behavior of #L in comparison with #NL spectra. These GR centers have a strong impact on the trapping mechanisms of the carriers: the presence of these traps are clearly evidenced by the presence of GR centers in the lower frequency band (below 100Hz) more pronounced for the leaky device than for the non-leaky devices. Even if no correlation has been found between S_{IG} and S_{ID} spectra, it is noticeable that leaky devices present higher number of charges (as shown in **Figure III-35**) in the vicinity of the gate (surface and volume charges). Moreover, when the biasing changes from V_{DS}=5V to V_{DS}=8V (constant I_{DS}, devices are quasi thermally stable), the space charge region evolves for both #NL and #L, and charges can be created between gate and drain terminals. The bias dependant charge variation under the gated zone and between gate and drain of the two types of devices can be the cause of an intrinsic modification of the gate control of the carriers (Schottky diode) [13] [27]. As a consequence of a higher number of charges close to the gate controlled-zone, the drain current I_{DS} is reduced by 13% for the leaky devices (positive charges are located beneath the gate metallization whereas negative charges are positioned on the opposite side at the AlGaN/GaN interface). This phenomenon is observed on the DC and pulsed I_{DS}-V_{DS} characteristics as well as on S_{ID}/I_D LFN measurements for #NL and #L. When considering the normalized drain current noise spectral density in **Figure III-41**, leaky and non-leaky devices feature almost the same normalized noise level for frequencies above 100Hz, whereas the noise behavior in the lower frequency band largely differs between these two sets of devices. Once again, the traps involved between 1Hz-100Hz can be associated with a higher density of charges for the leaky device under the gated zone (with time constants ranging from 5ms to few seconds, also revealed by transient measurements).

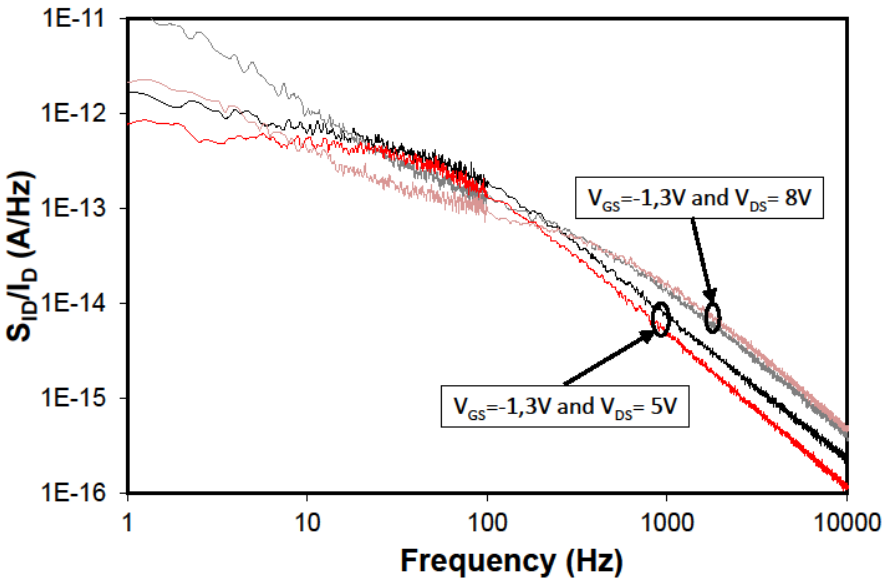


Figure III-41. Drain noise current spectral densities of #NL and #L at V_{GS}=-1.3V and V_{DS}=5V and 8V. The red and grey plots correspond to #NL and #L respectively.

Figure III-42 presents the drain noise current measurements carried out on the non-leaky device at constant V_{DS} of 7V when V_{GS} varies from -1.9 to -1.3V by step of 0.3V; It can be assumed that the device is sensitive to the thermal steady state of the channel as first order consideration ($P_{DC}=V_{DS}.I_{DS}$) . Similar trends and noise levels are found for #NL and #L devices. The GR centers extracted between 10Hz and 1 kHz are thermally activated (as shown in **Figure III-42**); the time constant of the involved traps decrease when the temperature increases (using a first order assumption considering the temperature to be proportional to $P_{DC}=I_D.V_{DS}$).

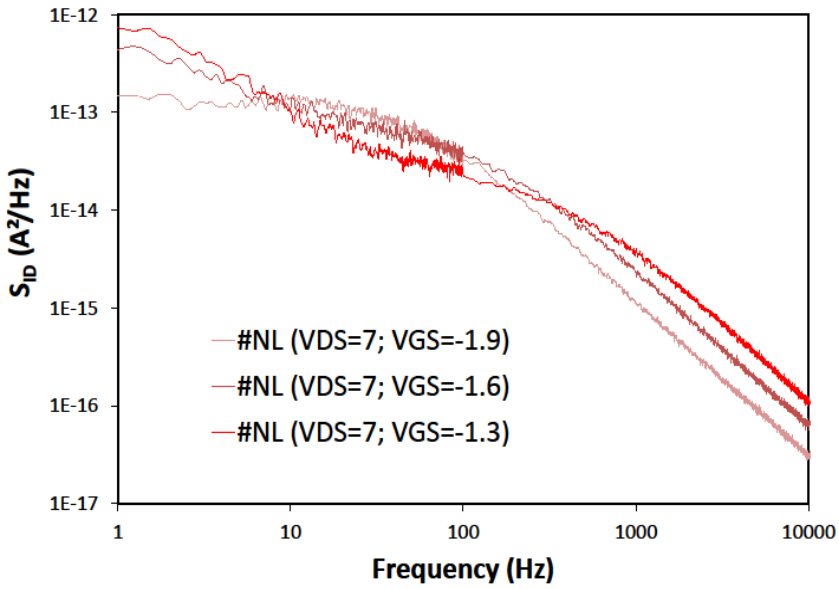


Figure III-42. Drain noise current spectral densities of #NL only at constant V_{DS} values of 7V and at V_{GS}=-1.9 to -1.3V with ΔV_{GS}=0.3V.

Table III-11 synthesizes the drain current values from the LFN measurements extracted at constant V_{DS} of 7V and when V_{GS} varies from -1.9V to -1.3V for #NL and #L. Lastly, the only drain

current analysis (DC, pulsed or LFN) is not convenient to evidence a possible evolution of the gate controlled charges in the 2DEG (as a consequence of the gate access evolution versus stress).

	V_{GS}(V)	-1.9	-1.6	-1.3
#NL (Non-leaky device)	**I_D (Transistor at V_{DS}=7V) (mA)**	85	170	250
#L (Leaky device)	**I_D (Transistor at V_{DS}=7V) (mA)**	55	130	218

Table III-11. Drain current values.

The measurements performed on the **Declination_L** devices are statistically confirmed; **Figure III-43** reports on the drain LFN measurements of three samples from the same set of devices (non-leaky devices: #NL) at constant V_{DS} of 7V and when V_{GS} varies from -1.9V to -1.3V. The obtained results can be considered as statistically relevant. Moreover, the LFN drain current noise spectra are known to be an accurate prober of the crystal defects in the transistor: the absence of dispersion stands as a good indicator of the homogeneity of the devices under test.

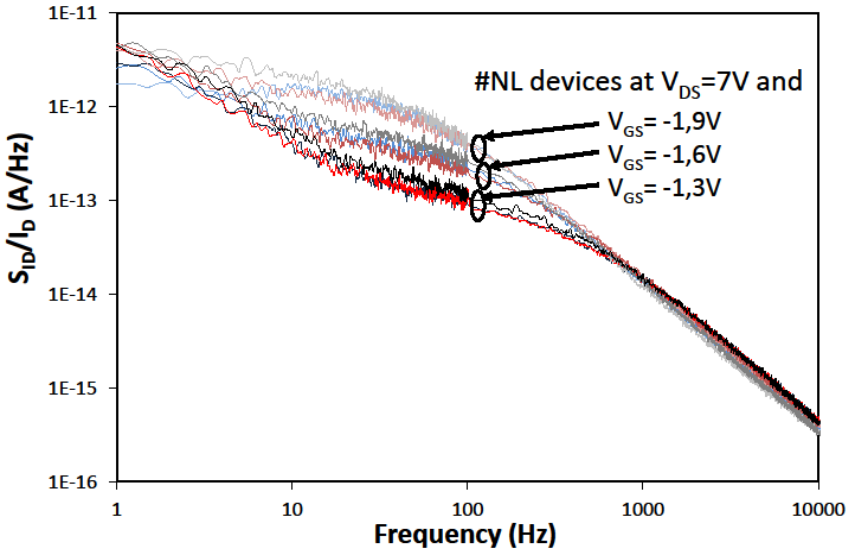


Figure III-43. Drain noise current spectral densities normalized versus drain current for three #NL-type devices. The measurements are performed at constant V_{DS} values of 7V and at V_{GS}=-1.9V to -1.3V with ΔV_{GS}=-0.3V. [9]

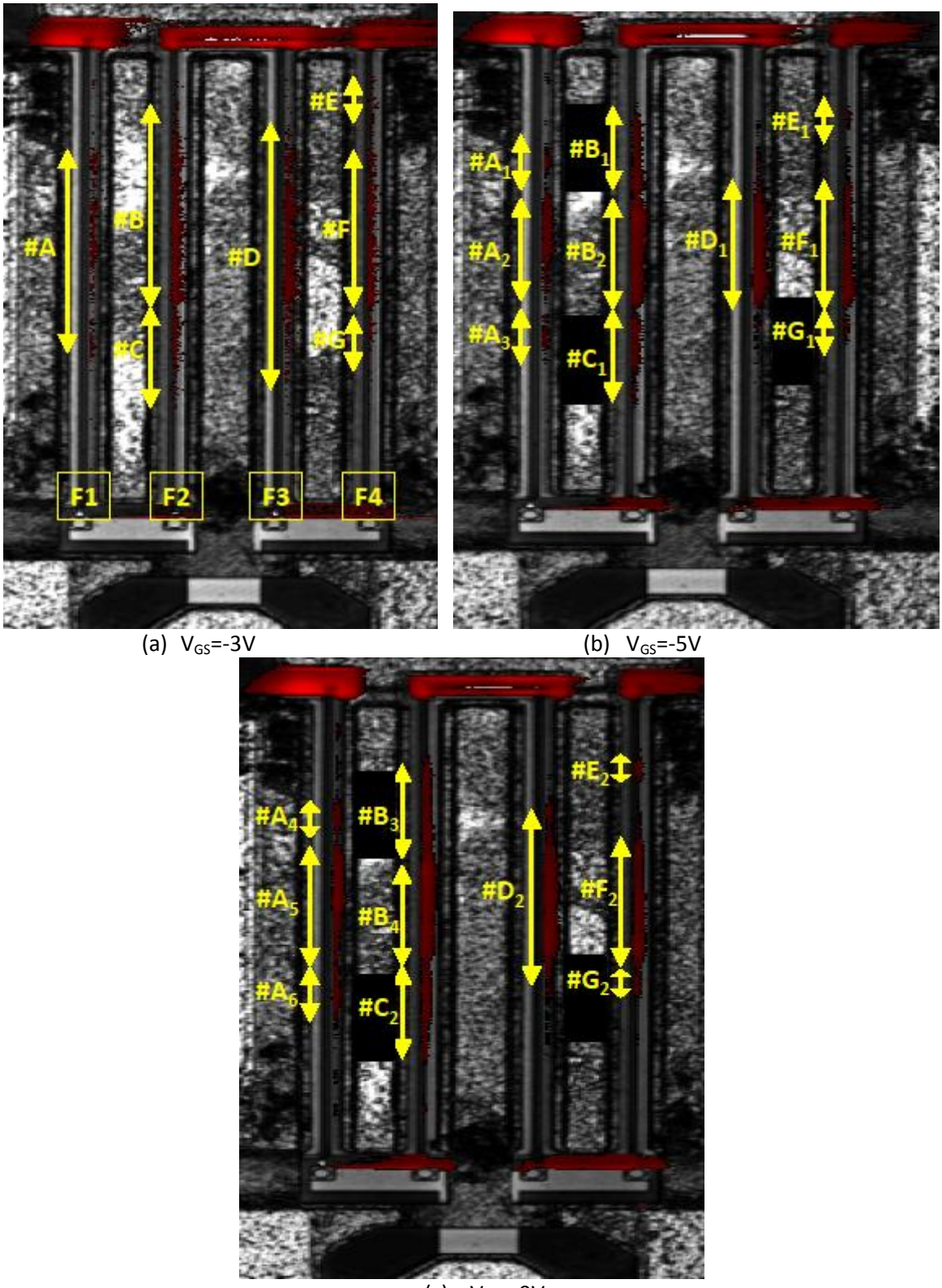
From previous studies to ReAGaN project, and also verified on the first set of devices from REAGAN, it has been found that the GR extracted from SID spectral density (bulge noticed in **Figure III-43** for example) evolves with the voltage variation (i.e. at first order consideration with the space charge region evolution); this evolution has been noticed whatever the extension of the space charge region (SCR) between gate-drain and/or gate-source at different biasing conditions (constant V_{DG}, constant V_{DS}, constant V_{GS}). The magnitude of the GR increases linearly with the voltage variation for these 3 different voltage conditions, and hence it can be concluded that more traps are activated between gate-drain and/or gate-source when the SCR spreads towards the drain or source terminals [24]. Theses GR centers seems to be located at the interface between the two semiconductors AlGaN/GaN, as they feature the same LFN signatures versus biasing conditions than devices previously characterized from other technologies or other wafers in previous works. Moreover, a

temperature law can be found when the dissipated power evolves in the 2DEG channel of the devices, as explained previously.

III.3.5 OBIRCh results on Declination_L devices

Similarly to **Declination_S** devices, the **Declination_L** devices have shown red spots when an increase in the current and a decrease in the resistivity happened. The measurements performed on virgin (leaky and non-leaky devices) devices did not reveal any resistivity fluctuation unlike by HTOL (High Temperature Operating Life) stressed devices. Hence, only the results of OBIRCh analysis on stressed devices are presented next.

Figure III-44 shows the measurements performed on the Schottky diode (open drain configuration) at V_{GS}=-3V, -5V and -9V. The analysis drawn from these measurements are presented in **Table III-12**.



(a) V_{GS}=-3V (b) V_{GS}=-5V

(c) V_{GS}=-9V

Figure III-44. OBIRCh measurements between gate and source regions of the transistor: the Schottky diode is biased at V_{GS}=-3, -5 and -9V. F1, F2, F3 and F4 correspond to the 1st, 2nd, 3rd and 4th fingers respectively at each bias.

	1st finger (F1)	2nd finger (F2)	3rd finger (F3)	4th finger (F4)
At V_{GS}=-3V	Noisy spread of spots is observed (#A).	Two spots are observed on the gate width but #B has a greater width than #C.	Localized spot is noticeable in the middle of the gate width.	Two small spots (#E and #G) revealing a very local current paths can be seen on the both sides of homogenously spread spot (#F).
At V_{GS}=-5V	When the current increases, #A is divided into three localized spots: #A_1, #A_2 and #A_3.	At V_{GS}=-5V, #B is divided into two localized spots: #B1 and #B2, but #B2 shows more current fluctuations than #B1. As for #C, it conserves the same width with more pronounced resistivity fluctuations.	The width of the #D spot decreases into #D1 but more significant resistivity fluctuation can be seen with greater area of red spots.	All the three spots observed at V_{GS}=-3V, conserves the same width with more pronounced red spots.
At V_{GS}=-9V	More pronounced marking of the red spots (#A4, #A5 and #A6).	Homogenous spread of the spots lead to the connection of the three spots (#B3, #B4 and #C2).	The increase in the resistivity fluctuation leads to a decrease in the marking of the spots.	The localized small spots (#E1 and #G1) increase their marking (#E2 and #G2). The same phenomenon is observed on #F2 spot.

Table III-12. OBIRCH analysis.

As for the devices on **Declination_S** wafer, LFN and OBIRCh feature the same trend of an increase of the GR magnitude and of the spot spreading/density when the leakage current increases. Once again, it is noticeable on **Declination_L** that the spots can move with the reverse voltage (increase of the leakage level). Piezoelectric effects can be the origin of these spot moves as the strains evolve with the application of the voltage between gate and source.

III.3.6 Deep level trap study: I-DLTS

Deep Level Transient Spectroscopy (DLTS) measurements on the drain current (I-DLTS) are performed to extract the activation energies of the involved traps seen during LFN measurements. The measurements are carried out on different devices than **Declination_L**. The devices under test are here labeled as Cassini. Since the measurement bench shows limitations on the current level, this required some adjustments for power devices.

The measurements are performed on 3 Cassini devices (8×125µm×0.5µm): A virgin device and two stressed devices grown on SiC substrate and featuring 25% of Al content. The applied stress is HTRB (described in chapter 1) for 1000 hours at a junction temperature Tj=200°C and for V_{DS}=30V, V_{GS}=-7V and I_{DS}=0 A/mm. During the I-DLTS measurements, V_{DS} pulses of 10 ms are applied on the devices with different magnitudes at constant V_{GS}. The purpose is injecting the carriers and filling the traps during the pulse then controlling the behavior during the relaxation (at negligible drain current).

The trap observed on the virgin device (#TB19) is associated to an electron trap (ME6) usually attributed to an Oxygen pollution or to a defect formation related to the Oxygen in AlGaAs/GaAs structures. Indeed, the temperatures where the I-DLTS signal appears confirm the phenomenon, since they are already observed for AlGaAs/GaAs devices [28] [29]. However, it is difficult to attribute the same mechanisms for our structures given the large differences in lattice mismatch. The activation energy of the observed trap on the virgin device is 0.704 eV (**Figure III-45**) with a capture cross section of $7.46.10^{-15}$ cm². It should be known that no DX [30] [31] traps are detected (inherent in Silicon doping). Moreover, a DX center is usually attributed to the interaction between a donor trap and the Al or the Ga whereas; the devices under test are non-intentionally doped, so this confirms the absence of these traps.

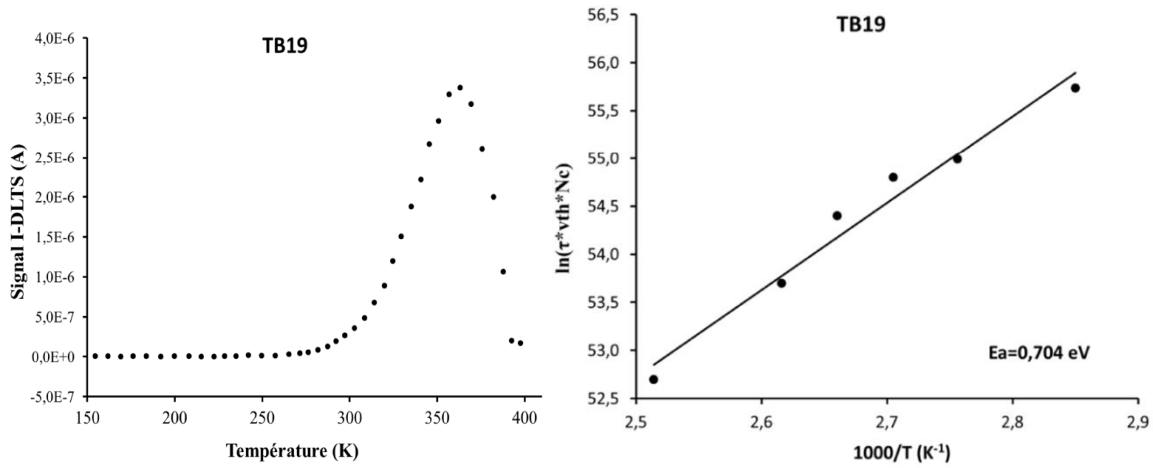


Figure III-45. I-DLTS study on the virgin #TB19 device.
(a) I-DLTS signal extracted versus temperature at V_{DS}=3V and V_{GS}=-2.2V.
(b) Arrhenius plot to extract the activation energy (Ea=0.704 eV).

After the application of the HTRB stress with a junction temperature of 200°C, two different behaviors are observed on the stressed devices. The #B8 device shows a hole-trap at activation energy of 0.32 eV (**Figure III-46**). On the other hand, the second stressed device #B12 did not show a

hole-trap device, but the same trap as the virgin device with activation energy of 0.67 eV (**Figure III-47**). It should be noticed that under different biasing conditions that same characteristics are observed on the involved traps as shown in the **Figure III-48** for #B12 device.

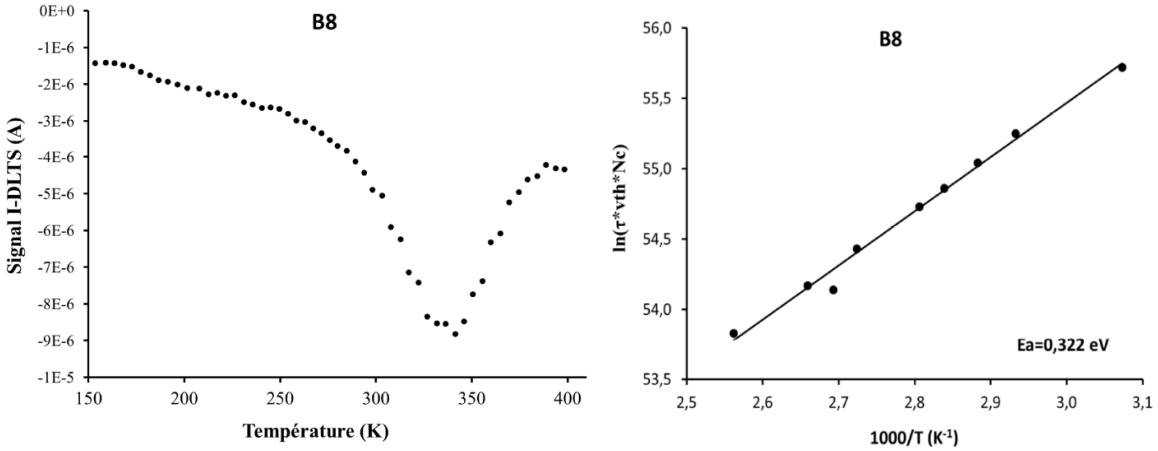


Figure III-46. I-DLTS study on the virgin #B8 device.
(a) I-DLTS signal extracted versus temperature at V_{DS}=15V and V_{GS}=-2.2V.
(b) Arrhenius plot to extract the activation energy (Ea=0.322 eV).

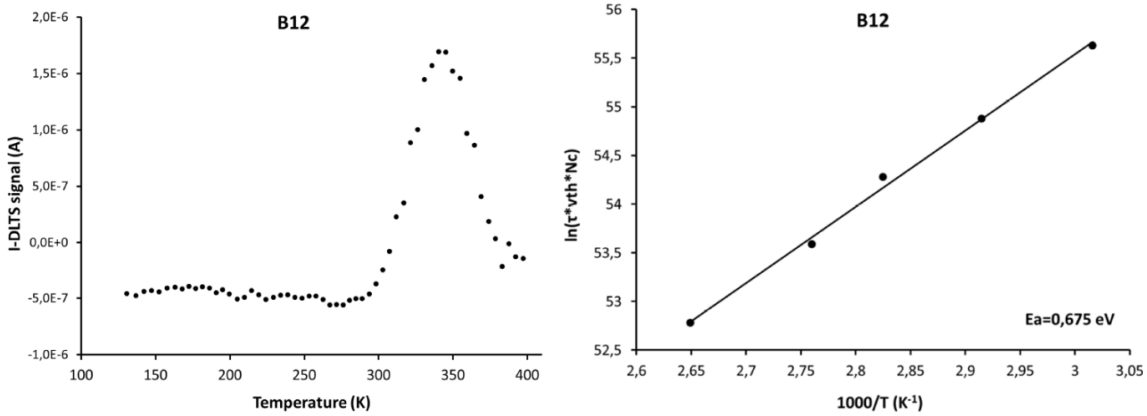


Figure III-47. I-DLTS study on the virgin #B12 device.
(a) I-DLTS signal extracted versus temperature at V_{DS}=15V and V_{GS}=-2.2V
(b) Arrhenius plot to extract the activation energy (Ea=0.675 eV).

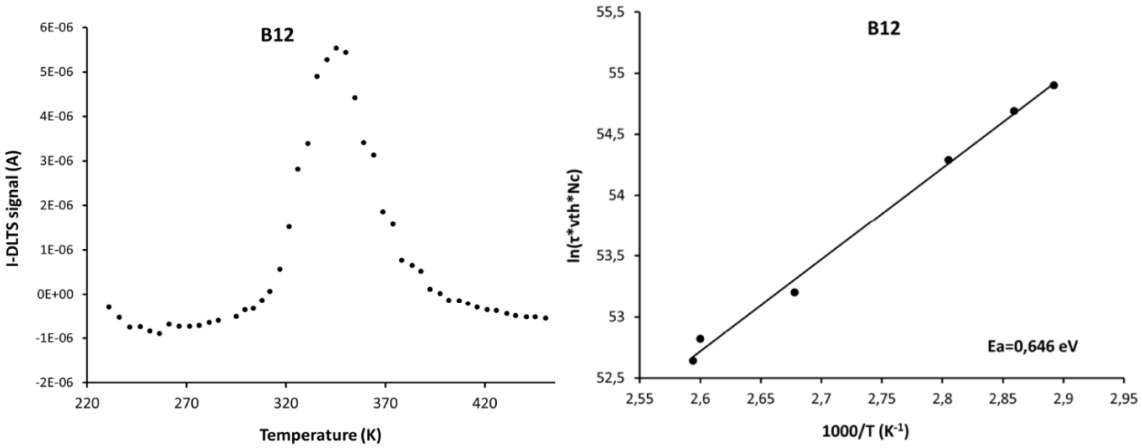


Figure III-48. I-DLTS study on the virgin #B12 device.
(a) I-DLTS signal extracted versus temperature at V_{DS}=7V and V_{GS}=-1.7V.
(b) Arrhenius plot to extract the activation energy (Ea=0.646 eV).

III.4 Conclusions

The chapter presents the results issued from all the experimental techniques developed or used by LAAS as presented in chapter 2 and performed on the AlGaN/GaN HEMTs. The techniques are applied on small and research level devices (1×100µm×0.5µm), as well as on large and commercial devices (4×400µm×0.5µm).

The Schottky barrier height homogeneities studied first consolidate the next assumption: the difference in Richardson's constant after applying Werner's model on Richardson's equation is physically related to the real effective mass. Moreover, gate conduction mechanisms and gate defects under reverse biasing are investigated in diode configuration and in transistor operating mode using gate LFN characterization and OBIRCh techniques. It can be concluded that:

- Defects between gate and source are localized by OBIRCh and identified by LFN technique. S_{IG} spectra feature $I_G^{1.3}$ power law under high reverse biases, where a common origin of the gate leakage current is found for the diode and for the transistor. Moreover, spots measured by OBIRCh spread on a larger zone of the gate width as the gate to source voltage decreases (high reverse V_{GS}). This is consistent with the increase of the I_G leakage current when V_{GS} decreases.

- Trapping-detrapping centers are also detected with LFN measurements. The S_{IG} spectra, normalized to the gate current $I_G^{1.3}$, feature the same GR frequency and magnitude signatures on a large reverse V_{GS} range both under diode and transistor biasing conditions: the leakage current originate from the same defects (same path for the electrons). Moreover, the GR centers provide distinct trends at the vicinity of V_{GS}=-3V. This is attributed to a change in the conduction mechanism of the leakage current, also tangible through the analytical modeling of I_G-V_{GS} proposed in the chapter (Fowler-Nordheim and Pool-Frenkel's models).

- The origin of the extension of the spots (OBIRCh technique), and the peculiar signature of the LFN spectra for the devices under test can be explained considering the large electrical field supported by the device (essentially between Gate and Source terminals, i.e. the smaller dimension in comparison with Gate-Drain terminals). This electrical field induces mechanical strains via the elastic tensors and piezoelectric moduli within the dislocations of the device. The involved mechanisms are in agreement with the order of magnitude of the applied electrical field, with respect to the dimension between the two intrinsic G-S terminals.

The EBIC technique developed and studied by the DGA is able to track invisible defects located within the gate metallurgy. Further investigations have been defined for reducing EBIC signal noise and to be able to reveal hidden defects below field plate HEMTs structures, whatever is their geometry. The plan is to continue these studies in relationship with electrical characterisations and aging tests on X band GaN HPA dedicated to airborne applications for a better management of device risks in military programs.

From the drain and gate LFN measurements on **Declination_L** devices, it can be concluded that devices with slight differences in drain current noise can have quite different gate current noise. Actually, these results are consistent with pulsed electrical characterizations, as the numerous traps revealed by LFN on the gate terminal can reasonably be correlated with a higher level of gate lag on the leaky devices (analysis confirmed by lag measurements at IMS Bordeaux on the same devices [9]). These traps act as trapping-detrapping processes with time constants ranging from few microseconds to some seconds (also revealed by pulsed I-V transient characterizations). The surface passivation and the mastering of the gate Schottky diode are key points concerning the performance and the reliability of the devices, through a reduction of traps and leakage currents. Concerning the drain terminal, no strong difference is noticed between leaky and non-leaky sets of devices, in spite of numerous GR centers revealed by LFN characterization in the lower frequency band. Traps have been located at the interface between the AlGaN and GaN layers, and are activated with the extension of the space charge region between gate-source and gate-drain regions when the respective voltages V_{GS} and V_{DG} are applied. Moreover, no correlation is found between noise current densities of gate and drain terminals.

Despite the importance of the drain access and hence of the drain current, the gate leakage current is a major indicator to follow up; the results indicate that the gate technological process remains a critical issue for the qualification of competitive and reliable GaN technologies. However, at this stage of the development, the devices feature an elevated median time to failure (MTTF) at 3×10^7 (resp. at 2×10^6) hours for a junction temperature of 175°C (resp. 200°C) [1] [32].

This study roadmap developed at LAAS-CNRS during the ReAGaN ANR project and performed on GH50 devices will be applied on other devices throughout the same project (gathering of all electro-mecanico-thermal data and models) with another PhD student (Oana LAZAR).

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GENERAL CONCLUSION

The maturity of the GaN technology for the fabrication of integrated circuits such as power amplifiers (PA), low noise amplifiers (LNA), voltage control oscillators (VCO), mixers represents a major technological challenge. This thesis is based on the reliability study and failure analysis of AlGaN/GaN HEMTs for high power and high frequency applications.

As the reliability study requires different multi-physical experimental tools. Our study first focused on the development of different measurement benches (electrical, LF noise and electro-optical) and a study roadmap with the goal of defining a design of experiment on these technologies. Adjustments have been made considering the first roadmap of the project on its submission stage; depending on the priorities given to the study cases or to the new (unexpected) results. Destructive and non-destructive techniques are applied on the devices, but this manuscript that represents major part of the work performed at LAAS – CNRS highlights only on non-destructive techniques: electrical measurements, low frequency noise, transient I-V, OBIRCh and EBIC techniques, I-DLTS. These techniques are organized into characterization campaigns, and for more accuracy the test-benches and the stability of the devices are controlled regularly during the considered campaign.

The reliability study cases presented in this work are divided into two main types: electrical and electro-optical. They are carried out on two different set of devices: small size and research level devices featuring a single gate finger (1×100µm×0.5µm) and large size commercial devices with 4 gates fingers (4×400µ×0.5µm) and with different gate leakage rates.

In the first place, DC electrical I_G-V_{GS} measurements are performed versus temperature to study the Schottky barrier height homogeneity. The original approach of Werner's model associated to Richardson's equation brings accurate information on the barrier homogeneity. The devices - although their structural difference - have shown inhomogeneous barriers at their metal-semiconductor interface. Moreover, gate and drain LFN measurements are performed. The gate conduction mechanisms are investigated under reverse biasing conditions on the diode (open drain) and on the transistor (saturated region) revealing a common gate current path between gate and source (gate and drain) terminals. As for the drain current LFN measurements, they are carried out only on large scale devices; the results have not shown significant difference between leaky and non-leaky devices, hence the mastering of the drain current only is not sufficient for the qualification of transistors for high power applications and the gate access has an important impact on the reliability and the lifetime of a device.

The second type of failure analysis is the electro-optical measurements. The OBIRCh technique localized defects associated to an increase in current and decrease in resistivity. However, the localized defects have shown different activation processes between the small and large devices: As for the small devices, it is noticed that the spots spread deeper into the middle of the gate finger as $|V_{GS}|$ increases (I_G increases), the phenomenon is not observed for the large devices where the defects appeared randomly throughout the gate width. This is attributed to the mono-finger property of the small devices where the mechanical attraction of the gate finger is performed directly on the pad near the finger; whereas for the large scale devices with four gate fingers, the mechanical stress is less significant since the fingers are all connected to a single pad (hence a more relaxed attach). On the other hand, the EBIC analysis is only performed on small-size devices to assess to gate leakage instabilities of GaN power devices. Further investigations are defined for the EBIC measurements to be able to reveal defects below field-plate when studying HEMTs with field plate.

All these characterization techniques take part of the ReAGaN ANR project, hence when gathering all these skills with the other partners of the project, this will lead to gain an improved understanding of physical and failure mechanisms, nature of defects and their link with the macroscopic electrical performances limiting the reliability of the devices. The project is still ongoing and an important study cases remain for better understanding the degradation mechanisms. As for our laboratory (LAAS – CNRS), new characterization techniques have been developed during the internship of Oana LAZAR that will continue this work during her thesis under the supervision of Jean-Guy TARTARIN.

PUBLICATIONS LIST

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- **S. Karboyan**, J.G. Tartarin, M. Rzin *et al*., *"Influence of gate leakage current on AlGaN/GaN HEMTs evidenced by low frequency noise and pulsed electrical measurements,"* Microelectronics Reliability, July 2013.
- B. Lambert, N. Labat, D. Carisetti, **S. Karboyan**, J.G. Tartarin, J. Thorpe, L. Brunel, A. Curutchet, N. Malbert, E. Romain-Latu, M. Mermoux, *"Evidence of relationship between mechanical stress and leakage current in AlGaN/GaN transistor after storage test,"* Microelectronics Reliability, July 2012.

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