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Strain integration and performance optimization in sub-20nm FDSOI CMOS technology

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"SiGe, il s'appelle SiGe, je suis folle de lui..."

Contents

Symbols and Acronyms

Symbol	Definition	Unit
α	Activity factor	-
γ	Body factor	V/V
$\Delta\omega_{SiSi}$	Si-Si Raman frequency peak shift	m^{-1}
ε	Strain	-
ε_0	Permittivity of vacuum	F/m
ε_{Si}	Permittivity of Silicon	F/m
η	Viscosity	Pa.s
θ_i	Mobility attenuation parameters	V^{-i}
λ (Chap.2)	Parameter of access resistance dependence with inversion charge	Ω/V
λ (Chap.3-5)	Typical relaxation length	m
λ_0	Mean free path	m
μ_0	Low-field mobility	m^2/Vs
μ_B	Apparent ballistic mobility	m^2/Vs
μ_{eff}	Effective mobility	m^2/Vs
ν	Poisson's ratio	-
Ξ	Deformation potential	eV
Π	Piezoresistive coefficient	Pa^{-1}
σ	Mechanical stress	Pa
σ (Chap.2)	Parameter of access resistance dependence with inversion charge	Ω.V
τ	Relaxation time	s
τ_P	Propagation delay	s
ϕ_f	Fermi potential	eV
ϕ_M	Metal work function	eV
ϕ_S	Semiconductor work function	eV
χ_S	Electron affinity	eV
ψ_S	Surface potential	eV
ω	RX-jog ratio	-
ω_0	Raman frequency peak of Silicon	m^{-1}
C_d	Drain capacitance	F
C_{EFF}	Effective capacitance	F
C_g	Gate capacitance	F
C_{gc}	Gate-to-channel capacitance	F
C_{ij}	Elastic constants	Pa
C_{ox}	Gate oxide capacitance	F

C_w, C_{BE}	Wire (or Back-End) capacitance	F
DIBL	Drain-Induced Barrier Lowering	V or V/V
CTE	Coefficient of Thermal Expansion	K^{-1}
E	Moung's modulus	Pa
$E_{//}$	Longitudinal field	V/m
E_C	Conduction band energy	eV
EDP	Energy Delay Product	J.s
E_{eff}	Transverse effective field	V/m
E_G	Band gap energy	eV
EOT	Equivalent Oxide Thickness	m
E_V	Valence band energy	eV
$Freq$, f	Frequency	Hz
gm	Transconductance	A/V
$\hbar$	Reduced Planck constant	J.s
I_{DDQ}	Leakage current (also called stand-by or static current)	A
I_{DYN}	Dynamic current	A
I_{EFF}	Effective drain current	A (or µA/µm)
I_{LIN}	Linear drain current	A (or µA/µm)
I_{ODLIN}	Linear drain current at a given gate overdrive	A (or µA/µm)
I_{OFF}	OFF-state current or leakage current of a MOSFET	A (or A/µm)
I_{ON}	ON-current or saturation current	A (or µA/µm)
I_{th}	Drain current criterion for threshold voltage extraction	A
k, k_B	Boltzman constant	J/K
$\mathbf{k}$	Wavevector	-
L	Transistor gate length	m
m^*	Effective mass	kg
m_0	Longitudinal mass	kg
m_l	Transverse mass	kg
m_t	Rest mass of electron	kg
N_A	Acceptor impurities concentration	A/cm^3
n_i	Intrinsic carriers concentration	cm^{-3}
P_{DYN}	Dyamic power	W
P_{STAT}	Static power	W
P_{TOT}	Total power	W
q	Elementary charge	C
Q_{DEP}	Depletion charge	C

Q_{INV}	Inversion charge	C
R_{ACC}	Access resistance	Ω (or Ω.µm)
R_{EFF}	Effective resistance	Ω (or Ω.µm)
R_{ON}, R_{TOT}	ON-resistance in linear regime and at a given gate overdrive	Ω or Ω/µm
S_{ij}	Stiffness constants	Pa^{-1}
SNM	Static Noise Margin	V
SS	Subthreshold swing	mV/dec
t_{ox}	Gate oxide thickness	m
V_B	Back-bias voltage (Body voltage)	V
v_d	Drift velocity	m/s
v_{inj}	Injection velocity	m/s
v_{sat}	Saturation velocity	m/s
v_T	Thermal velocity	m/s
V_D	Drain voltage	V
V_{DD}	Supply voltage	V
V_{FB}	Flat-band voltage	V
V_G	Gate voltage	V
V_S	Source voltage	V
V_T	Threshold voltage	V
V_{TLIN}	Threshold voltage in linear regime	V
V_{TSAT}	Threshold voltage in saturation regime	V
W	Transistor width	m
WNM	Write Noise Margin	V

Acronym	**Definition**
BEOL	Back-End Of Line
BOX	Buried OXide
CA	Active contact layer
CB	Gate contact layer
CESL	Contact Etch Stop Layer
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical-Mechanical Planarization
CPP, CGP	Contacted-Poly Pitch, Contacted Gate Pitch
CRX	Continuous-RX
DDB	Double-Diffusion Break

DFEH	Dark Field Electron Hologrpahy
DITO	Dual Isolation by Trenches and Oxidation
DTCO	Design/Technology Co-Optimization
EDX	Energy-dispersive X-ray spectroscopy
FBB	Forward Back-Bias
FDSOI	Fully Depleted Silicon On Insulator
FEOL	Front-End Of Line
FWHM	Full Width at Half Maximum
FO	Fan-Out
GAA	Gate-All-Around
GP	Ground Plane
HH	Heavy Holes
HVT	High-VT
IoT	Internet of Things
IV	Inverter
LH	Light Holes
LLE	Local Layout Effects
LOCOS	LOCal Oxidation of Silicon
LPCVD	Low-Pressure Chemical Vapor Deposition
LVT	Low-VT
M1	First level of metal
M1P	First-level metal pitch
MEOL	Middle-End Of Line
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBED, NBD	Nano-Beam Electron Diffraction
NEGF	Non-Equilibrium Green's Function
nFET, nMOS	n-type Metal Oxide Semiconductor Field Effect Transistor
PD	Pull-Down
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PED	Precession-Electron-Diffraction
pFET, pMOS	p-type Metal Oxide Semiconductor Field Effect Transistor
PG	Pass-Gate
PPA	Power/Performance/Area
PU	Pull-Up
RBB	Reverse Back-Bias
RCS	Remote Coulomb Scattering
RTO	Rapid Thermal Oxidation
RVT	Regular-VT

RX	Active area layer
S/D	Source/Drain
SA, SB	Gate-to-STI distance from left, right, side
SADP	Self Aligned Double Patterning
SAIPS	Self-Aligned In-Plane Stressor
SCE	Short Channel Effects
SDB	Single-Diffusion Break
SDRASS	Source and Drain from Recrystallization of Amorphized SiGe on SOI
SiGeOI	Silicon-Germanium On Insulator
SIT	Sidewall Image Transfer
SLVT	Super-Low-VT
SMT	Stress Memorization Technique
SOI	Silicon On Insulator
SPER	Solid Phase Epitaxial Regrowth
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SRB	Strain-Relaxed Buffer
SRS	Surface Roughness Scattering
sSOI	Strained-SOI
STI	Shallow Trench Isolation
STRASS	Strained Si by Top Recrystallization of Amorphized SiGe on SOI
TEM	Transmission Electron Microscopy
TU	Tucked-Under
UTBB	Ultra-Thin Body and Buried oxide
XRD	X-Ray Diffraction

Introduction

Context

For the past 50 years, the semiconductor industry has known an exponential growth that has affected our everyday life. From the discovery of the transistor effect by W. Shockley, J. Bardeen and W. H. Brattain at the Bell Labs in 1947, the first microprocessor was manufactured by Intel in 1971, embedding around 2300 transistors (Intel 4004). Today, a microprocessor can count more than 7 billion transistors (22-core Xeon Broadwell-E5 from Intel) and the global semiconductor industry sales raised to $335.2 billion in 2015. Such a growth has been enabled by an aggressive scaling of the integrated circuit dimensions. This so-called "happy scaling" has lost its efficiency to keep reducing the power consumption. Innovations were required, especially during the last decade when physical barriers had to be pushed back. As a result, the technology complexity has increased and different ingredients have been implemented.

In this context, the introduction of new transistor architectures has been necessary to meet the requirements both in terms of density and performance. Especially, the Fully Depleted Silicon On Insulator (FDSOI) technology has appeared as an alternative to the FinFET to succeed the historical planar bulk technologies. FDSOI technology has several strengths such as a good electrostatic control, a low variability and a great back-biasing capability. In addition to the change of transistor architecture, the use of strain as a performance booster has been widely discussed and is today mandatory in advanced technology. The work of this thesis deals with the strain integration in Fully Depleted Silicon On Insulator technology in order to boost and optimize the performance.

Manuscript organization

The manuscript is organized as follows:

The **first chapter** details the context of this work. The basics of the Complementary Metal Oxide Semiconductor (CMOS) technology are presented. First, a focus is made on the principle of operation of the field effect transistor, which is the key element for digital computing. Then, the CMOS technology evolution through the well-known scaling is depicted. Finally, the interest of strain integration to boost the performance is discussed.

The **second chapter** focuses on the performance of strained devices. In particular, the impact of strain on carrier mobility is investigated. A dedicated attention is paid on the electrical characterization of short channel transistors, emphasizing the crucial role of the access resistance and its strain dependence.

The **third chapter** discusses the use of strained SiGe channel in FDSOI technology. After presenting the FDSOI technology, a focus is made on the strain measurement and modelling in patterned SiGe active areas. An extensive study of the strain-induced layout effects is finally presented.

The **fourth chapter** aims at providing solutions to boost the performance of scaled devices embedding strain. This chapter is splitted into two main parts: design- and technology-based solutions.

In the **fifth and last chapter**, new strain integration techniques in FDSOI technology are investigated. In particular, a focus is made on tensile strain generation. For instance, the BOX-creep technique is assessed though mechanical simulations and experimental results. Finally, the great back-biasing capability of FDSOI technology is evaluated in a dynamic approach enabled by 3D monolithic.

This work has been carried out in STMicrolectronics, Crolles, and in the CEA-LETI, Grenoble.

CHAPTER 1

Boosting sub-20nm CMOS technology performance: the relevance of strain

Contents

In this Chapter, the context of this thesis work is presented. The CMOS logic is first introduced, focusing on the MOSFET principle of operation and the main metrics used for its assessment. Then, the second section provides a brief history of the CMOS technology scaling. Finally, the last section gives some insights about the strain integration in CMOS technology.

1.1 Introduction to CMOS logic

The aim of this section is to provide the basics of CMOS logic. Especially, the operation of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is presented. First, the use of the MOSFET as a switch to perform logic operations is detailed. Then, the MOSFET metrics and figures of merit are discussed with a particular attention on the crucial role of carrier mobility. Finally, a focus is made on the different metrics of digital CMOS integrated circuits in terms of performance and power consumption.

1.1.1 The MOSFET, device at the heart of logic

1.1.1.a The MOSFET switch

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the key element of integrated circuits. It features 4 terminals which are the Gate (G), the Source (S), the Drain (D) and the Body (B). A schematic of the transistor is given in Figure 1.1. According to the voltage applied on the gate, an electrical current is allowed to flow or not from the source to the drain. As a result, the MOSFET can be considered as a switch between an OFF state and an ON state.

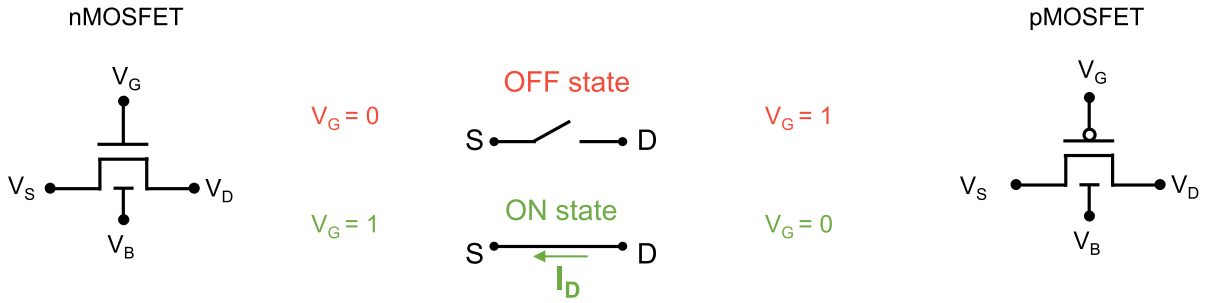


Figure 1.1: Schematic of the MOSFET, made of 4 terminals: Gate, Source, Drain and Body. The MOSFET is considered of a switch whose state ON or OFF is controlled by the gate voltage V_G. An nMOSFET (pMOSFET) is OFF if V_G="0" (V_G="1") and turned ON if V_G="1" (V_G="0"), respectively. The n- and p-MOSFETs behave complementary, hence the name CMOS technology.

The MOSFET can either be of n- of p-type depending on the carrier type in the source/drain and body. An nMOSFET (also called nMOS or nFET) consists in n-type source and drain, and a p-type body. The major carrier in the source and drain reservoirs are thus electron. It is the opposite for a pMOSFET, featuring p-type source and drain (hole reservoirs) and n-type body.

The nMOSFET is in OFF state if a "0" is applied on its gate. In this case, it acts as an open switch, i.e. no current flows. On the other hand, if a "1" is applied on the gate, the switch is closed, allowing a current to flow between the source and the drain. It is the exact opposite for the pMOSFET, which is in OFF (ON) state if a "1" ("0") is applied on the gate, respectively. As a consequence, the

nMOSFET and pMOSFET are complementary (hence the CMOS technology). This is summarized in Figure 1.1.

1.1.1.b Boolean functions using logic combinatory gates

In the CMOS technology, the two types of MOSFET are enjoyed to achieve Boolean functions using logic gates. The most simple logic gate is the inverter. As its name indicates, the inverter output is the inverse of its input. The inverter is made with one nMOS transistor and one pMOS transistor, as shown in Figure 1.2. The nMOS source is connected to the ground (G_{ND}) while the pMOS one is connected to the supply voltage V_{DD}. Both nMOS and pMOS gates are connected to the input (A) and both drains to the output (Z). This way, if the input is "0", the nMOS is OFF and the pMOS ON. The output is thus pulled up to V_{DD}, i.e. "1". If the input is "1", the pMOS is open (i.e. OFF) and the nMOS is closed (i.e. ON), pulling down the output to "0", since it is connected to the ground. The inverter output is thus well given by $Z=\overline{A}$.

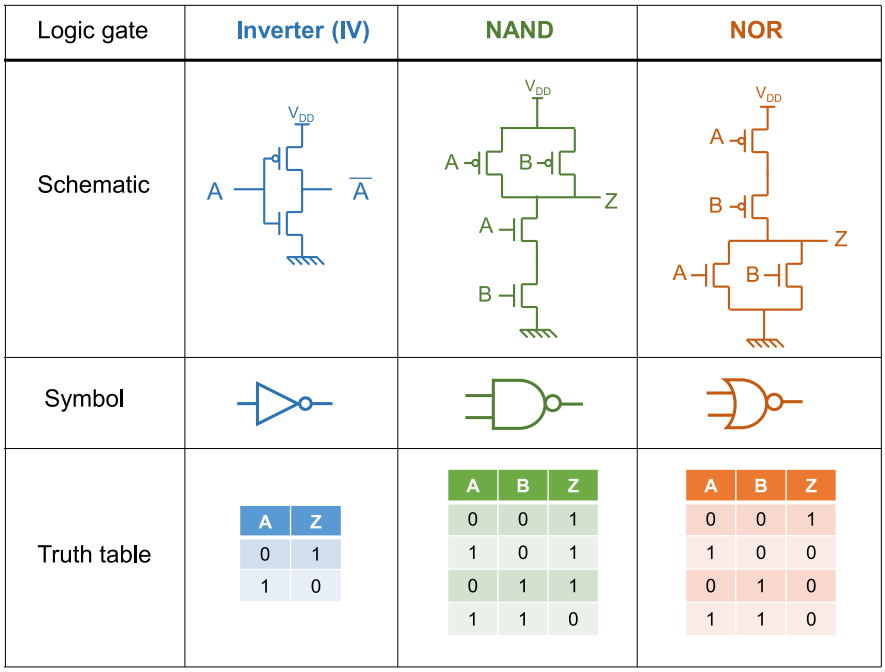


Figure 1.2: Schematic, symbol and truth table of inverter, NAND and NOR logic gates. The nMOSFET network is called pull-down because it connects the output to the ground and the pMOSFET network is called pull-up because it connects the output to the supply voltage V_{DD}. The transistors inside networks are connected in series or in parallel according to the logic function.

Figure 1.2 algo gives the schematic, symbol and truth table of the NAND and NOR 2-input logic gates. The NAND logic gate consists in two pMOSFETs in parallel and two nMOSFETs in series. It is the opposite for the NOR gate. The input A is connected to the gate of one pFET and one nFET and the remaining two gates are connected to the second input B. Let us consider a NOR gate. If either A or B is "1", at least one nFET is ON, creating a path from the ground to the output (i.e. Z="0"). The output is pulled-up to V_{DD} if and only if both inputs A and B are "0" since the two pMOS transistors are in series.

The pMOSFET network is called the pull-up network because it connects the output to the supply

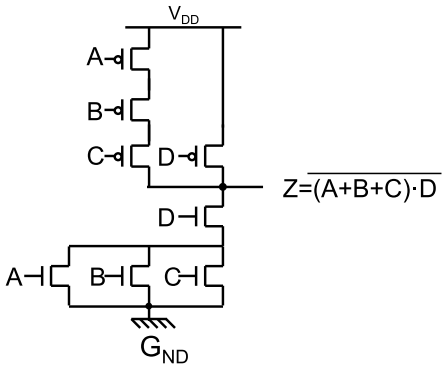


Figure 1.3: Schematic of the OR-AND-INVERT-31 (OAI-31) compound gate. The logic function is achieved by relevantly building the pull-down and pull-up networks. Transistors in series in the pull-up network are in parallel in the pull-down network and vice versa.

voltage V_{DD} and the nMOSFET network is called the pull-down because it connects the output to the ground G_{ND}. More complex logic functions can be achieved by using pull-up and pull-down networks made of transistors in series or in parallel. Figure 1.3 shows the example of the compound gate achieving the function $Z=\overline{(A+B+C)\cdot D}$. This logic compound gate is called OR-AND-INVERT-31 or OAI-31. In the pull-down network, the 3 inputs A, B and C built in parallel are connected in series with the fourth input D. It is the opposite for the pull-up network. The logic function of OAI-31 could have been achieved with several logic gates such as inverter or NOR. However, it would have required to use more transistors. Hence the interest of relevantly using pull-up and pull-down networks.

1.1.2 The Power/Performance/Area metrics

In this section, a focus is made on the Power/Performance/Area (PPA) metrics. These metrics are of great interest to characterize a CMOS technology [1].

1.1.2.a Power/Performance: the ring-oscillator metrics

In a digital integrated circuit, the logic gates are used for operating boolean functions. The circuit speed is directly linked to the ability of the logic gates to perform their operation. The ring-oscillator is a device enabling a dynamic characterization [Sai15]. It consists in a circular chain made of an odd number of inverters. Figure 1.4 shows an example with three inverters. The output of the last inverter is connected to the input of the first inverter. This way, the output is not stable as it will oscillate between the "1" and "0" states (i.e. V_{DD} and G_{ND}). The oscillation frequency $Freq$ (or f) depends on the number of inverters N and the propagation delay of each inverter τ_P:

$$Freq = \frac{1}{2.N.\tau_P} \tag{1.1}$$

When the inverter is not switching (i.e. input and output are at a fixed value), the current flowing through the inverter is the leakage current I_{DDQ}. This current is also referred as the stand-by or static current. It is measured through the supply voltage in the quiescent state (hence the name

1 In addition to the Power/Performance/Area metrics, the Cost, Yield and also Reliability are sometimes also mentioned.

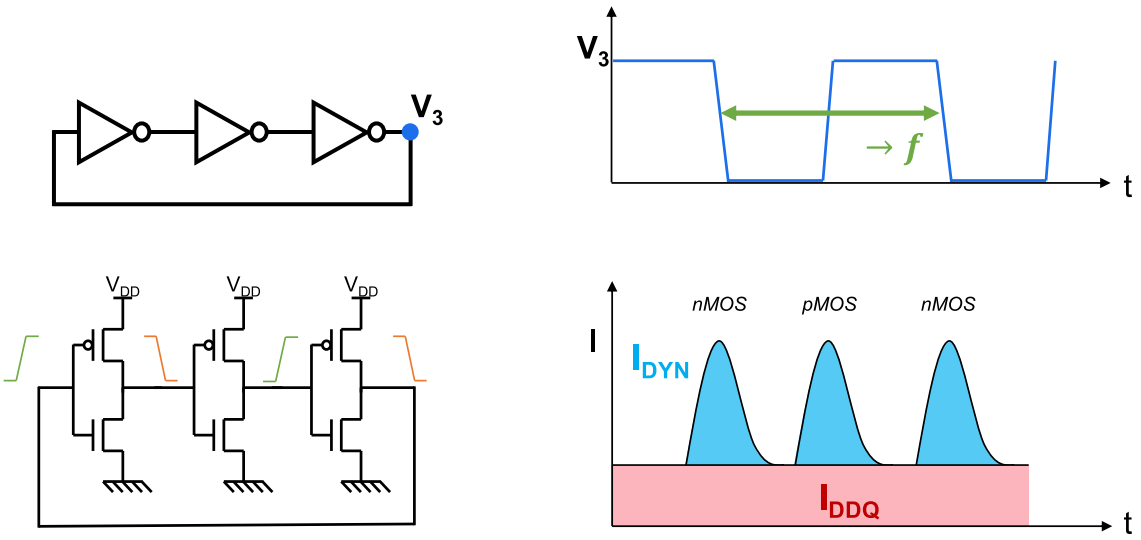


Figure 1.4: (left) symbolic and schematic views of a ring-oscillator made of three inverters. (right) Voltage at the output of the third inverter as a function of time, oscillating between "1" (V_{DD}) and "0" (G_{ND}) at a frequency f. The current flowing through an inverter is composed of the dynamic current I_{DYN} and the static current I_{DDQ}. The dynamic current is the drive current of either the pMOS or the nMOS to load the output capacitance (i.e. the gates from the next level inverter) during a switching and the static current is the leakage when the inverter is not active.

I_{DDQ}). This leakage current is directly linked to the nMOS and pMOS leakage currents I_{OFF}, defined in section 1.1.3.

When a stage of inverter is switching because of a change of input, a dynamic current loads the output capacitance. In a ring-oscillator, this dynamic current I_{DYN} is successively generated by each inverter stage. It flows alternatively through the nMOS (pull-down) and the pMOS (pull-up) according to the switching operation ("0" to "1" or "1" to "0"). I_{DYN} is measured through V_{DD} [1]. The delay can be expressed as a function of the dynamic current [2]:

$$\tau_P = \frac{V_{DD}\, C_{EFF}}{2\, I_{DYN}} \tag{1.5}$$

where C_{EFF} is the effective capacitance to be loaded. This capacitance includes the gate capacitance of the next level inverter (the active part) and all parasitic capacitances (discussed later on in section 1.2.4).

1 Even though no current flows through V_{DD} when the output capacitance is discharged by the nMOS (the current flows through the output to the ground), it is the exact same current that is injected from the supply voltage to load the capacitance. That is why I_{DYN} can be measured through V_{DD}.

2 Starting from:

$$-I = C_{EFF}\frac{\mathrm{d}V}{\mathrm{d}t} \tag{1.2}$$

and by defining I_{DYN} as the average current during the switching and integrating:

$$-I_{DYN}\tau_P = C_{EFF}\int_0^{\tau_P}\frac{\mathrm{d}V}{\mathrm{d}t}dt \tag{1.3}$$

One can also write:

$$\tau_P = R_{EFF}\, C_{EFF} \tag{1.6}$$

with $R_{EFF} = \frac{V_{DD}}{2\, I_{DYN}}$.

In terms of power, the dynamic and static powers are deduced from the currents. The dynamic power is given by:

$$P_{DYN} = I_{DYN}\, V_{DD} = \frac{{V_{DD}}^2 \cdot C_{EFF}}{2\, \tau_P} \tag{1.7}$$

and the static power by:

$$P_{STAT} = I_{DDQ} V_{DD} \tag{1.8}$$

The total power of a circuit depends on the activity factor α:

$$P_{TOT} = \alpha P_{DYN} + P_{STAT} \tag{1.9}$$

This activity factor depends on the application. Finally, the Energy-Delay-Product EDP, defined as

$$EDP = E \cdot \tau_P = P_{TOT} \cdot \tau_P \cdot \tau_P \tag{1.10}$$

is a good figure of merit for energy efficient circuits. Its minimum translates the sweet point between consumption and performance.

1.1.2.b Area: standard cell design

In the previous paragraph, the dynamic power/performance metrics have been presented. In this paragraph, the last term of PPA, i.e. the Area, is discussed by the means of a typical layout of a standard cell. A standard cell consists in a physical implementation of a function operated by transistors. Standard cells include combinatory logic (e.g. inverter, NAND, NOR) and sequential logice or storage (e.g. flipflops) functions. Figure 1.5 shows the layout of the 1-finger inverter standard cell (also called IV-SX1).

The main layers are represented on the layout: active area (RX), gate (or poly, PC), active contact (CA), gate contact (CB), first level of metal (M1). The active areas are isolated from each other by the means of Shallow Trench Isolation (STI). The pMOS and nMOS sources are connected to the power rails (power supply V_{DD} for pMOS and ground G_{ND} for nMOS). The function of a standard cell is determined by the way the transistors are connected to each other with the metal lines. In

which leads to:

$$-I_{DYN}\tau_P = C_{EFF}\left[V(\tau_P) - V(0)\right] = C_{EFF}\left[\frac{V_{DD}}{2} - V_{DD}\right] \Leftrightarrow \tau_P = \frac{V_{DD}\, C_{EFF}}{2\, I_{DYN}} \tag{1.4}$$

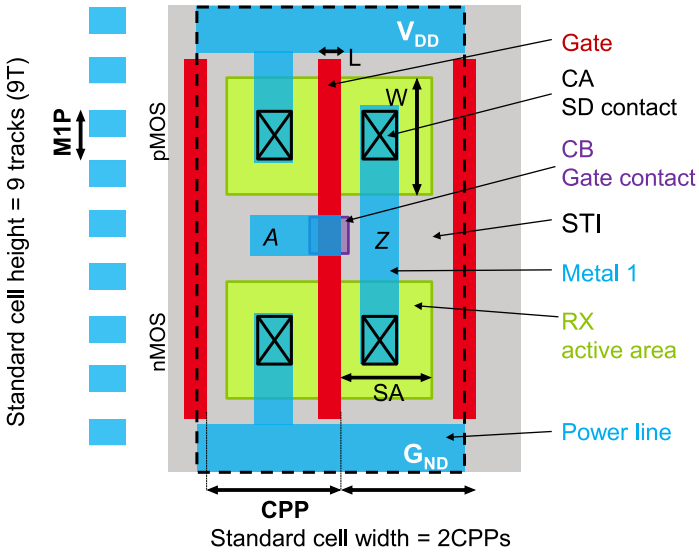


Figure 1.5: Layout of the 1-finger inverter standard cell. The pMOS and nMOS are designed between the two power rails. The standard cell height is expressed as a function of the number of Metal-1 pitches and its width is expressed as a function of the number of poly pitches (CPPs).

the case of the inverter, the pMOS and nMOS drains are connected to the output. In an integrated circuit, the standard cells are abutted to each other and can be flipped in order to share the power rails.

The area of a standard cell is defined by its height and width. The height is expressed as a function of the number of M1 pitches (M1P), also called tracks[1], and the width as a function of the number of Contacted Poly Pitches (CPPs). The product M1P×CPP is therefore a good figure of merit of a technology density, i.e. node. The area of the Static Random Access Memory (SRAM) cell (see appendix B) is also a good indicator of a technology density.

In advanced technologies, efforts have been made on the optimization of the standard cell rather than only focusing on the transistor. This is referred as the Design/Technology Co-Optimization (DTCO).

1.1.3 The MOSFET operation and metrics

In the previous section, the MOSFET has been presented as an ideal switch that is used in the CMOS technology to perform logic operations. The aim of this section is to provide some insights about the MOSFET operation and the main metrics used in this work. A more detailed theory and modeling of the MOSFET transistor can be found in [Sko00] and [Hu10].

1.1.3.a The MOSFET structure

An illustration of a MOSFET device is shown in Figure 1.6. The control electrode, i.e. the gate, consists in a Metal Oxide Semiconductor (MOS) capacitance, whose geometry is defined according to the gate length L and transistor width W. The gate oxide is characterized by its thickness t_{ox}, which is crucial for the device performance. The two reservoirs of carrier, i.e. the source and drain,

1 In a FinFET technology (see section 1.2.3.a), the height of standard cell is a multiple of the fin pitch.

are placed at each side of the gate. Figure 1.6 also shows a typical layout of a transistor. The active area is represented in green and the gate in red.

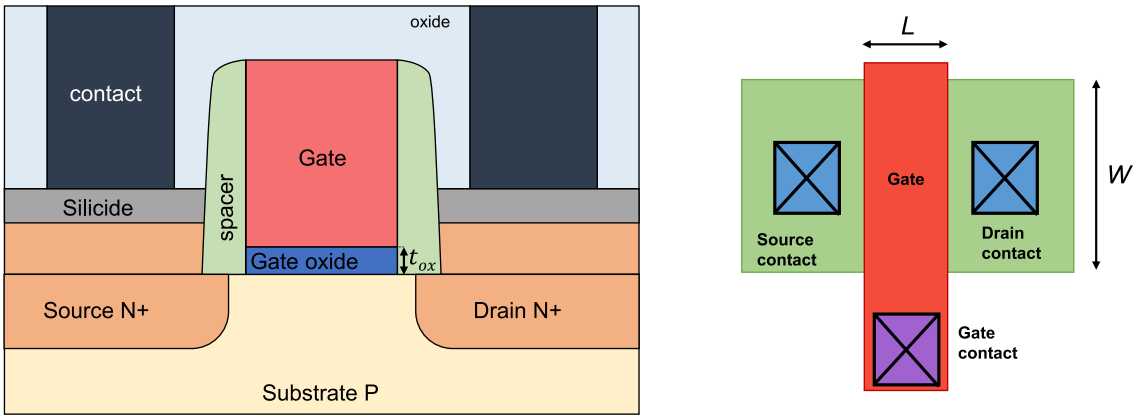


Figure 1.6: Illustration of typical MOSFET (left) cross-section and (right) top-view, i.e. layout.

1.1.3.b The MOSFET operation

The MOS capacitance can operate in different regimes, according to the potential at the semiconductor/oxide interface ψ_s, dependent on the gate voltage V_G. Let us consider a MOS with a p-type semiconductor, which is the case of the nMOSFET. The three regimes are:

- *The accumulation* ($\psi_s < 0$; $V_G < V_{FB}$). The majority carrier (holes in a p-type substrate) are attracted by the electric field towards the gate. The flat-band voltage V_{FB} is defined as the gate voltage that must be applied in order to have a flat energy band in the semiconductor, (i.e. no charge in the capacitor). Figure 1.7 shows the band diagram of the MOS structure under flat-band condition and accumulation. The band diagram from the source to the drain is also represented. A barrier of potential prevents the electron to flow from source to drain. The MOSFET is in OFF state.
- *The depletion* ($0 < \psi_s < \phi_f$; $V_G > V_{FB}$). ϕ_f is the Fermi potential, given by $\phi_f = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$ where N_A is the dopant concentration is the substrate. Under the depletion regime, majority carriers are pushed away from the oxide/semiconductor interface. The charge in the semiconductor is due to the ionized dopants (negative charge in the case of an nMOSFET).
- *The inversion* ($\psi_s > \phi_f$; $V_G >> V_{FB}$) or strong inversion ($\psi_s > 2 \cdot \phi_f$). In inversion, the previously minority carriers become more numerous. In strong inversion, there are more minority carriers (electrons) than majority carriers (holes) in the bulk. A conduction path, called the channel, appears. The electrons are allowed to flow between the source and drain as illustrated in Figure 1.7. The MOSFET is in ON state.

The threshold voltage is defined as the criterion of strong inversion. In the case of the historical planar bulk[1] technology, the threshold voltage is defined by :

$$V_T = V_{FB} + 2\phi_f + \frac{Q_{dep}}{C_{ox}} \tag{1.11}$$

1 For the threshold voltage of FDSOI MOSFET, see equation 1.31

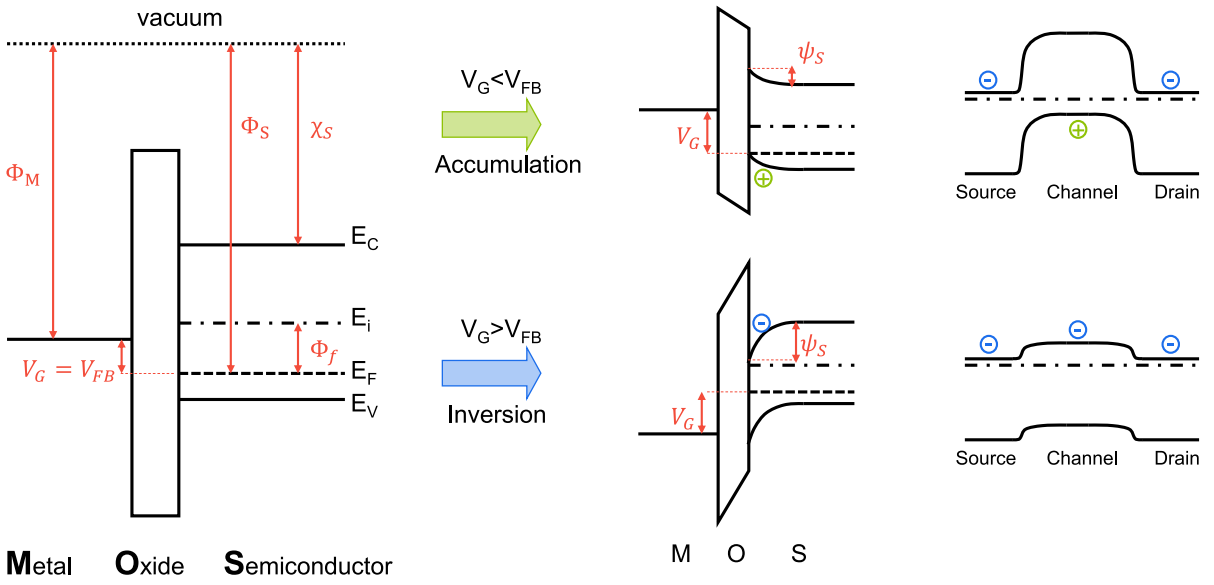


Figure 1.7: (left) Band diagram of the MOS structure under flat band condition. ϕ_M and ϕ_S are the metal and semiconductor work functions, respectively. χ_S is the electron affinity. ϕ_f is the Fermi potential. E_F is the Fermi level. E_i is the intrinsic Fermi level. E_C is the bottom of the conduction band and E_V the top of the valence band. (right) Band diagrams of a MOSFET in (top) accumulation or OFF state, i.e. no current from source to drain, and (bottom) inversion or ON state, i.e. carriers are free to flow from source to drain because of the reduced potential barrier.

where $V_{FB} = \phi_M - \left(\chi_S + \frac{E_g}{2} + \phi_f\right)$, Q_{dep} is the charge of depletion and C_{ox} the gate oxide capacitance.

1.1.3.c The MOSFET principal metrics

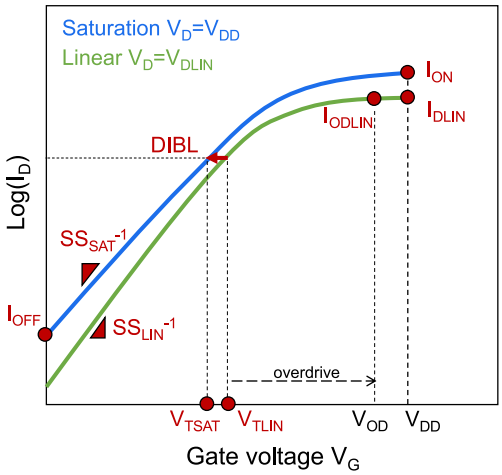
The ideal MOSFET switch is closed (i.e. ON) if the gate voltage is above V_T and open (i.e. OFF) otherwise. Actually, a real MOSFET is not an ideal switch. It exhibits a leakage current in OFF state, a relatively smooth transition from OFF to ON states, and can provide a limited current in ON state. This is illustrated on the $I_D(V_G)$ curve in log scale, also called transfer characteristic, of Figure 1.8. Two regimes are distinguished:

- The linear regime, where the voltage applied on the drain is small (typically less than 50mV)
- The saturation regime, where the voltage applied on the drain is V_{DD}.

A MOSFET is characterized by different parameters that allow its performance to be evaluated. Most of these parameters can be directly extracted from electrical measurements. The table of Figure 1.8 defines the main electrical characteristics of a transistor.

As far as the threshold voltage is concerned, it is usually extracted at a given current of value I_{th}, whose value is typically 100nA$\cdot\frac{W}{L}$. In the subthreshold regime, the drain current increases exponentially with the gate voltage. We can express the drain current as:

$$I_D = \frac{W}{L}\mu_0 C_{dep}\left(\frac{kT}{q}\right)^2\left(1-\exp\left(\frac{-qV_D}{kT}\right)\right)\cdot\left(\exp\left(q\frac{V_G - V_T}{(1+\frac{C_{dep}}{C_{ox}})kT}\right)\right) \tag{1.12}$$



Parameter	Definition	V_G	V_D	Typical unit
I_{OFF}	OFF current or leakage current	0	V_{DD}	A/µm
I_{ON}	ON current or saturation current	V_{DD}	V_{DD}	µA/µm
V_{TSAT}	Threshold voltage in saturation regime		V_{DD}	V
V_{TLIN}	Threshold voltage in linear regime		V_{DLIN}	V
SS_{SAT}	Subthreshold swing in saturation regime		V_{DD}	mV/dec
SS_{LIN}	Subthreshold swing in linear regime		V_{DD}	mV/dec
I_{DLIN}	Linear drain current	V_{DD}	V_{DLIN}	µA/µm
I_{ODLIN}	Linear drain current at a given overdrive V_G=V_{TLIN}+V_{OD}	V_{TLIN} + V_{OD}	V_{DLIN}	µA/µm
R_{ON}=R_{TOT}	ON resistance or total resistance =V_{DLIN}/I_{ODLIN}	V_{TLIN} + V_{OD}	V_{DLIN}	Ω.µm

Figure 1.8: (left) MOSFET $I_D(V_G)$ curves in linear and saturation regimes, also called transfer characteristics. (right) Table of the main electrical metrics of the MOSFET, also shown on the $I_D(V_G)$ curve.

where μ_0 is the low-field mobility and C_{dep} the capacitance of depletion.

The subthreshold swing SS, translating the exponential increase of the drain current with respect to the gate voltage, is defined as:

$$SS = \frac{\mathrm{d}V_G}{\mathrm{d}\log(I_D)} \tag{1.13}$$

and can be expressed according to 1.12 as:

$$SS = \frac{kT}{q}\ln(10)\frac{\mathrm{d}V_G}{\mathrm{d}\psi_S} = \frac{kT}{q}\ln(10)\left(1+\frac{C_{dep}+C_{ss}}{C_{ox}}\right) \tag{1.14}$$

where C_{ss} is the capacitance related to the surface states. By neglecting C_{ss} and C_{dep} the theoretical subthreshold swing is SS=60mV/dec. The subthreshold swing is a good indicator of the electrostatic control. The current in the subthreshold regime can be expressed according to the subthreshold swing by:

$$I_D = I_{th}\exp\left(\frac{V_G - V_T}{SS/\ln(10)}\right) \tag{1.15}$$

which leads to the expression of the leakage current (assuming an OFF state in the subthreshold regime):

$$I_{OFF} = I_{th}\exp\left(\frac{-V_T}{SS/\ln(10)}\right) \tag{1.16}$$

In the strong inversion, the linear drain current can be written as:

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \tag{1.17}$$

with μ_{eff} the effective mobility of the carriers in the channel. More details about the physics of carrier mobility is given in section 1.1.3.g.

Rather than the linear drain current, the I_{ODLIN} current is preferred in order to have an image of the mobility in a MOSFET device. The I_{ODLIN} current is measured at a given overdrive $(V_G - V_T)$. This way, the current value is free from threshold voltage variation.

The historical metric of performance is the ON current I_{ON}, also called the saturation current. It is the drain current at $V_G = V_D = V_{DD}$.

1.1.3.d The effective drive current in an inverter

Actually, in an inverter, the input and output voltages vary as the MOSFET current is loading the output capacitance. In other words, the MOSFET does not operate at a given bias configuration in dynamic. The parameters presented in Figure 1.8 are all DC parameters, i.e. obtained from static measurements. Na et al. [Na02] proposed a DC approximation of the drive current in an inverter. The inverter switching delay τ_P is defined as the delay between the point where the input voltage $V_{IN} = \frac{V_{DD}}{2}$ and the point where the output voltage $V_{OUT} = \frac{V_{DD}}{2}$. This is represented in Figure 1.9.

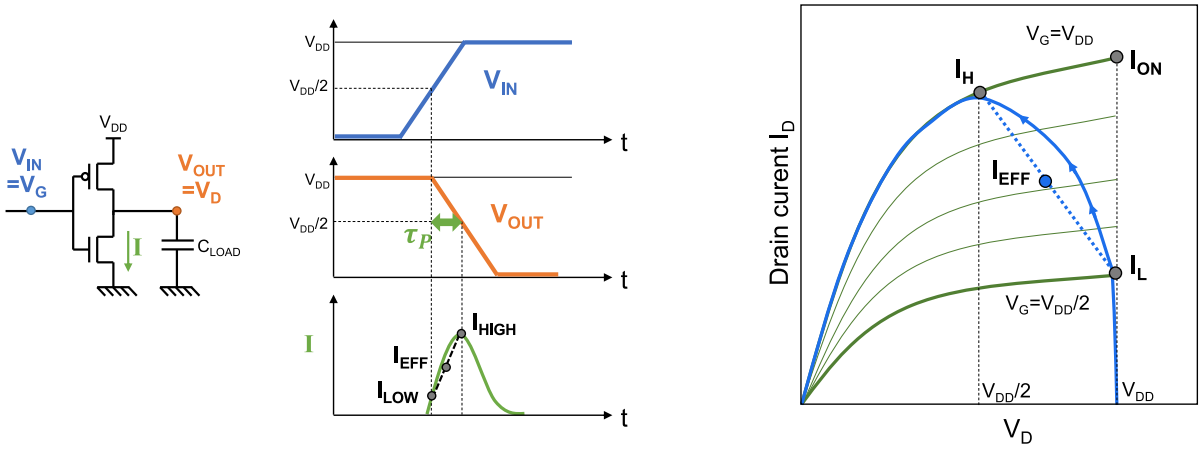


Figure 1.9: Illustration of the effective drive current in an inverter [Na02]. I_{EFF} is a DC approximation of the average drain current during the switching delay τ_P (also called propagation delay).

The effective drive current I_{EFF} is the average of the drain current during the switching. It is approximated by:

$$I_{EFF} = \frac{I_H + I_L}{2} \tag{1.18}$$

where

$$\begin{cases} I_H = I_D \left[V_G = V_{DD} \ ; \ V_D = \frac{V_{DD}}{2} \right] \\ I_L = I_D \left[V_G = \frac{V_{DD}}{2} \ ; \ V_D = V_{DD} \right] \end{cases} \tag{1.19}$$

Although the I_{EFF} current is a relevant approach, it has been shown that it can deviate from the actual drive current in an inverter [Gwo08]. This is because the drain current trajectory of Figure

1.9 is impacted by the capacitance to load.

1.1.3.e The importance of the electrostatic control

In a short channel MOSFET, the control of the channel potential by the gate is not as efficient as for long channel devices. This is illustrated in Figure 1.10. The Short Channel Effect (SCE) translates the fact that the shorter the gate length, the lower the barrier from the source to the channel. This is due to the band curvature induced by the source-channel and drain-channel PN junctions and results in a lower threshold voltage for short channel devices.

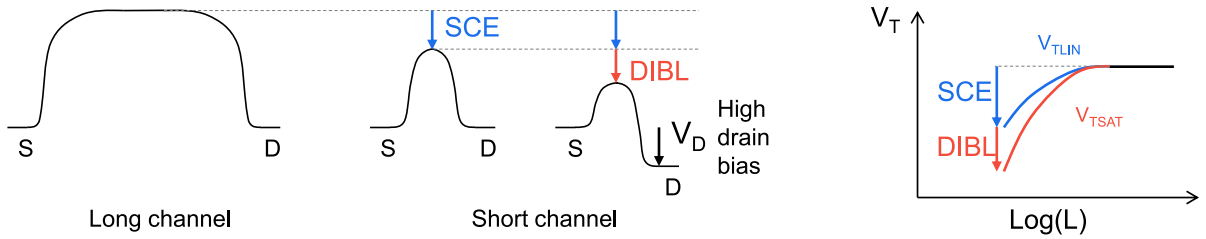


Figure 1.10: Top of the band schematic. The potential barrier is lowered for short channel (Short Channel Effect, SCE) and under a drain bias (Drain-Induced Barrier Lowering, DIBL).

In addition, the barrier further reduces when a high voltage is applied on the drain. This effect is called the Drain-Induced Barrier Lowering (DIBL). The DIBL is thus defined as the difference between the threshold voltage extracted in linear regime V_{TLIN} and the one extracted in saturation regime V_{TSAT}:

$$\text{DIBL} = \left| \frac{V_{TSAT} - V_{TLIN}}{V_{DSAT} - V_{DLIN}} \right| \tag{1.20}$$

The DIBL is also sometimes expressed in mV according to $DIBL = |V_{TSAT} - V_{TLIN}|$. A low DIBL value is an evidence of a good electrostatic control. It is crucial for the performance of the MOSFET since it impacts its effective drive current. At a given leakage I_{OFF} and ON current I_{ON}, the I_H current is strongly impacted by the DIBL, as illustrated in Figure 1.11 (because of higher V_T for V_D=V_{DD}/2 than for V_D=V_{DD}).

1.1.3.f The performance/leakage trade-off

Finally, the main figure of merit of the MOSFET is the trade-off between performance and leakage (Figure 1.12). The best performance, i.e. the highest effective drive current, is wanted at the lowest leakage. A CMOS technology offers different V_T flavors in order to cover a large range of performance/leakage. This is interesting for designing efficient circuits, depending on the application [1]. High-V_T (HVT) are suitable for low power and Low-V_T (LVT) for high performance.

1 Mixing different V_T flavors is also efficient for enhancing the circuit performance thourgh critical path optimization [Wei98]

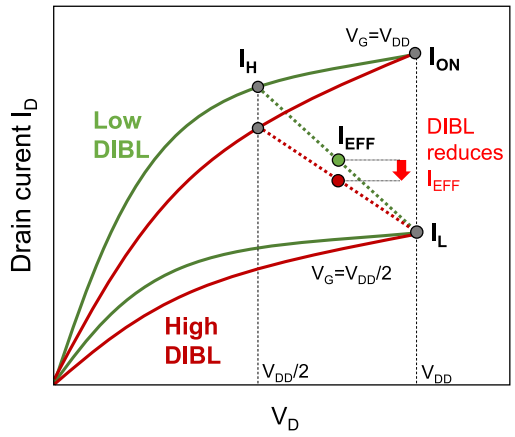


Figure 1.11: Illustration of the impact of the DIBL on the effective current I_{EFF}. A weak electrostatic control, i.e. high DIBL, is translated into I_{EFF} degradation (same leakage is considered).

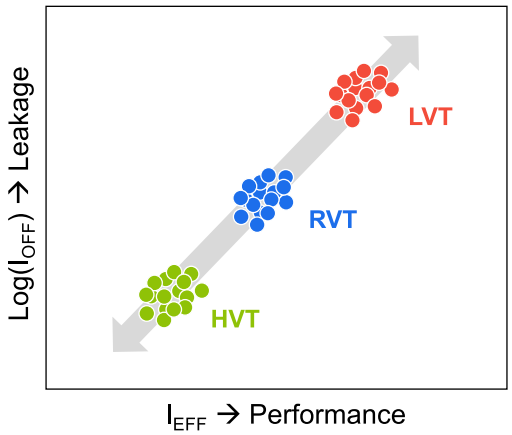


Figure 1.12: Performance/Leakage trade-off. A large range is covered thanks to multi V_T flavors (HVT=High-V_T, RVT=Regular-V_T and LVT=Low-V_T).

1.1.3.g The crucial role of carrier mobility

The mobility μ characterizes the ability of a carrier (electron or hole) to move under an electric field E. The drift velocity is therefore given by:

$$v_d = \mu E \tag{1.21}$$

In a semiconductor, the carriers experience several scattering mechanisms. Among them, the main scattering mechanisms present in a MOSFET channel are:

- Remote Coulomb scattering or interactions with ionized impurities (or any charged element like traps for instance). The ionized impurities in a MOSFET are typically the dopants. As a carrier is flowing, it can be deflected by the Coulomb forces induced by a ionized dopant.
- Phonon scattering. Phonons are acoustic waves created by the vibrating atoms of the crystal lattice. The more the carriers are interacting with phonons, the lower the mobility. At low temperature, the crystal vibration is decreased, which results in less phonons and thus in higher mobility.
- Surface Roughness scattering. The roughness of the oxide/semiconductor interface causes fluctuations of the energy levels. The more the carrier are located close to the interface, the more they are subjected to surface roughness scattering. Such a scattering mechanism thus limits the carrier mobility especially under high transverse electric field (i.e. in strong inversion).

These scattering mechanism dependence with the transverse field and the temperature are different [Che96; Tak94b].

The carrier mobility can be given by:

$$\mu = \frac{q \cdot \tau}{m^*} \tag{1.22}$$

where q is the elementary charge, τ the average time between two interactions (also called average

scattering time or average free time of flight) and m^* the effective mass. The carriers in the crystal are not free since they interact with the lattice. The effective mass is the mass of the carrier assumed to be free and accounting for the aforementioned interactions with the crystal. It can be derived from the curvature of the band structure E(**k**):

$$\mathrm{E}(\mathbf{k}) = \mathrm{E}_0 + \frac{\hbar^2 \mathbf{k}^2}{2m^*} \tag{1.23}$$

In an operating MOSFET, the carriers can be subjected to several sources of scattering at the same time. The Matthiessen's rule allows to combine their effects according to:

$$\frac{1}{\mu} = \sum_i \frac{1}{\mu_i} \tag{1.24}$$

with μ_i the mobility associated to the i scattering mechanism. The Matthiessen's rule is an approximation since it assumes no interaction between the different scattering mechanisms.

Figure 1.13 illustrates the electron effective mobility in a MOSFET according to the effective transverse field. The transverse field E_{eff} is given by:

$$E_{eff} = \frac{\eta Q_{DEP} + Q_{INV}}{\varepsilon_{Si}} \tag{1.25}$$

where η is an empirical parameter relating the average field in the inversion layer and whose value is 1/2 for electrons and 1/3 for holes. Under high transverse field, the mobility is not impacted by the remote Coulomb scattering. It is thus independent of the doping level. The mobility of Si/SiO_2 MOSFETs follows an universal mobility trend with respect to the effective field [Tak94a; Tak94b].

In a CMOS technology, there are numerous elements that can affect the scattering mechanisms such as the level of doping in the substrate, the metal used in the gate stack or the level of strain in the device. The latter will be discussed in section 1.3.2.

Actually, the equation 1.21 is no longer valid under a high longitudinal electric field. When the carrier exhibits a high kinetic energy, the interaction with phonons is predominant and the carrier velocity saturates. The saturation velocity v_{sat} is typically $\approx 10^7$cm/s for electrons in Silicon and the critical electric field is approximately $\approx 10^4$V/cm. If the carrier velocity is limited by v_{sat}, the drain current is expressed as:

$$I_D = W\, Q_{INV}\, v_{sat} \tag{1.26}$$

In the current CMOS technologies, short channel devices are operating close to the saturation regime. The carrier mobility may not be the most relevant indicator of performance. Nevertheless, it has been showed that the saturation current is still highly correlated to the mobility in short channel devices [And05; Loc02].

The transport can also be discussed under ballistic considerations. If the channel length is shorter than the mean free path between two scattering events, the carriers can move from the source to

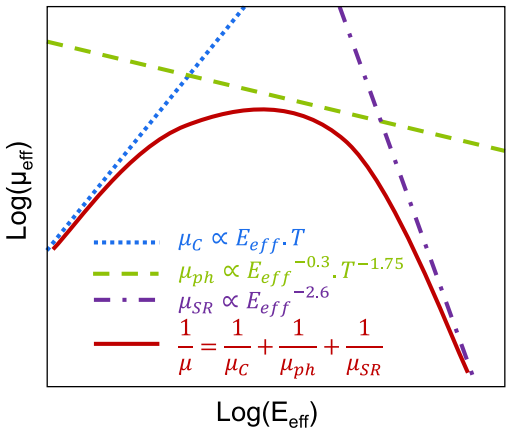


Figure 1.13: Illustration of the electron effective mobility dependence with the transverse electric field. The total mobility is derived from the three components (remote Coulomb, phonons, surface roughness) according to Matthiessen's law. The dependence with temperature and field is specific to each scattering mechanism [Che96; Tak94b].

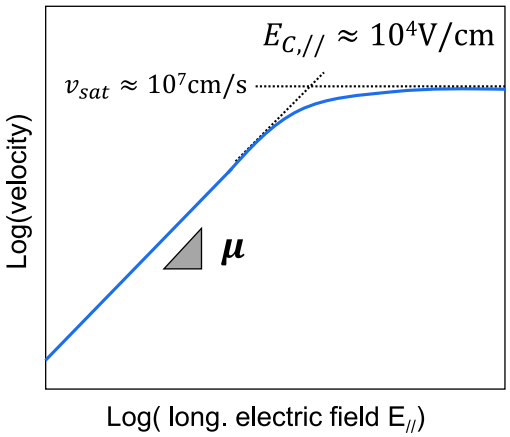


Figure 1.14: Carrier velocity as a function of the longitudinal electric field. Below the critical field, the velocity is directly proportional to the field through mobility. The velocity saturates under high field.

the drain without experiencing any interaction. In that case, the current is limited by the injection velocity v_{inj}:

$$I_D = W\, Q_{INV}\, v_{inj} \tag{1.27}$$

This expression can been used to reproduce the transistor characteristics with the help of a simple compact model [Kha09] [1].

If only a part of the carriers experiences ballistic transport, it can be relevant to introduce the channel back-scattering coefficient r (which depends on the mobility) and write the expression of the current as [Lun01]:

$$\begin{cases} I_D = W\, Q_{INV}\, \dfrac{v_T}{2kT/q}\,(1-r)\,V_D \;;\; r = \dfrac{L}{L+\lambda_0} & \text{in linear regime} \\ I_D = W\, Q_{INV}\, v_T \left(\dfrac{1-r}{1+r}\right) \;;\; r = \dfrac{\ell}{\ell+\lambda_0} & \text{in saturation regime} \end{cases} \tag{1.28}$$

where v_T is the thermal velocity, λ_0 is the mean free path and ℓ the distance for the potential to drop by kT/q.

Despite the different approaches for dealing with the transport under a high longitudinal field, it is commonly accepted that mobility still plays a significant role on the transport [Ant06; Kha13; Sai09]. Especially, the velocity is correlated to the effective mass and so is the mobility. The mobility remains a good indicator of the intrinsic performance of the MOSFET.

1 The model of Khakifirooz et al. [Kha09] has been used in section 4.3.2 to compare MOSFETs of two different integration schemes.

1.2 CMOS technology scaling: the king is dead, long live the king !

The well-known "scaling" has been the driving force for improving the Power/Performance/Area and most of all Cost metrics discussed in the previous section. Nevertheless, the task has become more and more challenging over the years. This section gives a brief historic review of the CMOS technology scaling and presents the main limitations.

1.2.1 The happy scaling, the good old days

When discussing about CMOS scaling, Moore's law is inevitable [Moo65]. Moore observed that there is an optimum number of components for achieving the lowest cost per component (Figure 1.15). This optimum results from the positive impact of miniaturization and the negative impact of yield degradation when the circuit becomes too complex. From this observation, **Moore predicted that the number of transistors on a chip would double every two years.** At the time, Moore's projection was based on the data from 1959 to 1965 and was projected until 1975 (Figure 1.15). It has been proven accurate for several decades. Reducing the size of transistors and therefore the size of a chip for a given functionality results in a cost reduction. This has been the driving force of the CMOS technology scaling. Manufacturers adopted Moore's law as a roadmap for setting the next generation targets.

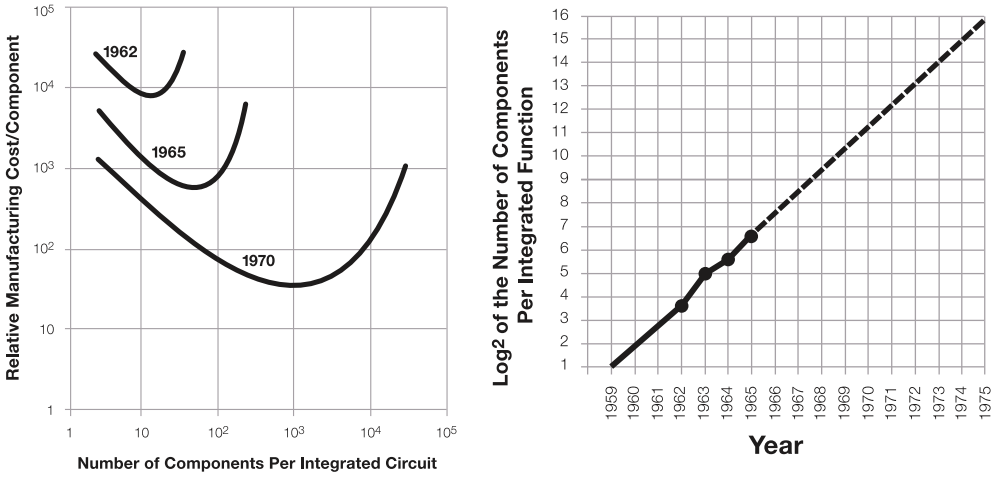


Figure 1.15: (left) Optimum number of components for achieving the lowest cost per component. (right) Moore's projection about the exponential growth of the number of transistors per integrated circuit over the years [Moo65]. Figures from [Moo06].

By cramming more components on a die, the functionality of the circuit is increased. The improvement in terms of performance was later discussed by Dennard et al. [Den74]. **Scaling the transistor dimensions** (gate length, width and oxide thickness) **by a constant factor κ provides a delay improvement at a constant power density** (Figure 1.16). Transistors enjoyed Dennard's scaling until the 130nm node. This period is today referred as the "happy scaling" since cost, functionality and performance benefit from dimension reduction without any trade-off.

SCALING RESULTS FOR CIRCUIT PERFORMANCE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_a	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time/circuit VC/I	$1/\kappa$
Power dissipation/circuit VI	$1/\kappa^2$
Power density VI/A	1

Figure 1.16: Dennard's scaling: Reducing the transistor dimensions (gate length, width and oxide thickness) by a constant factor κ provides a delay improvement at a constant power density. Scaling according to Moore's and Dennard's laws is refered as the "happy scaling" since cost, functionality and performance benefit from dimension reduction. Figure from [Den74].

1.2.2 The introduction of goodies

For sub-100nm nodes, the performance gain from Dennard's happy scaling reached a limit. Dennard's assumptions were no longer valid and parasitic effects from dimension reduction appeared.

Especially, the threshold voltage must be reduced by a factor κ without degrading the leakage. This imposes an improvement on the subthreshold swing, yet limited to 60mV/decade. Since the threshold voltage can not follow the supply voltage scaling, the gate overdrive (V_{DD}-V_T) decreases for a constant static consumption. In order to compensate for the drive loss while supply voltage is scaled, additional knobs to boost the performance are used. Intel introduced mechanical stress in their 90nm technology [Gha03; Tho04] (Figure 1.17). Stress is an efficient way to boost the carrier mobility, as discussed in section 1.3.2. This enables a performance improvement without degrading the leakage.

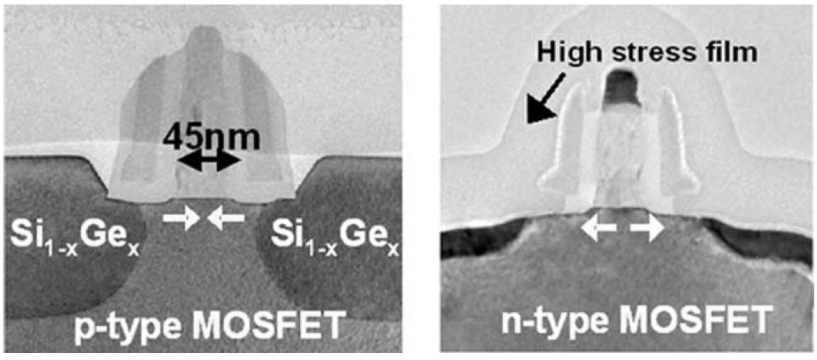


Figure 1.17: First stress introduction in Intel's 90nm technology [Gha03][Tho04]. Both pMOS and nMOS benefit from local stress introduction. Compressive stress from SiGe source/drain is used for the pMOS and tensile stress from a stressed SiN film is used for nMOS. Figure from [Tho04].

Then, the reduction of the gate oxide thickness needed for current improvement (and short channel effect control) comes along with increased gate leakage from tunneling currents. The introduction of a "high-κ" (or high-k) dielectric allowed to increase to gate oxide capacitance C_{ox} without reducing the oxide physical thickness t_{ox} by taking advantage of a higher dielectric constant κ than conventional SiO_2 ($\kappa_{SiO_2} = 3.9$). The Equivalent Oxide Thickness (EOT) is defined as the thickness of SiO_2 giving the same capacitance as the one of a "high-κ" dielectric of thickness $t_{\text{high}-\kappa}$:

$$EOT = t_{\text{high}-\kappa}\frac{\kappa_{SiO_2}}{\kappa_{\text{high}-\kappa}} \tag{1.29}$$

Hafnium-based dielectrics have been introduced at the 45nm node, along with metal gate, as shown

in Figure 1.18 [Mis07].

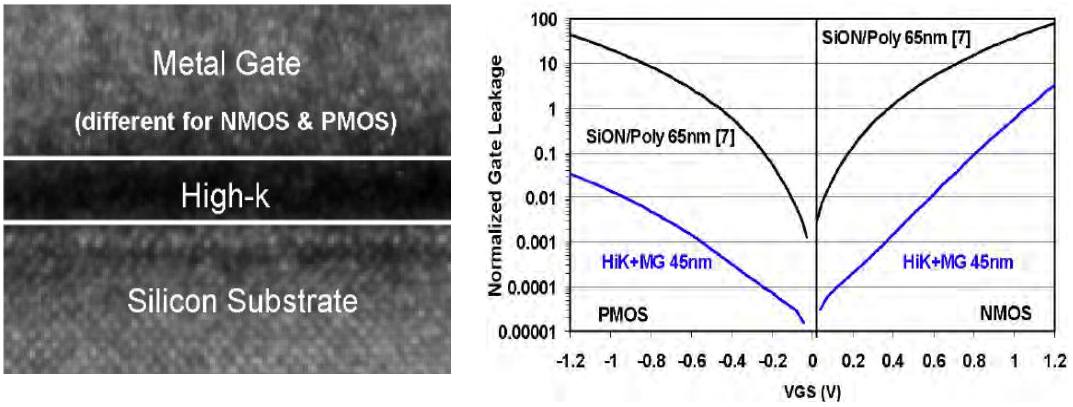


Figure 1.18: High-κ introduction at the 45nm node, from [Mis07]. (left) Gate stack with high-κ dielectric and metal gate. (right) Gate leakage reduction with high-κ introduction because of a thicker oxide at a constant capacitance.

1.2.3 The rise of new architectures

As discussed in section 1.1.3.e, the electrostatic control of the channel by the gate is degraded for short channels. This is due to a parasitic coupling from drain to source. As previously discussed, the DIBL impacts the performance. It is therefore mandatory to maintain a good electrostatic control in order to achieve high performance at a given leakage. New architectures have been developed, relying on multi-gate transistors [Fer11]. These architectures have replaced the historical bulk planar transistors for sub-30nm technologies.

1.2.3.a The FinFET

The FinFET consists in a 3D transistor where the gate wraps a channel fin, as illustrated in Figure 1.19. The first report of a FinFET device was made by Hisamoto et al. [His98] (called "folded-channel" transistor). It was first manufactured by Intel at the 22nm node [Aut12; Jan12] and became mainstream for the next nodes (TSMC's 16nm [Wu13], Intel's 14nm [Jan15; Nat14], GlobalFoundries' 14nm, Samsung's 14nm [Son14] and 10nm [Cho16; Seo14]).

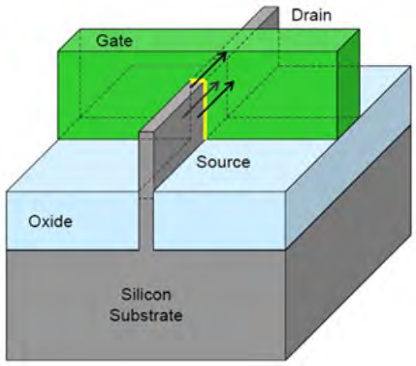


Figure 1.19: FinFET schematic. The FinFET is a 3D transistor where the gate is wrapped around the fin-shaped channel. A FinFET is also referred as a tri-gate transistor. Figure from Intel.

The FinFET features a thin channel, which is fully depleted. It can be seen as a double-gate device or tri-gate if the top width is taken into account. The FinFET architecture provides a good electrostatic control and therefore makes it more immune to short channel effects.

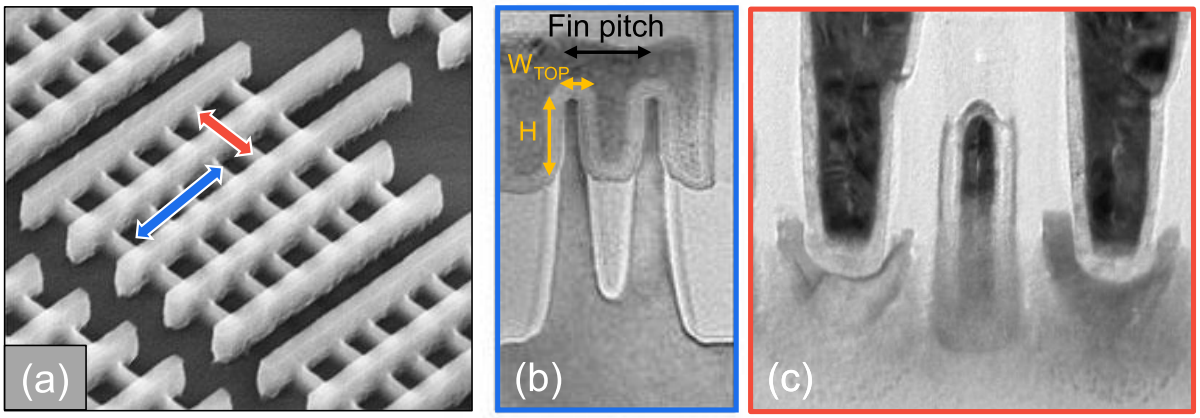


Figure 1.20: (a) FinFET SEM tilted top view, emphasizing the 3D architecture, from [Aut12]. (b) Cross-section in the gate of FinFET from 14nm node [Nat14], showing the FinFET height, top width and footprint. (c) Cross-section along the source/drain direction, from [Aut12].

In addition, an other strength of the FinFET relies on the effective width of the transistor, defined by:

$$W_{EFF} = W_{TOP} + 2 \cdot H \tag{1.30}$$

where W_{TOP} is the top width and H the height of the fin (see Figure 1.20). The 3D channel yields increased transistor width at a given footprint, especially for aggressive fin pitches. This results in high drive current, which is required for high performance, and also a reduced variability. Nevertheless, achieving high density is challenging and costly since it requires multiple patterning. The fins are indeed fabricated by Sidewall Image Transfer (SIT), also called spacer patterning or Self Aligned Double Patterning (SADP).

FinFET is today still seen as a viable option for sub-10nm nodes (TSMC's 7nm [Wu16], IBM's 7nm technology [Xie16]).

1.2.3.b The FDSOI technology

The Fully Depleted Silicon On Insulator (FDSOI) technology refers to the use of a SOI substrate instead of a bulk Silicon substrate. The SOI substrate is fabricated by the Smart Cut technique which relies on direct bonding [Bru95]. If the Silicon film is thin enough, it is fully depleted[1]. In this case, the depletion thickness and the junction depth are equivalent to the film thickness. This results in an enhanced electrostatic control with respect to planar bulk technologies.

Nevertheless, a coupling between the drain and the channel occurs through the buried oxide (BOX) [Ern07]. The thinnest the BOX thickness and the highest the Ground Plane (GP) doping, the more this effect is mitigated [Gal06]. The electrostatic control is maximized for thin Silicon film and BOX, hence the Ultra-Thin Body and Buried oxide Fully-Depleted Silicon On Insulator technology (UTBB-FDSOI).

1 In contrast to the Partially Depleted SOI (PDSOI) in which the film is thicker than the depletion region.

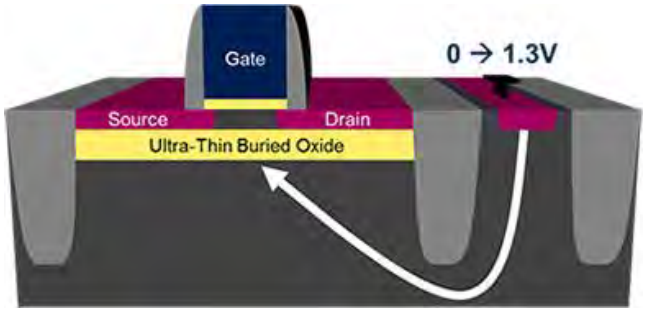


Figure 1.21: FDSOI transistor schematic, from STMicroelectronics. The transistor is built on a Silicon On Insulator (SOI) substrate. The thin Silicon film and buried oxide (BOX) allow a good electrostatic control. The channel-body coupling due the BOX enables a high back-bias efficiency.

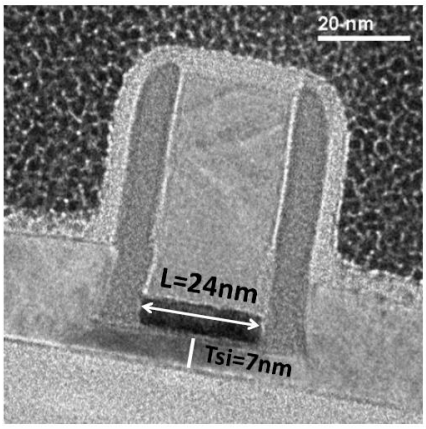


Figure 1.22: Cross-section of a FDSOI transistor from 28nm technology. The film thickness t_{Si} is 7nm. Figure from [Pla12].

Figures 1.21 and 1.22 present a transistor from UTBB-FDSOI technology. The UTBB-FDSOI technology has been developed at the 28nm node [Pla12] and 14nm node [Web14; Web15] by STMicroelectronics/LETI and at the 22nm node by GlobalFoundries/LETI [Car16]. More details about 28nm and 14nm FDSOI technologies are given in section 3.1, with a specific focus on 14nm, which is at the heart of this thesis work.

For thin film devices as in FDSOI, the threshold voltage criterion $\psi_s > 2 \cdot \phi_f$ (see section 1.1.3.b) is not relevant as the depletion charge is limited by the film thickness. This criterion has been changed to $C_{inv} = C_{ox}$, i.e. the capacitance of inversion equals the one of the gate oxide [Poi05]. This leads to the expression of the threshold voltage [Poi05]:

$$V_T = V_{FB} + \frac{kT}{q} \ln\left(\frac{2 \cdot C_{ox} \cdot kT}{q^2 \cdot n_i \cdot t_{Si}}\right) + \frac{\hbar^2 \cdot \pi^2}{2 \cdot q \cdot m^* \cdot {t_{Si}}^2} \tag{1.31}$$

where t_{Si} is the SOI thickness and m^* the effective mass of confinement. The last term translates the effect of the confinement induced by the quantum well formed by the thin silicon layer between the two dielectrics.

In FDSOI, there is a strong coupling between the channel and the body, thanks to the buried oxide. The threshold voltage is therefore highly sensitive to the back-bias and Ground Plane GP doping [And10; Fen09; Web10]. The body factor γ is defined by the threshold voltage variation with respect to the voltage applied on the body (i.e. the back-bias). Assuming an inversion at the gate oxide/channel interface, neglecting the depletion in the ground plane and considering a capacitance divider, the back-bias efficiency on long channels can be expressed as [Lim83; Noe11]:

$$\gamma = \frac{\Delta V_T}{V_B} = \frac{C_{BOX} \cdot C_{Si}}{C_{OX}(C_{BOX} + C_{Si})} \tag{1.32}$$

The lower the BOX thickness, the higher the body factor. A typical value of γ =80mV/V is obtained

with a 20nm BOX and a front oxide thickness of ≈0.8-0.9nm. Thanks to the high back-bias efficiency, a large range of performance/leakage can be obtained on a FDSOI device. This is illustrated in Figure 1.23 and discussed in sections 3.1 and 4.3.2.e [1].

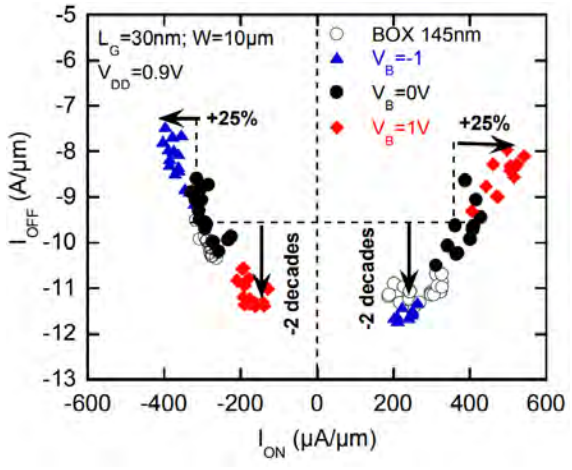


Figure 1.23: Impact of back-bias on FDSOI I_{ON}/I_{OFF} trade-off, from [And10]. The BOX thickness is 10nm. A positive (negative) back-bias on nMOS (pMOS, respectively) shifts the V_T toward low value, resulting in an increased ON current at the expense of high leakage. This is called Forward Back-Bias (FBB). It is the opposite for Reverse Back-Bias (RBB).

The back-bias can be used in two regimes:

- **"Reverse Back-Bias" (RBB)**. A negative (positive) voltage is applied on the nMOS (pMOS) body, respectively. This leads to a threshold voltage shift towards higher value [2] and in turn to **low leakage, at the cost of low performance**.
- **'Forward Back-Bias" (FBB)**. A positive (negative) voltage is applied on the nMOS (pMOS) body, respectively. This leads to a threshold voltage shift towards lower value and in turn to **high performance, at the expense of high leakage**.

An other interesting feature of the back-bias is the process variation compensation. The performance/leakage distribution due to process variation can be narrowed by applying a FBB on slow dies, for instance.

In a conventional architecture, the nMOS and pMOS ground planes form a diode (PN junction). The so-called Regular-well architecture consists in a P-type ground plane for nMOS and an N-type ground plane for pMOS. In order not to avoid a dramatic leakage from the diode biased in direct, the Regular-well architecture allows Reverse-Back-Bias, i.e. $V_{B,N}<V_{B,P}$. It is the opposite for the so-called Flip-well architecture (N-type ground plane for nMOS and P-type for pMOS) which allows Forward Back-Bias. In order to take full advantage of the back-bias bidirectional capability on the same device, a dual isolation scheme is required [Gre12], as discussed more widely in section 4.3.2.e.

1.2.3.c Stacked nanosheets

In the pursuit of electrostatic control, the gate-all-around (GAA) transistors, or nanowires, are the most relevant architectures. However, nanowires suffer from a low drive current due to their small

1 Back-bias is also discussed in section 5.4 in a dynamic approach, enabled by monolithic 3D integration.

2 V_T are discussed in absolute value in order to avoid any confusion about the pMOS threshold voltage shift. A low $|V_T|$ means high leakage and therefore high performance and a high $|V_T|$ means low leakage and therefore low performance.

section. In order to provide a sufficient drive current, nanowires can be vertically stacked [Bar16; Ern08; Mer16]. The higher the number of nanowires, the larger the effective width of the transistor. The drive can also be enhanced by designing nanowires with a width significantly larger than the height. These so-called nanosheets have been presented as the solution for sub-5nm nodes [Lou17]. Figure 1.24 shows a transverse cross-section of a superlattice of nanosheets.

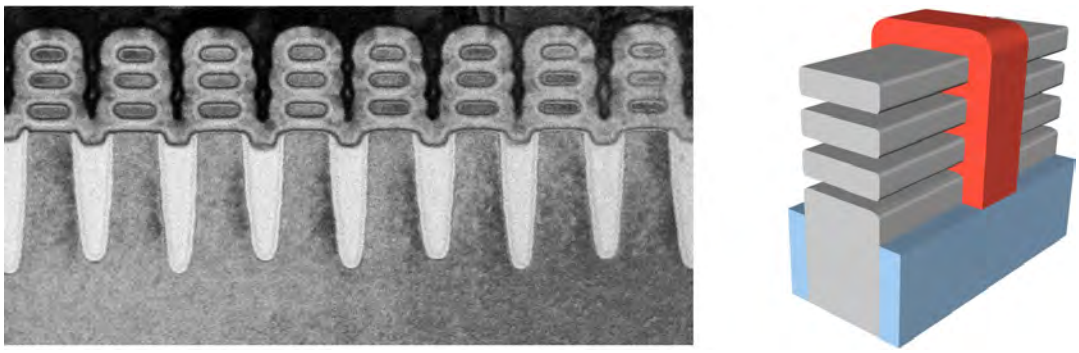


Figure 1.24: (left) Stacked nanosheets cross-section, from [Lou17] and (right) 3D view. The gate all around architecture enables a good electrostatic control. A high drive current is achieved by stacking the nanosheets and using a large width (hence the name nanosheet is preferred to nanowire).

Stacked nanosheets have the strong interest to provide a finer granularity of effective width compared to discrete FinFETs. However, their fabrication is challenging. Among the particularities inherent to stacked nanosheets, one can mention the formation of the channel stack using several epitaxy steps (Si/SiGe/Si/...), the nanosheet reveal by selective etching, the integration of inner spacers. Nonetheless, stacked nanosheets appear as the most promising solution for High Performance (HP) applications at sub-5nm nodes.

1.2.4 The parasitics, key players

As dimensions scale down, the impact of parasitics become more and more important on the final circuit performance.

At the device level, the parasitic capacitances play a major role on the total capacitance of the device C_{tot} . The main parasitic capacitances include the gate-to-source and gate-to-drain capacitances, as illustrated in Figure 1.25 [Wei11].

The performance is strongly impacted by these parasitic capacitances as they directly contribute to the effective capacitance to be loaded. One can write [Wei11]:

$$C_{eff} = C_d + FO.C_g + C_w \tag{1.33}$$

where C_d, C_g and C_w are the drain, the gate and the interconnection capacitances, respectively, and FO is the FanOut, i.e. the number of stages to be loaded. C_d is given by:

$$C_d = M \cdot C_{gd} + C_j \tag{1.34}$$

with $C_{gd} = C_{ov} + C_{of} + C_{pcca} + C_{corner}$ where C_{ov} is the overlap capacitance, C_{of} the outer fringe capacitance, C_{pcca} the gate-to-contact capacitance and C_{corner} is the 3D capacitance between the

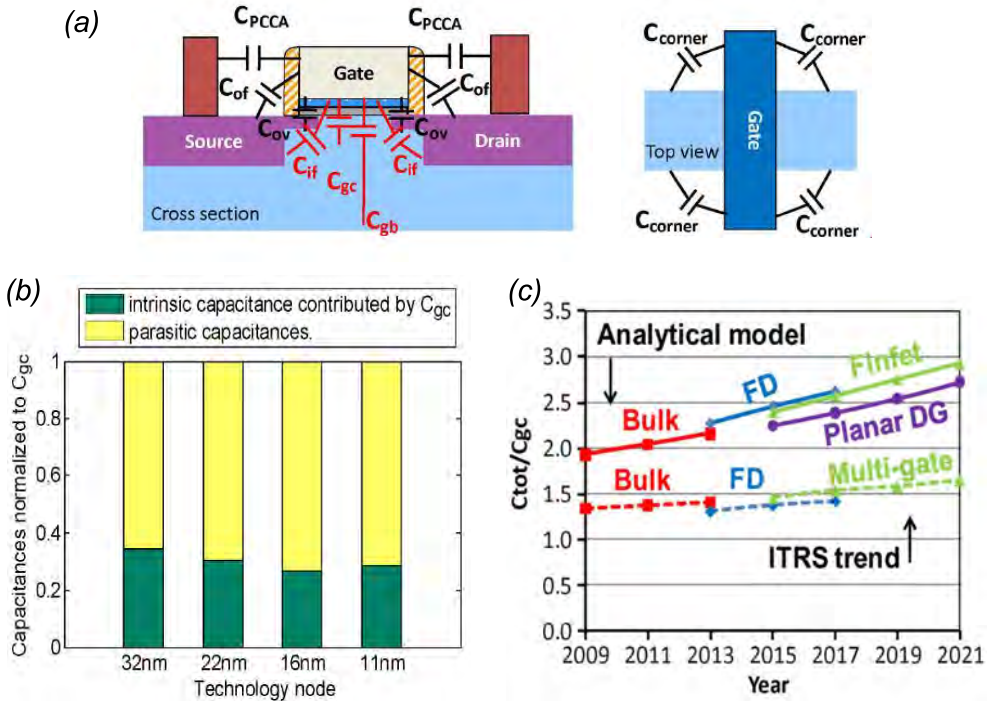


Figure 1.25: (a) Parasitic capacitances, from [Wei11]. (b) Parasitic capacitance contribution with respect to the intrinsic capacitance according to the technology node, from [Wei11]. (c) Total vs. intrinsic capacitance over the years for the different architectures, from [Lac12]. The parasitic capacitances become more and more dominant.

gate overhang and the source/drain extension regions. The M factor translates the Miller's effect. As the voltages of C_{gd} capacitance electrodes vary oppositely (input and output of the inverter), M=2 must be considered.

C_g is given by:

$$C_g = \frac{1}{4}C_{goff} + \frac{3}{4}C_{gon} \tag{1.35}$$

where

$$\begin{cases} C_{goff} = 2 \cdot C_{gd} + C_{if} + C_{gboff} \\ C_{gon} = C_{gc} + 2 \cdot C_{gd} \end{cases} \tag{1.36}$$

Because of the dimension scaling, the parasitic capacitances are expected to be at least twice larger than the intrinsic gate-to-channel capacitance C_{gc}, as shown in Figure 1.25 [Lac12; Wei11].

Still at the device level, the parasitic access resistance are detrimental for the drive current because of the induced voltage drop. The access resistance includes the contact resistance (metal to the doped source/drain), the junction itself and the near-spacer region. This is discussed more widely in section 2.2.

In addition to the parasitics at the device level, the impact of interconnections must be considered. The wire delay contribution increases as the dimensions scale down (Figure 1.26) [Huy17; Yea13].

When only considering the wire dimension reduction with scaling, the wire delay is not impacted since the increase of resistance is compensated for by the capacitance reduction, resulting in same RC delay. However, the wire resistance increases with the dimension reduction because of two reasons. First, the Copper resistivity increases due to electron scattering at the sidewall and the effect of grain boundaries (Figure 1.26). Secondly, the relative volume of Cu in the metal line decreases since the barrier can not be scaled down. As a consequence, the interconnect delay becomes more and more predominant. Alternative materials to Copper such as Cobalt have been proposed to mitigate this effect [Kel16].

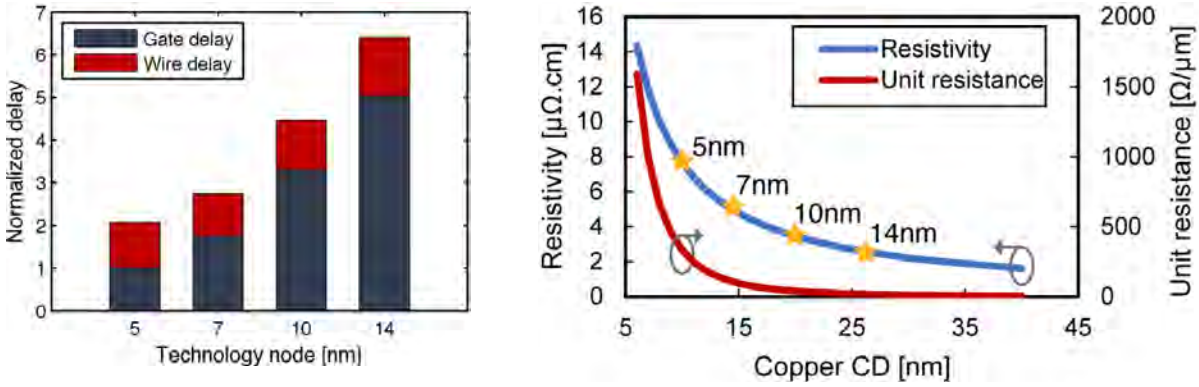


Figure 1.26: (left) Delay partitioning between gate (i.e. transistors) and wire (i.e. interconnections) according to the technology node, from [Huy17]. The interconnection delay becomes more predominant as the technology scales down. (right) Wire resistance and resistivity *vs.* critical dimension, from [Huy17]. The interconnection resistance rises dramatically when the dimensions are scaled down, especially because of the Copper resistivity increase.

1.2.5 CMOS scaling: conclusion and perspectives

The scaling has been a driving force for CMOS technology. Integrated circuits have been benefiting from transistor dimension reduction in terms of power, functionality and cost for several decades. This "happy scaling", characterized by Dennard's laws, eventually came to an end.

Even though it is accepted that Moore's law has slowed down, the CMOS technology scaling has however not stopped yet, helped by Design/Technology Co-Optimization. Different goodies have been introduced to push the limits back. New architectures have replaced the historical bulk planar devices. FinFET and FDSOI technologies have demonstrated excellent electrostatic control.

Nevertheless, the parasitics are becoming more and more predominant. The performance is limited by the parasitic capacitances and the interconnection delay. Even though the FDSOI architecture shows less parasitics, they can not be compensated for by a large effective width as in FinFET technology. This makes the wire delay even more detrimental for FDSOI. In addition, it has been shown that the mobility in thin film tends to decrease [Uch02; Uch03]. As a result, there is a need for FDSOI device intrinsic performance improvement.

The use of alternative channel materials featuring high mobility has been discussed. Especially, III-V materials or pure Ge have been considered [Hut10b; Sko10] but there are still challenges to be addressed such as the integration on Si substrate or the leakage induced by band-to-band tunneling

for instance. Strain engineering remains one of the most powerful knob to increase the performance of CMOS technology [Tak08]. It is indeed today discussed for achieving sub-10nm node requirements [Bae16]. More details about the strain integration in CMOS technology are given in the next section.

Finally, other essential factors need to be considered when developping a technology in an industrial context such as for instance the variability [Web08], the reliability [Web16] or the yield.

1.3 Strain integration in CMOS technologies

This section focuses on the strain introduction in CMOS technology. First, the strain-stress relationship is discussed through the theory of elasticity. The impact of strain on the band structure of Silicon is then detailed. In a second step, some techniques used in CMOS technologies to introduce strain are presented. Finally, a brief state of the art of the local layout effects is provided.

1.3.1 Theory of elasticity

Hooke's law describes the relationship between stress σ and strain ε:

$$\underline{\sigma} = \underline{\underline{C}} \cdot \underline{\varepsilon} \;\Leftrightarrow\; \underline{\varepsilon} = \underline{\underline{S}} \cdot \underline{\sigma} \tag{1.37}$$

where $\underline{\underline{C}}$ and $\underline{\underline{S}}$ are the fourth rank tensors of stiffness and compliance, respectively. Taking into account strain and stress symmetry properties, Hooke's law can be written as:

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} \tag{1.38}$$

According to Voigt's notation (i.e. $xx \rightarrow 1$; $yy \rightarrow 2$; $zz \rightarrow 3$; $yz \rightarrow 4$; $xz \rightarrow 5$ and $xy \rightarrow 6$), Hooke's law can be expressed in a matrix form:

$$\begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} & C_{14} & C_{15} & C_{16} \\ C_{21} & C_{22} & C_{23} & C_{24} & C_{25} & C_{26} \\ C_{31} & C_{32} & C_{33} & C_{34} & C_{35} & C_{36} \\ C_{41} & C_{42} & C_{43} & C_{44} & C_{45} & C_{46} \\ C_{51} & C_{52} & C_{53} & C_{54} & C_{55} & C_{56} \\ C_{61} & C_{62} & C_{63} & C_{64} & C_{65} & C_{66} \end{pmatrix} \cdot \begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{pmatrix} \tag{1.39}$$

where C_{ij} are the elastic constants.

For an isotropic material, Hooke's law can be written as:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{pmatrix} = \frac{1}{E} \begin{pmatrix} 1 & -\nu & -\nu & 0 & 0 & 0 \\ -\nu & 1 & -\nu & 0 & 0 & 0 \\ -\nu & -\nu & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2+2\nu & 0 & 0 \\ 0 & 0 & 0 & 0 & 2+2\nu & 0 \\ 0 & 0 & 0 & 0 & 0 & 2+2\nu \end{pmatrix} \cdot \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{pmatrix} \tag{1.40}$$

where E and ν are the Young's Modulus and Poisson's ratio, respectively.

As far as Silicon is concerned, it is not an isotropic material and can therefore not be described by unique values of Young's Modulus and Poisson's ratio [Hop10]. Considering the symmetry of the cubic diamond lattice of Silicon (see Figure 1.27), its stiffness matrix in the reference coordinates (i.e.

X, Y, Z directions along <100>, <010>, <001>, respectively) is given by:

$$C^{<100>} = \begin{pmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{pmatrix} \tag{1.41}$$

The Silicon elastic constants C_{11}, C_{12} and C_{44} values are given in Table 1.1.

Table 1.1: Elastic constants (in GPa) of Silicon and Germanium [Mas56; Wor65].

Material	C_{11}	C_{12}	C_{44}
Silicon	165.7	63.9	79.6
Germanium	129.2	47.9	67.0

In order to derive the stiffness matrix in the <110> orientation (i.e. X and Y along <110> and Z along <001>), a rotation of θ=45° is performed. The matrix of transformation R is given by:

$$R = \begin{pmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{pmatrix} = \begin{pmatrix} \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & 0 \\ -\frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{1.42}$$

The stiffness in the new orientation $C^{'}$ is derived according to:

$$C'_{ijkl} = R_{ig}R_{jh}C_{ghmn}R_{km}R_{ln} \tag{1.43}$$

In the <110> orientation, the stiffness matrix is given by:

$$C^{<110>} = \begin{pmatrix} C'_{11} & C'_{12} & C'_{13} & 0 & 0 & 0 \\ C'_{12} & C'_{11} & C'_{13} & 0 & 0 & 0 \\ C'_{13} & C'_{13} & C'_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C'_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C'_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C'_{66} \end{pmatrix} \tag{1.44}$$

where:

$$\begin{cases} C'_{11} = \dfrac{C_{11} + C_{12} + 2C_{44}}{2} \ ; \ C'_{12} = \dfrac{C_{11} + C_{12} - 2C_{44}}{2} \ ; \ C'_{13} = C_{12} \\ C'_{33} = C_{11} \ ; \ C'_{44} = C_{44} \ ; \ C'_{66} = \dfrac{C_{11} - C_{12}}{2} \end{cases} \tag{1.45}$$

Figure 1.28 shows the equivalent Young's Modulus and Poisson's ratio of Silicon according to the

orientation, for a (001) plane. The Young's modulus has been derived according to:

$$E = \frac{1}{S_{11}} = \frac{1}{{C^{-1}}_{11}} \text{ which is equivalent to } E = \frac{1}{S_{22}} = \frac{1}{{C^{-1}}_{22}} \tag{1.46}$$

and the Poisson's ratio:

$$\nu = -S_{12} \cdot E \tag{1.47}$$

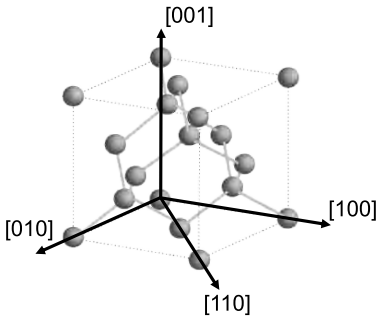


Figure 1.27: Lattice of Silicon. Silicon has a diamond cubic lattice structure.

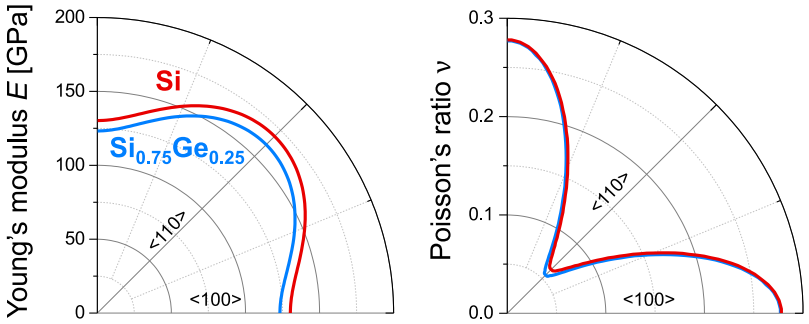


Figure 1.28: Equivalent (left) Young's Modulus and (right) Poisson's ratio of Silicon and SiGe with 25% of Germanium according to the crystal orientation. The plane is (001) oriented.

1.3.2 The impact of strain on Silicon properties

1.3.2.a Band structure of Silicon

The band structure of a solid describes the range of allowed energies for an electron. In the Silicon conduction band, the relation of dispersion $E(k)$, where k is the wave vector of the electron, can be written for the Δvalley i as:

$$EC_i(k) = \frac{\hbar^2}{2m_l}(k_i - k_0)^2 + \frac{\hbar^2}{2m_t}\left({k_j}^2 + {k_k}^2\right) \tag{1.48}$$

where i, j, k correspond to the x, y, z orientations and m_l ($\approx 0.92m_0$) and m_t ($\approx 0.19m_0$) are the longitudinal and transverse effective masses (see 1.1.3.g). According to equation 1.48, the shape of the energy iso-surfaces is ellipsoidal, as shown in Figure 1.29. The minimum of energy is given by the center of the ellipsoid, at the position k=k_0 along the Δ-direction (i.e. <100> orientation). The six equivalent valleys are called Δ-valleys. One differ the out-of-plane valleys oriented along the direction of confinement, so-called Δ_2, from the in-plane ones, so-called Δ_4.

The valence band of Silicon is more complex. By considering the coupling between the first two subbands at the top of the valence band (Γ point), Bir and Pikus derived the expression of the valence band [Bir74]:

$$EV_{1,2}(k,\varepsilon) = Ak^2 \pm \sqrt{E_k} \qquad E_k = B^2k^4 + C^2(k_x^2k_y^2 + k_x^2k_z^2 + k_y^2k_z^2) \tag{1.49}$$

where A, B and C parameter values in units of $\frac{\hbar^2}{2m_0}$ are A=-4.27 , B=-0.63 and C=4.93 [Hen63].

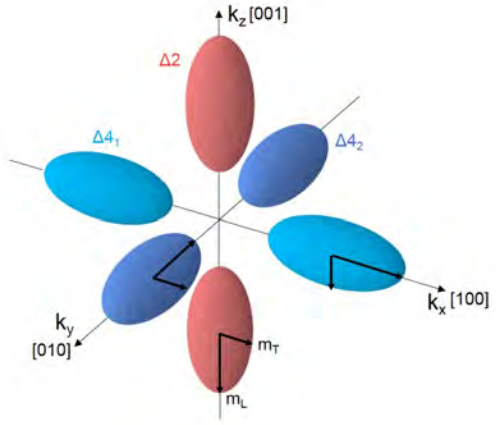


Figure 1.29: Iso-energy ellipsoids of the conduction band (Δ valleys). The Δ_2 valleys correspond to the out-of-plane direction (i.e. the orientation of confinement) and Δ_4 valleys correspond to the in-plane valleys. The transverse and longitudinal effective masses are represented.

Figure 1.30 shows the energy iso-surfaces of the two subbands, derived from equation 1.49. The curvatures of these subbands are strongly anisotropic. The two subbands are called "Heavy Holes" (HH) and "Light Holes" (LH), according to their curvature. The effective mass is indeed inversely proportional to the E(k) curvature:

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{\delta^2 E}{\delta k^2} \tag{1.50}$$

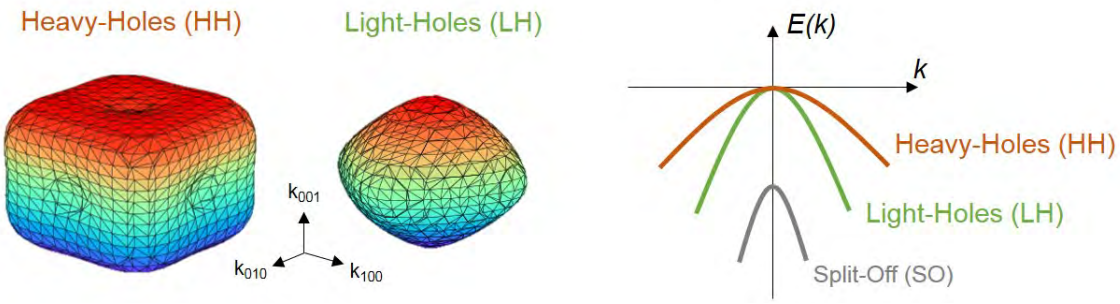


Figure 1.30: (left) Iso-energy surfaces of the two valence subbands at the Γ point, called "Heavy Holes" (HH) and "Light Holes", derived from equation 1.49. (right) Schematic of the relation of dispersion in the valence band. The effective mass is inversely proportional to the curvature, hence the "Heavy Holes" and "Light Holes" subband names.

1.3.2.b Deformation potential theory

By modifying the crystal structure, strain alters the band structure. To account for the band structure modification with strain, the theory of deformation potential was introduced [Bar50; Her57; Sho50]. According to this theory, the energy of the conduction band valleys is given by $EC_i(k,\varepsilon) = EC_i(k) + \Delta EC_i(k,\varepsilon)$ where:

$$\Delta EC_i(k,\varepsilon) = \Xi_d\left(\varepsilon_{ii} + \varepsilon_{jj} + \varepsilon_{kk}\right) + \Xi_u\varepsilon_{ii} + \Xi_m\hbar^2 k_j k_k \varepsilon_{jk} \tag{1.51}$$

where i, j, k are x, y, z directions, EC_x and EC_y correspond to Δ_4 subbands and EC_z to Δ_2, and Ξ_d, Ξ_u and Ξ_m are the deformation potentials. Ξ_d translates the band shift induced by the hydrostatic strain component, that is to say the change of volume. Ξ_u is related to the uniaxial strain component

along one axis and is responsible for the subband splitting because crystal symmetry is broken. Ξ_m is the shear component. For instance, the shear component is present for a uniaxial stress in the <110>-orientation [1].

For the valence band, the impact of strain on the relation of dispersion is expressed according to the analytical model of Bir and Pikus [Bir74]:

$$EV_{1,2}(k,\varepsilon) = Ak^2 + a_v\varepsilon_{hydr} \pm \sqrt{E_k + E_{k\varepsilon} + E_\varepsilon} \tag{1.53}$$

with

$$\begin{cases} E_k = B^2k^4 + C^2(k_x^2k_y^2 + k_x^2k_z^2 + k_y^2k_z^2) \\ E_\varepsilon = \frac{b^2}{2}\left[(\varepsilon_{xx} - \varepsilon_{yy})^2 + (\varepsilon_{yy} - \varepsilon_{zz})^2 + (\varepsilon_{zz} - \varepsilon_{xx})^2\right] + d^2\left(\varepsilon_{xy}^2 + \varepsilon_{xz}^2 + \varepsilon_{yz}^2\right) \\ E_{k\varepsilon} = Bb\left[3\left(k_x^2\varepsilon_{xx} + k_y^2\varepsilon_{yy} + k_z^2\varepsilon_{zz}\right) - k^2\varepsilon_{hydr}\right] + 2Dd\left(k_xk_y\varepsilon_{xy} + k_xk_z\varepsilon_{xz} + k_yk_z\varepsilon_{yz}\right) \end{cases} \tag{1.54}$$

where $D = -\sqrt{C^2 + 3B^2}$ and a_v, b and d are the valence band deformation potentials.

The table 1.2 summaries the different values of deformation potentials for both the conduction and valence bands.

Table 1.2: Deformation potentials [eV].

Ξ_u	Ξ_d	Ξ_m	a_v	b	d
9.16[a]; 8.5[b]; 10.5[c]	1.13[a]; -5.2[b]; 1.1[c]	86.8[d]	2.46[a]	-2.35[a]	-5.32[a]

[a] Data from [Van86];
[b] Data from [Kan91];
[c] Data from [Fis96];
[d] Data from [Hen63]

Figure 1.31 shows the energy iso-surface of the HH and LH subbands derived from equations 1.53 and 1.54 for three different stress configurations: unstressed, biaxial compressive stress, and uniaxial compressive stress along the [110] direction. This figure shows how strain modifies the valence band structure of the Silicon. In particular, the shear component of the [110] uniaxial stress yields a strong anisotropy [Iri04; Uch05].

Even though the analytical expressions of Bir et al. [Bir74] for the valence band allow to simply account for the impact of strain, the validity of such a model is strongly limited. In order to take into account the strong interaction between the subbands (especially the split-off orbit), other techniques

1 Expression of the stress in the <100> coordinates according to a uniaxial stress in <110> coordinates σ_0 using the transformation matrix R of equation 1.42:

$$\sigma^{<100>} = R\sigma^{<110>}R^T = R \cdot \begin{pmatrix} \sigma_0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \cdot R^T = \begin{pmatrix} \frac{\sigma_0}{2} & -\frac{\sigma_0}{2} & 0 \\ -\frac{\sigma_0}{2} & \frac{\sigma_0}{2} & 0 \\ 0 & 0 & 0 \end{pmatrix} \Rightarrow \varepsilon_{xy} \neq 0 \tag{1.52}$$

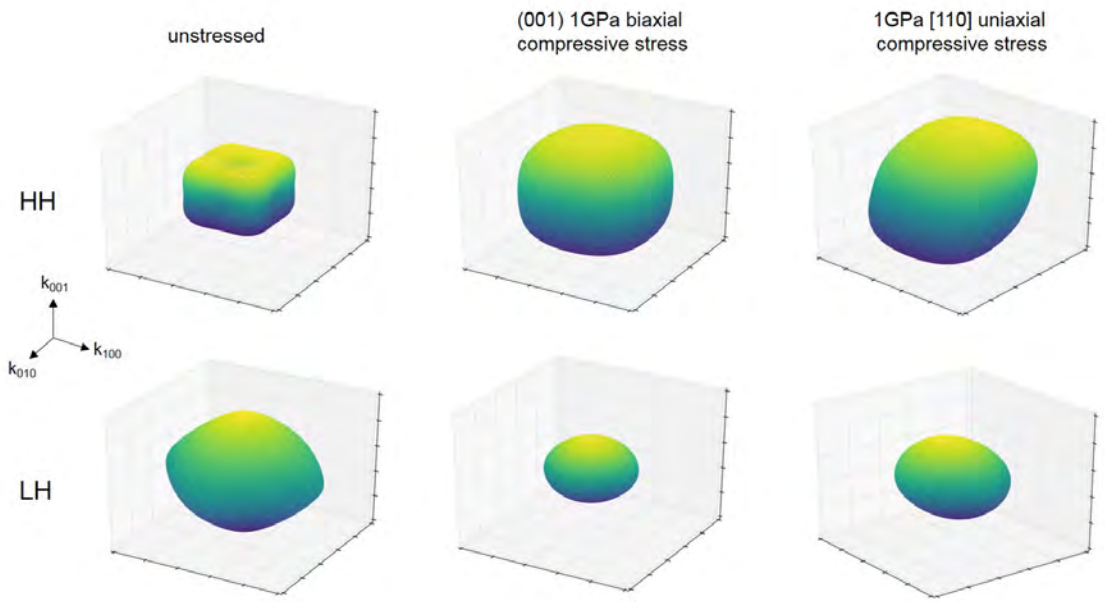


Figure 1.31: Energy iso-surfaces of (top) HH and (bottom) LH under different stress configuration: (left) unstressed, (middle) (001) biaxial compressive stress, (right) [110] uniaxial compressive stress.

such as the "**k·p** method" must be used. This method consists in solving Schrödinger's equation using Taylor expansions [Ric04]. Figure 1.32 illustrates the relation of dispersion E(k) for the valence band, obtained from **k·p** method [Lee05; Nay94; Sun07]. This figure highlights the impact of strain on the band structure. The bands are shifted and the degeneracies are lifted if the strain is not purely hydrostatic. In addition, band warping can occur, strongly altering the effective mass. As can be seen on Figure 1.32, the HH subband is subjected to strong band warping under <110> uniaxial compressive stress. It results in an even lower effective mass than the LH subband. The naming of these subbands loses its meaning in that case.

Figure 1.33 well summarizes the impact of strain on the band diagram, focusing on the band shift and split. The hydrostatic strain component modifies the band gap without splitting the subbands since the crystal symmetry is not broken. The degeneracies are lifted by a uniaxial strain component.

The carrier mobility is directly impacted by the band structure modification [Uch05]. The mobility is indeed straightforwardly linked to the effective mass by $\mu = \frac{q \cdot \tau}{m^*}$. The band split leads to repopulation from a subband to an other. For instance, the splitting of the Δ_2 and Δ_4 valleys with (001) biaxial tensile stress results in a preferential population of electrons in the Δ_2 valley. Yet the latter valley features a lower effective mass in the direction of transport (m_t). As a consequence, a biaxial tensile stress enhances the electron mobility. In addition to the repopulation effect, the intervalley scattering rate is impacted by band splits. This also plays a significant role on the mobility, changing the average time between two scattering events τ. Finally, the band warping, especially in the valence band, changes the effective mass and thus the mobility.

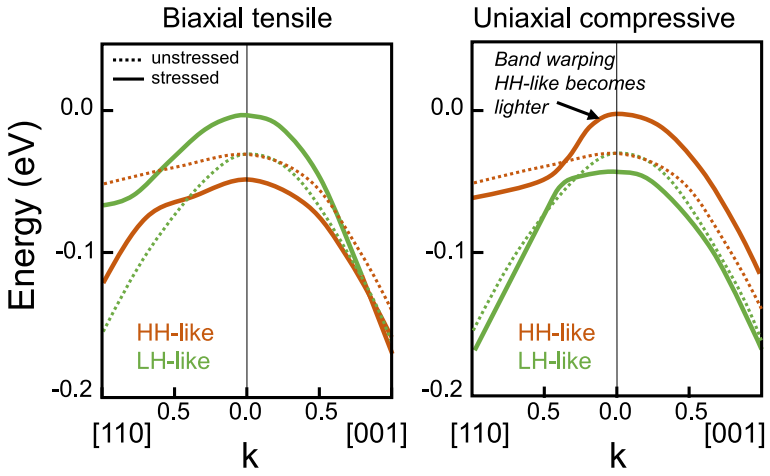


Figure 1.32: Relation of dispersion E(k) for the valence band in case of (left) biaxial tensile stress and (right) <110> uniaxial compressive stress, compared with the unstressed reference (dotted lines), adpated from [Lee05; Nay94; Sun07]. The strain leads to band shifting, degeneracy lifting and also band warping.

1.3.2.c Interaction with confinement

The impact of strain on the material properties have only been discussed for bulk Silicon so far. However, the transport in a driving MOSFET is governed by the carriers confined in the inversion layer. In inversion, the band curvature results in a potential barrier, usually assumed to be triangular, as illustrated in Figure 1.34. The motion of carriers is restricted in the gate direction, i.e. the out-of-plane direction z. The confinement in the out-of-plane direction results in band shifts and/or splits. The different available energy states can be derived by solving simultaneously Schrödinger's and Poisson's equations. Under electric confinement in the (001) plane, the Δ_2 valleys are preferentially populated with respect to Δ_4 ones (because of different effective masses in the direction of confinement

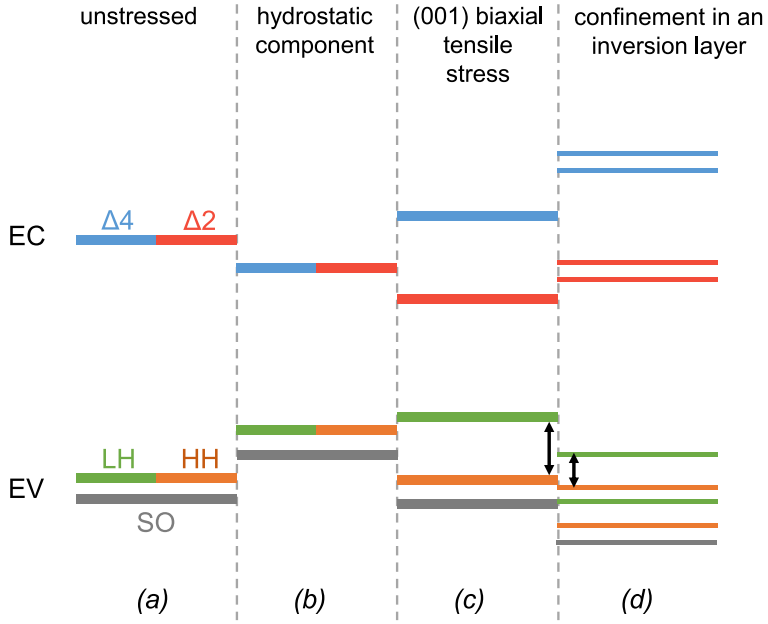


Figure 1.33: Diagrams of band splitting. (a) unstrained Silicon. (b) impact of a hydrostatic strain (i.e. change of volume), altering the band gap but no degeneracies are lifted. (c) impact of biaxial tensile stress, lifting the degeneracies (Δ_2 and LH subbands are more favorable). (d) impact of confinement (i.e. in an inversion layer).

m_l and m_t, respectively), as illustrated in Figure 1.33. As far as the valence band is concerned, the confinement-induced subband split results in a more populated HH subband (Figures 1.33 and 1.35).

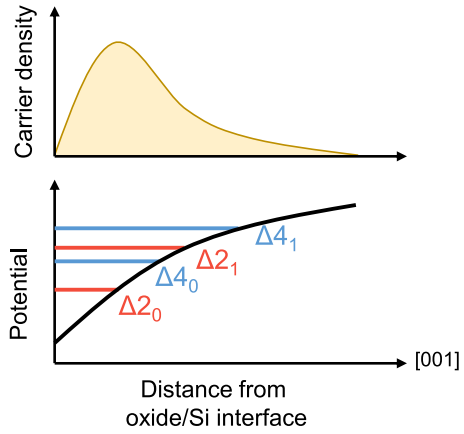


Figure 1.34: Schematic (top) carrier density and (bottom) band diagram in a MOSFET in inversion with respect to the distance from the oxide/Silicon interface. The electric confinement in the out-of-plane direction results in band splitting. Δ_2-valleys are preferentially populated in the conduction band (and HH in the valence band).

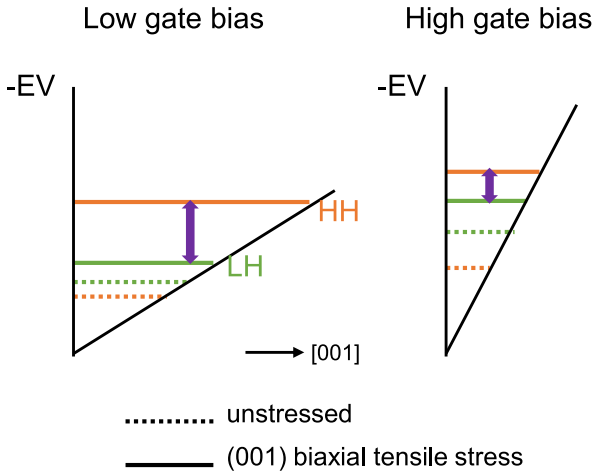


Figure 1.35: Schematic of the valence band diagram under (left) low and (right) strong electric confinement (i.e. inversion) for unstressed and biaxial tensile stressed Silicon. The strain-induced HH and LH subband splitting is canceled out by the one induced by the electric confinement.

The subband splitting induced by the quantum confinement can be additive or subtractive to the strain-induced subband splitting. For instance, a biaxial tensile strain splits the Δvalleys in the same trend as the confinement. In this case, it is beneficial for electron mobility. On the other hand, the LH and HH subband split induced by confinement reduces the one induced by strain, as illustrated in Figure 1.35.

1.3.2.d Summary

To sum up, the strain engineering consists in altering the band structure of the material by changing its crystal structure. Three mechanisms occur with strain:

- **Band shift**: the change of volume of the lattice, i.e. the hydrostatic strain component, results in band shifts.
- **Band split**: if strain breaks the crystal symmetry, which is the case for a uniaxial stress, band split occurs. In the conduction band, the sixfold Δ-valleys degeneracy is lifted and so for the HH and LH in the valence band. This results in carrier repopulation from a subband to an other, featuring a different effective mass. The intervalley scattering is also reduced by the subband splitting.
- **Band warping**: the band curvature is modified by the strain. This is particularly true for the valence band. The effective mass (inversely proportional to the band curvature) is therefore modified.

All these effects directly impact the carrier mobility in the MOSFET channel. The interaction with

electric confinement must be considered: the strain and electric confinement band splitting can be additive or cancel each other according to the stress configuration.

1.3.3 Strain integration techniques

In this section, the main strain integration techniques used in CMOS technology are presented. These techniques can be sorted in two categories:

- The "locally-introduced strain" techniques, in which the MOSFET channel is strained by the means of an external element.
- The "globally-introduced strain" techniques, in which the MOSFET channel material is intrinsically strained.

1.3.3.a Locally-introduced strain techniques

The first CMOS technology to embed strain used local stressors [Gha03; Tho04]. In particular, nMOSFETs where stressed by the means of a stressed nitride film deposited prior to the contact realization. This nitride film original purpose is to act as a stop layer for the contact etching, hence its name **Contact Etch Stop Layer (CESL)**. The CESL can show an intrinsic stress from the process of deposition. This stress is transferred into the MOSFET channel because of the gate topology. The use of CESL to locally introduce stress was described by Ito et al. [Ito00]. Because nMOS and pMOS do not require the same stress type, the use of dual CESL has been discussed [Shi01]. The stress generated by CESL strongly depends on the device geometry. It is highly dependent on the transistor gate length [Mor12] and the contacted poly pitch [Ene07; Xu12]. The shorter the CPP, the lower the stress generated into the channel, because of the nitride film shape between two gates. As a result, the use of CESL in scaled technologies to locally stress the devices becomes inefficient (see Figure 1.36).

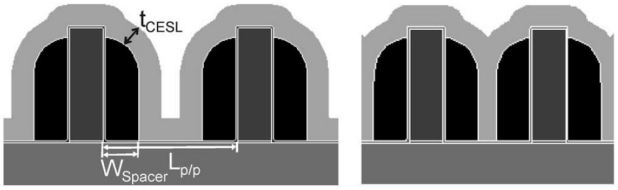


Figure 1.36: Schematic of the impact of contacted poly pitch reduction on the CESL morphology, from [Ene07]. The shorter the CPP, the lower the stress generated in the channel, making this technique irrelevant for aggressively scaled devices.

The local stressor used in Intel's 90nm for pFETs consists in **SiGe source/drain**. It was introduced by Gannavaram et al. [Gan00] and is still widely used today for sub-20nm technologies. This technique has been implemented in FinFET technologies, as shown in Figure 1.37 [Aut12], as well as in FDSOI technology [Web15]. Since SiGe has a larger lattice parameter than Si, it features an intrinsic compressive stress, as widely discussed in Chapter 3. By using SiGe in source and drain, a compressive stress is generated into the channel through the relaxation of the SiGe stress. This is more detailed in section 3.3, focusing on the use of SiGe source and drain in FDSOI technology. Similarly to CESL, such a local stressor technique loses its efficiency when the CPP is scaled down, as illustrated in Figure 1.38 [Kha12]. As the volume of embedded SiGe diminishes, the strain transfer drops. Nevertheless, the generated stress is still significant enough, especially combined with other

elements such as the gate-last integration scheme [Idr15; Mor13; Wan09]. The stress generated by SiGe source/drain is indeed higher in gate-last than in gate-first, since the dummy gate removal allows a higher SiGe stress relaxation and thus a higher transfer (see Figure 1.39).

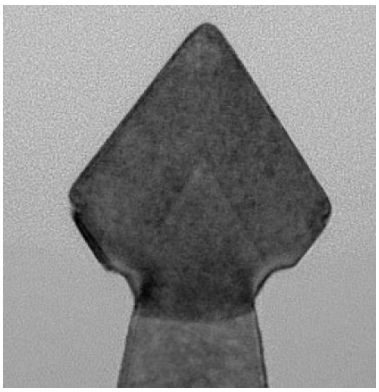


Figure 1.37: TEM cross-section of a FinFET in the source/drain area, showing the SiGe epitaxy, from [Aut12]. The compressive stress generated by SiGe source/drain has been introduced since the bulk 90nm technology [Gha03] and has been integrated into FinFET technologies as well as FDSOI technologies [Web15]. The diamond shape is due to the growth rate dependence with crystal orientation.

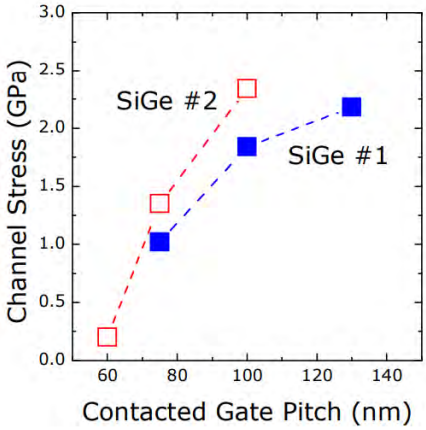


Figure 1.38: Stress generated by SiGe source/drain with respect to CPP (also called Contacted Gate Pitch CGP), from [Kha12]. As the volume of embedded SiGe diminishes, the strain transfer drops. Local stressors are less and less efficient as the CPP scales down.

As far as FDSOI is concerned, the stress can be enhanced by integrating SiGe not only in the raised source and drain but also in the thin film region underneath, as illustrated in Figure 1.40. This is called **Self-Aligned In-Plane Stressor (SAIPS)** [Mor16]. The Ge integration below the raised source/drain can be achieved by Ge-enrichment (also called Ge-condensation, see section 3.1.2.a). the higher stress with SAIPS is due to the increase of average Ge fraction in source/drain region and to the reduction of the distance between the stressor and the channel [Mor16].

Regarding nMOS, the generation of tensile stress from the source/drain material can be achieved by using **Si:C source/drain**. Since Carbon has a smaller lattice parameter than Silicon, Si:C features a tensile stress. Because of the low solid solubility of Carbon in Silicon, the main challenge of this technique is to avoid silicon–carbide precipitation with anneals (the Carbon must be substitutionally incorporated for the Si:C to be stressed) [Tog12]. Nevertheless, some gains have been demonstrated (+20% I_{ON} [Lio08]), as shown in Figure 1.41.

An other locally-introduced strain technique to be mentioned is the **Stress Memorization Technique (SMT)**, early discussed by Ota et al. [Ota02]. It consists in taking advantage of the stress field induced by a dislocation, strategically located close to the channel [Lim10; Web11; Wei07]. The dislocation results from a Solid Phase Epitaxial Regrowth (SPER). This technique generates a tensile stress, beneficial for nMOS. Even though it can be locally introduced for nMOS area only, the co-integration can be problematic because of Boron deactivation issue for pMOS [Ort06]. This technique is anyway not relevant for FDSOI technology since it requires an edge dislocation in for

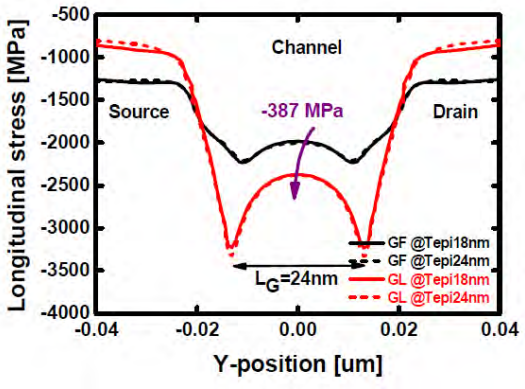


Figure 1.39: Stress profile for Gate-First and Gate-Last FDSOI technology embedding SiGe source/drain stressor, from [Idr15]. In Gate-First integration scheme, the gate holds the structure. The stress transfer is more efficient (-387MPa achieved) in a Gate-Last scheme thanks to the dummy gate removal.

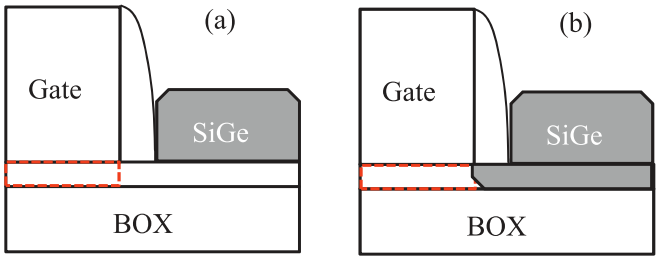


Figure 1.40: Schematic of the (b) Self-Aligned In-Plane Stressor (SAIPS) compared to the (a) conventionnal SiGe source/drain stressor, from [Mor16]. SAIPS induces an additional compressive stress in the channel from an increased volume of SiGe stressor, which is also better localized for transferring the stress into the channel.

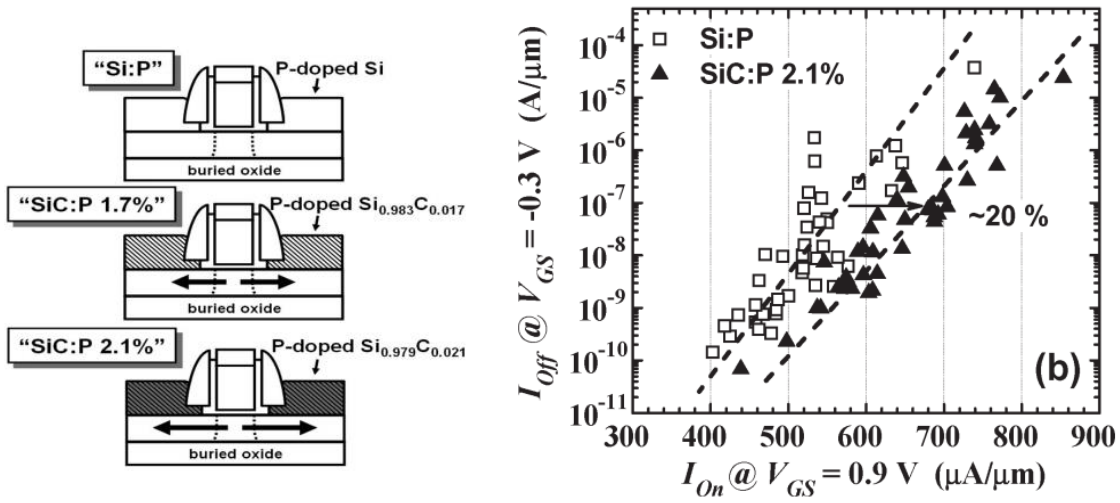


Figure 1.41: (left) Schematic of the tensile stress generated by SiC:P source/drain for nMOSFETs and (b) I_{ON}/I_{OFF} trade-off highlighting +20% ON-current with the introduction of Carbon in source/drain, from [Lio08]. The principle of this technique is the same as using SiGe source/drain stressor but since Carbon has a smaller lattice parameter than Silicon, a tensile stress is generated. Only few percents of Carbon lead to a significant tensile strain. The main challenge of this technique is to avoid silicon–carbide precipitation with anneals (the Carbon must be substitutionally incorporated for the Si:C to be stressed) [Tog12].

generating the stress. Yet it is not compatible with the use of a thin film on insulator.

1.3.3.b Globally-introduced strain techniques

The techniques based on local stressors lose their efficiency with the dimension scaling. That is why the use of intrinsically strained channel is highly relevant. Especially, high level of strain can be achieved.

The most commonly used strained channel is **SiGe channel** for pMOSFETs. As SiGe can be locally

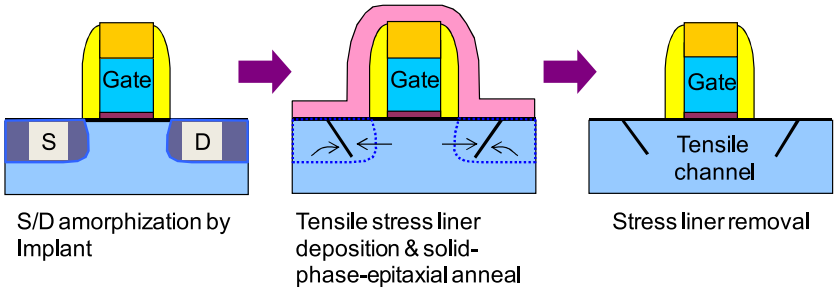


Figure 1.42: Principle of the Stress Memorization Technique (SMT), from [Lim10]. The SMT generates a tensile stress from the edge dislocation induced by Solid Phase Epitaxial Regrowth (SPER), as shown in Figure 1.43.

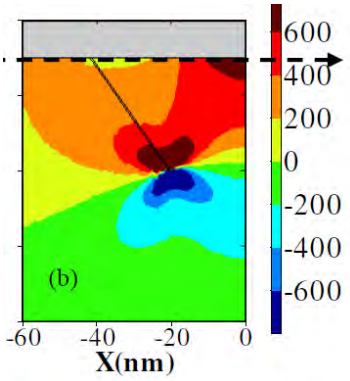


Figure 1.43: Mapping of stress induced by an edge dislocation created by SMT, from [Web11].

grown in pFET areas, it is highly relevant in a co-integration context [Ngu14]. The use of SiGe channel has been demonstrated to be efficient for FinFET performance [Guo16; Has15; Has16; Has17]. As far as FDSOI technology is concerned, the integration of SiGe directly on insulator has been discussed [Che12]. This is achieved by the Ge-enrichment technique, also called Ge-condensation [Glo14], as detailed in section 3.1.2.a. Figure 1.44 illustrates two integration schemes for fabricating SiGeOI and shows the pFET performance enhancement induced by the use of strained SiGe channel [Che12]. The role of the strain on the performance improvement has been pointed out by Khakifirooz et al. [Kha13]: relaxed SiGeOI features same performance as Silicon.

In this work, the integration of SiGe in FDSOI technology is widely discussed in Chapters 3 and 4.

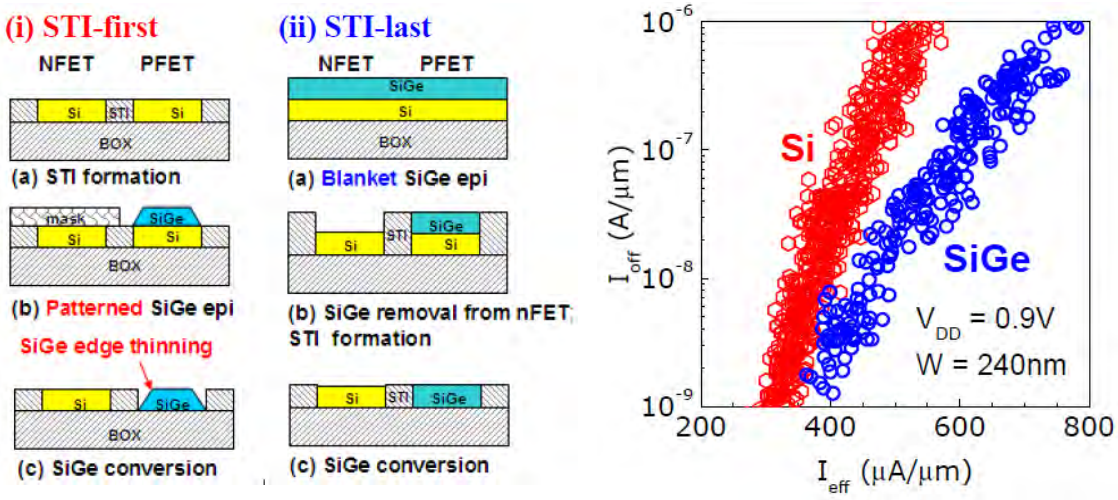


Figure 1.44: (left) Schematic of SiGe integration schemes in FDSOI technology and (right) I_{EFF}/I_{OFF} trade-off for Si and SiGe channel pMOSFETs, from [Che12]. The SiGeOI is fabricated by Ge-enrichment technique (see section 3.1.2.a). It can be done after, before, the STI formation in a so-called STI-first, STI-last, integration scheme, respectively [a]. The SiGe effective current at the same leakage is increased with respect to Si thanks to the compressive stress in SiGe.

a Different SiGe integration scheme in 14nm FDSOI technology have been investigated in section 4.3.1

Regarding nFETs, a tensely strained channel is required. It can be achieved by growing Silicon on a relaxed SiGe buffer [Hua01; Rim03]. As for FDSOI, the interest of using a **strained-SOI (sSOI)** substrate has been widely discussed [And14; Bon16c; DeS14; Rim03]. The tensely strained Silicon directly on insulator is fabricated by first growing a Silicon layer on a gradually relaxed SiGe buffer and then using the SmartCut process to transfer it into a handle wafer [Sch12]. Obviously, the Silicon layer is tensely strained on the whole wafer with such a fabrication process. As a result, it impacts both nMOS and pMOS. This rises one of the main challenge of the use of sSOI: the co-integration, as illustrated in Figure 1.45. The performance of nMOS is significantly improved with sSOI but the pMOS performance is degraded. The use of SiGe channel in pMOS areas with a high concentration of Germanium has been discussed to compensate for the tensile strain of sSOI [And14; Cas12b; Cas12c; Hut10a].

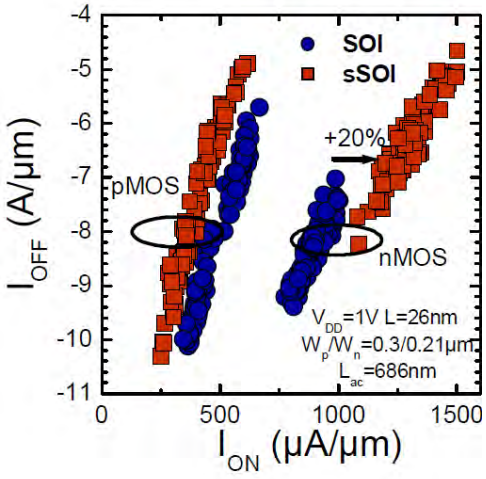


Figure 1.45: I_{ON}/I_{OFF} trade-off for both nMOS and pMOS fabricated on SOI or sSOI substrate, from [And14]. The tensile strain of sSOI results in an improvement of nMOS performance but decreases the pMOS saturation current. This figure highlights the challenge of stress co-integration. In order to enhance the pMOS performance, the tensile stress must be compensated for, by integrating SiGe of high Germanium content [And14; Cas12b; Cas12c].

As for sSOI, the use of a **SiGe Strain Relaxed Buffer (SRB)** in bulk technologies allows a tensely strained Si channel [Ene12; Rim02b]. This technique has been discussed for sub-10nm FinFET technologies [Bae16; Xie16], as illustrated in Figures 1.46 and 1.47. In these integration schemes, the pFET channel consists in SiGe with a higher Ge concentration than in the SRB, in order to achieve a compressive stress. These studies highlight that strain integration is highly required for the scaling of CMOS technology beyond 10nm node.

Finally, the particularity of FDSOI architecture paves the way for innovative strain integration techniques such as the so-called **BOX-creep technique** [Chi08], investigated in this work in section 5.2 or the Strained Si by Top Recrystallization of Amorphized SiGe on SOI (STRASS) [Bon15b; Hal16; Mai15], discussed in section 5.3.

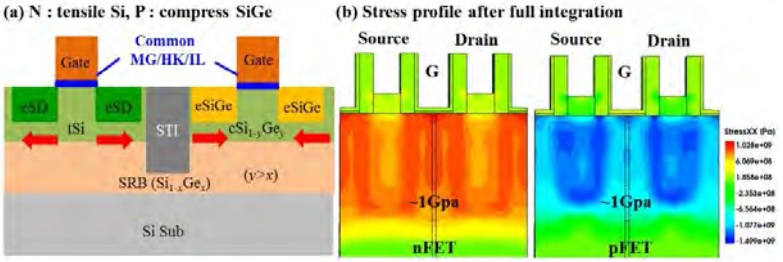


Figure 1.46: (left) Schematic of the dual stress integration technique using a Strain-Relaxed SiGe Buffer (SRB) and SiGe channel for pFET, and (right) inherent simulated stress mapping, from [Bae16]. The Si nFET channel is tensely strained because of the SRB. The SiGe pFET channel is compressively stressed under the condition that the Ge concentration in the channel in higher than the one in the SRB (i.e. $y > x$).

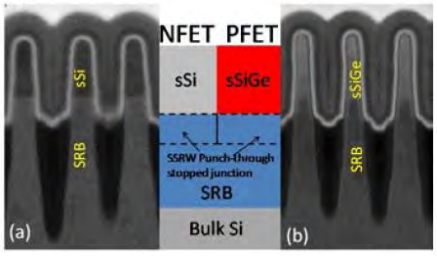


Figure 1.47: TEM cross-section of FinFETs fabricated on SRB, from [Xie16].

1.3.4 Local Layout Effects

In an integrated circuit, the transistor characteristics can vary according to the device environment, i.e. the layout. This is called the Local Layout Effects (LLE). For instance, the Well Proximity Effect (WPE) is related to scattering of ions near photoresist edge during implantation of a specific area. As discussed previously, the stress generation is strongly geometry dependent. In this thesis work, we focus on the **strain-induced layout effects**.

Optimizing an integrated circuit design requires a good knowledge of the performance dependence with the environment. For instance, a circuit can be optimized through an STI-induced stress aware standard cell placement [Kah08]. In this study, the STI generates a stress in the device that impacts the performance. By optimizing the standard cell placement according to this layout effect, a clock frequency improvement of up to 6.3% has been reported.

Aikawa et al. [Aik08] provided an extensive study of the local layout effects in 45nm technology, with focus on stress effects induced by STI and CESL. The study showed that the characteristics depend on the active area shape and the contact location because of different stress levels. Sato et al. [Sat13] investigated the SiGe source/drain and SMT stress-induced layout effects in a 20nm planar technology. Regarding the layout dependence of SiGe source/drain performance booster, it has been widely studied from bulk planar to FinFET devices [Bar13; Jan13; Muj12; Sat13; Son12]. The main layout effect is related to the difference between the "tucked-under" layout, also called Double-Diffusion Break (DDB) or PC-bounded, and the "untucked" layout, also called Single-Diffusion Break (SDB) or STI-bounded (Figure 1.48). The tucked-under layout features active area borders located below dummy gates, contrarily to the untucked layout. The untucked layout shows a slower performance for two reasons. First, the SiGe source/drain volume is smaller in the untucked configuration with respect to the tucked-under one. Secondly, the SiGe stress can relax through the STI in an untucked layout and therefore a low stress is generated into the channel [Sat13]. The stress generated by SMT is also lower for untucked layout because of missing dislocation on active edge [Sat13].

As far as the intrinsically strained channel layout effect are concerned, the dependence with the active area dimension has been evidenced. In particular, Irisawa et al. [Iri05] highlighted the change

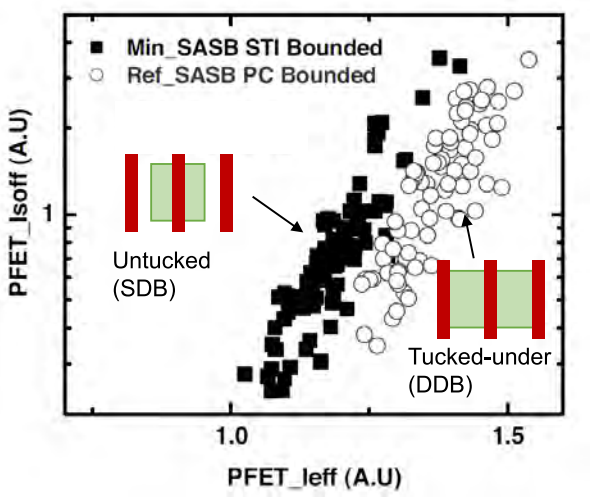


Figure 1.48: Local Layout Effect induced by embedded SiGe source/drain, from [Son12]. A "tucked-under" layout, also called Double-Diffusion Break (DDB) or PC-bounded, features active area borders located below dummy gates, contrarily to an "untucked" layout, also called Single-Diffusion Break (SDB) or STI-bounded. A higher stress is generated in the channel in the case of a tucked-under layout, featuring a higher volume of SiGe source/drain. For an untucked layout, the SiGe stress also relaxes through STI and therefore results in a low stress generated into the channel [Sat13].

of stress configuration induced by the active area patterning, as illustrated in Figure 1.49.

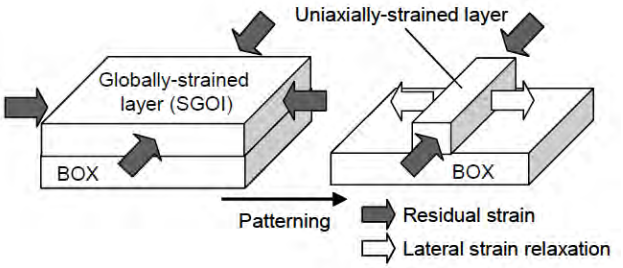


Figure 1.49: Illustration of pattering-induced SiGe strain relaxation, from [Iri05]. The patterning of SiGe on insulator (SGOI) active area shape changes the stress configuration from biaxial to uniaxial.

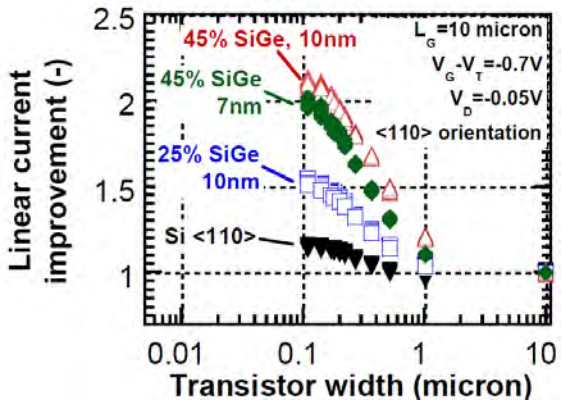


Figure 1.50: Bulk device linear drain current improvement with SiGe active narrowing, from [Ene10]. The enhancement is due to beneficial uniaxial stress configuration.

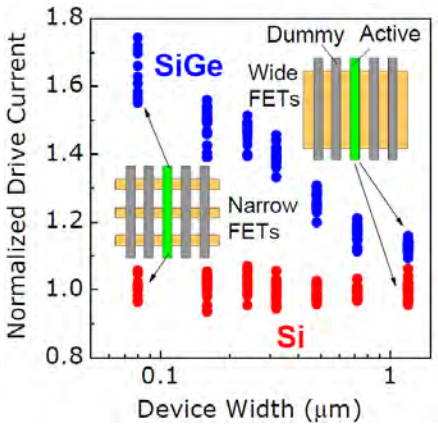


Figure 1.51: FDSOI device drive current improvement with SiGe active narrowing, from [Che12]. The enhancement is due to beneficial uniaxial stress configuration. Inset: optimized design by slicing a large active into several narrow actives.

It has been demonstrated that narrowing the active area of <110>-oriented SiGe channel pFETs results in performance enhancement [And14; Che12; DeS14; Ene10]. This has been highligted for bulk planar, as shown in Figure 1.50 [Ene10], as well as for FDSOI, as as shown in Figure 1.51

[Che12]. This is explained by the lateral strain relaxation induced by the patterning (see Figure 1.49) resulting in uniaxial stress configuration, which is highly beneficial for hole mobility as discussed more widely in Chapter 2.

Also, the detrimental effect of the stress relaxation in the longitudinal direction has been evidenced [And14; DeS14]. This is at the heart of this thesis work. In Chapter 3, the strain-induced local layout effects in FDSOI technology are deeply investigated. In Chapter 4, solutions to mitigate the LLE in order to optimize the performance in FDSOI are presented. Recently, this issue has been also adressed in FinFET technology embeding SiGe channel [Tsu17]. Figure 1.52 shows the relative deformation profile with respect to Silicon in a short fin, measured by Nano-Beam Diffraction. A dedicated fin etching in the longitudinal direction, so-called Poly-Open Cut (POC), enables a higher strain in the fin and in turn improves the performance. The stress is better maintained with this integration scheme because the 3D fin is maintained by the interlayer oxide during the fin cut.

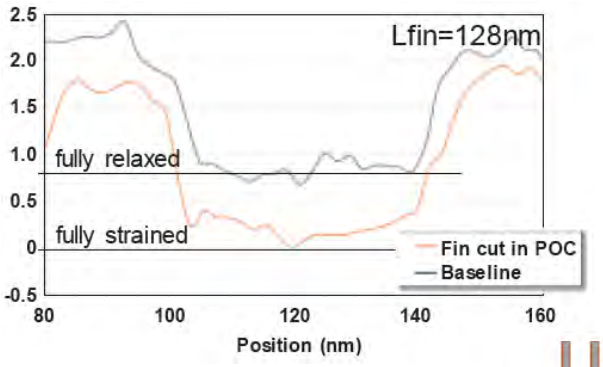


Figure 1.52: Relative deformation profile in a SiGe finFET measured by NBED, from [Tsu17]. The Poly-Open Cut integration scheme yields a higher strain in the 138nm-long fin compared to the baseline, i.e. reference. This is due to the interlayer oxide, which is present during the cut and helps the 3D structure to be held and therefore the strain to be maintained.

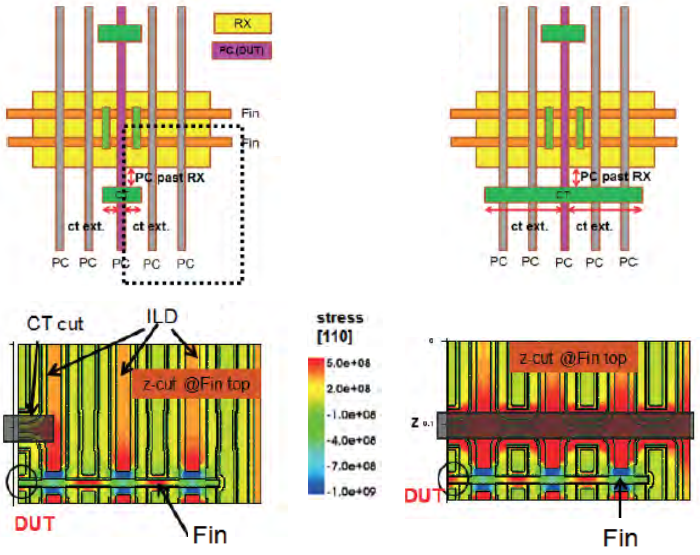


Figure 1.53: Layout and mechanical simulation of FinFETs with different gate cut (labelled CT) configurations, from [Zha17]. The level of stress in the device under test is altered by the gate cut configuration. This is due to the stress induced by the interlayer oxide (ILD).

Beyond the impact of SiGe strain relaxation, the local layout effect induced by the position of the gate cut in advanced FinFET technology has also been recently investigated [Zha17]. In this study, the authors found that the position/configuration of the gate cut modifies the stress generated in the fin by the interlayer oxide, assumed to be tensely stressed, as shown in Figure 1.53.

1.3.5 Summary on strain integration in CMOS technology

By breaking the crystal symmetry, strain modifies the band structure of the Silicon. This directly impacts carrier mobility since the effective mass and scattering mechanisms are altered. Different techniques of stress introduction have been developed in order to boost the CMOS technologies. On the one hand, the local stressors are becoming less and less efficient as the dimensions are scaled down. On the other hand, the introduction of intrinsically strained channel has become necessary to achieve high level of stress and therefore high performance. One of the main challenge of strain engineering is the co-integration, as electron and hole do not benefit from the same stress configuration. The management of the Local Layout Effects (strain is strongly geometry-dependent) is also a main concern.

1.4 Conclusion to Chapter 1

This chapter described the context of this thesis work.

In the first section, the **CMOS logic** has been introduced. Boolean functions are achieved by combining two types of Metal Oxide Semiconductor Field Effect Transistor (MOSFET), acting as switches. The **MOSFET principle of operation** and the main metrics used for its characterization have been presented. In addition, the **Power/Performance/Area metrics** of a CMOS technology have been defined.

The **CMOS technology evolution** over the years has been discussed in the second section. The happy scaling governed by **dimension reduction** has eventually come to an end due to physical limits. The **introduction of goodies** such as the strain engineering in order to keep the scaling and the power consumption reduction has become necessary. **New architectures** such as FinFET and FDSOI have now replaced the historical bulk planar transistors to maintain a good electrostatic control. The stacked nanosheets appear as the most promising candidate to keep the CMOS scaling.

Finally, the last section has provided some insights about the **physics of strained Silicon**. The strain breaks the crystal symmetry and in turn alters the band structure. It results in modified effective masses and scattering events, which are translated into carrier mobility variation. Different **strain integration techniques** used in CMOS technology to boost the performance have been reviewed. The co-integration challenge has been underlined and the local layout effects have been defined.

CHAPTER 2

Strained channel MOSFET performance: mobility and access resistance

Contents

In this Chapter, the performance of strained devices is discussed, focusing on the carrier mobility. Firstly, long channel devices are assessed and the piezoresistive model, which enables to analytically describe the impact of strain, is detailed. Secondly, a focus is made on short channel devices and especially the crucial role of the access resistance. A new method of access resistance extraction is presented. Finally, the impact of strain on the access resistance is discussed through electrical characterizations.

2.1 Long channel mobility impacted by strain

2.1.1 The split-CV technique

The split-CV technique [Koo73; Sod82] allows the effective mobility μ_{eff} in the channel to be extracted. This technique relies on capacitance and current measurements. The gate-to-channel capacitance C_{GC} allows the charge of inversion Q_{INV} to be extracted by integrating from accumulation to inversion according to:

$$Q_{INV}(V_G) = \int_{V_{acc}}^{V_G} C_{GC}(V_G)\,\mathrm{d}V_G \tag{2.1}$$

The linear drain current can be expressed as:

$$I_{DLIN} = \frac{W}{L}\mu_{eff}Q_{INV}V_D \tag{2.2}$$

which leads to the expression of the effective mobility :

$$\mu_{eff} = \frac{L}{W}\frac{I_{DLIN}}{Q_{INV}V_D} \tag{2.3}$$

An example of the mobility extraction from split-CV technique is shown in Figure 2.1.

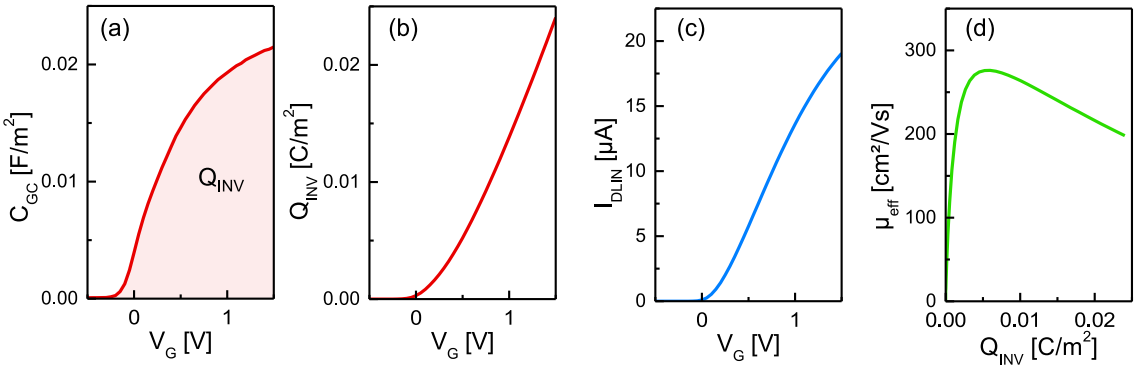


Figure 2.1: The CV-split technique. (a) C_{GC} *vs.* $\mathrm{V_G}$. The integral gives the inversion charge Q_{INV}, shown in (b). (c) Linear drain current. (d) Extracted effective mobility μ_{eff} *vs.* Q_{INV}.

The split-CV has the advantage to directly extract the mobility according to the inversion charge without any assumption. However, this technique is not relevant for short channel devices. The extraction of the intrinsic inversion charge in short channels is limited by the impact of parasitic capacitances (fringing capacitance). A method to take this effect into account has been proposed

[Rom04]. Besides, the impact of the access resistance is neglected. The linear drain current of devices with gate length shorter than 100nm are however strongly impacted by the access resistance. The mobility and access resistance extraction for short channel devices is discussed in section 2.2.

2.1.2 Impact of strain on long channel mobility

The mobility extracted by split-CV for long <110>-oriented channel devices built on either SOI or strained-SOI (sSOI) [Sch12] substrate is shown in Figure 2.2. The electron mobility is highly enhanced by the biaxial tensile strain ($\varepsilon = 0.76\%$ in sSOI). This is mainly due to the conduction band shift leading to repopulation from Δ_4 valleys to Δ_2, featuring a lower effective mass (see 1.3.2). As far as the hole mobility is concerned, the biaxial tensile strain is only advantageous at low inversion charge. This is explained by the opposite effects of strain and confinement on the valence band structure (Light-Hole and Heavy-Hole subbands splitting) [Ber14].

The effective hole mobility for SiGe channel with different Germanium concentrations is shown in Figure 2.3. The higher the Ge content, the higher the hole mobility. This is mainly due to the higher compressive strain induced by the lattice mismatch between Si and Ge. It is worth noting that the hole mobility of SiGe with 22% of Germanium integrated on a sSOI substrate yields similar mobility to the SOI reference. This is because the initial tensile strain in sSOI is counterbalanced by the introduction of SiGe. This result shows that the hole mobility is mainly impacted by the level of strain rather than the amount of Germanium.

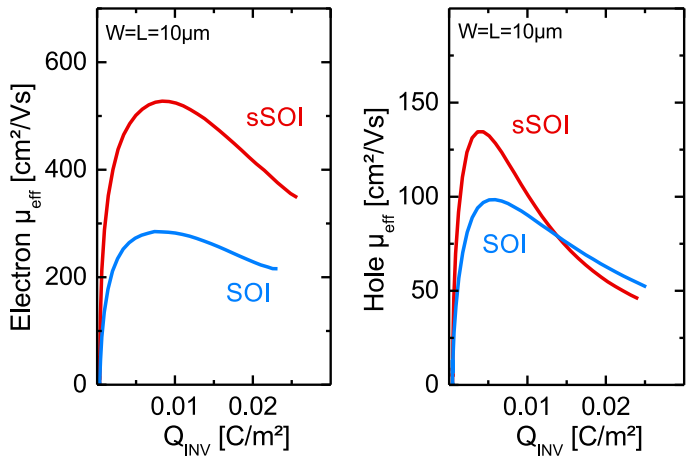


Figure 2.2: Effective (left) electron and (right) hole mobility extracted by split-CV on long channel devices built either on SOI or sSOI. The biaxial tensile strain improves the electron mobility. The hole mobility is enhanced at low inversion charge only.

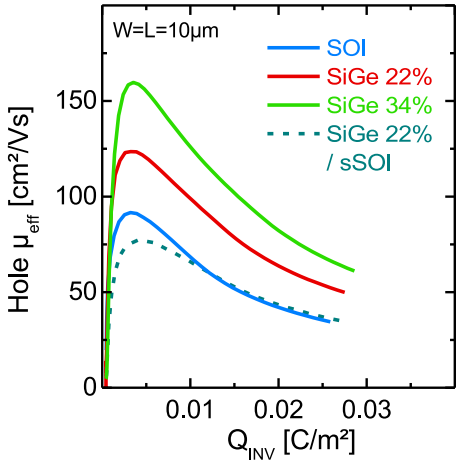


Figure 2.3: Effective hole mobility extracted by split-CV on long channel devices with different Germanium concentrations. The higher the Ge content, the higher the biaxial compressive strain and in turn the higher hole mobility. Similar mobility to SOI is obtained with 22% Ge integrated on sSOI substrate.

2.1.3 The piezoresistivity model

The theory of piezoresistivity links the relative change of mobility (inversely proportional to resistivity) to the stress through the piezoresistivity tensor $[\Pi]$ according to:

$$\left[\frac{\Delta\mu}{\mu}\right] = -[\Pi]\cdot[\sigma] \tag{2.4}$$

It was applied to bulk Silicon and Germanium by Smith [Smi54]. According to the anisotropy of the Silicon crystal, the piezoresistivity tensor is expressed as:

$$\Pi = \begin{pmatrix} \Pi_{11} & \Pi_{12} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{11} & \Pi_{12} & 0 & 0 & 0 \\ \Pi_{12} & \Pi_{12} & \Pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \Pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \Pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \Pi_{44} \end{pmatrix} \tag{2.5}$$

with Π_{11}, Π_{12} and Π_{44} the piezoresistive coefficients. For convenience, the piezoresistive coefficients can be expressed according to the MOSFET channel orientation. The longitudinal, transverse, piezoresistive coefficient corresponds to a stress parallel, perpendicular, to the current flow, respectively. This is illustrated in Figure 2.4 (a). Depending on the channel orientation, the longitudinal and tranverse piezoresistive coefficients for a (001) surface are given by:

$$\begin{aligned} {\Pi_L}^{100} &= \Pi_{11} \\ {\Pi_T}^{100} &= \Pi_{12} \\ {\Pi_L}^{110} &= \frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2} \\ {\Pi_T}^{110} &= \frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2} \end{aligned} \tag{2.6}$$

The piezoresistive model is then expressed as:

$$\frac{\Delta\mu}{\mu} = -\Pi_L\sigma_L - \Pi_T\sigma_T \tag{2.7}$$

where σ_L and σ_T are the longitudinal and transverse stress, respectively. In the case of a biaxial stress, i.e. $\sigma_L = \sigma_T$, the biaxial piezoresistive coefficient Π_S is defined as $\Pi_S = \Pi_L + \Pi_T$. The piezoresistive coefficients can be extracted by a wafer bending technique. The stress is applied with the help of a 4-point apparatus, as shown in Figure 2.4 (a). The linear drain current of a long channel device is measured under different applied stress (Figure 2.4 (b)). The relative change of mobility is assumed to be equal of the current variation. The piezoresistive coefficient is extracted from a linear regression. Figure 2.4 (c) shows the case of the longitudinal piezoresistive coefficient Π_L extraction for SOI and SiGe <110>-oriented pFET. As reported in the literature, the piezoresistive coefficients depend on the initial level of stress in the device. Especially, the piezoresistive coefficents have

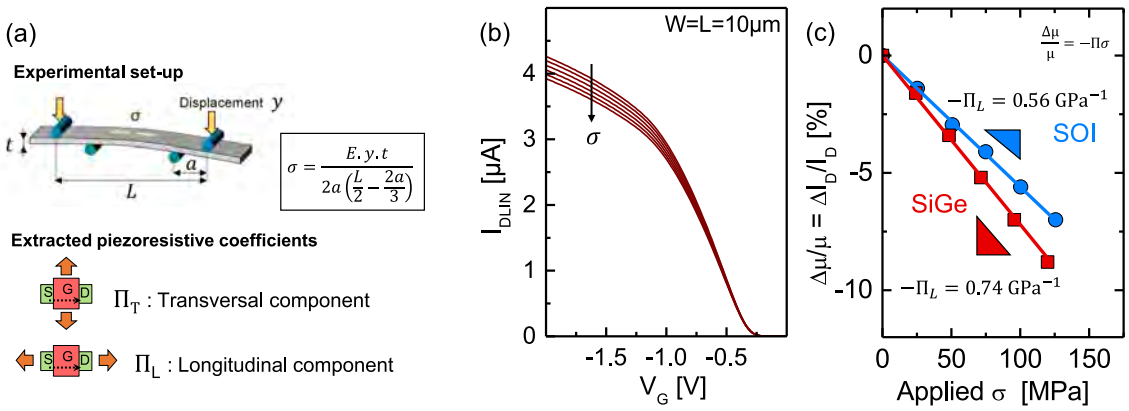


Figure 2.4: (a) Experimental set-up of wafer bending for piezoresistive coefficient extraction and definition of Π_L and Π_T. (b) Si pFET linear drain current *vs.* V_G for different externally applied stress. (c) Longitudinal piezoresistive coefficient extraction from linear regression of linear drain current relative variation w.r.t stress. Π_L of both Si and SiGe <110>-oriented pFETs are extracted.

been measured on sSOI and SiGe channels [Cas12a; Gom10; Web07]. By taking into account the piezoresistive coefficient dependence with the initial level of stress in the channel, the piezoresistivity model can be derived by integrating:

$$\int_0^{\sigma_L,\sigma_T} \frac{\delta\mu}{\mu} = \int_0^{\sigma_L} -\Pi_L(s)\delta s + \int_0^{\sigma_T} -\Pi_T(s)\delta s \tag{2.8}$$

which leads to:

$$\frac{\mu(\sigma_L,\sigma_T)}{\mu(\sigma_L=\sigma_T=0)} = \exp\left(\int_0^{\sigma_L} -\Pi_L(s)\delta s\right)\cdot\exp\left(\int_0^{\sigma_T} -\Pi_T(s)\delta s\right) \tag{2.9}$$

Figure 2.5 shows the piezoresistive coefficients for electron measured on SOI and sSOI with <110>/(001) orientation. Assuming a linear variation of Π with stress (σ=0 for SOI and σ=1.36GPa for sSOI), the model of electron mobility variation with stress is derived according to the equation 2.9. The best strain configuration for electron mobility is biaxial tensile. The gain is mainly due to the longitudinal component in <110>-oriented channel. The transverse piezoresistive coefficient Π_T, which is negative for SOI, becomes positive at high stress (sSOI). This indicates that the transverse stress eventually has a negative impact on mobility. It is thus favorable to integrate a longitudinal stress in nFET to boost their performance.

As far as the hole mobility is concerned, Figure 2.6 shows the piezoresistive coefficients extracted as a function of the Germanium concentration in the SiGe channel. Results show a relatively good agreement with literature [Cas12a; Gom10; Pel14; Web07]. For <110>-oriented channel, the Π_L and Π_T piezoresistive coefficients are of opposite signs. The positive value of Π_L indicates that a longitudinal compressive stress is beneficial. On the other hand, a transverse compressive stress is detrimental for hole mobility since Π_T is negative. For a Germanium concentration higher than 30%, we find that the biaxial piezoresistive coefficient tends to 0, indicating that the hole mobility gain induced by a biaxial compressive stress saturates. The high value of Π_L, maintained with the introduction of Germanium, translates the strong mobility improvement (×4 at σ=-2GPa) induced

by a longitudinal compressive stress.

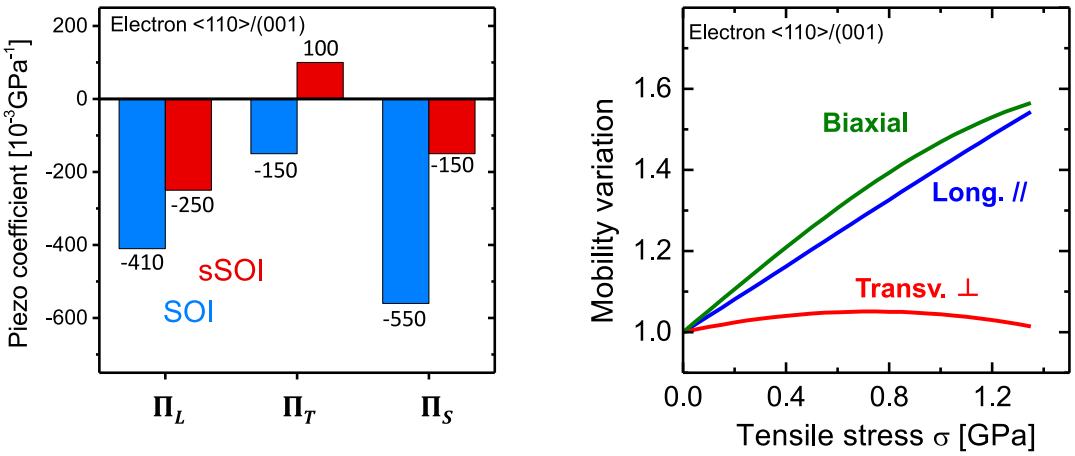


Figure 2.5: (left) Π_L, Π_T and Π_S piezoresistive coefficients extracted on <110>-oriented nFET fabricated on SOI and sSOI. (right) Electron mobility variation with tensile stress derived from equation 2.9. The electron mobility enhancement under biaxial strain is mainly due to the longitudinal component.

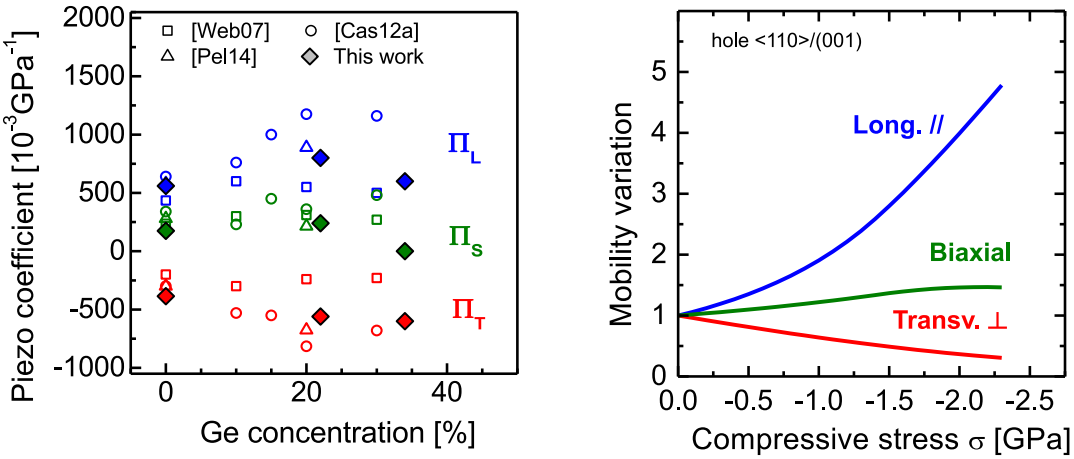


Figure 2.6: (left) Piezoresistive coefficients extracted on <110>-oriented SiGe pFET according to the Germanium concentration. Results are compared with data from [Cas12a; Pel14; Web07]. (right) Hole mobility variation with compressive stress derived from equation 2.9. The longitudinal compressive stress is highly beneficial for hole mobility while the transverse stress is detrimental.

Finally, Figure 2.7 summarizes the impact of stress on electron and hole mobility according to the stress and channel orientations, based on piezoresistive measurements and simulations under the **k·p** framework [Pac08].

Effect of **tensile** stress on **electron** mobility

Orientation	Long.	Transv.	Biaxial
<110>/(100)	++	/	++
<100>/(100)	++	/	++

Effect of **compressive** stress on **hole** mobility

Orientation	Long.	Transv.	Biaxial
<110>/(100)	++++	- -	++
<100>/(100)	+	+	++

Figure 2.7: Summary of the effect of (top) tensile stress on electron mobility and (bottom) compressive stress on hole mobility for <110> and <100> oriented channel on (001) surface.

2.2 Short channel mobility and access resistance extraction

In addition the the mobility, the short channel device performance is also governed by the access resistance. The extraction of both mobility and access resistance has been widely discussed in literature [Cha07; Cro05; Fle09; Ghi88; Hen16; Hu87; Mou00; Rim02a; Tau92]. In this section, we first present the most commonly used methods and then propose a new technique.

2.2.1 Total resistance method

In a MOSFET operating in linear regime, the channel drain current can be expressed as:

$$I_{DCH} = W\mu_{eff}Q_{INV}E_{//} \tag{2.10}$$

with W the channel width, μ_{eff} the effective mobility, Q_{INV} the inversion charge and $E_{//}$ the longitudinal electric field, which can be expressed as $E_{//} = \frac{V_D}{L}$ with V_D the drain voltage and L the channel length. For short channel, the access resistance R_{ACC} must be taken into account. Since the channel and access resistance are in series, we have:

$$R_{TOT} = R_{CH} + R_{ACC} \;\Leftrightarrow\; R_{TOT} = \frac{L}{W\mu_{eff}Q_{INV}} + R_{ACC} \tag{2.11}$$

By measuring the total resistance of transistors with several gate lengths, it is possible to extract the access resistance and mobility from linear regressions [Cha07; Hen16; Rim02a]. The slope gives μ_{eff} and the intercept gives R_{ACC}. Since R_{TOT} can be measured at different V_G, i.e. at different inversion charge, this method allows the extraction of $\mu_{eff}(Q_{INV})$ and $R_{ACC}(Q_{INV})$. Figure 2.8 shows the extraction performed on W=170nm nMOS and pMOS transistors from 14nm FDSOI technology[1]. The extracted mobility and access resistance as a function of the inversion charge is presented in Figure 2.9. The mobility behavior is similar as split-CV method (Figure 2.2 for instance), translating the scattering mechanisms (remote Coulomb, phonon scattering and surface roughness).

1 More details on 14nm FDSOI technology are given in section 3.1

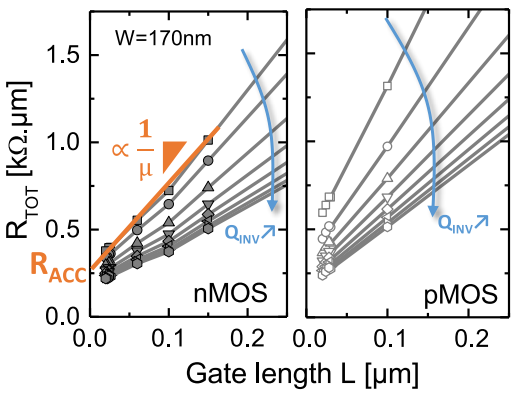


Figure 2.8: $R_{TOT}(L)$ for (left) nMOS and (right) pMOS measured at different inversion charge Q_{INV}. The slope is inversely proportional to the mobility and the intercept gives the access resistance.

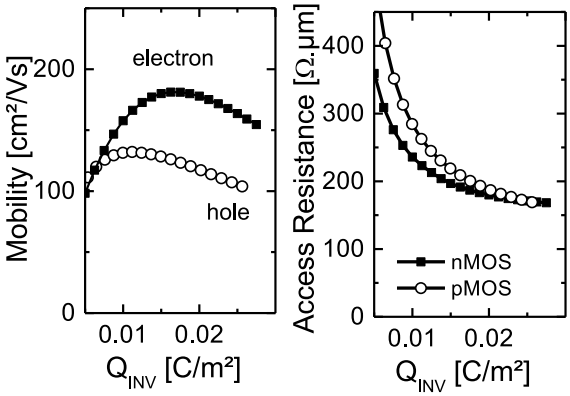


Figure 2.9: (left) $\mu(Q_{INV})$ and (right) $R_{ACC}(Q_{INV})$ for nMOS and pMOS, extracted from the $R_{TOT}(L)$ plot of Figure 2.8. A strong access resistance dependence with inversion charge is evidenced.

The strong advantage of the $R_{TOT}(L)$ technique is its simplicity. It can be used from parametric tests for a rapid evaluation of the device characteristics. Also, it does not make any assumption on the $\mu_{eff}(Q_{INV})$ and $R_{ACC}(Q_{INV})$ behaviors. Nevertheless, this technique assumes a constant mobility with gate length. This is a strong assumption, especially when assessing strained devices where the geometry plays a significant role on the level of strain in the channel. That is why dedicated methodologies are required to extract the mobility in short channel devices.

2.2.2 The Y-function methodology

2.2.2.a Principle

The Y-function methodology [Ghi88; Mou00] has been proposed to extract the short channel mobility. The Y-function method uses the model of current of equation 2.10 . Models of inversion charge and mobility are required. The inversion charge model, only valid in the strong inversion regime, is given by:

$$Q_{INV} = C_{ox,eff} V_{GT} \tag{2.12}$$

with $V_{GT} = V_G - V_T$, V_T being the threshold voltage extrapolated from strong inversion. The mobility dependence with the transverse field (i.e. with the inversion charge) is modeled by:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_{1,0} V_{GT} + \theta_{2,0} {V_{GT}}^2} \tag{2.13}$$

with μ_0 the low field mobility and $\theta_{1,0}$ and $\theta_{2,0}$ the empirical parameters of mobility dependence with inversion charge. The current is thus expressed as:

$$I_{DCH} = \frac{\frac{W}{L} \mu_0 C_{ox,eff} V_{GT} V_D}{1 + \theta_{1,0} V_{GT} + \theta_{2,0} {V_{GT}}^2} \tag{2.14}$$

which can be written as:

$$I_{DCH} = \frac{\beta V_{GT} V_D}{1 + \theta_{1,0} V_{GT} + \theta_{2,0} {V_{GT}}^2} \tag{2.15}$$

with $\beta = \frac{W}{L} \mu_0 C_{ox,eff}$.

By injecting the expression of the channel current (equation 2.15) into the one considering the access resistance (equation 2.11), we have:

$$I_D = \frac{\beta V_{GT} V_D}{1 + (\theta_{1,0} + \beta R_{ACC}) V_{GT} + \theta_{2,0} {V_{GT}}^2} \tag{2.16}$$

The access resistance R_{ACC} has been considered as constant [Ghi88; Mou00] or linearly dependent [Cro05] with the inversion charge Q_{INV}. Assuming a linear dependence:

$$R_{ACC} = R_0 + \lambda \cdot Q_{INV} \tag{2.17}$$

By injecting equation 2.17 into 2.16, we can write:

$$I_D = \frac{\beta V_{GT} V_D}{1 + (\theta_{1,0} + \beta R_0) V_{GT} + \left(\theta_{2,0} + \beta \frac{\lambda}{C_{ox,eff}} \right) {V_{GT}}^2} \tag{2.18}$$

which can be rewritten as:

$$I_D = \frac{\beta V_{GT} V_D}{1 + \Theta_1 V_{GT} + \Theta_2 {V_{GT}}^2} \tag{2.19}$$

2.2.2.b Extraction procedure

The determination of the 4 parameters β, V_T, Θ_1 and Θ_2 by the Y-function methodology is based on an iteration of two successive linear regressions [Mou00]. First the Y-function is derived from:

$$Y = \frac{I_D}{\sqrt{gm}} \tag{2.20}$$

where gm is the transconductance defined as:

$$gm = \frac{\mathrm{d}I_D}{\mathrm{d}V_G} \tag{2.21}$$

By neglecting the Θ_2 term in a first step, the Y-function is expressed as:

$$Y = \sqrt{\beta V_D} V_{GT} \tag{2.22}$$

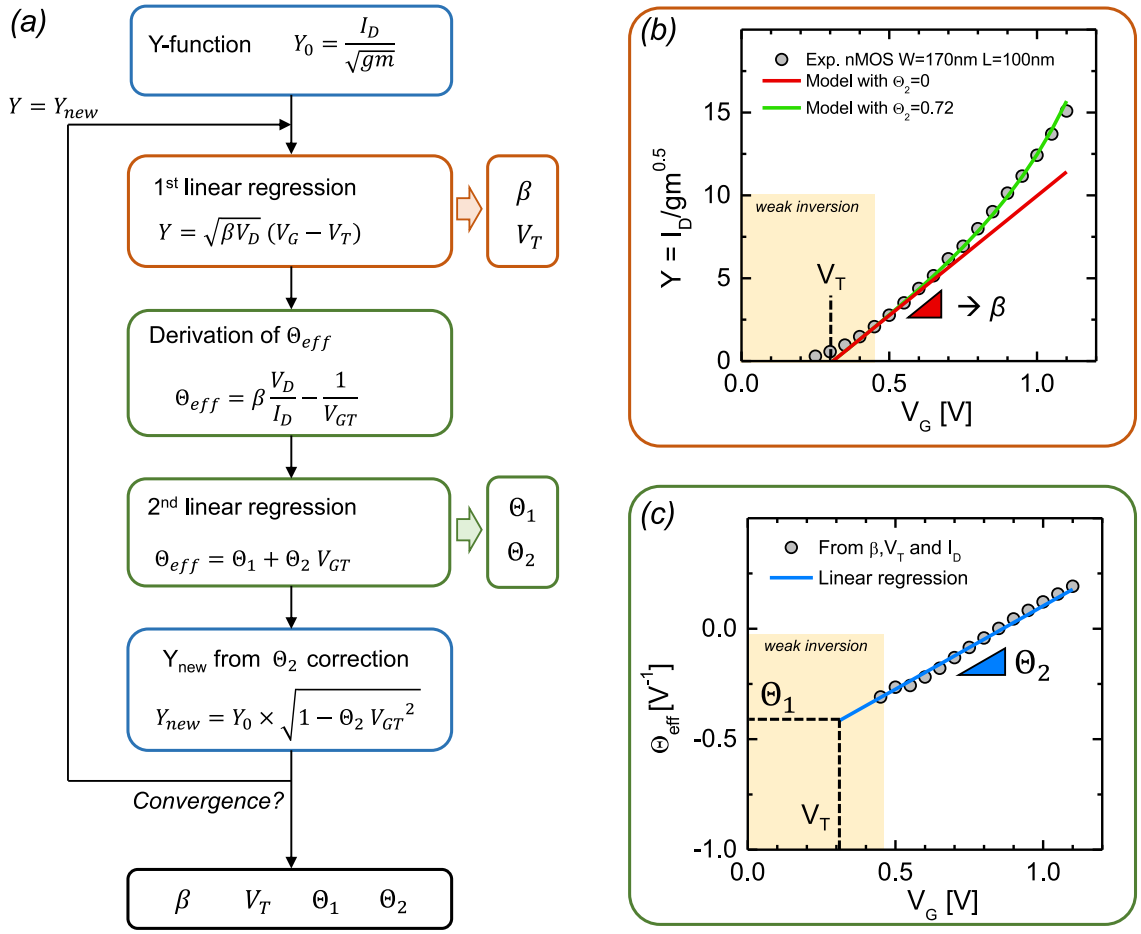


Figure 2.10: Y-function iterative procedure for extraction of parameters. Two successive linear regressions are performed until convergence is achieved.

A linear regression allows the extraction of β and V_T. Then, the Θ_{eff} function is derived according to:

$$\Theta_{eff} = \frac{\beta V_D}{I_D} - \frac{1}{V_{GT}} \tag{2.23}$$

Since Θ_{eff} can also be expressed as $\Theta_{eff} = \Theta_1 + \Theta_2 V_{GT}$, a second linear regression gives Θ_1 and Θ_2. The Y-function is then corrected from the Θ_2 term, initially neglected, according to:

$$Y_{new} = Y \cdot \sqrt{1 - \Theta_2 V_{GT}^2} \tag{2.24}$$

Then, the procedure can be repeated (linear regression on Y_{new} according to equation 2.22 and so on) until convergence is achieved. The Y-function methodology for parameter extraction is illustrated in Figure 2.10.

The $I_D(V_G)$ and transconductance $gm(V_G)$ for W=170nm nFETs from 14nm technology of various gate lengths are shown in Figure 2.11. The experimental data are well reproduced by the model of equation 2.19 in the strong inversion regime.

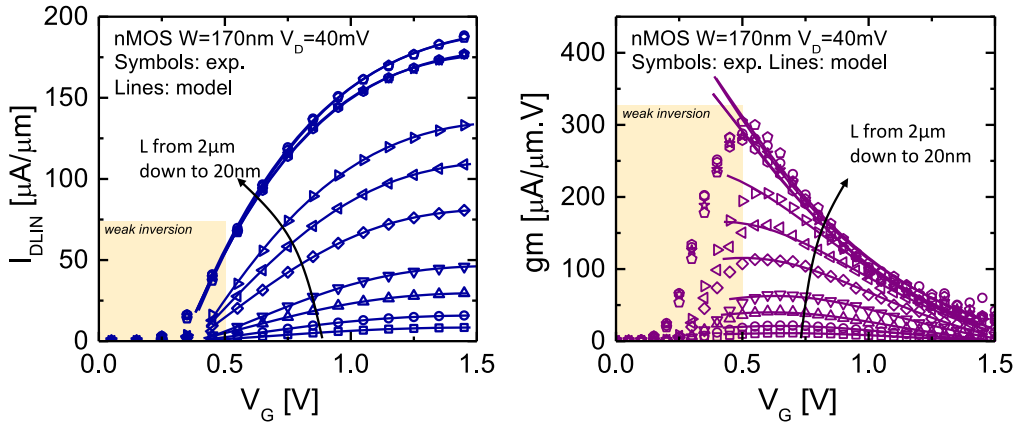


Figure 2.11: (left) $I_D(V_G)$ and (right) $gm(V_G)$ experimental data fitted with Y-function method for nMOS of various gate lengths. The model well reproduces the experimental data in strong inversion regime.

Another method has been proposed to extract the 4 parameters using a so-called ξ-function [Fle08]. This method gives similar results to the classical iterative Y-function method.

Another approach consists in defining the threshold voltage V_T from the one extracted in the subthreshold regime according to:

$$V_T = V_{T,IDth} + \Delta V_T \tag{2.25}$$

with $V_{T,IDth}$ the threshold voltage extracted at a constant current in the subthreshold regime and ΔV_T the shift from subthreshold to strong inversion $\mathrm{V_T}$, with typical value between 50 and 100mV. The 3 others parameters (β, Θ_1 and Θ_2) are then extracted by fitting[1] $R_{TOT} \cdot V_{GT}$ which can be expressed as a polynomial of second order:

$$R_{TOT} \cdot V_{GT} = \frac{V_D}{I_D} V_{GT} = \frac{1}{\beta} + \frac{\Theta_1}{\beta} V_{GT} + \frac{\Theta_2}{\beta} {V_{GT}}^2 \tag{2.26}$$

The inversion charge model $Q_{INV} = C_{ox,eff} V_{GT}$ approximates the $C_{GC}(V_G)$ as a staircase function. This can be considered as a strong assumption regarding the $C_{GC}(V_G)$ behavior (Figure 2.1 (a)). That is why it can be relevant to extract the inversion charge by measuring $C_{GC}(V_G)$ on a long channel device and then considering the threshold voltage shift from long to short. The inversion charge is then given by:

$$Q_{INV}(L) = \int_{V_{acc}}^{V_G + V_{T,IDth}(L) - V_{T,IDth}(L_{long})} C_{GC}(V_G)\, \mathrm{d}V_G \tag{2.27}$$

where $V_{T,IDth}$ is extracted in the subthreshold regime at a constant current. Once Q_{INV} is known, the mobility-related parameters can be extracted by fitting $R_{TOT} \cdot Q_{INV}$ which can be expressed as

1 Levenberg–Marquardt algorithm

a polynomial of second order:

$$R_{TOT} \cdot Q_{INV} = \frac{V_D}{I_D} Q_{INV} = \frac{1}{\beta'} + \frac{\Theta_1{}'}{\beta'} Q_{INV} + \frac{\Theta_2{}'}{\beta'} {Q_{INV}}^2 \tag{2.28}$$

In this case, the β', $\Theta_1{}'$ and $\Theta_2{}'$ parameters have been normalized by $C_{ox,eff}$ according to:

$$\begin{cases} \beta' = \dfrac{\beta}{C_{ox,eff}} = \dfrac{W}{L}\mu_0 \\ \Theta_1{}' = \dfrac{\Theta_1}{C_{ox,eff}} \\ \Theta_2{}' = \dfrac{\Theta_2}{{C_{ox,eff}}^2} \end{cases} \tag{2.29}$$

To summarize, the linear drain current is modeled according to:

$$I_D = \frac{\beta Q_{INV} V_D}{1 + \Theta_1 Q_{INV} + \Theta_2 {Q_{INV}}^2} \tag{2.30}$$

The parameters β, Θ_1 and Θ_2 (which can be normalized by $C_{ox,eff}$) can be extracted either by the iterative Y-function method or a direct fit. The partitioning between mobility and access resistance is then performed in a second step, as discussed in the next sections.

2.2.2.c Access resistance extraction

Once the parameters have been extracted, the access resistance is deduced from the $\Theta_i(\beta)$ plots. By considering a linear dependence of the access resistance with the inversion charge (equation 2.17), the Θ_i parameters are given by:

$$\begin{cases} \Theta_1 = \theta_{1,0} + \beta R_0 \\ \Theta_2 = \theta_{2,0} + \beta \lambda \end{cases} \tag{2.31}$$

Linear regression on $\Theta_1(\beta)$ plot gives $\theta_{1,0}$ and R_0 from the intercept and slope, respectively. Similarly, a linear regression on $\Theta_2(\beta)$ gives $\theta_{2,0}$ and λ. Figure 2.14 shows the $\Theta_i(\beta)$ plots for nMOS, highlighting the good linearity for access resistance parameters extraction. An other method has been proposed, based on the $R_{TOT}(1/\beta)$ plot [Fle09]. However, this method uses the same model of current for the extraction of the β parameter. As a consequence, the result is in line with the classical Y-function based method.

2.2.3 Adapted Y-function with a new model of access resistance

2.2.3.a Motivation: the role of the near spacer region

In previous sections, two methods of access resistance extraction have been presented. The Y-function based method assumes a linear dependence of the access resistance with the inversion charge. However, the extraction with the $R_{TOT}(L)$ method shows a strong $R_{ACC}(Q_{INV})$ dependence, which can not be relevantly approximated by a linear dependence (Figure 2.8).

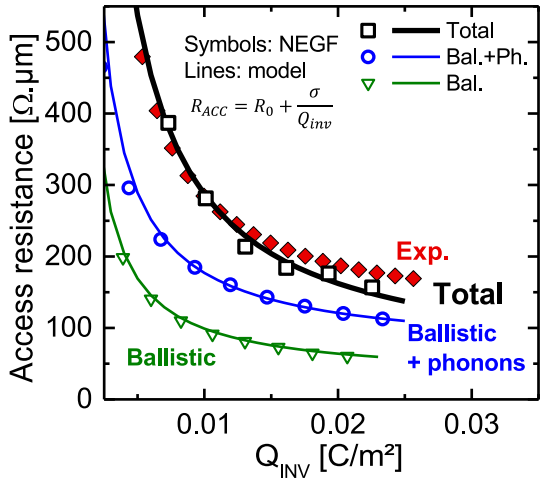


Figure 2.12: Comparison of the access resistance with respect to the inversion charge between a 3D NEGF simulation (black squares) and experiment (red diamonds) for a SiGe pMOS from 14nm FD-SOI technology. The ballistic component and the ballistic+phonon contributions to the access resistance are also plotted. The lines show the fit with equation 2.32.

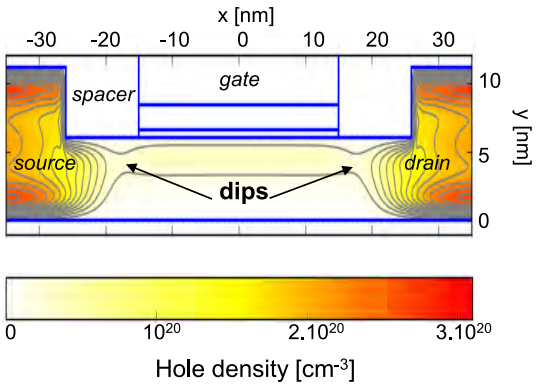


Figure 2.13: Hole density map at large gate overdrive in a planar SiGeOI pMOSFET, obtained from a 2D NEGF simulation. A density dip is observed under the spacer.

Figure 2.12 shows the access resistance of SiGe FDSOI pFETs obtained from Non-Equilibrium Green's Function (NEGF) simulations [1]. Analysis of local quantities has shown that the access resistance can be attributed to the near-spacer region and that the main scattering mechanisms in this region are ionized impurities and phonons. For underlapped devices such as the ones considered in this work, simulations show that, at high gate overdrive, the ballistic resistance is governed by the carrier density dips in the spacer regions. Such dips, illustrated in Figure 2.13, are due to the weak electrostatic control under the spacer. The impact of the near-spacer region has been evidenced in literature [Bou16a; Mon14; Rid14]. Figure 2.12 also shows a breakdown of the access resistance

1 This is a quantum transport method, which accounts for quantum confinement and for the main carrier scattering mechanisms (phonons, surface roughness, ionized dopants, and remote Coulomb). Electrons are described with a 2-band **k.p** model, and holes with a 3-band **k.p** model. Once the microscopic scattering parameters (deformation potentials, surface roughness amplitude) have been calibrated on experimental long channel mobilities, no further parametrization is needed: the simulation treats transport in the whole device, including the inhomogeneous regions. The simulation includes all scattering mechanisms. Surface roughness, ionized dopants, and trapped charges in the gate stack are explicitly included in the geometry, using random roughness profiles and random distributions of charges. Simulations are performed for different channel lengths L, and the access resistance R_{ACC} and channel mobility μ_{eff} are extracted from a $R_{TOT}(L)$ linear regression. The whole methodology and its application to silicon nMOSFETs is detailed in [Bou16a] and references therein.

contributions. The total access resistance is compared with ballistic + phonon contribution, as well as the contribution of ballistic resistance only. All components show a $1/Q_{INV}$ dependence. Especially, each component can be well reproduced using the following model:

$$R_{ACC} = R_0 + \frac{\sigma}{Q_{INV}} \tag{2.32}$$

with R_0 the constant component and σ the parameter of inversion charge dependence.

2.2.3.b New Y-function-based method

By injecting equation 2.32 into the current model of equation 2.16, we can write:

$$I_D = \frac{\beta Q_{INV} V_D}{1 + \left(\theta_{1,0} + \beta\left(R_0 + \frac{\sigma}{Q_{INV}}\right)\right) Q_{INV} + \theta_{2,0} {Q_{INV}}^2} \tag{2.33}$$

which can be rewritten as:

$$I_D = \frac{B Q_{INV} V_D}{1 + \Theta_1 \cdot Q_{INV} + \Theta_2 \cdot {Q_{INV}}^2} \tag{2.34}$$

with:

$$\begin{cases} B = \dfrac{\beta}{1 + \beta\,\sigma} \\ \Theta_1 = \dfrac{\theta_{1,0} + \beta R_0}{1 + \beta\,\sigma} \\ \Theta_2 = \dfrac{\theta_{2,0}}{1 + \beta\,\sigma} \end{cases} \tag{2.35}$$

with $\beta = \frac{W}{L}\mu_0$. Since the expression of the current (equation 2.34) is similar to equation 2.19, the parameters can be extracted according to the methods presented in section 2.2.2. It should be noted that the parameters are expressed with respect to Q_{INV} and not V_{GT}. This is strictly equivalent (normalization by $C_{ox,eff}$). The Θ_i parameters of equation 2.35 can be rewritten as:

$$\begin{cases} \Theta_1 = \theta_{1,0} + B\,(R_0 - \sigma\,\theta_{1,0}) \\ \Theta_2 = \theta_{2,0}\,(1 - B\,\sigma) \end{cases} \tag{2.36}$$

By measuring transistors of different gate lengths, a linear regression on $\Theta_2(B)$ plot yields first σ and $\theta_{2,0}$ parameters. Secondly, R_0 and $\theta_{1,0}$ parameters are given by the slope and intercept of $\Theta_1(B)$ (Figure 2.14).

The extracted access resistance as a function of the inversion charge is presented in Figure 2.15. This result is benchmarked with $R_{TOT}(L)$ method and classical Y-function considering a linear dependence.

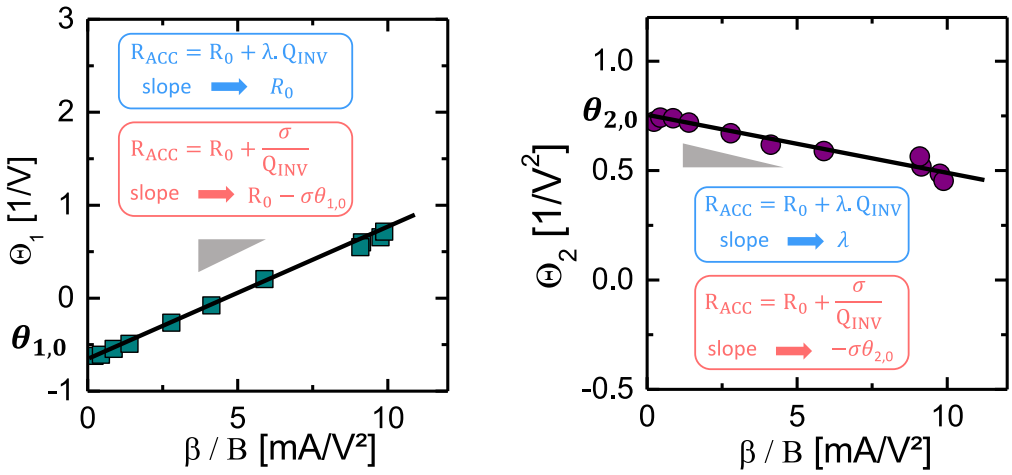


Figure 2.14: (left) Θ_1 and (right) Θ_2 *vs.* β (or B). Linear regressions enable to extract the mobility and access resistance parameters, depending on the model of access resistance (either equation 2.17 or equation 2.32).

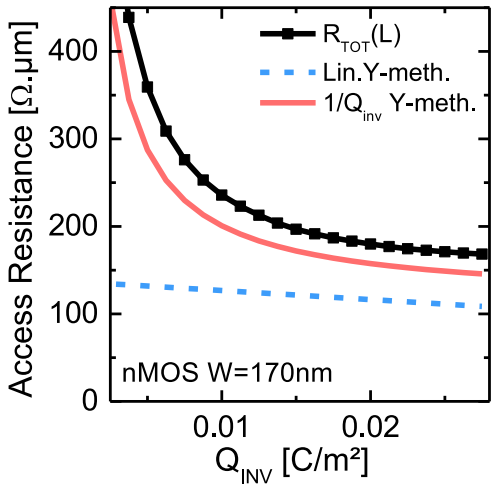


Figure 2.15: Extracted access resistance with respect to the inversion charge according to the method used. Our new methodology gives consistent result with the $R_{TOT}(L)$ method without assuming a constant mobility.

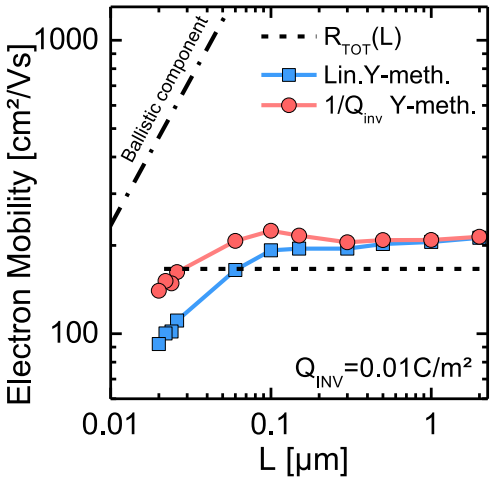


Figure 2.16: Extracted electron mobility at Q_{INV}=0.01C/m^2 with respect to the channel length according to the method used. The mobility drop obtained with the classical Y-function is mitigated with our proposed method.

The access resistance dependence extracted according to our new methodology is consistent with the $R_{TOT}(L)$ methodology, especially at low inversion charge. Besides, it does not assume a constant mobility with respect to the gate length. Once σ has been extracted, the mobility for each gate length can be derived from:

$$\mu_0 = \frac{L}{W} \cdot \frac{B}{1 - \sigma B} \tag{2.37}$$

Figure 2.16 presents the extracted mobility at Q_{INV}=0.01C/m^2. While $R_{TOT}(L)$ assumes a constant mobility, Y-function based methods enable the extraction of the µ(L) behavior. Classical Y-function method suggests a strong mobility degradation when the gate length is reduced (typically for

gate lengths lower than 100nm). This mobility degradation is mitigated with our new extraction methodology. Actually, the low-field mobility μ_0 extracted by the linear Y-function is only an "apparent" mobility since it does not take into account the ballistic regime. According to Shur's model [Shu02], we can write the Matthiessen's rule:

$$\frac{1}{\mu_0} = \frac{1}{\mu} + \frac{1}{\mu_B} \tag{2.38}$$

with μ the intrinsic mobility and μ_B the apparent ballistic mobility defined as:

$$\mu_B = \frac{q \cdot L \cdot v_{th}}{2k_B T} \tag{2.39}$$

giving μ_B/L=23.8cm^2/(V.s.nm) for electron. However this approach does not fully explain the drop of mobility for short gate lengths. This is because the ballistic contribution is not the only responsible for the strong $R_{ACC}(Q_{INV})$ dependence, as the near-spacer region also plays a significant role. As a result, the linear Y-function fails to properly distinguish the channel resistance (i.e. the mobility component) from the access resistance. On the other hand, our new methodology provides a more precise partitioning since the $1/Q_{INV}$ model of access resistance well describes all resistance contributions, including the ballistic one (as seen in Figure 2.12). As a consequence, the extracted mobility μ_0 with this technique should be equivalent to the real intrinsic mobility in the channel. From our results, we evaluate the 20nm-gate-length FDSOI nMOSFETs devices to be 23% ballistic, with μ=140cm^2/(V.s) and apparent ballistic mobility per unit length μ_B/L=23.8cm^2/(V.s.nm), and considering Shur's model [Shu02].

2.2.4 Summary

Table 2.1 summarizes the assumptions of the access resistance extraction methods discussed in this work.

Table 2.1: Summary of access resistance and mobility extraction methods.

Method	µ(Q_{INV})	µ(L)	$R_{ACC}(Q_{INV})$	Ballistic component
$R_{TOT}(L)$	extracted	constant	extracted	in R_{ACC}
Classical Y-function	model	extracted	model	in μ
New Y-function	model	extracted	model	in R_{ACC}

2.3 The impact of strain on access resistance

In this section, we investigated the impact of strain on access resistance by the means of experimental measurements and simulations.

2.3.1 Planar FDSOI

2.3.1.a Experimental results on sSOI

Our new methodology, detailed in the previous section, has been applied to nMOSFETs from 14nm FDSOI technology ([Web15], see section 3.1). NFETs built on either a reference SOI substrate or a strained-SOI (sSOI [Sch12]) substrate are assessed. The latter substrate induces a tensile strain of ε=0.75%. Figure 2.17 shows the linear regressions performed on $\Theta_1(B)$ and $\Theta_2(B)$ plots. Both SOI and sSOI plots show good linearity, making the extraction of access resistance parameters meaningful.

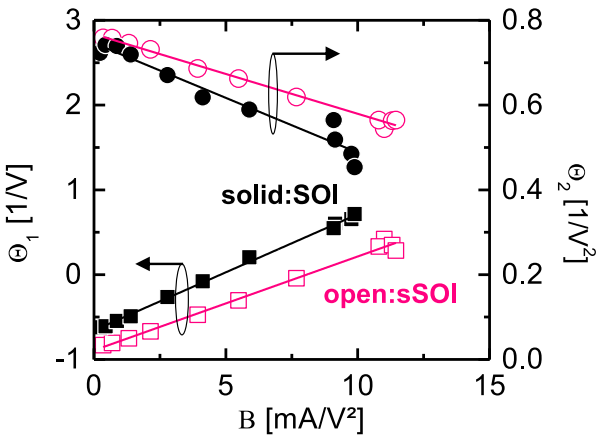


Figure 2.17: Extraction of parameters using $\Theta_1(B)$ and $\Theta_2(B)$ plots for both SOI and sSOI nMOSFETs. Extracted parameters of mobility and access resistance from linear regressions are presented in Table 2.2.

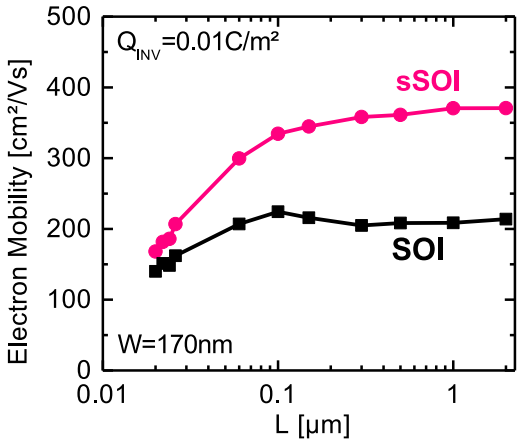


Figure 2.18: Extracted electron mobility μ at Q_{INV}=0.01C/m^2 by our new $1/Q_{INV}$ Y-method (presented in section 2.2.3.b) as a function of the gate length L for W=170nm nFETs built on either SOI or sSOI substrates.

Table 2.2: Extracted parameters from our new Y-function methodology.

Parameter (unit)	SOI	sSOI
σ (Ω.µm.V)	35	25
R_0 (Ω.µm)	114	89
$\theta_{1,0}$ (V^{-1})	-0.66	-0.9
$\theta_{2,0}$ (V^{-2})	0.75	0.76
μ L=20nm (cm^2.V^{-1}.s^{-1})	140	168

The Table 2.2 summarizes the extracted parameters. One has to note that Θ_1, Θ_2 and σ parameters have been normalized by $C_{ox,eff}$ for convenience purpose. Figure 2.19 shows the extracted electron mobility of a 2µm gate-length and 170nm-gate-width device as a function of the inversion charge for both SOI and sSOI. As expected, the tensile stress is highly beneficial for electron mobility. An improvement of +68% is observed at an inversion charge of Q_{INV}=0.01C/m^2.

The extracted access resistance according to the inversion charge is presented in Figure 2.19. In addition to the mobility gain, the access resistance is significantly reduced by integrating tensile strain in the channel. Both R_0 and σ parameters are significantly lower for sSOI than SOI (89 *vs.* 114 Ω.µm and 25 *vs.* 35Ω.µm.V, respectively). By using a strained-SOI substrate, the nMOS access resistance is reduced by 25% at Q_{INV}=0.01C/m^2. The Figure 2.18 depicts the µ(L) behaviors, evidencing

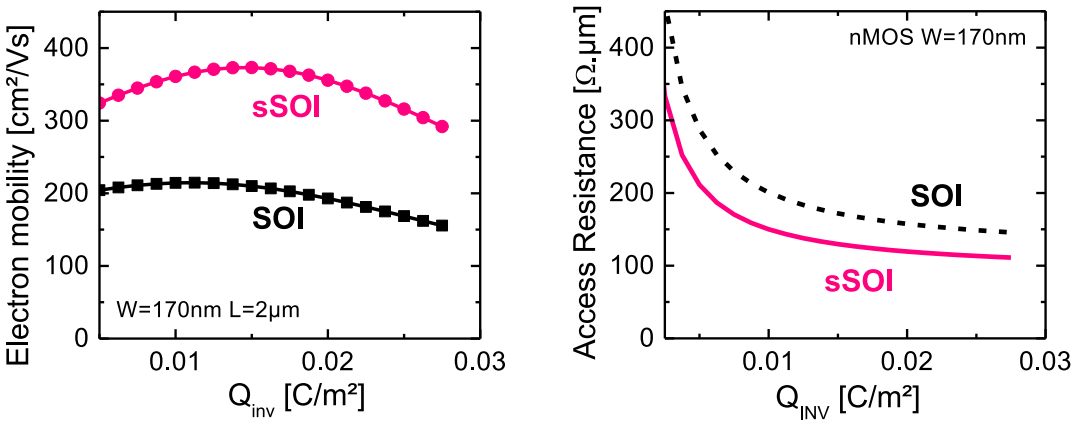


Figure 2.19: Extraction by our new $1/Q_{INV}$ Y-method of (left) electron mobility as a function of the inversion charge for L=2µm W=170nm nMOS built on SOI and sSOI substrates and (right) access resistance *vs.* inversion charge. Tensile strain from sSOI substrate yields both an enhancement of the electron mobility and a reduction of the access resistance (-25% at Q_{INV}=0.01C/m^2).

a higher mobility degradation for sSOI than SOI when the gate length is reduced. This could be attributed to a partial strain relaxation for short gate lengths. Finally, a mobility improvement of 20% is obtained using sSOI for L=20nm at Q_{INV}=0.01C/m^2.

By integrating strain, the band structure of Silicon is altered. The effective mass is modified by band warping and subband repopulation. In addition, the phonon scattering mechanisms are affected by subband splitting. As a result, the carrier mobility in the channel is impacted by strain. There is no reason for the near-spacer region not to be subjected to the same physical phenomenon. As a consequence, strain not only impacts the carrier mobility in the channel but also the access resistance component.

2.3.1.b SiGeOI NEGF simulations

The impact of strain on the access resistance has been experimentally evidenced on tensely strained nFETs. In order to investigate the effect of strain on p-type devices, SiGeOI pMOSFETs under different compressive stress configurations are assessed by the means of 2D NEGF simulations. 2D simulations provide the ballistic and phonon contributions to the access resistance. The studied stress configurations are unstressed, biaxial compressive and uniaxial longitudinal compressive (i.e. parallel to the current flow in the <110> direction). Figure 2.20 reports the calculated access resistance for the three stress configurations. Similarly to nMOSFETs, the calculated access resistance is found to be highly sensitive to the stress configuration for pMOSFETs. Especially, a longitudinal compressive stress is even more beneficial than a biaxial stress. This is consistent with what is observed on hole mobility (section 2.1.3). Figure 2.21 shows that both ballistic and phonon contributions are impacted by the strain configuration. The ballistic resistance reduction mainly comes from the change in effective mass, while the diffusive one is more sensitive to the reduced phonon scattering events induced by subband splitting.

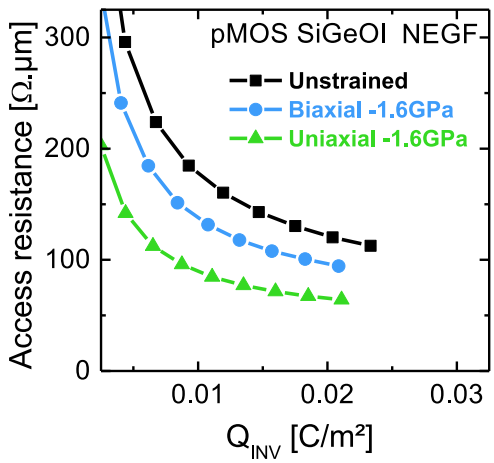


Figure 2.20: 2D NEGF simulations of SiGeOI pMOSFET access resistance under different stress configurations considering ballistic and phonon contributions. The access resistance is reduced under compressive stress. Especially, the longitudinal stress (i.e. parallel to the 110-oriented channel) is highly beneficial.

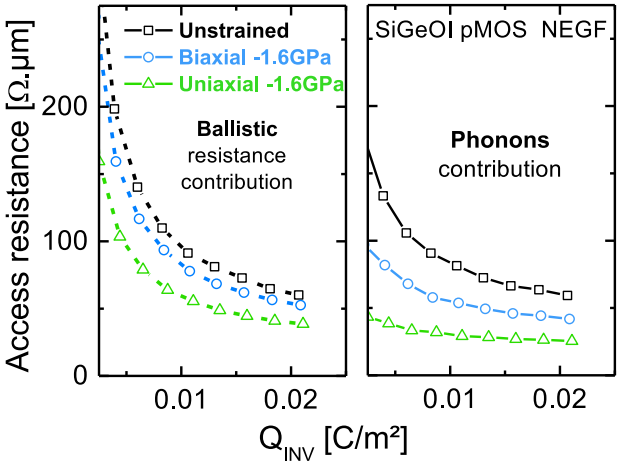


Figure 2.21: 2D NEGF simulations of SiGeOI pMOSFET access resistance under different stress configurations with (left) ballistic contribution only and (right) phonon contribution only. The ballistic resistance reduction is mainly due to the effective mass change, while the diffusive one is induced by subband splitting.

2.3.2 Nanowires embedding strain

Besides planar FDSOI devices embedding global stressor, we investigated Ω-gate-shaped nanowires embedding local stressors. The section of such devices, which are fabricated at CEA-LETI, is defined by the sidewall height H and the top width W_{TOP}. Figure 2.22 shows a TEM cross-section of an Ω-gate nanowire.

First, n-type nanowires with critical dimensions of W_{TOP}=9nm and H=11nm are assessed. Their narrow section ensure a good electrostatic control with DIBL as low as 50mV/V for nMOSFETs at L=20nm. These devices embed CESL of compressive, neutral and tensile stress (c-CESL, n-CESL and t-CESL, respectively). We applied our new Y-function based methodology (section 2.2.3.b) to extract both the mobility and the access resistance. The extracted electron mobility is reported according to the gate length in Figure 2.23. For gate lengths shorter than 50nm, the mobility is degraded and no effect of CESL type is observed. This is because the mechanical stress transfer becomes inefficient at such dimensions, as discussed in [Ene07]. Nevertheless, the CESL impact is manifest for longer gate lengths, in the range 50-400nm. The electron mobility is degraded with compressive CESL whereas a tensile CESL yields a mobility enhancement, as already observed in the literature [Mor12]. The mobility variation with the gate length emphasizes the interest of our new methodology to assess the impact of strain. It would indeed be irrelevant to consider a constant mobility with the gate length in such strained devices. Figure 2.23 also shows the extracted access resistance as a function of the inversion charge. Similarly to planar devices, a strong access resistance dependence with inversion charge is observed. In addition to the CESL stress effect on mobility, we evidence its impact on access resistance. The trend is consistent with the mobility behavior: compared to a neutral CESL, a tensile (compressive) CESL yields a lower access resistance (higher, respectively).

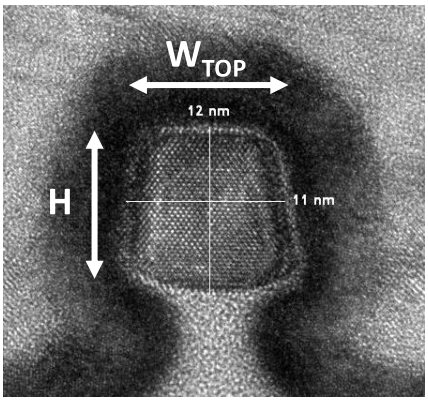


Figure 2.22: TEM cross-section of Ω-gate-shaped nanowires investigated in this work. The section is defined by the sidewall height H and the top width W_{TOP}. The narrow section ensures a good electrostatic control.

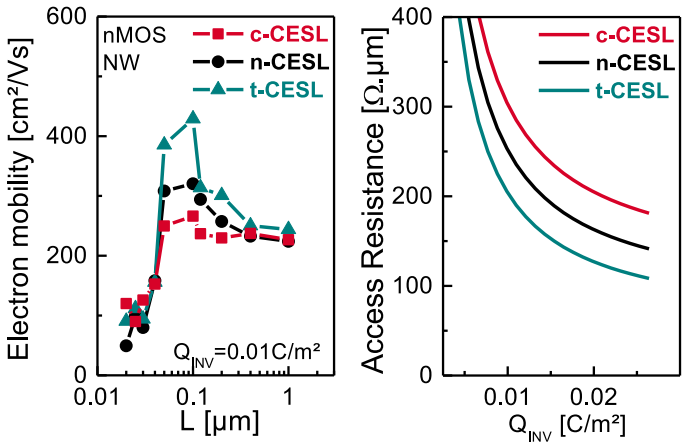


Figure 2.23: (left) Extracted electron mobility for Ω-gate nMOSFET nanowires according to the gate length. (right) Extracted access resistance as a function of the inversion charge for the same devices. As for mobility, the CESL stress impacts the access resistance. A tensile-CESL (compressive CESL) is beneficial (detrimental, respectively).

Our new methodology is also applied to pMOSFET Ω-gate nanowires with either Si or SiGe source and drain. These devices show DIBL of 33-40mV/V at L=80nm, W_{TOP}=20nm and H=14nm. The extracted hole mobility is reported in Figure 2.24 as a function of the gate length. Long channel (L=1µm) mobility is not impacted by the SiGe source/drain. The shorter the gate length, the higher the mobility with SiGe source/drain. This is consistent with the mechanical behavior of the structure. As the pseudomorphically grown SiGe source/drain tend to relax, longitudinal compressive stress is generated into the channel. The shorter the gate length, the higher the mechanical stress transfer, hence the strong mobility improvement when gate length is reduced. In addition, using SiGe source/drain results in access resistance reduction (-37% at Q_{INV}=0.01C/m^2), as reported in Figure 2.24. Our simulations (see section 2.3.1.b) suggest that this access resistance reduction is at least partly due to the strain integration in the device. In this case however, the access resistance reduction could also be the consequence of the source/drain material change [1].

Finally, pMOSFET Ω-gate nanowires with either Si or SiGe channel are studied. The impact of the global stress induced by SiGe is assessed by the means of the R_{TOT}(L) method [2]. The linear regression performed at V_{GT}=0.8V and the extracted access resistance are shown in Figure 2.25. The use of a SiGe channel leads to -39% R_{ACC} reduction with respect to reference Si channel. This result is in agreement with our previous findings.

2.3.3 Summary and SPICE predictions

The impact of strain on the access resistance has been experimentally evidenced on a large set of devices (planar and Ω-gate nanowires) featuring different strain integration techniques (global and

1 The use of SiGe in source/drain could result in a better dopant activation and/or contact resistance reduction.
2 Y-function based methods were not possible on these devices since only the parametric tests were available (i.e. no full $I_D(V_G)$ measurements).

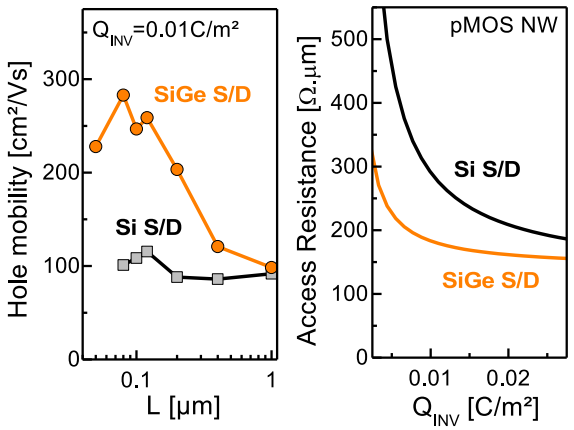


Figure 2.24: (left) Extracted hole mobility as a function of the gate length of pMOSFET Ω-gate nanowires with either Si or SiGe source/drain. (right) Extracted access resistance on the same devices. SiGe source/drain leads to enhanced hole mobility, especially for short channel devices, and also yields lower access resistance.

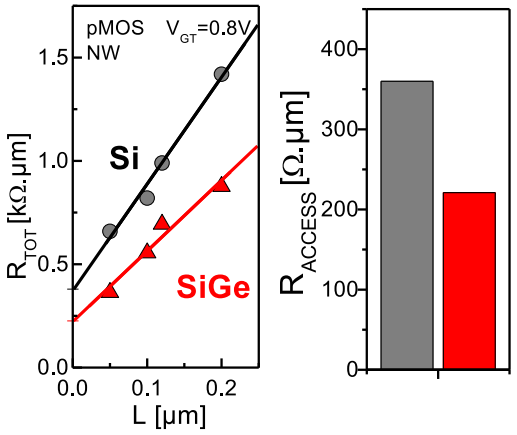


Figure 2.25: (left) $R_{TOT}(L)$ at V_{GT}=0.8V for Ω-gate pFET nanowires featuring Si or SiGe channel. (right) Extracted access resistance from the intercept of the linear regression. The access resistance is reduced by 39% from Si to SiGe channel.

local stressors). In addition, such a behavior is theoretically confirmed by NEGF simulations. We attribute this phenomenon to the crucial role of the near-spacer region in the access resistance of the device. The strain indeed alters the transport properties in this region.

Figure 2.26 plots the relative variation of the access resistance with respect to the one of the channel resistance (inversely proportional to the mobility). For all the devices investigated, a good correlation is observed with almost a 1:1 trend [1].

We have included the experimental $R_{ACC}(strain)$ dependence into the compact model of FDSOI (UTSOI compact model [Poi15]). We then simulate a ring-oscillator of inverter through Simulation Program with Integrated Circuit Emphasis (SPICE) using ELDO software [Men]. Our conditions of reference include a three-finger inverter IV-SX3, a supply voltage of V_{DD}=0.8V and a fan-out FO=3. Assuming a strain increase of ε_n=0.75% for nFETs and ε_p=-0.5% for pFETs, the ring-oscillator frequency is enhanced by +11% considering only the mobility enhancement with strain (Figure C.6). If we now consider the $R_{ACC}(strain)$ dependence, the frequency enhancement is expected to reach +18%. This evidences that it is mandatory to take into account the impact of strain on R_{ACC}.

1 The "planar pMOS SiGe channel"-labeled devices are discussed in section 3.4.3, Figures 3.53, 3.54 and 3.55

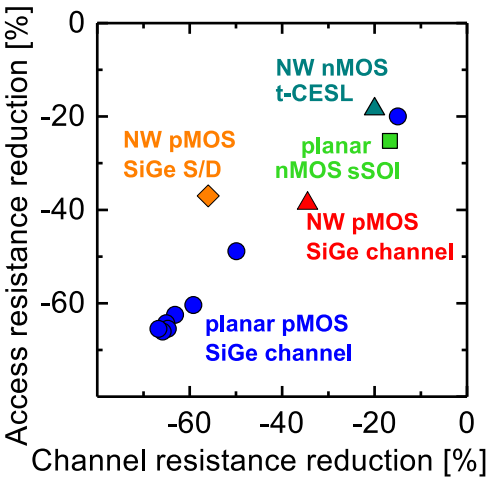


Figure 2.26: Correlation plot of access resistance variation with respect to channel resistance variation. The reference is unstrained device (except for the "planar pMOS SiGe channel", discussed in Figure 3.53). The access resistance is impacted by strain to the same extent as the mobility is.

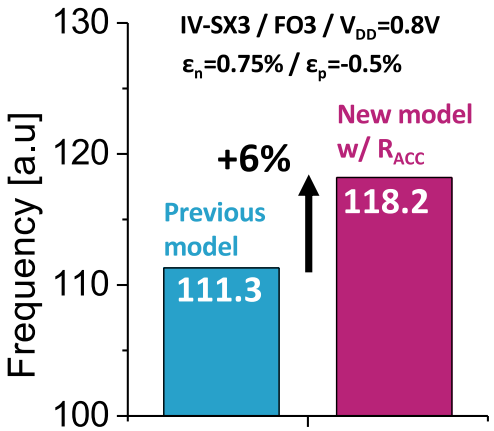


Figure 2.27: Three-finger inverter ring-oscillator frequency considering additional strains with respect to the previous planar FDSOI model ([Poi15], 14nm technology). The access resistance dependence with strain contributes to +6% frequency improvement.

2.4 Conclusion to Chapter 2

In this Chapter, the performance of strained MOSFETs has been discussed.

First, long channel devices have been investigated. By altering the crystal properties, strain modifies the carrier mobility. The carrier mobility in long channel devices embedding strain has been extracted by the means of the CV-split technique. The electron and hole mobility are enhanced by the integration of a tensile, compressive, strain, respectively. The piezoresistive model is relevant to assess the impact of strain on mobility. Especially, it provides the mobility sensitivity to the different stress configurations. For instance, **the longitudinal stress component is highly efficient in 110-oriented channels, especially for holes.**

In a second step, focus was made on strained short channel devices. The extraction of both mobility and access resistance has been widely discussed. **A new method, based on the Y-function technique, has been presented.** It enables the role of the near-spacer region in the access resistance to be well accounted for. This has been confirmed by NEGF simulations. Finally, our new methodology for parameter extraction allowed us to investigate the impact of strain on access resistance. **The access resistance dependence with strain has been evidenced on a large set of devices** (planar FDSOI and Ω-gate nanowires). It has also been confirmed by NEGF simulations. This is attributed to the near-spacer region, which is subjected to the strain-induced change of material properties.

This conclusion reinforces the interest of strain integration for increasing the performance of advanced CMOS devices. In addition, it must be taken into account into spice for predictive benchmarking and optimized integrated circuit designs.

CHAPTER 3

Strain-induced layout effects in SiGeOI pMOSFETs

Contents

As discussed in previous chapters, strain integration is an effective knob to boost the device performance. Especially, intrinsically strained channels exhibit high level of stress (>1GPa). Regarding pFETs, introducing a SiGe channel yields high compressive stress, which is beneficial for hole mobility.

In this chapter, we assess the Local Layout Effects inherent to the introduction of a SiGe channel in FDSOI pFETs. After briefly defining the FDSOI technology we have studied, a focus is made on the level of strain in patterned SiGeOI by the means of physical characterizations and mechanical simulations. The impact of SiGe source/drain is also discussed. We then propose an empirical model of stress relaxation to reproduce the layout dependence of SiGeOI pFETs electrical characteristics.

3.1 FDSOI technologies and devices

3.1.1 28nm and 14nm FDSOI technologies at a glance

The heart of this thesis work relies on Fully Depleted Silicon On Insulator (FDSOI) technology. This technology has been jointly developed by STMicroelectronics and the CEA-Leti. FDSOI technology appears as an alternative to mainstream FinFET based technology especially when it comes to low-power applications driven by Internet of Things (IoT) market. Among the strengths of FDSOI, one can mention the lower cost, the ease to transfer a bulk design into FDSOI because it is planar, its relevance for RF applications and, and last but not least, its great back-biasing capability.

STMicroelectronics first developed the 28nm FDSOI technology [Pla12], followed by the 14nm one [Web14; Web15]. The key elements of both technologies are summarized in Figure 3.1.

Element	28nm FDSOI	14nm FDSOI
Substrate	<100>	<110>
Channel	7nm (Si)	6nm (dual Si/SiGe)
BOX	25nm	20nm
Gate	HKMG single metal	HKMG dual WF
Source/drain	Si epi + Implant	Dual raised in-situ doped Si:CP / SiGe:B
Well LVT/RVT	Flip-well / Regular-well	Flip-well / Flip-well
CPP	136nm	90nm
M1 pitch	90nm	64nm
L_{gate}	30nm → 46nm	20nm → 34nm

Figure 3.1: Key element comparison of 28nm *vs.* 14nm FDSOI technologies.

From 28nm to 14nm, significant changes have been made:

- The channel orientation is rotated from <100> to <110>. Since the longitudinal compressive stress is highly beneficial in the <110> orientation, it results in high pFET performance.
- A dual channel Si/SiGe for nMOS/pMOS is used in 14nm FDSOI in order to boost the performance of pFET and reduce the threshold voltage.
- The Buried Oxide thickness is reduced from 25nm to 20nm to maintain a good body-bias efficiency while the EOT is reduced for the electrostatic control, enabling the gate length to be

scaled without suffering from dramatic short channel effects.

- Both technologies embed a High-k[1] Metal Gate (HKMG) stack constituted of 1nm interlayer (IL) SiO_2, 2nm HfO_2 and 3.5nm TiN. However, a dual Work-Function is available in 14nm to better adjust the threshold voltage of the different flavors. In logic, the T_{inv} of nFET, pFET, is 13Å, 14.5Å, respectively.
- Raised source/drain of 28nm are made of two-step Si epitaxy and dopants are introduced by implants. For 14nm, junctions consist of a dual raised in-situ doped epitaxy with Si:CP for nFET and SiGe:B for pFET. The latter introduces compressive stress in the channel as discussed in section 3.3.1.
- Both 28nm and 14nm Low-VT (LVT) flavors are in flip-well architecture (see Figure 3.3). The flip-well architecture consists in a N-type well for nFET and a P-type for pFET. This allows Forward-Back-Bias (FBB), on the opposite of a regular-well architecture (P-type well for nFET, N-type well for pFET) that enables Reverse Back-Bias (RBB). The Regular-VT (RVT) flavor of 14nm is also in flip-well architecture to allow flavor mix-ability (designing LVT and RVT standard cells close together at a fine granularity).
- The Contacted Poly Pitch (CPP) is scaled from 136nm to 90nm while the first level of metal (M1) pitch is scaled from 90nm to 64nm for density.
- The minimum designed gate length in 28nm FDSOI is 30nm while it is 20nm for 14nm FDSOI. Both technologies allow larger gate at minimum CPP by the means of poly-bias. This offers a fine tuning of performance/leakage trade-off, basically based on the $V_T(L)$ behavior.

Figure 3.2 shows a simplified process flow of the 14nm FDSOI technology. The SiGe channel and the hybrid areas[2] are fabricated prior to the active area patterning. The dual raised source and drain are fabricated after the gate in a so-called gate-first scheme. Figure 3.2 also shows TEM pictures at the end of the process flow, focusing on the nFET and pFET nominal devices as well as on the MEOL interconnections.

In the 14nm FDSOI technlogy, both Low-VT and Regular-VT flavors are in Flip-well architecture. In such a configuration, the nMOS, pMOS, back plane is N-type, P-type, respectively. The two back planes are isolated from each others by a PN junction, i.e. a diode. This diode must be biased in reverse to avoid leakage. As a result, the Flip-well architecture allows Forward back-bias (FBB), i.e. positive back-bias applied on nMOS and negative back-bias applied on pMOS. This leads to a possible V_T reduction for both nMOS and pMOS, achieving high speed at the expense of high leakage. On the other hand, the Regular-well architecture consists in a P-type back plane for nMOS and an N-type for pMOS. The PN junction allows Reverse back-bias (RBB), i.e. negative back-bias applied on nMOS and positive back-bias applied on pMOS. The threshold voltage can thus be increased, leading to low static power consumption but at the expense of low speed. A dual-isolation scheme

1 "High-k" dielectrics have a higher dielectric constant than SiO_2. This allows to increase the capacitance without reducing the physical thickness that could lead to dramatic gate leakage by tunnel effect. The most commonly used high-k dielectric are Hafnium-based.

2 also called NOSO for No SOI

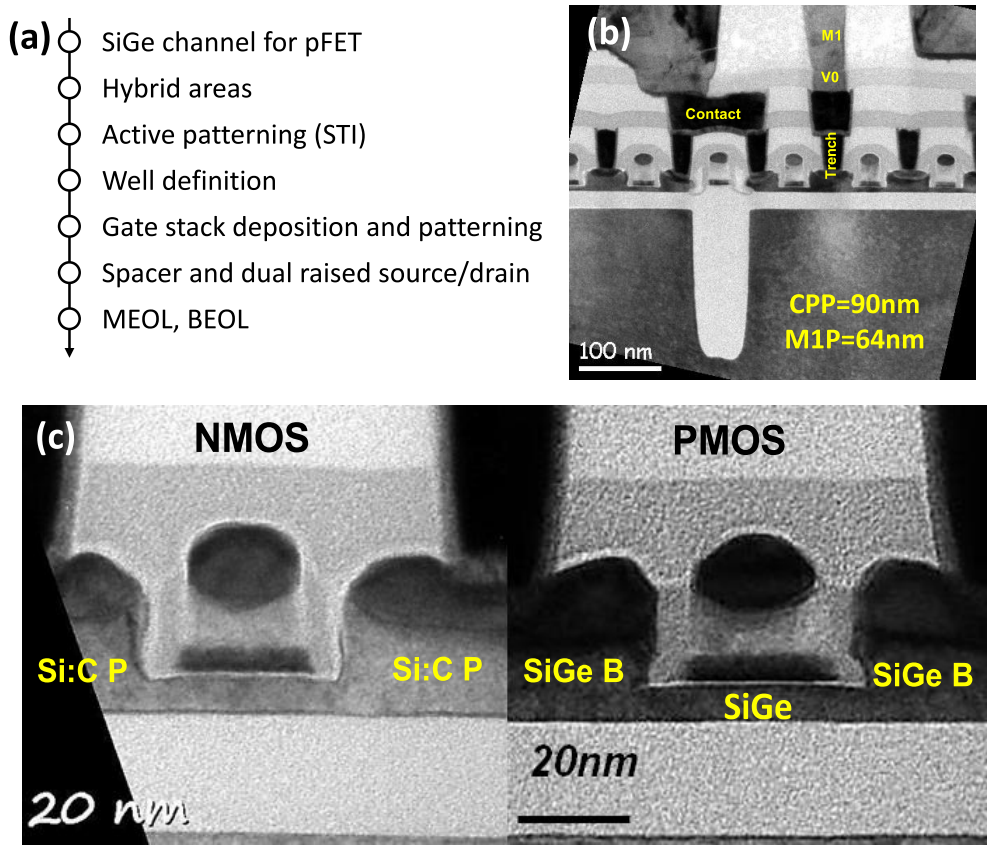


Figure 3.2: (a) Simplified process flow of 14nm FDSOI technology. SiGe channel integration for pFET is performed prior to the definition of active areas. Junctions made of dual raised source/drain are fabricated after the gate, i.e. gate-first scheme. (b) TEM image at the end of the process flow showing MEOL interconnections. Contacted Poly Pitch is 90nm and first level of metal M1 pitch is 64nm. (c) Focus on nFET and pFET nominal devices, emphasizing the dual channel and dual raised in-situ doped source and drain.

enabling bidirectional back-bias (both FBB and RBB on the same devices) as been presented in the literature [Gre12] and is discussed in section 4.3.2.

3.1.2 Integration of SiGe in FDSOI

3.1.2.a The condensation technique

The thermal oxidation of Silicon has been widely used in CMOS integrated circuits fabrication. For instance, this process has been used for the formation of the gate oxide or to create the isolation (LOCOS[1]). The famous Deal and Grove model [Dea65] accounting for the oxidation kinetics has been demonstrated to fail for oxide thicknesses below 30nm [Mas85]. As far as SiGe oxidation is concerned, it has been shown that the Germanium is not oxidized but rejected into the underlying SiGe layer [LeG89]. This phenomenon is called "snow-plow effect". The reason for a preferential oxidation

1 LOCal Oxidation of Silicon [App70].

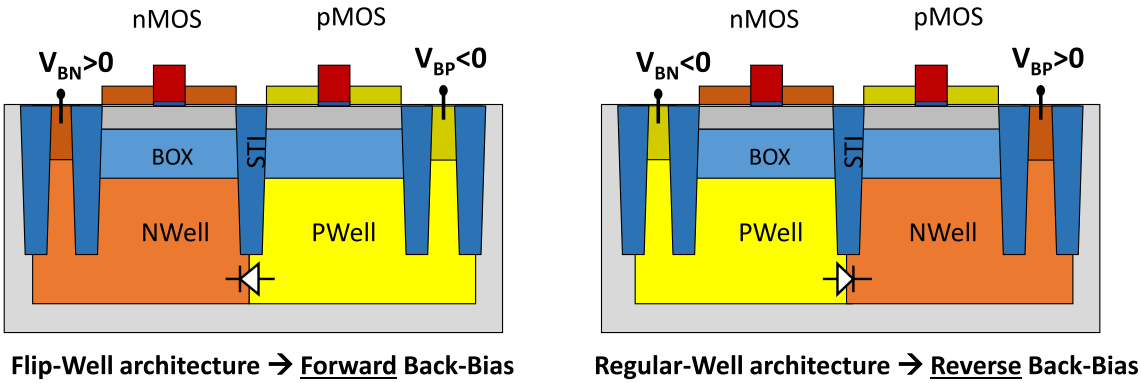


Figure 3.3: Illustration of Flip-well and Regular-well architectures. Flip-well architecture allows Forward-Back-Bias (FBB) while Regular-well allows Reverse-Back-Bias (RBB) because of the PN junction.

of Silicon rather than Germanium relies on thermodynamics consideration[1]. The accumulation of Germanium below the SiGe/oxide is governed by two mechanisms: the Ge injection and the Silicon-Germanium interdiffusion assisted by vacancies. Both mechanisms are dependent to the oxidation temperature. The so-called condensation process consists in performing a SiGe oxidation on a SOI substrate [Glo14; Gou14; Mor15; Nak03; Tez01; Vin07]. This technique consists in two steps, as described in Figure 3.4. First, a SiGe layer is grown by epitaxy on a SOI substrate. The structure is then oxidized. Because of the preferential oxidation of Silicon, the Germanium atoms are injected into the SiGe/Si. If the temperature is high enough (typically above 950°C), an interdiffusion of Silicon and Germanium happens. The Buried Oxide (BOX) acts as a diffusion barrier. The Germanium atoms are thus confined between the top and bottom oxides. This mechanism eventually leads to an increase of the Germanium concentration in the SiGe solid solution [2]. That is why the condensation technique is also referred as the "Ge-enrichment".

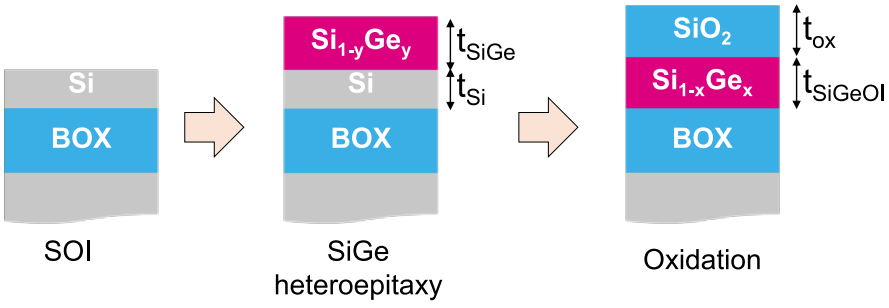


Figure 3.4: Schematic of condensation technique, constituted of two steps: a SiGe heteroepitaxy on a SOI substrate and an oxidation. Silicon atoms are preferentially oxidized. Germanium atoms are thus rejected in the underlying SiGe layer. Interdiffusion of Si and Ge finally leads to a SiGe layer directly on insulator (SiGeOI).

1 Standard Gibbs energies (at 1000K, in kJ.mol^{-1}) related to the Si-Ge-O ternary system [Bar77]:

Si	SiO_2	Ge	GeO_2	O_2
-30.39	-981.78	-44.12	-641.31	-220.93

The lower Gibbs energy value of SiO_2 indicates that it is more stable than GeO_2.

2 This happens when the equivalent thickness of Si in the starting SOI substrate has been consumed by oxidation.

The final Germanium concentration can be derived assuming Ge conservation[1]:

$$t_{SiGe} \times y = t_{SiGeOI} \times x \tag{3.1}$$

with t_{SiGe} and t_{SiGeOI} the thicknesses of the SiGe layer after epitaxy and condensation, respectively, and y and x, their respective Germanium concentrations, as illustrated in Figure 3.4. Since 2.25 volumes of SiO_2 are generated from the oxidation of one volume of Silicon, we have:

$$t_{Si} + t_{SiGe} \cdot (1 - y) = t_{SiGeOI} \cdot (1 - x) - \frac{t_{ox}}{2.25} \tag{3.2}$$

with t_{ox} the oxide thickness. The final SiGeOI thickness obtained after condensation is thus given by:

$$t_{SiGeOI} = t_{Si} + t_{SiGe} - \frac{t_{ox}}{2.25} \tag{3.3}$$

and the Germanium concentration by:

$$x = \frac{t_{SiGe} \times y}{t_{Si} + t_{SiGe} - \frac{t_{ox}}{2.25}} \tag{3.4}$$

Finally, a targeted SiGeOI film can be obtained from several ways, under the condition that the SiGe epitaxy provides the right amount of Germanium.

This simple model assumes a homogeneous SiGeOI film. However, in the case of a Rapid Thermal Oxidation (RTO) performed around 950°C for instance, the Germanium diffusion is slower than the oxidation kinetics, leading to a Germanium composition gradient [Mor15; Roz17].

Below critical thickness and without assuming plastic relaxation, the compressive strain in a SiGe solid solution is directly linked to its Germanium concentration x. During the condensation process, the Germanium atoms are injected into the Silicon lattice. Because of the back interface rigidity, the SiGe lattice is only free in the out-of-plane direction. The in-plane strain $\varepsilon_{//}$ is therefore given by:

$$\varepsilon_{//} = \varepsilon_{XX} = \varepsilon_{YY} = \frac{a(Si) - a(SiGe)}{a(SiGe)} \tag{3.5}$$

with $a(Si)$ and $a(SiGe)$ the lattice parameters of relaxed Si and SiGe, respectively. The lattice parameter of $Si_{1-x}Ge_x$ according to the Germanium content x is given by:

$$a(Si_{1-x}Ge_x) = 5.43105 + 0.2005x + 0.0263x^2 \tag{3.6}$$

after Dismukes [Dis64]. The out-of-plane strain ε_{ZZ} is directly linked to the in-plane strain through Poisson's ratio effect:

$$\varepsilon_{ZZ} = -2\frac{C_{13}(x)}{C_{33}(x)}\varepsilon_{//} \tag{3.7}$$

1 Loss of Germanium has been observed for highly concentrated SiGe film, close to pure Germanium [Xue14].

with $C_{ij}(x)$ the elastic constants of $Si_{1-x}Ge_x$ interpolated from those of Si and Ge using Vegard's law [Veg21]. The Figure 3.5 shows the strain and stress according to the Germanium concentration in a pseudomorphic SiGe solid solution.

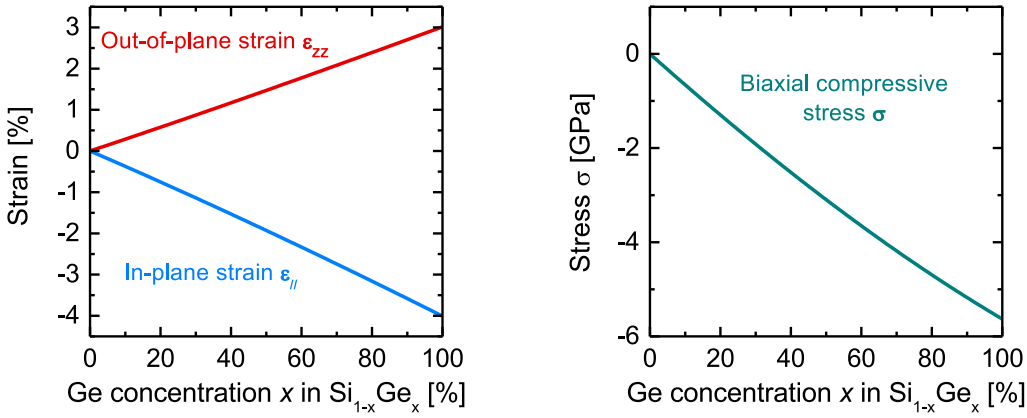


Figure 3.5: (left) In-plane and out-of-plane strains and (right) biaxial stress in pseudomorphic SiGe according to its Germanium concentration.

3.1.2.b SiGe integration in 14nm FDSOI technology

As it is the case in the 14nm FDSOI technology, the Ge-condensation technique can be performed locally [Tez05], that is to say on specific areas of the wafer. For that matter, a nitride hard mask is used to protect the areas where the SiGe epitaxy is not wanted. This is an attractive feature for co-integration purpose since the SiGeOI channel can be fabricated for pFET areas only [Che12; Gou14].

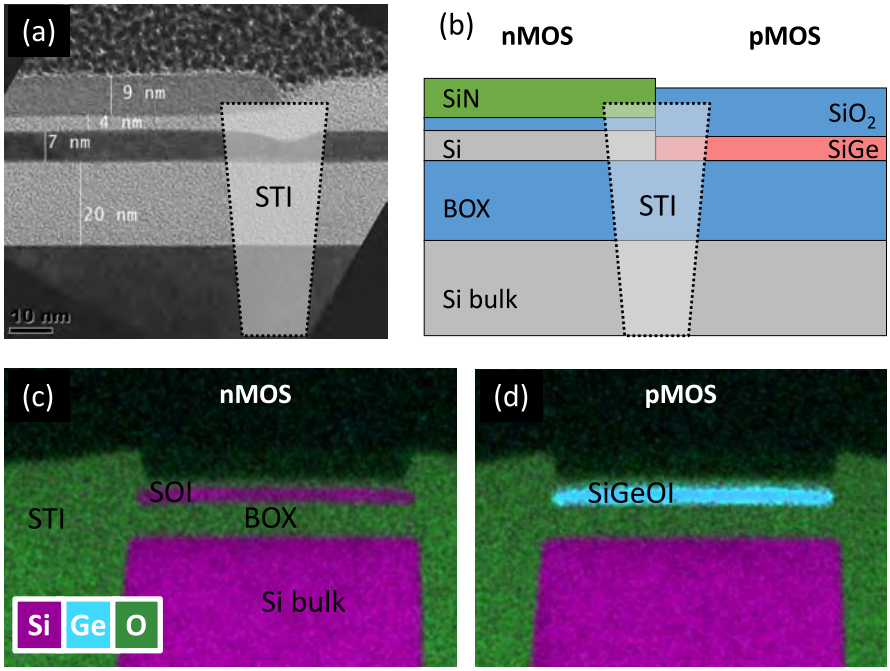


Figure 3.6: (a) TEM and (b) scheme of the SOI/SiGeOI border before STI fabrication. The nMOS area is protected by a SiN hard mask, allowing local introduction of SiGe by condensation. EDX mappings after STI in the (c) SOI and (d) SiGeOI regions.

In the process of reference (POR), the SiGe film for pFET areas is created before the active area patterning while nFET areas are protected with a nitride hard mask. This integration scheme is called "SiGe-first"[1]. Figure 3.6 (a) shows a TEM image after SiGe condensation, focusing on the nMOS/pMOS active border. The nMOS areas are protected by a SiN hard mask. This allows the SiGe to be locally integrated for pMOS areas. The SOI/SiGeOI border is then etched to form the STI. This finally yields SOI and SiGeOI active areas isolated from each other by STI, as shown on the EDX images of Figure 3.6 (c) and (d). The nMOS are then fabricated on the SOI regions and so are the pMOS on the SiGeOI ones.

1 Different integration schemes are investigated in Chapter 4.

3.2 Strain measurement, simulation and modeling in patterned SiGeOI

3.2.1 Nano-Beam Electron Diffraction measurements

In the Process Of Reference (POR), the SiGeOI is fabricated prior to the active area patterning and only in the pFETs areas. In order to define the active areas, the SiGeOI and the Si films are then patterned and isolated by STI.

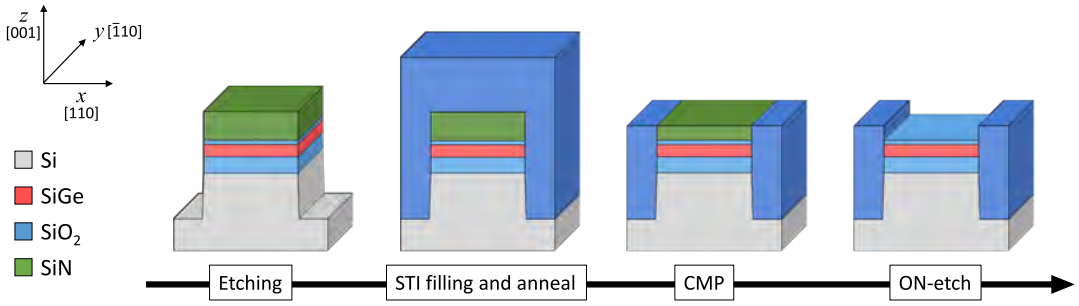


Figure 3.7: Illustration of the process steps of the STI module, defining the active area. Focus is made on pFET area with SiGe channel previously obtained by condensation technique.

The STI module, illustrated in Figure 3.7, is constituted of the following steps:

- Pad oxide deposition (TEOS of 4nm).
- SiN hard mask deposition by LPCVD. The SiN layer is 55nm thick and exhibits a tensile stress around 1.2GPa.
- Photolithography with three-layer stack.
- Deep dry etching.
- Liner oxide of 3nm obtained by Rapid Thermal Oxidation (RTO) In-Situ Steam Generation (ISSG) at 850°C.
- Shallow Trench Isolation (STI) filling.
- STI densification anneal at 1050°C during 30min.
- Chemical-Mechanical Planarization (CMP).
- Selective SiN removal by wet etching (called ON-etch for Oxide Nitride etch).

The critical step of the isolation module is the deep etching which introduces a free boundary condition that allows the compressive stress in the SiGeOI to relax. The Figure 3.8 shows the relative deformation e_{xx} profile obtained by Nano-Beam Electronic Diffraction (NBED) after etching. One has to emphasize the different notation used in this work. The use of ε means real strain, i.e. the deformation of the material (here SiGe) with respect to its relaxed lattice parameter. On the other hand, e stands for the deformation with respect to the lattice of relaxed Silicon, which is in most cases used as a reference in strain chracterization techniques. It is the case for the NBED measurements, which give the relative deformation e by comparing the diffraction pattern with the one of the underneath unstrained bulk Silicon. In the x direction (see Figure 3.7), which is here the <110> channel orientation:

$$e_{xx} = \frac{a_{SiGe,x} - a_{Si}}{a_{Si}} \tag{3.8}$$

where $a_{SiGe,x}$ is the lattice parameter of SiGe in the x direction. If $e_{xx} = 0$, the lattice of SiGe is the one of Silicon meaning that the SiGe is fully strained. However, if $e_{xx} > 0$, the SiGe lattice is larger than the one of Silicon. This indicates that the SiGe lattice parameter tends towards its unstrained value.

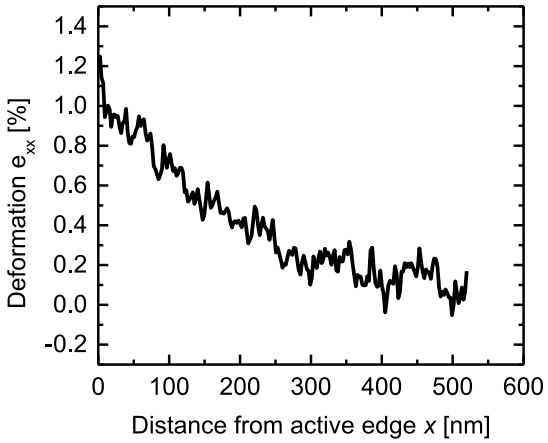


Figure 3.8: SiGeOI active area relative deformation e_{xx} profile after etching measured by NBED. The profile shows a progressive relaxation of the SiGeOI layer until it is fully strained at a distance of approximately 300nm from the edge.

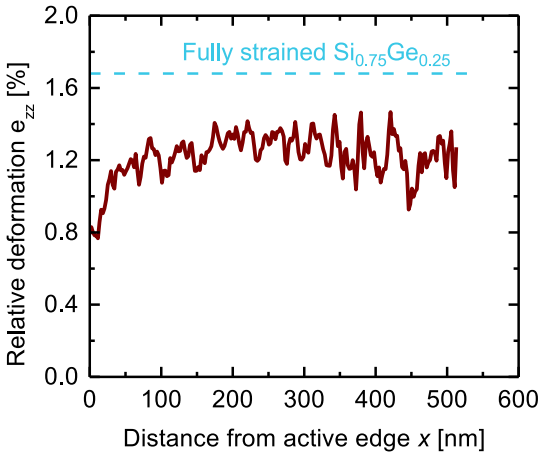


Figure 3.9: SiGeOI active area relative deformation e_{zz} profile after etching measured by NBED. The measured value is lower than expected for a pseudomoprhic $Si_{0.75}Ge_{0.25}$ (see the dashed line). This is attributed to the thin lamella effect, enabling relaxation in the y transverse direction.

The profile observed in Figure 3.8 evidences the relaxation occurring close to the active edge. At $x = 0$, i.e. at the active area edge, the relative deformation e_{xx} is about 1%. The relative deformation of a relaxed SiGe with 25% of Germanium is 0.95%, which means that the SiGe is totally relaxed at the active border. The profile shows a progressive relaxation of the SiGeOI layer until it is fully strained at a distance of approximately 300nm from the edge. Figure 3.9 shows the measurement of the relative deformation in the out-of-plane direction z. For a biaxially strained SiGe layer, the lattice in the out-of-plane direction depends on both the Germanium content and the level of in-plane strain $\varepsilon_{//}$ through Poisson's ratio effect:

$$e_{zz} = \frac{a_{SiGe,z} - a_{Si}}{a_{Si}} \tag{3.9}$$

$$a_{SiGe,z} = (1 + \varepsilon_{zz}) a_{SiGe,rel} = \left(1 - 2\frac{C_{13}}{C_{33}}\varepsilon_{//}\right) a_{SiGe,rel} \tag{3.10}$$

where $a_{SiGe,rel}$ is the lattice parameter of a relaxed SiGe, depending only on the Ge content (see Equation 3.6). In the case of a pseudomorphic SiGe layer with 25% of Germanium, $\varepsilon_{//}$=0.95% and e_{zz} is theoretically 1.68%. The value measured is significantly lower, around 1.3%. This can be explained by the effect of thin lamella: the sample must be thin enough in order to measure the deformation by NBED technique. The lamella, which is prepared by FIB (Focused Ion Beam), is usually thinner than 100nm and thus suffers from lateral relaxation. The value of 1.3% is consistent

with a relaxed SiGe in the y direction. The introduction of 25% of Ge is responsible for 0.94% of lattice change with respect to Si. In a biaxial configuration, the change in the z direction from Poisson's effect is 0.74%, which leads to $e_{zz} = 1.68\%$. Considering only half of Poisson's ratio (relaxation only in the lamella thickness, i.e. the y direction) leads to $e_{zz} \approx 0.95 + \frac{0.74}{2} \approx 1.3\%$.

The relaxation profile measured by NBED is consistent with Dark Field Electron Hologrpahy (DFEH) discussed in the work of Victor Boureau [Bou16b]. Figure 3.10 shows the relaxation profile obtained after etching of the SiGeOI film. The strain relaxes over a distance of approximately 300nm, as for NBED measurements of Figure 3.8.

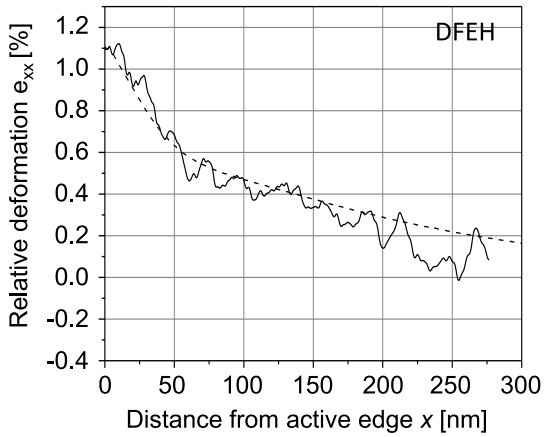


Figure 3.10: SiGeOI active area relative deformation e_{xx} profile measured by DFEH after etching. Courtesy of Victor Boureau [Bou16b].

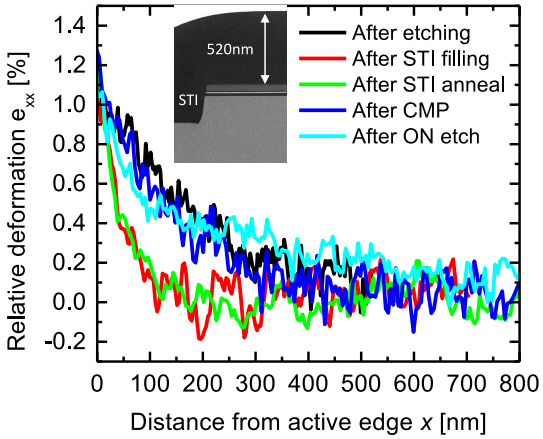


Figure 3.11: SiGeOI active area relative deformation e_{xx} profile measured by NBED after each process step of the STI module. Strain profile at the end of active area patterning is governed by the etching step that induces a strong relaxation. The change in profile after STI filling is attributed to a thermal stress from the thick (520nm) oxide layer on top of the structure (see TEM image after filling in inset).

The Figure 3.11 shows the NBED measurements of relative deformation e_{xx} after different process steps of the isolation module. The STI filling is responsible for a change in the relaxation profile, reducing the relaxation distance down to approximately 200nm, corresponding to an additional compression effect. The densification anneal does not change the deformation profile. After CMP, the profile obtained after etching is recovered. This suggests that the change of profile due to the STI filling can be explained by a thermal stress[1] induced by the thick oxide layer (520nm, see inset of Figure 3.11). Finally, after the removal of the nitride layer by selective wet etching (ON etch), the profile is not significantly different from the one after etching. The SiN deposited by LPCVD exhibits an intrinsic tensile stress of around 1.2GPa. Removing this stressed layer could change the strain configuration in the underneath SiGe layer. Nevertheless, the boundary conditions are not free when it is removed since the STI is present. The STI acts as a buffer, preventing further relaxation.

In conclusion, the main contributor for the strain profile on the active area edge is the etching step,

1 Stress from Coefficient of Thermal Expansion (CTE) mismatch

which introduces a free boundary condition enabling the relaxation.

3.2.2 Mechanical simulations

We performed Finite Element Method (FEM) mechanical simulations using COMSOL [COM12] software to confront with the NBED measurements.

3.2.2.a Hypotheses and model

The FEM mechanical simulations with COMSOL software have been performed using the "structural mechanics" module. The considered structure is in 2D (xz plan) under the plane-strain approximation, i.e. infinite structure in the y direction. Although this approximation is not valid because of the thin lamella, as discussed in the previous section, we focus here only on the x direction. The relative deformation e_{xx} is not significantly impacted by the transverse stress relaxation in the y direction, especially for <110> orientation[1]. We only consider the elastic domain as we focus on the etching step, which is performed at low temperature[2]. Only half of the structure is simulated for symmetry reasons (at $x = L_{act}/2$, the displacement in the x direction is not allowed). At $x = 0$, a free boundary condition is introduced. The material mechanical properties used for the simulations are given in Table 3.1.

Table 3.1: Material mechanical properties used for FEM simulation.

Material	Young's Modulus	Poisson's ratio
$Si_{0.75}Ge_{0.25}$	Anisotropic material: ${C_{ij}}^{<110>}$ with Vegard's law [GPa] $\begin{pmatrix} 184.6 & 31.8 & 60.0 & 0 & 0 & 0 \\ 31.8 & 184.6 & 60.0 & 0 & 0 & 0 \\ 60.0 & 60.0 & 156.5 & 0 & 0 & 0 \\ 0 & 0 & 0 & 76.4 & 0 & 0 \\ 0 & 0 & 0 & 0 & 76.4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 48.2 \end{pmatrix}$	
Si	Anisotropic material: ${C_{ij}}^{<110>}$ [GPa] $\begin{pmatrix} 194.5 & 35.3 & 63.9 & 0 & 0 & 0 \\ 35.3 & 194.5 & 63.9 & 0 & 0 & 0 \\ 63.9 & 63.9 & 165.8 & 0 & 0 & 0 \\ 0 & 0 & 0 & 79.6 & 0 & 0 \\ 0 & 0 & 0 & 0 & 79.6 & 0 \\ 0 & 0 & 0 & 0 & 0 & 51.0 \end{pmatrix}$	
SiN	280 GPa	0.23
Oxide	70 GPa	0.17

1 Poisson's ratio ${\nu_{xy}}^{<110>} = 0.06$, please refer to section 1.3.1.
2 SiO_2 creeping does not happen below ≈ 960°C [Eer77].

In order to model a pseudomorphic SiGe with COMSOL, the "initial strain and stress" option is used. To properly take into account the intrinsic strain of the SiGe layer, initial stress must be set to 0 while initial strain in all 3 directions (x, y and z) must be set to $-\varepsilon_{//}(x_{Ge})$. Actually, it can be seen as an initial force coming from the lattice mismatch between SiGe and Si driving the SiGe to expand. Without considering edge effects, the SiGe is only free in the z direction, it will thus expand in this direction. This way, the pseudomorphic SiGe exhibits a compressive in-plane strain. The out-of-plane deformation e_{zz} obtained with this method is exactly the one given by the theory, confirming the validity of this approach.

3.2.2.b Results and discussion

The Figure 3.12 shows the intrinsic longitudinal strain ε_{xx} mapping after etching, with a focus on the first 50nm close to the free edge (at $x = 0$). In this simulation, the SiN layer is considered unstressed. The compressive strain close to the edge is lower than the initial strain (lighter blue) due to the free boundary condition. The strain is extracted along the white dashed arrow, in the middle of the SiGe layer and reported in Figure 3.13.

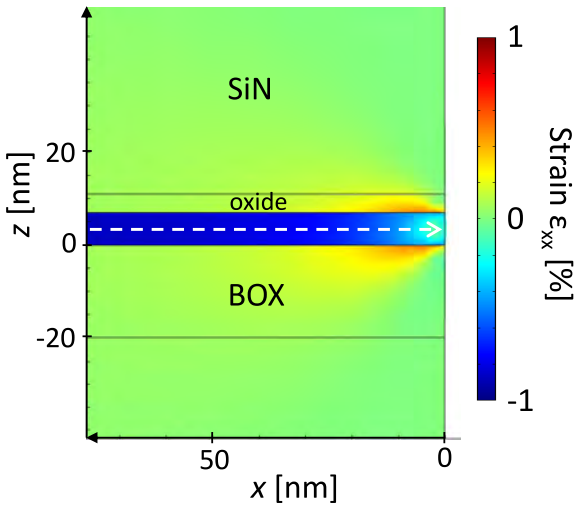


Figure 3.12: Strain ε_{xx} mapping of SiGeOI active area after patterning (with focus on the 50nm close to right side). The 55nm-thick SiN layer is considered unstressed. Strain relaxaton because of free boundary condition is evidenced. The strain profiles are extracted in the middle of the SiGe layer (represented by the white arrow).

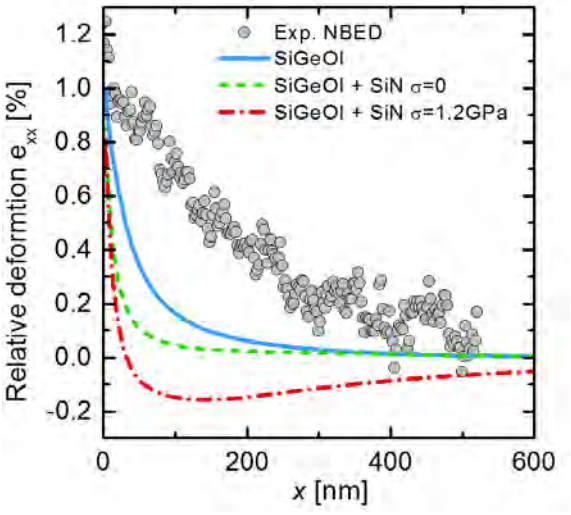


Figure 3.13: SiGeOI active area relative deformation e_{xx} profile after etching measured by NBED compared to elastic simulations considering different stacks. The strong relaxation observed experimentally is not consistent with simulations. Besides, the SiN hard mask should prevent the relaxation, especially if it is intrinsically tensely stressed.

The NBED results obtained after etching are compared with three different simulation cases: without any SiN layer, with an unstressed SiN layer and with a tensely stressed SiN layer at σ=1.2GPa. For all three cases, the experimental profile shows a larger relaxation than predicted from simulation. This has been evidenced in the work of Victor Boureau [Bou16b]. In addition, the SiN layer should help maintaining the compressive strain in the SiGe layer, especially if the said SiN layer is tensely

strained[1]. Since the etching step is performed at low temperature, the oxide creeping can not be incriminated to explain the over relaxation.

As a conclusion, our elastic simulations do not explain the measured SiGeOI lateral stress relaxation. A physical mechanism is missing in the simulation hypotheses.

3.2.3 Stress relaxation compact modeling

In this section, an analytic model of stress relaxation is proposed in order to reproduce the lateral stress relaxation observed on patterned SiGeOI. This model is later used for reproducing the layout effects of SiGeOI channel transistors (section 3.4).

3.2.3.a Theoretical approach: Hu's model

The problem of stress distribution in a patterned thin film has been investigated by [Hu79; Hu91], detailed in Appendix A. The structure considered consists in a heteroepitaxial thin film on a bulk substrate. The initial stress in the film is σ_0. The thickness of the substrate is considered as infinite compared to the one of the film h. The etching configuration is a mesa etching, i.e. only the stressed thin film is etched, at $x = 0$. The free boundary condition introduced by the mesa etching gives rise to a non balanced force. This will cause the film to move and drag the underneath substrate, generating a stress field in the latter and relaxing the stress in the film. Hu's model is based on Flamant's problem and solution [Fla92]. It is detailed in Appendix A. The stress in the film is given by :

$$\sigma_f(x) = \sigma_0 - \frac{2h}{\pi K}\int_0^{\infty} \frac{d\sigma_f(u)}{du}\frac{1}{x-u}du \tag{3.11}$$

where K is the relative rigidity factor, given by:

$$K = \frac{E_{sub}\left(1-{\nu_f}^2\right)}{E_f\left(1-{\nu_{sub}}^2\right)} \tag{3.12}$$

The Figure 3.14 shows the normalized stress profile in a patterned 7nm-thick SiGe directly on a 20nm-thick BOX obtained by FEM simulations (section 3.2.2) and compared with Hu's model. The simulated profile is rather consistent with a rigidity factor K between 0.2 and 0.5 (i.e. the film is more rigid than the substrate by a factor between 2 and 5). Hu's model profile is however not perfectly in agreement with the simulation. This is due to two effects. First, the substrate is not constituted of only one material. It features a SiO_2 layer whose rigidity is lower than bulk Silicon (E_{SiO_2}=70GPa *vs.* ${E_{Si}}^{<110>}$=169GPa). Secondly, the etching configuration is not mesa, but a deep trench in the substrate (≈200nm depth). This allows a higher expansion of the underneath substrate.

1 This effect is exploited by the so-called "BOX-creep" technique. It aims at generating strain into the SOI by the means of an anneal at high temperature allowing the BOX to creep and the SiN elastic energy to relax. This technique is discussed in section 5.2.

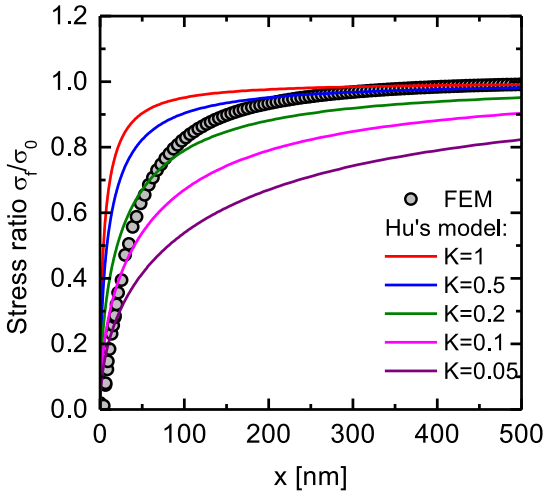


Figure 3.14: Hu's model compared to simulation of a patterned SiGeOI layer with deep trenches. The model does not perfectly reproduces the simulation because of both the impact of the BOX and the deep trenches etching (and not mesa).

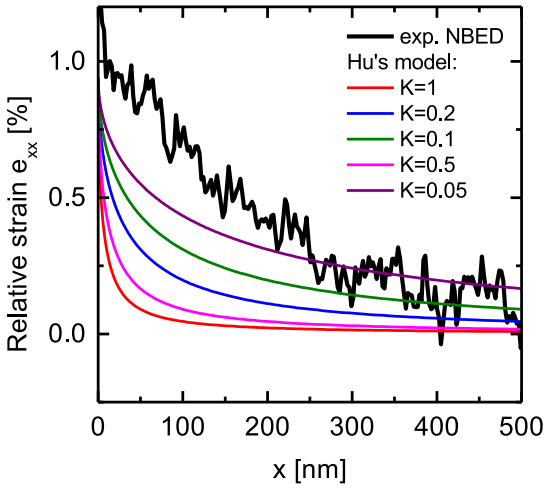


Figure 3.15: Hu's model compared to NBED profile of a patterned SiGeOI. A rigidity factor lower than K=0.05 (i.e. SiGe 20 times more rigid than the substrate) is needed to fit the experimental data. This reinforces the fact that the relaxation profile can not be explained by purely elastic models.

The Figure 3.14 compares the strain profile in the patterned SiGeOI close to the edge measured by NBED (same as in Figure 3.8) with the profile obtained from Hu's model. The strong relaxation observed experimentally would result in a rigidity factor lower than K=0.05. This emphasizes the findings of section 3.2 stating that the relaxation of patterned SiGeOI can not be explained by purely elastic models.

Hu's model has the strong advantage of being physically based, making this approach fully predictive. However, it is valid under specific assumptions:

- The film is patterned by a mesa etching.
- The film thickness is considered small compared to the substrate and the non-uniformity of the stress field in its thickness is not taken into account.
- The substrate and the film are perfectly adherent.

Despite these assumptions, the equation 3.11 has no analytic form and must be solved numerically. Besides, taking into account two edges with Hu's model and considering the principle of superposition fails to satisfy the condition $\sigma_f = 0$ on both edges, as discussed in [Hsu00; Jai95]. For these reasons, deriving a physical model for patterned SiGeOI deeply etched into the substrate with such an approach might appear out-of-touch. The relaxation observed experimentally is anyhow not consistent with elastic simulations. That's why we have used an empirical model to describe the stress relaxation occurring in patterned SiGeOI.

3.2.3.b Empirical approach: stress from SiGe channel

In this section, an empirical model of stress relaxation is presented. This model is then used in section 3.4.3 to reproduce the pFETs from 14nm FDSOI technology electrical parameter dependence

with layout.
First, the initial level of stress σ_0 on a heteroepitaxial SiGe layer of Germanium concentration x_{Ge} is given by:

$$\sigma_0 = \left(C_{11}(x_{Ge}) + C_{12}(x_{Ge}) - 2\frac{C_{12}(x_{Ge})}{C_{11}(x_{Ge})} \right) \varepsilon_{//} \tag{3.13}$$

where the elastic constants C_{ij} are deduced from the one of Silicon and Germanium using Vegard's law [Veg21]:

$$C_{ij}(x_{Ge}) = C_{ij}(Si) + x_{Ge}\big(C_{ij}(Ge) - C_{ij}(Si)\big) \tag{3.14}$$

and the in-plane strain $\varepsilon_{//}$ is given by [Dis64]:

$$\varepsilon_{//} = \frac{a_{Si} - a_{SiGe}}{a_{SiGe}} \tag{3.15}$$

with

$$a_{SiGe} = a_{Si} + 0.2005 x_{Ge} + 0.0263 {x_{Ge}}^2, \; a_{Si} = 5.43105 \tag{3.16}$$

Since the edge relaxation model from Hu ([Hu91] presented in 3.2.3.a) is not analytical, empirical forms have been proposed [Fis94; Lou03]. The model we propose uses a simple exponential decay with only one parameter, the typical relaxation length λ. The relaxation considering the impact of only one edge is given by $f_{relax,1}$:

$$f_{relax,1}(x) = 1 - \exp\left(-\frac{x}{\lambda}\right) \tag{3.17}$$

where x is the distance from the active edge. The effect of two edges is taken into account as follows:

$$f_{relax}(x, L_{act}) = f_{relax,1}(x) + f_{relax,1}(L_{act} - x) - f_{relax,1}(L_{act}) \tag{3.18}$$

where L_{act} is the active area length. This way, the condition $f = 0$ is respected for both edges. This explicitly gives:

$$f_{relax}(x) = 1 - \exp\left(-\frac{x}{\lambda}\right) - \exp\left(-\frac{L_{act} - x}{\lambda}\right) + \exp\left(-\frac{L_{act}}{\lambda}\right) \tag{3.19}$$

The stress σ at a given position x is thus given by:

$$\sigma(x,L_{act}) = \sigma_0(x_{Ge}) \cdot f_{relax}(x,L_{act}) \tag{3.20}$$

The mean stress $< \sigma >$ is derived by the integrating along the active length:

$$< \sigma(L_{act}) >= \sigma_0(x_{Ge}) \cdot \frac{1}{L_{act}} \int_0^{L_{act}} f_{relax}(x)dx \tag{3.21}$$

which leads to:

$$< \sigma(L_{act}) >= \sigma_0(x_{Ge}) \left(1 - \frac{2\lambda}{L_{act}} + \exp\left(-\frac{L_{act}}{\lambda}\right)\left(1 + \frac{2\lambda}{L_{act}}\right)\right) \tag{3.22}$$

Our model differs from the one used in UTSOI [Poi15] compact model[1]. We used a different model for two reasons. First, the model used in UTSOI does not satisfy $f(x = 0) = f(x = L_{act}) = 0$. Secondly, we use the relaxation model in both longitudinal and transverse directions, while the relaxation function is only used for the longitudinal effect in UTSOI. Yet the effect in the transverse direction requires an integration in order to have the mean stress. It should also be noted than in the UTSOI version used for 14nm FDSOI, this model is directly applied on electrical parameters, while we use our model to describe the stress profile. The link between stress and electrical parameters is made in a second step (section 3.4.1).

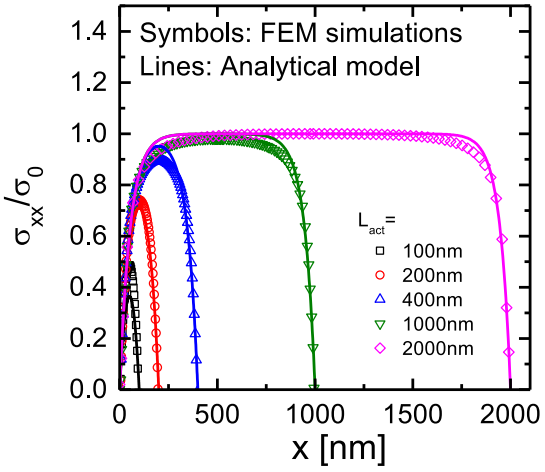


Figure 3.16: Normalized stress along patterned SiGeOI of various active lengths given by FEM simulations and compared to the analytical model of Equation 3.19 using $\lambda = 54$nm.

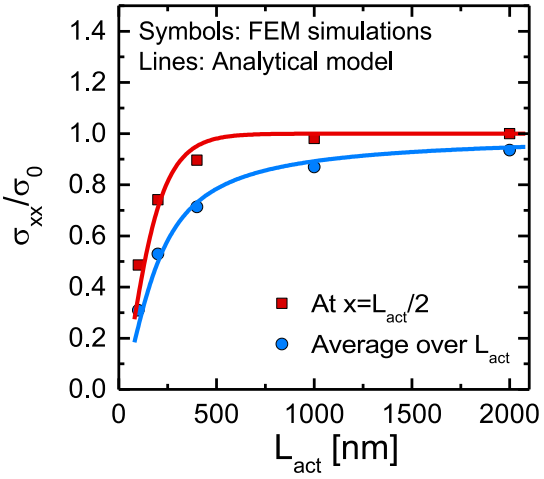


Figure 3.17: Patterned SiGeOI normalized stress at the center (i.e. at $x = L_{act}/2$) and mean stress given by FEM simulations and compared to the analytical model of Equation 3.19 using $\lambda = 54$nm. The analytical model enables to properly reproduce the impact of the relaxation on two edges.

Figures 3.16 and 3.17 compare the empirical analytical model with results obtained by mechanical simulations (see section 3.2.2). The normalized stress profiles are shown in Figure 3.16 for different active lengths. The two-edge proximity effect is well accounted for. This is highlighted on Figure 3.17, which compares the normalized stress from the model and the simulation according to the active length. Both the average stress and the stress in the middle of the active area are considered. The layout effect induced by lateral stress relaxation are well reproduced using only one fitting parameter,

1 The model used in UTSOI compact model is given by:

$$f(x,L_{act}) = \left[\frac{2}{\left(1 - \exp\left(\frac{-x}{\lambda}\right)\right)^{-\alpha} + \left(1 - \exp\left(-\frac{L_{act} - x}{\lambda}\right)\right)^{-\alpha}}\right]^{1/\alpha} \tag{3.23}$$

the typical relaxation length λ. In the case of a patterned 6nm-thick SiGeOI, the elastic relaxation predicted by simulation is well modeled using $\lambda = 54$nm.

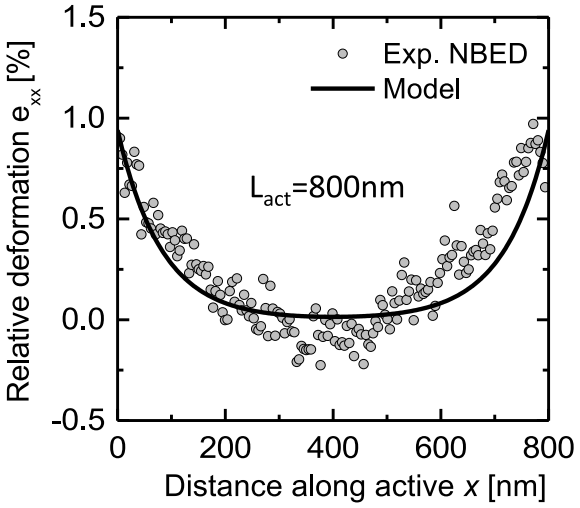


Figure 3.18: Relative deformation after etching from NBED measurment and analytical model for an active length of 800nm. The model well reproduces the experimental data assuming a typical relaxation length $\lambda = 84$nm.

The Figure 3.18 shows the relative deformation profile on a SiGeOI of active length L_{act}=800nm, measured by NBED. The profile is confronted with the empirical model. The model being based on stress, it has been translated into relative deformation assuming a Germanium concentration of x_{Ge}=25% and considering the elastic constants. The relaxation that occurs on both edges is well reproduced by the model, assuming a typical relaxation length of $\lambda = 84$nm. Such a model allows us to describe the strain profile in different SiGeOI active areas. It will then be used to model the electrical characteristic dependence with the layout geometries in section 3.4.3.

3.2.4 µRaman measurements

In this section, we assess the patterning-induced strain relaxation by the means of µRaman spectroscopy. First, the dedicated SiGe samples fabricated to investigate the relaxation with a non-destructive method are presented. Then, the theory of SiGe strain measurement by µRaman is detailed. Especially, the methodology of strain measurement assuming a unidirectional relaxation is presented. Finally, experimental measurements and strain extraction are presented and discussed.

3.2.4.a Experimental details: samples and structures

The different fabricated SiGe samples are presented in Figure 3.19.

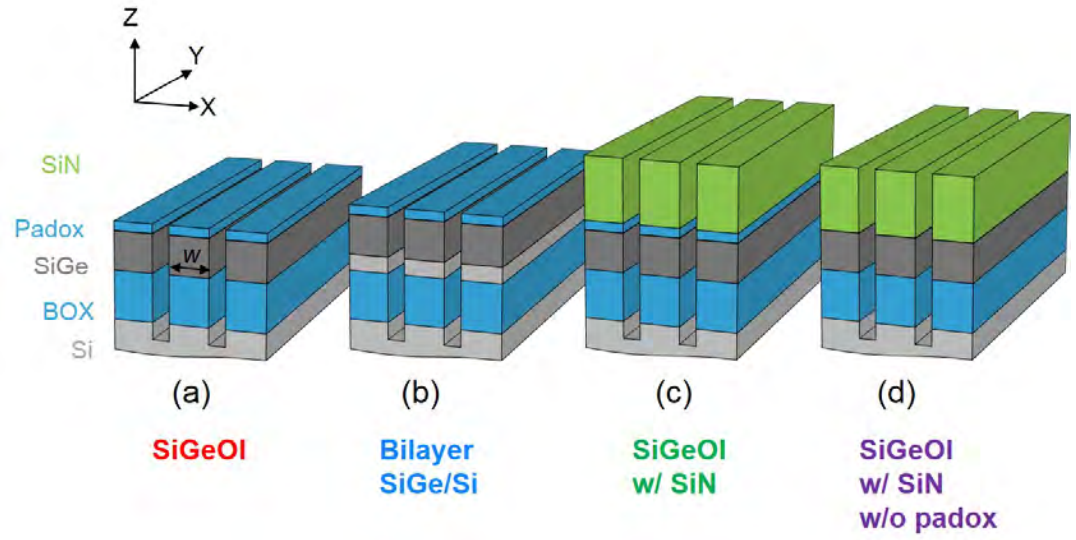


Figure 3.19: Sketches of the four different samples investigated: (a) the reference condensed SiGe directly on insulator, (b) The SiGe/Si bilayer case, i.e. without condensation, (c) reference SiGeOI before SiN hard mask removal, (d) same case as (c) but without pad oxide. The SiGe stripes of width w in the X direction [110] are 2mm long in the Y direction, which is long enough to be considered as infinite. The vertical direction Z is oriented along the [001] direction.

The reference process is as follow: starting from a SOI substrate with 20nm-thick BOX, the SiGe layer is grown by heteroepitaxy. The thickness of the deposited SiGe is 20nm with a targeted Germanium concentration of 24 at%. Then, SiGe directly on insulator is obtained by condensation at 1050°C (Rapid Thermal Oxidation), taking advantage of the preferential oxidation of Silicon over Germanium (see section 3.1.2.a). The condensation oxide is then removed by wet etching. Before the deposition of a 55nm-thick SiN hard mask by LPCVD, a 4nm-thick oxide pad is deposited. In order to achieve a uniform SiGe layer directly on insulator, an anneal of 30min at 1050°C under N2 is then performed to allow Silicon-Germanium atom interdiffusion. The SiGe is then patterned by UV lithography and a deep etching step. The SiN hard mask is then removed by selective H_3PO_4 assisted etching. This reference sample (Figure 3.19 (a): SiGeOI) is compared with samples of different integration schemes. In order to study the role of the SiN hard mask, a sample is measured prior to the SiN removal (Figure 3.19 (c): SiN/SiGeOI). Similarly, a sample without oxide pad is characterized (Figure 3.19 (d)). It is fabricated as follows. An HF-last desoxidation was used to ensure that the SiN was

deposited directly on the SiGe layer. A "bilayer" sample is also studied (Figure 3.19 (b)). The latter sample did not undergo the condensation process neither the annealing, yielding a SiGe/Si bilayer.

The mask used for patterning has been developed at LETI to investigate geometry effects. This mask, called "DIVA", embeds several structures such as squares, rectangles and lines of different sizes. In this work, µRaman measurements have been done on SiGe stripes. The stripe width varies while the length is fixed at 2mm, which can be considered as infinite.

3.2.4.b Pseudomorphic SiGe strain extraction by µRaman

The Raman spectoscopy is a non-destructive technique based on the interaction between light and matter. The interaction of the photons with the sample results in elastic scattering, i.e. Rayleigh scattering, and inelastic scattering, i.e. Stokes and anti-Stokes scattering. Especially, the Raman spectroscopy studies the Stokes scattering corresponding to a wavelength shifted towards lower wavelength. Such an inelastic scattering consists in an excitation of an electron into a virtual state followed by a relaxation into an excited state. As a result, the photon loses part of its energy. The evidenced vibration mode is directly related to the sample chemical bonds. The µRaman spectroscopy consists in using a monochromatic laser source and allows to achieve spatial resolution of around 500nm.

The measurement of strain by the means of µRaman spectroscopy is based on Stokes scattering frequency peak shift of the sample with respect to an unstrained reference. The µRaman frequency shift is thus sensitive to the out-of-plane relative deformation with respect to the lattice of Silicon (and not w.r.t. relaxed SiGe), which is defined as:

$$e_{ZZ} = \frac{(1+\varepsilon_{ZZ})\,a(SiGe) - a(Si)}{a(Si)} \tag{3.24}$$

In a biaxially strained pseudomorphic SiGe, ε_{ZZ} is directly linked to the in-plane strain $\varepsilon_{//}$ by Poisson's ratio (see section 1.3.1):

$$\varepsilon_{ZZ} = -2\frac{C_{12}(x)}{C_{11}(x)}\varepsilon_{//} \tag{3.25}$$

with $C_{ij}(x)$ the elastic constants of $Si_{1-x}Ge_x$ interpolated from those of Si and Ge using Vegard's law [Veg21]. The Si-Si Raman peak frequency shift is finally expressed as:

$$\Delta\omega_{SiSi} = \frac{1}{2\omega_0}\cdot p \cdot e_{ZZ} \tag{3.26}$$

with ω_0 the peak position of Silicon and p the value of deformation potential ($p = -1.85{\omega_0}^2$) [Ana90; Wol96; Wol99; Won05]. As a result, the shift associated to a biaxially strained pseudomorphic SiGe film only depends on its Germanium concentration. The theoretical Raman shift according to the Germanium concentration is presented in Figure 3.20. A good approximation of a linear relationship can be given by $\Delta\omega_{SiSi}(x) = -33.3x$ for Germanium concentration below 50%. Experimental measurements in literature show a good agreement with this theoretical sensitivity [Rou14; Sch05].

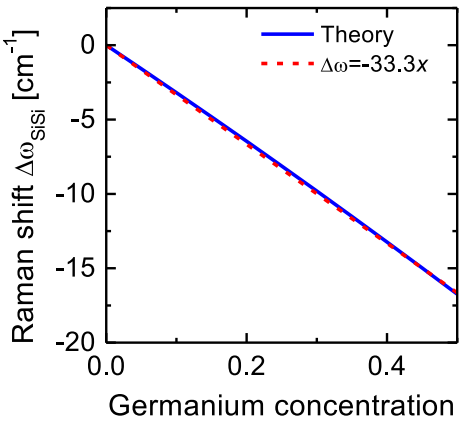


Figure 3.20: Raman frequency shift according to the Germanium concentration in a fully strained SiGe layer. Good approximation is given by $\Delta\omega_{SiSi}$=-33.3x_{Ge} for x_{Ge} below 0.5.

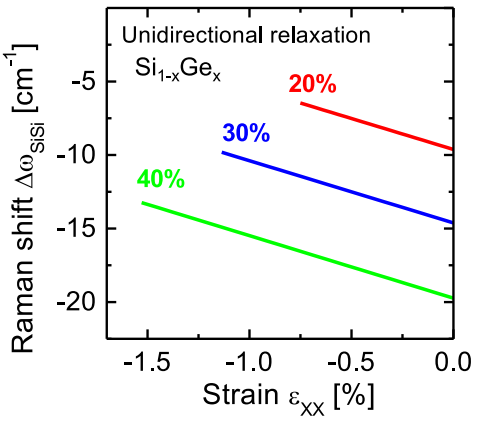


Figure 3.21: Raman frequency shift according to the level of strain in the X direction. The strain in the Y direction is assumed to be fully maintained since the SiGe stripes are considered infinite. The Raman frequency shift depends both on the level of strain in the X direction and on the Germanium concentration.

Raman measurements on a wide area, considered as similar to a blanket wafer configuration, thus enable the Germanium concentration to be extracted.

3.2.4.c Unidirectional strain relaxation extraction by μRaman

In order to assess the relaxation by the means of μRaman characterizations, measurements are performed on SiGe stripes. In our case, the X, Y, Z, directions are along the [110], [1$\bar{1}$0], [001] directions, respectively, as shown in Figure 3.19. The patterning of the SiGe in one direction (parallel to Y direction) introduces a free boundary condition that is responsible for strain relaxation. The biaxial configuration is no longer valid. By investigating 2mm-long SiGe stripes in the Y direction, one can assume that the strain is fully maintained in this direction (plane-strain configuration). On the other hand, the strain in the X direction is free to partially relax.

The relative deformations are thus given by:

$$\begin{pmatrix} e_{XX} \\ e_{YY} \\ e_{ZZ} \end{pmatrix} = \begin{pmatrix} (1+\varepsilon_{XX})\,\dfrac{a(SiGe)}{a(Si)} - 1 \\ (1+\varepsilon_{//})\,\dfrac{a(SiGe)}{a(Si)} - 1 \\ \left(-\dfrac{C_{12}}{C_{11}}\left(\varepsilon_{XX}+\varepsilon_{//}\right)+1\right)\dfrac{a(SiGe)}{a(Si)} - 1 \end{pmatrix} \tag{3.27}$$

With $\varepsilon_{//}$ the initial strain before patterning. The Raman shift is given by [Ana90; Wol99; Won05]:

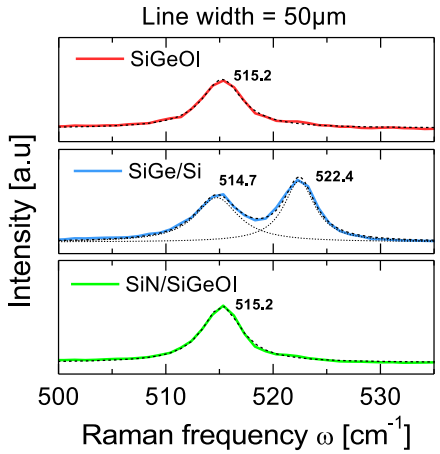
$$\Delta\omega_{SiSi} = \frac{1}{2\omega_0}\cdot\left[q\cdot(e_{XX}+e_{YY})+p\cdot e_{ZZ}\right] \tag{3.28}$$

With q and p the deformation potentials ($q=-2.31{\omega_0}^2$, $p=-1.85{\omega_0}^2$) [Ana90; Ndo13]. The Germanium concentration being formerly extracted on a wide area assuming pseudomorphic SiGe

(see section 3.2.4.b), the parameters $a(SiGe)$, C_{12}, C_{11} and $\varepsilon_{//}$ are known. As a result, the Raman shift only depends on the strain in the X direction ε_{XX}. The Raman shift according the level of strain in the X direction is shown in Figure 3.21 for several Germanium concentrations.

3.2.4.d Results

First, the Germanium concentration of the samples presented in Figure 3.19 is extracted by measuring a wide (w=50µm) stripe and assuming a pseudomorphic SiGe. The µRaman spectra are shown in Figure 3.22, focusing on the peak related to Si-Si vibration mode.



Si peak: 522.4 cm^{-1} FWHM=3.7

Sample	$\Delta\omega_{SiSi}$ [cm^{-1}]	x_{Ge} [%]	$\varepsilon_{//}$ [%]
SiGeOI	-7.2	22.2	-0.84
SiGe/Si	-7.7	23.7	-0.89
SiN/SiGeOI	-7.2	22.2	-0.84
SiN/SiGeOI (without padox)	-7.2	22.2	-0.84

Figure 3.22: (left) Raman spectra for a wide SiGe stripe of w=50µm, equivalent to blanket wafer configuration. (right) Table summarizing the in-plane strain and associated Germanium concentration extracted from the Raman frequency shift $\Delta\omega_{SiSi}$ with respect to the Si reference measured at ω_0=522.4cm^{-1} with Full Width at Half Maximum of FWHM=3.7cm^{-1}.

The unstrained-Si reference sample peak is measured at ω_0=522.4cm^{-1}. The peaks are fitted using nonlinear least-square minimization associated to a Lorentzian function. The in-plane strain and associated Germanium concentration of each sample are given in the table of Figure 3.22. The bilayer sample features a slightly higher Germanium content (23.7% *vs.* 22.2%). This is attributed to the condensation process, in which the SOI layer has not been totally oxidized. According to the Ge concentration difference, the thickness variation is estimated at approximately 1nm. Nevertheless, one can assume that this mismatch has very low impact on the mechanical behavior. It should also be emphasized that the Silicon peak in the bilayer is clearly visible, compared to SiGeOI samples. This peak is attributed to the SOI layer.

In order to assess the relaxation occurring at the edge of the stripe, µRaman scans have been performed. The µRaman spectra are measured every 200nm, the size of the spot being approximately 500nm wide.

Figure 3.23 shows the frequency shift as a function of the position from the edge x. From $\Delta\omega_{SiSi}$, the strain in the X direction, ε_{XX}, is extracted according to the methodology described in section 3.2.4.c. Both the SiGeOI and the bilayer samples show an increase of $\Delta\omega_{SiSi}$ towards the negative values, which is synonym of compressive strain reduction. Even though the level of strain decreases, the last measured point (at x=0) still exhibits a high strain (higher than 50% of the initial strain).

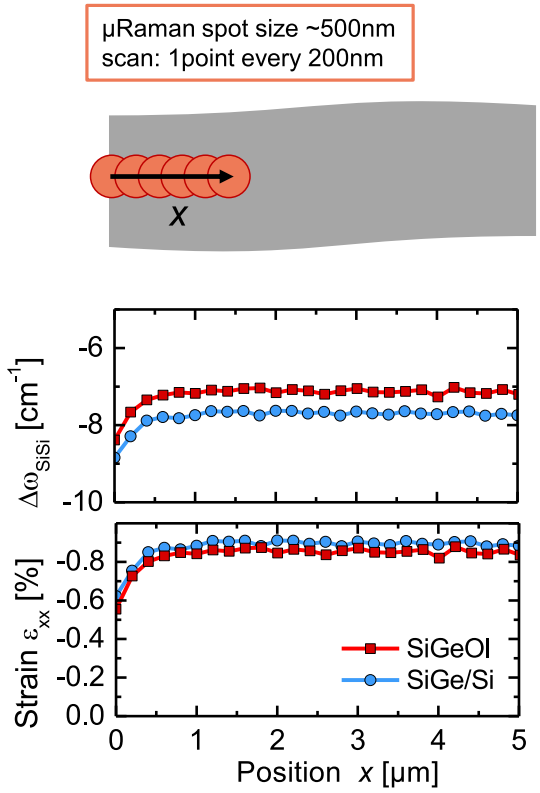


Figure 3.23: Raman scans close to the edge of the w=50µm stripe for both the SiGeOI and the bilayer samples. (top) Raman frequency shift and (bottom) extracted strain assuming relaxation in one direction. Raman spectra are measured every 200nm. The size of the spot is approximately 500nm, making it impossible to assess the relaxation profile with a sufficient resolution.

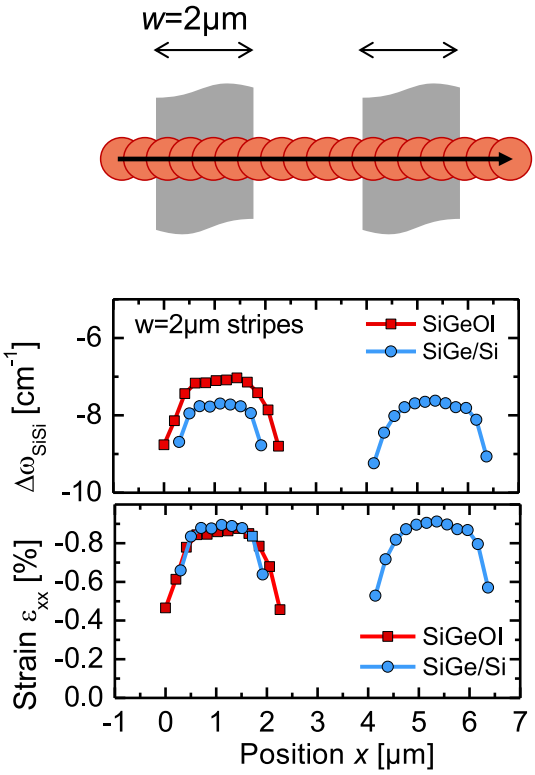


Figure 3.24: Raman scans perpendicular to the 2µm-wide stripes for both the SiGeOI and the bilayer samples. (top) Raman frequency shift and (bottom) extracted strain assuming relaxation in one direction. As for Figure 3.23, the µRaman resolution does not allow a precise measurement of the relaxation profile.

This is attributed to the large µRaman spot of approximately 500nm, which does not provide a sufficient resolution.

The same observation can be made about the scans on 2µm-wide stripes (Figure 3.24). The impacts of the two edges are visible on these scans. However, the resolution does not allow an accurate extraction of the strain profile. It is difficult to evaluate the difference between the SiGeOI and the bilayer cases based on these measurements.

A more relevant approach to assess the stress relaxation induced by the free boundary condition on the edges is to perform µRaman measurement on an array of stripes. This way, the spot covers several stripes and the frequency shift is associated to the mean strain in the stripes. We have measured stripes of width w=100nm, w=250nm and w=500nm. It should be noted that for the latter, the Raman spot covers only one stripe. The spectra are shown in Figures 3.25, 3.26 and 3.28 for the SiGeOI, the SiGe/Si bilayer and the SiN/SiGeOI sample, respectively.

For the SiGeOI sample of reference (Figure 3.25), the narrower the SiGe stripe, the lower value of SiGe Raman frequency peak. That is to say the frequency shift with respect to the unstrained

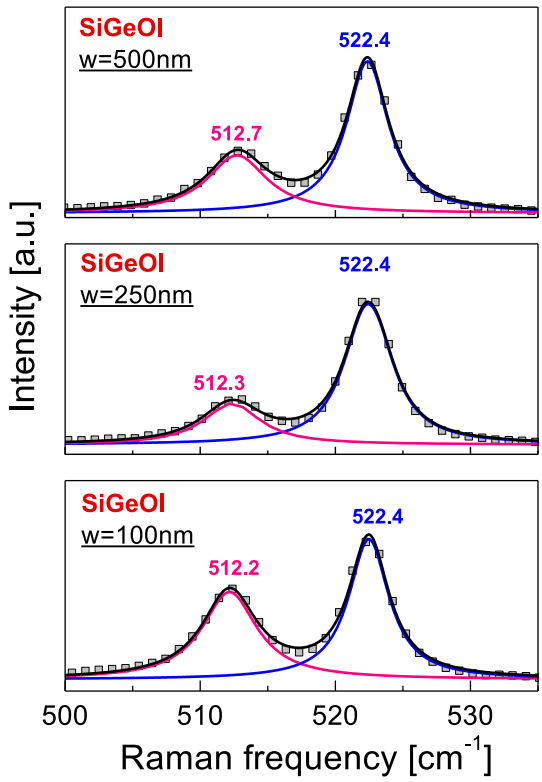


Figure 3.25: SiGeOI sample µRaman spectra for different stripe widths. The peak positions are determined using Lorentzian function fit. The pink line corresponds to the SiGe peak and the blue line to the Si bulk reference. The narrower the stripe, the lower frequency, because of the strain relaxation occurring at the edge.

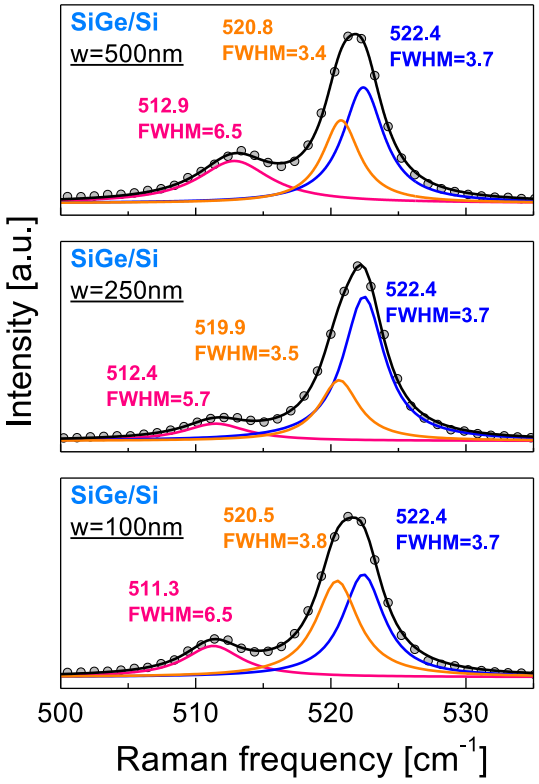


Figure 3.26: SiGe/Si bilayer sample µRaman spectra for different stripe widths. The peak positions are determined using Lorentzian function fit. Three regions are considered: the SiGe, the SOI and the Si bulk (see Figure 3.27). The pink line corresponds to the SiGe peak whose position tends toward low frequency when the stripe width is reduced, because of the strain relaxation. The Si bulk reference parameters are fixed (blue line). The SOI peak tends toward low frequency indicating a tensile strain.

references $|\Delta\omega|$ increases. This is because the relaxation of the strain close to the edge becomes more and more predominant. The mean strain in the X direction ε_{XX} thus decreases when the stripe width is reduced.

The same observation can be made on the SiGe peak of the SiGe/Si bilayer sample (Figure 3.26). For this sample, the FWHM of the Si peak appears wider than expected from an unstrained Silicon peak. The shape of the Si peak thus suggests a strain distribution. The Si peak is actually constituted of two elements: the unstrained bulk Si and the SOI layer. The Figure 3.27 shows the three considered regions for this sample: the SiGe (pink), the SOI (orange) and the bulk Si (blue). The µRaman spectrum fit is then performed considering three Lorentzian functions. The Lorentzian function parameters relating to the bulk Si, considered as the unstrained reference, are fixed as ω_0=522.4cm^{-1} and FWHM=3.7cm^{-1}.

The SiGe peak behaves similarly to the one of the SiGeOI sample. That is to say the narrower the stripe, the lower value of frequency (i.e. the higher $|\Delta\omega|$). The Si peak related to the SiGe/Si

Figure 3.27: The three considered regions for µRaman spectra fitting. The SOI layer is only present for the SiGe/Si bilayer case (orange lines of Figure 3.26.

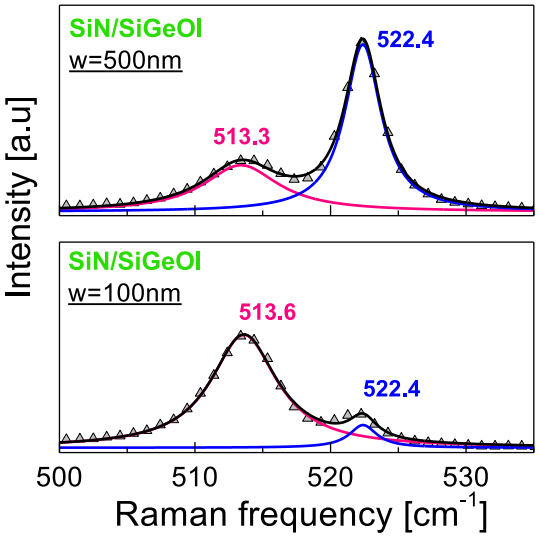


Figure 3.28: SiN/SiGeOI sample µRaman spectra for different stripe widths. The peak positions are determined using Lorentzian function fit.

bilayer, i.e. the SOI layer, also tends towards lower frequency when the stripe width is reduced. This indicates a tensile strain. Such a tensile strain is purely uniaxial, since the lattice of the SOI remains the one of unstrained Silicon in the direction parallel to the stripe (Y direction). The value of the strain in the SOI can be deduced from the $\Delta\omega_{SiSi}$ frequency shift according to:

$$\varepsilon_{XX,Si} = \frac{\Delta\omega_{SiSi}}{\frac{1}{2\,\omega_0}\cdot\left(q + p\cdot\frac{-C_{12,Si}}{C_{11,Si}}\right)} \tag{3.29}$$

The strain ε_{XX} deduced from the Raman frequency shift $\Delta\omega$ is plotted as a function of the stripe width in Figure 3.29. For w=2µm, the value is obtained by averaging over the scan of Figure 3.24. The error bars are given by an error on peak position assumed to be $\pm 0.1\text{cm}^{-1}$. The experimental data are compared with FEM simulations (see section 3.2.2), represented by the lines.

The FEM mechanical simulations predict a similar relaxation behavior for SiGeOI and the bilayer samples. The SOI layer in the bilayer case is not found to play a significant role mechanically speaking. The strain in 100nm-wide and 250nm-wide stripes is found to be almost totally relaxed for both the SiGeOI and the SiGe/Si bilayer samples. The simulated compressive strain for w=250nm stripes is however expected to be higher (around -0.5%).

For w=500nm, the strain is significantly higher in the bilayer sample. In this case, the level of strain is actually consistent with the simulation. On the other hand, the relaxation of the SiGeOI stripes is stronger than expected from the simulation. This result suggests a different behavior for the two samples. It will be discussed in section 3.2.5.

As far as SOI in the bilayer is concerned, the tensile strain experimentally extracted by µRaman measurements is consistent with simulations. As the SiGe layer relaxes, it drags the underlying SOI

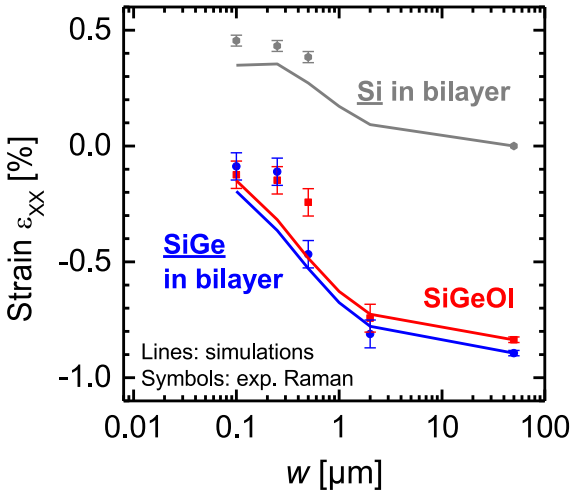


Figure 3.29: Extracted mean strain ε_{XX} according to the stripe width w for SiGeOI and SiGe/Si bilayer. The lines correspond to FEM mechanical simulations. The SiGe compressive strain decreases when the stripe width is reduced for both samples because of the relaxation on edges. The SOI of the bilayer shows an increased uniaxial tensile strain for reduced stripe widths.

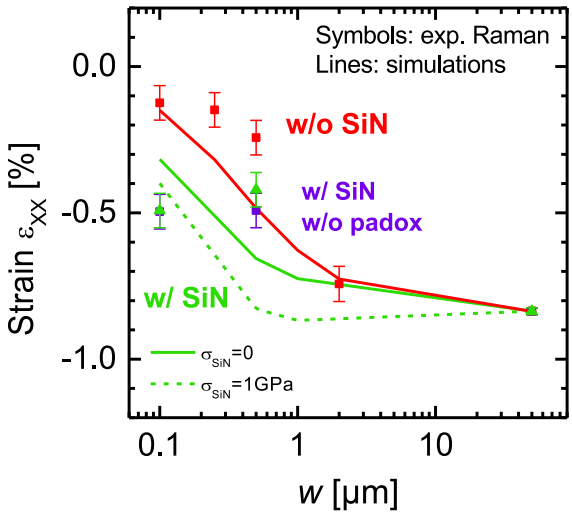


Figure 3.30: Extracted mean strain ε_{XX} according to the stripe width w for SiGeOI with and without SiN. The SiN layer enables to better maintain the compressive strain in the SiGe layer, especially for w=100nm. The lines correspond to FEM simulations assuming an unstressed (solid) and a 1GPa tensely stressed (dashed) SiN layer.

layer in tension. The more the SiGe loses its compressive strain, the more tensile strain is transferred into the SOI.

The impact of the SiN is shown in Figure 3.30. The compressive strain in the SiGe layer is better maintained for narrow stripes with the presence of the SiN layer, especially for w=100nm. This is expected from simulation since the SiN layer mechanically acts as a spring in parallel, preventing the SiGe to relax. This is even more true when considering that the SiN layer deposited by LPCVD exhibits an intrinsic tensile stress of 1GPa. Nevertheless, the strain experimentally extracted for the 500nm-wide stripe is lower than expected from simulations, like for the SiGeOI sample.

The role of the pad oxide between the SiGe and the SiN is found to be insignificant, showing same strain relaxation with or without this layer.

3.2.4.e Conclusion on µRaman measurements

In this section, a methodology to assess the patterning-induced relaxation of the stress in SiGe is presented. This methodology relies on µRaman measurements, which has the advantage of being a non-destructive physical characterization technique. Different patterned SiGe samples have been fabricated. The lateral strain relaxation in SiGeOI seems stronger than in a SiGe/Si case, even though the difference is not obvious. The role of the SiN hard mask layer is also investigated, preventing the SiGe relaxation.

3.2.5 Discussion

The strain profile measurement by NBED (and DFEH [Bou16b]) in patterned SiGeOI has evidenced a strong lateral relaxation. Such experimental strain profile is not consistent with mechanical simulations in the domain of elasticity. A possible explanation for the strong relaxation may be a weak SiGe/BOX interface that would result in a "sliding". A model of sliding interface allows the reproduction of the strain relaxation profile [Bou16b] with the help of a sliding coefficient parameter but the physical meaning of such parameter is questionable.

Different patterned SiGe samples have been assessed by µRaman, measuring stripes of varying widths. Compared to the reference condensed SiGeOI, the SiGe/Si bilayer does not show the same relaxation behavior, although the difference is not significant. In the latter bilayer sample, the SiGe/Si interface behaves as expected, since the SOI layer is found to be tensely strained when the SiGe layer relaxes, demonstrating the strain transfer. In addition, the relaxation evidenced by NBED and DFEH occurs despite the presence of the SiN hard mask layer. The SiN is not directly deposited on SiGe: a pad oxide layer is present between the SiGe and the SiN layers. This suggests a weakness of the SiGe/SiO_2 top interface, as well as the SiGe/BOX inteface. Nevertheless, µRaman measurements have demonstrated that the SiN layer plays a significant role, enabling to better maintain the strain in narrow stripes. The absence of the pad oxide does not change the picture.

We think that the over relaxation might be related to the behavior of the interface between a strained crystal and an amorphous material. However, it is impossible to incriminate the presence of Germanium at the SiGe/BOX interface. For instance, XRD measurements on strained-SOI (i.e. without Ge) have also shown an important relaxation induced by patterning [Bau09]. As a bilayer sample seems to be consistent with elastic simulations that only consider the geometry of the structure, the over relaxation could be related to the process of condensation.

In order to further investigate this relaxation, additional experiments could be carried out. It would be interesting to locally measure the strain profile in a patterned sSOI sample. This would give insights about the role of Germanium presence at the interface. In addition, measuring the strain profile in patterned SiGeOI obtained by smart-cut could incriminate the condensation process.

3.3 Stress from SiGe source/drain: measurements, simulations and modeling

3.3.1 Additional stress from SiGe source/drain in a non-patterned SiGeOI active layer

In the 14nm FDSOI technology, pFET channel is not only stressed by the use of an intrinsically strained SiGeOI but also by embedded in-situ Boron-doped SiGe source and drain. These SiGe source/drain are fabricated by epitaxy after the gate formation[1], with a Germanium concentration of 30%.

3.3.1.a NBED measurements and simulations

The relative deformation e_{xx} in the SiGeOI layer measured by NBED at the end of the process flow is shown in Figure 3.31. The studied structure consists in a long active area with several gate fingers, with a Contacted Poly Pitch (CPP) of 90nm (which is the minimum CPP of the 14nm FDSOI technology). As a first step, the measurement is performed far from the edges of the active area. The relative deformation below the gates is found to be negative $e_{xx} < 0$, meaning that the SiGeOI channel lattice parameter is smaller than the one of Silicon. The intrinsic strain in the channel is thus higher than the strain induced by the SiGeOI lattice mismatch between SiGe and Silicon. This additional strain is due to the SiGe source/drain that tend to relax, dragging the SiGeOI underneath (in the source/drain region) in tension and thus inducing a compression into the channel. The impact of Boron can be neglected as it is low compared to the one of Germanium[2].

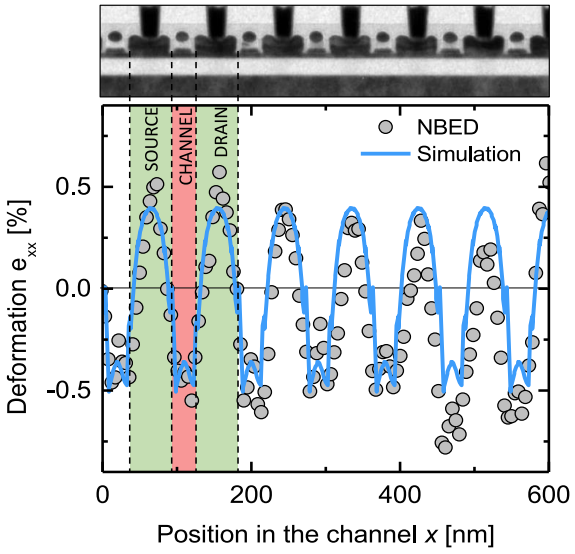


Figure 3.31: Relative deformation e_{xx} profile at the end of the process flow measured by NBED. The evidenced additional strain from SiGe source/drain is consistent with elastic simulations.

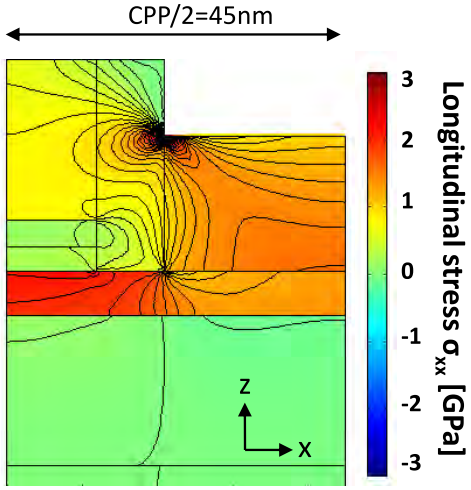


Figure 3.32: Simulated longitudinal stress σ_{xx} mapping in a pMOSFET with SiGe channel and SiGe source/drain. Only half of the structure is simulated for symmetry reasons.

1 Integration scheme called "Gate-first".

2 It is estimated that a Boron doping of 10^{20}at.cm^{-3} results in -0.06% of lattice deformation [Bou16b], which is approximately equivalent to the impact of the introduction of 1.5% Germanium.

Figure 3.32 shows the longitudinal stress mapping obtained by elastic simulations. The inherent relative deformation profile is plotted in Figure 3.31. A good agreement between the experimental result and the simulation is observed. The stress generated by SiGe source/drain is only longitudinal, which is highly beneficial for hole mobility in the <110> orientation (please refer to section 2.1.3). The global stress from the SiGeOI channel and the local stress from SiGe source/drain are additive.

3.3.1.b The influence of Germanium concentrations

The level of stress induced by SiGe source/drain is however significantly lower than the one achieved with the SiGe channel. In addition, the reduction of the CPP with the technology scaling further reduces the impact of SiGe source/drain since the volume of the strained source/drain reduces. This technique is however still relevant, especially if the Germanium concentration in the source/drain is increased[1] [Muj12; Xue14]. The Figure 3.33 shows the longitudinal stress achieved for different Germanium concentrations in the channel and in the source/drain, noted x_{Ge} and y_{Ge}, respectively. This simulation result is obtained considering the structure of the 14nm FDSOI technology with 90nm CPP (section 3.1). From this figure, we can extract the additional stress from source/drain by subtracting the stress from SiGe channel. This is represented in the Figure 3.34 as a function of the Germanium concentration y_{Ge}.

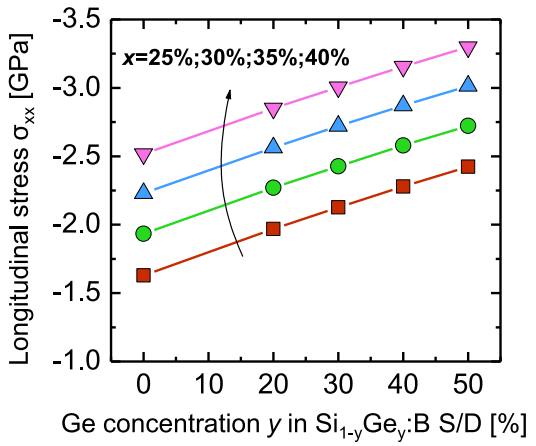


Figure 3.33: Simulated total longitudinal stress according to the Ge concentration in the source/drain y_{Ge} and for different Ge concentrations in the channel x_{Ge}. The simulation is for a non-patterned channel.

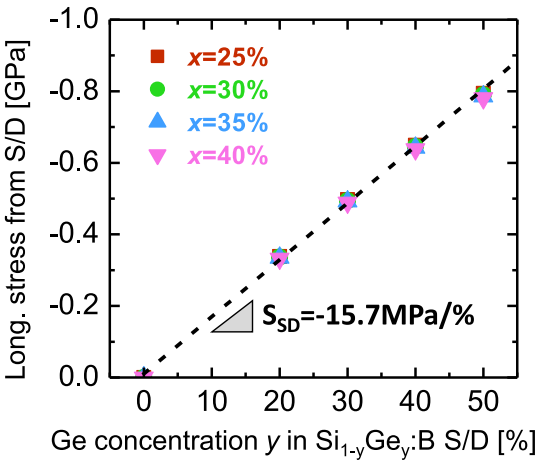


Figure 3.34: Simulated additional longitudinal stress from the source/drain only according to the Ge concentration in the source/drain and for different Ge concentrations in the channel. The additional stress related to the source/drain only depends on y_{Ge}, with sensitivity $S_{SD} = -15.7$MPa/%, because the in-plane lattice parameter of the channel (i.e. substrate) is the one of Silicon, whatever its Germanium concentration. The simulation is for a non-patterned channel.

The stress from source/drain does not depend on the Germanium concentration in the channel x_{Ge}. Although this result might appear counter-intuitive, it is actually simply explained by the fact that

1 The use of strained source/drain is also more effective for the Gate-last integration schemes, as the relaxation of source/drain is enhanced when the sacrificial gate is removed [DeS14; Idr15].

both SiGe channel and SiGe source/drain in-plane lattice parameters are the one of Silicon. As a result, the intrinsic strain in the SiGe source/drain only depends on its Germanium concentration y_{Ge}. Consequently, the stress in the channel induced by the relaxation of the SiGe source/drain does not depend on the Germanium concentration in the channel x_{Ge}. A good linearity between the additional stress induced by the SiGe source/drain and the Germanium concentration in source/drain y_{Ge} is observed with a proportionality coefficient S_{SD}=-15.7 MPa/% for the considered geometry.

3.3.2 The impact of SiGeOI relaxation on stress from source/drain

In section 3.3.1, the stress from the SiGe source/drain is investigated without considering the channel relaxation induced by the patterning, discussed in section 3.2.1. The deformation profile at the end of the process flow measured by NBED close to an active area edge (see Figure 3.35) is shown in Figure 3.36. The profile obtained after the STI module is also plotted. The impact of the SiGe source/drain is obvious, consistently with Figure 3.31. However, the closer to the active edge, the higher the level of relative deformation ($e_{xx} = 0.2\%$ under the gate the closest to the active edge *vs.* $e_{xx} = -0.3\%$ under the gates located far from the active edge). This translates the strain relaxation of the channel due to the active area etching. The three gate fingers located close to the active area edge are impacted by the relaxation.

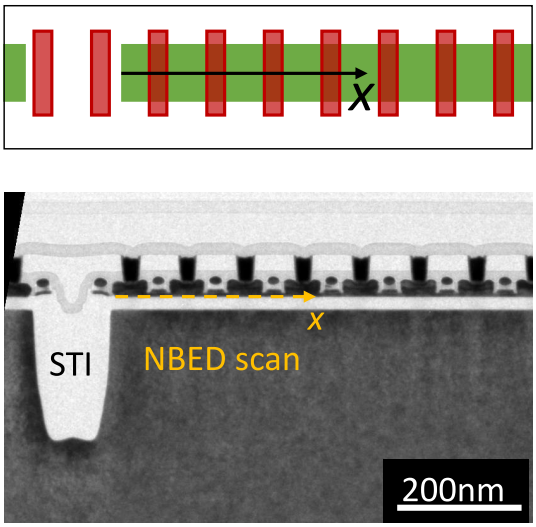


Figure 3.35: Layout and TEM image of the NBED measurement of Figure 3.36 realized after MEOL from the active edge (x=0).

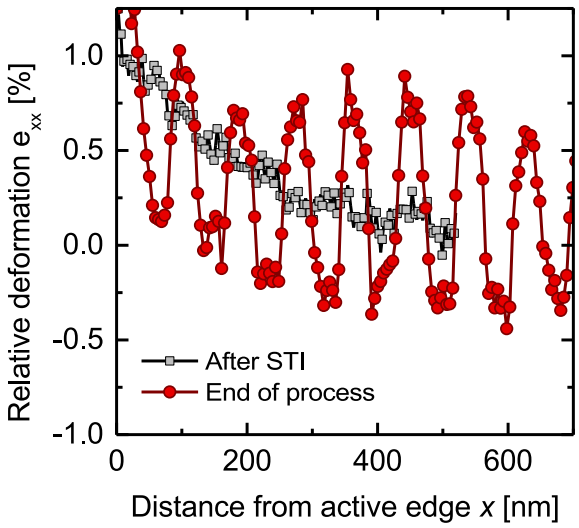


Figure 3.36: Relative deformation e_{xx} profile at the end of the process flow measured by NBED and compared with the profile after etching. Even though SiGe source/drain induces an additional compressive strain, the channels close to the active edge suffer from the relaxation occurring during the patterning.

The efficiency of the source/drain stress induced on a partially relaxed substrate is also investigated by the means of elastic simulations. In order to do so, the process must be simulated sequentially. The initial stresses and strains calculated from the previous process steps need to be properly defined using COMSOL. The so-called "dependent variables" in the solver must also been set according to the previous steps.

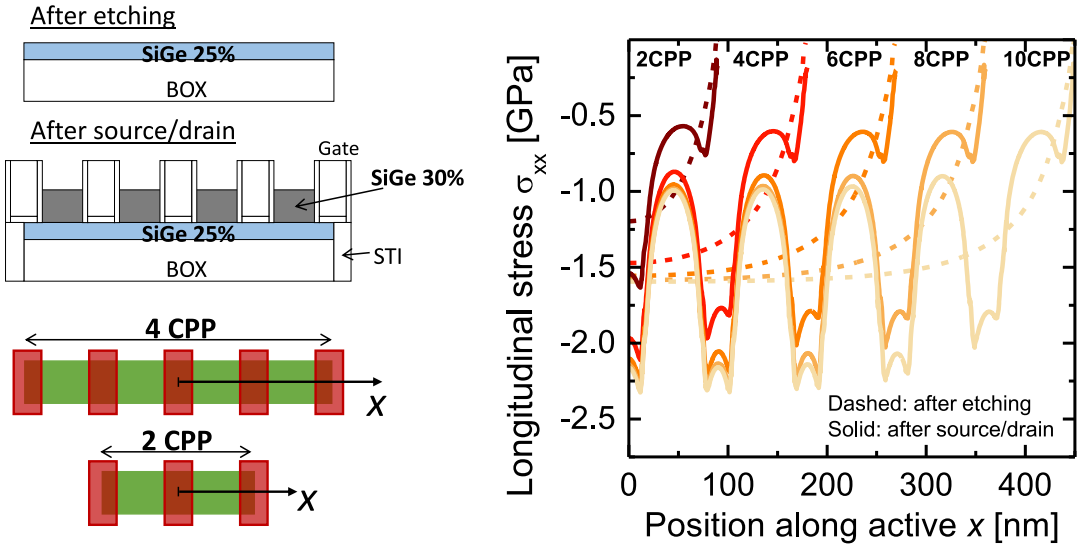


Figure 3.37: (left) Simulated structures with different active lengths (different numbers of CPP). (right) Simulated longitudinal stress profiles for different active lengths, after etching (dashed lines) and after source/drain epitaxy (solid lines). The additional stress from source/drain in the middle of the active area (x=0) is deduced by subtracting the two curves and reported in Figure 3.38.

Figure 3.37 shows the longitudinal stress profile after etching and after source/drain formation for structures of different active lengths obtained by varying the numbers of CPP. The additional stress from source/drain can be deduced after subtracting the stress after patterning. Figure 3.38 focuses on the channel located in the middle of the active area (i.e. at x=0). The additional stress from the source/drain is plotted with respect to the stress in the channel after patterning. The lower the stress in the substrate, the lower the stress induced by source/drain. This is because SiGe source/drain are fabricated by heteroepitaxy, the substrate being the SiGeOI channel. Yet, after patterning, the SiGeOI relaxes, as seen in section 3.2.1. The SiGe source/drain heteroepitaxy is thus performed on a substrate featuring a larger lattice than the one of Silicon, as represented in Figure 3.38. As a result, the intrinsic strain in the SiGe source/drain is lower. The force dragging the channel in compression is thus lower, resulting in a lower compressive stress generated in the channel. For instance, the additional stress from SiGe source/drain with 30% of Ge on a totally relaxed SiGeOI channel with 25% of Ge is equivalent to the stress from SiGe source/drain with 5% of Ge on a fully strained SiGeOI channel (whatever its Germanium concentration, since its lattice is the one of Silicon).

Finally, the active area patterning impacts the level of stress generated by both the SiGeOI channel and the SiGe source/drain.

3.3.3 Stress from SiGe source/drain compact modeling

The empirical model presented in the section 3.2.3 gives the stress in a patterned SiGe active area. Let us now consider the stress from SiGe source/drain, which plays a significant role on the final level of stress in the device. We have seen in section 3.3.1 that the additional stress from SiGe source/drain noted σ_{SD} is proportional to the Germanium concentration in source/drain y_{Ge} for a fully strained SiGe channel (see Figure 3.34). However, in the case of a relaxed channel, the efficiency

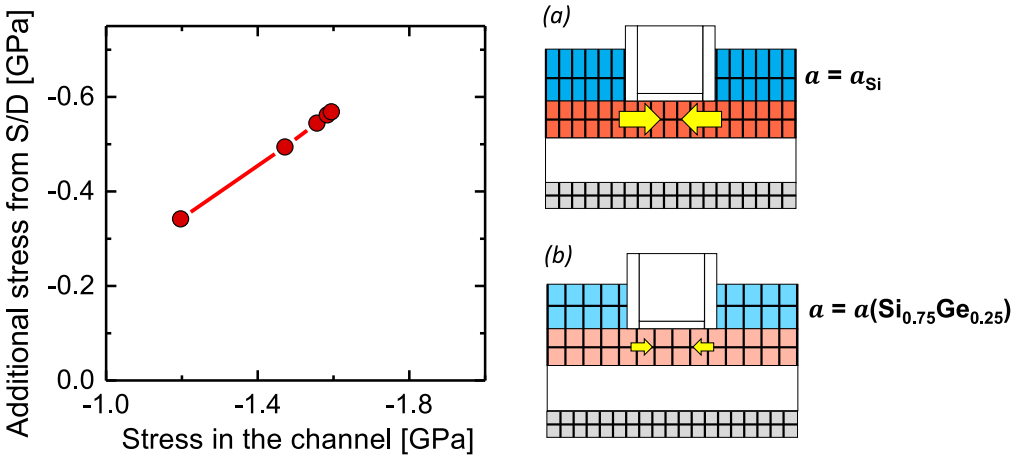


Figure 3.38: Simulated additional stress induced by the source/drain *vs.* stress in the channel after etching. Because of the $Si_{0.75}Ge_{0.25}$OI channel stress relaxation after patterning, $Si_{0.7}Ge_{0.3}$ source/drain are grown on a substrate with a larger lattice parameter than Si. As a result, the lower the stress in the channel, the lower the additional stress from source/drain, as illustrated on the right.

of the source/drain stressor is reduced because the SiGe source/drain epitaxy is made on a substrate featuring a lattice parameter larger than the one of Silicon (see Figure 3.38). In order to take this effect into account, we consider the equivalent Germanium concentration in the source/drain $y_{Ge,eq}$ defined as:

$$y_{Ge,eq} = y_{Ge} - x_{Ge} \cdot (1 - f_{relax}) \tag{3.30}$$

The additional stress is then given by:

$$\sigma_{SD} = S_{SD} \cdot y_{Ge,eq} \tag{3.31}$$

with S_{SD}=-15.7MPa/% for the geometry considered (14nm FDSOI with 90nm CPP). If the SiGe channel is fully strained, f_{relax}=1. This leads to $y_{Ge,eq}$=y_{Ge}. If the SiGe channel is totally relaxed, the intrinsic strain in the source/drain comes from the Germanium concentration difference between the source/drain (y_{Ge}) and the channel (x_{Ge}). As a consequence, the generated stress in the channel is lowered. For instance, using $Si_{0.7}Ge_{0.3}$ source/drain on a relaxed $Si_{0.75}Ge_{0.25}$ channel gives y_{Ge}=5% and would result in an additional compressive stress σ_{SD} of only $-15.7 \times 5 = 79$MPa. Finally, the total longitudinal stress σ_L, taking into account both channel and source/drain contributions is expressed as:

$$\sigma_L(x,L_{act},x_{Ge},y_{Ge}) = \sigma_0(x_{Ge}) \cdot f_{relax}(x,L_{act}) + S_{SD} \cdot \Big(y_{Ge} - x_{Ge}\big(1 - f_{relax}(x,L_{act})\big)\Big) \tag{3.32}$$

Figure 3.39 shows the relative deformation in the longitudinal direction measured at the end of the process flow by NBED. The additional stress from the source/drain is well taken into account by our empirical model. Especially, the variation close to the active edge due to the channel relaxation is in good agreement with the NBED measurement. It is worth noting that the same typical relaxation length of $\lambda = 84$nm is used after patterning (Figure 3.18) and at the end of the process flow.

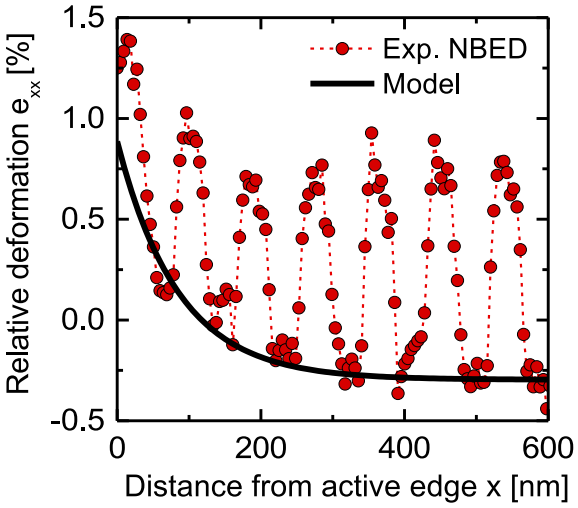


Figure 3.39: NBED and model relative deformation with source/drain stress taken into account. The model well reproduces the experimental data in the channels, i.e. under the gates (which are the region of interest for electrical behavior of the device). The typical relaxation length is $\lambda = 84$nm (the same as for the relaxation without source/drain of Figure 3.18).

3.4 Local Layout Effects: electrical results

A typical layout of a transistor is shown in Figure 3.40.

In the previous section 3.2, we have seen that the patterning of SiGeOI leads to a strong strain relaxation on the active area edges. The level of stress in the channel of a transistor thus depends on its proximity to the edge of active area.

3.4.1 Electrical characteristics modeling

In order to model the electrical characteristic layout dependence, we use the stress model previously described in sections 3.2.3 and 3.3.3. The longitudinal stress σ_L is given by:

$$\sigma_L(x,L_{act},x_{Ge},y_{Ge}) = \sigma_0(x_{Ge}) \cdot f_{relax}(x,L_{act}) + S_{SD} \cdot \Big(y_{Ge} - x_{Ge}\big(1 - f_{relax}(x,L_{act})\big)\Big) \quad (3.33)$$

with x_{Ge} and y_{Ge} the Germanium concentrations in the channel and in the source/drain, respectively, and considering that the gate is located at the position x along the active of length L_{act}. In the y direction, the gate covers the full active width W. The transverse stress σ_T is thus given by equation 3.22 and is expressed as:

$$\sigma_T(W) = \sigma_0(x_{Ge}) \left(1 - \frac{2\lambda}{W} + \exp\left(-\frac{W}{\lambda}\right)\left(1 + \frac{2\lambda}{W}\right)\right) \quad (3.34)$$

The layout dependence of electrical characteristics is investigated by focusing on two crucial parameters for MOSFETs: the mobility and the threshold voltage.

As far as mobility is concerned, the link with stress is established by the piezoresistive model, as detailed in section 2.1.3. The mobility as a function of the final longitudinal and transverse stresses, σ_L and σ_T respectively, is given by:

$$\frac{\mu(\sigma_L,\sigma_T)}{\mu(\sigma_L = \sigma_T = 0)} = \exp\left(\int_0^{\sigma_L} -\Pi_L(s)ds\right) \cdot \exp\left(\int_0^{\sigma_T} -\Pi_T(s)ds\right) \quad (3.35)$$

where Π_L and Π_T are the longitudinal and transverse piezoresistive coefficients, respectively. This model takes into account the dependence of the piezoresistive coefficients with stress. The electrical

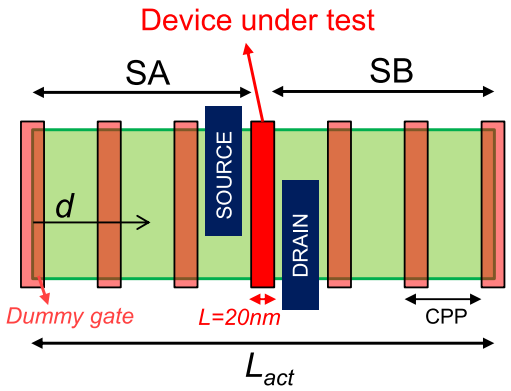


Figure 3.40: Definition of investigated parameters in Local Layout Effects study. SA/SB are the gate-to-STI distances from left and right sides, respectively. The active length L_{act} varies with the number of dummy gates used in the layout.

parameter of interest for assessing mobility variations is I_{ODLIN} which is the linear drain current at a given overdrive (V_G-V_{TLIN} = 0.5). This parameter is directly linked to the total resistance R_{TOT} ($I_{ODLIN} = \frac{V_{DLIN}}{R_{TOT}}$). Assuming that the access resistance is also impacted by the stress (see Chapter 2) and at a same extent (i.e. same piezoresistive coefficients), I_{ODLIN} is given by:

$$I_{ODLIN}(\sigma_L,\sigma_T) = I_{ODLIN,0} \cdot \exp\left(\int_0^{\sigma_L} -\Pi_L(s)ds\right) \cdot \exp\left(\int_0^{\sigma_T} -\Pi_T(s)ds\right) \tag{3.36}$$

where $I_{ODLIN,0}$ is the unstrained current value.

Regarding the threshold voltage of a pFET, the shift induced by strain can be expressed according to band shift [Cas12b; Lim04]:

$$\Delta V_T = \frac{\Delta EV(\varepsilon)}{q} + \frac{kT}{q} \ln\left(\sqrt{\frac{N_C N_V}{N_C(\varepsilon) N_V(\varepsilon)}}\right) \tag{3.37}$$

where ΔEV is the valence band edge shift and N_C and N_V are the density of states in the conduction band and valence band, respectively. The theory of potential deformation [Bal66; Her57; Rie93; Van86; Van89] (see section 1.3.2) gives the valence band shift according to the level of strain. The splitting of the valence band edge can be expressed as:

$$\Delta EV(\varepsilon) = a_v \varepsilon_{hydr} \pm \sqrt{\frac{b^2}{2}\left((\varepsilon_{xx}-\varepsilon_{yy})^2 + (\varepsilon_{yy}-\varepsilon_{zz})^2 + (\varepsilon_{zz}-\varepsilon_{xx})^2\right) + d^2\left({\varepsilon_{xy}}^2 + {\varepsilon_{yz}}^2 + {\varepsilon_{xz}}^2\right)} \tag{3.38}$$

where ε_{hydr} is the hydrostatic strain ($\varepsilon_{hydr} = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}$) and a_v , b and d are the deformation potentials. However, an uncertainty on these parameters is reported in the literature [Cas12b; Fis96; Van89], especially for the parameter related to the hydrostatic component (band shift without altering the degeneracy), which can not be directly measured. Also, the strain impact on the density of states is related to the change of effective mass, which is not straightforward. As a consequence, we use in this work a linear relationship with an empirical value of sensitivity that best fit our experimental data. This stress sensitivity is deduced once the stress relaxation has been formerly extracted on mobility results.

3.4.2 28nm SiGeOI results

3.4.2.a Impacts of orientation and Germanium concentration on performance

We have carried out experiments with SiGe channel integration in the STMicroelectronics' 28nm FDSOI route. The introduction of a SiGe channel in this so-called "ULPv2" technology is considered, along with other element changes (such as the gate stack and spacer material for instance, not evaluated in this work). The main purpose of SiGe integration in pFET channel is to tune the threshold voltage. The compressive stress will also impact the performance by impacting the mobility. The 28nm technology substrate is oriented along the <100> direction. Both orientations are investigated. The performance of the nominal device (W=300nm, L=30nm, SA=SB=353nm)

is presented in Figure 3.41 and compared with the performance of the reference 28nm FDSOI technology.

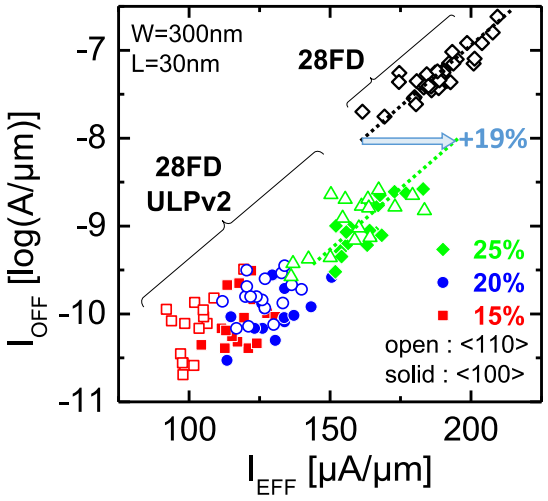


Figure 3.41: I_{EFF}/I_{OFF} trade-off for <100> and <110> SiGe channel pFETs of different Germanium concentrations. Performance is improved by 19% with respect to reference 28nm FDSOI technology. While the impact of Ge content is manifest, especially from V_T shift, the channel orientation does not play a significant role.

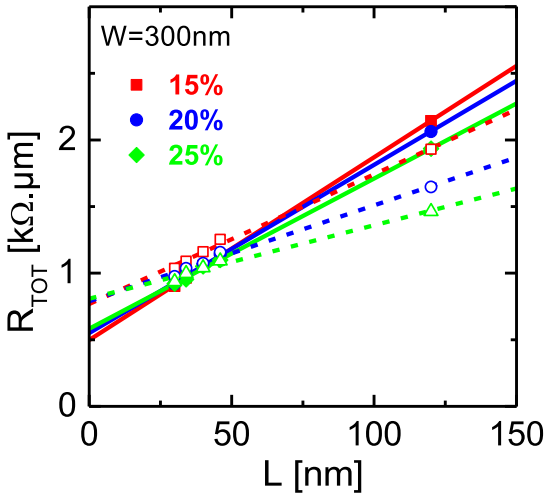


Figure 3.42: R_{TOT} *vs.* L for <100> and <110> SiGe channel pFETs of different Germanium concentrations. The slope and intercept give the β factor ($\beta = \frac{W}{L}\mu C_{ox}$) and access resistance R_{ACC}, respectively (see Chapter 2).

The impact of Germanium concentration is manifest: the higher the Ge content, the lower the V_T and in turn the higher leakage and effective drive currents. When comparing with 28nm FDSOI, a gain of +19% is achieved when 25% of Germanium is integrated. It has to be noted that the ULPv2 technology is significantly slower than the reference 28nm, i.e. of higher V_T, due to a different gate-stack. As far as the channel orientation is concerned, no effect is observed on the nominal device, showing same I_{EFF}/I_{OFF} trade-off.

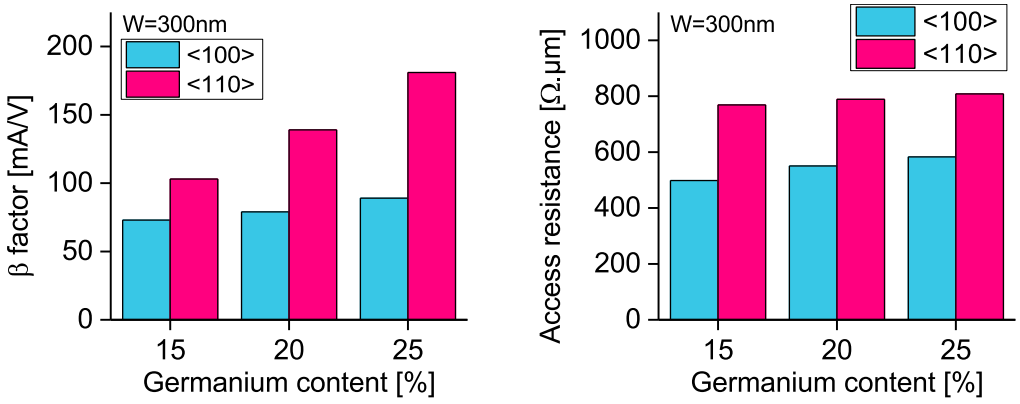


Figure 3.43: (left) β factor and (right) R_{ACC} for <100> and <110> SiGe channel pFETs of different Germanium concentrations. <110> oriented channels benefit from a higher mobility thanks to the uniaxial longitudinal stress configuration. However, they also show a degraded access resistance with respect to <100> oriented channel. This R_{ACC} degradation is attributed to the faceted source/drain epitaxy.

Figure 3.42 shows the R_{TOT} *vs.* L plot enabling the extraction of the β factor (proportional to mobility $\beta = \mu C_{ox} V_{GT,0}$, with $V_{GT,0} = 0.5$ the overdrive for R_{TOT} measurmeent) and the access

resistance R_{ACC} from the slope and intercept of the linear regression. Results are given in Figure 3.43. As expected, <110>-oriented channel mobility is higher than the one of <100> (×2 for 25% of Ge). This is because the stress configuration is more likely to be uniaxial at these dimensions. Yet the uniaxial longitudinal stress in <110> direction is the most favorable for hole mobility. However, <110>-oriented channels show a significantly higher access resistance (+39% for 25% of Ge), counter-balancing the gain on mobility. The degraded access resistance in <110> with respect to <100> is attributed to faceted Si source/drain epitaxy, as illustrated in Figure 3.44 As a result, the performance of the nominal device (Figure 3.41) is identical even though transport mechanisms are different.

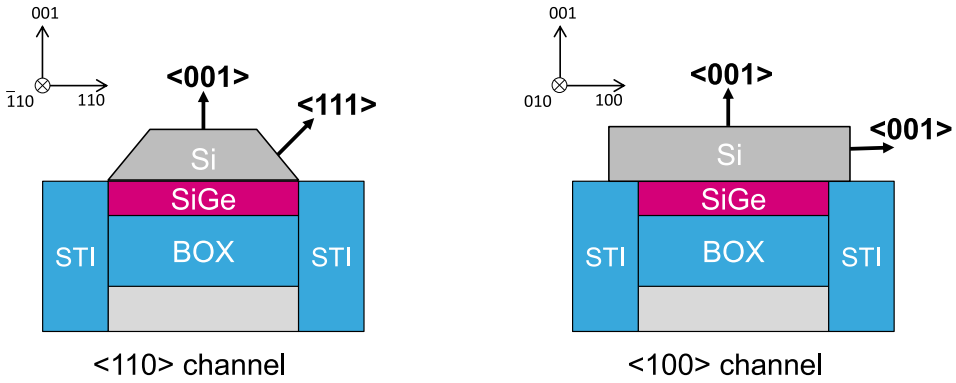


Figure 3.44: Illustration of different raised source/drain facets for <100> and <110> oriented channels. The cut is along W. The growth rate along the <111> oriented crystallographic plan is slower than <001> [Tun65]. This could lead to a degraded silicidation on the sides, responsible for a higher access resistance. The facets after SiGe epitaxy for <110> oriented channels can be observed on a TEM image of devices fabricated at LETI in Figure 5.35.

3.4.2.b Local layout effects

The layout effects are first assessed as a function of the active width. Figure 3.45 shows the R_{TOT} *vs.* W for L=1µm long channel devices, directly reflecting the carrier mobility. On the one hand, the <110> oriented channel mobility is enhanced when the active is narrowed. On the other hand, the <100> oriented channel mobility is degraded. This can be explain by the stress relaxation. The transverse stress reduces when the active is narrowed because of edge effects. The loss of compressive stress has opposite effect for <110> and <100> orientations. This result is expected from piezoresistive coefficients predicting that the best compressive stress configuration for hole in <100>-oriented channels is biaxial while it is uniaxial longitudinal for <110> [Web07]. The transverse stress is thus beneficial for <100> and detrimental for <110>. Its relaxation when the active is narrowed thus degrades <100> channels and enhances <110> ones.

The W-effect is also measured on short channels and presented in Figure 3.46. Contrarily to long channels, short channels are strongly impacted by the access resistance, which is found to be different for <100> and <110>. Nevertheless, the opposite effect of stress relaxation is also evidenced.

The <110> short channel $R_{TOT}(W)$ behavior shows lower gain than for long channel. This is also attributed to faceted raised source/drain. The narrow the active, the higher impact of the facets on the active edges. This results in an increasing access resistance with W that could explain the

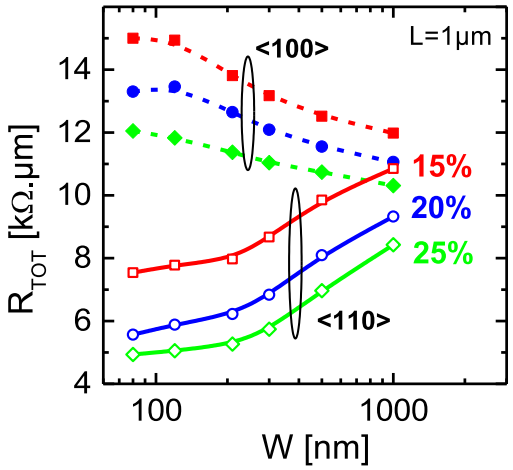


Figure 3.45: R_{TOT} *vs.* W for L=1µm <100> and <110> SiGe channel of different Germanium concentrations. The narrower the active, the higher mobility for <110> and the lower mobility for <100>. This can be explained by the transverse stress relaxation. The transverse stress is detrimental for <110> channel, hence the gain when this stress component is reduced. It is the opposite for <100> channels.

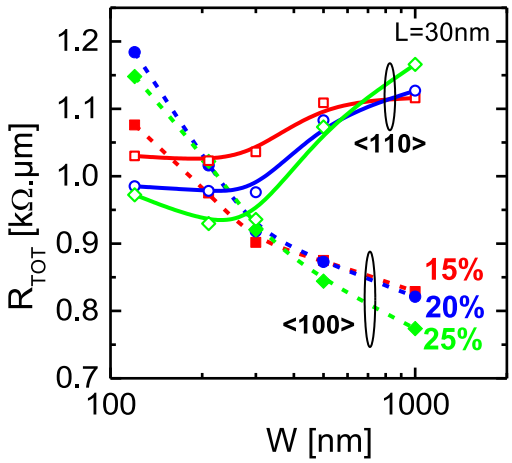


Figure 3.46: R_{TOT} *vs.* W for L=30nm <100> and <110> SiGe channel of different Germanium concentrations. As for long channels, the active narrowing is beneficial for <110> channel while it is detrimental for <100> channel. This can be explained by the transverse stress relaxation. For large W, <110> orientation is degraded compared to <100>, which is not the case for long channel. This change of behavior from long to short channel is attributed to a different access resistance (see Figure 3.44).

behavior change from long to short channels. This effect is also observed in the 14nm FDSOI technology, as discussed later on Figure 3.62.

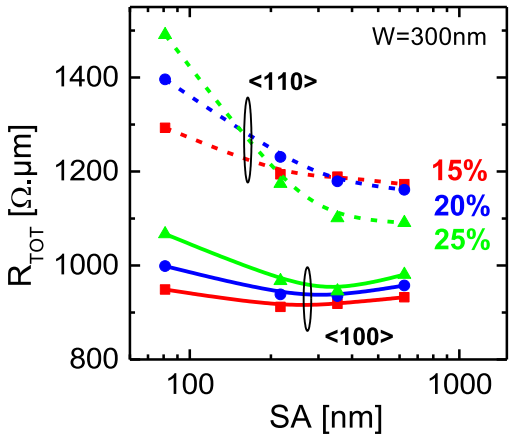


Figure 3.47: R_{TOT} *vs.* SA for <100> and <110> SiGe channel of different Germanium concentrations. <110> oriented channels suffer from longitudinal stress relaxation while <100> oriented ones are less sensitive.

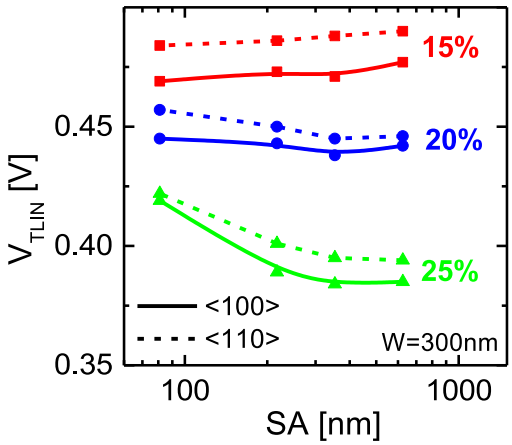


Figure 3.48: V_{TLIN} *vs.* SA for <100> and <110> SiGe channel of different Germanium concentrations. The higher the Germanium concentration, the lower the threshold voltage, as already observed [Cas12b; Sou13].

The layout effect in the other direction is assessed on short channels with different active lengths varying through SA/SB parameters (see Figure 3.40). Figure 3.47 shows the variation of R_{TOT} as a function of SA=SB. Both <100> and <110> oriented channels show mobility degradation for

short actives. This is attributed to the longitudinal stress relaxation, beneficial for both <110> and <100> channels. Nevertheless, <110> channels are more sensitive, as predicted from piezoresistive coefficients [Web07]. As far as the threshold voltage is concerned, plotted in Figure 3.48, the main effect is the Germanium concentration (the higher the Ge content, the lower V_{TLIN}). The impact of the longitudinal stress relaxation is only visible for 25% of Germanium, at a similar extent for <100> and <110> channel orientations.

3.4.2.c Conclusion to 28nm results

The integration of SiGe channel in 28nm FDSOI pFET channel is an efficent knob for reducing the threshold voltage. Besides, the compressive stress leads to hole mobility improvement. Despite a higher sensitivity to strain in <110>-orientation, the <100>-orientation of 28nm FDSOI is beneficial in terms of access resistance. The main layout effect is the impact of the transverse stress relaxation, beneficial in <110> orientation but detrimental in <100> one. Nevertheless, The <100> orientation appears as preferential for a SiGe channel 28nm FDSOI technology. For the 14nm FDSOI technology, the <110> orientation is preferred to take the most benefit from the purely longitudinal stress induced by SiGe:B source/drain.

3.4.3 14nm SiGeOI results

We investigated the layout effects in devices from the 14nm FDSOI embedding SiGe channel and source/drain for pMOSFETs (see section 3.1).

3.4.3.a Rectangular symmetrical and asymmetrical layouts

Figure 3.49 shows V_{TLIN} and I_{ODLIN} variations for nMOSFETs built on active area of different lengths, while the active width is W=170nm and the gate length is L=20nm. The active length varies with the number of dummy poly gates, as shown in Figure 3.40. The CPP is constant with a value of 90nm. The device under test is located in the middle of the active area, that is to say the layout are symmetric (SA=SB). The flat behavior observed is expected since the nMOSFET channel is made of unstrained Silicon. In addition, it indicates that no significant stress from STI alters the electrical characteristics of the device.

On the other hand, the pMOSFET electrical characteristics are strongly impacted by the layout geometry. As shown in Figure 3.50, the threshold voltage increases[1] and the linear drain current at a given overdrive (I_{ODLIN}) significantly decreases. This is due to the loss of longitudinal compressive stress for short active. The shorter the active, the lower stress because of the relaxation occurring on the active edge (see section 3.2.1). The 14nm FDSOI technology features <110> oriented channels. The loss of longitudinal stress is highly detrimental for the <110> hole mobility. That is why the I_{ODLIN} current of pMOSFETs built on short active area is strongly degraded.

The lines in Figure 3.50 correspond to the model presented in section 3.2.3. Both V_{TLIN} and I_{ODLIN} variations are well reproduced. The typical relaxation length that best fit the experimental results is λ =66nm. The unstressed values of reference are $V_{T0} = -0.49V$ and $I_{OD,0} = 63\,\mu A/\mu m$.

Figure 3.51 compares the layout effect of SiGe and Si channel pMOSFETs. The lines in this Figure correspond to the stress-based model presented in section 3.2.3 and used in Figure 3.50. I_{ODLIN} data

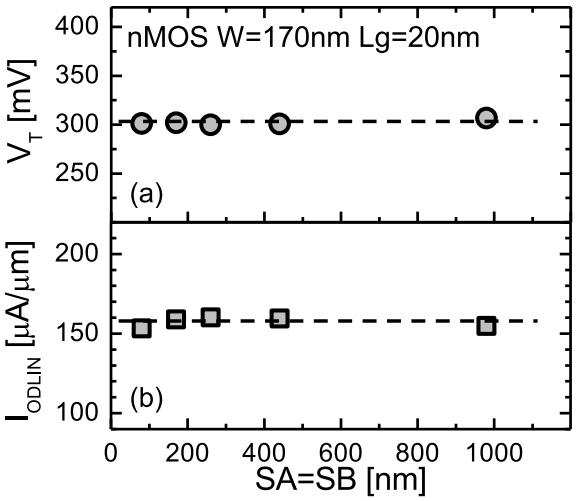


Figure 3.49: (a) V_{TLIN} and (b) I_{ODLIN} as a function of the gate-to-STI distance SA (=SB) for a W=170nm L=20nm nMOS device. No layout effect is observed because nMOS channel is unstrained. This result also shows that possible stress generated by STI proximity is not significant.

1 The threshold voltage variation are always discussed in absolute value. This makes sense for circuit design.

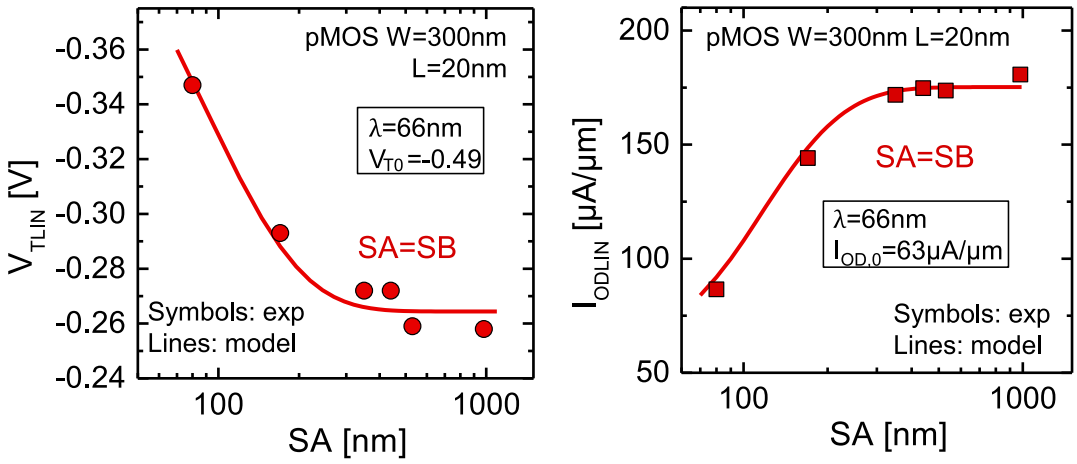


Figure 3.50: (left) V_{TLIN} and (right) I_{ODLIN} as a function of the gate-to-STI distance SA (=SB) for a W=300nm L=20nm pMOS device. The threshold voltage increases and I_{ODLIN} decreases for short active areas. This is due to a lower strain coming from the relaxation on the active edges. The model described in section 3.2.3 enables to reproduce the layout effect with a typical relaxation length λ=66nm. The used stress sensitivity is S_σ = 110mV/GPa.

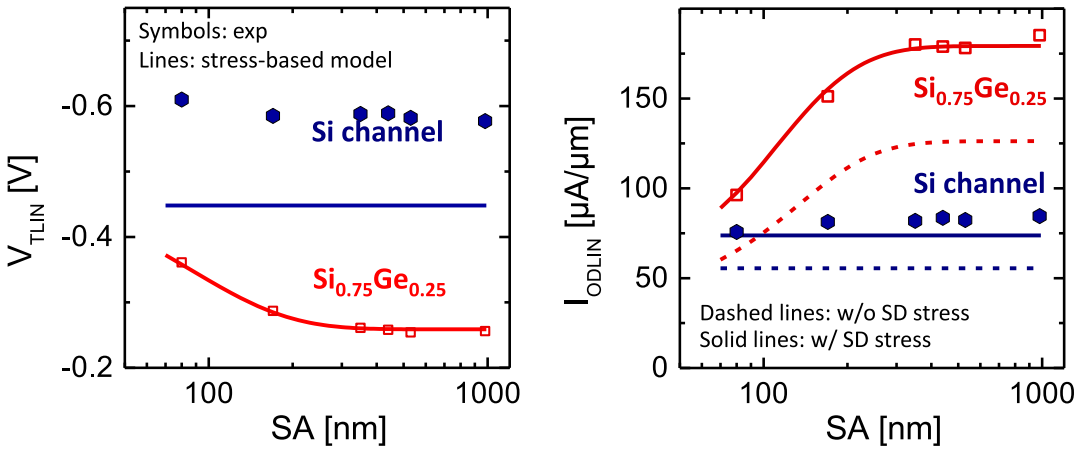


Figure 3.51: (left) V_{TLIN} and (right) I_{ODLIN} *vs.* gate-to-STI SA (=SB) for W=170nm L=20nm pMOS with SiGe and Si channels. The lines derive from the stress-based model calibrated on SiGe channel layout effects. The Si data are well predicted for I_{ODLIN}. The threshold voltage V_{TLIN} is however highly underestimated. This result suggests that the V_T shift with SiGe introduction is not only due to strain, as already evidenced in literature [Cas12b; Sou13].

of Si channel are well predicted by the model, provided the stress from SiGe:B source/drain is taken into account (solid line). The impact of the source/drain is emphasized in this Figure by comparing the solid lines to the dashed ones.

As far as the threshold voltage is concerned, the model fails to predict the V_{TLIN} shift from SiGe to Si. The threshold voltage induced by SiGe channel integration is not fully explained by strain-induced band shifts. This has been already observed and discussed in the literature. The presence of dipoles has been proposed [Sou13].

Asymmetric layouts are investigated in Figure 3.52. In these layouts, the gate-to-STI distance on the drain side SB is fixed at either 80nm or 980nm. The gate-to-STI on the source side, SA,

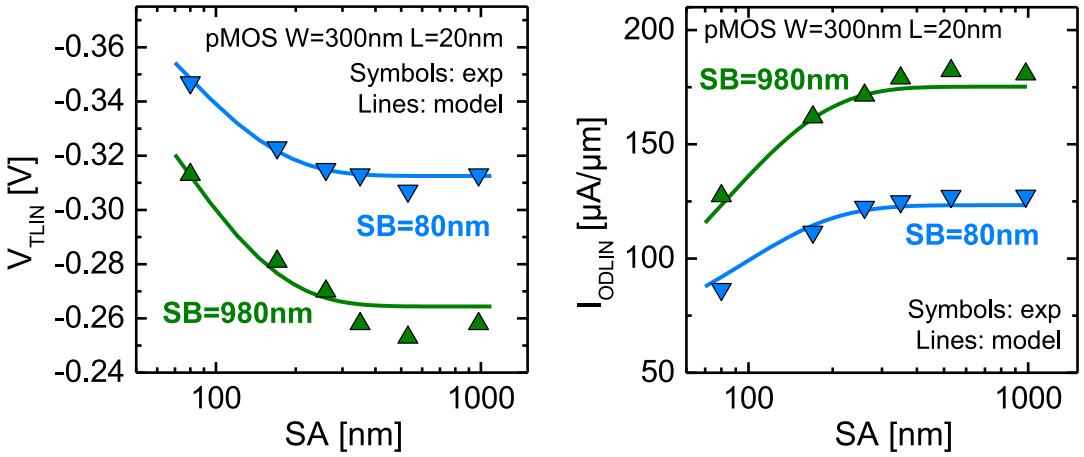


Figure 3.52: (left) V_{TLIN} and (right) I_{ODLIN} as a function of the gate-to-STI distance SA while SB value is fixed at either 980nm or 80nm for a W=300nm L=20nm pMOS device. The behavior is similar to the symmetric case of Figure 3.50, this time showing the impact of one edge proximity. The model parameters are the same as for Figure 3.50 (especially $\lambda = 66$nm).

varies according to the number of dummy gates. This enables to assess the impact of only one edge proximity. Similarly to symmetric layouts, the proximity of the active border leads to threshold V_{TLIN} and I_{ODLIN} decrease. Both electrical parameters are directly limited by the shorter gate-to-STI distance. The model shows a good agreement with experimental data. It is worth noting that the same and unique parameter of relaxation $\lambda = 66$nm enables to reproduce the symmetric and asymmetric layout effects.

In order to properly reproduce the I_{ODLIN} degradation for short active area, we consider I_{ODLIN} to be strictly proportional to the mobility. This means that we do not take into account the series resistance, expected not to be dependent on the stress level. Since the assessed devices feature a short gate length, the access resistance plays a significant role on the total resistance. Nevertheless, results of Chapter 2 evidenced the role of strain on access resistance. Especially, the region under the spacer, which acts as a parasitic series transistor, is sensitive to the gate voltage and to the level of strain in the device.

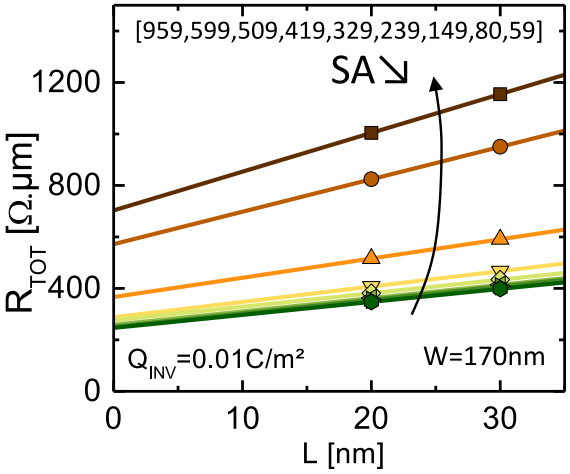


Figure 3.53: R_{tot} *vs.* L for SiGeOI pMOSFETs of different L_{act}. Slope and intercept of linear regressions give the mobility and the access resistance, respectively.

Figure 3.53 shows the total resistance R_{TOT} as a function of the gate length L for devices built on

different active area lengths. Only two short gate lengths (L=20nm and L=30nm) are available at a given active length. This allows to keep a similar configuration regarding the active edge proximity. From this plot, linear regressions enable the extraction of the mobility μ and the access resistance R_{ACC} from the slope and intercept, respectively.

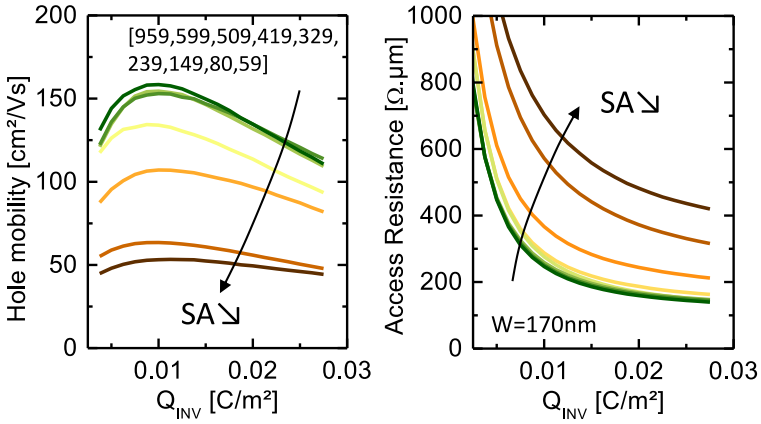


Figure 3.54: (left) Mobility and (right) access resistance *vs.* the inversion charge Q_{inv} for SiGeOI pMOSFETs of different L_{act}, extracted from linear regressions of Figure 3.53.

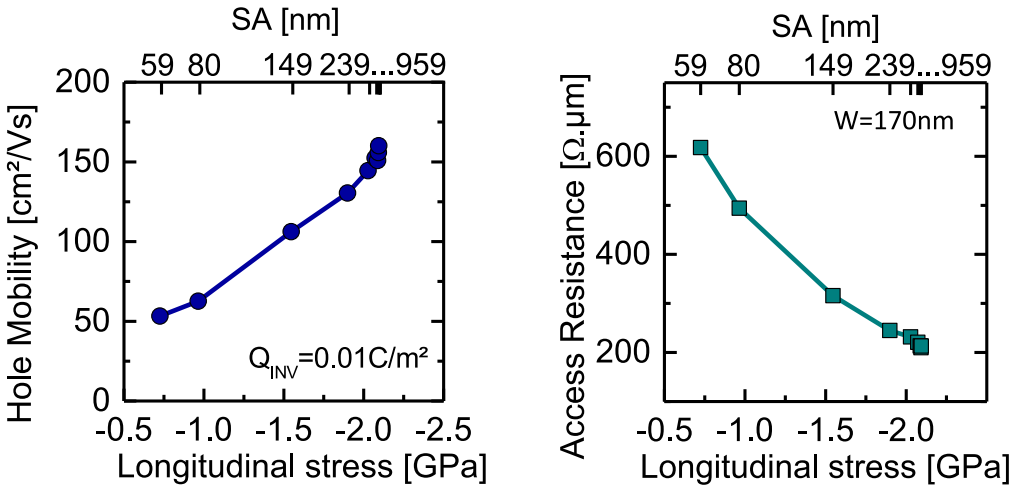


Figure 3.55: Extracted mobility and access resistance at Q_{inv} according to the longitudinal stress of each active length L_{act}. The value of stress is deduced from the relaxation model. The longitudinal stress impacts both the mobility and the access resistance. This result is consistent with Chapter 2.

The extracted mobility and access resistance as a function of the inversion charge are shown in Figure 3.54. The access resistance strongly depends on the inversion charge, as widely discussed in Chapter 2. Figure 3.55 shows the mobility and access resistance extracted at Q_{INV}=0.01C/m^2 according to SA. The corresponding longitudinal stress for each value of SA is deduced from the stress profile model presented in section 3.2.3, assuming a typical relaxation length of $\lambda = 82$nm that best fit the experimental data. We should note that for these measurements obtained on an other experiment using a different maskset, the relaxation length differs from the previous results (Figure 3.50).

The shorter the active, the lower the stress and thus the lower the mobility. The access resistance also strongly depends on the active length: the shorter the active, the higher the access resistance. That is to say, the higher the longitudinal compressive stress, the lower the access resistance. This finding is consistent with the results of Chapter 2: strain impacts the access resistance, as also evidenced

here on layout effects of SiGeOI pMOSFETs.

3.4.3.b Non-rectangular layouts

In integrated circuit designs, the active area is not necessarily rectangular[1]. Figure 3.56 shows the non-rectangular active layouts investigated here. The active corners present in such layout are called "RX-jogs". Two layout configurations are available: symmetric (T-shaped), with one RX-jog on each side and asymmetric (Γ-shaped), with only one RX-jog on drain side. The layouts are defined with 2 sets of gate-to-STI distances (SA_1,SB_1 and SA_2,SB_2), whose values are fixed to either 80nm (1 CPP) or 980nm (considered as infinite active).

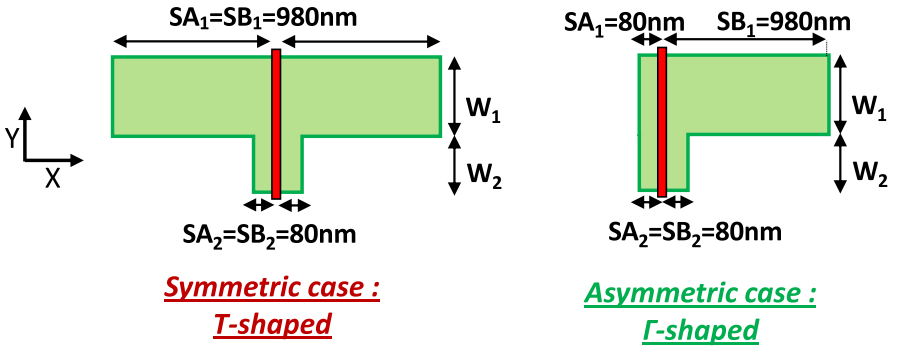


Figure 3.56: Scheme of non-rectangular layouts, i.e. with the presence of a least one RX-jog. Symmetric case (T-shaped) on the left and asymmetric case (Γ-shaped) on the right.

The jog ratio is defined as the width ratio:

$$\text{Jog ratio } \omega = \frac{W_2}{W_1 + W_2} \tag{3.39}$$

If $\omega = 0$ or $\omega = 1$, the layout is rectangular. In order to model the layout effect induced by stress

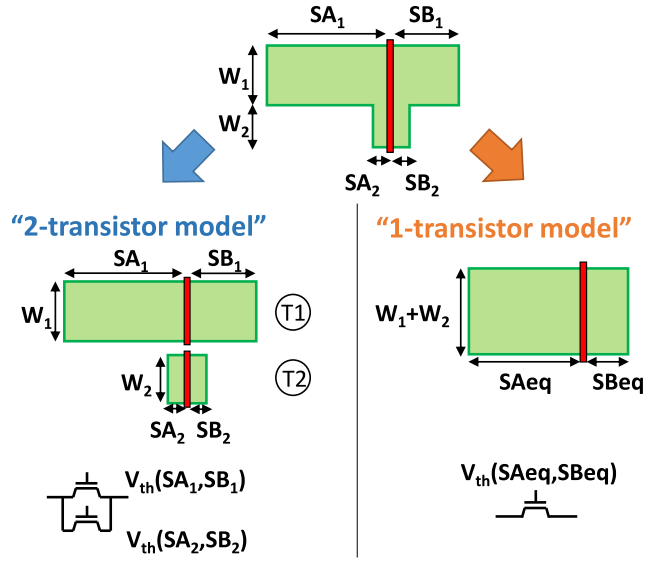


Figure 3.57: Illustration of the two approaches used to model the device built on a non-rectangular active area, i.e. with presence of a RX-jog. The so-called "2-transistor" model considers two transistors in parallel, each one with its own gate-to-STI distances SA and SB. The "1-transistor" model assumes equivalent gate-to-STI distances SAeq and SBeq (see equation 3.43).

1 Non-rectangular active area are common inside logic standard cells like flip-flops for instance. It might also result from abutment of standard cells featuring active of different widths (see section 4.2.2).

relaxation on such non-rectangular active devices, two approaches are investigated, illustrated on Figure 3.57.

- The so-called "2-transistor" model considers two transistors in parallel, each one with its own gate-to-STI distances SA_1,SB_1 and SA_2,SB_2. Considering that V_{TLIN} is extracted in the subthreshold regime, equation 3.40 is used.

$$I_{D,subVt} = I_{th0}\frac{W}{L}\exp\left(\frac{V_G - V_T}{SS/\ln(10)}\right) \tag{3.40}$$

  with I_{th0} the constant current criterion for V_T extraction (usually 100nA) and SS the subthreshold swing, assumed to be 80mV/decade. Considering two transistors in parallel, the threshold voltage V_{TLIN} of the whole device is derived by solving:

$$\begin{aligned} & I_{D,subVt}\Big[W = (1-\omega)W\,,\, V_T = V_T(SA_1,SB_1)\,,\, V_G = V_{TLIN}\Big] \\ + \; & I_{D,subVt}\Big[W = \omega W\,,\, V_T = V_T(SA_2,SB_2)\,,\, V_G = V_{TLIN}\Big] \\ = \; & I_{th0} \end{aligned} \tag{3.41}$$

  This leads to:

$$V_{TLIN}(\omega) = \frac{SS}{\ln(10)}\cdot\ln\left[(1-\omega)\,\exp\left(\frac{V_{TLIN}(SA_1,SB_1)}{SS/\ln(10)}\right) + \omega\,\exp\left(\frac{V_{TLIN}(SA_2,SB_2)}{SS/\ln(10)}\right)\right] \tag{3.42}$$

  In this approach, the two transistors have their own level of stress according to their (SA,SB) couple. In other words, they are assumed to be strictly independent. However, there is a 2D effect because they are built on a single active. The shortest part (i.e. with smaller SA/SB values) is not totally free to relax because it is partly maintained by the second part of the active (with longer SA/SB values). Nevertheless, this effect is of second order compared to the longitudinal relaxation and is not required to properly reproduce the experimental data.

- The so-called "1-transistor" model assumes equivalent gate-to-STI distances SAeq and SBeq which are empirically derived from equation 3.43.

$$SAeq = \left(\frac{1-\omega}{SA_1} + \frac{\omega}{SA_2}\right)^{-1} \tag{3.43}$$

The variation of V_{TLIN} with respect to the jog ratio ω is shown in Figure 3.58. When $\omega = 0$, the active is rectangular with SA=SB=980nm for the symmetric case. This means that the device is not impacted by the relaxation on the active edge since it is located far enough. When $\omega > 0$, there is a part of the channel which is located close to the active edge. This part of the channel is impacted by the stress relaxation. As a consequence, the higher the jog ratio, the higher V_{TLIN}.

The partial relaxation also impacts the mobility, leading to an I_{ODLIN} degradation when the jog ratio increases (Figure 3.59). Both modeling approaches enable to reproduce the experimental results with

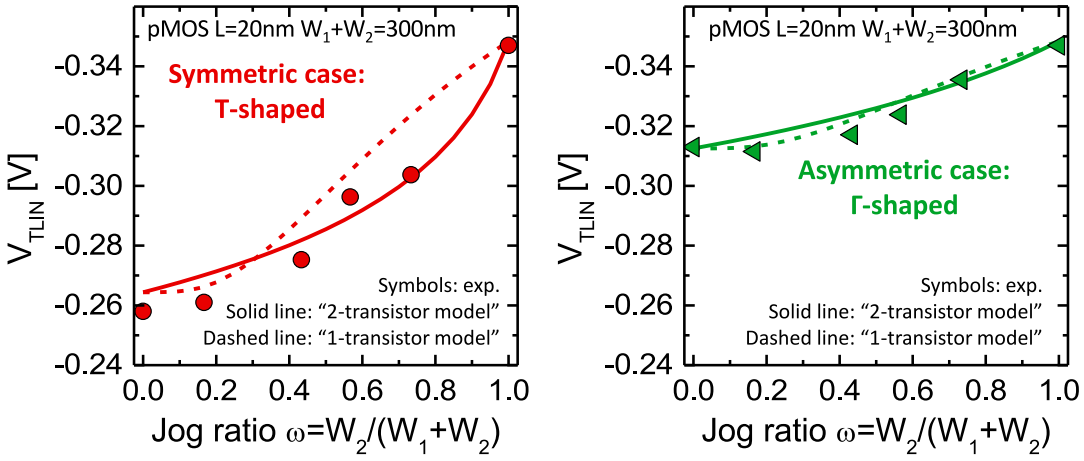


Figure 3.58: pMOS V_{TLIN} as a function of the jog ratio for two different cases of non-rectangular active area: symmetric (left) and asymmetric (right). Experimental data are well reproduced by the two different model approaches.

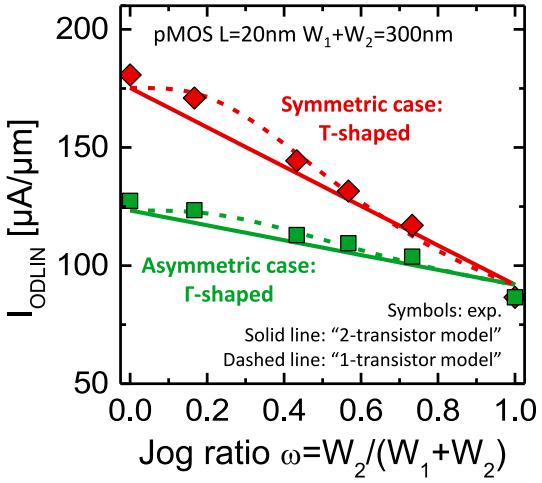


Figure 3.59: pMOS I_{ODLIN} as a function of the jog ratio for two different cases of non-rectangular active area: symmetric and asymmetric. Experimental data are well reproduced by the two different model approaches.

good accuracy, this for both symmetric and asymmetric layouts. The advantage of the '1-transistor' model is to consider only one device for Layout Vs. Schematic (LVS), which in turn results in faster SPICE simulations.

3.4.3.c Multifinger layouts

So far, the devices under test consist in one active gate finger while others are dummies, i.e. not connected. This enables a better characterization of the device under a specific environment. In standard cells however, all the gate fingers are connected either in series or in parallel according to the logic function (see section 1.1.1.b). In these so-called multifinger layouts, each gate finger is characterized by its own gate-to-STI distances SA_i and SB_i as illustrated in Figure 3.60.

The threshold voltage of multifinger built in parallel as a function of the number of fingers N_f is presented in Figure 3.60. The more fingers, the lower V_{TLIN} since only the two fingers located close to the active edge are impacted by the relaxation. The multifinger data are compared with the one-active-finger case (i.e. data from Figure 3.50) to emphasize the impact of fingers located close to the active edge. For an active of 11 fingers, the fingers impacted by the relaxation are

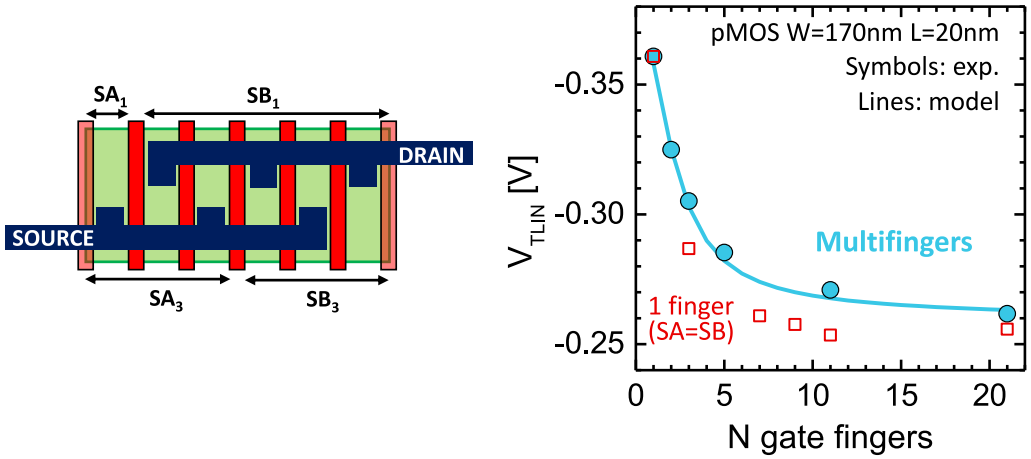


Figure 3.60: (left) multifinger layout with all the gate fingers connected in parallel. (right) V_{TLIN} as a function of the number of gate fingers. The 1-finger case is also plotted to highlight the impact of strain relaxation on fingers close to the active area edge. Multifinger model reproduces well the experimental data.

responsible for 20mV V_{TLIN} shift. The model of V_{TLIN} for multifinger considers parallel transistors in the subthreshold regime. Equation 3.44 is used, assuming a subthreshold swing SS of 80mV/decade, similarly as the 2-transistor model used for non-rectangular layouts. The model properly accounts for the gate fingers close to the active edge, impacting the V_{TLIN} of the whole multifinger device.

$$V_T(N_f) = -SS/\ln(10)\ \ln\left(\frac{1}{N_f}\sum_{i=1}^{N_f}\exp\left(\frac{-V_T(SA_i,SB_i)}{SS/\ln(10)}\right)\right) \tag{3.44}$$

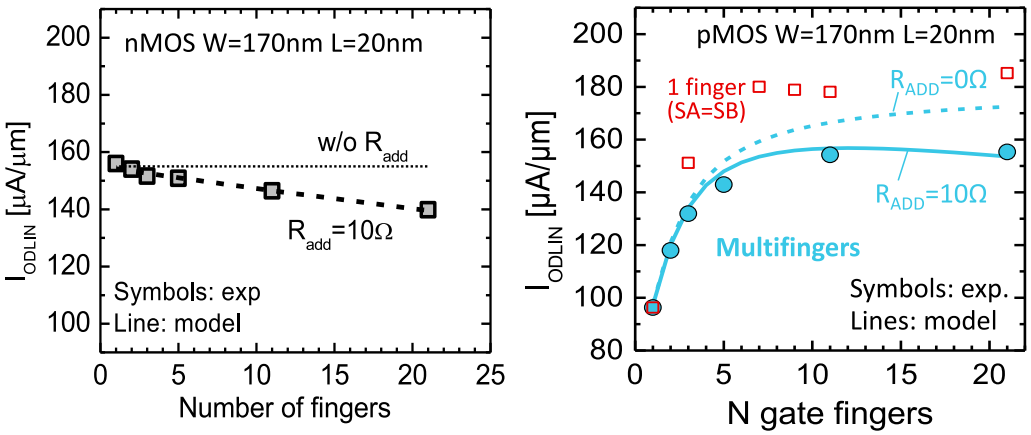


Figure 3.61: Multifinger (left) nMOS and (right) pMOS I_{ODLIN} as a function of the number of gate fingers. The multifinger model reproduces well the experimental data, provided that an additional parasitic series resistance is considered, consistently with nMOS results.

Figure 3.61 shows the I_{ODLIN} for multifinger device. As for the threshold voltage, the mobility of gate fingers located close to the active edges is degraded by the stress relaxation. This impacts the overall I_{ODLIN} current. In order to properly model multifinger I_{ODLIN}, it is necessary to take into account the fact that each finger has not the same V_{TLIN} (because of stress effects) and thus operates

at a different overdrive. It thus requires the use of a model of linear drain current. We use a simple model given by equation 3.45:

$$I_D(V_G) = \beta \frac{\mid V_G - V_T \mid}{1 + \theta_1 \mid V_G - V_T \mid} \tag{3.45}$$

We can thus express the current in each gate finger as a function of I_{ODLIN}:

$$I_D(SA,SB) = I_{ODLIN}(SA,SB) \cdot \frac{V_{GT}}{V_{GT0}} \cdot \frac{1 + \theta_1 \mid V_{GT0} \mid}{1 + \theta_1 \mid V_{GT} \mid} \tag{3.46}$$

with $V_{GT} = V_G - V_T$, V_{GT0} is the overdrive used in the measurement of I_{ODLIN}, i.e. 0.5V, and θ_1 is the parameter of mobility attenuation and access resistance, which is fixed at 0.3 V^{-1}. Finally, the I_{ODLIN} is measured at $V_G = V_T(N_f) + V_{GT0}$, with $V_T(N_f)$ previously described by equation 3.47 and can thus be calculated by summing on each gate finger:

$$I_{ODLIN}(N_f) = \frac{1}{N_f} \sum_{i=1}^{N_f} I_D(SA_i,SB_i) \tag{3.47}$$

Our model of multifinger well reproduces the experimental data, provided an additional series resistance of 10 Ohm is considered. This additional resistance may be linked to wires/contact in our structure since it also affects multifinger nMOS I_{ODLIN} to the same extent (see Figure 3.61).

3.4.3.d Active narrowing

As far as the transverse stress relaxation is concerned, devices of different widths are investigated. Focusing on long channel devices allows us to directly sensing the mobility since the access resistance is negligible.

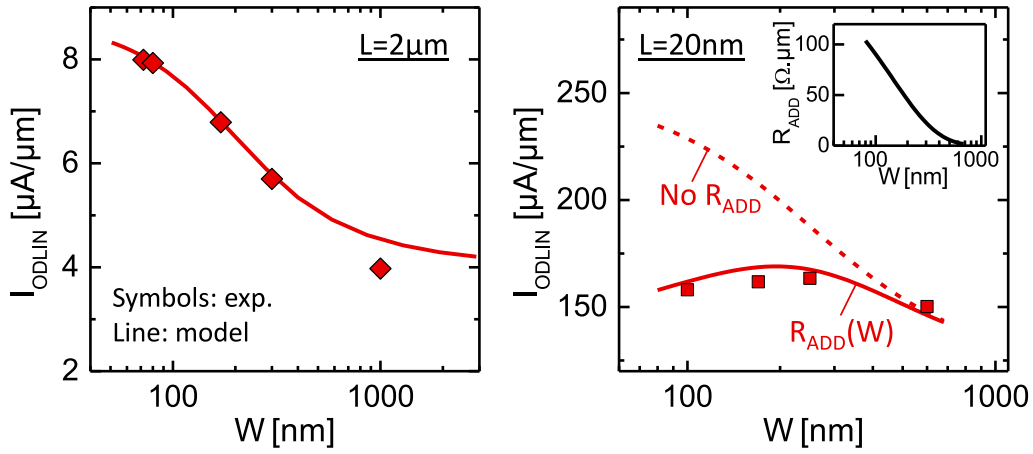


Figure 3.62: I_{ODLIN} *vs.* active width W for (left) long channel L=2µm and (right) short channel L=20nm. While the model considering transverse stress relaxation enables to well reproduce long channel I_{ODLIN} increase, it fails for short channel. This can be attributed to a higher access resistance for narrow devices (see inset). Such access resistance behavior could result from a faceted SiGe source/drain epitaxy (discussed in Figure 3.44).

Figure 3.62 shows the I_{ODLIN} as a function of the active width W for both long (L=1µm) and short

(L=20nm) channel devices. The narrower the active, the higher I_{ODLIN}. This is because the stress configuration becomes uniaxial longitudinal. Since the transverse compressive stress is detrimental in <110>-oriented channels, the relaxation is beneficial. The long channel behavior is well reproduced by the model of average stress (see eq 3.34, using the same relaxation length as for longitudinal relaxation, i.e. $\lambda = 66$nm).

However, short channel behavior is different, with a "bell-shaped" $I_{ODLIN}(W)$ curve. The model thus fails to reproduce the experimental trend. By adding an additional series resistance that increases with W, a good agreement with measurements is achieved. A possible explanation for this additional series resistance could be the faceted epitaxy of raised SiGe:B source and drain. This has been discussed in section 3.4.2 when comparing <100> and <110> channel orientations. The faceted regions could lead to a degraded silicidation on the sides, responsible for a higher access resistance. These faceted regions on the sides become predominant when the active is narrowed. This is translated into an increasing access resistance with W reduction (see inset of Figure 3.62).

If an optimization of the raised source/drain epitaxy could be achieved, the performance of short channels on narrow active would be highly enhanced.

3.4.3.e Impact of Germanium concentration

In this section, different Germanium concentrations in the channel have been investigated. In this experiment[1], the Ge content varies from 25% to 34%. In addition, the samples feature different TiN thicknesses in the gate stack. The samples are summarized in Table 3.2.

Table 3.2: Samples investigated.

Sample	Ge concentration [%]	TiN thickness [Å]
A	25	45
B	25	15
C	30	15
D	30	10
E	34	10

The impact of the Germanium concentration on I_{ODLIN} current is shown in Figure 3.63. The TiN thickness does not affect I_{ODLIN} (not shown on the Figure). For W=600nm and SA=959nm, the higher the Germanium concentration, the higher current because of higher beneficial longitudinal stress. For W=600nm and SA=59nm however, the higher the Germanium concentration, the lower I_{ODLIN}. In such layout, the longitudinal stress is almost relaxed and thus the dominant stress component is the transverse one, even though it is also partially relaxed. Yet this component is detrimental for hole mobility.

Using a single typical relaxation length ($\lambda = 82$nm) and the same reference unstrained I_{ODLIN} current ($I_{OD,0} = 59\,\mu A/\mu m$), the model succeeds to reproduce the layout effect and especially the crossover

1 These results come from an other experiment w.r.t previous sections and uses a different maskset.

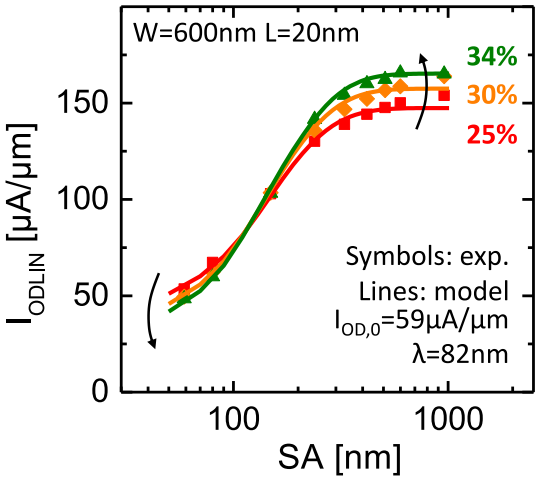


Figure 3.63: I_{ODLIN} *vs.* gate-to-STI SA (=SB) for W=600nm L=20nm pMOS with SiGe channels of different Germanium concentrations. The model represented by the lines well reproduces the experimental data assuming the same typical relaxation length. Especially, the crossover is explained by the stress configuration. For long active areas, the higher the Germanium content, the higher mobility due to beneficial uniaxial longitudinal strain configuration. For short active areas however, the main strain component is transverse, which is detrimental. Hence the higher mobility for lower Germanium content (i.e lower strain).

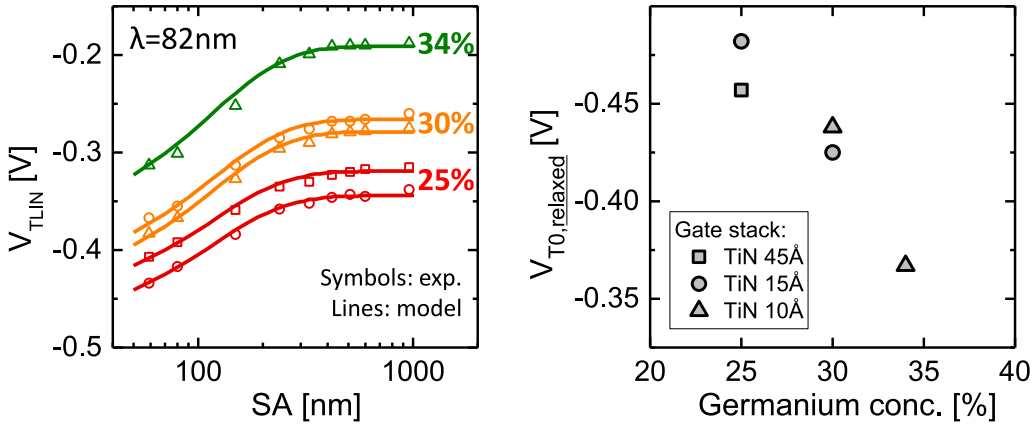


Figure 3.64: (left) V_{TLIN} *vs.* gate-to-STI SA (=SB) for W=600nm L=20nm pMOS with SiGe channels of different Germanium concentrations and different gate stacks (TiN thicknesses). The stress-based model reproduces the experimental data using the same typical relaxation length. (right) $V_{T0,relaxed}$ extracted from the model as a function of the Germanium concentration for different gate stacks. Consistently with Figure 3.51, the threshold voltage shift induced by SiGe is not entirely explained by strain.

due to change of the main stress component. This result suggests that the typical relaxation length of the patterned SiGeOI does not depend on the initial level of strain or Ge concentration. Nevertheless, it is worth noting that the range of Germanium concentration investigated remains narrow.

As for I_{ODLIN}, a single value of typical relaxation enables to properly model the V_{TLIN} layout effect for different Germanium concentrations (Figure 3.64). Contrarily to I_{ODLIN}, the threshold voltage is impacted by the TiN metal gate thickness. While the typical relaxation length λ is the same for all samples, the fitted unstressed threshold voltage parameter $V_{T0,relaxed}$ varies. $V_{T0,relaxed}$ for each configuration is plotted as a function of the Germanium concentration. Two effects are observed. First, at a given Ge concentration, the thinner the TiN layer, the higher V_T. Then, the higher

the Ge concentration, the lower the threshold voltage. We insist on the fact that this effect is not strain-related as the $V_{T0,relaxed}$ parameter is the threshold voltage of a relaxed channel. In other words, the strain is not the only responsible of V_T shift when Germanium is introduced in the channel. This has been already evidenced in Figure 3.51 and reported in the literature [Cas12b; Sou13].

3.5 Conclusion to Chapter 3

In this Chapter, details on FDSOI technology have been first provided, highlighting the different key elements from 28nm to 14nm derivations.

Then, a special focus has been made on the strain integration in FDSOI. Especially, high level of compressive stress is achieved by integrating SiGe by the means of the condensation technique. The SiGeOI layer is then patterned in order to define the active area. The introduction of a free boundary condition on the active edge has been evidenced to cause stress relaxation. The relaxation of patterned SiGeOI has been experimentally observed by NBED and DFEH measurements and has also been confirmed by µRaman measurements on patterned SiGe stripes. The strong relaxation can not be explained by mechanical simulations considering elastic relaxation. The results suggest a specific behavior of the interface between the strained crystal and the amorphous BOX.

An empirical model of stress relaxation has been proposed. The model also takes into account the stress generated by SiGe:B source and drain. This model allows the layout effects of pFETs from 14nm FDSOI technology to be reproduced. A focus has been made on V_{TLIN} and I_{ODLIN} electrical parameters since the threshold voltage and the mobility are strongly impacted by the level of stress in the device. A good agreement with experimental data is achieved on a large set of layouts (symmetric, asymmetric, non-rectangular and multifinger).

The longitudinal stress relaxation is highly detrimental for 14nm FDSOI pFET performance, increasing V_T and degrading the mobility. That is why devices built on short active area (or gate fingers close to an active edge) show poor performance. In the next Chapter, different solutions to overcome the strain-induced layout effect are investigated.

CHAPTER 4

Performance boosters for SiGeOI pMOSFETs

Contents

4.1 Introduction to chapter 4

In the previous chapter, the local layout effects induced by the introduction of SiGe in the pMOSFET channel have been detailed and modeled. Especially for the case of the 14nm FDSOI technology embedding SiGe directly on insulator, the strain relaxation length is in the order of magnitude of the nominal device active area dimensions. A significant loss of performance is thus observed for short active area devices. In this chapter, both technological and design solutions are investigated in order to **recover the performance**.

Firstly, assuming that the process integration scheme is already defined, **design solutions** are evaluated. These solutions aim at increasing the overall performance without changing the process integration scheme. In this context, two approaches have been assessed. The first one, so-called "Mix-V_T", consists in exploiting the different V_T flavors offered by the technology. The second approach, which requires more interactions with the process, involves designing the standard cells on a continuous stripe of active area. Hence its name "Continuous-RX". Consistently with the Continuous-RX approach, the integration of SiGe in Static Random Access Memory cell is also investigated.

Secondly, as design solutions present some drawbacks, **technological solutions** demanding to tune the process are investigated. The first approach aims at reducing the SiGe strain relaxation. The so-called "SiGe-last" integration scheme, in which the SiGe channel is fabricated after the STI module, is deeply assessed. Finally, a Dual Isolation by Trenches and Oxidation (DITO) scheme is presented. This isolation scheme aims at optimizing the stress configuration.

4.2 Design solutions

4.2.1 Intra-cell V_T-mixing

4.2.1.a Principle

When designing an inverter, the nFET and pFET drivability must be balanced. If it is not the case, the "slow" FET will limit the speed while the leakage will be governed by the "fast" one[1]. Obviously, an optimized cell achieves the highest speed at the lowest leakage. Historically, this was achieved by using a pFET of larger width to compensate for the lower hole mobility with respect to the electron mobility. By introducing SiGe channel in some of sub-20nm CMOS technologies, the hole mobility is now similar to the one of electron. Therefore, the pFET and nFET widths are the same in inverters of 14nm FDSOI technology. Such designed cell is balanced provided the threshold voltages are aligned.

In Chapter 3, we have seen that the patterning of the active area yields a stress relaxation in SiGeOI pFET channel. This relaxation is responsible for layout effects: the threshold voltage of pFET built on a short active area significantly increases in 14nm FDSOI technology. The V_T shift with respect to the nominal device (gate-to-STI distance SA=239nm)[2] is approximately +100mV for the shortest active layout (i.e. SA=59nm). As a result, the pFET and nFET threshold voltages are not aligned at SA=59nm.

Fortunately, this shift is of same order as the difference between two V_T flavors (such as Low-V_T LVT and Regular-V_T RVT). In the 14nm FDSOI technology, these flavors are defined by implantations in the channels. Other possibilities exist such as using a gate stack of different work function, changing the well type or the back-bias configuration. As shown on the transfer characteristics of Figure 4.1, the SA=59nm LVT pFET threshold voltage and thus OFF-current are aligned to the RVT nFET.

The concept of the so-called "Mix-VT" (MIX) approach is to design a cell by combining LVT and RVT devices. Especially, an LVT pFET is combined with an RVT nFET. The layout of the 1-finger inverter for the MIX flavor is illustrated in Figure 4.2. The use of a LVT pFET counterbalances the V_T increase induced by the stress relaxation. This Mix-VT cell aims at replacing the RVT one.

4.2.1.b SPICE simulation results

We investigated the interest of a Mix-VT cell by the means of SPICE simulations using the LETI's 14nm compact model. The layout effects are properly taken into account with the stress-based models of mobility and threshold voltage described in Chapter 3. The LVT and RVT flavors are defined with a V_T shift of 100mV. [3]

Figure 4.3 shows the Leakage/Delay trade-off of the 1-finger inverter (IV-SX1) for the LVT, RVT and MIX flavors. In order to have a speed/leakage trend, an additional V_T variation is added, equally

1 A "slow" ("fast") device features a higher V_T than the typical value (lower, respectively). A "slow" device has low speed and leakage. On the opposite a "fast" device has high speed and leakage.
2 Refer to the layout of Figure 3.40 for a definition of the gate-to-STI distance SA.
3 The intrinsic performance (mobility and access resistance) of LVT and RVT are assumed to be strictly the same. This allows to focus on threshold voltage effects.

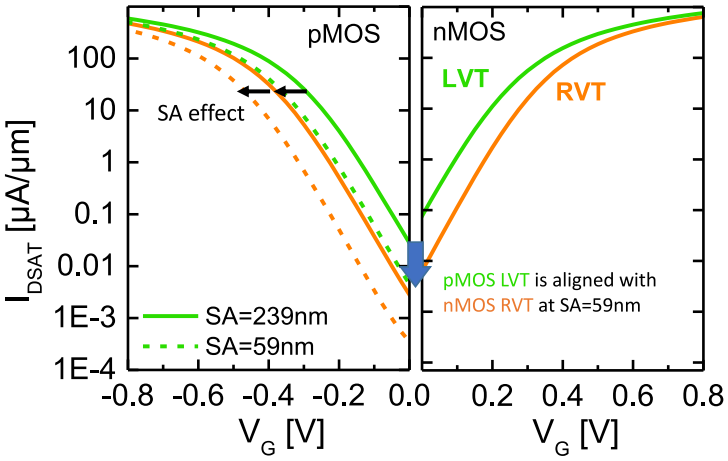


Figure 4.1: Experimental transfer characteristics of the two V_T flavors at V_{DD}=0.8V. Because of the V_T increase induced by stress relaxation, the LVT pFET is aligned with the RVT nFET at SA=59nm.

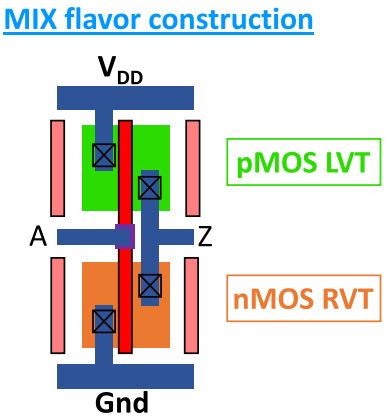


Figure 4.2: Layout of the 1-finger inverter for the MixVT flavor. The use of a LVT pFET compensates for the V_T increase due to the stress relaxation for short active.

to nFET and pFET. This additional variation can be thought as a process variation between the FF (Fast-Fast) and SS (Slow-Slow) corners. This allows a fair comparison between the assessed V_T flavors at same leakage. If not specified, the benchmark is realized under the following conditions of reference:

- ◊ The supply voltage V_{DD}=0.8V.
- ◊ The cells are loaded in a Fan-Out 3 configuration.
- ◊ The R/C network for the back-end is 200Ω/3fF.

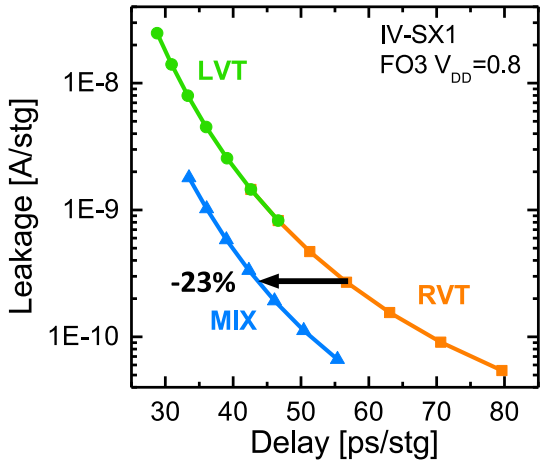


Figure 4.3: Simulated Leakage/Delay trade-off for a 1-finger inverter (IV-SX1) at $\mathbf{V_{DD}=0.8V}$ and for different flavors: LVT, RVT and MIX. The trend is obtained by simulating different V_T variations, equally to nFET and pFET. A -23% delay reduction at the same leakage is observed with the MIX flavor compared to RVT.

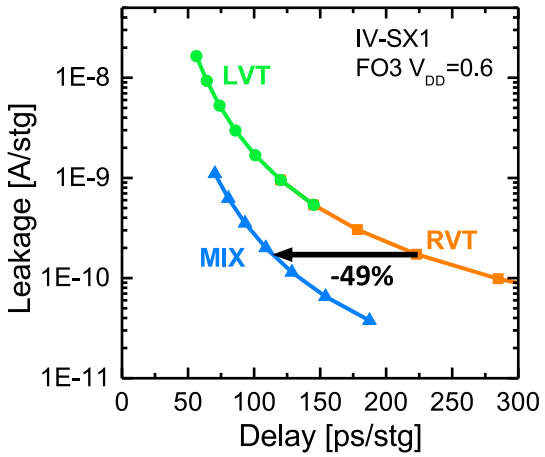


Figure 4.4: Simulated Leakage/Delay trade-off for 1-finger inverter (IV-SX1) at $\mathbf{V_{DD}=0.6V}$ and for different flavors: LVT, RVT and MIX. The MIX flavor delay is expected to be reduced by -49% at the same leakage with respect to RVT flavor. At low supply voltages, the gate overdrive (V_{DD}-V_T) is decisive. Hence the strong interest to have balanced threshold voltages.

The Mix-VT flavor yields -23% delay reduction at the same leakage with respect to the RVT flavor. Combining an LVT pFET and an RVT nFET is thus highly relevant for the 1-finger inverter. The increase of V_T due to the SiGeOI stress relaxation is well compensated for, resulting in a more balanced cell.

The MixVT flavor is even more relevant at low supply voltage, as emphasized in Figure 4.4. At V_{DD}=0.6V, the MIX flavor delay is expected to be reduced by -49% at the same leakage with respect to RVT flavor. The reason for the higher gain at low supply voltage is that the performance is basically proportional to the gate overdrive, V_{DD}-V_T. At low V_{DD}, the speed is thus more sensitive to a V_T shift.

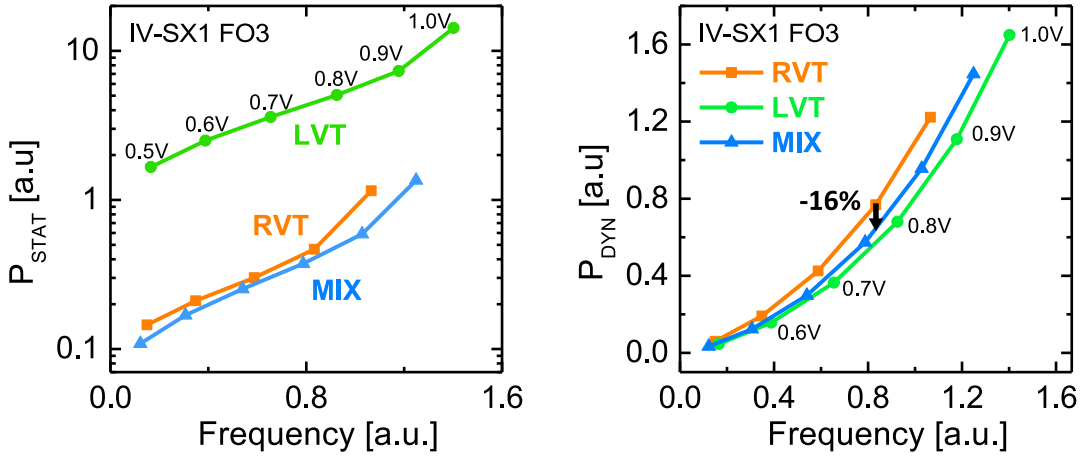


Figure 4.5: (left) P_{STAT} and (right) P_{DYN} *vs.* Frequency for RVT, LVT an dMIX flavors for different V_{DD}. The MIX flavor has similar P_{STAT} to RVT and achieves -16% dynamic consumption at same frequency.

Figure 4.5 shows the static power ($P_{STAT} = I_{DDQ} \cdot V_{DD}$) and dynamic power ($P_{DYN} = I_{DYN} \cdot V_{DD}$) according to the frequency for varying supply voltages. From RVT to MIX, the RVT pFET is replaced by a LVT one. One could expect a higher P_{STAT} because of pFET leakage increase. However, RVT and MIX show same P_{STAT}. This shows that the RVT leakage is governed by the nFET, because the RVT pFET V_T is too high due to stress effect. MixVT finally leads to -16% P_{DYN} at same frequency compared to RVT.

The IV-SX1 is obviously the inverter the more impacted by the stress effect because it features the shortest active area. Nevertheless, the gate fingers located close to the active edges are subjected to stress relaxation in all of the standard cells, whatever their active lengths[1]. Figure 4.6 shows the delay gain induced by MIX-flavor at same leakage according to the inverter drive (i.e. number of fingers SX). MIX flavor is relevant for 2-finger and 3-finger inverters, achieving -15% and -8% delay reduction at same leakage, respectively. As expected, the higher the drive of the cell (i.e. the more fingers), the less gain from switching the RVT pFET to a LVT one. For the IV-SX4, the MIX flavor shows same leakage/delay trade-off as LVT and RVT ones. This is because such a cell with an active length of several CPPs is almost perfectly balanced. Eventually, for long active layout standard

1 This has been discussed on layout effect of multifinger devices (Figure 3.60).

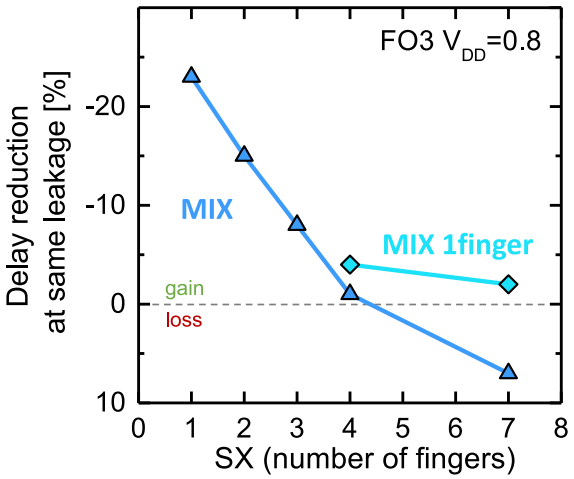


Figure 4.6: Delay gain at same leakage according to the inverter drive (SX, i.e. number of fingers). The higher drive, the lower gain because of longer active area. MIX flavor is even irrelevant for IV-SX7, degrading the delay by 7%. The MIX 1finger flavor (see Figure 4.7) improves the speed of IV-SX4 and IV-SX7.

cells, the MIX flavor will have exactly the opposite effect of what it was aimed at. A long active cell has indeed been designed to be balanced. The stress relaxation in SiGeOI pFET has low impact on the whole cell. Changing the pFET from RVT to LVT this time results in an unbalanced cell. Such a MixVT cell suffers from the high leakage of the LVT pFET and the low performance of the RVT nFET. This is verified for the MIX 7-finger inverter (L_{act}=658nm) showing +7% delay increase (Figure 4.6).

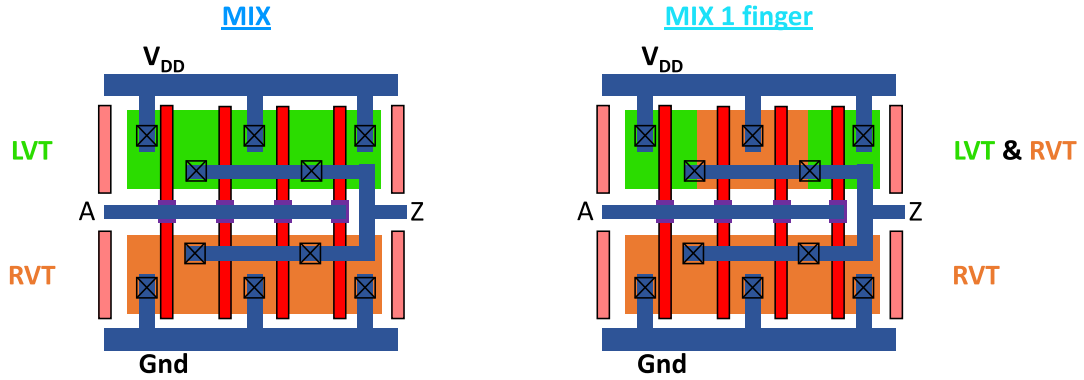


Figure 4.7: Illustration of the "MIX 1finger" flavor, consisting in changing the RVT pFET fingers close to the active edge to LVT. These fingers are the one the more impacted by the SiGeOI stress relaxation. This can be done by an implant mask for example.

Nevertheless, the gate fingers located close to the active edges are always impacted by the stress relaxation. It can be relevant to compensate the stress effect on these fingers only. This can be easily achieved when flavors are defined by an implant, as illustrated in Figure 4.7 on the layout of IV-SX4. The "MIX 1finger" consists in changing the RVT pFET into LVT only for the fingers the closest from the active edge, i.e. one finger on each side. This way, the V_T of all the pFET transistors are re-aligned. This MIX 1finger solution leads to -4% and -2% delay reduction at the same leakage for IV-SX4 and IV-SX7, respectively, as shown in Figure 4.6.

In such a MIX 1finger configuration, one could have a doping area (or a non-doping area) of only one CPP. This might not satisfy the design rules related to the implants. Regarding the gain achieved compared to the specific design rules that could emerge with such a MIX 1finger construction, this

solution might not be worth it.

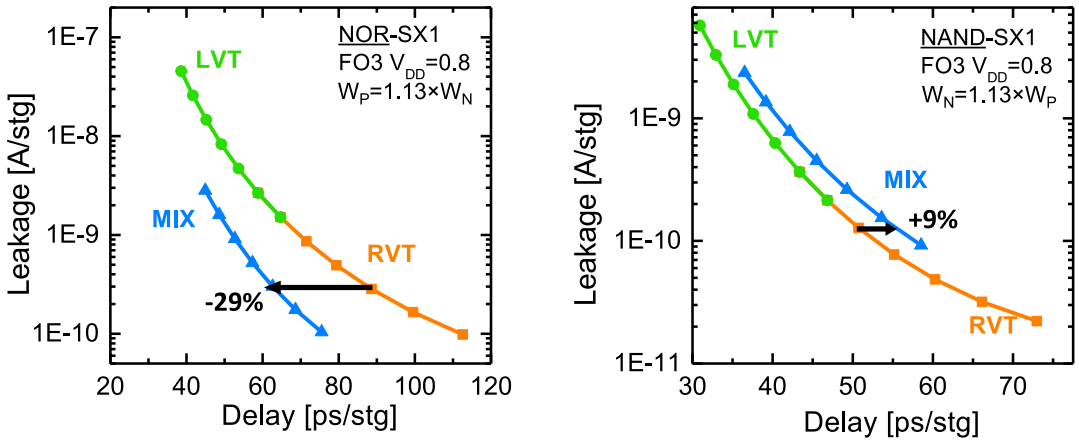


Figure 4.8: (left) NOR-SX1 and (right) NAND-SX1 simulated Leakage/Delay trade-off for the different VT flavors. The MIX flavor reduces the NOR delay by -29% at the same leakage. The NOR logic gate features pFET in series. Hence it is more sensitive to the leakage of the nFET and the speed of the pFET. Reducing the pFET V_T in such a cell improves the speed without a strong leakage penalty. It is the opposite for the NAND logic gate: the MIX flavor is thus irrelevant in this case.

Figure 4.8 shows the Leakage/Delay trade-off for NOR and NAND logic gates. The NOR gate features pFET in series and nFET in parallel while it is the opposite for the NAND gate (see section 1.1.1.b). The NOR and NAND gates are simulated under the inverter configuration, that is to say the inputs A and B are equivalent (which corresponds to the worst case). Such cells are intrinsically off-balance: the leakage is governed by the FET type built in parallel and the speed is more sensitive to the performance of the FET type built in series. In order to optimize the drivability of these cells, the most efficient knob is the width ratio W_n/W_p. In the 14nm FDSOI technology, the FET type in series is 13% larger than the FET type in parallel in order to compensate for the stacking effect. This W-ratio has been chosen to be optimized for the nominal device. Yet the nominal pFET is not significantly impacted by the SiGe stress relaxation. That is why it might be relevant to consider the MIX flavor for low drive cell.

The MIX flavor enables the NOR delay to be reduced by -29% at the same leakage *vs.* RVT. Reducing the pFET V_T in such a cell improves the speed without dramatically increasing the leakage, mainly governed by the nFET. As a consequence, the MIX flavor is highly relevant for this logic gate. The gain is even higher than for IV-SX1, despite a longer active (2 CPPs for IV-SX1 *vs.* 3 for NOR-SX1). However, the MIX flavor degrades the NAND speed/leakage trade-off. This is because the NAND cell is highly sensitive to the pFET leakage. Changing the pFET from an RVT to an LVT significantly increases the leakage along with little speed improvement.

4.2.1.c Mix-VT summary

The Mix-VT cell consists in changing the pFET flavor to a lower-VT to compensate for the strain-induced layout effect. This enables a balanced cell and significantly improves the performance at a given leakage. The 1-finger inverter delay is reduced by -23% in our conditions of reference. However, it does not solve the issue of mobility degradation. In addition, there is no VT flavor available for

replacing the LVT. Nevertheless, this solution comes at no extra cost which makes it highly relevant for managing the layout effect and optimize the performance of the circuit.

4.2.2 The continuous-RX design

4.2.2.a Principle

In the previous section, a design solution has been presented to optimize the performance by the means of a threshold voltage readjustment. However, the strain relaxation is not only responsible for a V_T increase but also for a strong mobility degradation, as widely discussed in Chapter 3. As a result, the effective current at a given leakage (i.e. free from V_T variation) is strongly degraded for short active layouts (Figure 4.9).

The effective current of the shortest active in a Tucked-Under[1] layout scheme (i.e. SA=SB=80nm at CPP=90nm) can be improved by up to +90% at same leakage when the active is lengthened. This highlights the great interest of long active layout designs. A design solution, so-called "Continuous-RX" (CRX)[2], consists in designing the devices on a long stripe of active [Nal14]. By doing so, the active area is not cut in the longitudinal direction, preventing any SiGe stress relaxation. In such a stress-optimized layout, illustrated in Figure 4.10, transistors are isolated by an "isolation-gate".

4.2.2.b Isolation-gate construct

The isolation-gates consist in an OFF-state biased transistor of 26nm gate length. Such gate length is achieved using "poly-bias" that allows to slightly change the gate length at a given CPP (here 90nm).

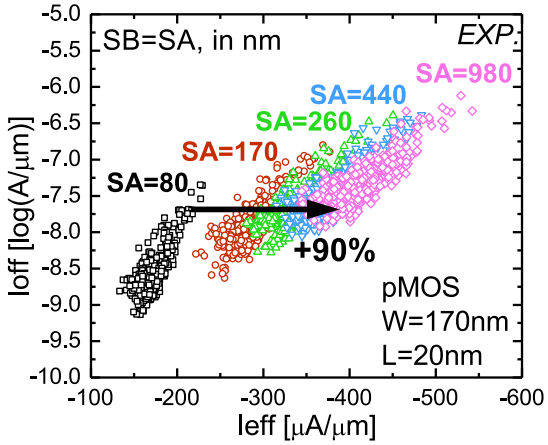


Figure 4.9: pFET I_{EFF}/I_{OFF} at V_{DD}=0.8V and for different gate-to-STI distances (SA). By increasing the active length, the effective current can be improved by up to +90% at the same leakage.

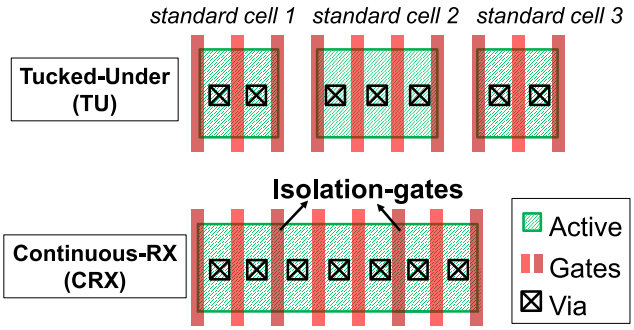


Figure 4.10: Tucked-Under (TU) and Continuous-RX (CRX) layout. Standard cell abutment results in a continuous active area. Isolation-gates are required to prevent leakage between two abutted standard cells.

1 Also called Double-Diffusion-Break (DDB), see Figure 4.10

2 In layouts, the active area layer is often referred as "RX". Hence the name Continuous-RX.

A special layout construct is defined, consisting in a shared contact between the isolation-gate and the source of the adjacent transistor (Figure 4.11). This way, the isolation-gate is connected to the power line, ensuring an OFF-state regime. The short-cut is performed using contact levels (CA/CB[1]) to prevent any Metal1 congestion [Nal14] as shown in the TEM of Figure 4.11.

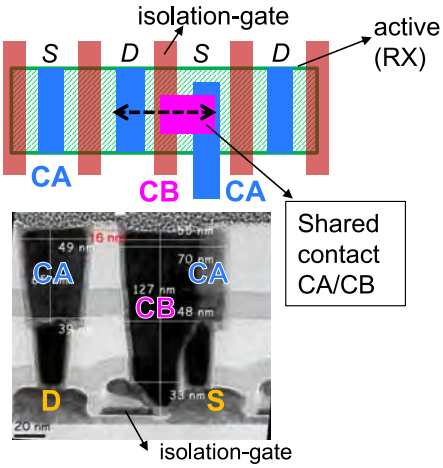


Figure 4.11: Isolation-gate layout construct and associated TEM image showing the shared contact.

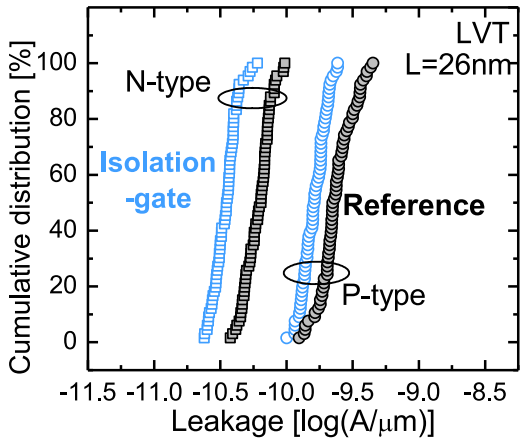


Figure 4.12: Cumulative distribution of the isolation-gate OFF-state leakage compared to reference.

The OFF-leakage of this isolation-gate is measured at a similar level as a reference transistor connected without the special construct (Figure 4.12). This ensures a good isolation between two adjacent devices.

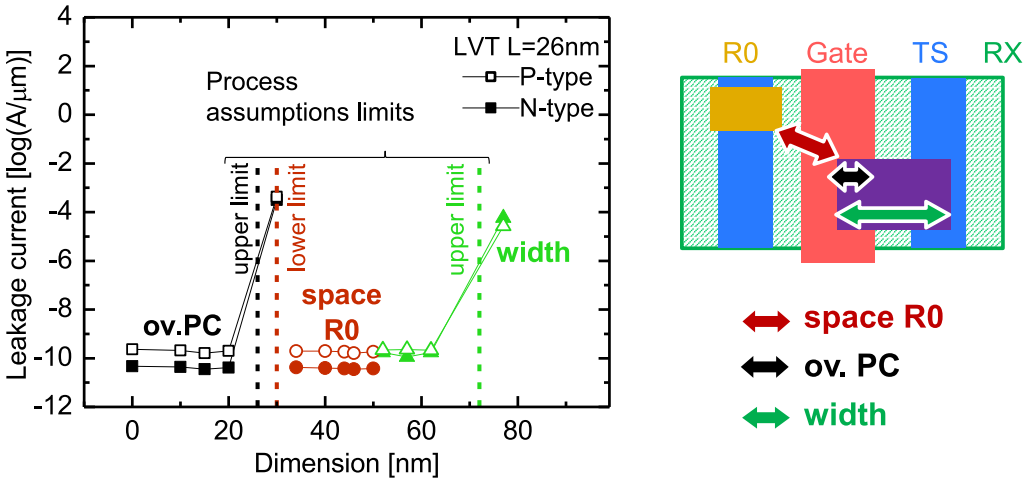


Figure 4.13: Isolation-gate leakage *vs.* critical dimension variation. No short-cut under process assumptions demonstrating the optimization of the design rules (width of the contact, distance to via and overlap on poly).

The critical design rules related to this isolation-gate (contact overlap on poly, width and distance to vias) demonstrate no short-cut failure under process assumption limits (Figure 4.13).

1 CA is the layer relative to the contacts on actives (i.e. source and drain of transistors) and CB is the layer relative to the contacts on poly (i.e. gates). CB are not allowed on actives, except for the dedicated isolation-gate construct.

4.2.2.c CRX performance evaluation

The performance of ring-oscillators with CRX design is compared with Tucked-Under ones in Figure 4.14. CRX designs highlight experimentally a -14% delay reduction at same leakage and nominal V_{DD}=0.8V for 3-gate-finger inverters (IV-SX3) and up to -28% for 1-finger inverters (IV-SX1). 1-finger inverter is more enhanced because it is the cell with the shortest active and thus the one the more impacted by the patterning-induced stress relaxation.

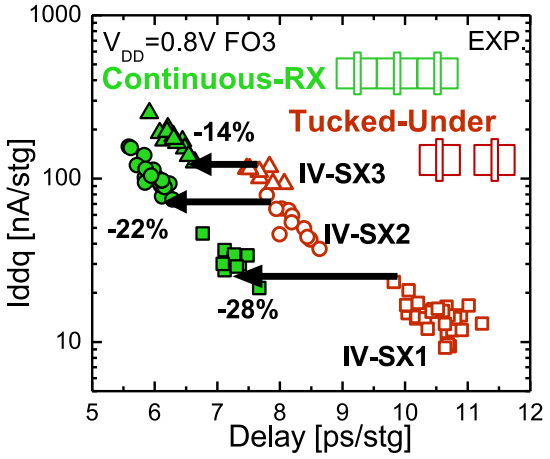


Figure 4.14: Experimental Delay/Leakage trade-off for ring-oscillators of inverters. Continuous-RX designs demonstrate high gain *vs.* Tucked-Under (-28% for 1-finger).

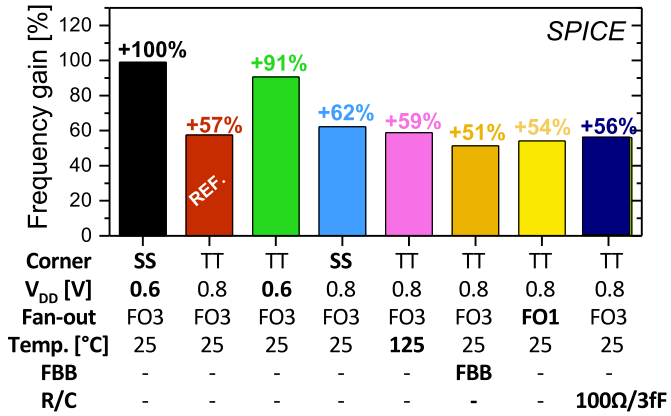


Figure 4.15: Simulated frequency gain expected by CRX design for various conditions. The major impact is V_{DD} reduction.

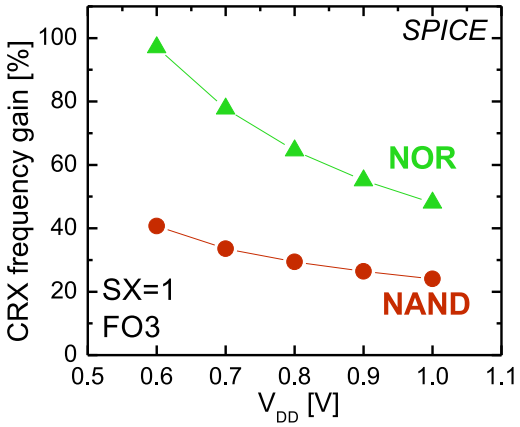


Figure 4.16: CRX frequency gain for NOR and NAND logic gates at different supply voltages. NOR are more impacted because more sensitive to pMOS performance, as they are built in series.

In order to assess more deeply the interest of CRX, the frequency gain has been calculated through SPICE under different conditions independently of the leakage. Results presented in Figure 4.15 shows that the CRX-frequency gain reaches nearly 100% in Worst Case (supply voltage of V_{DD}=0.6V, temperature of T=25°C; and SS[1] corner). Little impact of temperature, Forward Back-Bias FBB, corners, fan-out and back-end RC is observed. The main effect involves the V_{DD} reduction. The introduction of CRX manages keeping the longitudinal stress and thus both a high-mobility and a

1 SS stands for Slow Slow. It means that both nFET and pFET threshold voltages are higher than their nominal value, because of global process variations.

low-V_T. Both contribute to high pMOS current, mainly at low-V_{DD}, where gate-overdrive (V_{DD}-V_T) is decisive. This low-V_T along with the isolation-gate OFF-state current are responsible for higher leakage in CRX designs, as experimentally observed in Figure 4.14.

The standard cells that are the most improved are the NOR gates because of pMOS in series, as shown in Figure 4.16, and low-drive gates because of short active (dotted lines of Figure 4.23).

Finally, the interest of the Continuous-RX has been evaluated for a critical path of an A9 core. The critical path is made of several logic gates. All devices of each logic gate have been assumed to have a continuous active, i.e. infinite SA and SB values. By doing so, the frequency is improved by +15% with respect to the Tucked-Under reference case (Figure 4.24). This evaluation has been done before implementation, i.e. place and route has not been performed.

4.2.2.d The impact of RX-jogs

If transistors of different widths are designed on the same stripe of active area, RX-jogs are created. In this case, the active is not rectangular, as illustrated in Figure 4.17.

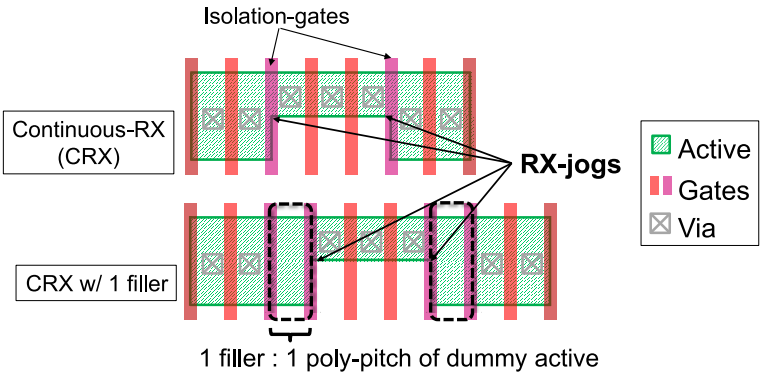


Figure 4.17: Layout of CRX in presence of RX-jogs, without and with a filler cell.

RX-jogs introduce a partial relaxation, as evidenced by finite element simulations (Figure 4.18). In this Figure, the RX-jog ratio ω is fixed at $\omega = 0.5$. The RX-jog ratio is defined as the width ratio of abutted transistors, as illustrated in Figure 4.19. The partial relaxation induced by RX-jogs strongly impact the performance. For instance, I_{ODLIN} is degraded by -35% at $\omega = 0.73$ (Figure 4.20). This is well predicted by the model (please refer to Chapter 3 and especially to section 3.4.3). In turn, the delay of ring-oscillators of 1-finger inverters is degraded by +21% for ω=0.66 (all inverters are at the same RX-jog), as presented in Figure 4.21.

4.2.2.e The interest of a filler cell

Not only the RX-jogs directly degrade the performance but they are also a source of variability. The performance of a standard cell now depends on the active width of its neighbor cells. The cell abutment in the Continuous-RX design is thus responsible for performance variability.

In order to optimize the performance/variability induced by cell abutment, a filler cell of 1 poly pitch width (CPP=90nm) can be introduced between the two abutted cells, without density loss compared to Tucked-Under designs (Figure 4.19). Such an abutted filler cell improves pMOS $I_{ODLIN}(\omega)$ (Figure 4.20). Especially, +20% is achieved at ω=0.5, almost reaching the performance of rectangular CRX ($\omega = 0$).

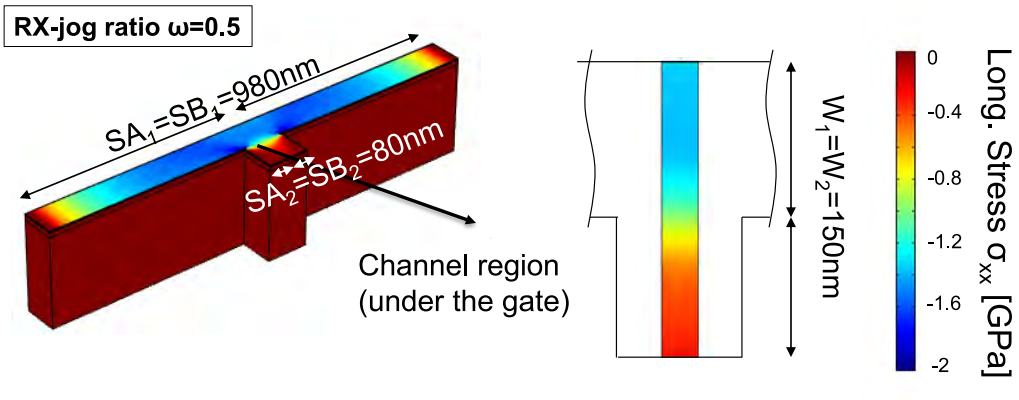


Figure 4.18: Mechanical simulation of an active area with RX-jog showing a partial stress relaxation.

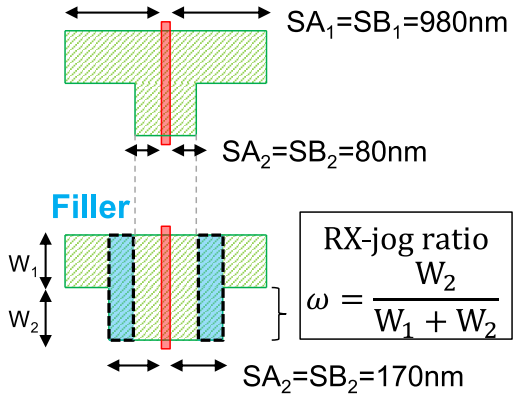


Figure 4.19: Schematics and definition of RX-jog ratio ω and dedicated test structures (with and without filler cell).

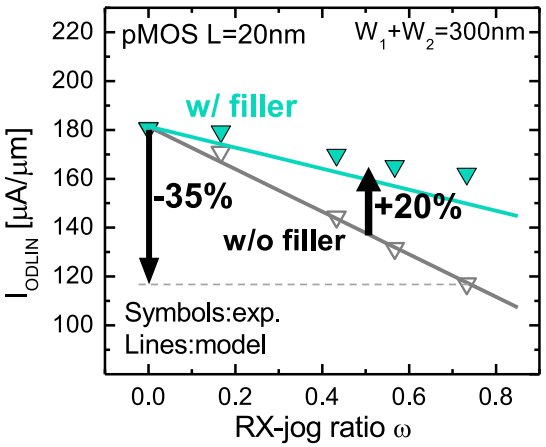


Figure 4.20: I_{ODLIN} as a function of the RX-jog ratio ω with or without filler cell. Using a filler cell enables a higher stress in the channel, which is translated into a higher mobility.

As far as ring-oscillators are concerned, SPICE simulations predict +16% frequency gain at $\omega = 0.5$ for IV-SX1 (Figure 4.22). At a high RX-jog ratio of $\omega = 0.75$, the abutment-induced frequency degradation is reduced from 28% to 11% for IV-SX1 (which is the cell the most impacted). For the other cells investigated at $\omega = 0.5$, the use of a filler leads to almost the same performance as for rectangular CRX (i.e. "ideal" CRX), as shown in Figure 4.23. This demonstrates the efficiency of the filler cell to reduce the performance variability induced by standard cell abutment. Regarding the critical path, the use of a filler improves the gain obtained by CRX *vs.* TU from +7% to +10% at $\omega = 0.5$ (Figure 4.24).

4.2.2.f Continuous-RX: summary

The continuous-RX approach consists in designing the transistors on a long stripe of active area. This way, the longitudinal stress in pFET SiGeOI channel is maintained. High performance gains are experimentally achieved (-28% delay for IV-SX1) and predicted by simulations. Nevertheless, such a design requires the introduction of isolation-gates, responsible for an additional leakage current. Also, the associated special construct demands a good process control. In addition, the presence of

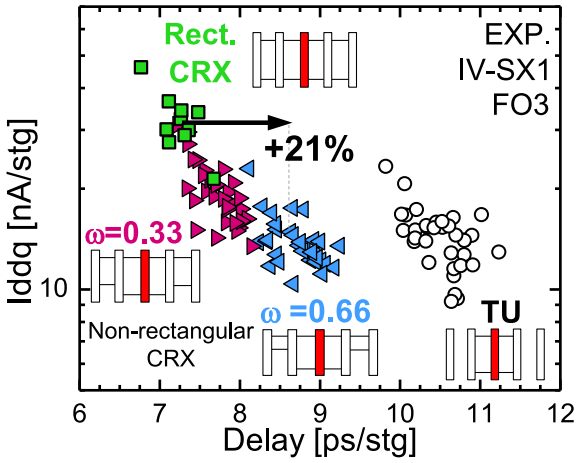


Figure 4.21: Delay/Leakage trade-off of 1-finger inverters with different RX-jog ratios. The higher the RX-jog ratio, the more the performance is degraded. This is due to the partial stress relaxation.

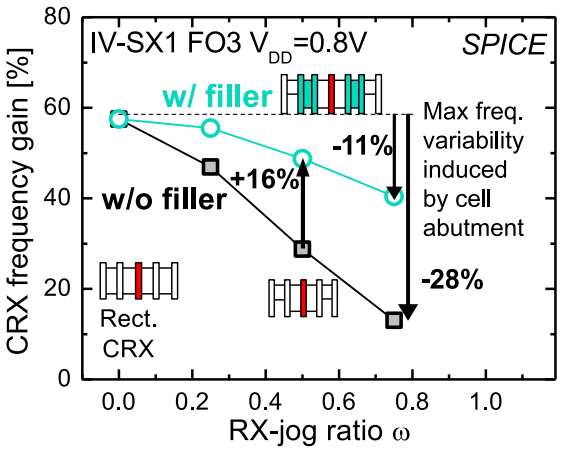


Figure 4.22: Simulated CRX frequency gain for IV-SX1 as a function of the RX-jog ratio showing the interest of a filler cell to limit the variability induced by standard cell abutment.

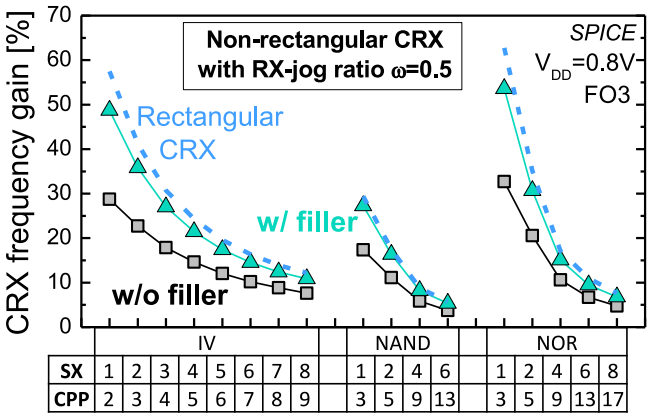


Figure 4.23: Simulated CRX gain for different standard cells (IV/NAND/NOR of different drive) with RX-jog ratio $\omega = 0.5$ compared to rectangular CRX (i.e. $\omega = 0$). The introduction of a filler cell yields gains close to ideal rectangular CRX.

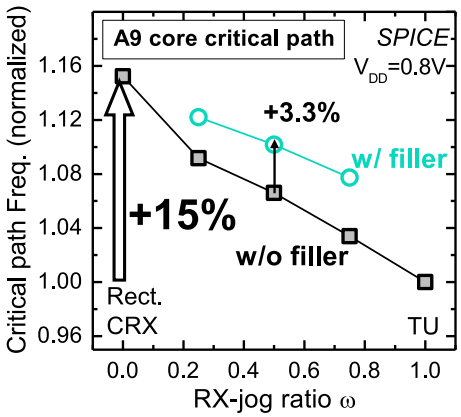


Figure 4.24: CRX frequency gain for a critical path of an A9 core according to the jog ratio (considered to be the same for each standard cell of the critical path). The relevance of a filler cell introduction is translated by +3.3% freq at ω=0.5.

RX-jogs yields a partial relaxation, translated into performance degradation. Consequently, standard cell abutment rises as a new source of variability. The performance indeed depends on the width of the neighbor cells. The introduction of a filler cell of active is an efficient way to reduce this effect, with a low penalty on density.

4.2.3 Design solution benchmark

In order to optimize the performance by managing the layout effect induced by SiGeOI relaxation, two design solutions have been investigated: the Mix-VT (MIX) and the Continuous-RX (CRX) approaches.

Figure 4.25 benchmarks them with the help of SPICE simulations. The studied standard cell is the

1-finger inverter (IV-SX1), which is the more impacted by layout effects. In the "ideal RVT", the SA/SB parameters are assumed to be infinite, i.e. the longitudinal stress is maintained. This is also the case for the CRX configuration but the isolation-gates are also taken into account (by using a transistor whose source and gate are connected to the ground for nFET and to the power supply for pFET).

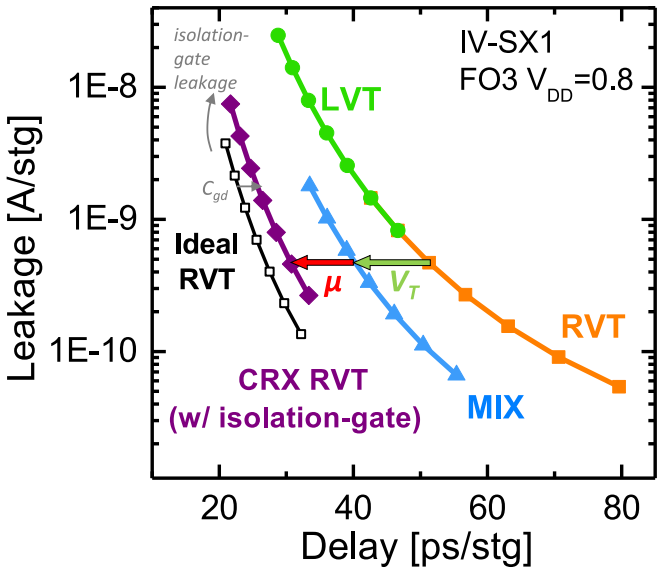


Figure 4.25: Iddq/τ_p trade-off of IV-SX1 at V_{DD}=0.8V simulated from SPICE for different design configurations. By re-balancing the V_T, the MIX approach yields a reduced delay with respect to reference RVT cell. The performance is however lower than the CRX approach because of the degraded mobility. The CRX performance is close to ideal. The increase of leakage is due to the isolation-gate and the performance loss is due to increased parasitic capacitance.

Mix-VT solution enables to re-balance the RVT standard cell, by compensating the V_T increase for short active. However, applying this solution to LVT cells requires a dedicated doping and thus an additional mask. In addition, such an approach does not fix the issue of the mobility degradation.

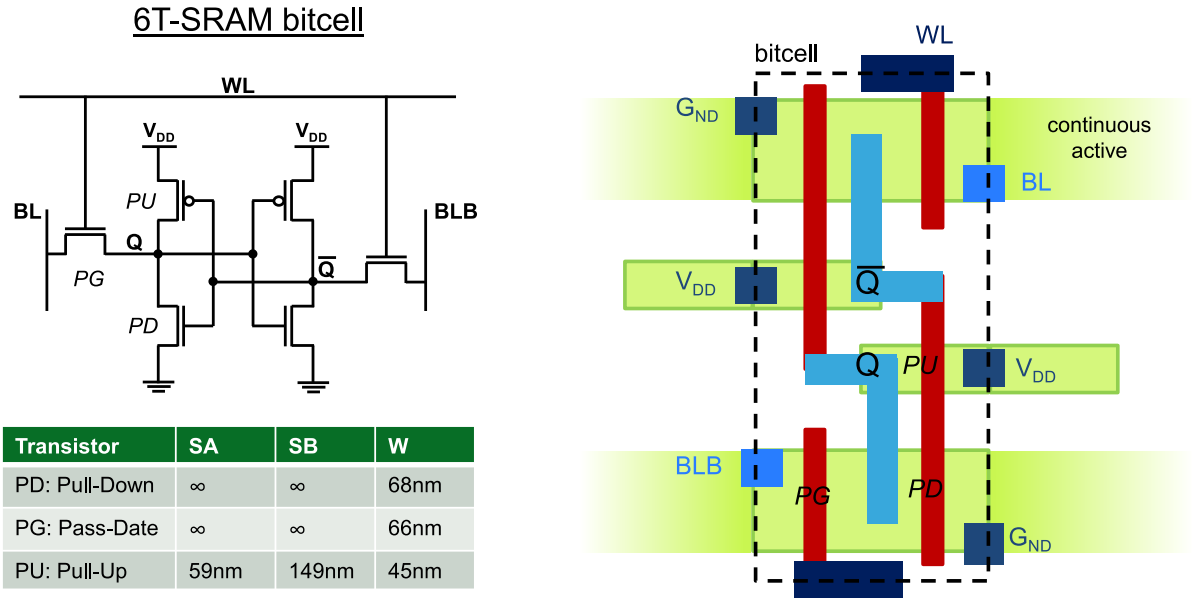
For performance purpose, the Continuous-RX approach is highly efficient. The Continuous-RX performance is close to the ideal case because it allows the longitudinal stress to be maintained. The increase of leakage is due to the isolation-gate which consists in a parasitic transistor in OFF state. The slight performance loss of CRX *vs.* the ideal case is due to an increased parasitic capacitance. Especially, the gate-to-drain capacitance C_{GD} of the isolation-gate contributes to the effective capacitance to be loaded by the inverter.

The CRX leakage and parasitic capacitance are not a dramatic issue to be solved. The presence of RX-jogs however might be, especially considering the variability induced by standard cell abutment.

4.2.4 SiGe introduction in FDSOI SRAM bitcells

4.2.4.a Introduction

In this section, a focus is made on Static Random Access Memory (SRAM) cells. The SRAM cell consists in two cross-coupled inverters, made of Pull-Up (PU, pFET) and Pull-Down (PD, nFET) transistors. In addition, two Pass-Gate transistors (PG, nFET) are used to access the bitcell for either a read or a write operation. The SRAM operation is described in appendix B. In order to maintain a good stability, two criteria have to be respected. Firstly, the PD must be stronger than the PG. This allows a reading operation without altering the stored bit. Secondly, the PG must be stronger than the PU, in order to be able to write a bit. Especially, a "0" will be written instead of a "1" when the Pass-Gate will be ON (i.e. WL=V_{DD}). These criteria impose the width ratios between the 3 different transistors operating in an SRAM cell.



Transistor	SA	SB	W
PD: Pull-Down	∞	∞	68nm
PG: Pass-Date	∞	∞	66nm
PU: Pull-Up	59nm	149nm	45nm

Figure 4.26: 6T-SRAM (left) schematic and (right) typical layout. An SRAM cell consists in two cross-coupled inverters made of Pull-Down (PD) and Pull-Up (PU) and two access transistors, also called Pass-Gate (PG).

Figure 4.26 shows a schematic and a layout of a typical SRAM bitcell. The PG and PD are designed on the same stripe of active. On the other hand, the PU is fabricated on a small island shared between two adjacent bitcells.

In the reference SRAM cell from 14nm FDSOI technology, the PU pFET channel is made of Silicon, for V_T targeting purpose. In this section, the introduction of SiGe in SRAM is discussed according to two configurations. The use of a SiGe channel is first briefly investigated in the classical SRAM cell. Then, a focus is made on a so-called CSRAM cell (Complementary-SRAM).

The results of this section are obtained by the means of SPICE simulations. As for the previous section, the layout effect inherent to SiGe channel are taken into account by the means of the model described in Chapter 3 (especially in section 3.2.3). The different SRAM metrics extracted from our testbench are the Static Noise Margin (SNM), the Write Noise Margin (WNM), the write

current (I_{WRITE}), the read current (I_{READ}) and the stand-by leakage current ($I_{LEAKAGE}$). All of these parameters are static figures of merit. The extraction is detailed in appendix B.

4.2.4.b SiGe in classical SRAM

As we have seen in Chapter 3, the introduction of SiGe in the pFET channel has two major impacts on the transistor characteristics: the threshold voltage and the mobility are modified. As far as the threshold voltage is concerned, it is impacted by both the stress and the presence of Germanium (apart from the SiGe stress). The two effects are taken into account with a stress sensitivity of $|S_{stress}|$=100mV/GPa and a Germanium sensitivity of $|S_{Ge}|$=6mV/% (the higher the compressive stress and the higher the Ge content leads to lower $|V_T|$). The mobility is modeled using the piezoresistive coefficients and the stress relaxation model of section 3.2.3.

%Ge =	0%=REF	10%	20%	25%
SNM [mV]	**147**	170	189	196
WNM [mV]	**336**	333	289	232
I_W [µA]	**31**	28	23	20
I_{READ} [µA]	**17**	17	17	17
$I_{leakage}$ [pA]	**23**	36	358	1677

Figure 4.27: SRAM metrics at V_{DD}=0.8V for different Germanium concentrations in the PU. Introducing Ge improves the SNM due to the PU V_T reduction, at the expense of leakage increase and loss of write ability.

Figure 4.27 shows the results of the reference SRAM cell (i.e. $x_{Ge} = 0$) and compare it to SRAM cells with different Ge concentrations in the PU channel. The leakage of the bitcell is strongly impacted by the introduction of SiGe since the V_T of the PU is lowered. The SiGe introduction reinforces the PU. The PG>PU criterion for write operation is weakened. As a result, both the WNM and the write current I_W are degraded by the introduction of SiGe. On the other hand, the SNM is improved thanks to the lower PU V_T.

%Ge =	0%=REF	25%
ΔV_T,p [mV]	**0**	+250
SNM [mV]	**147**	153
WNM [mV]	**336**	324
I_W [µA]	**30.6**	29.7
I_{READ} [µA]	**17.4**	17.4
$I_{leakage}$ [pA]	**23**	24

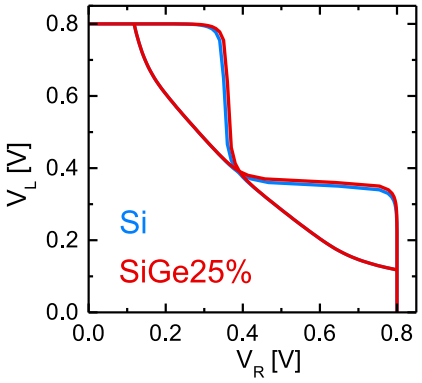


Figure 4.28: (left) SRAM metrics for Si and $Si_{0.75}Ge_{0.25}$ PUs at same leakage, obtained thanks to an additional V_T shift of $\Delta V_{T,p}$=+250mV and (right) SNM butterfly curve at V_{DD}=0.8V. No significant impact of SiGe because of the strong stress relaxation in the small active area of PU.

In order to benchmark the SRAM at the same leakage, an additional threshold voltage shift $\Delta V_{T,p}$ is

used for the PU. Figure 4.28 compares the results of the reference SRAM with a cell featuring 25% of Germanium in PU channel. The additional V_T shift in the $Si_{0.75}Ge_{0.25}$ SRAM is $\Delta V_{T,p}$=+250mV (i.e. slower) to recover the leakage. The different metrics of such SRAM cell with SiGe are almost similar to the one of the reference. This can be explained by the fact that the PU active area is small (i.e. short SA, SB and narrow W, see Figure 4.26). The SiGe PU is thus strongly impacted by the relaxation, resulting in similar hole mobility in Si and in SiGe and in turn in similar SRAM metrics.

Despite the low mobility enhancement, the introduction of Germanium can be an efficient way to adjust the threshold voltage. However, this can be a new source of variability, which is decisive for SRAM cell stability. In order to first-order evaluate the impact of the Germanium concentration fluctuation, we introduce an additional global variability parameter σ_{Ge}. This parameter relates the Germanium concentration variation on the wafer and from wafer to wafer. It is thus a source of global variability, as opposed to local variability (i.e. mismatch from stochastic variations). The σ_{Ge} value is assumed to be 1%, which is translated into a threshold voltage deviation of σ_{VT}=13mV. Such a value is based on ellipsometry measurements for a Germanium concentration around 25%. It is worth noting that this variation is assumed to be uncorrelated to the SiGe film thickness. However, the Germanium fluctuation after the condensation process can also be induced by film thickness variation. Especially, a thinner SOI leads to a more concentrated SiGe film because of the Ge dose conservation. Nevertheless, the thinner the SiGeOI, the higher the V_T [Maz14]. This will thus counterbalance the V_T reduction due to higher Ge concentration. By neglecting this effect, our assumption of Ge fluctuation is attributed to the epitaxy variation and can be seen as a worst case.

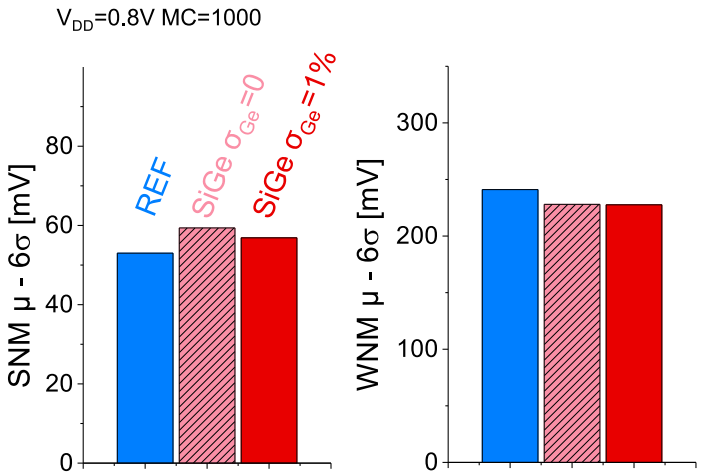


Figure 4.29: SRAM (left) SNM and (right) WNM $\mu - 6\sigma$ at V_{DD}=0.8V after 1000 Monte Carlo simulations. Considering an addional source of variability for Ge concentration fluctuation does not impact the margins as the SRAM cell is more sensitive to local variability than global one.

Figure 4.29 shows the results of 1000 Monte Carlo simulations of SRAM cells at V_{DD}=0.8V. The SRAM cells considered are the reference and the SRAM with SiGe at 25% of Ge in the PUs, both cells featuring the same leakage. The Ge concentration fluctuation does not significantly impact the SNM and WNM $\mu - 6\sigma$ figures of merit. This is due to the fact that SRAM cells are more sensitive to local variations than global ones.

4.2.4.c Complementary SRAM

In the classical SRAM cell, in order to satisfy the PD>PG and PG>PU criteria, the PDs and PGs consist in nFETs while the PUs are pFETs. This is because the electron mobility is higher than the hole mobility in Silicon. However, by introducing SiGe in the pFET channel, the hole mobility can be greatly enhanced, especially under the relevant stress configuration. In the previous section (4.2.2), the Continuous-RX design has been demonstrated to be highly relevant for logic cell performance since it provides the best stress configuration for <110>-oriented SiGe channel pFETs, i.e. longitudinal stress. As observed on the layout of Figure 4.26, a similar continuous active area is present in SRAM cells for the PG and PD.

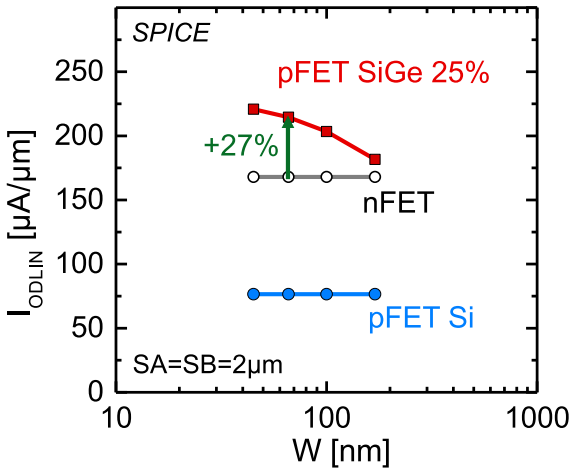


Figure 4.30: I_{ODLIN} *vs.* active with W from SPICE model at SA=SB=2µm and L=20nm. The introduction of SiGe leads higher hole mobility than electron, especially for short active area featuring the optimized longitudinal stress configuration. As a result, SiGe pFET I_{ODLIN} is expected to outperform nFET by +27% at W=66nm.

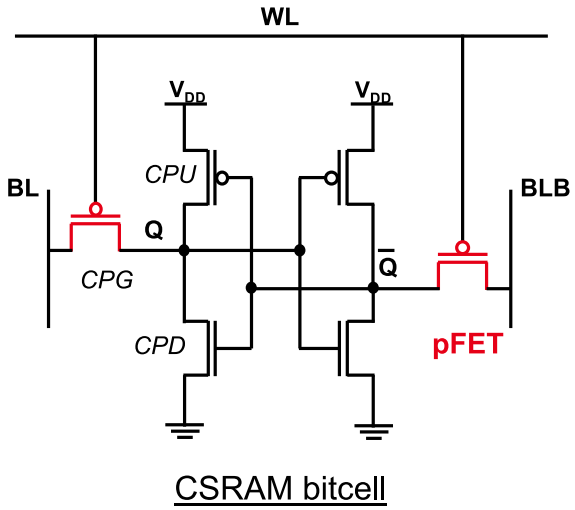


Figure 4.31: Complementary SRAM (CSRAM) bitcell layout. The Pass-Gates consist in pFETs instead of nFETs as in the reference. Such a CSRAM bitcell operates reversely to a classical SRAM: the read operation criterion becomes CPU>CPG and the write one becomes CPG>CPD.

In this section, the use of pFETs for Pass-Gates instead of nFETs is investigated. Figure 4.30 shows the simulated $I_{ODLIN}(W)$ behavior for both nFET and pFET, highlighting that $Si_{0.75}Ge_{0.25}$ pFET outperforms Si nFET for long and narrow active. Especially, +27% is expected at W=66nm, which is the active width of the Pass-Gate in our SRAM cell.

The SRAM cell with pFETs as Pass-Gates is called Complementary SRAM (CSRAM) and is presented in Figure 4.31. In such CSRAM cell, the transistors are referred as CPG, CPD and CPU for Complementary Pass-Gate, Complementary Pull-Down and Complementary Pull-Up, respectively. The operation of the bitcell is reversed. Especially, the WL=1 for retention and the bit lines are precharged to '0' instead of '1' for a read operation. The criterion PD>PG for reading becomes CPU>CPG and the PG>PU one for writing becomes CPG>CPD. As a result, the CPG and CPU, which are pFETs, are designed on the continuous active stripe, similarly to the Continuous-RX approach. This results in an optimized stress configuration (SA=SB=∞).

Figure 4.32 shows both the read and write currents as a function of the leakage of the cell. In order to

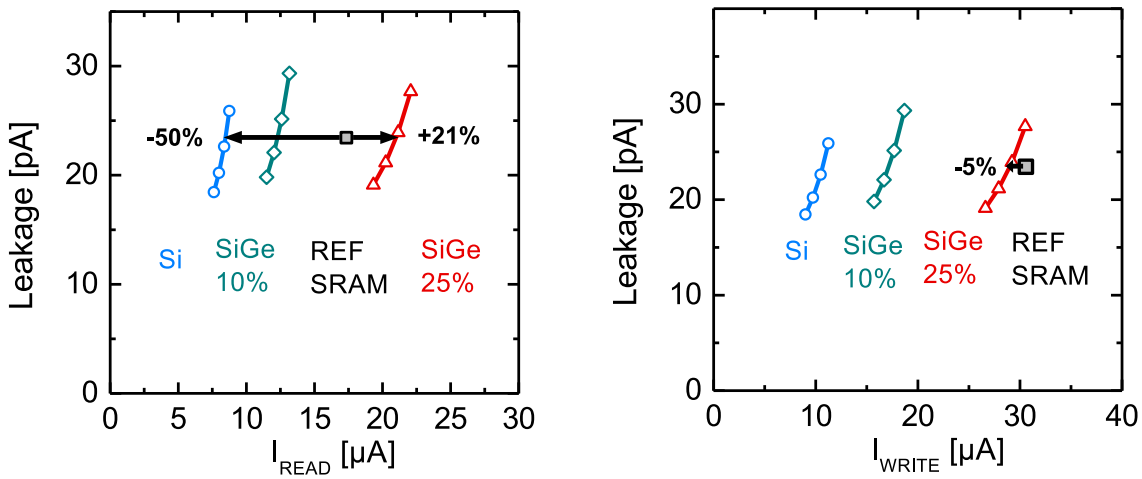


Figure 4.32: (left) Read current and (right) write current *vs.* cell leakage for different SRAM configurations at V_{DD}=0.8V. The $Si_{0.75}Ge_{0.25}$ CSRAM read current outperforms the reference SRAM by 21% thanks to the higher hole mobility w.r.t. electron.

compare the different cells at same leakage, an additional V_T re-targeting is necessary to compensate for the impact of SiGe. This allows a fair comparison, focusing on mobility effects. The CSRAM is obviously not relevant with Silicon channel, the read current being degraded by -50% with respect to the reference. By integrating SiGe however, the mobility gain significantly improves the SRAM operations. The higher the Germanium concentration, the higher the read and write currents. With 25% of Germanium, the read current of the CSRAM is enhanced by +21% with respect to the SRAM reference. This is due to the higher hole mobility than electron, making it relevant to use pFETs for Pass-Gates.

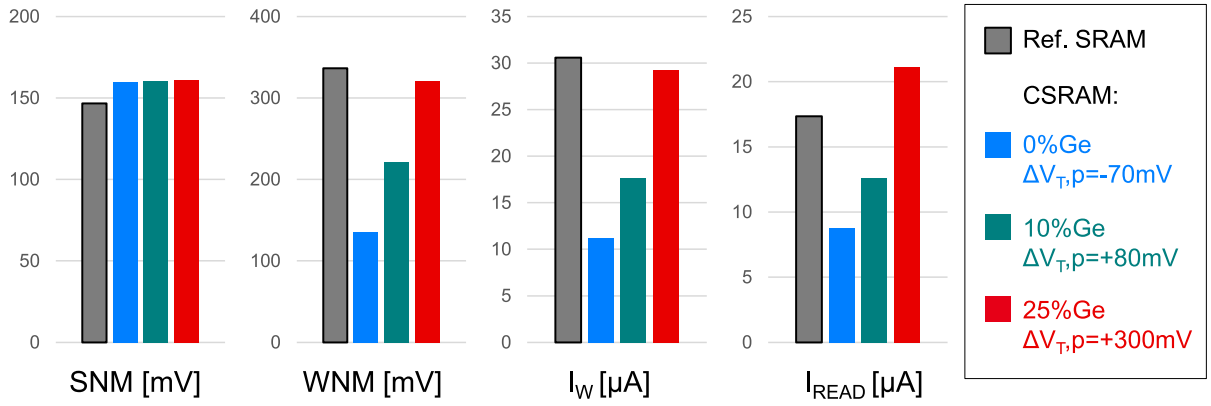


Figure 4.33: Reference SRAM and CSRAM metrics at V_{DD}=0.8V, benchmarked at same leakage obtained by an additional V_T shift, given in the legend. CSRAM improves the read current without significantly altering the other parameters.

Figure 4.33 summarizes the different SRAM metrics at same leakage. Despite the gain achieved on read current with 25% of Germanium, the write operation of the CSRAM cell is slightly degraded with respect to the reference SRAM (lower WNM and I_W). In the classical SRAM, the hole mobility in Si PU ($\mu_{h,Si}$) is low compared to the one of electron in PG ($\mu_{e,Si}$), ensuring a high PG>PU ratio. In the CSRAM, the hole mobility in the CPG ($\mu_{h,SiGe}$) is highly enhanced by SiGe integration. But

the mobility in the CPD is the one of electron. We can write:

$$\frac{\mu_{h,SiGe}}{\mu_{e,Si}} < \frac{\mu_{e,Si}}{\mu_{h,Si}} \tag{4.1}$$

which results in CPG>CPD ratio not as strong as the PG>PU one. Nevertheless, the WNM and I_W losses are not significant compared to the gain on the read current. In order to further optimize the CSRAM write ability, the width of the CPD could be reduced. This would also improve the density of CSRAM bitcells.

The V_T shifts required to achieve same leakage are given in Figure 4.33. At 25% of Ge, the pFET V_T shift to compensate for the introduction of SiGe is +300mV. Such a shift might be challenging to achieve. From the SRAM device construction, several changes can be made to meet this target. The pFET back-plane can be changed to N-type in a dual well configuration (i.e. regular-well), leading to approximately +80mV V_T shift. In addition, such a configuration allows the pFET to operate in Reverse-Back-Bias mode, i.e. $V_{B,p}$>0. This would also help the pFET V_T to be increased. If the V_T reduction induced by SiGe integration can not be totally compensated for, the CSRAM bitcell could still be relevant for a different application demanding more performance, at the expense of higher leakage.

As far as the variability is concerned, the distributions of CSRAM SNM and WNM after 1000 Monte Carlo simulations are shown in Figure 4.34. The considered Germanium concentration fluctuation ($\sigma_{Ge} = 1\%$) does not impact the CSRAM variability even though in such a configuration, 4 transistors out of 6 are pFETs. This is due to a low impact of global variability with respect to local one in SRAM, as already discussed in the previous section.

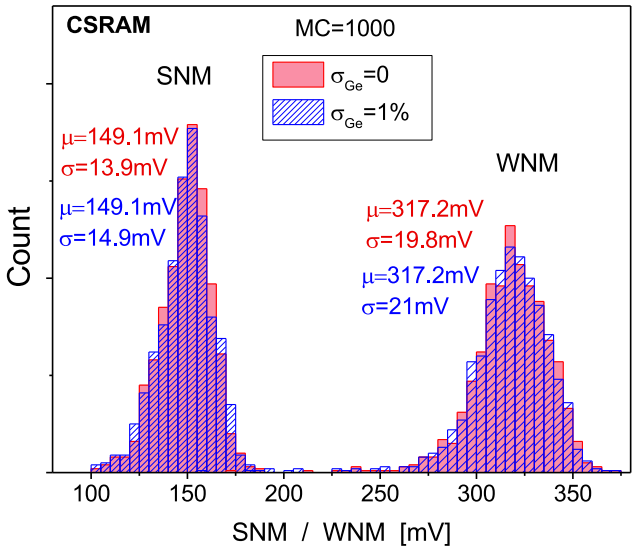


Figure 4.34: CSRAM SNM and WNM distributions at V_{DD}=0.8V with and without considering Ge concentration fluctuation.

4.2.4.d Conclusion

In this section, we have discussed the introduction of SiGe in SRAM bitcells. Especially, the mobility gain induced by the compressive stress makes it relevant to design a Complementary SRAM bitcell. In such a configuration, the Pass-Gates are made of SiGe pFETs. The operation of the SRAM is

reversed. It is expected to enhance the read current by +21% with respect to reference at same leakage. The Germanium concentration fluctuations are not expected to significantly impact the SRAM yield. However, the strong V_T reduction induced by SiGe integration must be considered. It might be the bottleneck for the realization of low leakage CSRAM cells. Nevertheless, the CSRAM bitcell could enlarge the SRAM offer by proposing high current bitcell, at the expense of leakage. Besides, the low threshold voltage of such CSRAM bitcell could make it suitable for low power supply voltage.

4.3 Technology solutions

4.3.1 The SiGe-last approach

In this section, an alternative integration scheme for the introduction of SiGe in pFET is investigated. The process of reference, described in section 3.1, is called "SiGe-first" as the SiGe channel is fabricated prior to the active patterning and the Shallow Trench Isolation (STI) module. A partial relaxation of the strain arises from the etching step and is responsible for strong layout effects, as discussed in Chapter 3.

4.3.1.a Process integration

The assessed alternative integration consists in a bilayer SiGe/Si formed after the STI module. Hence it is called "SiGe-last". In the latter, the Si film is thinned down to approximately 2nm so that the total thickness of the bilayer is comparable to the SiGe-first process.

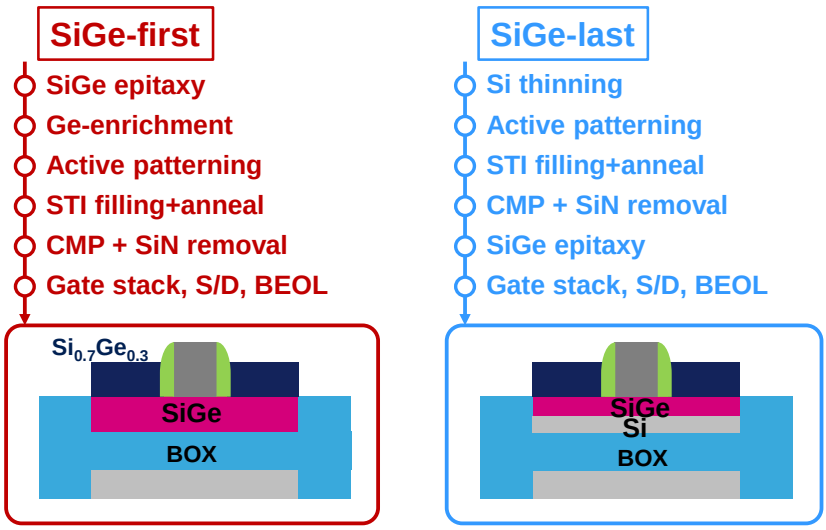


Figure 4.35: Process flow of SiGe-first and SiGe-last integration schemes. The SiGe-first integration scheme, i.e. the process of reference, uses the condensation technique prior to the active area patterning. On the opposite, the SiGe-last process consists in an epitaxy after the STI module, leading to a SiGe/Si bilayer.

The two process flows are detailed in Figure 4.35. It should be emphasized that the SiGe-last process does not include any condensation step (contrarily to the work of Cheng et al. [Che12]). An oxidation after patterning would result in lateral consumption and therefore active narrowing. In addition, skipping the condensation allows the HF budget (for oxide removal) to be reduced post STI formation.

Figure 4.36 shows the Energy-dispersive X-ray spectroscopy (EDX) mappings performed at the end of the complete CMOS integration. It highlights the presence of a Si layer in the SiGe-last approach. On the contrary, in the SiGe-first process of reference, a uniform Ge concentration is obtained over the film thickness. This is due to the high-temperature STI anneal after condensation that allows Si-Ge interdiffusion. The EDX scan over the channel thickness presented in Figure 4.37 shows a slightly lower maximum Germanium concentration in the $Si_{1-x}Ge_x$ channel for the SiGe-last

(x_{last}=20%) than for the SiGe-first process (x_{first}=25%). Also, a slight Ge concentration gradient is evidenced for the SiGe-last case.

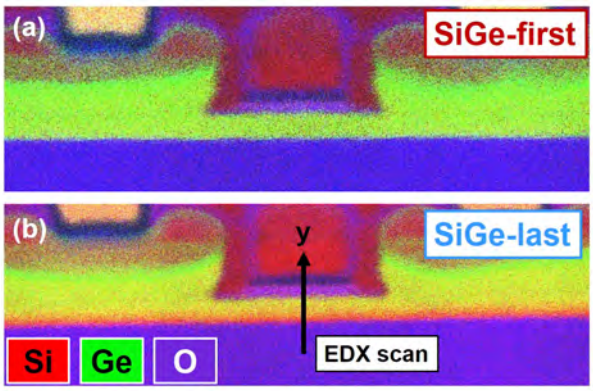


Figure 4.36: Energy-dispersive X-ray spectroscopy (EDX) mapping of (a) SiGe-first and (b) SiGe-last at the end of the process flow. A SiGe/Si bilayer is evidenced in the SiGe-last approach.

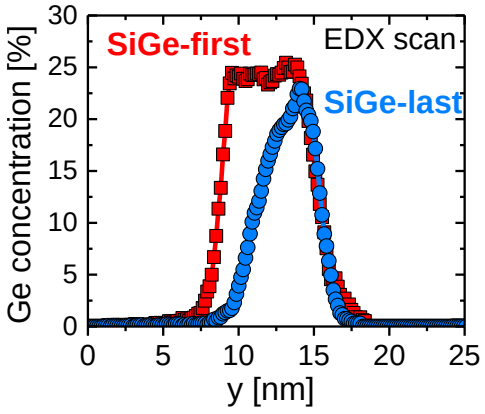


Figure 4.37: EDX scan of SiGe-first and SiGe-last accross the channel thickness (see Figure 4.36). The bilayer of SiGe-last is evidenced with x_{last}=20%, while SiGe-first Ge concentration is x_{first}=25%.

4.3.1.b Layout effects

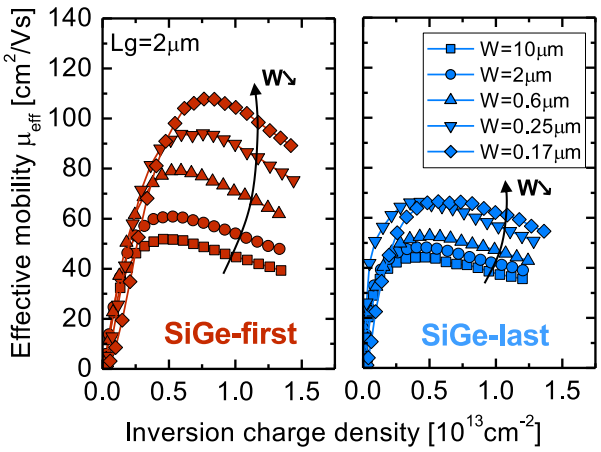


Figure 4.38: Hole effective mobility as a function of the inversion charge density for SiGe-first (left) and SiGe-last (right) for a long channel device (L=2µm) and for different channel widths W.

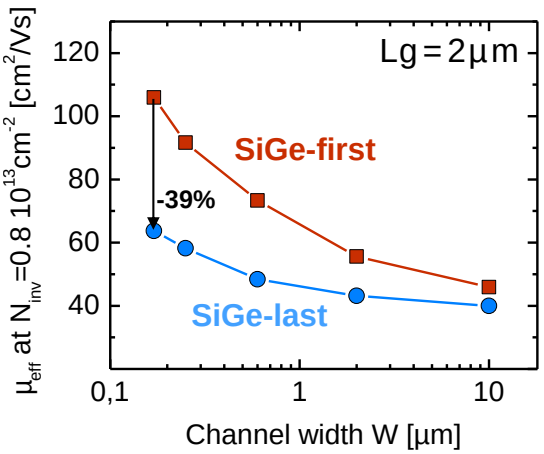


Figure 4.39: Long channel hole effective mobility at N_{inv}=0.8 $10^{13}cm^{-2}$ according to the channel width. Gain from biaxial to uniaxial stress configuration is higher for SiGe-first than for SiGe-last.

The hole mobility of <110>-oriented long channels (L=2µm) extracted by the split-CV method for different channel widths W is presented in Figure 4.38. For both processes, the hole mobility increases with the reduction of the channel width. This improvement is the consequence of the transverse stress relaxation occurring at the active edges. The stress configuration changes from biaxial for large active regions to uniaxial for narrow ones. Since the uniaxial longitudinal compressive stress is highly beneficial, the mobility is strongly improved by such a relaxation (as discussed in Chapter 3 and especially in section 3.4.3).

Figure 4.39 shows the mobility extracted at an inversion density of N_{inv}=0.8 $10^{13}cm^{-2}$ as a function

of the channel width (W). The mobility gain is lower for SiGe-last, leading to -39% μ_{eff} at W=170nm compared to SiGe-first. Similar result was already reported in the literature and assumed to be related to the SiGe morphology [Che12]. In our case, the SiGe-last approach does not exhibit any condensation process. Our result rather suggests a higher relaxation of the detrimental transverse stress for SiGe-first. To confirm this hypothesis, the layout effects have been investigated in the X-direction (i.e. the longitudinal source/drain direction) on layouts with variable gate-to-STI distances (SA, see insert Figure 4.40), while the channel length remains constant (L=20nm). The threshold voltage shift ΔV_T with respect to the long active configuration (SA=959nm) is plotted as a function of the gate-to-STI distance SA in Figure 4.40. ΔV_T is higher at a given SA for SiGe-first than SiGe-last. This result is consistent with the effective mobility dependence with active width of Figure 4.39, suggesting a lower stress relaxation in case of SiGe-last integration.

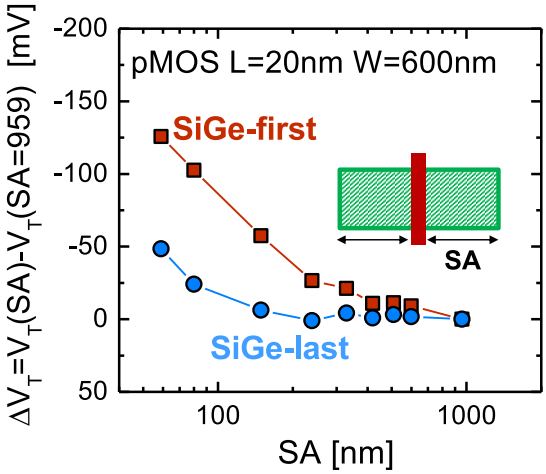


Figure 4.40: The threshold voltage shift ΔV_T with respect to the long active configuration (SA=959nm). Higher V_T shift is observed for SiGe-first compared to SiGe-last.

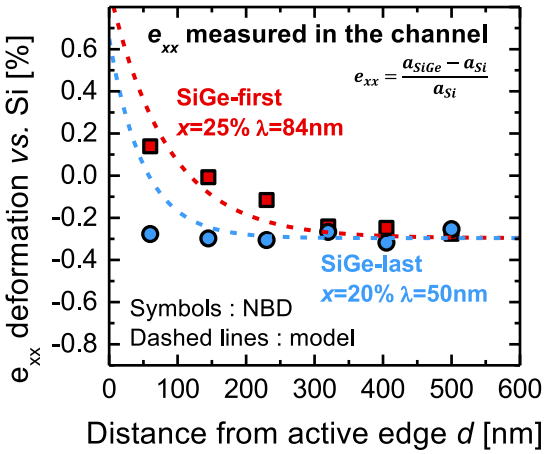


Figure 4.41: Deformation *vs.* Silicon reference e_{xx} measured by Nano-Beam Electron Diffraction (NBED) below the dummy gate and at the end of the process as a function of the distance from the active edge d. Higher strain relaxation for SiGe-first compared to SiGe-last is evidenced.

Nano-Beam Electron Diffraction (NBED) has been performed on both types of SiGe integration at the end of the process flow. As discussed in section 3.2.1, it is sensitive to the difference of lattice parameter between the SiGe layer and the Silicon substrate. The relative deformation e_{xx} is reported in Figure 4.41. The deformation is measured in the middle of the SiGe channel, below the dummy gates, as a function of the distance d from the active edge (located at $d = 0$). The negative value $e_{xx} = -0.3\%$ is the consequence of the additional compressive strain induced by $Si_{0.7}Ge_{0.3}$:B source/drain (detailed in section 3.3.1). The SiGe-first deformation measured below the three dummy gates located close to the active edge is impacted by the relaxation. It is not the case for the SiGe-last integration where the strain is maintained even for the closest dummy gate from the active edge. This strain characterization is is agreement with Figures 4.40 and 4.39: the SiGe-last approach features a lower relaxation on active edges than SiGe-first.

When comparing the SiGe-first and SiGe-last integrations, a crossover behavior is observed on I_{ODLIN}(SA) (Figure 4.42). For long active (SA>200nm), the SiGe-first I_{ODLIN} is higher than the

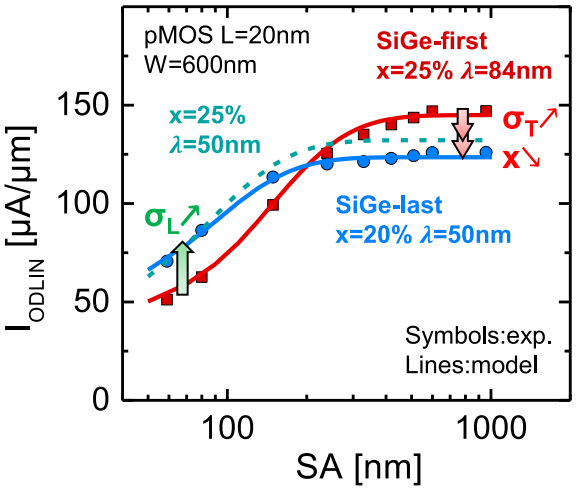


Figure 4.42: I_{ODLIN} *vs.* SA for SiGe-first and SiGe-last (W=600nm and L=20nm). Crossover is explained by both the lower intial stress from lower Ge concentration and the lower typical relaxation length in SiGe-last.

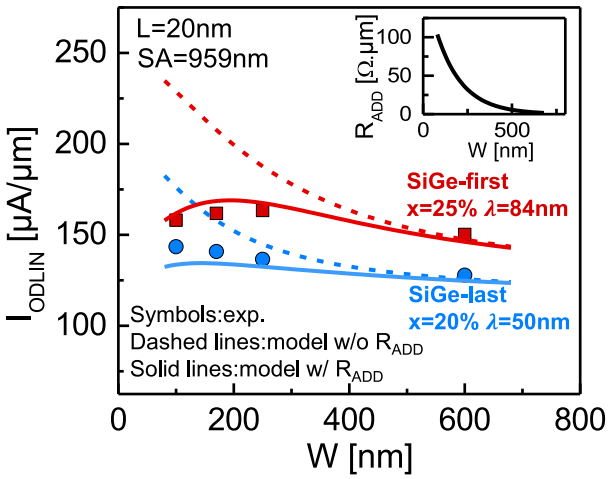


Figure 4.43: I_{ODLIN} *vs.* W for SiGe-first and SiGe-last short channel devices (L=20nm). The model well reproduces the behaviors if an additional series resistance is considered for both integrations. The additional access resistance is attributed to faceted source/drain epitaxy, as discussed in section 3.4 (Figure 3.44).

SiGe-last one, while it is the opposite for short active regions. This crossover behavior is the consequence of different stress-induced layout effects. At long SA, both SiGe-first and SiGe-last are not impacted by the longitudinal stress relaxation because the channel is located far enough from the active edge. The I_{ODLIN} difference is due to two factors. First, the SiGe-last integration features a slightly lower Germanium concentration (20% *vs.* 25%, see Figure 4.37) leading to lower initial stress. Secondly, the transverse stress, which is detrimental, is higher for SiGe-last (see Figures 4.38 and 4.39). Therefore, SiGe-last I_{ODLIN} at W=600nm is degraded compared to SiGe-first for long active layout. However, for short active layouts, the lower longitudinal stress in SiGe-first leads to lower I_{ODLIN}. The dependence of I_{ODLIN} *vs.* layout is reproduced by the model presented in section 3.2.3. It is found that the typical relaxation length λ is strongly reduced with the SiGe-last integration (λ = 50nm *vs.* λ = 84nm). The model prediction assuming the relaxation length of SiGe-last (λ = 50nm) and the Germanium concentration of SiGe-first (25%) is also shown in dashed lines. A crossover with the reference SiGe-first is also predicted with such a configuration. This is because of the opposite effect of longitudinal and transverse stresses. The different relaxation behavior is also observed on the W-effect for short channel devices (L=20nm) with long active (SA=959nm) where the longitudinal stress is maintained (Figure 4.43). The W-trend observed on long channel mobility (Figures 4.38 and 4.39) is not that important on short channels. A possible explanation could be an additional series resistance (R_{ADD}) for narrow devices. By considering a unique R_{ADD}(W) trend (insert Figure 4.43), the model well reproduces the I_{ODLIN} behavior of both integration schemes. This R_{ADD} may be attributed to faceted source/drain epitaxy, as discussed in section 3.4 (see Figure 3.44).

4.3.1.c Experimental performance

Focusing on performance, Figure 4.44 shows the I_{EFF}/I_{OFF} trade-off of W=170nm active width and L=20nm gate length transistors for two gate-to-STI distances SA=59nm and SA=239nm. For short active (SA=59nm), I_{EFF} increases by +21% with SiGe-last integration thanks to the higher longitudinal stress. However, for SA=239nm, I_{EFF} decreases by -9%, mostly due to the higher transverse stress. This result is consistent with the previously discussed crossover in Figure 4.42.

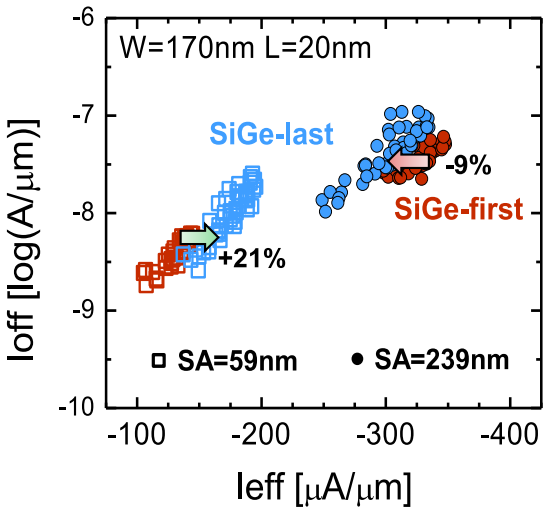


Figure 4.44: Experimental I_{EFF}/I_{OFF} trade-off demonstrating higher performance of SiGe-last for short active (SA=59nm) but lower perf. for long active (SA=239nm) regions at L=20nm gate length and W=170nm active width

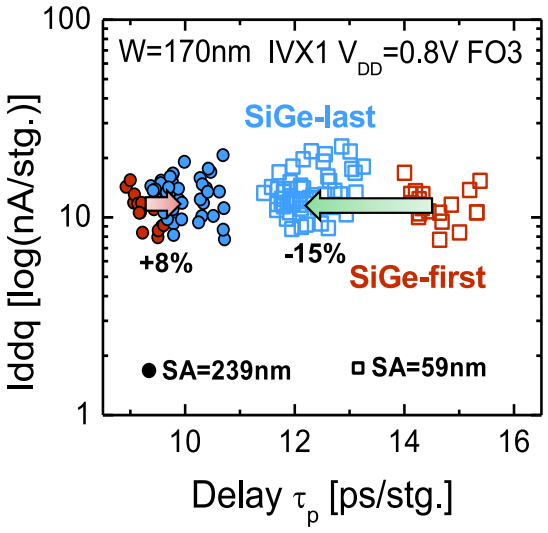


Figure 4.45: Experimental I_{DDQ}/τ_p of a inverter ring oscillator of inverter (IVX1, L=20nm, W_n=W_p=170nm, V_{DD}=0.8V) loaded with a fan-out 3. It demonstrates a delay increase with SiGe-last for long active regions (+8% for SA=239nm) and a delay reduction for short active (-15% for SA=59nm)

The strong layout dependence is also observed on the delay of ring-oscillators of 1-gate-finger inverters (Figure 4.45). The delay increases by +8% for SA=239nm long active. However, for short active (SA=59nm), which is the design of highest density, the delay is reduced by -15% with SiGe-last integration.

4.3.1.d Discussion

In this section, an alternative integration flow for SiGe channel pFETs in FDSOI has been presented. By fabricating the SiGe after the STI module, i.e. after the active area patterning, without condensation step, the strain lateral relaxation is significantly reduced. There are several hypotheses to explain the reduced relaxation:

- ◊ A different mechanical behavior of the unstrained-SOI/BOX interface with respect to the strained-SiGe/BOX one. This assumption would be consistent with the different strain relaxation observed with µRaman measurements (section 3.2.4);
- ◊ The thinner SiGe layer in SiGe-last than in SiGe-first;
- ◊ The STI could prevent the relaxation since there is no free boundary condition when the SiGe

is grown in SiGe-last, contrarily to the reference SiGe-first process.

In any case, a reduced relaxation does not necessarily imply a performance enhancement. The relevance of this integration is strongly layout-dependent: short actives are improved while long ones are degraded.

Such an integration scheme might be interesting for finFET or stacked-nanowire fabrication since the transverse stress is totally relaxed in such narrow devices. However, these devices are more susceptible to be fabricated on bulk rather than SOI substrate. In this case, they will not undergo the high relaxation peculiar to SiGe on insulator.

4.3.2 Dual Isolation by Trenches and Oxidation

In the previous section, the SiGe-last integration scheme has been presented. The strain relaxation inherent to SiGe patterning is considerably reduced with such an integration scheme. However, this is not synonym of performance improvement since the transverse stress is detrimental for hole mobility. There is no benefit to avoid the relaxation in this direction. That is why SiGe-first outperforms SiGe-last for long and narrow actives (typically W=170nm and SA=239nm), despite a higher stress relaxation. SiGe-last approach is only relevant for the shortest actives (SA<200nm).

In this section, a novel integration scheme involving a dual isolation is investigated. The aim is to achieve the best stress configuration for <110>-oriented pFET channels, that is to say uniaxial compressive stress. In order to do so, a dual isolation scheme is investigated. We call it DITO for Dual Isolation by Trenches and Oxidation.

4.3.2.a Process integration

The process flow of our dual isolation integration is presented in Figure 4.46, focussing on SiGe channel of pFETs. As in the process of reference, the SiGe layer is fabricated prior to the active patterning by the Ge-enrichment technique. The Germanium concentration is 25% that is to say the initial compressive stress is $\sigma = -1.6$ GPa. The active areas are then defined by two different isolations. This requires two masks, already existing in 14nm double patterning and known as "active" (RX) and "active-cut" (RC) masks.

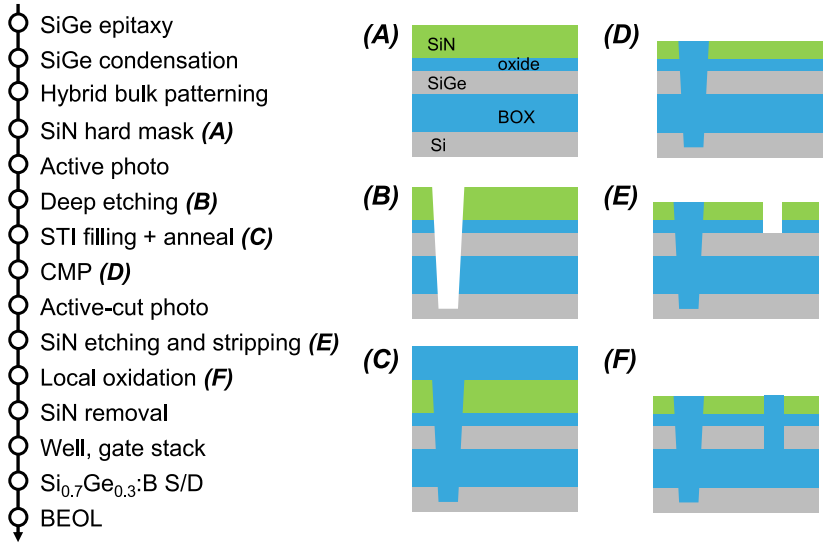


Figure 4.46: Process flow of DITO. The local oxidation is performed after the STI and CMP, reusing the SiN hardmask

Figure 4.47 shows a SEM picture after isolation and illustrates a typical layout with such a dual isolation. We call it "Dual Isolation by Trenches and Oxidation" (DITO) because the STI is used to separate the nMOS active stripes from pMOS ones, while a local oxidation isolation is used to separate adjacent devices of same type. First, the active area is etched in one direction. The STI is then filled. After CMP, the remaining nitride hard-mask on top of the active areas is kept and used for the local oxidation in the other direction. The nitride film is then locally etched using the

active-cut mask. The etch stops on the pad oxide on top of the channel (made of SiGe for pMOS and Si for nMOS) as shown in the TEM picture of Figure 4.48.

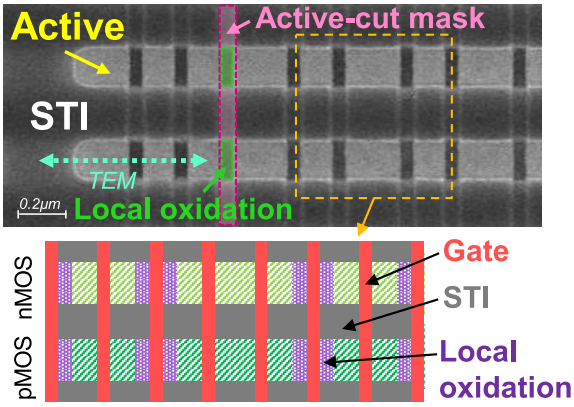


Figure 4.47: SEM top view of the DITO integration scheme after oxidation. Isolation of pMOS stripes from nMOS ones is made with STI while the isolation of transistors within the stripes is made of local oxidation. Corresponding layout is also illustrated showing the "Single-Diffusion-Break" scheme.

The local oxidation of the film until the BOX is then performed at a temperature below the melting point of Germanium. The process used is a Rapid Thermal Oxidation at 900°C for 540 seconds[1]. This isolation by oxidation is similar to the LOCOS process [App70]. It is used to avoid the SiGe layer etching, and thus to prevent any stress relaxation from the edges.

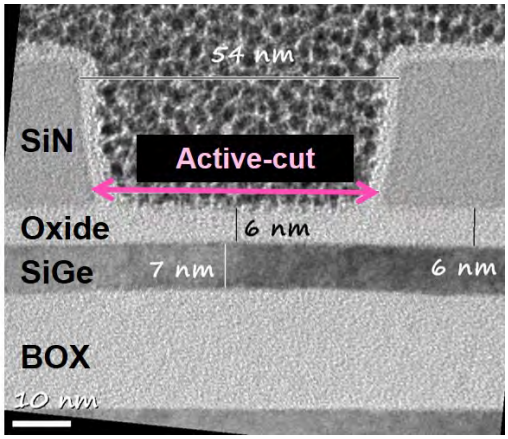


Figure 4.48: TEM picture after "active-cut" etching, corresponding of step (E) of Figure 4.46. The SiN hard mask is reused after CMP. The "active-cut" consists in the minimum distance of isolation in a "Single-Diffusion-Break" layout.

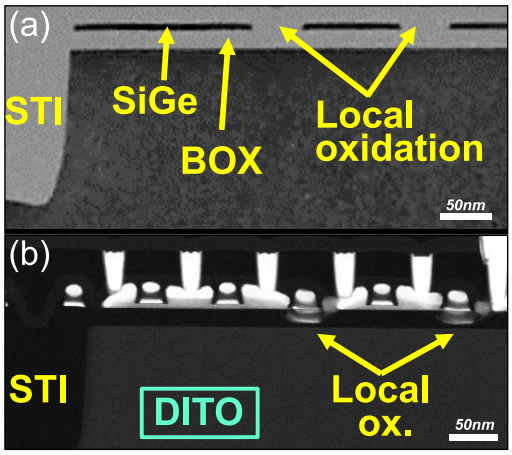


Figure 4.49: DITO TEM images (a) after the local oxidation module and (b) at the end of the process flow. In a "Single-Diffusion-Break" layout, a dummy gate is located above the local oxidation, as illustrated in the top-view of Figure 4.47.

The TEM pictures of Figure 4.49 show the DITO integration after the isolation module and at the end of the complete CMOS integration. The active areas are well isolated from each other as the oxidation reaches the BOX. The oxide formed by the SiGe local oxidation has been however partly consumed at the end of the flow. This is probably due to the HF-budget before the gate formation.

The Energy-dispersive X-ray spectroscopy (EDX) mappings are presented for both isolations in Figure 4.50. The EDX scan between two local oxidation isolations shows a $Si_{0.75}Ge_{0.25}$ channel with higher Ge concentration under source/drain, possibly due to lateral enrichment or Germanium

1 Two other RTO conditions have been tried: 940°C for 540sec and 940°C for 350°C. We focus here only on the best results achieved, obtained with the RTO at 900°C for 540sec.

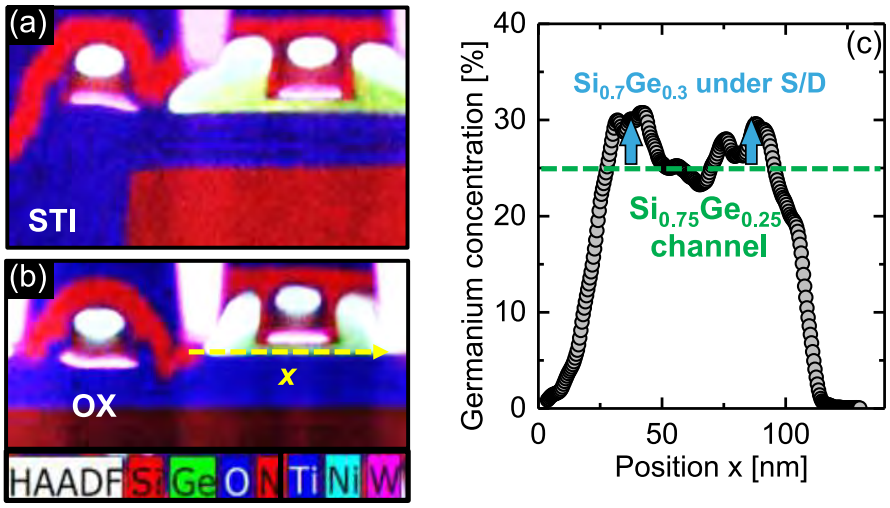


Figure 4.50: EDX mapping of a device close to (a) an STI isolation and (b) a local oxidation. (c) scan of Germanium concentration for a device located between two local oxidations. The Germanium concentration is 25% in the channel and close to 30% in the source/drain region

diffusion from $Si_{0.7}Ge_{0.3}$ source and drain.

4.3.2.b Device electrical results

The DITO device electrical characteristics are assessed and compared with the process of reference called single-STI.

Unfortunately, only one device layout uses the double patterning on our available maskset. Few structures can thus be tested. The layout consists in an active width of W=170nm, a gate length of L=20nm and a gate-to-isolation distance of SA=59nm, designed in a "Single-Diffusion-Break" scheme (see layout of Figure 4.47). It is the layout of highest density and consequently the one the more sensitive to SiGe strain relaxation. As a result, this is the best layout to evaluate our dual integration scheme.

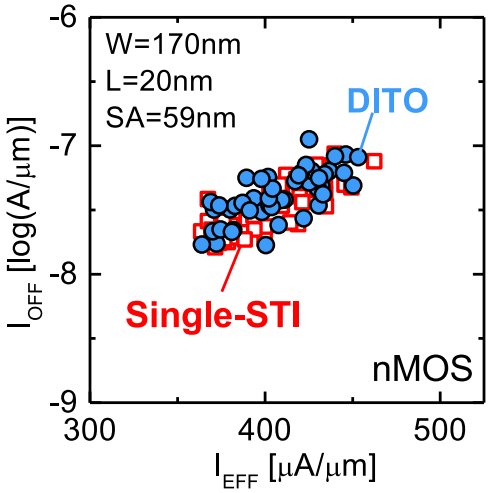


Figure 4.51: I_{EFF}/I_{OFF} trade-off for nFETs. Same results are obtained for single-STI and DITO.

DITO integration does not impact nMOS performance, as demonstrated by the trade-off between effective current and leakage current (I_{EFF}/I_{OFF}) of Figure 4.51. This result shows that the local

oxidation does not introduce a significant stress on unstrained Si channel. For pMOS, Figure 4.52 shows the $I_D(V_G)$ and $I_D(V_D)$ curves for both isolation schemes. Both the transfer and output characteristics are strongly impacted by DITO. Experimental data are reproduced by the virtual source model [Kha09].

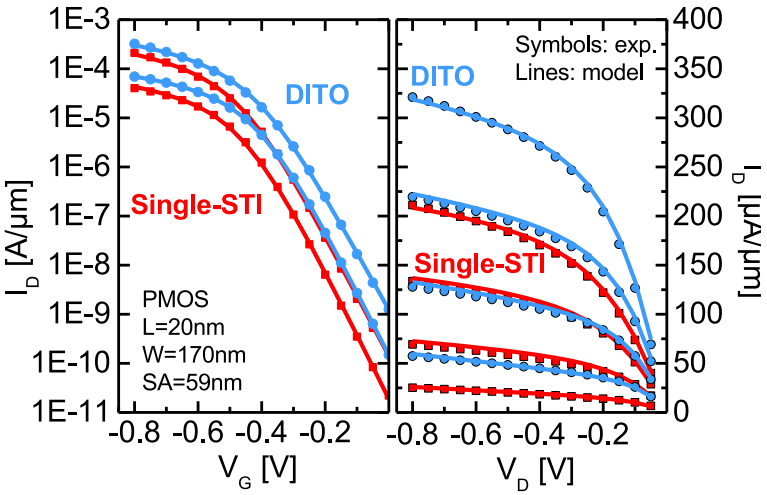


Figure 4.52: Transfer and output characteristics for pFET from DITO and single-STI integration schemes. Model from [Kha09].

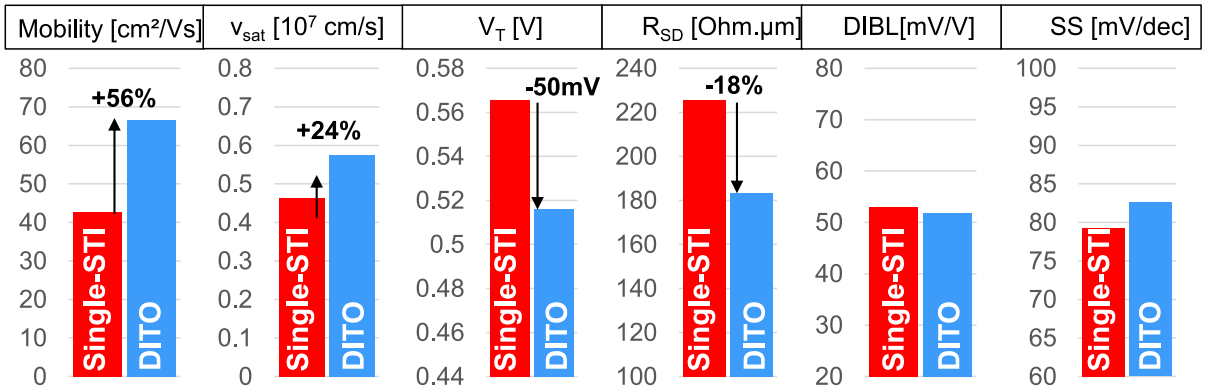


Figure 4.53: Extracted parameters from virtual source model [Kha09]. DITO leads to +56% mobility, +24% saturation velocity, -50mV threshold voltage and -18% access resistance. Similar DIBL and subthreshold swing obtained with DITO, highlighting no impact on electrostatics.

DITO leads to +56% hole mobility, +24% saturation velocity, -50mV threshold voltage shift and -18% access resistance, showing the great performance improvement of DITO. In addition, DIBL and subthreshold swing are similar for both isolation schemes demonstrating that DITO does not alter the electrostatic control.

Figure 4.54 shows the I_{ODLIN} ($I_D[V_G\text{-}V_T\text{=-}0.5V;\ V_D\text{=-}50mV]$) as a function of V_{TLIN} (extracted at constant linear drain current) for both isolations. DITO improves I_{ODLIN} by +51% *vs.* single-STI, while reducing V_{TLIN} by -63mV.

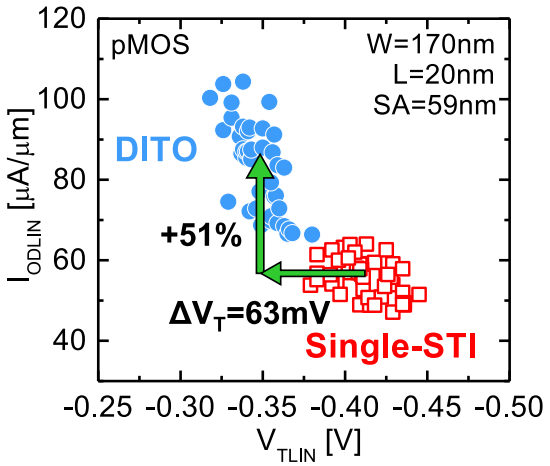


Figure 4.54: I_{ODLIN} *vs.* V_{TLIN} for DITO and single-STI. DITO improves I_{ODLIN} by +51% and reduces V_{TLIN} by -63mV.

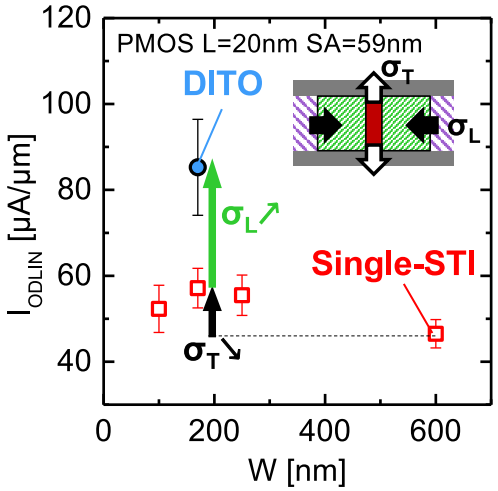


Figure 4.55: I_{ODLIN} *vs.* W evidencing the interest of DITO to optimize the strain configuration i.e. relaxing the transverse component while maintaining the longitudinal one.

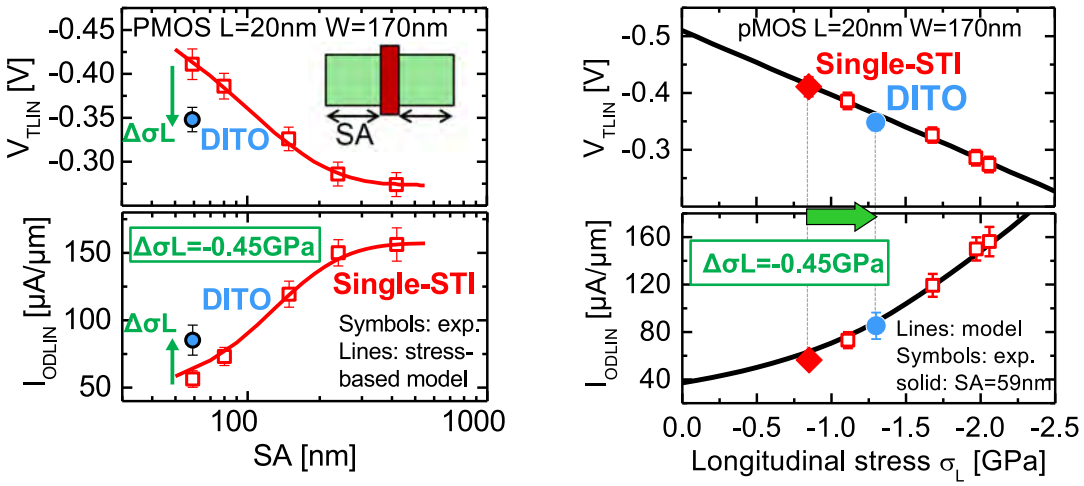


Figure 4.56: I_{ODLIN} and V_{TLIN} as a function of (left) SA and (right) the extracted stress from the model described in section 3.2.3. Both I_{ODLIN} and V_{TLIN} shifts at SA=59nm are consistent with an additional compressive stress of $\Delta\sigma_L = -0.45$GPa.

Figure 4.56 (a) shows the V_{TLIN} and I_{ODLIN} as a function of SA in a single-STI scheme. DITO improves the I_{ODLIN}(SA) behavior thanks to the local oxidation. Despite the gain demonstrated at SA=59nm with DITO, the I_{ODLIN} does not reach the performance of a long active area. This result suggests that even though the stress is higher with local oxidation isolation than with a single STI, it is not fully maintained. From our stress-based model (presented in Chapter 3), the additional longitudinal stress in the case of DITO is evaluated at $\Delta\sigma_L = -0.45$GPa at the end of process *vs.* single-STI. This higher stress can explain both the V_{TLIN} shift and the I_{ODLIN} gain (Figure 4.56 (b)).

In the transverse direction, DITO uses STI as isolation. As a result, the STI-induced stress relaxation for narrow actives, which is beneficial in the transverse direction, is maintained with DITO. The stress configuration is thus optimized by maximizing the longitudinal stress while relaxing the transverse one (see Figure 4.55). It provides the most favorable uniaxial longitudinal compressive

stress configuration in <110>-oriented channel.

4.3.2.c Strain characterization

Figure 4.57 shows a mapping of stress after the isolation by local oxidation of the SiGe film from process TCAD simulation [spr14] (half-structure is simulated). The oxidation (blue line) helps to maintain a high level of stress (-1.3GPa) since it avoids etching the SiGe film. The slight loss of stress, compared to the fully stressed SiGe (dashed green line), is due to the fact that the oxide is less rigid than the SiGe film. The STI stress-based model calibrated on electrical results is also plotted for comparison (dashed red line). High relaxation is expected in such a short active area.

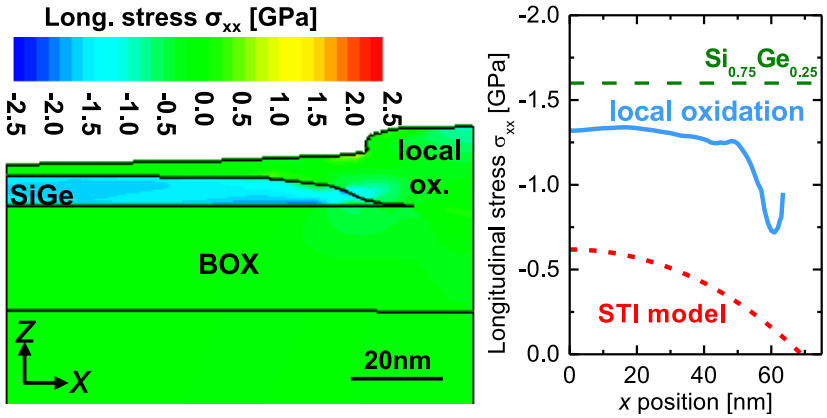


Figure 4.57: sprocess simulation of local oxidation: (left) mapping of longitudinal stress after oxidation and (b) scan in the SiGe layer (blue line). Even though the stress is not fully maintained (lower value than the dashed green line), a high level of stress is expected (-1.3GPa). The STI model (dashed red line) is also plotted for comparison.

In order to further characterize the DITO integration, the relative in-plane deformation *vs.* Silicon substrate reference ($e_{XX} = (a_{SiGe} - a_{Si})/a_{Si}$) has been measured by Precession-Electron-Diffraction (PED) [Coo15]. Figure 4.58 shows the PED scan in SiGeOI isolated by either STI or oxidation. A higher compressive strain is obtained by oxidation (lower e_{XX} value). However, STI results suggest that SiGe is not fully relaxed. Also, the deformation profile is flat, indicating no edge effect. This is not in total agreement with what as been deduced from NBED, dark holography and electrical measurements detailed in Chapter 3.

Figure 4.59 shows the PED e_{XX} mapping and scan in a the SiGeOI channel of a device constituted of two gates and isolated by local oxidation. The role of $Si_{0.7}Ge_{0.3}$:B source/drain is clearly visible, dragging the region under source/drain in tension ($e_{XX} > 1\%$) while the channel is put in compression. A high level of stress is however evidenced in the middle of the two channels: $e_{XX} = 0$ means approximately $\sigma_L = -1.6$ GPa for $Si_{0.75}Ge_{0.25}$. The profile is consistent with a relaxation close to isolation since e_{XX} increases, as illustrated by the arrow.

The mapping of the relative deformation extracted at the end of the process flow for a single device close to a STI isolation and for a device with DITO (i.e. with local isolation by oxidation) is presented in Figure 4.60. It is clear that the DITO channel relative deformation has a lower value (green color *vs.* orange). The deformation is extracted along the channel (dashed black arrows) and results are given in Figure 4.61. DITO strongly improves the strain, achieving $e_{XX} = 0.1\%$, which

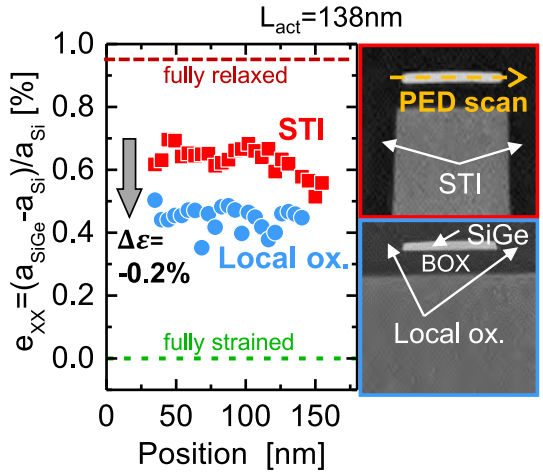


Figure 4.58: PED scan in SiGeOI isolated by STI or oxidation. A higher compressive strain is obtained by oxidation.

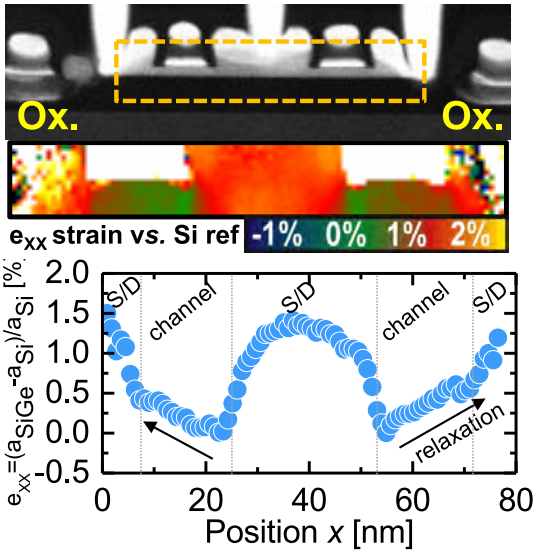


Figure 4.59: PED e_{XX} (top) mapping and (bottom) scan in a SiGeOI device constituted of two channels and isolated by local oxidation. The profile shows the impact of SiGe source/drain and evidences a slight relaxation close to the isolation (e_{XX} increases, represented by the arrow). High level of stress is however evidenced in the channels ($e_{XX} = 0 \approx \sigma_L = -1.6$ GPa).

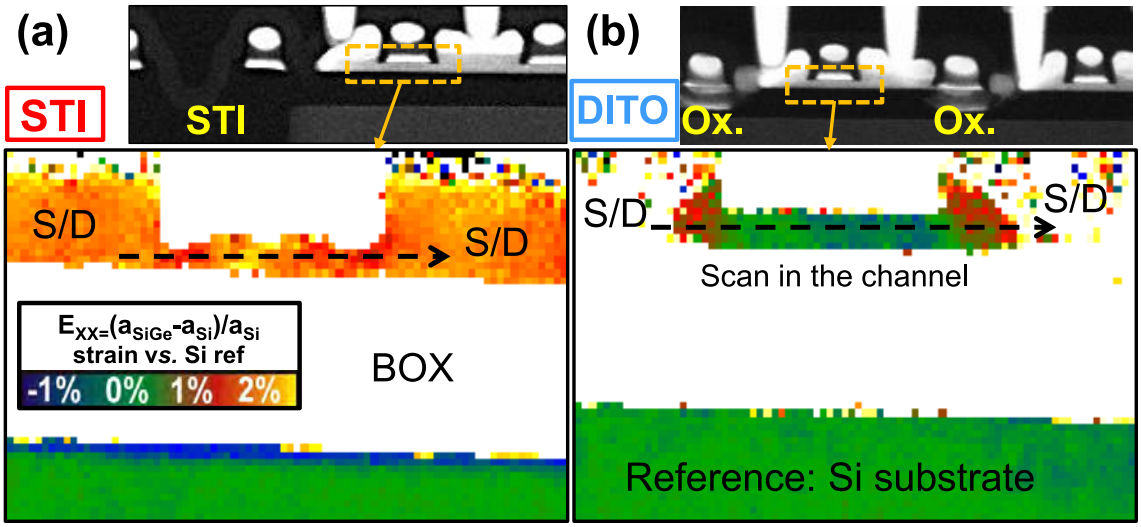


Figure 4.60: PED relative deformation mapping of a device (a) close to STI and (b) between two local oxidations.

is approximately equivalent to a longitudinal stress of $\sigma_L = -1.35$ GPa, in agreement with stress extracted from electrical measurements (Figure 4.56).

Strain measurements confirm that the DITO integration scheme enables the compressive stress in SiGe to be better maintained in short active layout.

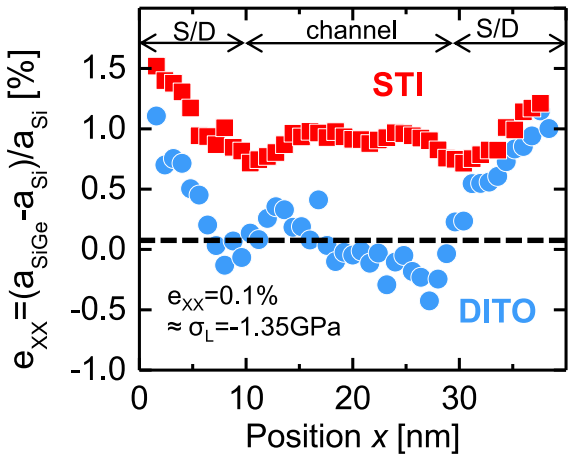


Figure 4.61: Relative deformation in SiGe active area extracted from PED mapping of Figure 4.60. Higher compressive strain observed for the device isolated by oxidation (compressive stress evaluated at $\sigma_L = -1.35$GPa).

4.3.2.d Performance

As demonstrated in previous sections, DITO enables the stress configuration to be optimized. This is translated into a hole mobility enhancement. As a result, the performance is improved: The I_{EFF} current increases by +36% at the same leakage with respect to single-STI (Figure 4.62).

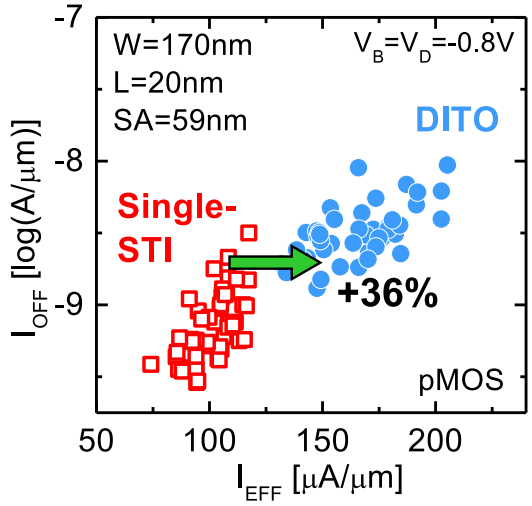


Figure 4.62: I_{EFF}/I_{OFF} trade-off for pMOSFETs showing +36% improvement with DITO over single-STI.

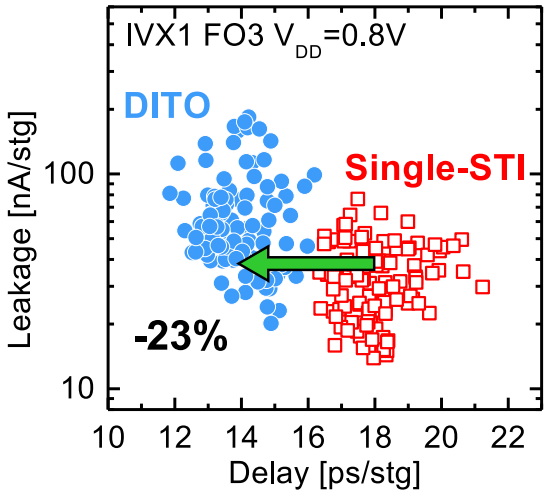


Figure 4.63: I_{DDQ}/τ_P for ring-oscillators of 1-finger inverters. DITO leads to 23% delay reduction over single-STI at same leakage.

This gain on pMOS while nMOS is not impacted is translated into a ring-oscillator speed improvement. Figure 4.63 shows the leakage/delay trade-off of 1-finger inverter ring-oscillators loaded by a Fan-Out 3 (FO3) for a supply voltage of V_{DD}=0.8V. The delay is reduced with DITO by -23% at a given static leakage. This improvement is the consequence of the higher longitudinal stress previously evidenced. The slight increase of the static leakage with DITO can be explained by the pMOS threshold voltage shift due to the higher longitudinal stress in the channel, in agreement with pMOS transistor I_{OFF} of Figure 4.62. For 1-finger inverter, the single-STI reference has an unbalanced n/p ratio since the pMOS V_T is too high because of stress relaxation. In addition to the mobility gain, DITO restores the balance by maintaining a low pMOS V_T. That is why the gain on the delay is significant.

In addition, the lower the supply voltage, the higher the gain induced by DITO, as shown in Figure

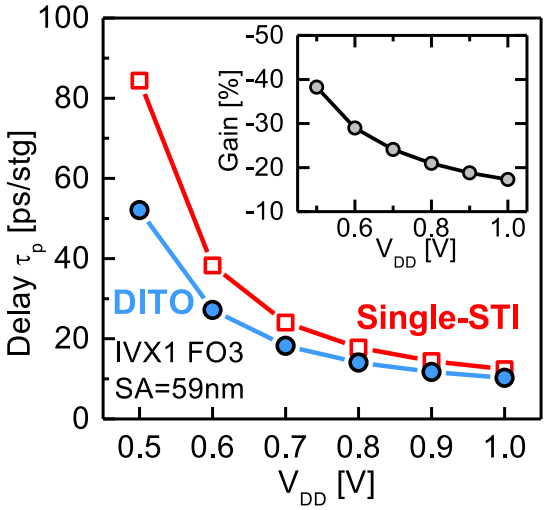


Figure 4.64: τ_P *vs.* V_{DD} for ring-oscillators of 1-finger inverters. The lower the supply voltage, the higher gain because DITO not only impacts the hole mobility but also allows to maintain a low pMOS V_T.

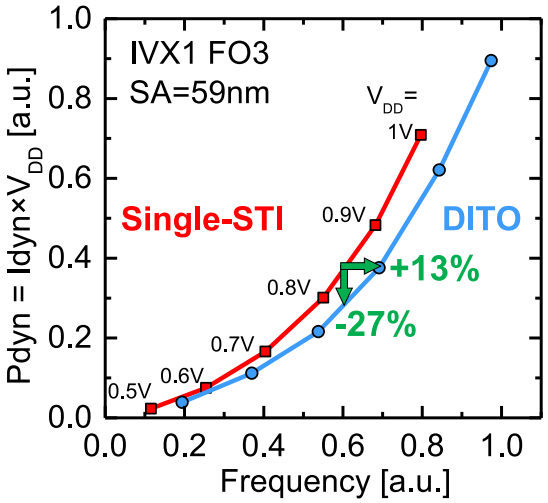


Figure 4.65: P_{dyn} *vs.* Frequency for DITO and single-STI at different supply voltages V_{DD}. DITO enables to reduces the dynamic consumption by -27% at a given frequency or improves the speed by +13% at same dynamic power.

4.64, demonstrating -29% delay at V_{DD}=0.6V. This is also due to the lower pMOS V_T with DITO, ensuring higher gate-overdrive (V_{DD}-V_T), which is decisive at low V_{DD}. Finally, Figure 4.65 shows that the dual-isolation leads to a dynamic consumption reduction of -27% at same speed or a +13% frequency improvement at a given dynamic power.

4.3.2.e Back-biasing enabled by DITO

DITO not only optimizes the stress configuration but also enables a complete isolation of the nMOS back plane from the pMOS one as shown in Figure 4.66.

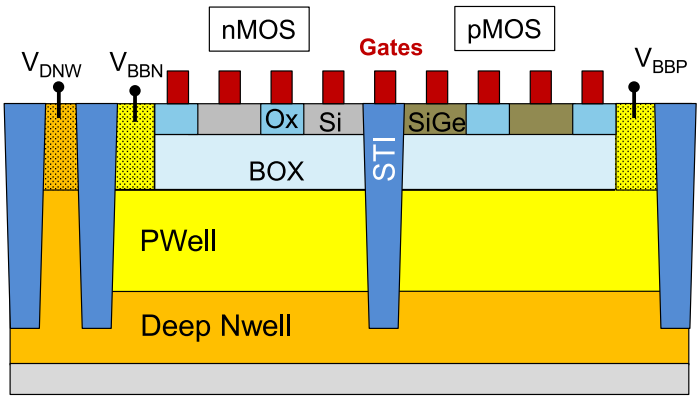


Figure 4.66: Cross-sectional scheme of the DITO integration enabling a full bidirectional back-bias (FBB and RBB). Deep trenches (STI) separate nMOS and pMOS back-planes while transistors of the same type are isolated with local oxidation.

It thus allows to use both positive and negative back-biases, i.e. Forward and Reverse Back Biasing (FBB and RBB) on nMOS and pMOS independently. By applying a back-bias in FDSOI technology, the V_T is significantly shifted. The back-bias efficiency is due to the strong coupling with the back-gate thanks to the thin BOX. It is defined by Equation 4.2, assuming an inversion at the front

(i.e. at the gate oxide / channel interface).

$$\gamma = \frac{\Delta V_T}{V_B} = \frac{C_{BOX} \cdot C_{Si}}{C_{OX}(C_{BOX} + C_{Si})} \tag{4.2}$$

where C_{OX} is the gate oxide capacitance, C_{BOX} the buried oxied (BOX) capacitance and C_{Si} the SOI channel capacitance. Figure 4.67 highlights the impact of back-bias on the transfer characteristics for both Forward and Reverse Back-Bias ranging from -2V to +2V.

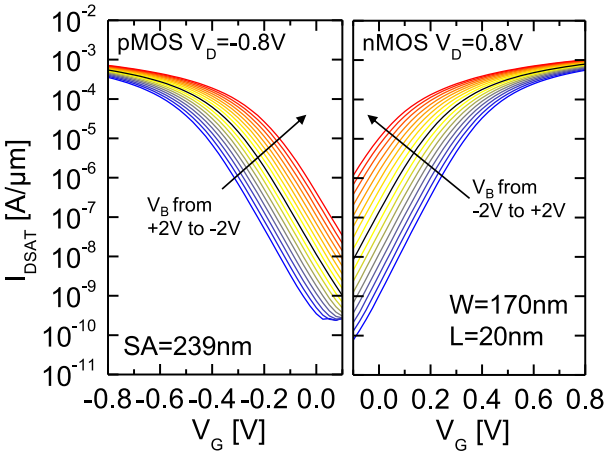


Figure 4.67: pFET and nFET $I_D(V_G)$ at different V_B with 4V body bias range, enabling to shift the threshold voltage. Forward Back-Bias consists in positive, negative, V_B for nFET, pFET, respectively. Reverse Back-Bias is the opposite.

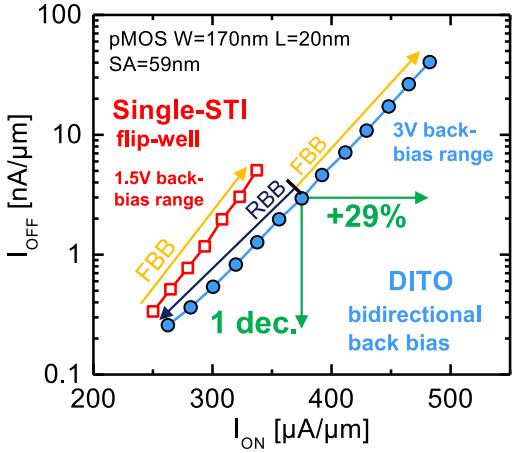


Figure 4.68: pFET I_{ON}/I_{OFF} trade-off at V_{DD}=0.8V for different back-biases. DITO enables a full back-bias operation while single-STI is limited to FBB in a flip-well architecture.

By isolating the back-planes, DITO enables a bidirectional back-bias on the same device while single-STI is limited to FBB range in flip-well architecture (and RBB in regular-well one) because of the PN well junction. DITO can thus achieve a large range of performance/leakage according to the back-bias, as shown on Figure 4.68. As a result, with a 3V back-bias range, the ON current (I_{ON}) can be enhanced by +29% and the leakage current (I_{OFF}) range extended by 1 decade compared to the single-STI flip-well FDSOI architecture. It should be pointed out that the difference DITO/single-STI at V_B=0 on Figure 4.68 is due to strain effects, detailed in previous sections.

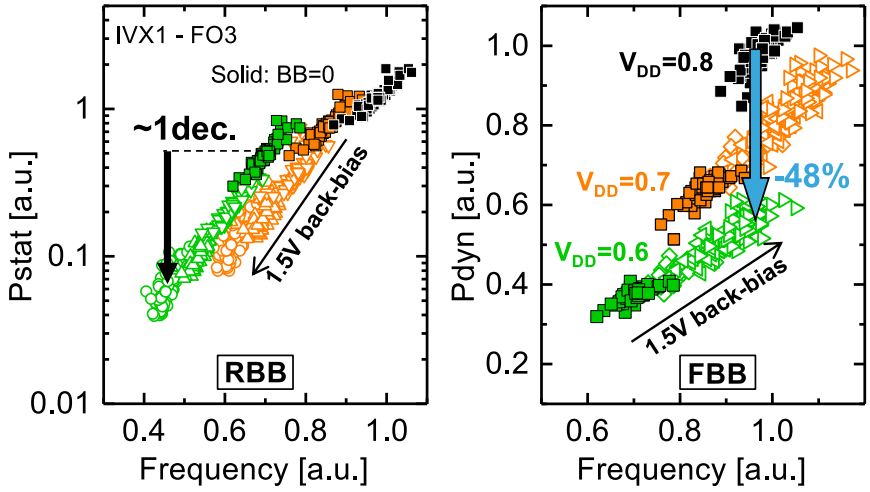


Figure 4.69: P_{STAT} and P_{DYN} as a function of the Frequency. Static power can be reduced by 1 decade under 1.5V RBB and FBB enables the dynamic power to be reduced by -48% at a given frequency.

Measurements on FO3 ring-oscillators show that the static power is reduced by almost 1 decade under 1.5V RBB (Figure 4.69). In addition, 1.5V FBB allows to reduce V_{DD} by 200mV while keeping the same speed, achieving -48% dynamic power improvement. These results highlight the strong interest to take full advantage of FDSOI back-biasing capability that only a dual isolation scheme such as DITO enables.

4.4 Conclusion to Chapter 4

In the previous chapter, the layout effect induced by SiGe relaxation have been deeply investigated. In this Chapter, different solutions to mitigate the layout effect and therefore optimize the performance have been evaluated via two approaches: design and technological solutions.

The first assessed design solution consists in mixing the V_T flavor inside the cell. Using a low-V_T flavor for pFET combined with a regular nFET for the short active standard cells such as the 1-finger inveter allows to counterbalance the strain-relaxation-induced layout effect. From simulations, it is expected to lead -23% delay reduction for the 1-finger inverter compared to the reference regular-V_T case. This so-called Mix-V_T approach has the advantage of being easily implemented. However, it only solves the problem of threshold voltage shift whereas the performance is still impacted by the mobility degradation.

The second design solution consists in designing the standard cells on a continuous active area. This so-called Continuous-RX approach enables the longitudinal stress to be maintained. A high performance improvement of -28% ring-oscillator delay reduction at the same leakage has been experimentally demonstrated. The CRX requires an isolation-gate construct to prevent fatal leakage between the abutted standard cells. Besides, the presence of RX-jogs, i.e. non-rectangular actives, when standard cells are abutted leads to partial relaxation and in turn performance degradation. The abutment-induced variability (the performance of a standard cell depends on its neighbors) is an issue of the CRX approach. The use of filler-cells has been discussed, reducing the abutment-induced variability but at the expense of density loss.

The introduction of SiGe in SRAM cells has then been discussed. Especially, the change of the Pass-Gate from nFET to pFET has been assessed. Such a Complementary SRAM benefits from the high performance of SiGe pFET built on a long active area, consistently with the CRX design. The read current is expected to be increased by +21% from simulations.

As far as technological solutions are concerned, the SiGe-last approach has been investigated. In such an integration scheme, the SiGe channel is fabricated after the STI module, without any condensation step. The patterning-induced relaxation has been demonstrated to be reduced by such an approach. However, this is not necessarily translated into performance gain. While short active devices benefit from a low relaxation, the long active devices are degraded because of the detrimental effect of the transverse stress in <110>-oriented channels.

Finally, a Dual Isolation by Trenches and Oxidation (DITO) scheme has been proposed. Such a configuration enables the best stress configuration for <110>-oriented SiGe channels, i.e. longitudinal. A better maintain of strain by oxidation has been demonstrated by the means of physical measurements and electrical characterizations. A ring-oscillator delay reduction of -23% has been experimentally observed. The strain is however not fully maintained in our experiment. Further process optimization is possible but full oxidation of SiGeOI is challenging. Nevertheless, such a dual isolation configuration allows to take full advantage of the bidirectional back-bias, highly efficient in FDSOI technology.

CHAPTER 5

Next generation strained FDSOI CMOS devices

Contents

5.1 Tensile strain from strained-SOI substrate

We have seen that the use of a compressively strained SiGeOI channel is highly efficient to boost the performance of the pFET. In the Chapter 3, we have shown that the introduction of such intrinsically strained channel comes along with strong layout effects. Some design and technological solutions to optimize the performance have been proposed and demonstrated in the Chapter 4.

As far as the nFET is concerned, tensile strain is needed to enhance the electron mobility. The strained-SOI (sSOI) substrate features a thin tensely strained Silicon layer directly on insulator. Such substrates are fabricated according to the Smart Cut process [Sch12]. Compared to a SOI substrate, a Silicon layer is deposited by hetero-epitaxy on a relaxed SiGe buffer before bonding. The level of tensile in-plane strain in the SOI layer depends on the Germanium concentration of the template.

In this section, we focus on the electrical characteristics of devices from 14nm FDSOI technology fabricated on a sSOI substrate (Aurore Bonnevialle's work [Bon16c]). First, the performance is briefly assessed. Then, we investigate the layout effects for such intrinsically tensely strained substrate.

5.1.1 sSOI performance

The impact of a tensile strain on the electron mobility has been widely discussed in the literature and performance gains have been demonstrated on a wide variety of devices [And14; Bae16; DeS14; Hua01; Kha12; Rim03; Xie16]. The Figure 2.5 of section 2.1.3 (page 56) shows the electron mobility enhancement according to the tensile stress for a <110>-oriented channel, deduced from piezoresistive coefficients measurements. In such orientation, the transverse stress has little impact on the electron mobility. The gain in a biaxial configuration is mainly due to the longitudinal stress component.

Devices have been fabricated according to the 14nm FDSOI process flow, starting from a sSOI substrate [Bon16c]. It has to be noted that for the sSOI substrate, the Buried Oxide thickness is 25nm while it is 20nm for the SOI reference.

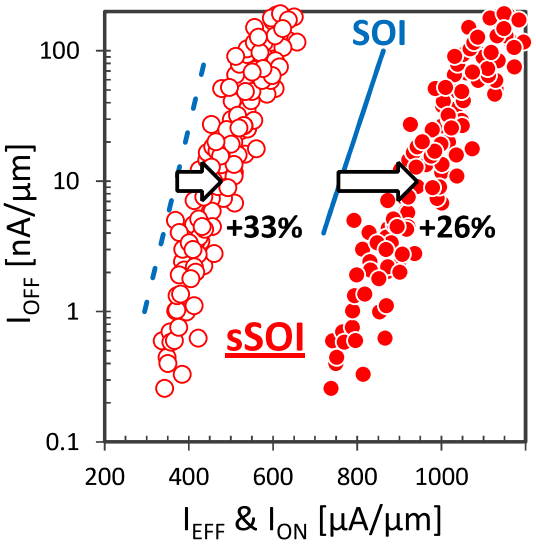


Figure 5.1: I_{EFF} & I_{ON} *vs.* I_{OFF} at V_{DD}=0.8 for sSOI W=170nm nFETs compared to reference SOI in 14nm FDSOI technology. Performance improvement is demonstrated with sSOI, showing +26% I_{ON} and +33% I_{EFF} at the same leakage.

The impact on the nominal nFET performance is shown in Figure 5.1. The I_{ON} and I_{EFF} currents are enhanced by +26% and +33%, respectively, at the same leakage. This result highlights the

strong interest of tensile strain to boost the nFET performance in scaled FDSOI technologies. In the next section, the impact of sSOI on layout effects is investigated.

5.1.2 sSOI Local Layout Effects

In Chapter 3, we have seen that the introduction of a strained SiGe channel for pFET comes along with strong layout effects. The electrical characteristic dependence with the active area geometry has been found to be related to the stress relaxation that occurs during the patterning.

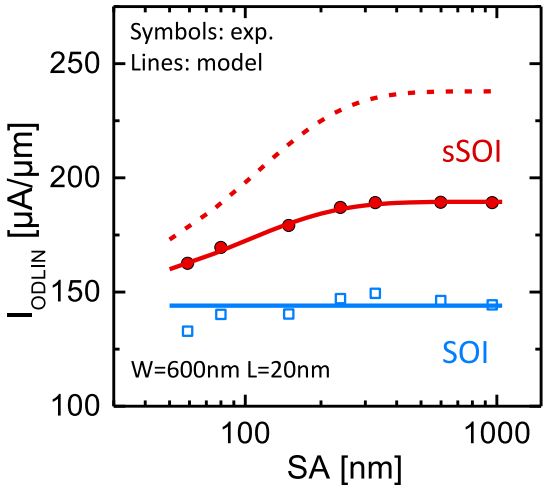


Figure 5.2: I_{ODLIN} current as a function of the gate-to-STI distance SA for both SOI and sSOI W=600nm L=20nm nFET devices. The sSOI I_{ODLIN} decrease for short active layout is attributed to the longitudinal stress relaxation. The model overestimates the gain (dashed line). In order to reproduce the experimental data, an access resistance of R_{ACC}=132 Ω.µm must be considered (solid line). The used typical relaxation length is λ=86nm.

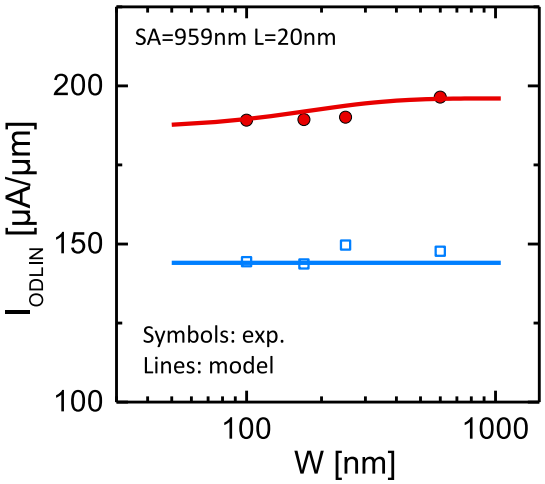


Figure 5.3: I_{ODLIN} current as a function of the active width for both SOI and sSOI SA=959nm L=20nm nFET devices. The sSOI I_{ODLIN} slightly varies with W. Even though the transverse stress is partially relaxed for narrow active, <110>-oriented channel electron mobility is not sensitive to the transverse stress.

Figure 5.2 shows the I_{ODLIN} variation with the gate-to-STI distance SA[1] for both SOI and sSOI nFETs of W=600nm and L=20nm. The sSOI I_{ODLIN} current is higher than SOI. This is due to the enhanced mobility with the tensile strain. For sSOI, the I_{ODLIN} current decreases when the active area becomes shorter. As for SiGe pFETs, this variation is attributed to the stress relaxation on the active edges.

The empirical relaxation model presented in section 3.2.3 is used to reproduce the layout dependence. The SOI channel is assumed to be unstressed. The sSOI initial stress is derived assuming a relaxed SiGe buffer with 20% of Germanium, yielding $\varepsilon_0 = 0.76\% \Leftrightarrow \sigma_0 = 1.37$GPa. As for the raised source/drain, the epitaxy of Si is made on a tensely strained substrate. As a result, the raised source/drain are intrinsically strained with the same ε_0 value as the substrate. The Si source/drain thus induce an additional tensile strain in the channel induced by their elastic energy relaxation, dragging the channel region as illustrated in Figure 5.4. This effect is also taken into account in the model, similarly to the impact of SiGe source/drain (section 3.3.1).

1 Please refer to Figure 3.40 for a definition of SA parameter.

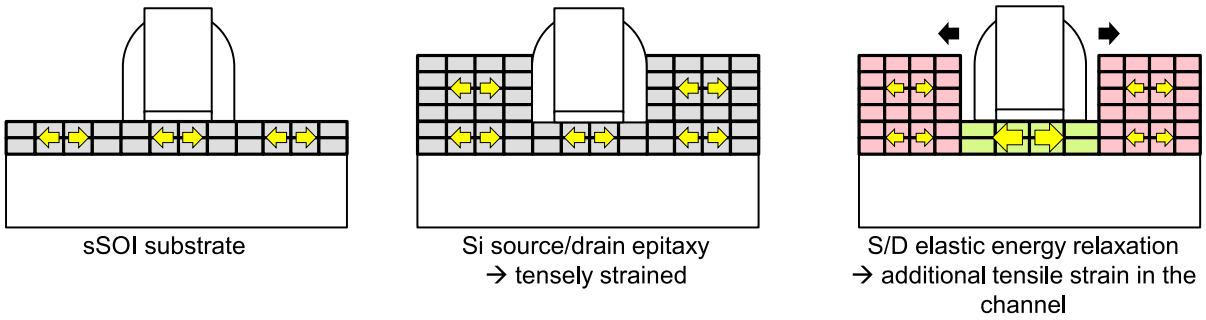


Figure 5.4: Illustration of the additional stress generated by Si epitaxy for devices built on a sSOI substrate. Since the raised source/drain are grown on a tensely strained substrate, they feature a tensile strain as well. As the elastic energy can partially relax in these regions because of the geometry, the channel region is dragged, generating a tensile stress.

The sSOI I_{ODLIN} value predicted by the model for a long active (SA=959nm) is represented by the dashed line in the Figure 5.2. The I_{ODLIN} gain with respect to SOI is clearly overestimated by the model. There are two reasons that could explain this mismatch. The first reason could be an overestimation of the mobility gain induced by the tensile stress, which is derived from the piezoresistive coefficients. The second reason could be a parasitic series resistance that is not impacted by the stress. We choose to assume that the second reason is valid and an additional parameter, R_{ADD}, is introduced in the model. This additional resistance is considered similar for both SOI and sSOI. The final model that fits best the experimental data is represented by the solid line. The parameters are: $I_{OD,0}$=234 µA/µm, R_{ACC}=132 Ω.µm and the typical relaxation length λ=86nm. It is worth noting that the typical relaxation length value is similar to the one of SiGeOI channels using the same maskset (see Figure 3.63). These electrical measurements suggest that the high relaxation for SiGeOI (see Chapter 3) is not related to the presence of Germanium atoms at the BOX/SiGe interface. Strain physical measurements are however required to confirm this hypothesis.

The impact of the active area width is shown in Figure 5.3. The sSOI I_{ODLIN} current does not significantly vary when the active is narrowed. This is explained by the low sensitivity of electron mobility to the transverse stress in a <110> oriented channel. The slight variation is captured by the model.

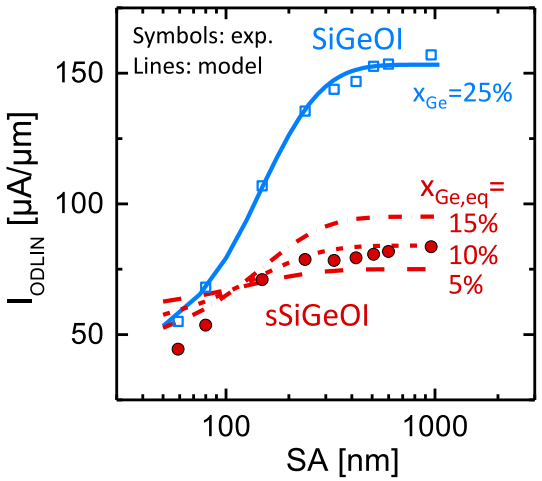


Figure 5.5: I_{ODLIN} current as a function of the gate-to-STI distance SA for both SiGeOI and sSiGeOI W=600nm L=20nm pFET devices. The sSiGeOI I_{ODLIN} current is degraded with respect to the reference SiGeOI because of lower initial compressive stress. The model, calibrated on the reference, enables to reproduce the sSiGeOI data assuming an equivalent Ge concentration of $x_{Ge,eq}$=10%. The typical relaxation length is λ=82nm.

As far as the pFET is concerned, the same SiGe condensation process as in the reference has been realized. Since the substrate is this time intrinsically tensely strained, the final level of strain in the so called sSiGeOI channel differs from the reference. Actually, the level of strain derives from the difference between the Germanium concentration in the SiGe buffer for the sSOI substrate fabrication and the one after the condensation. In our case, we can expect an initial stress of approximately $\sigma_0 = -0.33$GPa (i.e. the stress from the equivalent Ge concentration $x_{Ge,eq}$ of 25-20=5%).

The pFET I_{ODLIN}(SA) trend is represented in Figure 5.5. Obviously, by reducing the initial stress in the sSiGeOI channel, the I_{ODLIN} is strongly degraded with respect to the reference, especially for long active layout. This result emphasizes the challenge of stress co-integration. While compressive stress from SiGe channel can be locally introduced, it is not the case for the tensile counterpart. The sSOI substrate yields tensile stress on the whole wafer, impacting nFETs and pFETs simultaneously.

The layout dependence is confronted to the stress based model, calibrated on the reference SiGeOI channel. The model fits the sSiGeOI experimental data considering an initial stress equivalent to a Ge concentration $x_{Ge,eq}$=10%. This Ge concentration is slightly higher than expected. An explanation could rely on the impact of the level of stress on the condensation process kinetics. If the oxidation kinetics is faster than in the reference, the final Germanium concentration achieved could be increased.

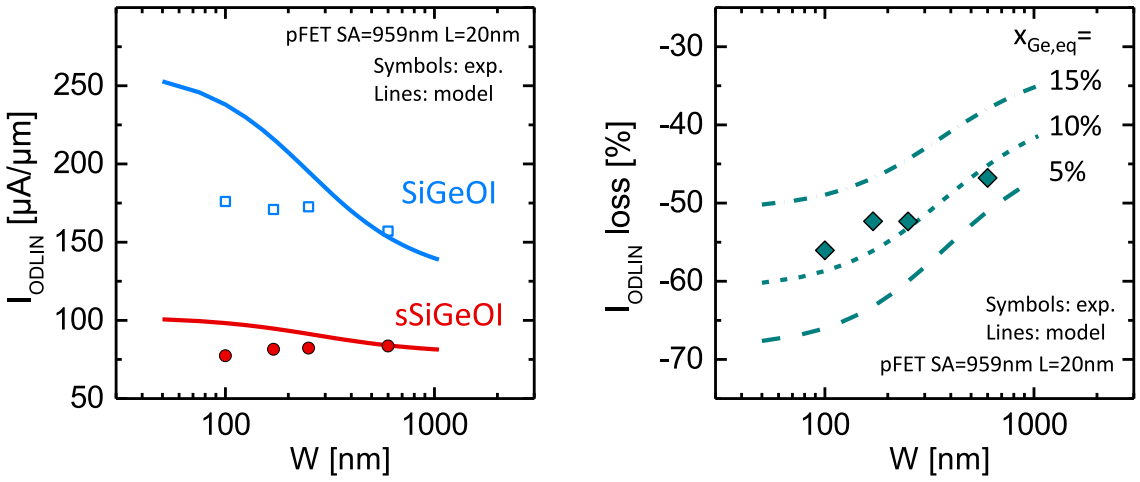


Figure 5.6: (left) I_{ODLIN} *vs.* W and (right) I_{ODLIN} loss from SiGeOI to sSiGeOI SA=959nm L=20nm pFETs. Even though the model fails to reproduce the impact of active narrowing (parasitic access resistance), the I_{ODLIN} variation from SiGeOI to sSiGeOI is well captured, assuming an equivalent Germanium concentration of $x_{Ge,eq}$=10%.

This equivalent Germanium concentration $x_{Ge,eq}$=10% is consistent with the impact of transverse stress relaxation, depicted in Figure 5.6. As discussed in Chapter 3, the model fails to reproduce the I_{ODLIN} increase when the active is narrowed. This has been attributed to parasitic access resistance induced by faceted raised source/drain. Nevertheless, the loss from SiGeOI to sSiGeOI is well reproduced, provided that the equivalent Germanium concentration is assumed to be $x_{Ge,eq}$=10%.

Regarding the threshold voltage, Figure 5.7 shows the V_T shift from SOI to sSOI, defined as $\Delta V_T = V_{TLIN}$[sSOI] - V_{TLIN}[SOI], according to the SA layout parameter. The impacts of both the active length and width are represented. The V_T shift depends on the active area dimension and is maximum

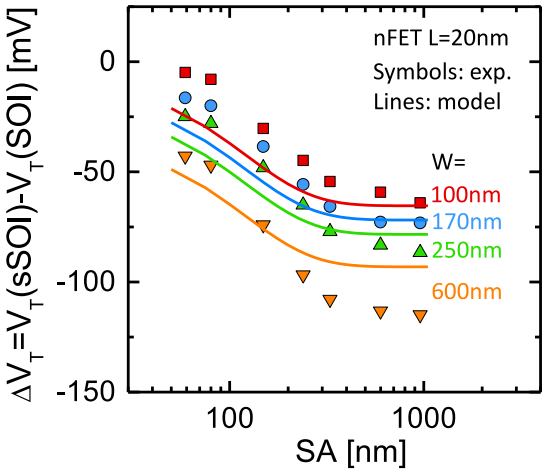


Figure 5.7: nFET V_T shift (ΔV_T = V_{TLIN}[sSOI] - V_{TLIN}[SOI]) according to the gate-to-STI distance SA and for different active widths. The longer and larger the active, the higher V_T shift due to strain. The V_T shift reduces when the active is narrowed and/or shortened because of the stress relaxation on active edges. The lines correspond to the model assuming the same stress sensitivity in longitudinal and transverse directions S_L=S_T=-34mV/GPa and a typical relaxation length of λ=86nm.

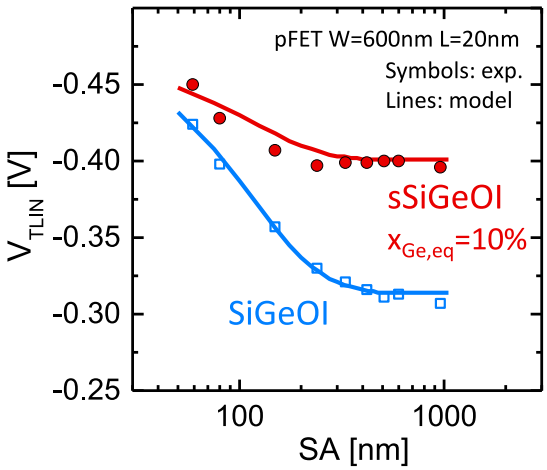


Figure 5.8: pFET V_{TLIN} *vs.* SA for SiGeOI and sSiGeOI. The lower strain in sSiGeOI yields increased V_{TLIN} and reduced layout effect compared to the SiGeOI reference. The lines correspond to the model, calibrated on the SiGeOI reference and assuming $x_{Ge,eq}$=10% in sSiGeOI.

for long and large active. This threshold voltage shift is attributed to the tensile strain in sSOI. The V_T shift reduces when the active is narrowed and/or shortened because of the stress relaxation on active edges. The stress relaxation model is used to reproduce the layout effect, assuming the same V_T-stress sensitivity in longitudinal and transverse directions S_L=S_T=-34mV/GPa and a typical relaxation length of λ=86nm. The model is not in total agreement with the experimental data. A possible explanation could be that the V_T shift is not purely due to stress. In addition to the global variability from one wafer to an other, the sSOI sample also features a thicker BOX than the SOI reference (25nm *vs.* 20nm). This could be the reason for a non-stress-related V_T shift.

For pFETs, the Figure 5.8 compares the V_{TLIN}(SA) trends of SiGeOI and sSiGeOI. The use of a sSOI substrate reduces the initial level of strain in the sSiGeOI sample, leading to a higher V_{TLIN}, especially for long active layouts. Short active area suffer from the longitudinal stress relaxation, leading to V_{TLIN} increase, as discussed in Chapter 3. The stress-based model, calibrated on the SiGeOI reference, gives a best agreement with the experimental data if the equivalent Ge concentration is assumed to be $x_{Ge,eq}$=10%, consistently with I_{ODLIN} data.

5.1.3 Conclusion

The use of a sSOI substrate significantly improves the performance of the nFET thanks to the advantageous tensile strain for electron mobility. Such intrinsically strained channel suffers from layout effects. As it is the case for SiGeOI pFETs, the layout effects are due to the patterning of the active, resulting in stress relaxation. Nevertheless, the electron mobility is not as sensitive to tensile stress as the hole mobility is to compressive stress. The mobility layout effects are thus less

pronounced for nFETs. The threshold voltage however significantly varies with the dimensions of the active area.

The layout effects have been reproduced using the same stress model approach as for SiGeOI pFETs. The typical relaxation length giving the best agreement with the experimental data is found to be similar to the one of SiGeOI. Based on these electrical measurements, it is suggested that the presence of Germanium atoms does not impact the relaxation of SiGeOI channels. The unexpectedly high relaxation could be attributed to a weak interface between the amorphous BOX and the strained crystalline channel.

One of the bottle-necks for the introduction of sSOI in the next FDSOI generations remains the n/p co-integration. The tensile strain is not introduced locally, degrading the pFET performance. The use of a highly concentrated SiGe to compensate for the initial tensile strain has been discussed [And14]. This approach is similar to what has been proposed for finFET using Strain Relaxed Buffer (SRB) [Bae16; Xie16]. The threshold voltage tuning with such highly concentrated SiGe channel might however be challenging. For these reasons, there is a need for a local introduction of tensile strain. This is discussed in the next sections.

5.2 The BOX-creep technique

5.2.1 Introduction : the BOX-creep principle

The BOX-creep technique has been proposed to locally[1] introduce strain into SOI [Chi08]. The BOX-creep technique consists in generating strain into the SOI from relaxing the elastic energy of a stressed SiN layer. This is achieved with the help of an anneal at high temperature. This technique takes advantage of the low viscosity of SiO_2 at high temperature, enabling the SiN stress to relax. The underneath SOI is dragged by the SiN, resulting in a stress generation. The principle is described in Figure 5.9. In this illustration, the SiN stress is assumed to be compressive. The generated stress in the SOI is of opposite sign, i.e. tensile stress.

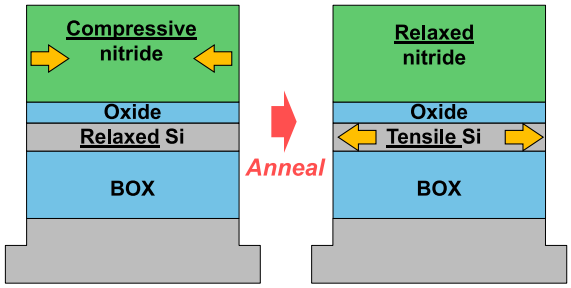


Figure 5.9: BOX-creep principle. Strain transfer from SiN layer into SOI by an anneal at high temperature. Low viscosity of SiO_2 allows the SiN to relax, dragging the underneath SOI. In this case, the use of a compressive SiN is translated into a tensile SOI after annealing.

A high level of strain has been experimentally measured (1.2GPa on 200mm wafer) [Bon15a], demonstrating the interest of such a technique.

5.2.2 Mechanical simulations

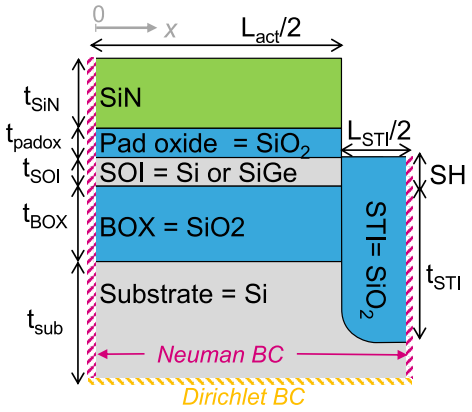
In order to assess the interest of the BOX-creep technique, we deeply investigated its efficiency through mechanical simulations.

5.2.2.a Hypotheses and model

COMSOL software [COM12] is used and especially the "structural mechanics" module. Time-dependent simulations are required to account for the SiO_2 visco-elasticity. In addition, the impact of the different process steps must be considered.

The process flow used for simulation is as follow: starting from a SOI substrate, a pad oxide is deposited before an intrinsically stressed SiN layer. The active areas are then defined by etching. A high temperature anneal enables the BOX to creep due to the low viscosity of SiO_2. The SiN layer is finally removed after STI filling and CMP. The simulated half structure, which considers symmetry axes, is represented in Figure 5.10. This structure is consistent with 14nm FDSOI technology (BOX thickness of 20nm). The values of the simulation parameters including material properties (Young's Modulus E and Poisson's coefficient ν along the <110> direction, and coefficient of thermal expansion CTE) are also given in Figure 5.10. The conditions of reference consist in an anneal of 10min at 1100°C, an active length L_{act} = 400nm, and a SiN layer of thickness t_{SiN} = 80nm and initially stressed at $\sigma_0 = -3$GPa.

1 On the opposite of sSOI where the strain is global, i.e. on the full wafer.



Anneal	
Duration	10min
Temperature	1100°C

Materials properties	E <110> (GPa)	ν <110>	CTE (/K)	Stress (GPa)
SiN	280	0.25	$3.0\ 10^{-6}$	-3
SiO2	73	0.17	$1.37\ 10^{-6}$	/
Si	169	0.063	$3.0\ 10^{-6}$	/
SiGe25%	161	0.055	$3.0\ 10^{-6}$	-1.6

Parameter	Value (nm)
t_{SiN}	80
t_{padox}	2
t_{SOI}	6
t_{BOX}	20
t_{sub}	174
t_{STI}	100
SH	6
$L_{act}/2$	200
$L_{STI}/2$	20

Figure 5.10: BOX-creep simulation half-structure and tables of reference parameters.

The SiO_2 viscosity model used for the simulations consists in a generalized Garofalo's model [Gar65] based on Eyring's one [Eyr36; Hu91]. It is shown in Figure 5.11 and given by:

$$\eta = \eta^0 \frac{\sigma}{\sigma_{crit}} \frac{1}{\sinh(\sigma/\sigma_{crit})} \tag{5.1}$$

where parameters η^0 and σ_{crit} are calibrated on results from literature [Sen96].

In this study, the intrinsic stress in the SiN layer is supposed to be constant with the anneal temperature. This can be a strong assumption as the SiN stress comes from the deposition process [Ses12]. Stress in SiN is mainly correlated to the concentration in Hydrogen: the lower the Hydrogen concentration, the higher the tensile stress. On the one hand, the Hydrogen concentration can strongly vary in SiN deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD), leading to a wide range of stress (from compressive -3GPa to tensile +2GPa). On the other hand, Low-Pressure Chemical Vapor Deposition (LPCVD) SiN is stoechiometric (Si_3N_4) with tensile stress around 1GPa. It has been shown that the stress can vary after an anneal at high temperature, assumed to be related to the Hydrogen desorption [Ben06; Ses12].

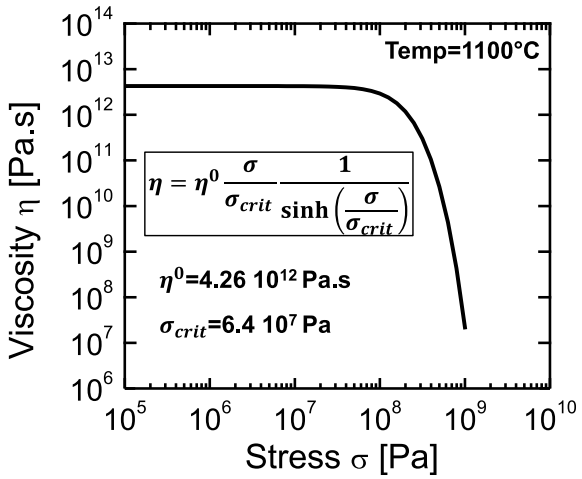


Figure 5.11: SiO_2 model of viscosity at T=1100°C used for BOX-creep simulations, based on a Garofalo's model [Eyr36; Gar65; Hu91] with parameters from [Sen96].

Regarding the uncertainty on the SiO_2 viscosity and SiN stress behaviors, this study aims at providing guidelines for BOX-creep optimization rather than quantitative expectations.

5.2.2.b The BOX-creep mechanism

The longitudinal stress σ_{xx} obtained along the different process steps of the BOX-creep is mapped in Figure 5.12. After etching, the compressively stressed SiN layer tends to relax due to the introduced free boundary condition. The underlying SOI is dragged by the SiN layer, giving birth to a tensile strain. At this point, the structure is maintained by the substrate. During the anneal however, the low viscosity of the BOX under shear stress and at high temperature enables further relaxation of the SiN stress. As the BOX is creeping, the substrate loses its ability to hold the structure. As a consequence, strain is transferred into the SOI layer. This behavior is highlighted in Figure 5.13, showing the stress mappings and profiles for different anneal durations.

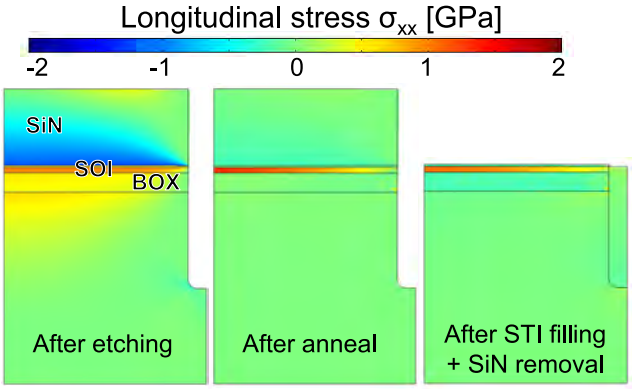


Figure 5.12: Simulated stress mapping along BOX-creep process steps. Using a compressive SiN leads to a tensile stress generated in the SOI layer. The stress is still present after SiN removal. The SiN layer is highly relaxed after anneal, hence the small impact of its removal on the SOI stress.

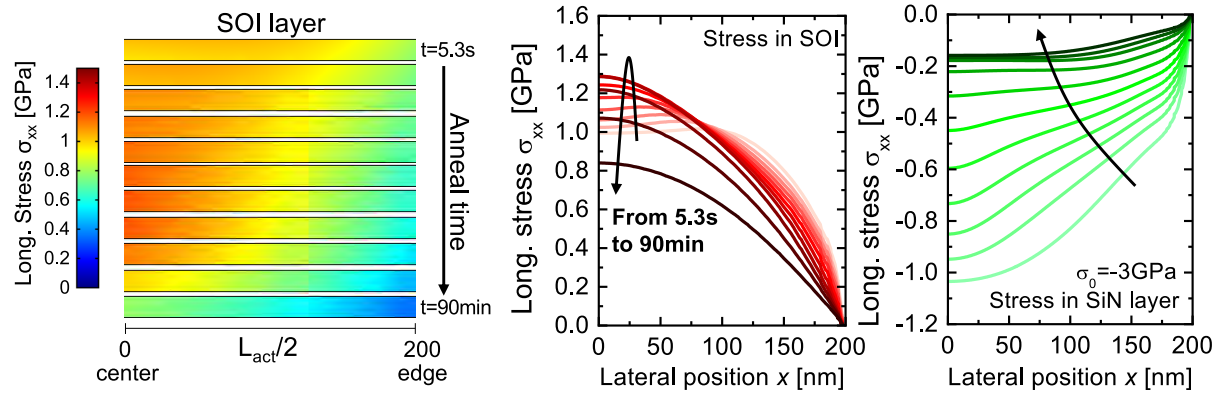


Figure 5.13: Simulated stress (left) mapping and (right) profiles during the BOX-creep annealing. From step to step, the anneal duration is multiplied by two. The compressive stress in SiN decreases and the tensile stress in SOI increases, due to the elastic energy transfer.

After a certain time, the stress in SOI decreases (Figure 5.14). There is thus an optimized anneal duration, which is found to be dependent on the active length L_{act}. This behavior will be discussed later on (section 5.2.2.d). After SiN removal, a significant amount of stress remains in the SOI layer (Figures 5.12 and 5.15). The SiN layer is highly relaxed after the anneal, hence the small impact of its removal. Finally, the level of longitudinal stress reaches $\sigma_{xx} = 1.1$GPa at the center of the active area i.e. (x=0) in the conditions of reference (Figure 5.15).

5.2.2.c Impact of SiN parameters

By carefully tuning the deposition conditions, a large range of initial stress in SiN can be obtained, from compressive to tensile stress (section 5.2.2.a). Figure 5.16 evidences a good linearity between the

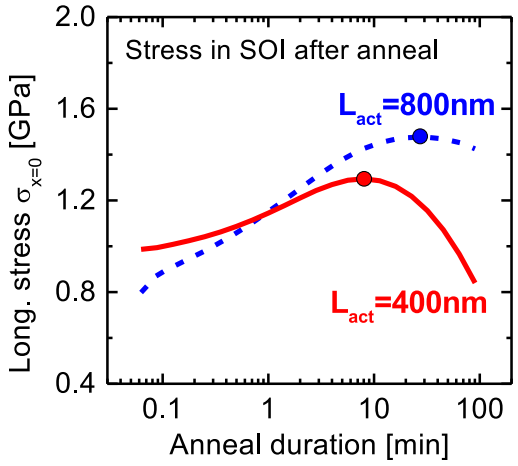


Figure 5.14: Stress in the middle of the active area according to the anneal duration. An optimal anneal duration is evidenced, which depends on the active length.

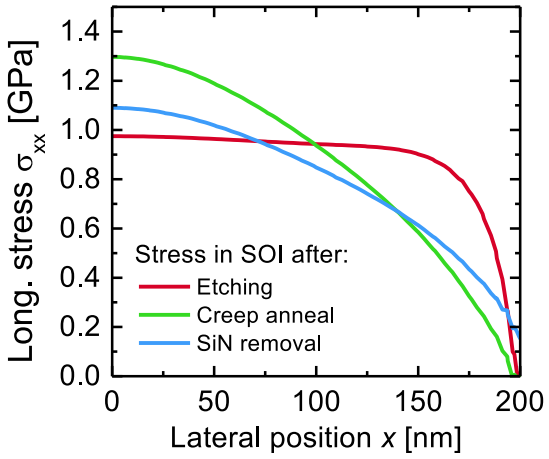


Figure 5.15: Stress profiles for the different BOX-creep process steps, extracted from Figure 5.12. After SiN removal, tensile stress is maintained in the SOI layer (σ_{xx} = 1.1GPa in the middle, i.e. at x=0).

initial stress in the SiN layer and the level of stress finally obtained after the BOX-creep module at the center (x=0) and under the conditions of reference. As a consequence, the BOX-creep technique can be used to induce either a tensile or a compressive stress.

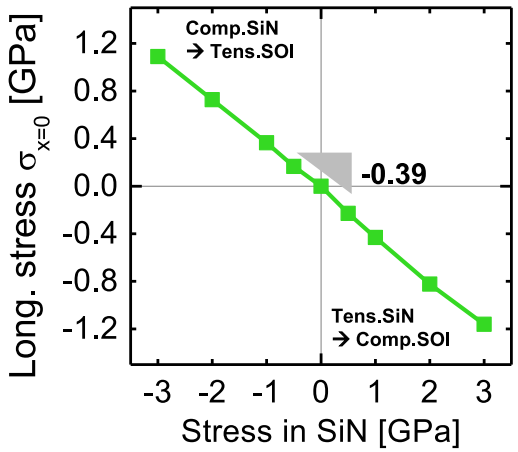


Figure 5.16: Simulated stress in the middle of the active area according to the initial stress in the SiN layer. Good proportionality is observed making BOX-creep technique suitable for both compressive and tensile stress generation in the SOI layer.

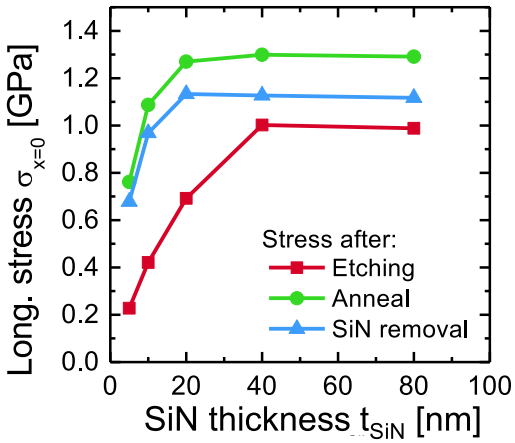


Figure 5.17: Impact of SiN thickness. Saturation of the final level of stress in the SOI. This is because a thick enough SiN totally relaxes and thus fully transfers its lattice deformation (i.e. strain) into the SOI.

The impact of the SiN layer thickness is reported in Figure 5.17, showing a saturation for SiN thicknesses above 20nm. This is because a thick enough SiN totally relaxes its elastic energy, generating the maximum strain into the SOI layer.

5.2.2.d The role of pad oxide and layout effect

During the anneal, not only the buried oxide creeps but also does the pad oxide. Because the pad oxide is located between the SOI and the SiN, its creeping results in a SiN stress relaxation without

an efficient strain transfer into the SOI. This parasitic creeping is responsible for the decrease of the SOI stress after a certain anneal time (see Figures 5.13 and 5.14). Consequently, the thinner the pad oxide, the higher the stress generated in the SOI layer as depicted in Figure 5.18.

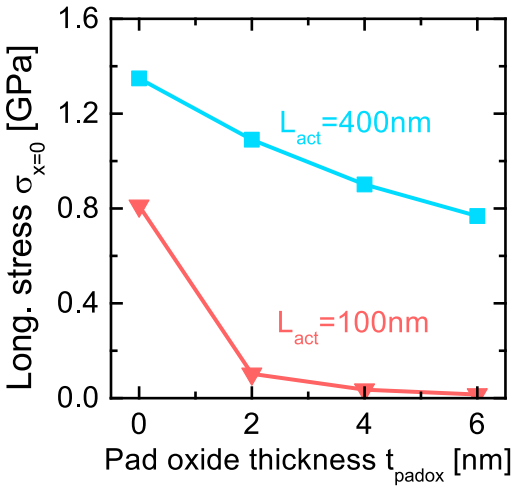


Figure 5.18: Impact of pad oxide thickness for two different active lengths. Strong impact of the presence of a pad oxide for L_{act}=100nm.

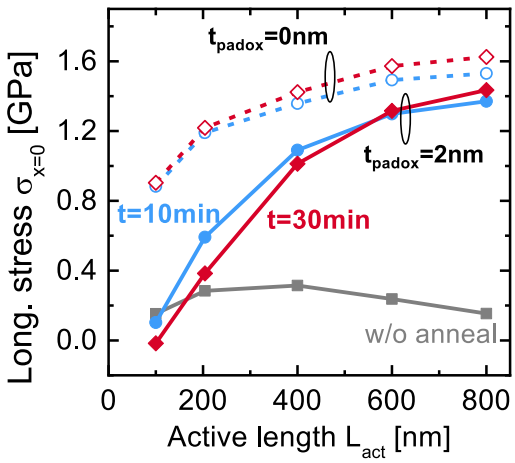


Figure 5.19: Impact of the layout dimension. The loss of efficiency for short active lengths is mainly due to the pad oxide creeping since the stress is highly increased when the pad oxide is not present.

Furthermore, without any pad oxide, a +0.8GPa improvement is achieved for a scaled active of L_{act} = 100nm. This is translated into the layout effect presented in Figure 5.19. With a 2nm-thick pad oxide, the stress strongly reduces for short active areas while a high stress is maintained without pad oxide. This is because the region of the pad oxide located close to the active edge is subjected to a high shear stress induced by the SiN elastic relaxation. In this region, the pad oxide viscosity is thus strongly reduced, leading to a poor strain transfer from SiN to SOI.

5.2.2.e Compatibility with SiGe channel

For pMOS, a high compressive stress can be obtained by integrating SiGe in the channel, e.g. thanks to SiGe enrichment as discussed in Chapter 3. In order to introduce an additional compressive stress, a tensely stressed SiN layer must be used. This is the case of LPCVD SiN exhibiting a tensile stress around 1GPa.

Figure 5.20 shows that with a pad oxide, the BOX-creep is detrimental as it allows the SiGe layer to relax [1]. BOX-creep is however beneficial if no pad oxide is used for active lengths longer than 200nm while shorter actives are not impacted.

Using a compressive SiN is an efficient way to relax the compressive stress in SiGe, as shown in Figure 5.21. Yet, there is an interest in relaxing the SiGe stress. In <110>-oriented channel, the transverse stress is detrimental for hole mobility (as widely discussed in previous Chapters). A

1 In these simulations focusing on the BOX-creep mechanism, the relaxation of SiGe is modeled under elastic considerations. This assumption has been found to be inadequate to explain the measured SiGeOI relaxation in Chapter 3.

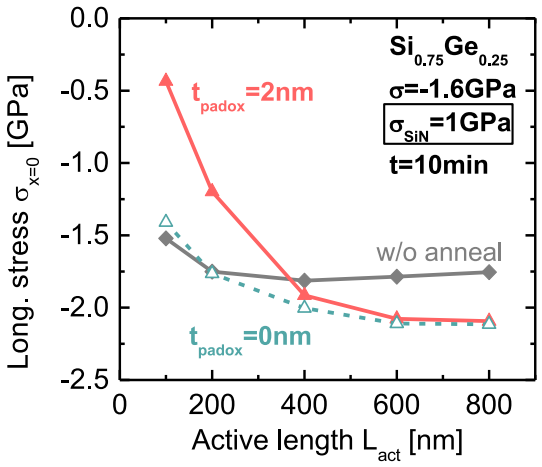


Figure 5.20: Simulated stress in the middle of the SiGe active area after BOX-creep with initially *tensely* stressed SiN layer. Without pad oxide, BOX-creep results in a slight increase of compressive stress in SiGe. With a pad oxide however, BOX-creep is detrimental as it allows the SiGe layer to relax. This is because the pad oxide creeping prevents the strain from SiN to be transferred.

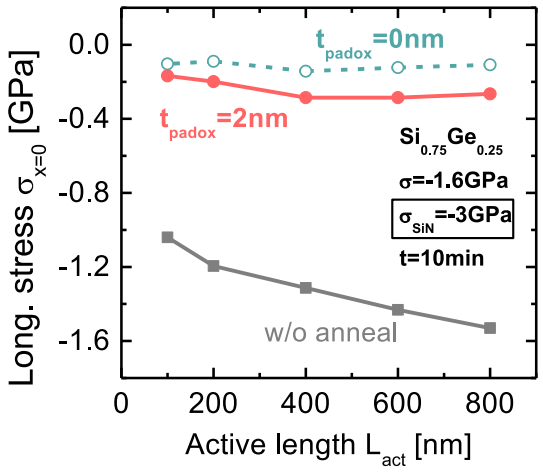


Figure 5.21: Simulated stress in the middle of the SiGe active area after BOX-creep with initially *compressively* stressed SiN layer. Strong relaxation of the SiGe compressive stress is expected.

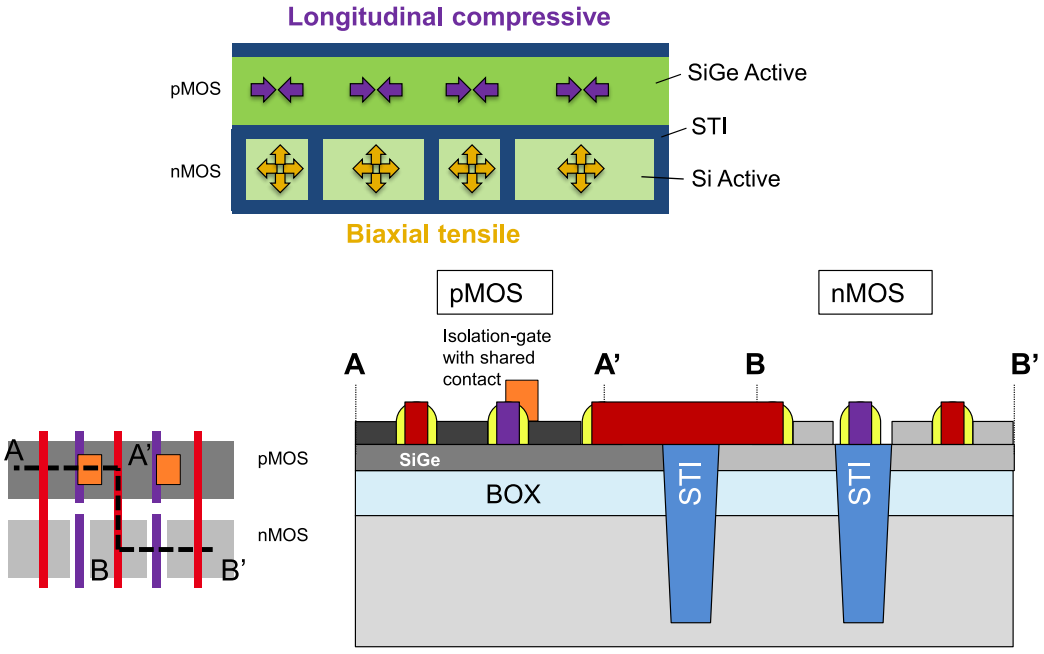


Figure 5.22: Illustration of stress configuration co-optimization by BOX-creep technique. A compressive SiN is used for the BOX-creep, introducing tensile stress after annealing. The isolation of nMOS is made with STI in both longitudinal and transverse directions to take benefit of the BOX-creep technique. The pMOS featuring SiGe channel is patterned only in the transvere direction, enabling the transverse stress to relax. Isolation-gates are used in the pMOS row as in a Continuous-RX approach (see section 4.2.2).

possible integration scheme aiming at co-optimize the performance of both nMOS and pMOS is presented in Figure 5.22.

The idea consists in using a single SiN layer, compressively stressed. In order to take advantage of the BOX-creep technique for both nMOS and pMOS, a dedicated patterning must be used. The active area of nMOS must be patterned in both longitudinal and transverse directions. On the other hand, the patterning of the pMOS active area must be done in the transverse direction only, ensuring that the longitudinal compressive stress is maintained. This way, after the strain transfer, the stress configuration is optimized for both nMOS (tensile in longitudinal and transverse directions) and pMOS (compressive in longitudinal only). The isolation of pMOS can be done by the means of an isolation-gate (see section 4.2.2) or by a local oxidation (see section 4.3.2); the latter requiring an additional mask however.

5.2.2.f Conclusion on mechanical simulations

Thanks to mechanical simulations, we assessed the BOX-creep technique to locally introduce stress in SOI. From the results, different observations can be made:

- √ The BOX-creep technique can generate either a tensile or compressive stress using a compressive, tensile SiN, respectively.
- √ The SiN layer must be at least 20nm in order to maximize the strain transfer into the 6nm-thick SOI.
- √ The presence of a pad oxide leads to a parasitic creeping, resulting in an optimum anneal duration.
- √ The presence of a pad oxide is also dramatic for short active areas.
- √ A relevant patterning design can be relevant to co-optimize nMOS and pMOS with the BOX-creep technique, using a single SiN, compressively stressed.

5.2.3 Electrical results

The BOX-creep technique has been integrated on FDSOI devices in order to evaluate its impact on the electrical performance. First, the use of a tensile SiN for BOX-creep has been investigated in the 14nm FDSOI technology (Aurore Bonnevialle's work [Bon16c]). We analyzed the layout effects inherent to this study. Then, we integrated the BOX-creep technique using a compressive SiN into LETI's FDSOI route.

5.2.3.a BOX-creep with tensile LPCVD SiN

In the 14nm FDSOI route, the SiN hard mask used for the active patterning is deposited by LPCVD. This 55nm-thick SiN features a tensile stress of approximately 1.2GPa. The BOX-creep anneal is done after the etching, i.e. before the STI filling. It is performed at 1100°C for 15min under N_2 atmosphere. This anneal is the only step that differs from the 14nm FDSOI process of reference.

Figure 5.23 shows the I_{EFF}/I_{OFF} trade-off for both nFET and pFET nominal devices. The nFET drive current is degraded by -4% at a given leakage while pFET one is enhanced by +6%. These variations are consistent with the introduction of a compressive stress by the BOX-creep technique, degrading the electron mobility and enhancing the hole one.

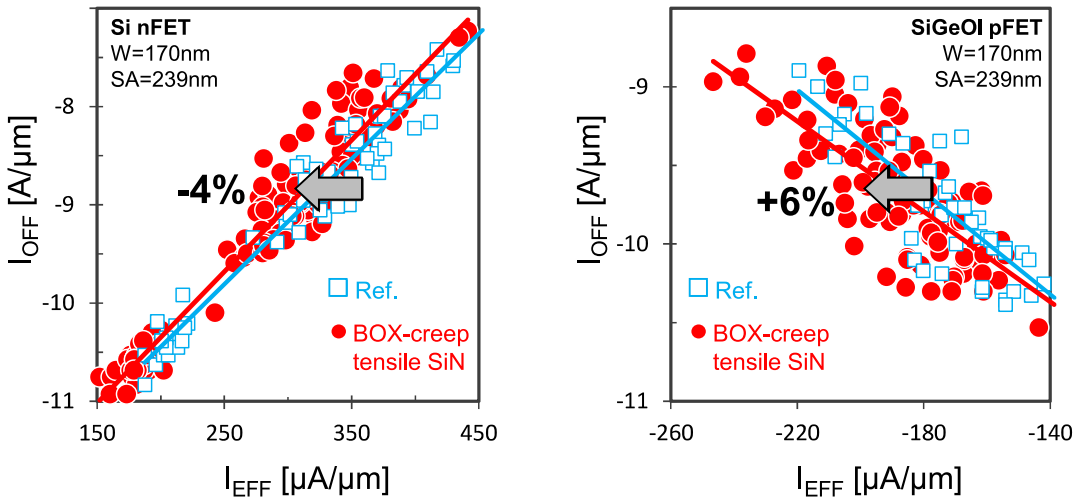


Figure 5.23: I_{EFF}/I_{OFF} trade-off for W=170nm SA=239nm (left) nFET and (right) pFET from 14nm FDSOI technology at V_{DD}=0.8V. The BOX-creep consists in an anneal at 1100°C for 15min after active patterning. The SiN tensile stress is approximately 1.2GPa. The drive current of nFET is degraded by -4% at the same leakage, while the one of pFET is enhanced by 6%. This result is consistent with the generation of a compressive stress in the channel.

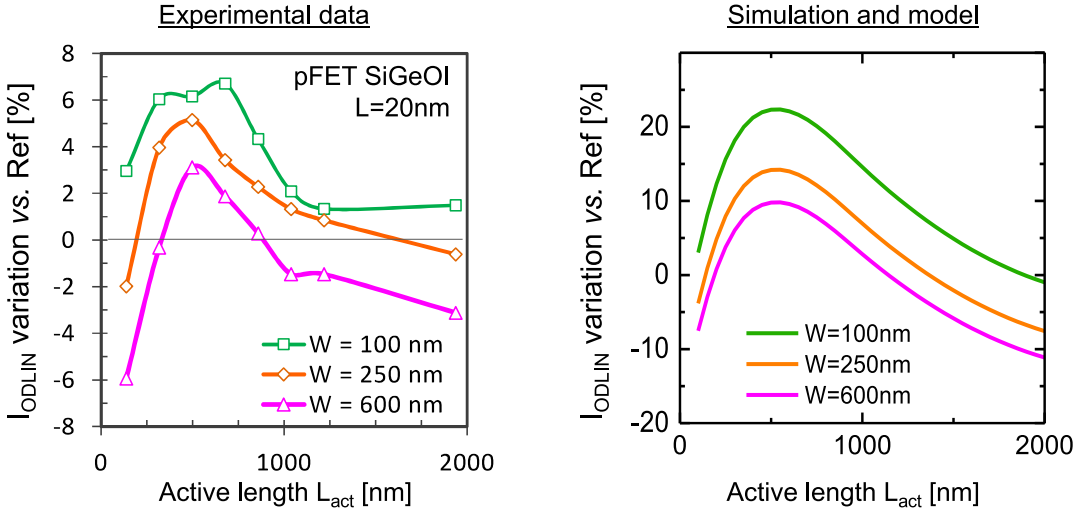


Figure 5.24: 14nm FDSOI BOX-creep pFET I_{ODLIN} variation w.r.t the reference according to the active length for different widths from (left) experimental measurements and (right) simulation and model. The highest gain is achieved for W=100nm and L_{act}≈500nm. The trend is qualitatively reproduced by the mechanical simulation and mobility model.

Figure 5.24 shows the pFET I_{ODLIN} variation with respect to the reference according to the active area length L_{act} and width W. The I_{ODLIN} variation is compared to the prediction from mechanical simulation and mobility variation (from piezoresistive model, see section 3.4.1). The experimental trend is qualitatively well predicted. Especially, there is an optimal active length (around 500nm) and the highest gain is achieved for the narrowest active. This sweet point is obtained when the BOX-creep technique introduces a compressive stress with a predominant longitudinal component.

Nevertheless, the model prediction overestimates the I_{ODLIN} variation, suggesting that the strain transfer efficiency is not as high as expected from the simulation.

5.2.3.b BOX-creep with compressive PECVD SiN

The introduction of compressive stress by the means of the BOX-creep technique has been discussed in the previous section. Regarding the electrical characteristic variations, the level of generated compressive stress is low, making the use of SiGe channel and source/drain more efficient to boost the pFET performance. The interest of the BOX-creep technique could rather lie in local introduction of tensile stress in order to boost the nFET performance. This requires a compressively stressed SiN. We evaluated the BOX-creep technique with a compressive SiN integrated in a LETI's route. The experiment is presented in Figure 5.25. The SiN layer, deposited by PECVD, features a compressive stress of approximately -3GPa. The anneal is performed at 1100°C under N2 atmosphere for 15min after active patterning in a mesa configuration. Two stacks have been considered: with and without pad oxide between the SOI and the SiN. This split is the consequence of the mechanical simulation conclusions (section 5.2.2). SEM top view images after active patterning and SiN wet removal as well as after gate patterning are presented in Figure 5.25.

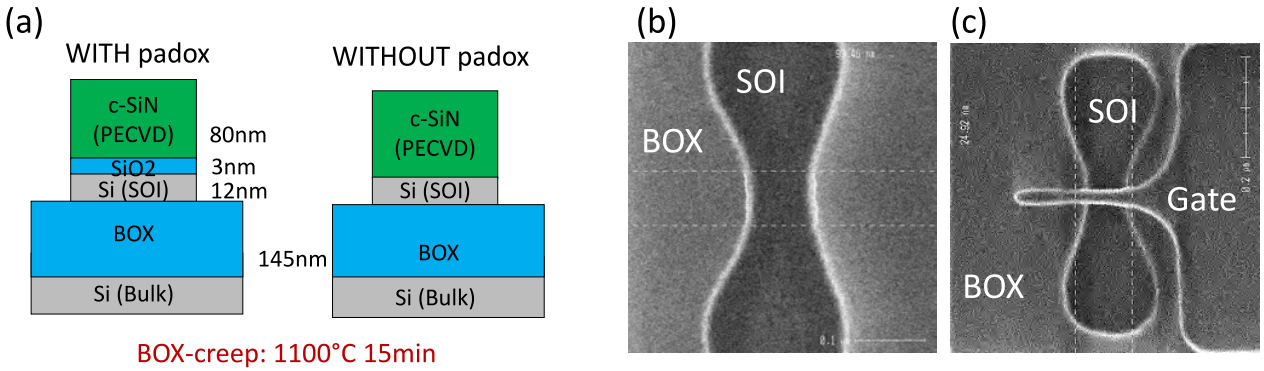


Figure 5.25: Presentation of BOX-creep technique integrated into LETI's device route. (a) Stack after active patterning for the two configurations with and without pad oxide. The etching is mesa (and not deep trenches as in STI). The buried oxide is 145nm thick. SEM top view after (b) SiN removal and (c) gate patterning.

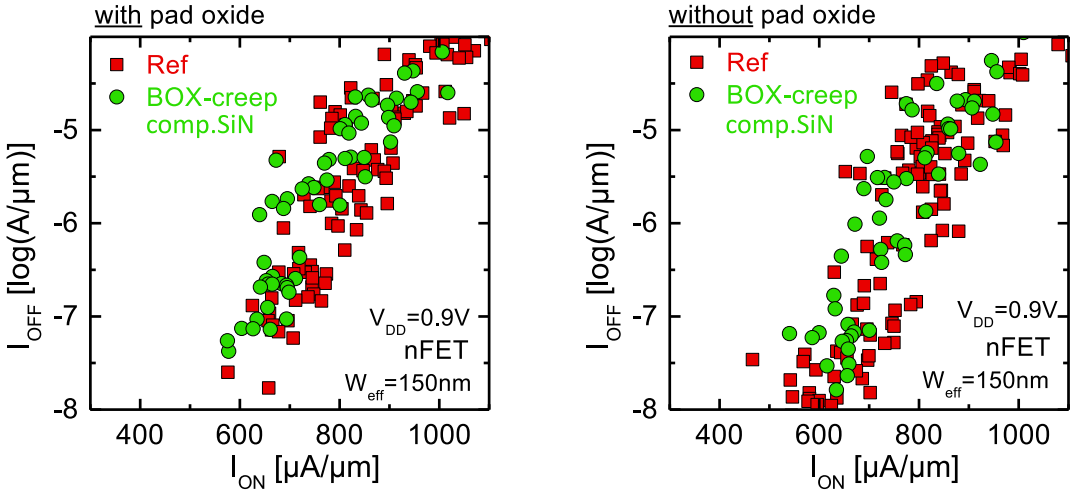


Figure 5.26: I_{ON}/I_{OFF} trade-off for nFET devices after BOX-creep (left) with a pad oxide and (right) without pad oxide. The SiN used for BOX-creep, deposited by PECVD, is compressively stressed ($\sigma_0 \approx -3$GPa). The anneal is performed at 1100°C for 15min. The BOX-creep technique has low impact on performance, suggesting an inefficient strain transfer.

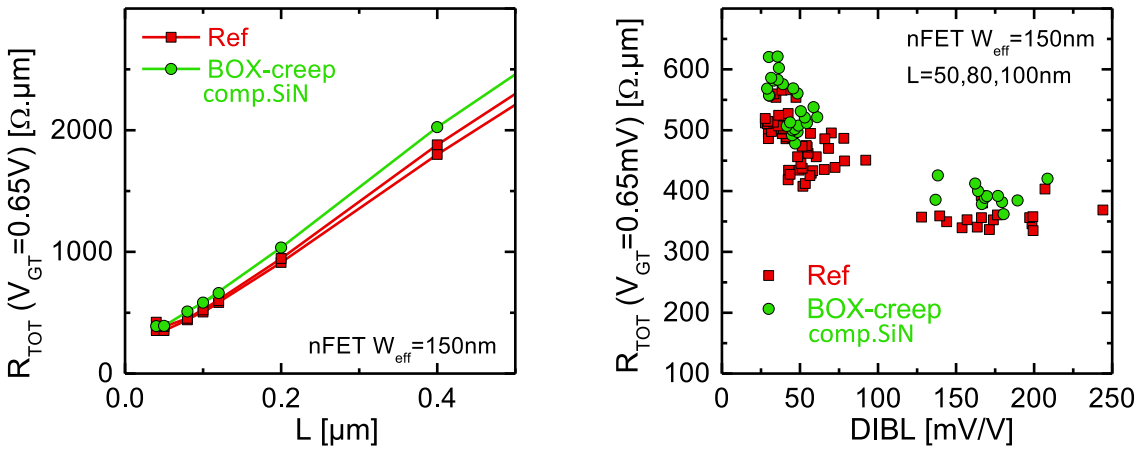


Figure 5.27: R_{TOT} *vs.* (left) gate length L and (right) DIBL for nFET with BOX-creep (15min anneal at 1100°C with PECVD SiN $\sigma_0 \approx -3GPa$) compared to the reference, i.e. without anneal (two wafers). While the electrostatic control is not impacted by the BOX-creep, the total resistance is degraded. This result is not consistent with a tensile stress generation into the SOI.

Figure 5.26 shows the electrical results of performance/leakage trade-off of the fabricated nFETs. The investigated devices feature an effective width of W_{eff}=150nm [1]. The BOX-creep technique has low impact on performance as the I_{ON}/I_{OFF} trade-off is similar to the reference. This result suggests that the BOX-creep failed to introduce a significant stress in the SOI. The same conclusion can be drawn on the stack without pad oxide.

Figure 5.27 focuses on the total resistance R_{TOT}, plotted as a function of the gate length or DIBL. While the electrostatic control is not altered by the BOX-creep, the R_{TOT} is slightly degraded compared to the reference. This might be the consequence of a compressive stress introduction by BOX-creep, degrading the electron mobility, even though a tensile stress was expected using a compressive SiN.

5.2.4 Discussion and perspectives

From the mechanical simulations, the BOX-creep technique is promising to locally introduce stress. However, experiments have not shown a significant gain on device performance. The use of tensile SiN (LPCVD) to introduce a compressive stress has shown only +6% pFET effective current improvement. Worst, the use of a compressive SiN (PECVD) to introduce a tensile stress has resulted in slightly degraded nFET R_{TOT} compared to the reference. This result indicates that no tensile stress has been generated.

The high level of compressive stress measured in [Bon15a] by µRaman has been obtained with a 1200°C anneal. In our case, the anneal temperature is 1100°C, which is the maximum temperature available internally for 300mm wafer tool. Such a difference might explain our result. But more probably, the PECVD behavior under high temperature anneal could be responsible for the failure

1 In our experiment, the top width is W_{top}=130nm and the SOI thickness is 10nm, which leads to $W_{eff}=W_{top}+2H$=150nm.

of tensile stress generation. Figure 5.28, adapted from [Ses12], shows that the compressive stress in PECVD SiN disappears under high temperature anneal. The SiN layer can even become tensely stressed after the anneal. This is confirmed by measurements of [Bon16a] presented in Figure 5.29. The compressive stress in PECVD SiN rapidly decreases after an anneal at high temperature. In this experiment, the PECVD SiN stress goes from -2GPa compressive as deposited to 0 (+0.5GPa tensile), after 10s (100s, respectively) at 1100°C. The change of stress is attributed to the Hydrogen desorption [Ben06; Bon16a; Ses12].

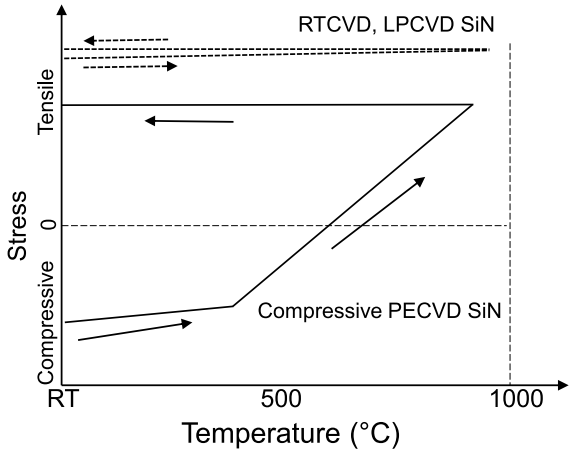


Figure 5.28: Evolution of stress in SiN according to the temperature, from [Ses12]. Both compressive SiN (PECVD) and tensile SiN (LPCVD) are considered. The PECVD SiN loses its compressive stress as the temperature increases. The stress can even be tensile after cooling.

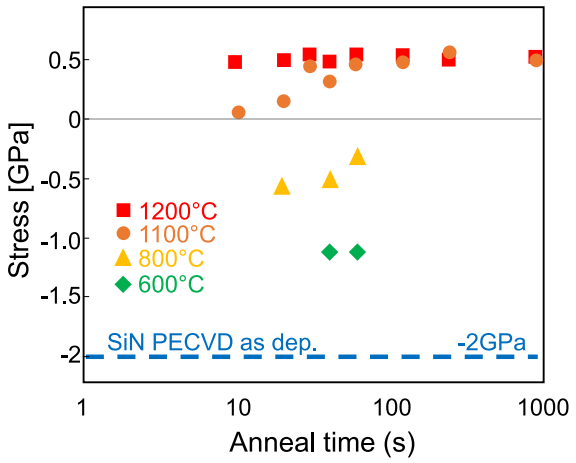


Figure 5.29: Evolution of PECVD SiN stress according to the anneal time, for different anneal temperatures, from [Bon16a]. The compressive stress obtained after deposition (-2GPa) rapidly decreases. After 10 seconds at 1100°C, the SiN is totally relaxed. For longer anneal, the SiN stress becomes tensile.

This SiN stress evolution with temperature, not taken into account in our simulations, could explain the inefficient tensile stress generation. Besides, considering that the PECVD SiN stress becomes tensile during the anneal, the BOX-creep can even result in a compressive stress generation into SOI. This would be consistent with the degraded nFET performance observed in Figures 5.26 and 5.27.

Since we have shown that the use of compressively stressed PECVD SiN is inefficient to locally introduce a tensile stress with the BOX-creep technique, we might consider the use of a different material. For instance, TiN appears as a promising candidate for stress considerations. Especially, the BOX-creep technique can take advantage of the coefficient of thermal expansion mismatch with Silicon (CTE_{Si}=3.10^{-6}K^{-1} *vs.* CTE_{TiN}=9.10^{-6}K^{-1} [Sch96]). This CTE mismatch induces a compressive stress in TiN at high temperature, enabling tensile stress generation in SOI by the means of BOX creeping. This concept has been evaluated by mechanical simulations, presented in Figure 5.30 (see section 5.2.2 for simulation hypotheses). It is worth noting that the TiN stress is assumed to be null after deposition, which is an optimist case as TiN deposited by PVD can be compressively stressed (-3.5GPa in [And06]). The compressive stress in TiN would add up to the one induced by CTE mismatch.

The stress profile in the SOI layer along the BOX-creep process is shown in Figure 5.30 (c). After

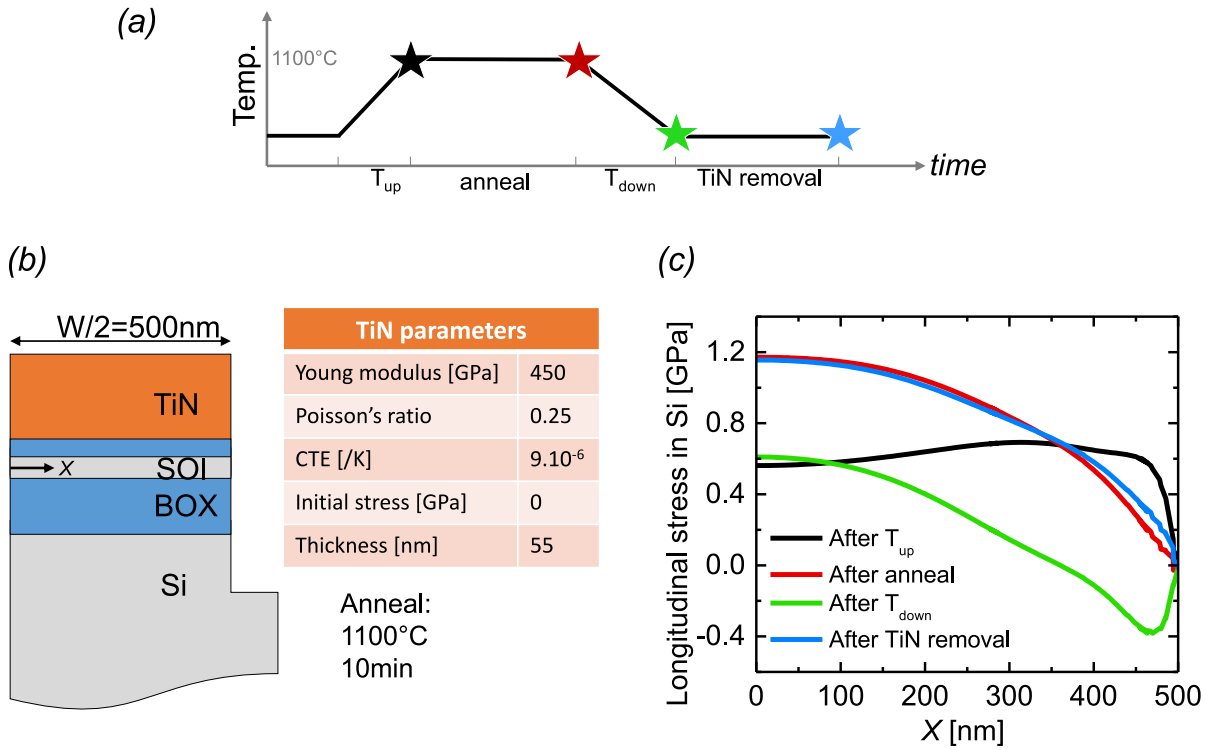


Figure 5.30: Principle of BOX-creep technique taking advantage of coefficient of thermal expansion mismatch. Mechanical simulation assuming TiN material. (a) Temperature along the different process steps (temperature ramp-up, anneal, temperature ramp down and TiN removal). (b) Mechanical simulation structure and parameters related to TiN (other parameters are the ones used in section 5.2.2). The TiN stress after deposition is considered null. (c) Longitudinal stress generated in the SOI along the different process steps. After TiN removal, tensile stress is expected.

the temperature ramp up, a tensile stress appears in the SOI due to the compressive stress in TiN induced by CTE mismatch. After the anneal, the creeping of the BOX leads to strain transfer from TiN to the SOI. The TiN stress is relaxed at this step. After the temperature ramp down, the CTE mismatch affects the structure in the opposite way as for the ramp up. The TiN is this time tensely stressed, which is translated into compressive stress in SOI (or at least a reduction of the tensile stress in SOI). However, this effect is canceled out when the TiN layer is removed, resulting in a tensely stressed SOI layer (σ=1.2GPa in the simulation conditions).

5.3 The SDRASS technique

This section discusses a strain integration technique aiming at generating a tensile strain in order to boost the nMOSFET performance. This technique is based on the so-called STRASS technique (Strained Si by Top Recrystallization of Amorphized SiGe on SOI) [Bon15b; Hal16; Mai15]. In our case, the technique is used in source/drain region, hence we name this technique SDRASS for Source and Drain from Recrystallization of Amorphized SiGe on SOI.

5.3.1 Introduction: the STRASS technique

The STRASS technique consists in generating a tensile strain by the means of a top-down Solid Phase Epitaxial Regrowth (SPER) of Silicon from a relaxed SiGe seed. Starting from a SOI, an heteroepitaxy of SiGe is performed. The SiGe layer is compressively strained because of the lattice mismatch with Silicon [1]. Then, the SOI and the SiGe layer are amorphized by ion implantation. By carefully chosing the conditions of implantation (specy, dose and energy), the top part of the SiGe layer can remain crystalline [Bon16a; Cla88; Mok05]. This crystalline layer is used as a seed for the next step: top-down recrystallization by Solid Phase Epitaxial Regrowth (SPER) [Pay16]. If the SiGe seed is relaxed, the SPER will result in a tensile strain generation into the SOI. The SiGe can then be selectively removed by a wet etching to finally yield a strained-SOI layer. It has to be pointed out that this technique is only relevant for FDSOI. In bulk, the implantation will result in a "sandwich" amorphous region and therefore the recrystallization will occur at two fronts simultaneously.

Tensile strain generation with the STRASS technique has been experimentally demonstrated (measured by µRaman spectroscopy) [Bon16b]. The high level of stress measured ($\approx$ 1.5GPa) suggests that the SOI recrystallization followed the lattice of relaxed SiGe.

5.3.2 SDRASS principle and experiment details

The STRASS technique is promising for locally introducing a tensile strain. However, the crystal quality of the channel can be deteriorated by the amorphization/recrystallization process, especially for non-optimized conditions. The presence of defects (dislocation or stacking faults) is dramatic for the MOSFET operation and would result in a poor yield. That is why we use the STRASS technique in the source/drain region only, in order to maintain a channel of good crystal quality. The process flow, described in Figure 5.31, is as follows:

- Starting with a SOI substrate of 10nm-thick Si and 145nm-thick BOX, the active area mesa patterning, gate-stack deposition and patterning, and spacer deposition and patterning are performed according to LETI's Ω-gate nanowire route.
- Epitaxy of 20nm-thick SiGe with 30% of Germanium in the source/drain regions. The SiGe is compressively strained.
- Implantation of Silicon at 40keV with a dose of 2.5 10^{14} cm^{-2} (not tilted). This implantation condition has been chosen according to the results of [Bon16b] in order to amorphize the SOI

1 Plastic relaxation can occur if the SiGe layer thickness exceeds the critical thickness [Har11].

and SiGe layers except for a top SiGe seed. Further optimization of these process conditions are possible. The channel region is protected by the gate (the SiN hard mask is present).

- Anneal at 600°C for 20min for top-down recrystallization through SPER.
- SiGe removal by selective wet etching.
- Anneal at 600°C for 2min.
- Epitaxy of Silicon for raised source/drain, consistently with the process of reference.
- End of process of reference (dopant implants, activation, MEOL)

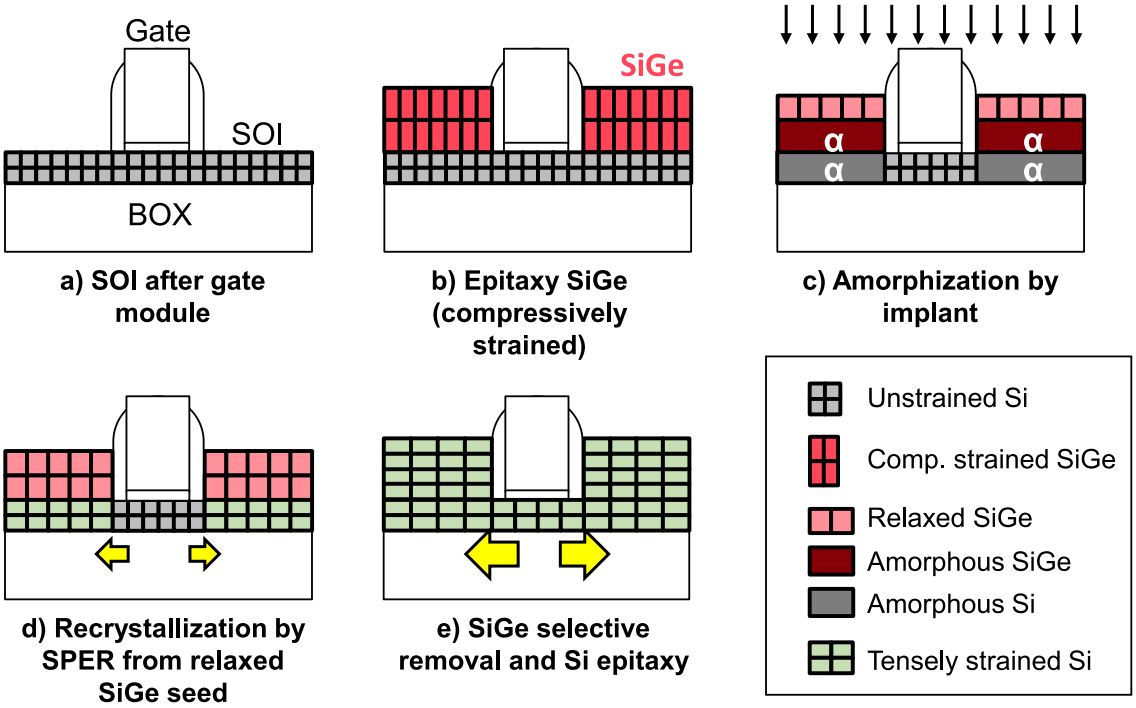


Figure 5.31: Process flow of the SDRASS technique. a) SOI device after gate module fabricated in a gate-first scheme. b) Heteroepitaxy of SiGe in the source/drain region. SiGe is compressively strained because of the lattice mismatch with Silicon. The Germanium concentration used in our experiment is 30%. c) Amorphization by Si implant at 40keV with a dose of 2.5 10^{14} cm^{-2}. This condition has been chosen according to the results of [Bon16b]. d) Recrystallization from the top seed of relaxed SiGe by Solid Phase Epitaxial Regrowth (SPER) consisting in an anneal at 600°C for 20min. The amorphous Silicon recrystallizes according to the lattice parameter of relaxed SiGe. It is thus tensely strained. e) SiGe selective removal by wet etching and epitaxy of Si for raised source and drain. This step allows a higher strain transfer into the channel thanks to the high volume of tensely strained source/drain.

5.3.3 Morphological results

Figure 5.32 shows a TEM image of a short channel device after the amorphization by implantation. Zooms in the two regions of the channel (A) and the source/drain (B) are shown in Figure 5.33. The high resolution TEM image of the channel region shows a defect-free crystal. This highlights that the channel is well protected by the gate during the implantation. In the source/drain region, the stack is constituted bottom to top of the BOX, the amorphous SOI, the amorphized part of SiGe and the crystalline SiGe seed. The crystalline SiGe thickness is around 7nm with a relatively rough interface with the underneath amorphous region. Nevertheless, the crystalline SiGe layer appears as continuous (i.e. the amorphous region does not reach the top surface). This configuration is desirable

for the next step of recrystallization.

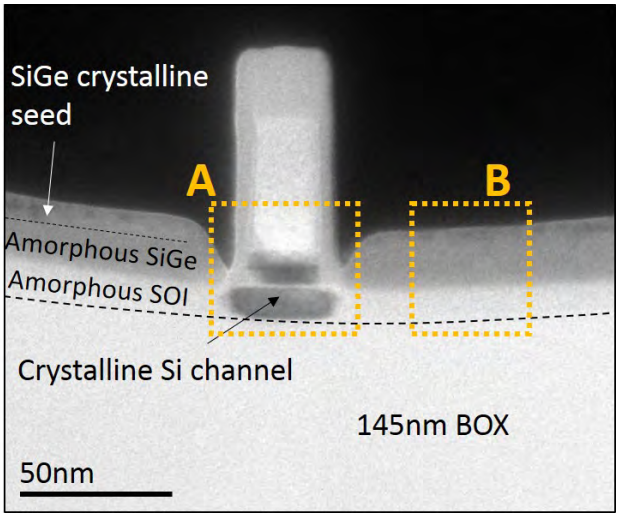


Figure 5.32: TEM after the SDRASS amorphization showing the top seed of crystalline SiGe in source/drain. The underlying SOI is amorphous while the channel is still crystalline since it is protected by the gate.

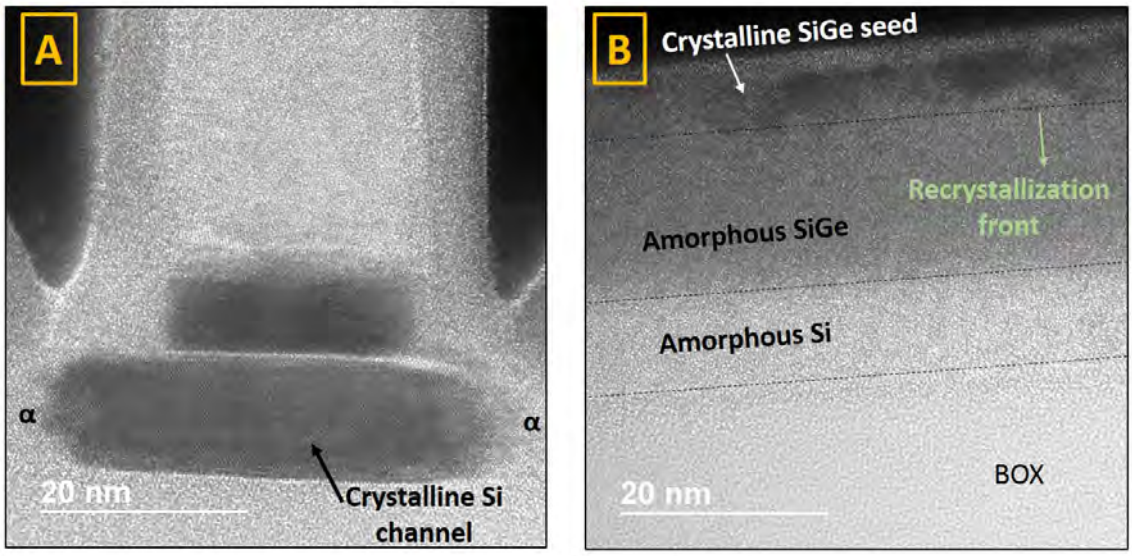


Figure 5.33: High resolution TEM after the SDRASS amorphization of the (A) channel region and (B) source/drain region. The channel is perfectly crystalline while the SOI in B region is amorphous after implantation. The top of the SiGe layer is crystalline and will act as a seed for recrystallization during the annealing.

A TEM image of a device after the SPER, which consists in a 20min anneal at 600°C, is shown in Figure 5.34. A focus is made on the channel region and especially at the junction, i.e. below the spacer. Defects are observed in the SOI layer in the source/drain region. In particular, defects are generated because of the recrystallization occurring from the crystalline channel which acts as a seed during SPER. Nevertheless, these defects are located far enough from the channel as evidenced on the TEM image. It is expected that these defects will not deteriorate the transport in the channel.

Figure 5.35 shows three different TEM images in the source/drain region after recrystallization. Even though the presence of defects is evidenced in both the SiGe and the SOI layers, the SOI layer has fully recrystallized from the SPER.

After SiGe selective removal, the Si layer thickness is measured at 8.5nm by ellipsometry, which is

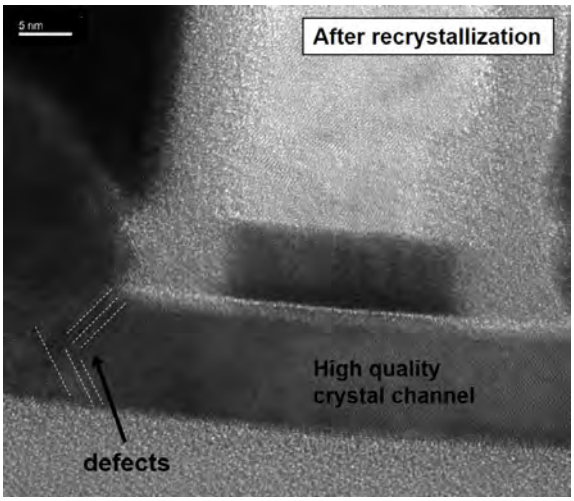


Figure 5.34: TEM after the SDRASS annealing of 20min at 600°C under N_2. Focus on channel region shows perfect crystal under the gate and spacers. Defects (stacking faults) are observed at the extremity of the channel, probably resulting from the different recrystallization rates of <100> and <110> crystal orientations.

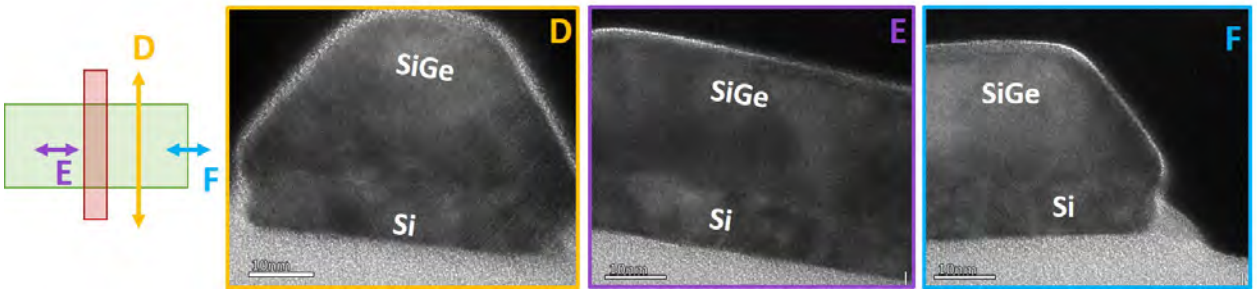


Figure 5.35: TEM after the SDRASS annealing in different source/drain regions. Cut D is transverse. After annealing, the SiGe/Si bilayer is crystalline with defects, especially in the Si layer.

highly sufficient for the epitaxial growth of the raised source/drain. The thickness measurement by ellipsometry after Si epitaxy confirms that the growth has gone well despite the presence of defects in the underlying SOI.

5.3.4 Electrical results

Transistors with SDRASS integration scheme have been electrically characterized and compared to the reference process.

Electron mobility has been extracted by split-CV technique (see section 2.1.1) on a long channel device. A similar mobility as the reference process is observed. As the SDRASS integration scheme aims at generating strain from the source/drain region, it is not expected to alter the long channel characteristics. The gate-to-channel capacitance measurement shows a significant effective oxide capacitance reduction with SDRASS. This is synonym of EOT (Equivalent Oxide Thickness) increase. This could be attributed to the thermal budget inherent to the annealing at 600°C during 20 minutes. Further investigations are however required to explain such an EOT increase.

The linear drain current of devices with gate lengths of L=1µm and L=80nm are shown in Figure 5.37. In subthreshold regime, the leakage is degraded with SDRASS. Especially, the $I_D(V_G)$ behavior suggests a parasitic transistor (double subthreshold swing). Nevertheless, this behavior is also visible on some of the reference samples for L=1µm. In addition, certain dies of SDRASS at L=80nm do

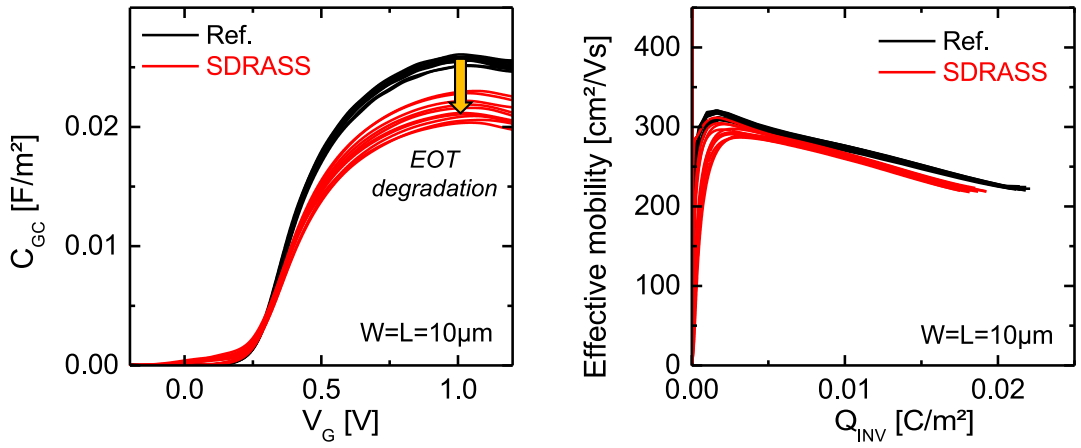


Figure 5.36: (left) Gate-to-channel capacitance *vs.* gate voltage for SRASS and reference integration schemes. The C_{GC} is lower for SDRASS, highlighting a lower EOT. (right) Long channel electron effective mobility extracted by split-CV (see section 2.1.1). Similar mobility is observed for both SDRASS and reference integration schemes.

not feature this parasitic leakage. From these observations, it is suggested that the strong leakage is not directly related to the SDRASS integration scheme but rather a side-effect that is strengthened by the experiment.

In the strong inversion regime, the SDRASS linear drain current behavior is similar to the reference process. The lower current for L=1µm is attributed to the EOT increase evidenced in Figure 5.36. For L=80nm, the current degradation is not as obvious. This could be because the access resistance plays a more significant role at such a gate length. In order to evaluate the access resistance and mobility contributions, we performed the access resistance extraction according to the Y-function based methodology, as discussed in Chapter 2.

The $\Theta(\beta)$ plots are shown in Figure 5.38, highlighting same access resistance for both SDRASS and the reference integration schemes, evaluated at 150Ω.µm at V_{GT}=0.5V. Figure 5.38 also shows the extracted mobility at Q_{INV}=0.01C/m^2 as a fucntion of the gate length. The mobility is derived from β parameter, assuming $C_{ox,eff}$=0.025F/m^2 for the reference and $C_{ox,eff}$=0.021F/m^2 for SDRASS. Consistently with the split-CV method, the mobility for L=10µm is not impacted by the SDRASS experiment. For L=80nm, the mobility is improved by +15% with the SDRASS integration. Such a result suggests that tensile strain has been introduced in the channel for this gate length. The EOT increase must however be confirmed for this gate length to ensure that the mobility has been improved.

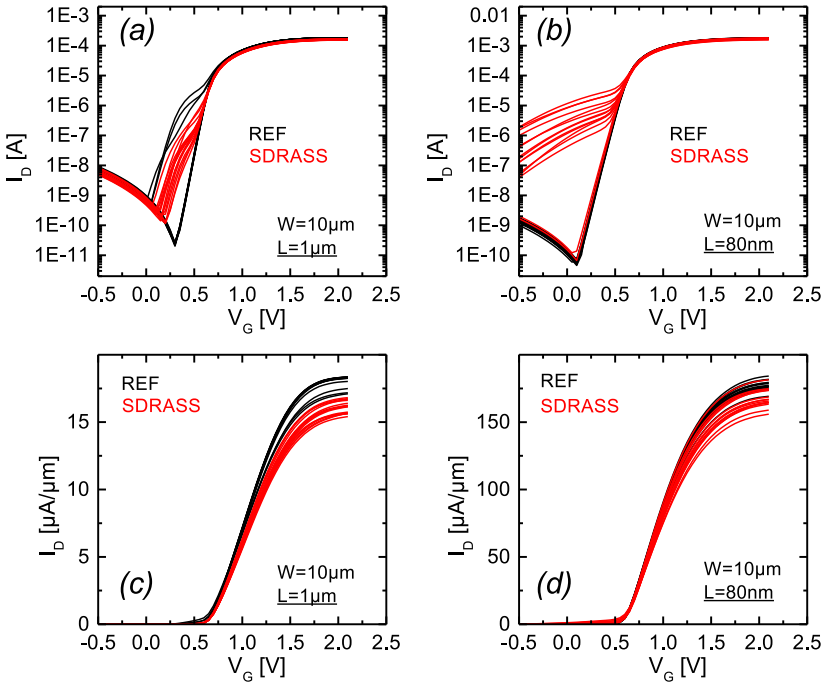


Figure 5.37: Linear $I_D(V_G)$ in log (a,b) and linear (c,d) scales for L=1µm (a,c) and L=80nm (b,d). A high leakage current in subthreshold regime is observed for most SDRASS data. In strong inversion, SDRASS linear drain current shows a similar behavior as the reference. For L=1µm (c), the degradation is attributed to the EOT increase evidenced in Figure 5.36. For L=80nm (d), the degradation is reduced.

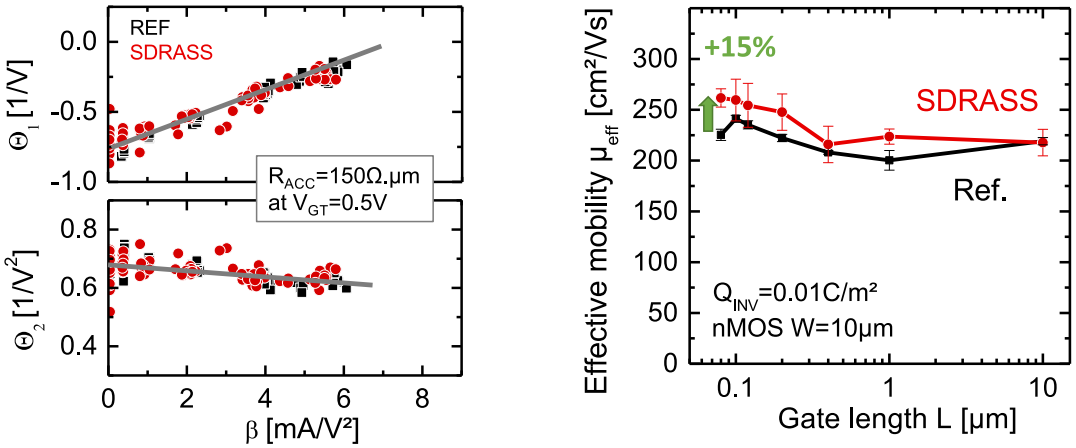


Figure 5.38: (left) Θ_1 and Θ_2 *vs.* β for access resistance extraction (see Chapter 2). Same access resistance for SDRASS and reference is evidenced. (right) Effective mobility extracted as a function of the gate length for both SDRASS and the reference process. For L=80nm, SDRASS leads to +15% mobility enhancement, assuming the EOT increase evidenced in Figure 5.36.

5.3.5 Conclusion and perspectives

The SDRASS technique consists in using the STRASS technique for source/drain regions only, in order to ensure a channel of good crystal quality. It has been implemented into a LETI's FDSOI route. Morphological characterizations have evidenced a successful amorphization/recrystallization of the SOI layer. Even though defects are observed in the source/drain region, the channel features a good crystal quality.

Electrical characterizations revealed an EOT increase with SDRASS, when compared to the reference process. Long channel mobility has been found equivalent for SDRASS and reference process. A strong leakage is observed but not exclusively for SDRASS samples, which makes us think that

this issue is not directly related to the SDRASS experiment. Fine access resistance and mobility extraction has shown that the mobility of L=80nm gate-length devices is improved by +15% with respect to the reference, assuming the EOT increase measured on long channel is conserved on short devices.

Even though these results are promising, physical strain characterization (by NBED, DFEH or PED for instance) are needed to confirm the strain generation. In addition, the relevance of the SDRASS technique for improving the performance has not been demonstrated. This is mainly due to the EOT degradation and requires further investigations.

5.4 Dynamic Back-Bias in 3D-monolithic

5.4.1 Introduction to 3D-monolithic

The 3D-monolithic integration consists in sequentially fabricating levels of transistors on top of each others. The great advantage of such an approach over other 3D integration schemes where the tiers are parallely processed on different wafers and then bonded is the high density of interconnections between the tiers. While the bonding precision limits other 3D integration schemes, the 3D-monolithic integration alignment precision is limited by the lithography. As a result, the density of contacts can reach $10^8/mm^2$ at 14nm node with respect to only $10^5/mm^2$ using Through Silicon Vias (TSVs) [Bru16]. This allows to take advantage of the third dimension at the system level (System-on-Chip), the design level (disruptive computing architecture like in-memory computing) or even down to the transistor level.

3D-monolithic integration enables to design N over P or P over N cells (top tier is nFET, or pFET, and bottom tier is pFET, nFET, respectively) and subsequently optimize both types independently. For instance, using two different channel materials such as III-V for nFET and SiGe for pFET [Des15] . Such an approach has however not been demonstrated to be highly efficient for scaling, because of the area loss for the 3D contacts [Lee13; Shi16]. In a CMOS over CMOS approach, performance gains can be expected from reducing the back-end interconnection lengths [Ayr17; Bil15]. Also, stacking tiers can improve the variability (from global variability component, i.e. across chip variation) [Ayr16].

The challenge of 3D-monolithic integration lies in maintaining the stability of the first tier while the second level is processed. This requires to process the top level at a reduced thermal budget. CoolCube^{TM} has demonstrated the feasibility of fabricating transistors with a "cold" process, i.e. at temperature below 650°C. Especially regarding the critical steps such as dopant activation [Pas16], the raised source/drain epitaxy [Lu17b], the gate stack and back-end-of-line reliability [Lu17a]. Performances within 10% of the reference "hot" process have been achieved. Finally, the functionality of two levels of transistors on 300mm wafers has been demonstrated [Bru16]. The process flow is described in Figure 5.39.

As discussed in the previous chapters, one of the great advantage of the planar FDSOI technology is its high back-bias capability. In this section, we have studied the back-bias in a 3D-monolithic integration context. Especially, we have investigated the asymmetric double-gate capability provided by the totally isolated and possibly local back-gate and the front gate. It enables Dynamic Back-Bias (DBB), opposed to Forward- and Reverse-Back-Bias (FBB and RBB) in which a static bias is applied on the back planes. First, the electrostatic coupling in 3D-monolithic top-tier devices is experimentally demonstrated. Then, the performance of standard cells is assessed thanks to a dedicated 3D Design-Kit with 14nm ground rules. Finally, some perspectives enabled by 3D-monolithic integration on 6T-SRAM cells are discussed.

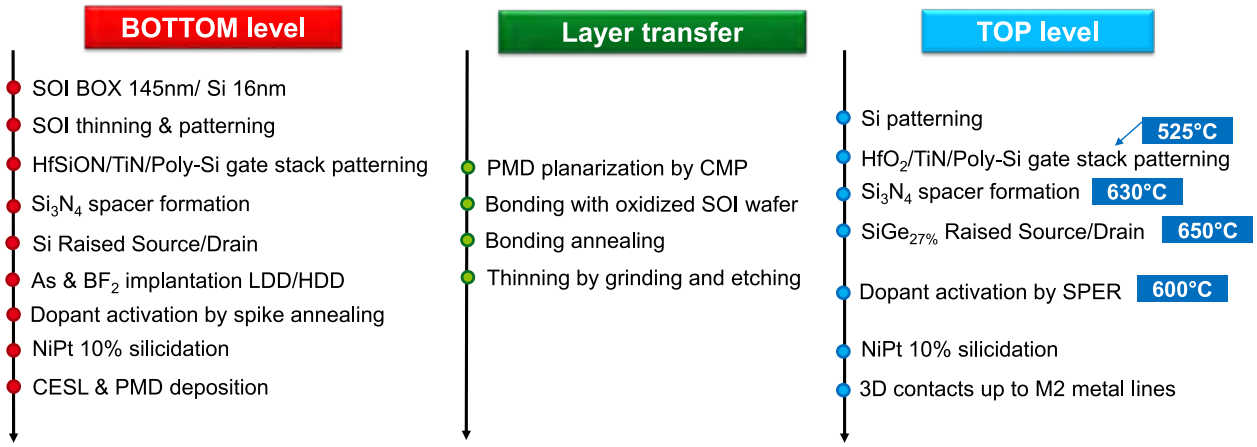


Figure 5.39: Process flow of the 3D-monolithic sequential integration, from [Bru16]. Low thermal budget is required for the second layer processing in order to maintain the stability of the first layer.

5.4.2 Electrostatic coupling in 3D-monolithic

5.4.2.a Experimental results

The electrostatic coupling in 3D-monolithic is experimentally demonstrated on stacked transistors. A typical layout is presented in Figure 5.40. The source, drain and gate of the two transistors are independently connected to pads. The gate of the bottom transistor can thus be used as a back-gate for the top one. The Figure 5.40 also shows a TEM picture of the stacked devices.

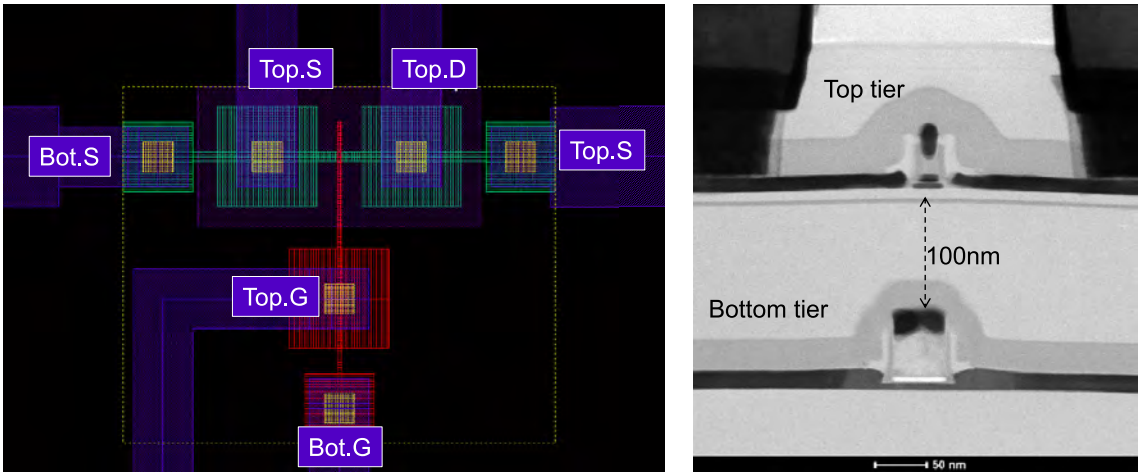


Figure 5.40: (left) Layout of the tested stacked devices. The poly-Si gate of the bottom transistor can be used as a back-gate electrode for the top level one. (right) TEM picture showing the two stacked transistors. The Inter-Layer Dielectric, also called BOX, is approximately 100nm-thick.

The buried line acts as a local back-gate and is able, when statically biased, to shift the top-tier transistor threshold voltage (Figure 5.41). The back-bias efficiency is measured at γ=16mV/V, consistently with the 100nm-thick dielectric stack between the top channel and the bottom poly-Si line (Figure 5.40).

The double-gate behavior enabled by a local back-gate is investigated in Figure 5.42. The double-gate mode V_B=V_G is closely similar to the single gate mode. This is due to the poor electrostatic coupling

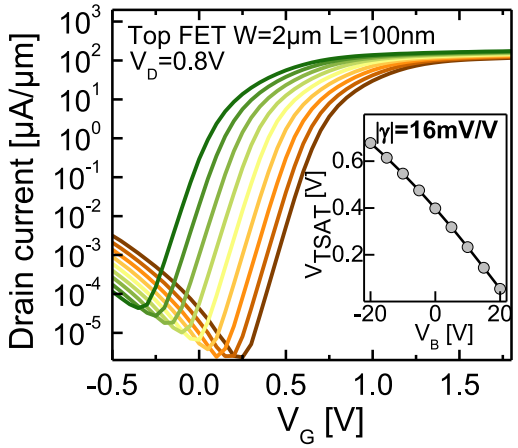


Figure 5.41: Top-tier nMOS transfer characteristics $I_D(V_G)$ in saturation for different back-biases V_B ranging from -20V to +20V. Inset: $V_{TSAT}(V_B)$ showing sensitivity γ=16mV/V. The back-bias V_B is applied on the gate of the bottom transistor (see Figure 5.40).

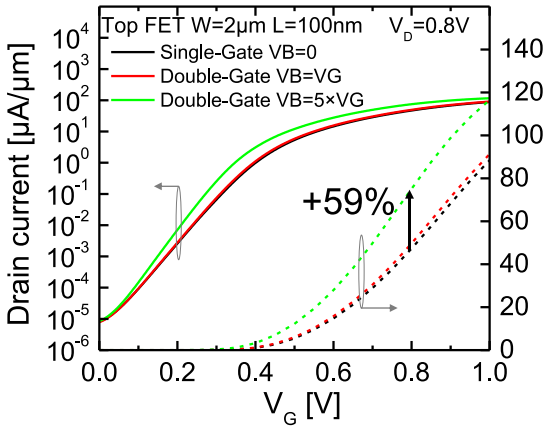


Figure 5.42: Top-tier nMOS $I_D(V_G)$ in log. and linear scales in single- or double-gate modes. Because of the poor electrostatic coupling with the 100nm BOX, the double-gate mode V_B=V_G is closely similar to the single gate mode. In order to first-order emulate a 20nm-thick BOX, V_B=5×V_G is applied, this time leading to +59% I_{ON} over single gate mode.

with a 100nm-thick BOX. In order to first-order emulate the sensitivity of a 20nm-thin BOX device in the double-gate regime, a back-bias of V_B=5×V_B is applied. Doing this, I_{ON} at V_{DD}=0.8V is improved by 59% while I_{OFF} is kept the same as in the single-gate mode (Figure 5.42). This experimentally highlights that a local back-gate connected to the top gate can greatly boost the I_{ON}/I_{OFF} trade-off of the top-tier transistors.

5.4.2.b 3D 14nm Design-Kit

In order to design a local back-gate for the top level, its patterning must be done prior to the second tier bonding. In other words, the local back-gate can be considered as the last bottom tier metal level. In order to use a dynamic back-bias, the front- and back-gates of the top tier transistor must be connected. A way to short the two gates is to use a 3D shared contact as shown in Figure 5.43. This Figure shows the result of process modeling performed using Coventor SEMulator3D [Cov] considering 28nm design rules. It suggests that such a 3D shared contact is feasible using a process similar to the active/gate contact, given a 20nm-thick BOX, a back-gate jog and specific contact design rules.

In order to evaluate the relevance of dynamic back-bias in 3D-monolithic, we assess the performance by the means of SPICE simulations. The used 2-tier 3D-monolithic Design-Kit with 14nm ground rules includes:

- The Leti-UTSOI compact model [Poi15], perfectly capturing the backside inversion;
- A 20nm-thick BOX for both the top and bottom levels;
- A 3D-dedicated parasitic extraction model (PEX);
- A layout environment with 4 intermediate metal levels.

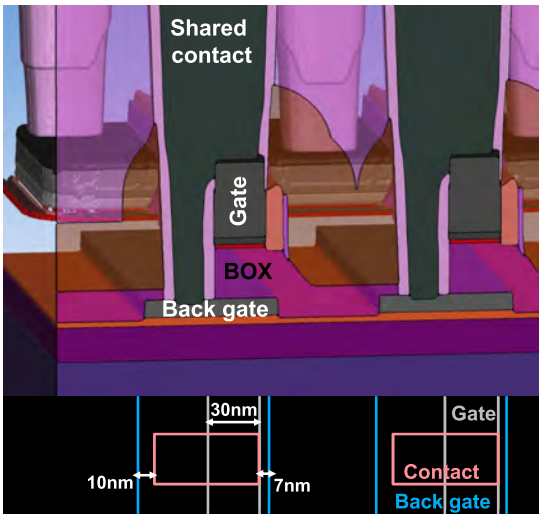


Figure 5.43: Coventor process simulation of the 3D shared contact between the front-gate and the local back-gate. Back-gate extension over the front-gate helps the realization of the shared contact. 28nm design rules are considered.

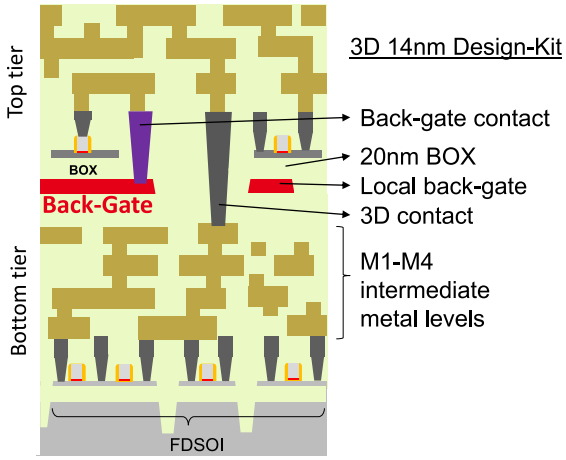


Figure 5.44: Schematic stack of the 3D 14nm Design Kit used for SPICE simulations. It features 4 intermediate metal levels, a 20nm-thick BOX and a 3D-dedicated parasitic extraction model.

It should be noted that the patterning of the back-gate prior to the bonding implies the bonding interface to be located into the top-tier BOX. Even though the bonding of two tiers with such a thin oxide is challenging, it has already been demonstrated on 200mm wafers [Bat11].

5.4.3 Performance/Power

High-Performance or Low-Leakage (HP/LL) 1-finger inverter loaded with fan-out=3 and by a back-end RC network (default values of wire resistance R_w=250Ω and wire capacitance C_w=3.5fF) are simulated in a chain of 71 cells at TT process corner and 25°C.

5.4.3.a The role of back-gate extension

First, the influence of the back-gate extension over the top-gate at the source and drain sides (LBGS/LBGD, respectively) is studied under prelayout assumption, i.e. without parasitic extraction (Figure 5.45).

While there is no significant impact of LBGS/LBGD when the back-gate is statically biased, the double-gate inverter frequency is lower for higher LBGS and particularly for higher LBGD. This evidences the strong detrimental impact of the parasitic backgate-to-drain capacitance on frequency and thus the great advantage provided by 3D-monolithic enabling a local back gate. A frequency improvement of +16% is expected for LBGS=LBGD=5nm, compared to the static reference, i.e. without back-bias.

5.4.3.b Layouts and environment

Regarding the prelayout results of Figure 5.45, the back-gate extension must be the shortest possible. However, an extension is required to allow the 3D shared contact. Different layouts are investigated,

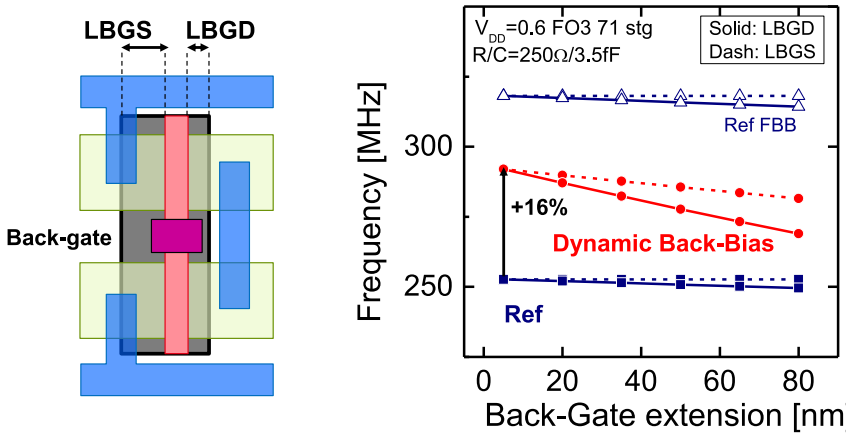


Figure 5.45: (left) Layout of the 1-finger inverter with local back-gate. Definition of the back-gate extensions over front-gate on the source and drain sides, LBGS and LBGD, respectively. (right) Frequency as a function of the back-gate extensions. Under static bias, the back-gate extension does not significantly impact the performance. Under dynamic back-bias however, LBGS and particularly LBGD reductions enhance the frequency.

presented in Figure 5.46:

- ◊ The "Ref" layout features two back planes for pFET and nFET (i.e. FDSOI-like).
- ◊ The "Full" layout features a single back-gate covering all the active.
- ◊ The "Half" layout features a local back-gate located on source side only.
- ◊ The "Quarter" layout features a local back-gate with extension on source side of half the CPP.
- ◊ The "Align" layouts feature a local back-gate of 5nm extension on each side. The back-gate is not necessarily uni-directional, especially in order to increase the overlap between the 3D-shared contact and the back gate.
- ◊ The "Align&Bot.M4" also embeds a metal line of bottom level 4.

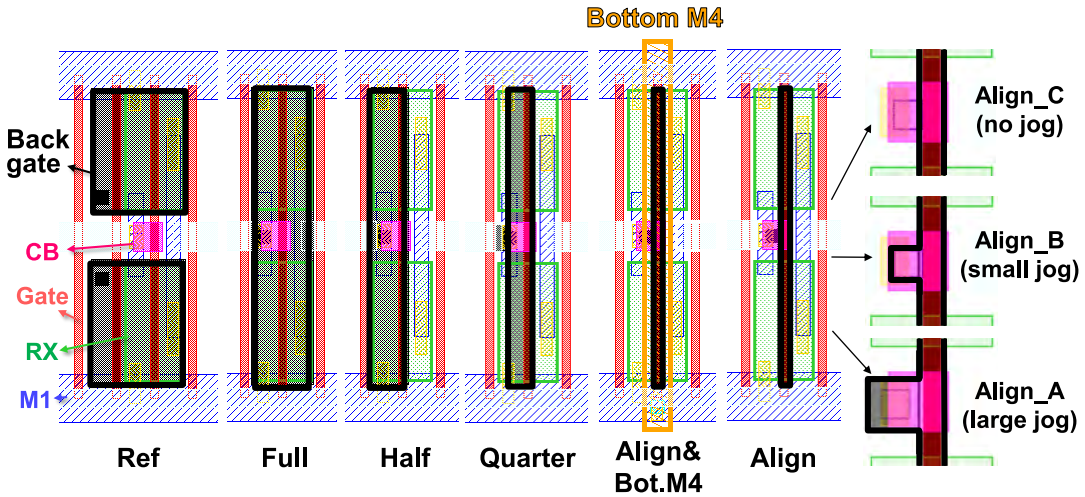


Figure 5.46: Different top level inverter layouts exploiting the double-gate mode *vs.* Ref, whose back-gate is at a given static bias (no back-bias, FBB or RBB). Optimization of the back-gate and shared contact shapes.

Frequency gains with respect to the reference at a supply voltage of V_{DD}=0.6V are given in Figure 5.47. "Align" cases yield +16% frequency improvement, with low impact of the jog dedicated to

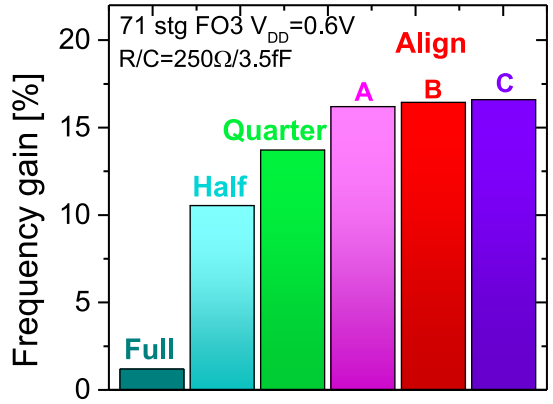


Figure 5.47: Frequency gain of the different inverter layouts *vs.* the Ref. The conditions of reference are V_{DD}=0.6V, fan-out 3, back-end network RC network with R_w=250Ω and wire capacitance C_w=3.5fF. Frequency in double-gate mode can be improved by up to +16% for the optimized "Align" layouts.

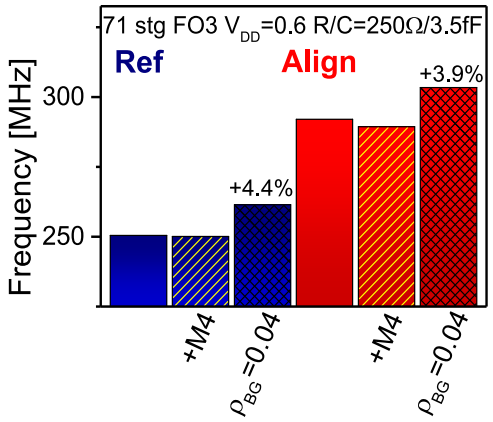


Figure 5.48: Inverters frequency with or without underlined M4 metal line (see the "Align&Bot.M4" layout of Figure 5.46) and for 2 back-gate resistivities $\rho = 0.28\Omega.\mu m$ (doped-Si) or $\rho = 0.04\Omega.\mu m$ (Cu). An underlying M4 metal line does not significantly impact the frequency. A Cu back-gate leads to +4% improvement for both the reference and the "Align" layouts.

the contact overlap, whereas it can significantly reduce the resistance and increase the yield of the contact. Finally, in terms of parasitic capacitances, the presence of a grounded intermediate M4 metal line directly below the dynamically-biased back-gate has negligible impact on the cell performance. This is due to the inter layer dielectric between the M4 line and the back-gate, resulting in a weak electrostatic coupling. As for the back-gate resistivity, it has small impact on frequency, showing only +4% improvement from $\rho = 0.28\Omega.\mu m$ (doped-Si) to $\rho = 0.28\Omega.\mu m$ (Cu).

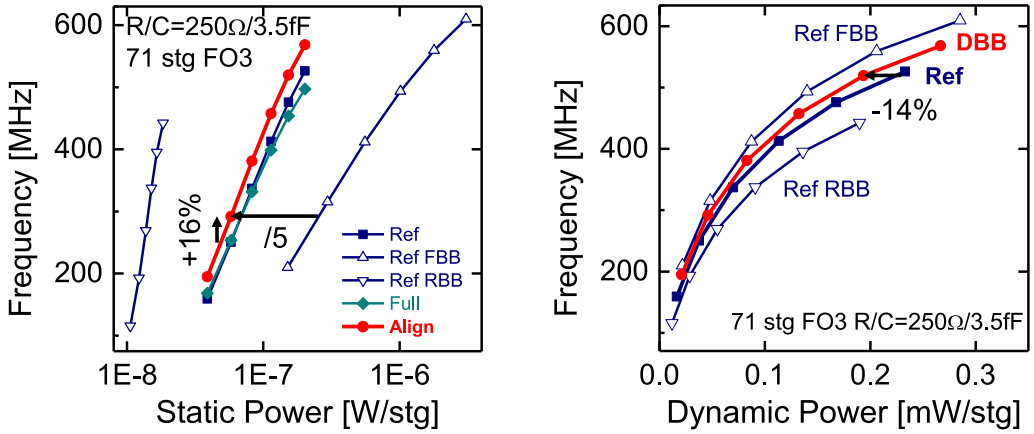


Figure 5.49: Frequency *vs.* (left) static power $P_{STAT}=I_{DDQ}\cdot V_{DD}$ and (right) dynamic power $P_{DYN}=I_{DYN}\cdot V_{DD}$. The local back-gate "Align" configuration has same static power than the reference because of same bias configuration in OFF-state, but frequency is improved by +16%. The Dynamic Back-Bias of the "Align" case leads to 14% dynamic power saving at same frequency compared to the reference. The FBB regime is still the most relevant for dynamic power, but at the expense of a higher static power consumption.

The Frequency/Power trade-offs of the Align_B case are reported in Figure 5.49 and compared to the reference under different static back-bias configurations (RBB, no back-bias, FBB). As expected,

the aforementioned +16% frequency gain is obtained without any leakage degradation (same static power P_{STAT}=I_{DDQ}·V_{DD} because of same I_{OFF}), unlike in the static Forward-Body-Biased Ref. As far as the dynamic power (P_{DYN}) is concerned, double-gate "Align" cells enable reducing the power consumption by 14% at a given frequency with respect to the reference. Nevertheless, the reference under FBB still outperforms the other configurations but at the expense of higher static power consumption.

From Figure 5.49, the top-tier reference still provides higher performance under FBB and lower leakage under RBB than the double-gate cell (i.e dynamically back biased). This makes both types of cells (statically biased and dynamically biased) complementary. Besides, the top-tier cell under static back-bias is more flexible than a classical bottom-tier one because of its capability to be either RBB- and FBB-biased. This is possible thanks to the complete isolation of the back plane by a dielectric (and not a by a diode). This flexibility on bottom-tier is however possible under a dedicated isolation scheme such as a dual-STI [Gre12] or a Dual Isolation by Trenches and Oxidation (DITO), as discussed in section 4.3.2.

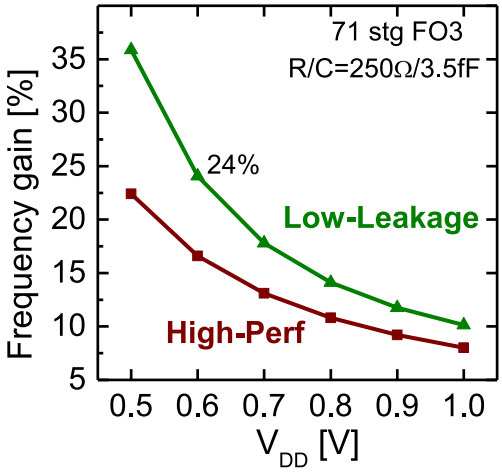


Figure 5.50: Frequency gain with respect to the reference according to the supply voltage V_{DD} for both the "High Performance" (HP) and "Low Leakage" (LL) cells. The better subthreshold swing in double-gate mode improves its efficiency at low gate overdrive V_{DD}-V_T. Reducing V_{DD} or increasing V_T (which is the case for LL cells) thus achieves higher frequency gain in double-gate mode over the single-gate reference.

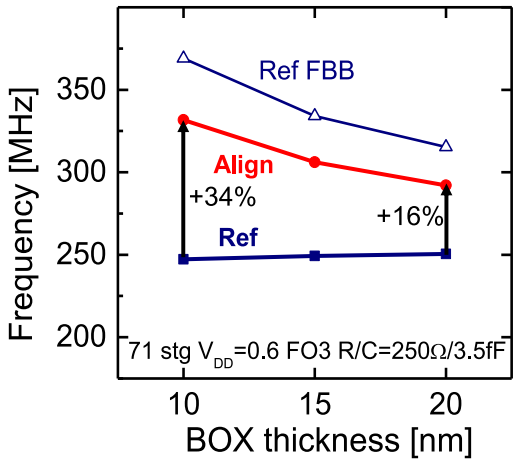


Figure 5.51: Frequency *vs.* top-tier BOX thickness for the "Align" layout (DBB) compared to the reference with or without FBB. The thinner the BOX, the higher the gain from Dynamic-Back-Bias, due to a better electrostatic coupling.

The frequency gain is higher at low V_{DD} and for Low-Leakage devices, i.e. high V_T devices, showing +24% at V_{DD}=0.6V (Figure 5.50). This is because the double-gate mode reduces the subthreshold swing (as observed on transfer characteristics of Figure 5.42), hence its relevance at low gate overdrive V_{DD}-V_T. The 3D-cells thus feature a good compromise between performance and static power, especially at low voltages and for low-leakage cells. In addition, the benefits from dynamic back-bias with a local back-gate are stronger for thinner top-tier BOX, as shown in Figure 5.51. This is due to an enhanced electrostatic coupling resulting in a more efficient double-gate mode.

Figure 5.52 shows the effective resistance R_{EFF}=V_{DD}/2I_{DYN} with respect to the effective capacitance

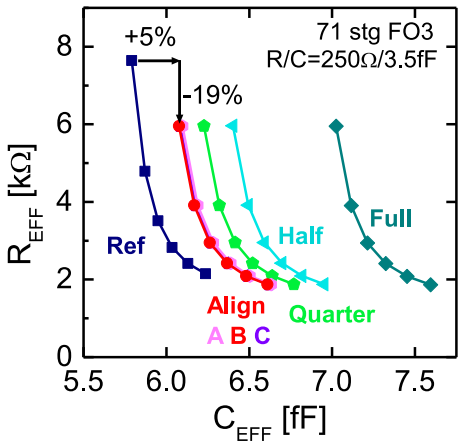


Figure 5.52: Effective resistance $R_{EFF}=V_{DD}/2I_{DYN}$ *vs.* effective capacitance $C_{EFF}=\tau_P/R_{EFF}$ for the studied layout configurations (see Figure 5.46). Cells operating in double-gate mode suffer from a larger capacitance (from both the active back-gate and parasitic source/drain overlap). The R_{EFF} gain for optimized layouts, especially "Align" cases, counterbalances the C_{EFF} degradation

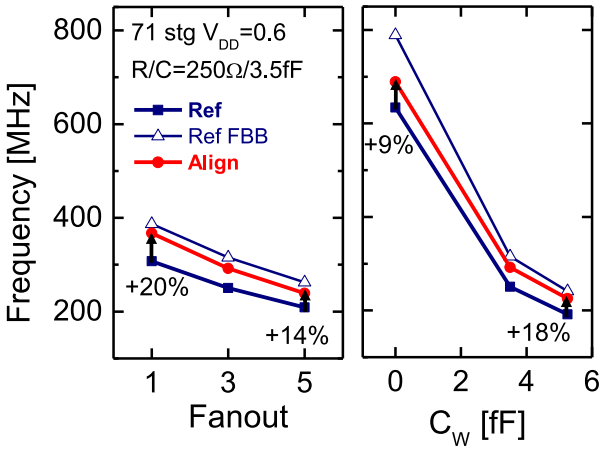


Figure 5.53: Frequency *vs.* (left) Fanout and (right) back-end wire capacitance C_w. The higher the fanout, the lower gain with DBB because of the C_{EFF} degradation. The higher the back-end load, the higher frequency gain, thanks to the improved R_{EFF}.

$C_{EFF}=\tau_P/R_{EFF}$. Double-gate cells have a larger capacitance: from the active back-gate to channel and from the parasitic back-gate to source/drain overlap (especially for the "Full" configuration). For optimized layouts, the R_{EFF} gain counterbalances the C_{EFF} degradation, especially at low V_{DD}. The C_{EFF} increase is mainly detrimental for high fanout (Figure 5.53). This is because the output capacitance consists in standard cell operating in asymmetrical double-gate mode. The R_{EFF} reduction is advantageous for high back-end load. This is because the C_{EFF} increase is alleviated by the presence of a high back-end capacitance. These observations can be well understood from the expression of the delay τ_P:

$$\tau_P \approx R_{EFF}\,(C_{EFF}+C_W) \tag{5.2}$$

5.4.4 6T-SRAM with local back-gate

Beyond logic standard cells, the concept of a local back-gate is also investigated on 6T-SRAM cells.

5.4.4.a Double-gate modes

Either the Pass-Gate (PG) or all the 6T-SRAM transistors (Pass-Gate PG, Pull-Up PU and Pull-Down PD) can operate under the double-gate mode. The schematic of the three studied configurations are represented in Figure 5.54. It should be noted than in the reference configuration the static back-bias applied on the pFET PU is $V_{dds}=G_{ND}$, meaning that it operates in Forward Back-Bias FBB regime.

In a 6T-SRAM, the reading and writing operation metrics depend on the strength balance between

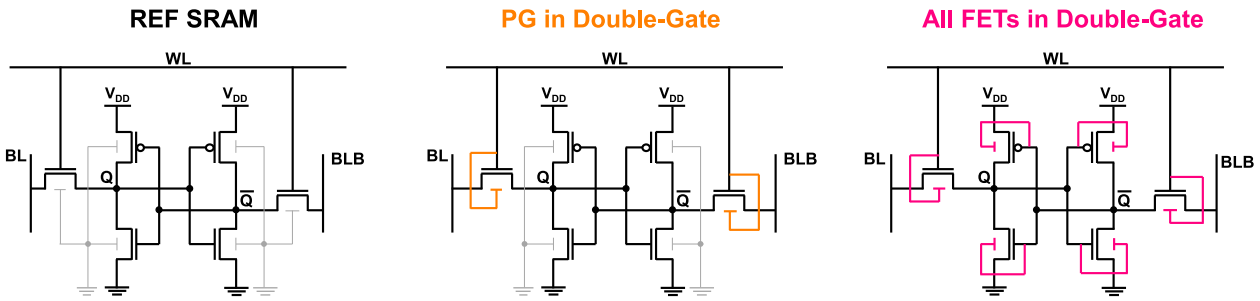


Figure 5.54: Schematics of the three 6T-SRAM configurations investigated. In the reference, back-bias for all FETs is grounded. Two cases of double-gate mode are assessed: only the Pass-Gate or all FETs in double-gate mode.

the FET types. The read stability is linked to the PD *vs.* PG ratio while the writing operation is governed by the PG *vs.* PU ratio. A FET in double-gate mode with a local back-gate connected to the front gate is strengthened. This changes the ratios inherent to the SRAM cell.

The SPICE simulation results operated at V_{DD}=0.8V are given in Figure 5.55.

6T-SRAM V_{DD}=0.8V	Ref	PG in DG	All FETs in DG
SNM [mV]	151	122	124
WNM [mV]	345	353	328
I_{write} [µA]	30	39	39
I_{read} [µA]	17.2	20.4	22.0
I_{leak} [pA]	17	17	15

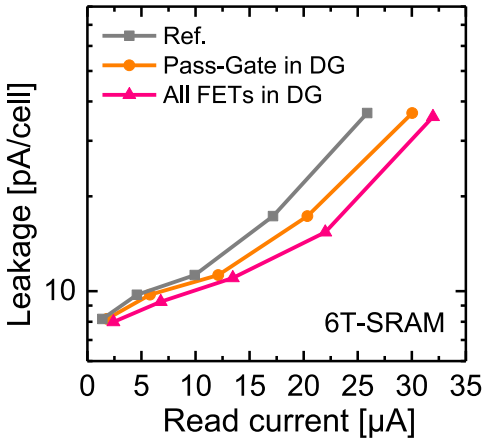


Figure 5.55: SRAM (left) table of metrics and (right) leakage *vs.* read current according to their double-gate configuration. The read and write currents are enhanced when the Pass-Gate is in double-gate mode, at the expense of a reduced SNM. All FETs in double-gate mode leads to +30% read and write currents without degrading the leakage.

When only the PG is double-gated, the Static Noise Margin (SNM) reduces from 151mV to 122mV. This is due to a weaker PD *vs.* PG ratio, leading to a weaker control of the internal storage node voltage by the PD. The write current is however highly enhanced (+30%) from the PG *vs.* PU increased ratio. The read current is also improved by +19%. This is because the read current results from the PG and PD in series.

When all transistors are connected in a double-gate mode, the write and read currents are both improved by +30%. No significant impact on leakage current are observed. The slight change in the configuration with all FETs in double-gate mode is due to the fact that the PU is in FBB in the reference, while in double-gate OFF-state it is equivalent to zero back-bias.

5.4.4.b Write-assist technique

Up to now, the local back-gate has been exclusively used in a double-gate mode, i.e. dynamic back-bias for both logic standard and SRAM cells. The local back-gate enabled by 3D-monolithic adds new opportunities. In this section, the local back-gate is used to tune the characteristics of the SRAM FETs on demand. Especially, we investigate here a write-assist technique enabled by the local back-gate. In this scheme, the local back-gate is not connected to the front-gate. Figure 5.56 shows two configurations in which either the PG or the PG+PU back-gates are connected to a second word line for write-assist.

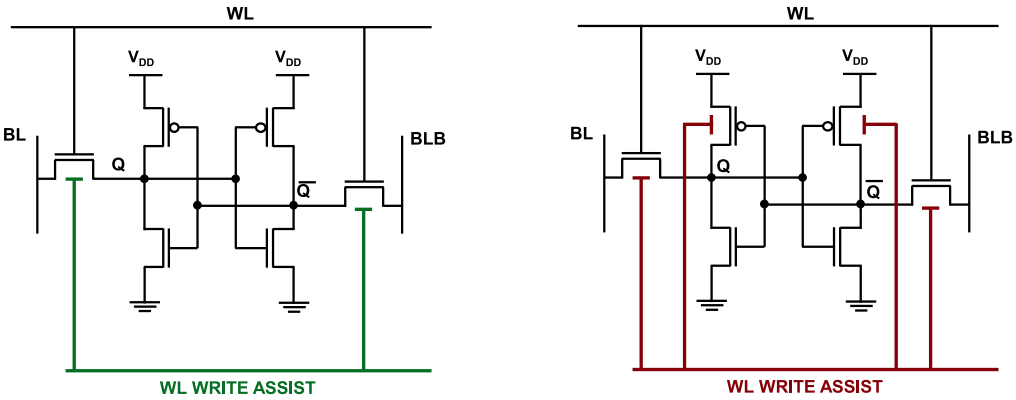


Figure 5.56: SRAM schematics with local back-gate connected to a second word line, dedicated to write-assist. Two configurations are presented. Either only the PG is connected to the write-assist word line or both the PG and the PU are connected.

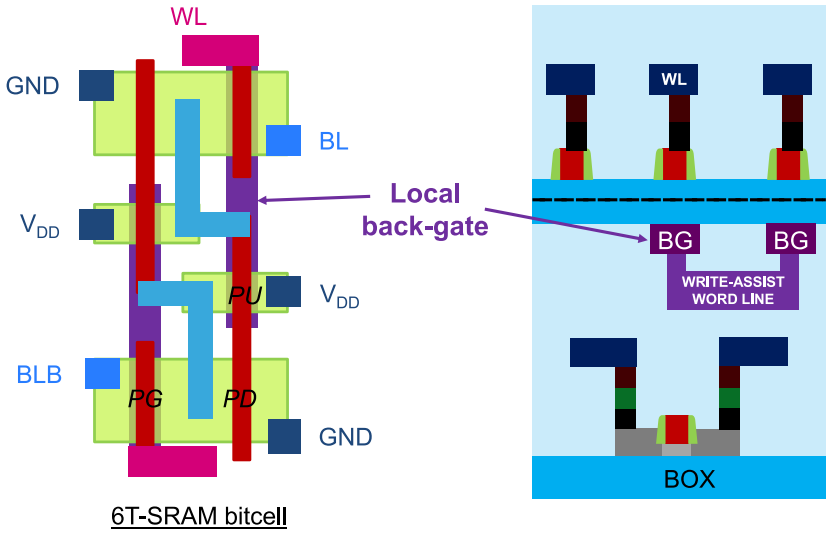


Figure 5.57: (left) Typical layout of an SRAM bitcell with the local back-gate layer in purple and (right) illustration of the 3D stack where the word line for write assist is embedded in an interlayer connection.

Figure 5.57 shows a typical layout of an SRAM bitcell with the local back-gate. It should be emphasized that the local back-gate in this case is not connected to the front gate. The local back-gate is rather connected to an independent second word line, used for write-assist. This second word line can be embedded in the interlayer connections between the two tiers of the 3D-monolithic stack. In the presented layout, the local back-gate covers both the PG and the PU of the opposite

inverter of the two cross-coupled inverters.

In order to improve the writability of the SRAM bitcell, a positive bias is applied on the second word line during a write operation only. In stand-by or during a read operation, no bias is applied. Doing so, the nFET Pass-Gate is in FBB regime for the write operation. This enhances the PG *vs.* PU ratio, decisive for a write operation. By applying 1V on the write-assist word line, +34% of write current achieving with respect to the reference case (Figure 5.58).

6T-SRAM V_{DD}=0.8V	REF	w/ WA 1V	w/ WA 1V +PU	
SNM [mV]	151	151	151	
WNM [mV]	349	353	364	
IW [µA]	**30.3**	**40.8**	**40.7**	**+34%**
I_{read} [µA]	17.2	17.2	17.2	
I_{leak} [pA]	17.3	17.3	17.3	

Figure 5.58: Impact of the local back-gate write assist on SRAM metrics. The 1V back-bias is applied for write operation only, leading to +34% write current improvement. This gain is due to the stronger PG *vs.* PU ratio obtained when Forward Back-Biasing the PG.

The gain is similar when the PU is also connected. It should be higher since the PU is in FBB in the reference case (because it is grounded, see Figure 5.54) while in this scheme, the applied back-bias of 1V results in RBB regime. Nevertheless, the PG *vs.* PU ratio is sufficiently strong when the PG is in FBB that the write current is only limited by the Pass-Gate performance. In this configuration, it would be possible to tune the PU characteristics to achieve a higher read stability and takes advantage of the write assist technique for maintaining a high write ability.

5.4.5 Conclusion

In this section, the great advantage of the efficient back-biasing in FDSOI technology is extended in a 3D-monolithic integration scheme.

First, the electrostatic coupling in a 3D-monolithic top-tier has been experimentally demonstrated. The 3D-monolithic integration enables to design a local back-gate. Then, by connecting this local back-gate to the front one with a shared contact, standard cells can operate in asymmetrical double-gate mode. This dynamic back-bias configuration has been extensively studied with SPICE simulations using a dedicated 14nm 3D Design-Kit featuring a 20nm top-tier BOX. Dynamic back-bias is expected to enhance the inverter frequency by +16% for an optimized layout in our conditions of reference (HP IV-SX1, V_{DD}=0.6, FO=3, R_w/C_w=250Ω/3.5fF). The dynamic back-bias cells feature a good compromise between performance and static power, especially at low voltages and for low-leakage cells.

Finally, the interest of a local back-gate enabled by 3D-monolithic has been assessed on SRAM bitcell performance. The asymmetrical double-gate mode can improve both the write and read currents by +30% when all transistors are double-gated. In addition, the use of the local back-gate for write-assist has been evaluated, achieving up to +34% with 1V back-bias applied on the PG during a write operation.

General conclusion

The switch behavior of the MOSFET makes it the key device of integrated circuits, enabling logic operations to be performed. The CMOS technology, which includes the chip design and manufacturing, has experienced a dramatic evolution over the past decade. Physical barriers have been pushed back in order to keep reducing the cost and improve the performance and/or functionality. In particular, new transistor architectures like finFET or FDSOI have been introduced to maintain a good electrostatic control in the MOSFET channel region. In addition, there is a need for intrinsic performance improvement. Strain engineering has been demonstrated to be highly efficient for boosting the carrier mobility. In this work, we have studied **the strain integration in FDSOI technology for sub-20nm nodes.**

As strain breaks the crystal symmetry, it alters the band structure of the material and therefore the carrier mobility. A relevant strain configuration results in mobility enhancement and thus in MOSFET performance improvement at the same leakage. Especially, tensile strain is highly beneficial for electron while compressive stress boosts hole transport. **In the chapter 2, we have shown that the strain not only impacts the carrier mobility but also the access resistance**. This has been evidenced on a large set of strained devices by the means of a novel access resistance extraction methodology. This method provides a relevant partitioning between the mobility and the access resistance components. In particular, the near-spacer region is well accounted for. It is proved to be subjected to the level of stress in the device. This finding reinforces the interest of strain integration for increasing the performance of advanced CMOS devices. Besides, it is relevant to take this behavior into account in compact models for predictive benchmarking and optimized integrated circuit designs.

In the chapter 3, we have investigated the strain-induced local layout effects related to the introduction of SiGe in FDSOI technology. The compressively strained SiGeOI is fabricated by the Ge-enrichment technique, which takes advantage of the preferential oxidation of Silicon over Germanium, in the pFET areas only. The free boundary condition introduced after active area patterning results in a lateral stress relaxation, observed by NBD (and DFEH) measurements. We have proposed a method for investigating the lateral relaxation using µRaman spectroscopy. It has been found that the SiGeOI relaxes on a longer length than predicted from elastic mechanical simulations. This has been attributed to the behavior of the interface between strained SiGe crystal and oxide. Because of the lateral stress relaxation, the electrical parameters of SiGe channel pFETs strongly depend on the transistor layout. Especially, the threshold voltage and the mobility vary

with the active area dimension. For <110>-oriented channel, **the relaxation of the longitudinal stress**, i.e. parallel to the current flow, **is highly detrimental for the pFET performance**. As a result, pFETs built on short active area (typically below 300nm-long) feature a high threshold voltage and a low mobility with respect to the ones built on a long active. We have proposed an empirical analytic model of stress relaxation that allows the local layout effects to be accurately reproduced.

Different solutions have been proposed to optimize the performance of short active SiGe channel pFETs in the chapter 4. First, a cheap and easy-to-implement design solution consists in an **intra-cell V_T-mixing**. This approach, so-called Mix-VT, consists in using a regular threshold voltage nFET along with a low threshold voltage pFET. This way, the threshold voltage increase due to strain relaxation is compensated for, resulting in a balanced cell. From simulation, the 1-finger inverter delay is expected to be reduced by -23% at the same leakage and for the nominal supply voltage. However, the Mix-VT approach does not solve the issue of mobility degradation. The **Continuous-RX approach** has also been evaluated. This Design/Technology Co-Optimization relies on the design on a long stripe of active area. It requires isolation-gates to prevent leakage between two abutted standard cells. Such an approach provides the best stress configuration, i.e. longitudinal compressive stress, and therefore a high performance improvement (-28% delay reduction experimentally demonstrated for the 1-finger inverter). Nevertheless, the presence of RX-jog, i.e. non rectangular active areas, rises an issue of standard-cell-abutment-induced variability. As far as technological solutions are concerned, an alternative integration scheme for SiGe introduction has been assessed. This so-called "SiGe-last" integration scheme consists in fabricating the SiGe layer after the active patterning by epitaxy only, i.e. no Ge-enrichment. The stress relaxation typical length has been evidenced to be significantly reduced with such an integration scheme. As a result, the performance of short active layout is enhanced due to the higher longitudinal stress. However, the transverse stress is also better maintained. Yet, this stress component is detrimental for hole mobility. The SiGe-last process flow is therefore only relevant for short active layouts highly impacted by the longitudinal stress relaxation. Finally, a **novel dual isolation scheme** has been proposed to achieve the best stress configuration. It consists in using conventional STI in the transverse direction and a local oxidation in the longitudinal one. This way, the SiGe layer is not etched in the longitudinal direction. From physical strain measurement (by PED), a better maintain of strain has been evidenced. In addition, both transistor and ring-oscillator performance enhancement have been demonstrated. Such a dual isolation scheme is also highly relevant to **take full advantage of the FDSOI back-bias capability**. Both Reverse and Forward Back-Bias are possible on the same device, which is not the case in a single-STI scheme because of the back-plane Pwell/Nwell junction.

In the chapter 5, a focus has been made on the tensile strain generation for boosting the nFET performance. The use of sSOI is obviously highly efficient to boost the nFET performance. Like SiGe channel, such an intrinsically strained channel is subjected to patterning-induced layout effects. Such local layout effects are well reproduced by our empirical model. The main challenge of sSOI is the pFET performance degradation. That is why techniques to locally introduce tensile strain have also been assessed. **The BOX-creep technique** aims at generating tensile strain from the

relaxation of a stressed SiN layer helped by the buried oxide creeping. Mechanical simulations allowed us to investigate the best configurations to maximize the tensile strain generation. In particular, the parasitic creeping of the pad oxide must be considered, especially for short active layouts. We have integrated the BOX-creep module into a FDSOI route and experimentally assessed the electrical characteristics of the devices. No performance improvement has been evidenced. This has been attributed to the loss of the SiN compressive stress under an anneal at high temperature. Taking advantage of thermal expansion coefficient mismatch by using another material than SiN (such as TiN for instance) could be efficient. We have also studied **a technique based on the solid phase epitaxial regrowth from top relaxed SiGe** to locally introduce tensile strain. High resolution TEM pictures have shown a successful recrystallization with stacking faults in the source/drain region and a crystal of high quality in the channel. From our electrical characterizations and fine extraction of mobility, a gain of +15% electron mobility has been observed. The feasibility of this technique has been demonstrated but further process optimization is required. Nevertheless, this technique is not expected to be highly efficient for short CPP. The STRASS technique would provide a higher stress but a good control of the channel crystal quality is necessary, especially for achieving high yield.

Finally, **the high back-bias efficiency of FDSOI has been evaluated in a 3D integration scheme**. Especially, the sequential 3D allows the design of a local back-gate. The concept has been electrically demonstrated, highlighting a capacitive coupling between bottom and top levels. We have performed simulations of standard cells operating in an asymmetrical double-gate regime. Such a dynamic back-bias is expected to provide +16% frequency improvement at the same leakage in our conditions of reference. In addition, the use of local back-gate has been investigated in SRAM bitcells in double-gate mode or for assist techniques.

In a nutshell, the strain integration is a powerful knob to boost the performance even though it comes with local layout effects, mostly induced by the active area patterning. We have seen that different design and/or technological solutions can be used to enhance the performance. For sub-10nm technologies, there is a need for tensile strain generation. It is however a great challenge in a context of co-integration. In order to keep scaling down the technology, the introduction of stacked nanowires (or nanosheets) is promising for sub-5nm. Such devices provide an excellent electrostatic control but it is very challenging to integrate strain in their multiple channels. Eventually, the replacement of Silicon by a high mobility material (III-V) will become necessary to keep increasing the performance as the dimensions are scaled down. However, devices using such materials have not demonstrated a suitable level of maturity from an industrial point of view. In addition to the Power/Performance/Area/Cost metrics, the time to market will also be a key element for the future of CMOS technology. In any case, the FDSOI technology is highly promising for applications demanding low power and low leakage (e.g. mobile, IoT, wearable applications); this mainly due to its great back-bias capability.

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APPENDIX A

Hu's model of patterning-induced strain relaxation

Hu's model is based on Flamant's problem and solution [Fla92], presented in Figure A.1. The stress components generated by point forces F_1 and F_2 on a solid whose geometry is defined by angles α and β is expressed as:

$$\begin{cases} \sigma_{rr} = \dfrac{2C_1 \cos\theta}{r} + \dfrac{2C_3 \cos\theta}{r} \\ \sigma_{\theta\theta} = 0 \\ \sigma_{r\theta} = 0 \end{cases} \tag{A.1}$$

in which C_1 and C_3 constants are related to the point forces F_1 and F_2 according to Flamant's solution by:

$$F_1 + 2\int_{\alpha}^{\beta} (C_1 \cos\theta + C_3 \sin\theta)\cos\theta d\theta = 0 \tag{A.2}$$

$$F_2 + 2\int_{\alpha}^{\beta} (C_1 \cos\theta + C_3 \sin\theta)\sin\theta d\theta = 0 \tag{A.3}$$

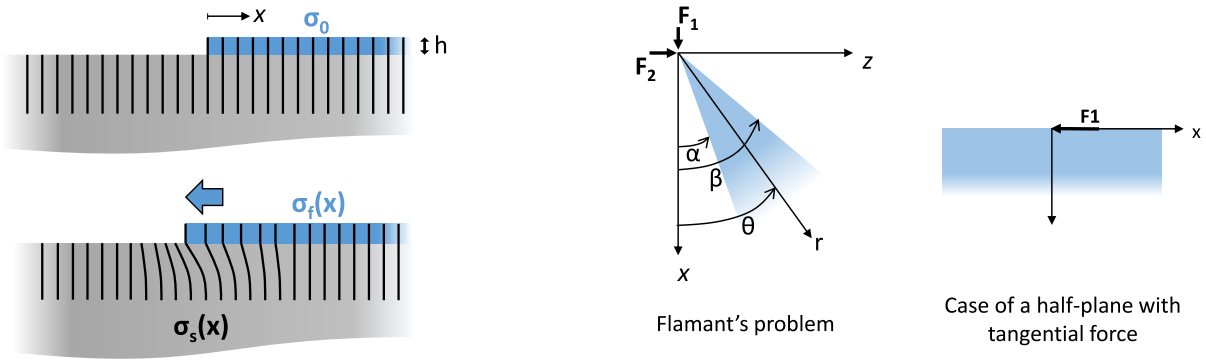

Figure A.1: (left) Illustration of Hu's model structure, consisting of a stressed film mesa etched [Hu79] [Hu91]. (right) Flamant's problem definition [Fla92] and particular case used for Hu's model derivation.

Hu's problem consists in a solid half-plane, i.e. the substrate. This means that $alpha = 0$ and $\beta = \pi$. The force generated by the stressed thin film is considered as a tangential force. This translates into $F_1 = F$ and $F_2 = 0$. Solving equations A.2 and A.3 gives $C_1 = -\frac{F}{\pi}$ and $C_3 = 0$. Finally, the stress

along the x direction generated by a tangential force F at $x = 0$ is given by:

$$\sigma_{xx} = \sigma_{rr} \cos^2 \theta = -\frac{2F}{\pi} \frac{x^3}{(x^2 + z^2)^2} \tag{A.4}$$

The introduction of a free boundary condition is responsible for a point force at $x = 0$ coming from the difference of stress. This will cause the film to relax and thus creating a non-uniform stress field in the film. The applied force on the top of the substrate ($z = 0$) at a point $x = u$ is given by:

$$\sigma_s(u) = -\frac{2F(u)}{\pi} \frac{1}{x - u} \tag{A.5}$$

where the force is directly related to the stress differential in the film at this point $x = u$:

$$F(u) = h \frac{d\sigma_f(u)}{du} \tag{A.6}$$

which gives:

$$\sigma_s(u) = -\frac{2h}{\pi} \frac{d\sigma_f(u)}{du} \frac{1}{x - u} \tag{A.7}$$

The stress in the substrate in not self-consistent as it depends on the stress in the film. In order to derive the stress field in the substrate σ_s as a function of the distance from the film free edge x, one has to integrate along the whole film:

$$\sigma_s(x) = \int_0^\infty \sigma_{xx}(u) du = -\frac{2h}{\pi} \int_0^\infty \frac{d\sigma_f(u)}{du} \frac{1}{x - u} du \tag{A.8}$$

The interface film/substrate interface is assumed to be totally adherent. This means that lattice continuity is considered between the substrate and the film:

$$\varepsilon_f(x) - \varepsilon_0 = \varepsilon_{sub} \Leftrightarrow \sigma_{sub}(x) = K \left(\sigma_f(x) - \sigma_0\right) \tag{A.9}$$

where K is the relative rigidity factor, given by:

$$K = \frac{E_{sub} \left(1 - {\nu_f}^2\right)}{E_f \left(1 - {\nu_{sub}}^2\right)} \tag{A.10}$$

APPENDIX B

SRAM static testbench

6T-SRAM bitcell

The six-transistor Static Random Access Memory (6T-SRAM) bitcell is a volatile memory made of transistors. The schematic of the bitcell is given in Figure B.1. The bit is stored by the means of two cross-coupled inverters, made of Pull-Up pFET and Pull-Down (PD) nFET transistors. The bit state can be either '0' (i.e. G_{ND}) or '1' (i.e. V_{DD}). The memory point is accessed by two Pass-Gate (PG) nFET transistors, both connected to the Word Line (WL) and to either the Bit Line (BL) or the second Bit Line (BLB). The different operations of an SRAM cell are the storage, the reading and writing operations.

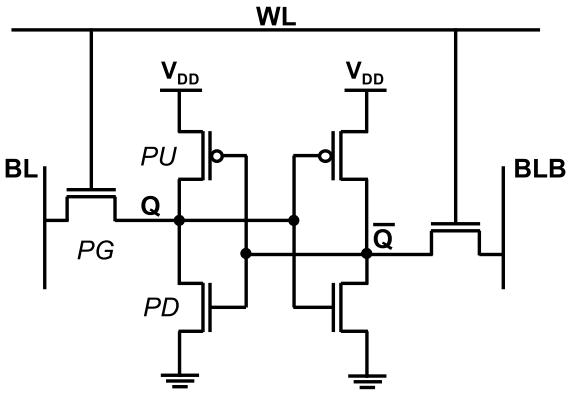

Figure B.1: SRAM bitcell schematic. The SRAM bitcell consists in two cross-coupled inverters, made of Pull-Up (PU) pFET and Pull-Down (PD) nFET transistors. The memory point is accessed by two Pass-Gate (PG) nFET transistors, both connected to the Word Line (WL) and to either the Bit Line (BL) or the second Bit Line (BLB).

SRAM operations

During the storage of the information, the Pass-Gate transistors are biased in OFF state, i.e. the WL=0. The bit is maintained by the two cross-coupled inverters in a stable state.

For a reading operation, the Pass-Gate transistors are activated by applying V_{DD} on the Word Line, i.e. WL=1. In addition, both Bit Lines are precharged to V_{DD} (Figure B.2). On the side of the bitcell where a '1' is stored, no current flows through the Pass-Gate (potentials of the source and drain are equal to '1'). On the other side where a '0' is stored, a reading current flows through both the PG and the PD, which are in series. In order not to alter the stored bit, the '0' must be maintained. This is achieved by designing a PD stronger than the PG, usually thanks to their width ratio. **The reading operation thus imposes PD>PG**. The bit is read from sensing the bit line voltage variation.

For a writing operation, the Bit Lines BL and BLB are biased according to the bit to be written. Figure B.3 shows the case where BL=1 and BLB=0. This is exactly the same for the other configuration since the SRAM bitcell is symmetric. On the left side, the '0' stored can not be changed to a '1' because of the reading criterion PD>PG, previously described. The writing operation thus relies on the right side where the '1' is changed to a '0'. This requires a PG stronger than the PU. **The writing operation thus imposes PG>PU.**

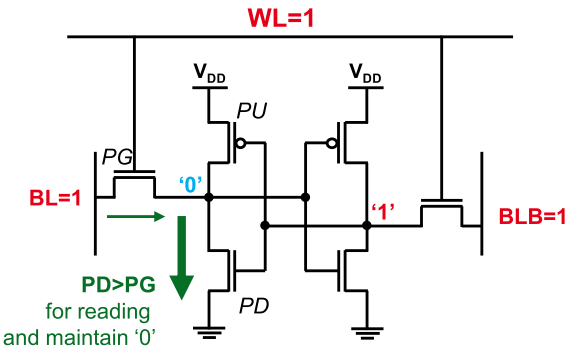

Figure B.2: SRAM reading operation. Both bit lines are precharged to '1'. The reading criterion PD>PG allows the internal node at '0' to be maintained.

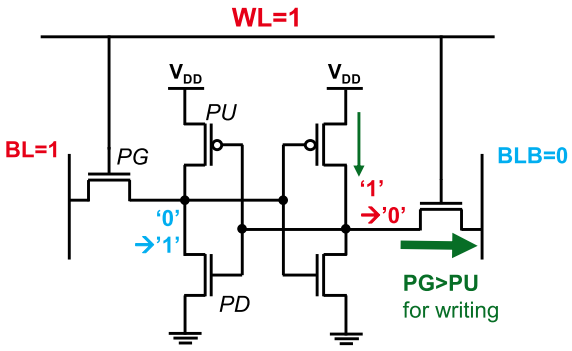

Figure B.3: SRAM writing operation. The bit flip is not possible where the internal node is at '0' (on the left side in this example) because of the read criterion PD>PG, discussed in Figure B.2. The writing operation imposes the PG>PU criterion, allowing the '1' to be flipped to '0'.

It should be emphasized that the SRAM bitcell access transistors (i.e. the Pass-Gates) are made of nFETs because of the higher electron mobility than hole one. This leads to a high current from PD and PG during a reading operation and helps the PG>PU criterion for writing. The use of pFET as Pass-Gate is discussed in section 4.2.4.

Extraction of SRAM static metrics

Different static metrics have been used in this work to characterized the SRAM bitcells [Guo09]. The metrics are extracted after SPICE simulations of the bitcell.

Read Static Noise Margin (SNM)

During a read operation, the voltage of the internal node where the bit is stored depends on the PD>PG ratio (the PG and the PD in series consist of a voltage divider). If the internal node voltage exceeds the trip point of the right-side inverter, the stored bit will flip. The most common metric used for read stability is the read Static Noise Margin (SNM, or RSNM). It represents the voltage margin before causing a bit flip during a read operation and is extracted from the voltage transfer characteristics. It is measured by sweeping the storage node VL (VR) and measuring the opposite storage node VR (VL) when WL=BL=BLB=1 (Figure B.4). The SNM is given by the side of the smallest square embedded between the two voltage transfer characteristics, i.e. the so-called butterfly curve (Figure B.4). The larger the SNM, the more stable the bitcell is during a read operation.

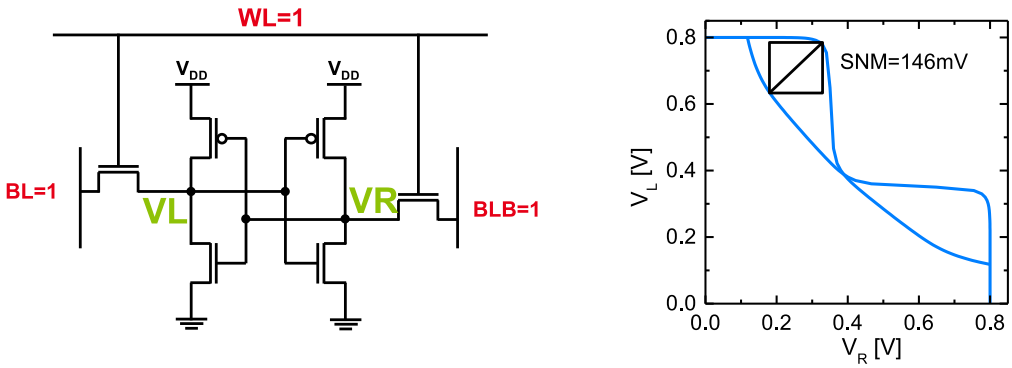

Figure B.4: (left) SRAM SNM extraction, consisting of two voltage transfer characteristics VR(VL) *vs.* VL(VR) while WL=BL=BLB=1. The SNM is given by the side of the smallest square embedded between the two curves in the so-called butterfly curve (right).

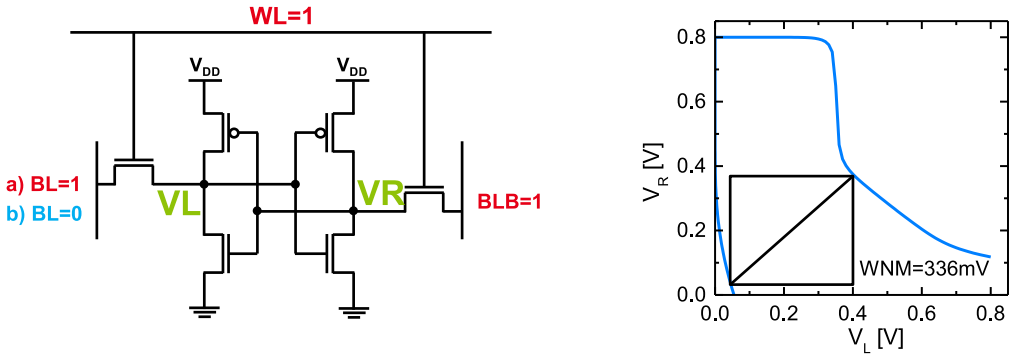

Figure B.5: (left) SRAM WNM extraction, consisting of two voltage transfer characteristics VR(VL) *vs.* VL(VR) while WL=BLB=1 and BLB=1(=0). The WNM is given by the side of the smallest square embedded between the two curves (right).

Write Noise Margin (WNM)

The Write Noise Margin (WNM) metric is similar to the SNM but for a write operation. It also consist in measuring two voltage transfer characteristics. In the first one, similar to the SNM, the storage node voltage VL is swept and VR is measured while WL=BL=BLB=1. The second one consists in sweeping VR and measuring VL while WL=BLB=1 but this time BL=0 (Figure B.5). The WNM is given by the side of the smallest square embedded between the two voltage transfer characteristics as shown in Figure B.5). The lower the WNM, the more likely the bit will flip, causing a writing operation failure.

Write current (I_W) from N-curve

A second metric to characterize the write-ability of the SRAM uses the so called "N-curve". It consists in sweeping the internal node voltage VR and measuring the current externally sourced while WL=BL=1 and BLB=0 (Figure B.6). This measures the current through the PG minus the one through the PU. The write current I_W is defined as the minimum current past the trip point of the inverter. The higher the write current, the higher the write ability of the cell.

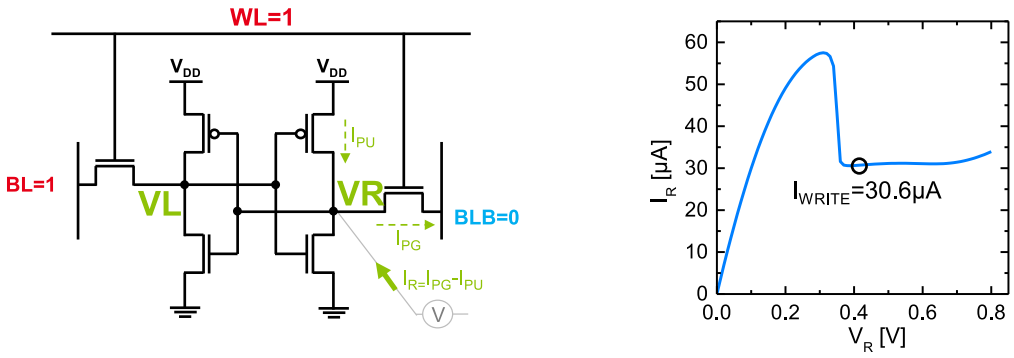

Figure B.6: (left) SRAM write current extraction, from sweeping the internal node voltage VR and measuring the current externally sourced while WL=BL=1 and BLB=0. The write current I_W is defined as the minimum current past the trip point of the inverter (right).

Read current (I_{READ})

SRAM cell performance can be characterized by its read current I_{READ}, also called I_{cell}. It is measured under reading operation condition, i.e WL=BL=BLB=1 (Figure B.7). Even though the current will decrease as the bit line will discharge, the initial current is a fair approximation.

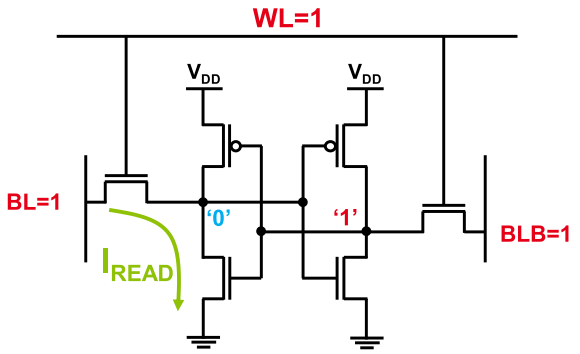

Figure B.7: SRAM read current extraction. The read current is defined as the current flowing from the Bit Line though the Pass-Gate and Pull-Down series transistors. Even though the current will decrease as the bit line will discharge, the initial current is a fair approximation.

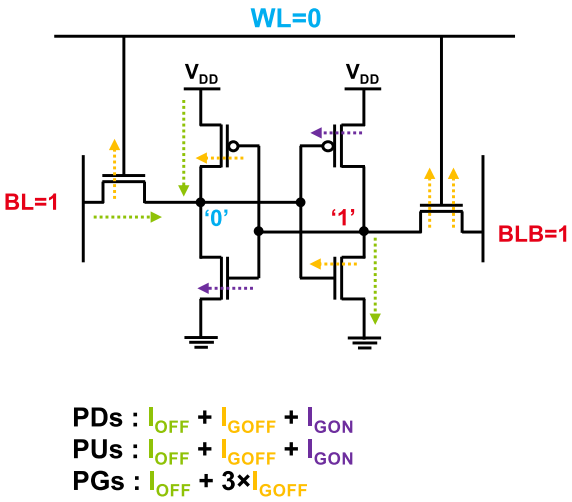

Figure B.8: SRAM leakage current extraction, measured when WL=0 and BL=BLB=1. The stand-by leakage can be approximated from the leakage of each transistor of the bitcell.

Leakage

Finally, one of the most important metric for SRAM is the leakage of the cell $I_{leakage}$ (or I_{sb} for stand-by current). It is defined by the current measured under the conditions WL=0 and BL=BLB=1, as shown in Figure B.8. The bitcell leakage current can be derived according to the leakage of the different transistors. The gate leakage plays a significant role.

Summary

The different static metrics extracted through our testbench are summarized in Table B.1.

Table B.1: SRAM metric extraction

Metrics	Extraction
SNM	2 sweeps VR *vs.* VL with WL=BL=BLB=1
WNM	2 sweeps VR *vs.* VL with WL=BLB=1 and BL=0,1
I_W	1 sweep IR *vs.* VR with WL=BL=1 and BLB=0
I_{READ}	Current measurement with WL=BL=BLB=1
$I_{leakage}$	Current measurement with WL=0 and BL=BLB=1

APPENDIX C

Résumé en français

C.1 Introduction: l'ingénierie de la contrainte en technologie CMOS

L'industrie de la micro-électronique a connu un incroyable essor depuis l'invention des premiers circuits intégrés à base de transistors à effet de champ (MOSFET). La drastique réduction des coûts associée à la miniaturisation des dispositifs a été le fer de lance de cette évolution, comme l'avait prédit Moore avec sa célèbre loi. Jusqu'au nœud 90nm, la réduction des dimensions a entrainé des gains en performances de façon systématique. Il a été ensuite nécessaire d'introduire de nouveaux éléments et d'utiliser de nouvelles architectures afin de répondre aux divers défis technologiques tels que la fuite de grille ou le contrôle électrostatique.

La technologie FDSOI (Fully Depleted Silicon On Insulator) apparait comme une solution alternative au FinFET, en particulier pour les applications à faible consommations comme les objets connectés. Un des points fort de la technologie FDSOI réside dans son efficace polarisation arrière. Afin de continuer la miniaturisation, des éléments permettant d'améliorer la performance des dispositifs sont requis. Ceci est d'autant plus vrai que les effets parasites deviennent significatifs. C'est pourquoi un fort intérêt est porté sur l'ingénierie de la contrainte. En effet, l'intégration de contrainte mécanique dans les transistors permet d'améliorer la mobilité des porteurs à travers une modification des propriétés du matériau. Il s'avère que les transistors de type n et p requièrent des contraintes de signes opposés: tension pour les électrons et compression pour les trous. De plus, des niveaux de contrainte élevés (supérieurs à 1GPa) sont recherchés afin d'impacter significativement les caractéristiques électriques des dispositifs.

C'est dans ce contexte que ce travail de thèse vise à étudier l'intégration de contrainte mécanique pour optimiser les performances des technologies FDSOI des nœuds 20nm et en deçà. Dans un premier temps, nous nous focalisons sur la performance des dispositifs contraints et en particulier sur le rôle de la résistance d'accès. Ensuite, nous nous intéressons particulièrement à l'utilisation de canal SiGe pour les transistors de type p en technologie 14nm. Nous caractérisons et modélisons les effets de géométrie induits par la relaxation latérale de la contrainte compressive du SiGeOI. Nous proposons des solutions de type "design" et technologiques afin d'optimiser la performance des cellules. Finalement, nous nous concentrons sur des techniques innovantes d'intégration de contrainte en tension, visant à améliorer la mobilité des électrons.

C.2 Résistance d'accès des transistors contraints

Dans le premier chapitre, nous nous intéressons à la performance des transistors contraints. En particulier, nous proposons une méthodologie d'extraction de résistance d'accès et montrons que celle-ci dépend du niveau de contrainte.

C.2.1 Nouvelle méthodologie d'extraction des résistances d'accès

Il existe plusieurs méthodologies pour extraire la mobilité des porteurs dans les canaux courts ainsi que la résistance d'accès. Parmi elles, les plus utilisées sont la méthode "Rtot(L)" et la méthodologie de la Fonction-Y. La méthode Rtot(L) a l'inconvénient de supposer une mobilité constante quelque soit la longueur de grille du transistor. La Fonction-Y quant à elle nécessite des modèles de dépendance de la mobilité et de résistance d'accès vis-à-vis de la charge d'inversion. Nous proposons une méthodologie basée sur la Fonction-Y, en adaptant le modèle de dépendance de résistance d'accès avec la charge d'inversion.

Le modèle de courant dans le canal d'un transistor en régime linéaire est donné par:

$$I_{DCH} = \frac{\beta Q_{INV} V_D}{1 + \theta_{1,0} Q_{INV} + \theta_{2,0} {Q_{INV}}^2} \tag{C.1}$$

avec $\beta = \frac{W}{L}\mu_0$, μ_0 étant la mobilité à faible champ transverse, Q_{INV} la charge d'inversion, et $\theta_{1,0}$ et $\theta_{2,0}$ les paramètres de dépendance de mobilité en fonction de la charge d'inversion, liés aux différentes interactions (Coulomb, phonons, rugosité de surface).

Nous utilisons ensuite le modèle de résistance d'accès suivant:

$$R_{ACC} = R_0 + \frac{\sigma}{Q_{INV}} \tag{C.2}$$

avec R_0 la composante constante et σ le paramètre de dépendance avec la charge d'inversion. Ce modèle est proposé car il permet de rendre compte de la région sous l'espaceur. Cette région est sensible au niveau d'inversion (c'est à dire à la tension de grille) par couplage électrostatique. De plus, ce modèle permet de prendre en compte la résistance dite balistique lorsque les porteurs sont injectés de la source vers le drain sans interaction dans le canal.

Finalement, en écrivant la résistance totale comme la somme de la résistance d'accès et la résistance du canal, nous obtenons:

$$I_D = \frac{\beta Q_{INV} V_D}{1 + \left(\theta_{1,0} + \beta\left(R_0 + \frac{\sigma}{Q_{INV}}\right)\right) Q_{INV} + \theta_{2,0} {Q_{INV}}^2} \tag{C.3}$$

qui peut être écrit:

$$I_D = \frac{B Q_{INV} V_D}{1 + \Theta_1 \cdot Q_{INV} + \Theta_2 \cdot {Q_{INV}}^2} \tag{C.4}$$

avec:

$$\begin{cases} B = \dfrac{\beta}{1+\beta\,\sigma} \\ \Theta_1 = \dfrac{\theta_{1,0}+\beta R_0}{1+\beta\,\sigma} \\ \Theta_2 = \dfrac{\theta_{2,0}}{1+\beta\,\sigma} \end{cases} \tag{C.5}$$

avec $\beta = \frac{W}{L}\mu_0$. Les paramètres Θ_i peuvent être exprimés selon:

$$\begin{cases} \Theta_1 = \theta_{1,0} + B\,(R_0 - \sigma\,\theta_{1,0}) \\ \Theta_2 = \theta_{2,0}\,(1 - B\,\sigma) \end{cases} \tag{C.6}$$

En mesurant des transistors de différentes longueurs de grille, les paramètres σ et $\theta_{2,0}$ peuvent être extraits à l'aide d'une régression linéaire sur la courbe $\Theta_2(B)$. Dans un second temps, les paramètres R_0 et $\theta_{1,0}$ sont extraits de la même façon sur la courbe $\Theta_1(B)$. Une fois que σ a été extrait, la mobilité pour chaque longueur de grille est déterminée selon:

$$\mu_0 = \frac{L}{W} \cdot \frac{B}{1-\sigma B} \tag{C.7}$$

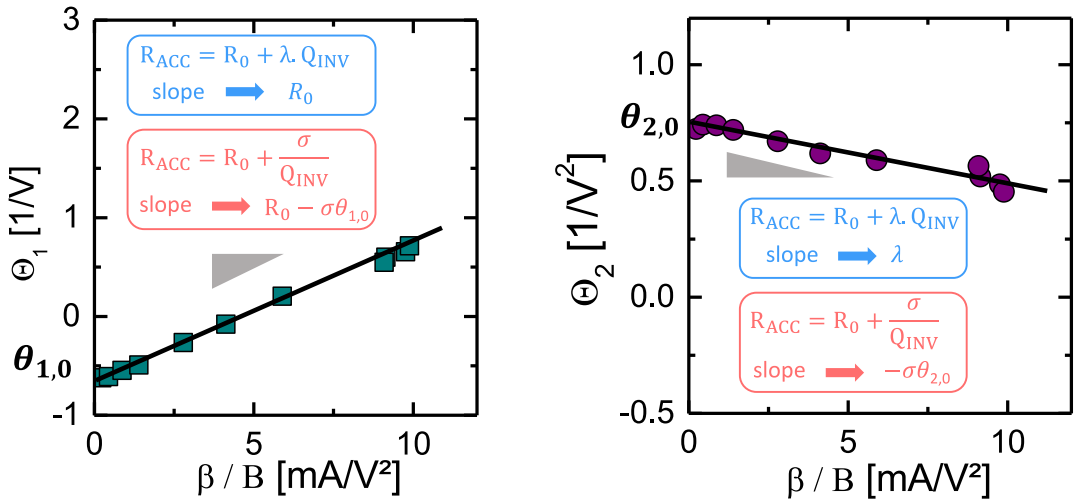

Figure C.1: (gauche) Θ_1 et (droite) Θ_2 *vs.* β (ou B). Les paramètres de mobilité et de résistance d'accès sont extraits à partir de régressions linéaires, selon le modèle de dépendance en charge d'inversion considéré.

La Figure C.1 montre les courbes $\Theta_1(B)$ et $\Theta_2(B)$ pour des nFETs de la technologie FDSOI 14nm. La linéarité de ces courbes prouve la pertinence de l'extraction. Une comparaison des différentes méthodes d'extraction est effectuée sur la résistance d'accès en fonction de la charge d'inversion (Figure C.2) et sur la mobilité en fonction de la longueur de grille (Figure C.3). Notre nouvelle méthode est cohérente avec la méthode Rtot(L) en ce qui concerne $R_{ACC}(Q_{INV})$.

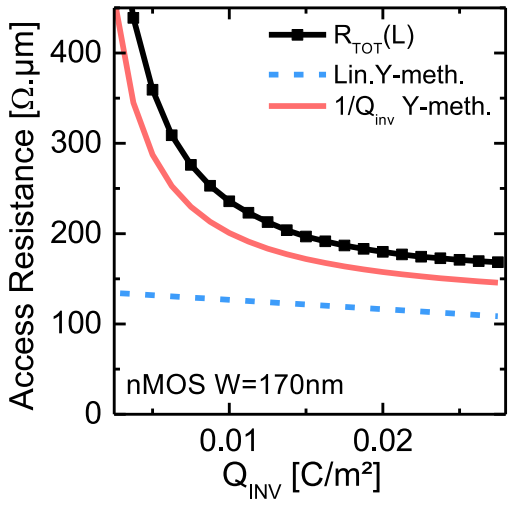

Figure C.2: Résistance d'accès en fonction de la charge d'inversion selon la méthodologie employée. Notre nouvelle méthode est en accord avec la méthode Rtot(L), sans faire l'hypothèse d'une mobilité constante.

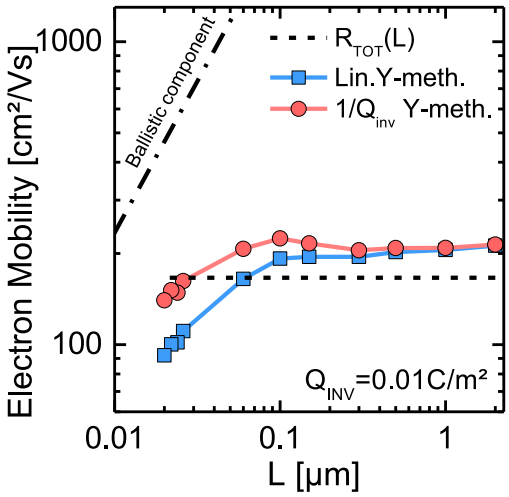

Figure C.3: Mobilité en fonction de la longueur de grille selon la méthodologie d'extraction employée. La chute de mobilité pour les transistors courts donnée par la Fonction-Y classique est atténuée pour notre méthodologie.

Qui plus est, notre méthode permet d'extraire le comportement µ(L). Par rapport à la Fonction-Y classique, la dégradation de la mobilité pour les transistors courts est réduite. La Fonction-Y classique ne permet pas de distinguer proprement la région d'accès du canal. Elle sous-estime la résistance d'accès et par conséquent la mobilité. Ceci est dû au fait que la Fonction-Y classique ne prend correctement pas en compte la région sous l'espaceur et la contribution balistique.

C.2.2 Résultats expérimentaux

Nous avons ensuite extrait la résistance d'accès pour différents transistors (FDSOI, nanofils) dont le canal est contraint par diverses techniques (sSOI, CESL, SiGe).

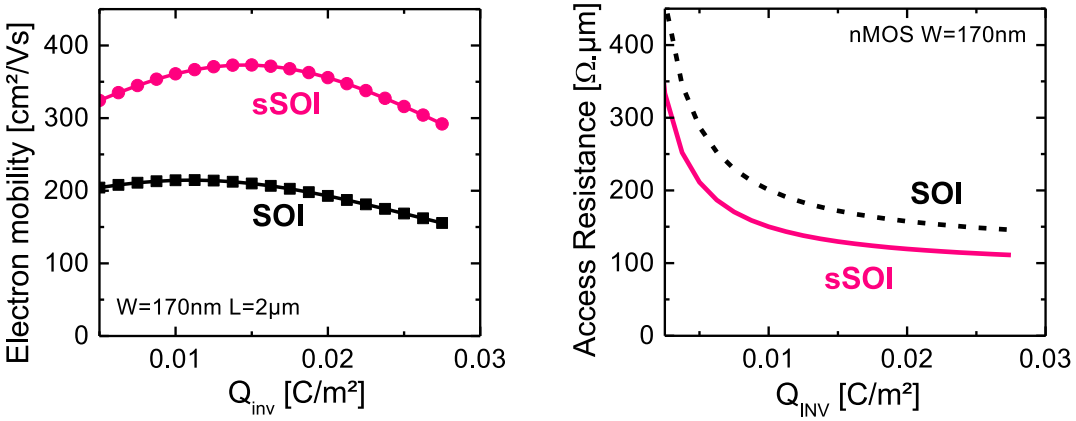

Figure C.4: Extraction de (gauche) la mobilité des électrons pour un canal long (L=2µm) et (droite) la résistance d'accès selon notre nouvelle méthodologie pour des nFETs fabriqués sur SOI et sSOI. La contrainte en tension améliore la mobilité mais également diminue la résistance d'accès des dispositifs.

En ce qui concerne l'utilisation d'un substrat sSOI (strained-SOI), une tension de l'ordre de 1.3GPa est présente dans le canal. Nous nous concentrons ici sur le transport dans les nFETs. La Figure C.4

montre la mobilité extraite par notre nouvelle méthodologie, présentée dans la section précédente. Comme attendu, la mobilité des électrons pour un canal long est fortement améliorée grâce à la contrainte en tension. La Figure C.4 représente également la résistance d'accès en fonction de la charge d'inversion, extraite pour les deux cas sSOI et SOI. En plus de l'effet sur la mobilité, la contrainte tensile réduit la résistance d'accès du dispositif (de -25% à Q_{INV}=0.01C/cm^2).

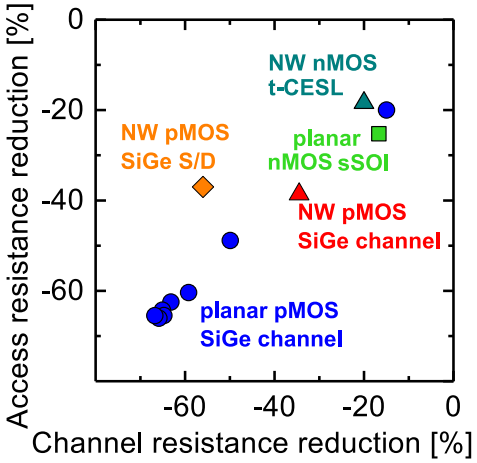

Figure C.5: Corrélation entre la variation de résistance d'accès par rapport à la variation de résistance de canal (c'est à dire mobilité) pour différents types de transistors et d'intégrations de contrainte. La résistance d'accès est impactée par la contrainte au même titre que la mobilité, avec une sensibilité similaire.

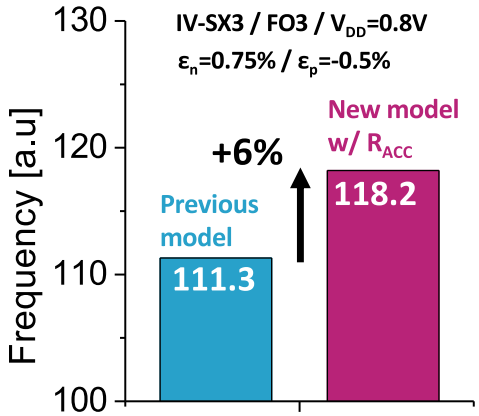

Figure C.6: Gain en fréquence dû à l'introduction d'une contrainte supplémentaire pour un oscillateur en anneau d'inverseurs à 3 doigts de grille. En considérant l'impact de la contrainte sur la résistance d'accès, le gain passe de +11% (ancien modèle) à +18% (nouveau modèle).

La Figure C.5 trace la variation de la résistance d'accès par rapport à celle du canal, gouvernée par la mobilité. Pour les différent transistors étudiés (FDSOI planaire et nanofils) et pour plusieurs techniques d'intégration de contrainte, une forte corrélation est observée. Ainsi, la contrainte impacte non seulement la mobilité dans le canal mais également la résistance d'accès des dispositifs. De plus, la sensibilité est similaire. Nous attribuons ce résultat à la région sous l'espaceur, qui contribue fortement à la résistance d'accès du transistor et qui n'a pas de raison d'être insensible à la contrainte. En outre, la résistance balistique est également impactée par la contrainte car sensible à la masse effective.

Finalement, nous avons ajouté la dépendance des résistances d'accès avec la contrainte dans le modèle compact. Nous avons simulé la fréquence d'oscillateur en anneau d'inverseurs à 3 doigts de grille. Avec le modèle de référence, l'ajout d'une contrainte supplémentaire au sein des nFETs (ε_n=0.75%) et pFETs (ε_p=-0.5%) se traduit par un gain en fréquence de +11%. Si nous considérons maintenant l'impact de la contrainte sur les résistances d'accès, ce gain est estimée à +18%. Ce résultat renforce l'intérêt de la contrainte pour améliorer la performance des technologies CMOS. En outre, il est primordial de considérer cette dépendance afin de réaliser des simulations prédictives et optimiser les circuits intégrés.

C.3 Effets géométriques induits par la contrainte du canal SiGe des pMOSFETs en FDSOI

Dans ce chapitre, nous nous concentrons sur le canal SiGeOI des pFETs de la technologie FDSOI 14nm. Celui-ci est réalisé par un procédé de condensation, qui tire parti de l'oxydation préférentielle du Silicium par rapport au Germanium. Cette technique permet donc d'obtenir localement un alliage de SiGe directement sur isolant, sur lequel sont ensuite fabriqués les pFETs.

C.3.1 Mesure et modélisation de déformation dans les pMOSFETs à canal SiGe

C.3.1.a Relaxation de contrainte en bord de motif

Lors du procédé de fabrication, la définition des zones actives est réalisée après la formation de SiGeOI sur les zones des pFETs. Ainsi, le SiGe est gravé pour réaliser les tranchées d'isolation (STI). Lors de cette gravure, une condition de bord libre est introduite, permettant à la contrainte compressive propre au SiGe de se relaxer latéralement. La Figure C.7 montre les profils de déformation dans le plan mesurés par diffraction d'électrons (NBD) en bord de zone active au cours des différentes étapes du module de définition des zones actives.

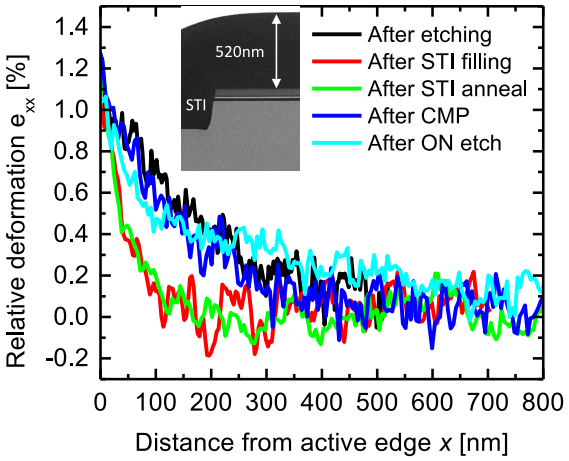

Figure C.7: Profil de déformation du SiGe relative au Silicium dans le plan (e_{xx}) mesurée par NBD en bord de zone active pour différentes étapes du procédé. La condition de bord libre introduite après gravure permet à la contrainte compressive du SiGe de se relaxer latéralement.

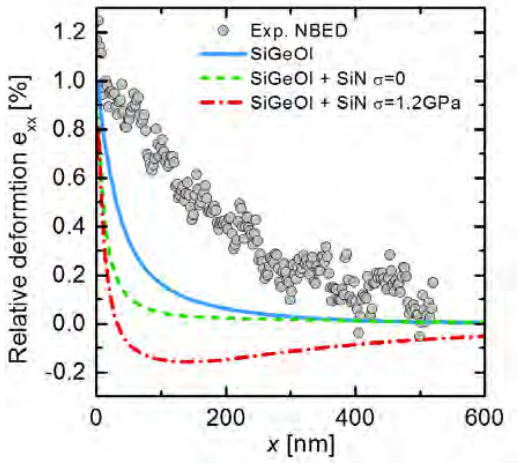

Figure C.8: Comparaison entre le profil de déformation expérimental et plusieurs simulations mécaniques dans le domaine élastique. La simulation ne prévoit pas une relaxation sur une distance aussi élevée, surtout si en considérant le masque dur SiN contraint en tension (1.2GPa après dépôt par LPCVD).

Une déformation relative par rapport au Silicium positive (e_{xx}>0) traduit une relaxation latérale de la contrainte compressive du SiGe. Après gravure, le profil mesuré montre une relaxation s'étendant sur une distance d'environ 300nm. Un profil semblable est obtenu après CMP et retrait du masque dur SiN malgré l'impact du remplissage de l'oxyde. Ce résultat montre que la relaxation est gouvernée par l'étape de gravure.

Nous avons confronté ces résultats à des simulations mécaniques dans le domaine élastique. La Figure C.8 compare le profil de relaxation avec des simulations aux différentes hypothèses concernant le

SiN. Pour tous les cas, les simulations n'expliquent pas la relaxation latérale expérimentale. Ceci est d'autant plus vrai lorsque l'on considère l'effet du SiN, supposé contraint en tension. En effet, le SiN doit aider à maintenir le SiGe en compression (il agit tel un ressort en parallèle). Nous avons émis l'hypothèse d'une faiblesse de la rigidité mécanique de l'interface SiGe/oxyde pour expliquer la forte relaxation observée expérimentalement.

Afin d'étudier plus largement la relaxation latérale du SiGeOI induite par la gravure, nous avons mis en place une méthodologie basée sur des mesures µRaman. En spectroscopie µRaman, le décalage en fréquence propre au mode de vibration Si-Si est directement lié à la déformation selon :

$$\Delta\omega_{SiSi} = \frac{1}{2\omega_0} \cdot [q \cdot (e_{XX} + e_{YY}) + p \cdot e_{ZZ}] \tag{C.8}$$

avec ω_0 la position du pic du Silicium massif, et q et p les potentiels de déformation ($q = -2.31{\omega_0}^2$, $p = -1.85{\omega_0}^2$). En mesurant des réseaux de lignes infinies, nous pouvons écrire sous l'hypothèse de déformation plane:

$$\begin{pmatrix} e_{XX} \\ e_{YY} \\ e_{ZZ} \end{pmatrix} = \begin{pmatrix} (1+\varepsilon_{XX})\,\dfrac{a(SiGe)}{a(Si)} - 1 \\ (1+\varepsilon_{//})\,\dfrac{a(SiGe)}{a(Si)} - 1 \\ \left(-\dfrac{C_{12}}{C_{11}}\left(\varepsilon_{XX}+\varepsilon_{//}\right)+1\right)\dfrac{a(SiGe)}{a(Si)} - 1 \end{pmatrix} \tag{C.9}$$

avec $\varepsilon_{//}$ la déformation initiale avant gravure des motifs. La concentration en Germanium étant déterminée préalablement sur une large zone en faisant l'hypothèse d'une contrainte biaxiale, les paramètres $a(SiGe)$, C_{12}, C_{11} et $\varepsilon_{//}$ sont connus. Il en découle que le décalage du pic Raman est directement lié à la déformation dans la direction perpendiculaire à la ligne de SiGe ε_{XX}.

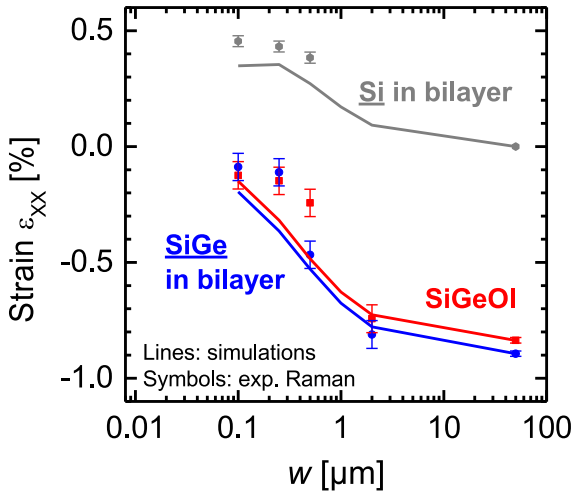

Figure C.9: Déformation e_{XX} extraite par mesures µRaman dans des lignes de SiGe en fonction de leurs largeurs w. Deux cas sont étudiés: SiGeOI obtenu par condensation et un bi-couche SiGe/Si obtenu par épitaxie. Plus la ligne est étroite, plus la déformation est sensible à la relaxation latérale à partir des bords. La mesure µRaman permet également d'extraire la déformation en tension dans le Si du bi-couche SiGe/Si.

La Figure C.9 montre la déformation extraite par µRaman en fonction de la largeur de la ligne pour deux cas distincts de SiGe d'épaisseur 20nm: SiGeOI obtenu par condensation et un bi-couche SiGe/Si obtenu par épitaxie. Alors que la simulation ne prédit pas de différence majeure entre les deux échantillons, le cas SiGeOI est plus relaxé que le cas SiGe pour une largeur de ligne de

500nm. Ce résultat laisse supposer que le comportement de l'interface SiGe/oxyde diffère de celui de l'interface Si/oxyde. De plus, la mesure µRaman permet d'extraire la déformation dans la couche Si du bi-couche SiGe/Si, mettant en évidence une tension générée par la relaxation du SiGe. Cela traduit la bonne rigidité mécanique de l'interface SiGe/Si.

En conclusion, le film SiGeOI obtenu par condensation permet d'atteindre un fort niveau de contrainte compressive dans le canal des pFETs. Cependant, lors de la définition des zones actives, une relaxation latérale de la contrainte a lieu en bord de motif.

C.3.1.b Contrainte générée par les source/drain SiGe

En technologie FDSOI 14nm, la contrainte compressive des pFETs provient du canal SiGe mais également de l'utilisation de source et drain surélevées en SiGe:B ayant une concentration en Germanium de 30%. Nous avons évalué le niveau de contrainte générée par les source/drain à l'aide de simulations mécaniques. La Figure C.10 montre le profil de déformation relative au Silicium dans le SiGeOI, mesuré en fin de procédé de fabrication. Les oscillations proviennent de l'alternance entre la région du canal (sous la grille) et la zone de source/drain. Un bon accord entre la simulation et la mesure expérimentale par NBD est observé.

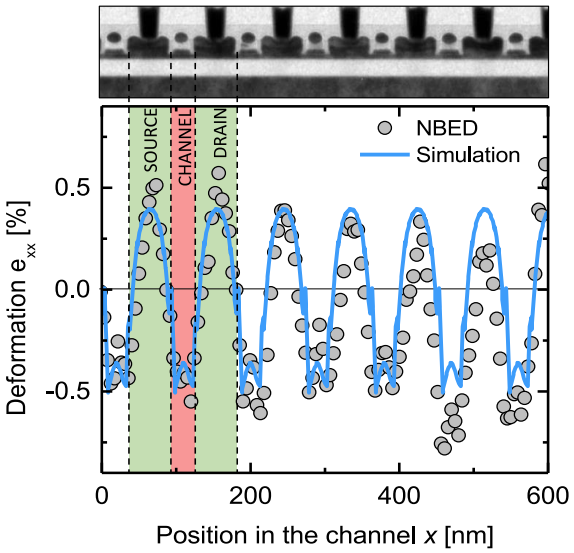

Figure C.10: Déformation relative par rapport au Silicium dans le SiGeOI en fin de procédé de fabrication. La simulation est en accord avec la mesure expérimentale par NBD. Les oscillations proviennent de l'alternance entre les canaux (sous la grille) et les régions de source/drain. Une déformation supplémentaire d'environ -0.4% est générée par les source/drain $Si_{0.7}Ge_{0.3}$:B.

Il est important de souligner que cette mesure est réalisée loin des bords de zone active et donc non impactée par la relaxation latérale due à la gravure. Nous avons montré que dans ce cas, la contrainte générée par les source/drain ne dépend pas de la concentration en Germanium dans le canal SiGeOI mais uniquement de celle des source/drain. En effet, le paramètre de maille du canal est celui du Silicium, quelque soit sa concentration en Germanium. La contrainte induite par les source/drain provient de la relaxation de leur énergie élastique. Or, plus ils sont concentrés en Ge, plus leur énergie élastique est importante. Le canal subit ainsi une contrainte compressive supplémentaire.

Nous nous sommes également intéressés aux régions impactées par la relaxation latérale du canal SiGeOI. Dans cette région, les source/drain SiGe:B sont fabriqués sur un substrat ayant un paramètre de maille plus large que celui du Silicium. Ainsi, la contrainte intrinsèque au sein des source/drain SiGe:B dépend de l'état de relaxation du substrat sous-jacent. La Figure C.11 illustre cet effet. La

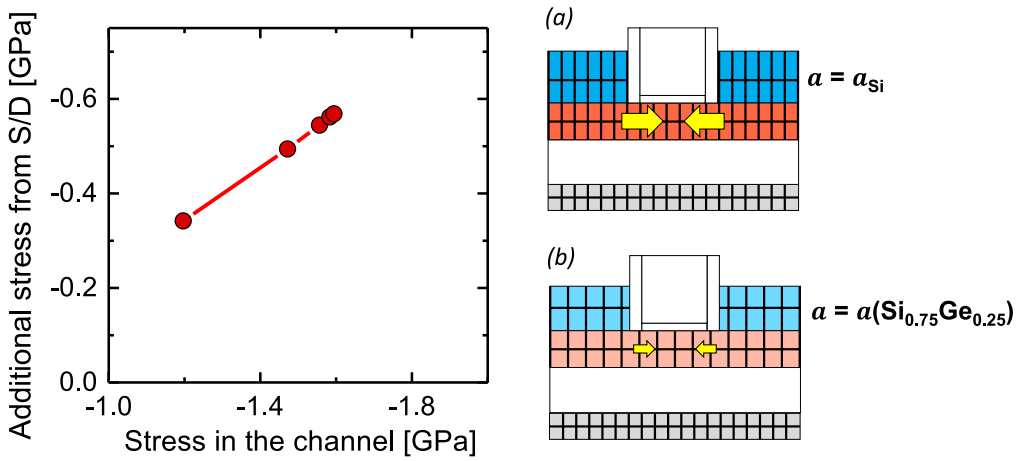

Figure C.11: Simulation de la contrainte additionnelle générée par les source/drain $Si_{0.7}Ge_{0.3}$:B en fonction de l'état de contrainte du substrat SiGeOI. A cause de la relaxation latérale du SiGeOI induite par la gravure, la croissance des source/drain est réalisée sur un substrat dont le paramètre de maille est plus large que celui du Silicium. En conséquence, la contrainte intrinsèque aux source/drain est plus faible et il est résulte une plus faible contrainte générée dans le canal.

contrainte additionnelle générée par les source/drain est plus faible lorsque la contrainte du canal est partiellement relaxée (à cause de la gravure de la zone active). Finalement, la relaxation latérale du canal SiGeOI diminue également la contrainte générée par les source/drain. Les dispositifs sont donc doublement impactés.

C.3.1.c Modélisation analytique

Nous proposons un modèle analytique pour rendre compte de la relaxation latérale de la contrainte induite par la définition des zones actives. La contrainte σ à une position x le long de la zone active est donnée par:

$$\sigma(x,L_{act}) = \sigma_0(x_{Ge}) \cdot \left[1 - \exp\left(-\frac{x}{\lambda}\right) - \exp\left(-\frac{L_{act}-x}{\lambda}\right) + \exp\left(-\frac{L_{act}}{\lambda}\right)\right] \tag{C.10}$$

où σ_0 est la contrainte initiale, dépendante de la concentration en Germanium x_{Ge}, L_{act} est la longueur d'active, et λ est la longueur typique de relaxation. Ce modèle respecte la condition de contrainte nulle en bords de zone active (pour x=0 et x=L_{act}). Ce modèle est utilisé dans les deux directions longitudinale et transverse. En direction transverse, la contrainte est moyennée en intégrant selon le profil puisque la grille recouvre l'ensemble de la zone active. En direction longitudinale, nous prenons également en compte la contrainte générée par les source/drain ainsi que l'impact de la relaxation du canal SiGeOI sur celle-ci.

C.3.2 Résultats électriques en technologie 14nm

C.3.2.a Impact des dimensions de zone active

Nous nous intéressons ici aux variations des caractéristiques électriques des pFETs en fonction de la géométrie. Ces variations sont plus communément appelés "effets layout". Un layout typique d'un transistor est illustré en Figure C.12.

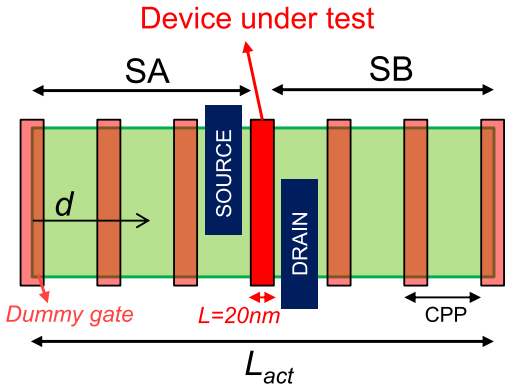

Figure C.12: Illustration d'un layout typique d'un transistor. SA/SB sont les paramètres de distance entre la grille et le bord de la zone active de part et d'autre du canal et W est la largeur d'active. La longueur d'active L_{act} dépend du nombre de pas de fausses grilles (CPP) utilisé.

Parmi les paramètres définissant la géométrie d'un dispositif, nous nous sommes focalisés sur les distances grille-bord de zone active de part et d'autre du canal, appelés SA et SB, ainsi que sur la largeur de la zone active W. Nous nous sommes particulièrement concentrés sur la tension de seuil du transistor et le courant I_{ODLIN}, mesuré en régime linéaire à une tension de grille fixe par rapport à la tension de seuil (V_G-V_T=0.5V). Ces paramètres sont en effet dépendants de la contrainte (décalage des niveaux d'énergie et modification de la mobilité des porteurs).

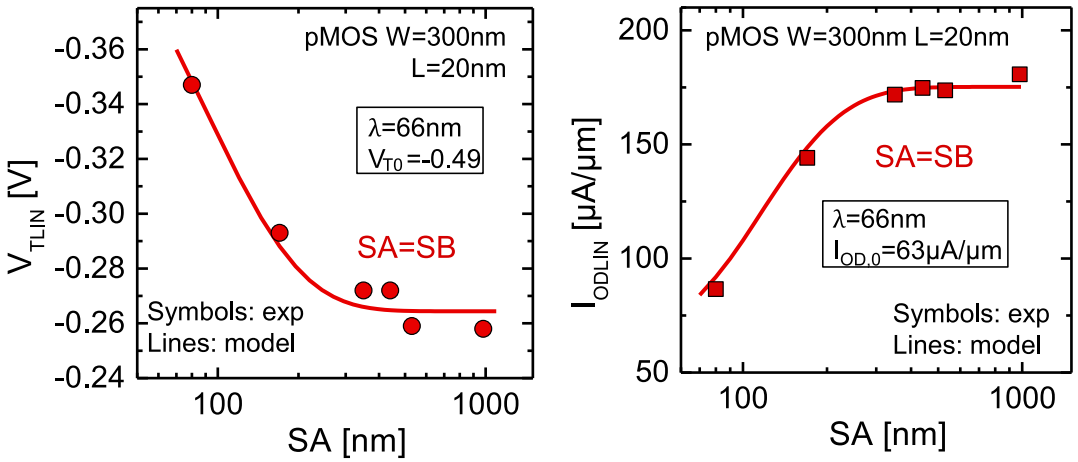

Figure C.13: (gauche) V_{TLIN} and (droite) I_{ODLIN} en fonction de la distance au bord de zone active SA (=SB) pour un pFET à canal SiGeOI (W=300nm L=20nm). La tension de seuil augmente et I_{ODLIN} diminue pour les zones actives courtes à cause de la relaxation de la contrainte longitudinale. Le modèle de relaxation nous permet de reproduire la variation des caractéristiques électriques.

L'effet de la relaxation de la contrainte dans le sens longitudinal est montré en Figure C.13. La tension de seuil augmente et I_{ODLIN} diminue pour les zones actives courtes. Ceci est la conséquence de la relaxation de la contrainte longitudinale. En utilisant le modèle de relaxation présenté précédemment, il nous est possible de reproduire les variations expérimentales des caractéristiques électriques du dispositif. En ce qui concerne le courant I_{ODLIN}, la sensibilité à la contrainte est donnée par le

modèle piezorésistif, en prenant en compte la dépendance des résistance d'accès.

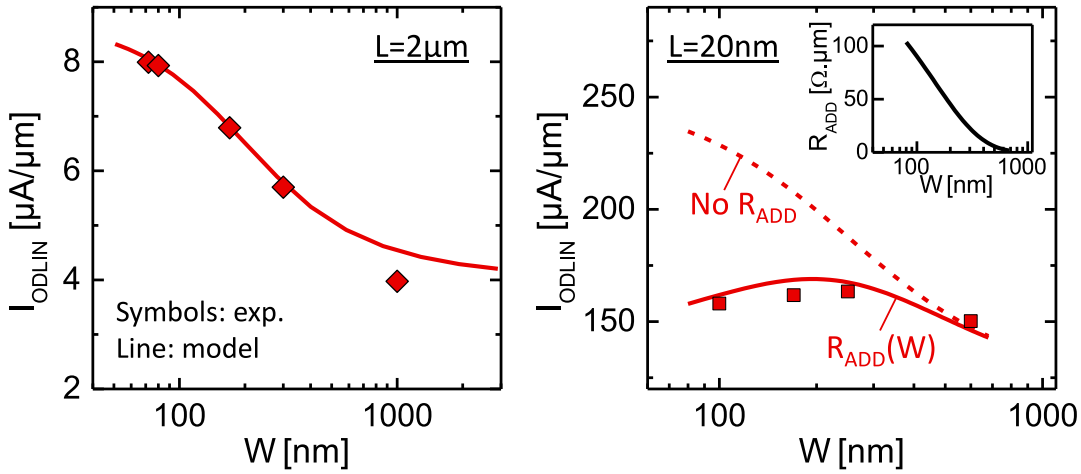

Figure C.14: I_{ODLIN} *vs.* largeur d'active W pour un canal (gauche) long L=2µm et (droite) court L=20nm. La relaxation de la contrainte transverse pour les zones actives étroite se traduit par un gain en mobilité. Alors que le modèle permet de bien reproduire l'effet layout pour un canal long, ce n'est pas le cas pour un canal court. Une hypothèse de résistance d'accès plus prononcée pour les zones actives étroites est avancée. Cette résistance d'accès pourrait provenir de l'épitaxie des source/drain avec facettes (faible vitesse de croissance des plans 111).

Dans le sens transverse, la relaxation de la contrainte se traduit par un gain en mobilité (Figure C.14). En effet, la contrainte compressive transverse est néfaste pour la mobilité des trous dans un canal orienté selon la direction <110>. Le modèle permet de reproduire l'augmentation du courant I_{ODLIN} pour les zones actives étroites dans le cas d'un canal long. Pour un canal court, il convient de prendre en compte une résistance d'accès parasite, plus importante pour les transistors étroits. Nous avons attribué cette résistance d'accès aux source/drain surélevés, pouvant montrer des facettes causées par la faible vitesse de croissance des plans 111.

En résumé, la relaxation en bord de motif impacte directement les caractéristiques électriques des dispositifs (V_T,I_{ODLIN}). Notre modèle basé sur un profil de contrainte nous permet de reproduire les variations expérimentales.

C.3.2.b Impact de la concentration en Germanium

Nous avons étudié les effets layout pour des canaux SiGeOI de différentes concentrations en Germanium: 25%, 30% et 34%. La Figure C.15 montre le comportement I_{ODLIN}(SA). Pour les SA longs, le courant I_{ODLIN} augmente avec la concentration en Germanium, car le niveau de contrainte augmente. En revanche, une dégradation est observée pour les SA courts. Ceci s'explique par les effets opposés des contraintes compressives longitudinales et transverses. En effet, pour une courte zone active, la composante majoritaire de la contrainte est transverse. Or cette composante est néfaste pour la mobilité des trous. Augmenter la contrainte avec la concentration en Ge se traduit donc par une dégradation de la mobilité. Pour les SA longs, la composante majoritaire est longitudinale et par conséquent bénéfique. De ce fait, les courbes I_{ODLIN}(SA) se croisent.

Le croisement des courbes expérimentales est bien prédit par le modèle, qualitativement et quantitativement. Il est intéressant de noter qu'une seule longueur typique de relaxation permet de reproduire

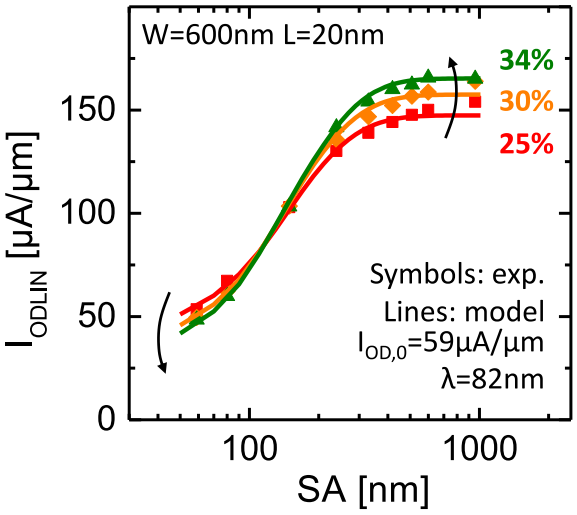

Figure C.15: I_{ODLIN} *vs.* SA (=SB) pour des pFETs à canal SiGeOI de différentes concentrations en Ge (W=600nm L=20nm). Pour les zones actives longues, plus la concentration en Ge est élevée, plus la mobilité est élevée. Ceci est dû à l'augmentation de la contrainte compressive et notamment de sa composante longitudinale, qui est bénéfique. En revanche, pour les SA courts, la composante majoritaire est transverse. Le fait que cette composante soit néfaste se traduit par une dégradation pour les concentrations en Ge plus élevées. Le modèle permet de reproduire qualitativement et quantitativement le croisement, en utilisant une seule longueur typique de relaxation.

les données expérimentales des trois concentrations en Germanium différentes. Cela laisse supposer que la relaxation latérale ne dépend ni du niveau de contrainte initiale ni de la teneur en Germanium. Ces propos sont toutefois à nuancer, la plage de concentration en Germanium étudiée étant limitée.

C.4 Solutions pour améliorer la performance des pMOSFETs à canal SiGe en technologie FDSOI

L'impact de la relaxation de la contrainte sur les caractéristiques électriques des transistors à canal SiGe a été étudié dans la section précédente. Il a été montré que la relaxation dans le sens longitudinal est fortement préjudiciable pour la performance car elle se traduit par une augmentation de la tension de seuil ainsi qu'une dégradation de la mobilité. Dans cette section, des solutions pour améliorer la performance des pMOSFETs à canal SiGe en technologie FDSOI sont proposées. Dans un premier temps, des solutions au niveau "design" sont évaluées. Dans un second temps, des procédés de fabrication alternatifs sont examinés, constituant des solutions dites "technologiques".

C.4.1 Solutions de type "design"

C.4.1.a L'approche "Mix-VT"

Dans une cellule logique telle qu'un inverseur, la performance et la fuite des deux types de transistors (nFETs et pFETs) doivent être équilibrées. Ceci est le cas lorsque les tensions de seuil sont alignées. Or, la relaxation du SiGe entraine une augmentation de V_T pour les zones actives courtes. De ce fait, une cellule logique ayant une courte zone active n'est pas équilibrée. C'est le cas de l'inverseur à un doigt de grille par exemple.

La première solution de type design consiste à utiliser au sein d'une même cellule un pFET et un nFET issus de différentes options de V_T. En particulier, combiner un nFET RVT (Regular-V_T, c'est à dire de tension de seuil normale) avec un pFET LVT (Low-V_T, c'est à dire de tension de seuil basse) permet de rééquilibrer la cellule. En effet, l'augmentation de V_T due à la relaxation de contrainte est compensée par l'utilisation d'une option de V_T plus faible par construction (par dopage du canal par exemple). Ceci est illustré en Figure C.16 montrant les caractéristiques de transfert des nFETs et pFETs de courte zone active pour deux différentes options de V_T. Le nFET RVT est aligné avec le pFET LVT pour SA=59nm.

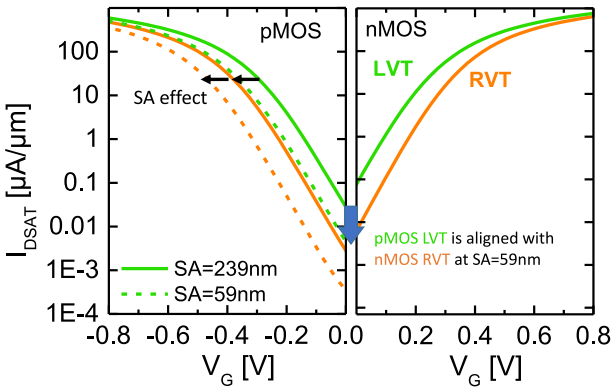

Figure C.16: Caractéristiques de transfert $I_D(V_G)$ pour les deux options de V_T et pour deux longueurs de zone active. Pour SA=59nm, le nFET RVT est aligné au pFET LVT à cause de la relaxation de la contrainte augmentant le V_T du pFET.

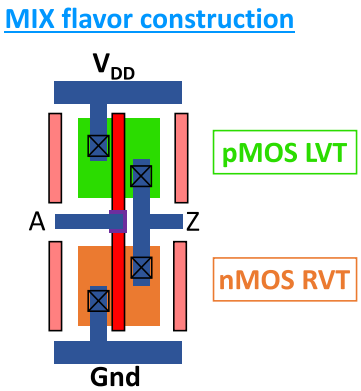

Figure C.17: Layout de l'inverseur à un doigt de notre approche MIX, qui consiste à mixer un pFET LVT avec un nFET LVT pour compenser l'effet de la relaxation de la contrainte.

Nous avons étudié cette approche appelée MIX et dont le layout est illustré en Figure C.17 à l'aide de simulations SPICE. Les effets de contraintes sont pris en compte avec le modèle présenté en section précédente et les différentes options de V_T sont définies manuellement par un décalage de 100mV.

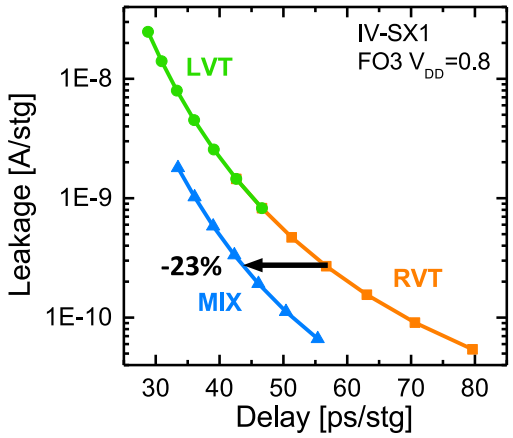

Figure C.18: Compromis fuite/délai simulé pour un inverseur à un doigt (IV-SX1) à V_{DD}=0.8V pour les différentes options de V_T. Une réduction du délai de 23% est prédite pour l'approche MIX par rapport à la référence RVT.

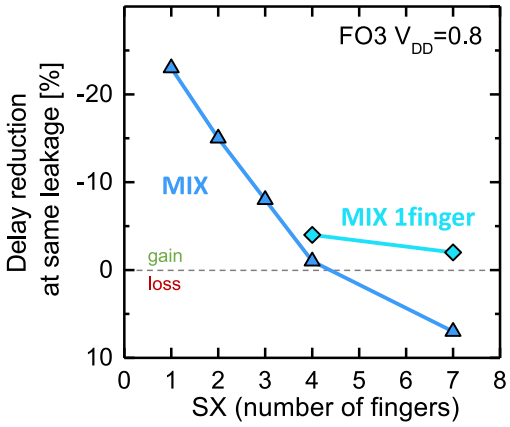

Figure C.19: Gain en délai pour une fuite donnée en fonction du nombre de doigts de grille de l'inverseur. Plus la zone active est longue, moins l'approche MIX est pertinente car la relaxation de la contrainte a lieu en bord de zone active. L'approche "MIX 1 finger" où seulement les premiers doigts de grille en partant du bord sont de type LVT au lieu de RVT permet d'améliorer le compromis pour les inverseurs à plus de 4 doigts de grille.

La Figure C.18 représente le compromis délai/fuite pour un inverseur à un doigt (IV-SX1) pour les deux options de V_T RVT et LVT ainsi que pour notre approche "MIX". Pour une consommation donnée, le délai est réduit de 23% par rapport à la cellule RVT de référence. La cellule RVT de référence souffre de la faible performance du pFET et d'une fuite gouvernée par le nFET. La cellule MIX assure un meilleur équilibrage nFET/pFET et donc une vitesse optimisée à une fuite donnée. Pour les plus faibles tensions d'alimentation, l'approche MIX est encore plus pertinente (-49% délai pour V_{DD}=0.6V). Ceci est dû au fait que la performance est proportionnelle à V_{DD}-V_T (appelé "overdrive"). Les effets de variation de V_T dont donc exacerbés à faible tension d'alimentation.

Puisque l'IV-SX1 est la cellule la plus impactée par la relaxation de la contrainte, l'approche MIX est d'autant plus pertinente pour cette cellule. Le gain en vitesse diminue lorsque la zone active de la cellule est plus longue (Figure C.19). L'approche MIX dégrade même le compromis pour les inverseurs ayant plus de 4 doigts de grille. Pour ces cellules, utiliser des pFETs de type LVT déséquilibre la cellule et donc augmente significativement la fuite, sans fortement améliorer la performance qui reste limitée par les nFETs. Puisque la relaxation a lieu en bord de zone active, utiliser des pFETs de type LVT seulement sur le doigt de grille proche de la bordure de zone active permet de rééquilibrer la cellule à une granularité plus fine. Cette approche, appelée "MIX 1 finger", reste pertinente pour les cellules de longue zone active comme l'inverseur à 7 doigts par exemple.

C.4.1.b L'approche de zone active continue (CRX)

La seconde solution de type design consiste à dessiner les cellules sur une zone active continue, c'est à dire non gravée dans le sens longitudinal. Cette approche, appelée Continuous-RX (CRX), est illustrée en Figure C.20. Par rapport à un dessin de type "Tucked-Under", l'approche CRX permet d'améliorer la densité, en économisant la largeur d'un pas de grille. En évitant la gravure dans le sens longitudinal, la contrainte compressive dans le canal SiGe des pFETs est maintenue.

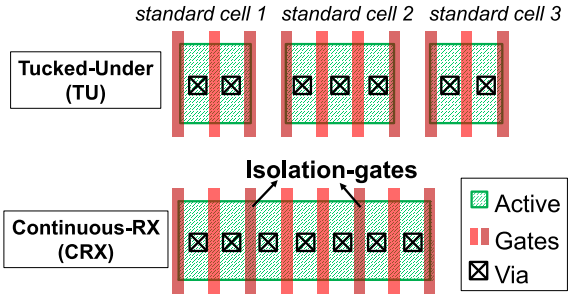

Figure C.20: Illustration des approches de dessin conventionnel ("Tucked-Under") et de type "Continuous-RX" (CRX). Le CRX consiste à dessiner les cellules sur une même bande de zone active et de les isoler à l'aide de grilles d'isolations. De ce fait, la zone active n'est pas gravée dans le sens longitudinal et la contrainte compressive est maintenue dans cette direction.

Afin de contrôler la fuite entre les cellules juxtaposées les unes aux autres, il est nécessaire d'utiliser des grilles d'isolation. Cette grille d'isolation constitue un transistor parasite qui est maintenu en régime bloqué par l'intermédiaire d'un contact spécifique. Ce contact permet de court-circuiter la source et la grille du transistor parasite, limitant la fuite entre deux cellules voisines.

La Figure C.21 montre le compromis Fuite/Délai pour des oscillateurs en anneau d'inverseurs à 1, 2 ou 3 doigts de grille. Le dessin de type CRX permet d'améliorer fortement la performance à une consommation donnée. L'inverseur à 1 doigt (IV-SX1) voit son délai réduit de 28% par rapport au design de référence de type "Tucked-Under". Ceci est dû au maintien de la contrainte longitudinal dans le canal SiGe des pFETs et donc un V_T plus en ligne avec celui du nFET et une mobilité des trous fortement améliorée. Le gain diminue plus le nombre de doigts de l'inverseur augmente car plus la zone active est longue, moins la cellule est impactée par la relaxation.

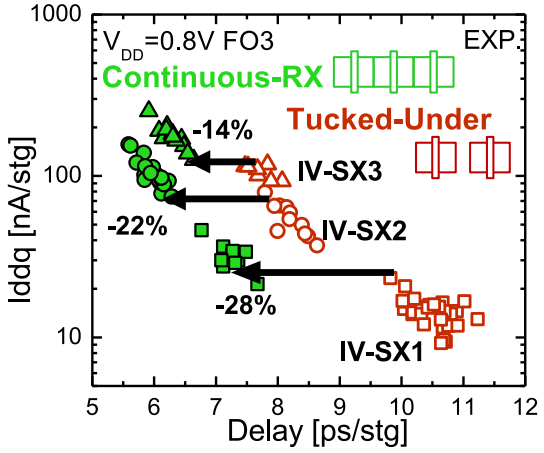

Figure C.21: Compromis Fuite/Délai pour des oscillateurs en anneau d'inverseurs à 1, 2 ou 3 doigts de grille selon la configuration CRX ou "Tucked-Under" (résultats expérimentaux). L'approche CRX permet de fortement réduire le délai (-28% pour l'IV-SX1) en optimisant l'état de contrainte. L'augmentation de la fuite est due au plus faible V_T des pFETs ainsi qu'aux grilles d'isolations (transistors parasites).

Hormis la fuite supplémentaire générée par la grille d'isolation, un autre inconvénient de l'approche CRX est la relaxation partielle pour les zones actives non rectangulaire. En particulier, des décrochés de zone active peuvent apparaitre lorsque deux cellules sont juxtaposées. Ces décrochés vont se traduire par une relaxation partielle de la contrainte qui va directement impacter les caractéristiques

électriques des pFETs. Non seulement la performance de la cellule va être dégradée mais surtout elle sera dépendante des cellules voisines. La juxtaposition devient alors une nouvelle source de variabilité de la performance d'une porte logique.

Afin de limiter l'impact des décrochés, l'utilisation de cellules tampons peut être judicieuse. Ces cellules tampons consistent en une zone active non connectée de la largeur d'un pas de grille. Cela permet d'éloigner le décroché des doigts de grille actifs et donc de limiter l'impact de la relaxation partielle de la contrainte. Même si cette cellule tampon est efficace du point de vue de la performance (une augmentation de +16% de la fréquence est simulée pour l'IV-SX1 ayant des cellules voisines aux zone actives 2× moins larges), elle a un coût en matière de densité.

C.4.2 Solutions technologiques

Les solutions de type dessin présentées dans la section précédente permettent d'améliorer la performance sans modifier le procédé de fabrication. Dans cette section, nous évaluons des schémas d'intégrations différents permettant d'augmenter la performance à travers une optimisation de la configuration de contrainte.

C.4.2.a Intégration alternative de SiGe: l'approche SiGe-last

En ce qui concerne le module de fabrication du canal SiGe, il est réalisé par condensation avant la gravure des zones actives dans le procédé de référence. C'est pourquoi celui est nommé "SiGe-first". Nous avons évalué un schéma d'intégration alternatif dans lequel le SiGe est fabriqué après la définition des zones actives (gravure et remplissage des tranchées d'isolation). Dans cette approche, appelée "SiGe-last", le SiGe est obtenu par épitaxie sans étape de condensation (voir Figure C.22). Il en résulte un bi-couche SiGe/Si sur isolant. Ceci est démontré par la cartographie obtenue par analyse dispersive en énergie (EDX) présentée en Figure C.23. La présence d'une fine couche de Silicium entre le BOX et le SiGe est clairement visible.

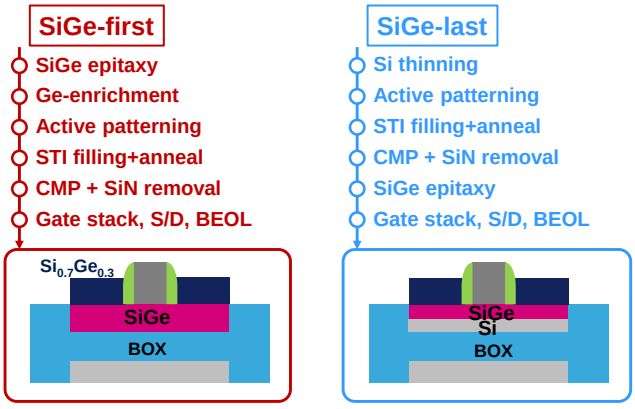

Figure C.22: Schémas d'intégration des procédés "SiGe-first" (référence avec condensation) et "SiGe-last", dans lequel le SiGe est fabriqué par épitaxie après le module de définition des zones actives.

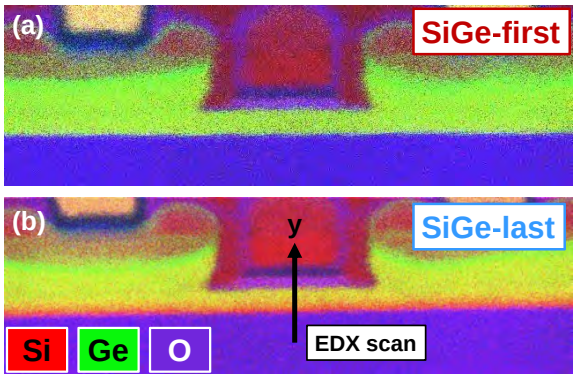

Figure C.23: Cartographie d'analyse dispersive en énergie (EDX) montrant un canal SiGe uniforme pour l'intégration "SiGe-first" et un bi-couche SiGe/Si pour le cas "SiGe-last".

Les caractéristiques des transistors obtenus selon ces deux modes de fabrications ont été évalués pour des géométries différentes. La Figure C.24 montre la variation de mobilité mesurée par la méthode

"split-CV" sur un canal long (L=2µm) en fonction de la largeur du transistor. Le passage d'une configuration biaxiale vers une configuration uniaxiale longitudinale lorsque W diminue se traduit par une augmentation de la mobilité des trous. Cette augmentation est nettement plus marquée pour le procédé "SiGe-first". Ainsi, pour un transistor de zone active étroite W=170nm, l'approche "SiGe-last" dégrade la mobilité de 39%. L'impact de la contrainte dans l'autre direction est évalué sur des transistors courts (L=20nm) pour différents paramètres de longueurs d'active SA (Figure C.25). L'intégration "SiGe-last" limite la dégradation du courant de drain I_{ODLIN} lorsque SA diminue. En résumé, les effets géométriques sont moins importants pour l'intégration "SiGe-last" par rapport à "SiGe-first". Cela est dû à une plus faible relaxation latérale de la contrainte du canal SiGe, c'est à dire sur une longueur typique de relaxation plus courte. Des mesures de déformation (NBED) confirment cette conclusion. La plus faible relaxation peut être expliquée par soit un comportement mécanique différent de l'interface BOX/SOI par rapport à l'interface BOX/SiGe, soit par l'action du STI étant réalisé en amont dans le cas de "SiGe-last".

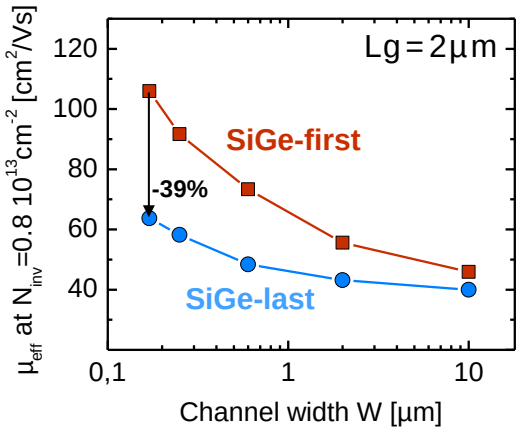

Figure C.24: Mobilité des trous extraite par split-CV sur canal long en fonction de la largeur du transistor pour les deux schémas d'intégration. L'amélioration due à la relaxation de la composante transverse de la contrainte est moins prononcée pour "SiGe-last".

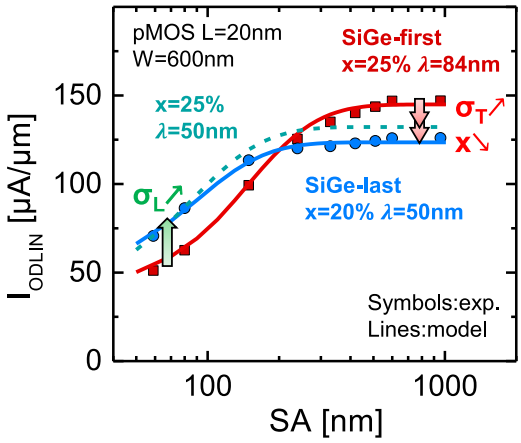

Figure C.25: Courant de drain I_{ODLIN} (mesuré à $V_G=V_T+0.5$) en fonction de SA (distance du transistor au bord de zone active dans le sens longitudinal). La réduction de I_{ODLIN} pour les petits SA est due à la relaxation de la contrainte, dégradation la mobilité des trous. L'approche "SiGe-last" est moins sensible, suggérant une plus faible longueur typique de relaxation latérale.

Toutefois, il est primordial de noter qu'une réduction de la longueur typique de relaxation ne se traduit pas nécessairement par une amélioration de la performance. En effet, la contrainte compressive est bénéfique dans le sens longitudinal pour les canaux orientés selon <110> mais néfaste dans la direction transverse. Cela se traduit par le croisement des courbes I_{ODLIN}(SA) observé en Figure C.25 et bien prédit par le modèle. Finalement, le procédé de fabrication "SiGe-last" est pertinent pour les cellules ayant une zone active courte, c'est à dire inférieure à environ 5 pas de grille en technologie 14nm.

C.4.2.b Isolation duale par tranchées et oxydation (DITO)

Afin de tirer le plus grand parti possible de la contrainte du canal SiGe, il convient de maximiser la composante longitudinale et de minimiser la composante transverse. Dans cette optique, nous

proposons une isolation duale par tranchées et oxydation, appelée DITO. Cette approche consiste à isoler les transistors par un STI classique dans le sens transverse et par une oxydation locale du SiGe dans le sens longitudinal. De ce fait, la gravure des tranchées va permettre la relaxation de la contrainte perpendiculaire au canal. L'oxydation locale du SiGe est réalisée jusqu'à ce que l'oxyde atteigne le BOX afin de parfaitement isoler des cellules construites sur la même bande de zone active. Cette isolation duale requiert deux masques pour la définition des zones actives, disponibles en technologie 14nm. La Figure C.26 montre une image MEB en vue du dessus prise après la définition des zones actives. Le schéma associé met en évidence l'isolation duale par tranchées et oxydation.

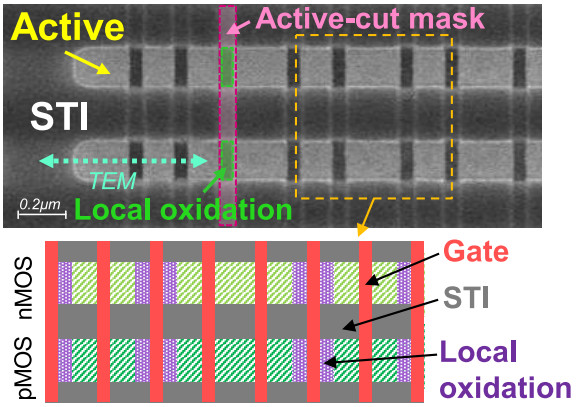

Figure C.26: Image MEB en vue du dessus prise après la définition des zones actives et dessin associé mettant en évidence l'isolation duale par tranchées et oxydation. L'isolation dans le sens longitudinal est réalisée par oxydation locale pour maintenir la contrainte compressive tandis que des tranchées classiques (STI) isolent les transistors dans la direction transverse.

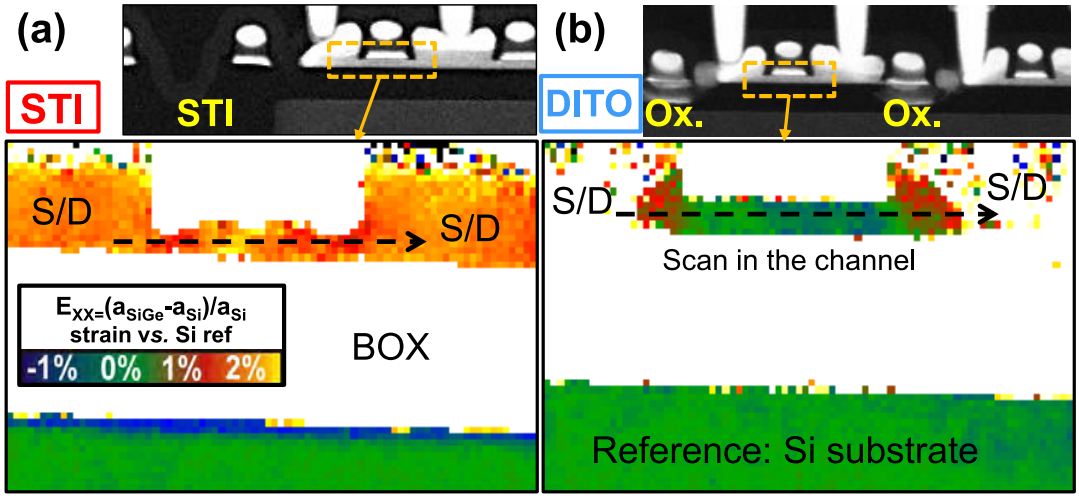

Figure C.27: Cartographie de la déformation par rapport à la référence Si, mesurée par diffraction d'électrons PED (Precession Electron Diffraction) pour un dispositif (a) proche d'une tranchée (STI) et (b) entre deux oxydations locales.

La Figure C.27 montre une cartographie de la déformation par rapport à la référence Si, mesurée par diffraction d'électrons PED (Precession Electron Diffraction). Deux dispositifs sont étudiés: le premier étant proche d'une tranchée (STI) et le second étant situé entre deux oxydations locales. La déformation dans le plan (e_{xx}) pour le dispositif proche du STI est de l'ordre de 1% dans le canal, indiquant que le SiGe de concentration 25% est relaxé. La déformation du dispositif isolé par oxydation locale est proche de e_{xx}=0.1% ce qui correspond à une contrainte compressive d'environ -1.35GPa. Ce résultat démontre que l'oxydation locale permet de maintenir d'avantage la contrainte compressive dans le canal SiGe. Cela impacte directement les caractéristiques électriques

des dispositifs.

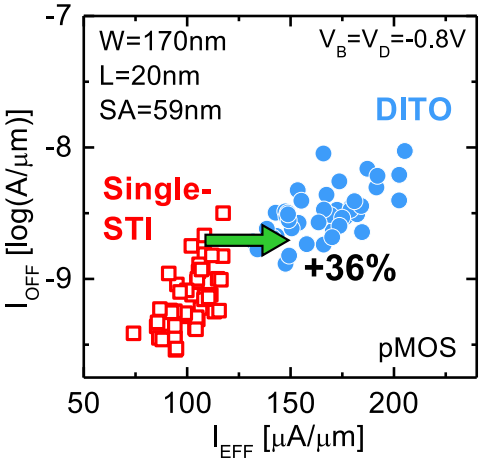

Figure C.28: Compromis I_{EFF}/I_{OFF} pour les pMOSFETs démontrant +36% de gain à même fuite avec une isolation duale (DITO) par rapport à la référence.

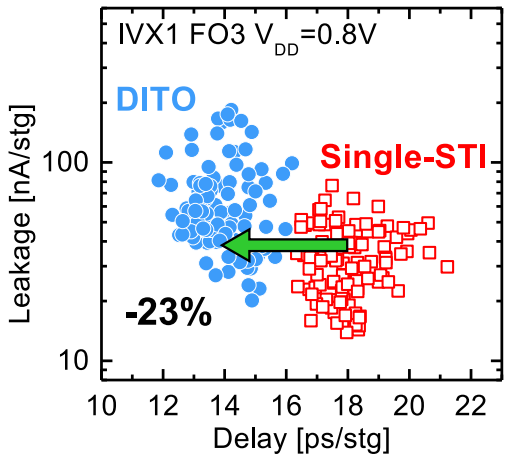

Figure C.29: Compromis fuite/délai (I_{DDQ}/τ_P) d'oscillateurs en anneaux d'inverseurs à un doigt de grille. L'intégration avec isolation duale permet de réduire le délai de 23% par rapport à l'intégration de référence avec STI.

Les dispositifs mesurés correspondent à un doigt de grille sur la zone active la plus courte en technologie 14nm (SA=59nm). La Figure C.28 montre un gain de +36% sur le courant effectif à même fuite avec une isolation duale (DITO) par rapport à la référence. Ce gain est dû à un meilleur maintien de la contrainte compressive et donc une mobilité des trous plus élevée. Ce gain sur la performance du pMOS se traduit par directement sur la vitesse de l'inverseur à un doigt de grille, comme en atteste la Figure C.29. Le délai est en effet réduit de 23% par rapport à l'intégration de référence.

Outre l'optimisation de la contrainte, cette isolation duale permet également d'isoler les caissons arrières des deux types de transistors. Ainsi, la polarisation arrière peut se faire en régime direct (FBB) ou inverse (RBB) sur la même cellule. Au contraire, une isolation avec un simple STI ne permet d'utiliser seulement l'un ou l'autre régime dû à la présence d'une diode PN. L'isolation duale permet donc de bénéficier de l'efficace polarisation arrière de la technologie FDSOI afin d'augmenter la performance ou de réduire la consommation, et ce sur le même dispositif.

C.5 Futures générations de technologie FDSOI

C.5.1 Intégration de contrainte en tension

C.5.1.a L'utilisation de substrats sSOI

Dans les sections précédentes, nous nous sommes focalisés sur l'intégration de contrainte compressive à travers l'introduction de canal SiGe afin d'améliorer la performance des pFETs. En ce qui concerne les nFETs, l'utilisation d'un substrat sSOI (strained-SOI) permet d'obtenir un canal fortement contraint en tension (1.35GPa en utilisant un substrat "tampon" de $Si_{0.8}Ge_{0.2}$). Nous avons étudié les effets layout de dispositifs fabriqués à partir de substrats sSOI en technologie 14nm.

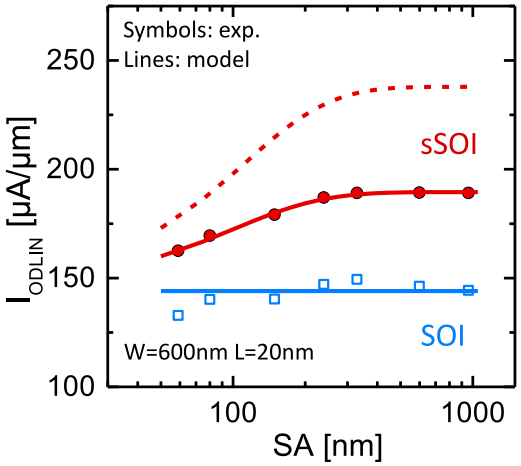

Figure C.30: Courant I_{ODLIN} en fonction de la distance grille-STI SA pour un nFET fabriqué sur substrat sSOI et comparé à la référence SOI. La dégradation du courant pour les petits SA est due à la relaxation longitudinale. Le modèle surestime le gain (tirets). Afin de reproduire les mesures, une résistance d'accès R_{ACC}=132 Ω.µm doit être considérée. La longueur typique de relaxation est λ=86nm.

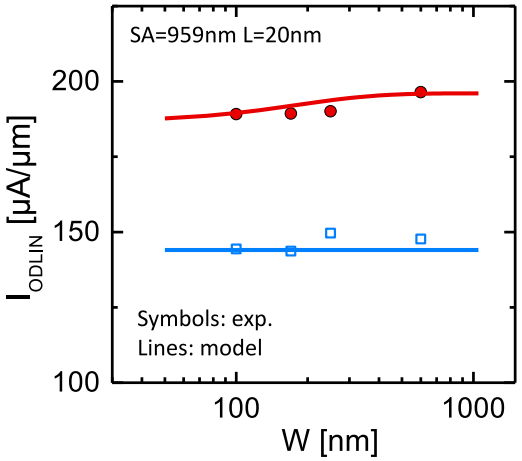

Figure C.31: Courant I_{ODLIN} en fonction de la largeur de zone active W pour des nFETs sSOI et SOI. La faible variation du courant I_{ODLIN} pour le substrat sSOI est due à la relaxation de la contrainte. La contrainte en tension transverse n'a que peu d'impact sur la mobilité des électrons.

La Figure C.30 montre la variation du courant I_{ODLIN} en fonction de la distance au bord de zone active SA. L'utilisation d'un substrat sSOI permet d'améliorer le courant I_{ODLIN} grâce à l'effet de la contrainte tensile sur la mobilité des électrons. La relaxation de la contrainte en bord de zone active se traduit par une dégradation du courant I_{ODLIN}. L'effet dans l'autre direction est présenté en Figure C.31. Néanmoins, la mobilité des électrons n'est que peu sensible à la contrainte tensile transverse. Cela se traduit par une courbe I_{ODLIN}(W) relativement plate.

Le modèle que nous avons développé nous permet de reproduire les données expérimentales, à condition de rajouter une résistance d'accès insensible à la contrainte. La longueur typique de relaxation extraite à partir de ces données électriques est de λ=86nm, ce qui est similaire au cas SiGeOI. Ce résultat laisse penser que la présence de Germanium n'influe pas sur le mécanisme de relaxation latérale. Des études supplémentaires sont néanmoins nécessaires (caractérisations physiques de la contrainte).

L'inconvénient majeur lié au substrat sSOI concerne le pFET puisque le fort niveau de tension est

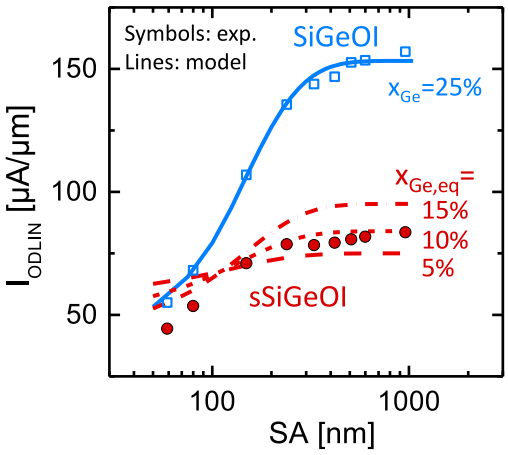

Figure C.32: Courant I_{ODLIN} en fonction de la distance grille-STI SA pour les pFETs à canal SiGe fabriqués sur substrat sSOI (sSiGeOI) et comparé à la référence SiGeOI. Le niveau de contrainte compressive dans le canal sSiGeOI est fortement réduit à cause de la tension du sSOI. Le modèle, calibré sur les données SiGeOI, permet de reproduire les données expérimentales en assumant une contrainte compressive équivalente à une concentration $x_{Ge,eq}$=10% après condensation. La longueur typique de relaxation est λ=82nm.

présent sur l'ensemble du substrat. La Figure C.32 montre le comportement I_{ODLIN}(SA) pour un pFET à canal SiGe fabriqué à partir d'un substrat sSOI (appelé sSiGeOI). Le courant I_{ODLIN} est dégradé à cause de la contrainte en tension présente initialement dans le substrat sSOI. Le niveau final de contrainte dépend de l'écart entre la concentration de Ge dans le substrat tampon pour la fabrication du sSOI et celle obtenue après condensation. Dans notre cas, la contrainte résultante est estimée équivalente à un SiGe de concentration $x_{Ge,eq}$=10%. Cette estimation est réalisée à l'aide de notre modèle, en reproduisant au mieux les données expérimentales.

C.5.1.b La technique de fluage de BOX (BOX-creep)

L'inconvénient majeur du sSOI est la co-intégration de la contrainte. Afin d'améliorer les performances des nFETs sans dégrader celles des pFETs, des techniques d'intégration locale de la contrainte sont nécessaires. C'est le cas de la technique de fluage de BOX, appelée "BOX-creep".

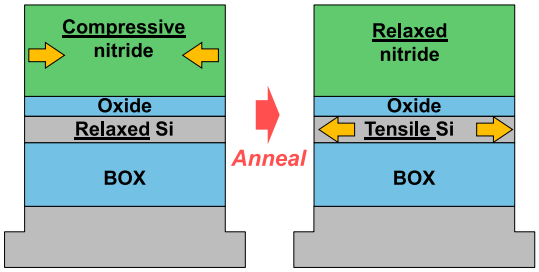

Figure C.33: Principe de la technique de BOX-creep. La faible viscosité du BOX sous recuit à haute température permet au SiN de se relaxer et donc de générer une déformation au sein du SOI. En utilisant un SiN de contrainte compressive, une contrainte en tension est générée dans le SOI.

Le BOX-creep consiste à générer de la contrainte dans le SOI en relaxant l'énergie élastique d'une couche contrainte. La relaxation de la couche contrainte résulte du fluage de l'oxyde enterré sous un recuit à haute température. De façon générale, la couche contrainte est du nitrure de Silicium dont la contrainte provient du procédé de dépôt (Plasma-Enhanced Chemical Vapor Deposition PECVD ou Low-Pressure Chemical Vapor Deposition LPCVD). Le principe du BOX-creep est illustré en Figure C.33. La faible viscosité du BOX sous haute température et sous contrainte permet au SiN de se relaxer, entrainant le SOI avec lui.

Nous avons réalisé des simulations mécaniques basées sur un modèle de viscosité du SiO_2 de type Garofalo. La Figure C.34 montre la contrainte générée dans le SOI au cours du recuit pour deux longueurs d'actives. Une durée de recuit optimale est mise en évidence. Cet optimum, qui dépend de

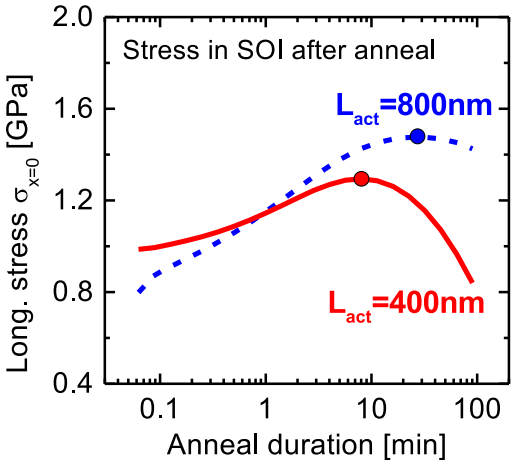

Figure C.34: Contrainte dans le SOI au cours du recuit pour deux longueurs d'active. Une durée optimale pour maximiser la contrainte est mise en évidence.

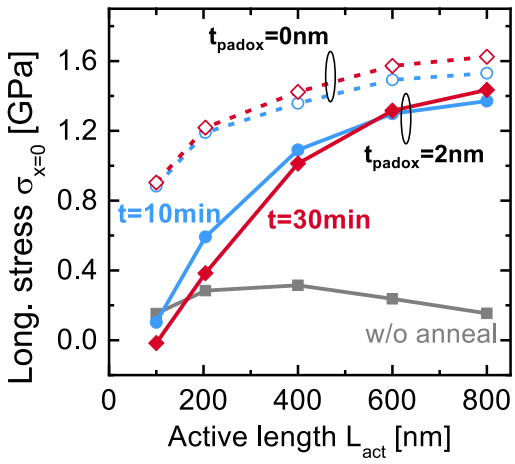

Figure C.35: Contrainte générée par BOX-creep en fonction de la longueur d'active. La diminution de la contrainte pour les courtes zones actives est fortement diminuée lorsqu'aucun oxyde pad n'est utilisé.

la longueur d'active, résulte du fluage parasite de la couche d'oxyde située entre le SOI et le SiN. La Figure C.35 représente la contrainte générée dans le SOI selon la longueur de la zone active. Pour les courtes zones actives, le niveau de contrainte générée par BOX-creep est faible. Une solution pour améliorer ce comportement consiste à ne pas utiliser d'oxyde entre le SOI et le SiN (appelé "oxyde pad").

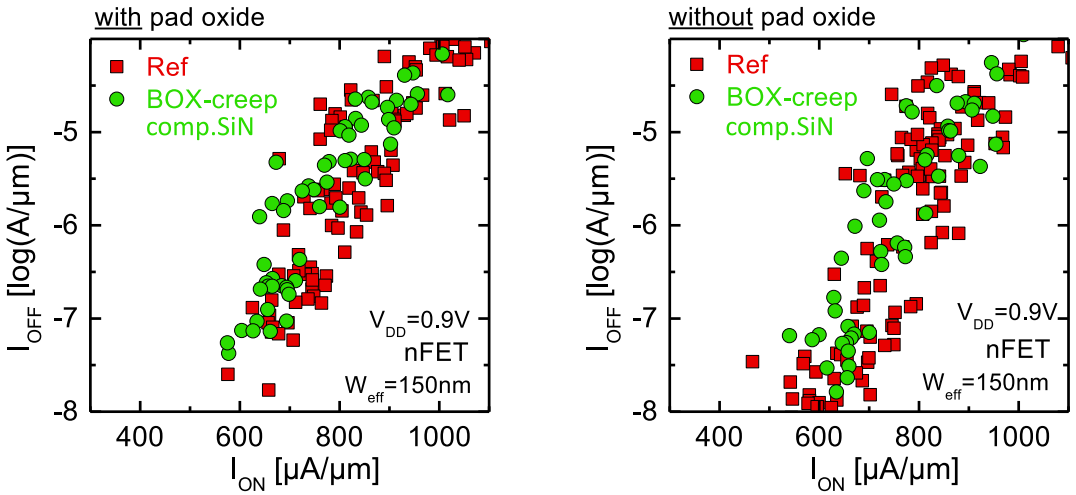

Figure C.36: Compromis I_{ON}/I_{OFF} de nFETs avec et sans BOX-creep que ce soit (gauche) avec ou (droite) sans oxyde pad. Le procédé de BOX-creep, qui utilise un SiN compressif obtenu par PECVD, n'a que très peu d'impact sur la performance. Ce résultat suggère qu'aucune contrainte tensile significative n'a été générée dans le SOI.

Nos simulations nous ont permis de définir des conditions propices pour générer une contrainte tensile locale en FDSOI. Nous avons ensuite fabriqué des dispositifs intégrant ce module de BOX-creep, en utilisant un SiN compressif, déposé par PECVD. La Figure C.36 montre les compromis I_{ON}/I_{OFF} des nFETs avec et sans BOX-creep que ce soit avec ou sans oxyde pad. Puisque les performances sont très proches de la référence, nos résultats électriques ne suggèrent pas une génération de contrainte

efficace avec le procédé BOX-creep. Nous attribuons ce résultat au comportement du SiN sous recuit. En effet, il a été montré qu'un SiN obtenu par PECVD perd rapidement sa contrainte compressive lorsqu'il est chauffé à haute température. Ainsi, la relaxation de son énergie élastique ne s'effectue pas grâce au fluage du BOX et donc aucune contrainte n'est générée dans le SOI.

C.5.1.c La technique de recristallisation de source/drain amorphisés

Nous avons également intégré au sein de la route FDSOI du LETI une autre technique pour générer une contrainte tensile. Cette technique consiste à amorphiser le SOI et le faire recroitre à l'aide d'une épitaxie en phase solide (SPER) en utilisant un germe de SiGe. Contrairement à la technique "STRASS", qui utilise ce procédé pour toute la zone active, nous avons intégré ce module seulement pour la zone des source/drain. Ainsi, la région du canal est protégée lors de l'amorphisation. Un schéma des différentes étapes de ce procédé appelé "SDRASS" est présenté en Figure C.37.

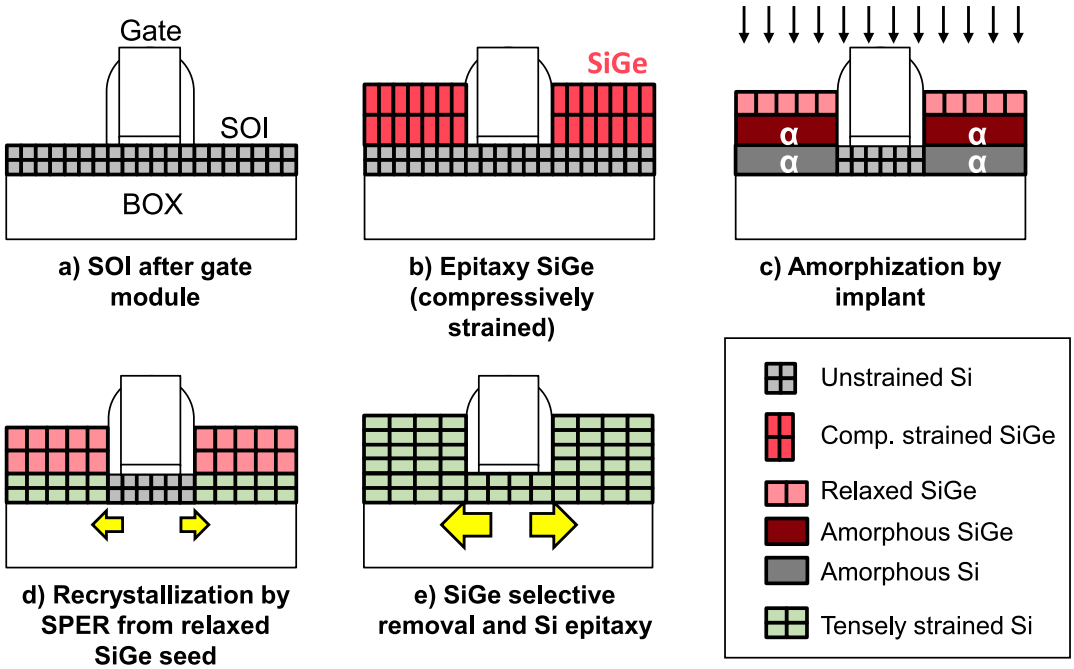

Figure C.37: Procédé de fabrication de la technique "SDRASS". a) dispositif SOI après formation de la grille et des espaceurs. b) Epitaxie de SiGe pseudomorphe dans la région des source/drain (30% Ge). c) Amorphisation par implantation Si (2.5 10^{14} cm^{-2} à 40keV sans tilt). Un germe de SiGe cristallin doit être maintenu à la surface. d) Recristallisation par épitaxie en phase solide (SPER). Le SOI recroit selon le paramètre de maille du germe SiGe. Une contrainte en tension est générée si le germe SiGe est relaxé. e) Retrait sélectif du SiGe et épitaxie des source/drain surelevés en Si. Cette dernière étape permet d'avoir un volume plus important de Si en tensions dans les source/drain et donc de favoriser la génération de contrainte dans le canal voisin.

Afin de maximiser la génération de contrainte dans le canal, le SiGe est sélectivement gravé et une épitaxie de Si est réalisée dans les source/drain. Le substrat étant le SOI recristallisé, le SOI dans cette région est en tension. La relaxation de l'énergie élastique dans les régions de source/drain va entrainer le canal en tension. Nous avons validé morphologiquement les étapes d'amorphisation et recristallisation à l'aide d'images TEM. Le canal n'est pas amorphisé lors de l'implantation et la recroissance à partir du germe SiGe s'effectue bien pour l'ensemble du SOI dans les régions de

source/drain.

Les performances électriques des dispositifs ainsi fabriqués ne montrent pas de gain évident par rapport à la référence. Cependant, une analyse fine nous a permis de mettre en évidence un gain en mobilité contrebalancé par une dégradation de l'EOT. De plus amples caractérisations sont requises pour confirmer la génération de contrainte tensile à l'aide de cette technique. Des mesures de déformation à l'échelle nanométrique (NBD, PED ou DFEH) seraient pertinentes.

C.5.2 Polarisation arrière dynamique en 3D séquentielle

Au delà de l'intégration de contrainte mécanique pour booster les performances, nous avons également étudié une force du FDSOI: la polarisation arrière. En particulier, nous avons étudié l'intérêt d'une polarisation arrière dynamique, rendue possible par une intégration 3D séquentielle.

C.5.2.a Principe et résultats de simulations

Avec une intégration 3D séquentielle, il est possible de dessiner une grille arrière locale pour un étage supérieur alors que la polarisation arrière de l'étage du bas s'effectue via un plan de masse. En connectant la grille arrière directement à la grille avant (avec un contact partagé), les dispositifs fonctionnent en régime de double-grille asymétrique. Nous avons évalué ce régime de fonctionnement à l'aide de simulations SPICE pour plusieurs layouts.

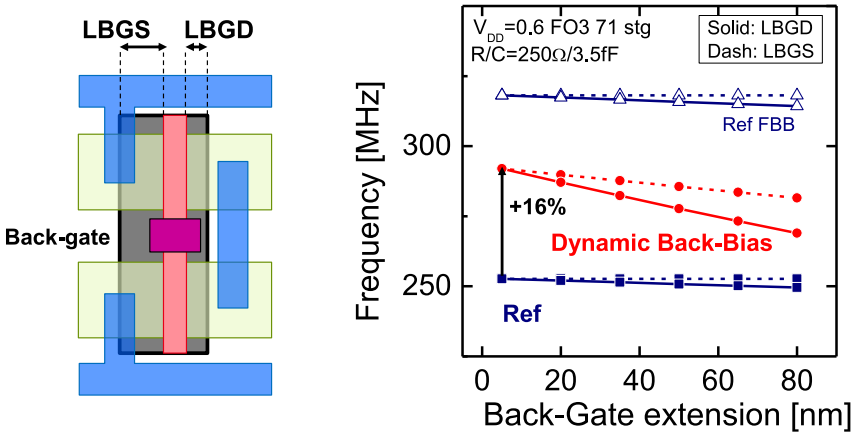

Figure C.38: (left) Layout of the 1-finger inverter with local back-gate. Definition of the back-gate extensions over front-gate on the source and drain sides, LBGS and LBGD, respectively. (right) Frequency as a function of the back-gate extensions. Under static bias, the back-gate extension does not significantly impact the performance. Under dynamic back-bias however, LBGS and particularly LBGD reductions enhance the frequency.

La Figure C.38 montre l'impact des paramètres d'extension de la grille arrière par rapport à la grille avant sur la fréquence d'un inverseur à un doigt de grille. Pour un minimum d'extension, la fréquence est améliorée de +16% par rapport au cas classique dans les conditions de référence. La fréquence n'atteint pas la performance du cas FBB mais la consommation statique reste identique à la référence, ce qui n'est pas le cas du FBB qui augmente fortement la fuite (décalage statique de la tension de seuil). Le gain provient de la réduction de la résistance effective malgré l'augmentation de la capacité effective (grille arrière). En réduisant les extensions latérales, la capacité effective est diminuée, ce qui permet d'améliorer la fréquence d'oscillation.

C.5.2.b Cellules SRAM avec grille arrière locale

En plus de la performance des portes logiques telles que l'inverseur, nous avons évalué l'intérêt d'une grille arrière locale pour les cellules SRAM. En connectant le transistor d'accès à la cellule (Pass-Gate PG) en mode double-grille, le courants d'écriture et de lecture sont respectivement améliorés de +30% et +19%, sans modifier la consommation de la cellule. Cependant, la stabilité en lecture est légèrement dégradée.

L'intérêt d'une grille arrière locale dans les cellules SRAM réside probablement plutôt dans des techniques d'assistance. Par exemple, la grille arrière peut constituer une ligne de mot supplémentaire, polarisée uniquement lors de l'écriture au sein de la cellule. Un gain de +34% sur le courant est prédit en appliquant 1V sur cette seconde ligne de mot lors d'une écriture.

C.5.2.c Conclusion

En résumé, la polarisation arrière constitue un atout majeur de technologie FDSOI. L'intégration 3D séquentielle peut permettre d'étendre la capacité de la polarisation arrière. Une polarisation dynamique permet d'améliorer significativement le compris performance/consommation des cellules logiques, à condition de pouvoir dessiner une grille arrière locale. Cette approche permet également d'améliorer la performance des cellules SRAM, que ce soit en régime de double grille ou à travers des techniques d'assistance.

C.6 Conclusion générale

La technologie CMOS comprenant la conception et la fabrication de circuits intégrés à base de transistors à effets de champ a connu une forte évolution sur la dernière décennie. Un meilleur contrôle électrostatique dans le canal a été rendu possible grâce à des architectures à film mince tel que le FDSOI et la performance peut être améliorée grâce à l'intégration de contrainte mécanique. Dans ce travail de thèse, nous avons étudié l'intégration de contraintes mécaniques en technologie FDSOI pour les noeuds 20nm et en deçà.

Dans un premier temps, nous avons démontré à travers une technique d'extraction innovante que la contrainte influe non seulement la mobilité des porteurs mais également la résistance d'accès des dispositifs. Ceci s'explique par le rôle important de la région sous l'espaceur dans la résistance totale du dispositif. Nous nous sommes ensuite focalisés sur les effets géométriques des transistors de type p à canal SiGe en technologie FDSOI 14nm. Nous avons étudié la relaxation latérale de la contrainte compressive des canaux SiGeOI à l'aide de caractérisations physiques (NBED, µRaman) et nous proposons un modèle empirique permettant de reproduire le comportement des dispositifs. Nous montrons que la relaxation de la contrainte dans le sens longitudinal est néfaste pour la performance des dispositifs car elle se traduit par une chute de la mobilité des trous. Nous avons proposé plusieurs solutions afin d'optimiser la performance des dispositifs contraints impactés par la relaxation latérale. En ce qui concerne les solutions de type "design", l'approche "Mix-VT" permet de recentrer les dispositifs mais n'évite pas la dégradation de performance associée à la chute de mobilité. L'approche de zone active continue "CRX" permet d'atteindre des performances optimales mais présente certains inconvénients tels que la variabilité associée à la juxtaposition des cellules standards. Pour ce qui est des solutions technologiques, le procédé "SiGe-last" permet de réduire la relaxation latérale mais cela ne se traduit pas systématiquement par un gain en performance. En revanche, une isolation duale par tranchées et oxydation ("DITO") permet d'obtenir la configuration de contrainte préférentielle. Enfin, nous nous intéressons à l'intégration de contrainte en tension. Nous avons montré que l'utilisation de substrat sSOI s'accompagne également d'effets géométriques, bien que ceux-ci soient moins prononcés que pour les canaux SiGeOI. Nous avons également investigué la technique de fluage de BOX ("BOX-creep") ainsi qu'une technique innovante basée sur la recroissance en phase solide de source/drain amorphisés. Pour cette dernière, des résultats morphologiques et électriques encourageants ont été obtenus, ouvrant la voie pour de futures améliorations. De plus, nous avons étudié l'intérêt de la polarisation en face arrière de façon dynamique dans une technologie 3D séquentielle. Nous avons montré qu'à travers une co-optimisation du design et de la technologie, une grille arrière locale permet d'améliorer la performance des cellules logiques et mémoire (SRAM).

En résumé, l'intégration de contrainte mécanique est un moyen efficace d'améliorer la performance des dispositifs et ce malgré l'apparition d'effets géométriques. Toutefois, la co-intégration de niveaux élevés de contrainte reste un défi majeur pour les technologies 10nm et en deçà. Néanmoins, la technologie FDSOI est pertinente pour les applications à faible consommation, en particulier grâce au potentiel de son extraordinaire efficacité de polarisation en face arrière.

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Patents

1. Berthelon, R. and F. Andrieu: 'Dual doping in standard cells with strained SiGe pMOSFET (application numbers: FR 1658731; US 15706935)'.

2. Berthelon, R. and F. Andrieu: 'Dual doping in standard cells with strained SOI nMOSFET (application numbers: FR 1658733; US 15706952)'.

3. Berthelon, R. and F. Andrieu: 'Standard cells with local back-gate in 3D monolithic (application number: FR 1761404)'.

4. Berthelon, R. and F. Andrieu: 'Stress cointegration in FDSOI (application number: FR 1754199)'.

5. Berthelon, R., F. Andrieu, D. Dutartre, E. Baylac, and P. Morin: 'Dual isolation for strained-channel MOSFETS with optimized performances (application numbers: FR 1563507; US 15387712)'.

Strain integration and performance optimization in sub-20nm FDSOI CMOS technology

Abstract
The Ultra-Thin Body and Buried oxide Fully Depleted Silicon On Insulator (UTBB FDSOI) CMOS technology has been demonstrated to be highly efficient for low power and low leakage applications such as mobile, internet of things or wearable. This is mainly due to the excellent electrostatics in the transistor and the successful integration of strained channel as a carrier mobility booster. This work explores scaling solutions of FDSOI for sub-20nm nodes, including innovative strain engineering, relying on material, device, process integration and circuit design layout studies. Thanks to mechanical simulations, physical characterizations and experimental integration of strained channels (sSOI, SiGe) and local stressors (nitride, oxide creeping, SiGe source/drain) into FDSOI CMOS transistors, we provide guidelines for technology and physical circuit design. In this PhD, we have in-depth studied the carrier transport in short devices, leading us to propose an original method to extract simultaneously the carrier mobility and the access resistance and to clearly evidence and extract the strain sensitivity of the access resistance, not only in FDSOI but also in strained nanowire transistors. Most of all, we evidence and model the patterning-induced SiGe strain relaxation, which is responsible for electrical Local Layout Effects (LLE) in advanced FDSOI transistors. Taking into account these geometrical effects observed at the nano-scale, we propose design and technology solutions to enhance Static Random Access Memory (SRAM) and digital standard cells performance and especially an original dual active isolation integration. Such a solution is not only stress-friendly but can also extend the powerful back-bias capability, which is a key differentiating feature of FDSOI. Eventually the 3D monolithic integration can also leverage planar Fully-Depleted devices by enabling dynamic back-bias owing to a Design/Technology Co-Optimization.

Key words: strain; stress; FDSOI; SiGe; Local Layout-Effects; Design/Technology Co-optimization; 3D monolithic

Intégration de contraintes mécaniques et optimisation des performances des technologies CMOS FDSOI pour les noeuds 20nm et en deçà

Résumé
La technologie CMOS à base de Silicium complètement déserté sur isolant (FDSOI) est considérée comme une option privilégiée pour les applications à faible consommation telles que les applications mobiles ou les objets connectés. Elle doit cela à son architecture garantissant un excellent comportement électrostatique des transistors ainsi qu'à l'intégration de canaux contraints améliorant la mobilité des porteurs. Ce travail de thèse explore des solutions innovantes en FDSOI pour nœuds 20nm et en deçà, comprenant l'ingénierie de la contrainte mécanique à travers des études sur les matériaux, les dispositifs, les procédés d'intégration et les dessins des circuits. Des simulations mécaniques, caractérisations physiques (µRaman), et intégrations expérimentales de canaux contraints (sSOI, SiGe) ou de procédés générant de la contrainte (nitrure, fluage de l'oxyde enterré) nous permettent d'apporter des recommandations pour la technologie et le dessin physique des transistors en FDSOI. Dans ce travail de thèse, nous avons étudié le transport dans les dispositifs à canal court, ce qui nous a amené à proposer une méthode originale pour extraire simultanément la mobilité des porteurs et la résistance d'accès. Nous mettons ainsi en évidence la sensibilité de la résistance d'accès à la contrainte que ce soit pour des transistors FDSOI ou nanofils. Nous mettons en évidence et modélisons la relaxation de la contrainte dans le SiGe apparaissant lors de la gravure des motifs et causant des effets géométriques (LLE) dans les technologies FDSOI avancées. Nous proposons des solutions de type dessin ainsi que des solutions technologiques afin d'améliorer la performance des cellules standard digitales et de mémoire vive statique (SRAM). En particulier, nous démontrons l'efficacité d'une isolation duale pour la gestion de la contrainte et l'extension de la capacité de polarisation arrière, qui un atout majeur de la technologie FDSOI. Enfin, la technologie 3D séquentielle rend possible la polarisation arrière en régime dynamique, à travers une co-optimisation dessin/technologie (DTCO).

Mots-clefs: déformation; contrainte; FDSOI; SiGe; effets géométriques; co-optimisation dessin/technologie; 3D séquentielle