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Bandwidth enhancement of three-device Doherty power amplifier based on symmetric devices

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Abstract: This paper proposes a method for extending the bandwidth of a three-device Doherty power amplifier (DPA) based on symmetric devices. $\lambda/4$ transmission lines are inserted between each peaking amplifier output and carrier amplifier output to compensate load impedance of carrier amplifier. In order to achieve perfect load modulation, carrier amplifier output circuit total electrical length is designed to 90 degrees, and the peak amplifier output total electrical length is designed to 180 degrees. The proposed method is demonstrated by designing a three-device broadband DPA using three 10-W packaged GaN HEMT devices. Measurement results show that over 40% drain efficiency is achieved at 9-dB back-off power, over the frequency band of 1.45–2.35 GHz, accounting for 46% fractional bandwidth.

Keywords: Doherty power amplifier, broadband, drain efficiency, three-device, symmetric devices

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Modern wireless communication networks usually apply complicated modulation schemes in order to increase data throughput in limited frequency bandwidth. Nevertheless, complex signals with high peak-to-average power ratios (PAPRs) and wide bandwidths are usually required. However, high PAPRs poses severe linearity constrains on the power amplifiers, forcing a large output back-off (OBO) power operation to ensure the acceptable linearity [1]. Unfortunately, this scenario makes traditional power amplifier very poor in efficiency, especially at large back-off power.

To improve efficiency at large OBO power level, Doherty power amplifiers (DPA) has been widely used due to its high efficiency at the reduced power condition [2, 3, 4, 5, 6, 7, 8]. To meet the increasing demand on information capacity, the signal modulation formats are becoming more and more complicated. In particular, the PAPR value is becoming even larger. Nevertheless, conventional two-ways DPAs can only provide roughly 6-dB OBO level. Therefore, in order to increase the back-off range, multi-way solutions have been proposed to improve efficiency at high back-off range in the literatures [9, 10, 11]. Among them, the three-way is the most feasible configuration because of its moderate complexity and adequate efforts. However, these structures are also limited by narrow bandwidths.

In this paper, a novel three-device Doherty power amplifier (DPA) with wide bandwidth based on symmetric devices is introduced. Section 2 presents the

theoretical analysis of the proposed three-devices structure. Section 3 discusses design process and simulation results of the prototype devised. Section 4 describes measurement results, followed by a conclusion.

2 Analysis of the proposed method for extending bandwidth

Conventional three-ways DPAs are implemented based on a load modulation network consisting of several $\lambda/4$ transmission lines to achieve anticipated load modulation [11]. For efficient amplification of modulated signals, effective load impedance of the carrier amplifier in the low-power region is $3Z_{opt}$. In fact, however, this condition is fulfilled only at center frequency (where Z_{opt} is optimum load impedance for amplifier and it is usually assumed $50\ \Omega$). When the operation frequency deviates from center frequency, the modulated impedance degrades quickly from $3Z_{opt}$. This impedance degradation will significantly impair the performance of three-way DPA in the low-power region [10]. As a consequence, bandwidth is deeply limited. Furthermore, a $\lambda/4$ transmission line can only do real impedance transformation. As the optimal transistor output impedance are generally a complex value, the conventional output combiner cannot realize the perfect load modulation. DPA also can not reach the optimal performance.

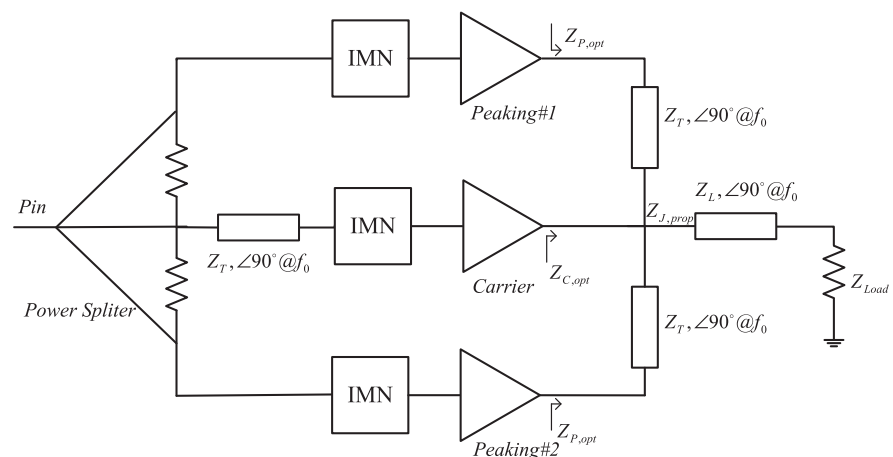


Fig. 1. Simplified schematic diagram of the proposed three-device broadband DPA

As shown in Fig. 1, elimination of the $\lambda/4$ transmission line on output of carrier amplifier in the conventional three-way Doherty amplifier reduces phase dispersion, and reducing the output impedance of the carrier amplifier with the frequency changes in order to achieve the purpose of stabilizing the output impedance of the carrier amplifier. Meanwhile, a $\lambda/4$ transmission line is inserted at each peak amplifier output to compensate the load impedance of the carrier amplifier, making the three-way Doherty power amplifier has a broader bandwidth capability.

Fig. 2(a) compares the simulated load impedance of the carrier PA versus normalized frequency for the conventional and proposed DPA in the low-power region. The load impedances of the conventional and proposed DPA are $3Z_{opt}$ and $Z_{opt}/3$ at the central frequency, respectively. Z_{opt} is assumed $50\ \Omega$. It is clear that both the real and imaginary parts of the proposed carrier load is kept close to a

constant value in a broad band. Fig. 2(b) shows the carrier and peaking load impedances versus normalized frequency of the two DPAs in the high-power region. It is obvious that real part of carrier load impedances of the proposed DPA tend to constant value over wide frequency range. While for a constant output impedance, the design of the broadband output matching network is simplified, so it is more suitable for broadband strategy design.

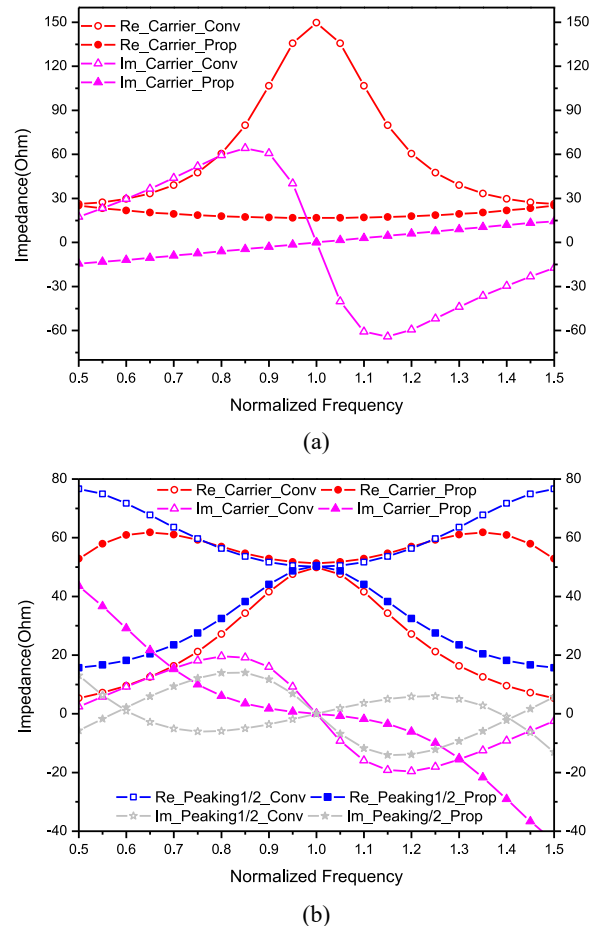


Fig. 2. Simulated carrier load impedance versus normalized frequency of the conventional and proposed DPA for: (a) carrier PA in the low-power region and (b) carrier and peaking PAs in the high-power region

For sake of simplicity, the sub-amplifiers are often assumed as ideal current sources with no parasitic parameters for theoretical analysis. Under these scenarios, $\lambda/4$ transmission lines are directly connected to the carrier and peak power amplifier outputs, and the impedance modulation occurs directly at the transistor's current generator plane. However, a practical power amplifier, parasitic inductance and capacitance are not negligible. In addition, the load impedance of the transistor generally has a lower impedance value, and it needs to be converted the impedance of the output port. Load modulation happens at the common point Z_J , and then output matching networks (OMN) provide the carrier and peak amplifiers with optimal impedances required. Fig. 3 shows the actual configuration of the proposed three-device DPA structure.

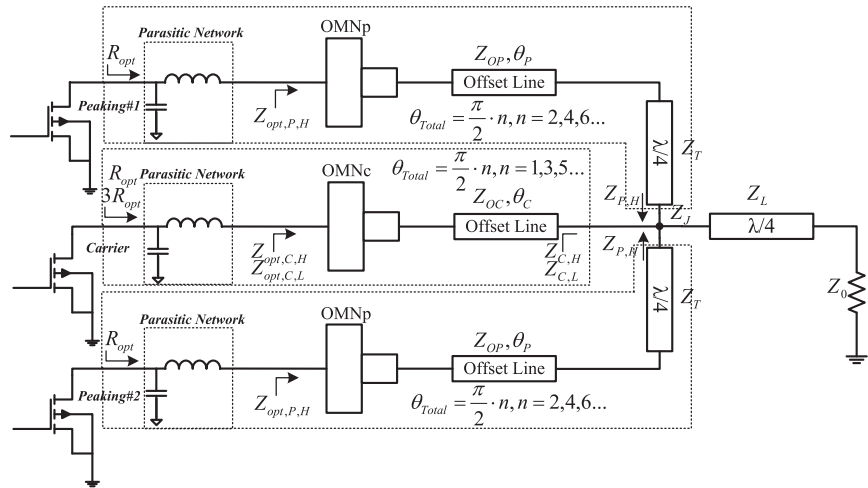


Fig. 3. The actual proposed three-device DPA topology

For the carrier amplifier, the OMN_C converts $Z_{C,H}$ to the optimal load impedance $Z_{opt,C,H}$ in the high-power region. And the load impedance of the transistor die (Current Generator Plane) is R_{opt} after taking the parasitic parameters of the transistor into consideration. $Z_{opt,C,H}$ can be obtained from load-pull technique. In the low-power region, the peaking amplifier is turned off, and the OMN_C will match $Z_{C,L}$ to $Z_{opt,C,L}$, which is a value described by a constant VSWR circle as the circle center, as shown in Fig. 4. The specific position is determined by the phase of OMN_C's scattering parameter S₂₁. In other words, it is necessary to add an offset line with proper electrical length θ_C to the output of the OMN_C to make the load impedance reach $3R_{opt}$, which finally ensures large output power and high efficiency of the DPA. The characteristic impedance Z_{OC} of the offset line is generally set to $Z_{C,H}$ to keep the impedance matching intact in the high-power region. For the peaking amplifiers, an offset line must be added after its output matching network OMN_P to convert the output impedance to the high impedance region, thereby reducing power leak, and to ensure that the DPA back-off efficiency and power.

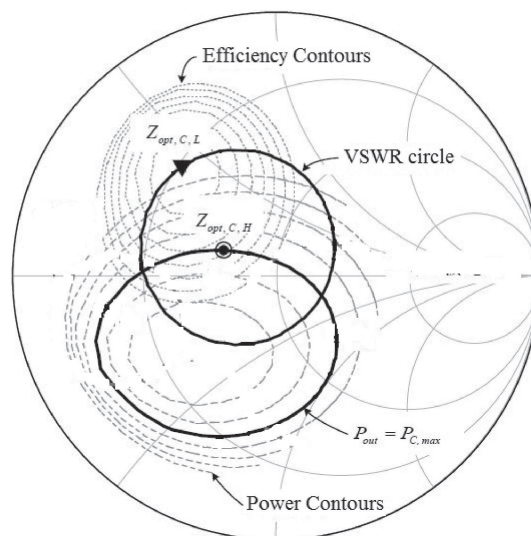


Fig. 4. Operation principle of the output of the carrier amplifier

In the conventional Doherty power amplifier design, the output of the carrier amplifier generally has a $\lambda/4$ transmission line that operates like an impedance inverter to achieve load modulation. While the $\lambda/4$ transmission line is eliminated in the proposed DPA topology. An impedance inverter may have an electrical phase shift of 90° or its odd multiple of it. And any matching network have this property in the frequency band of operation may operate as an impedance inverter. Therefore, the total electrical length of the output network (including the transistor parasitic network, the output matching network and the offset line) of the carrier amplifier must be an odd multiple of 90° to achieve proper load modulation. The peaking amplifiers is turned off in the low-power region, whose impedance is large if seen at the internal current plane. To prevent undesired reverse power leakage and efficiency degradation, the peaking impedance presented at the common junction point must be high enough. According to classical impedance transformation theory [9], the total electrical length of the output network of the peaking amplifier must be a multiple of 180° , keep large impedance condition intact after the introduction of matching network. This is often realized by adding an offset line with an appropriate length. In sum, the total electrical length of the output matching network of the carrier amplifier $\theta_{C,Total}$ and the peak amplifier $\theta_{P,Total}$ is

$$\theta_{C,Total} = \frac{\pi}{2} \cdot n, n = 1, 3, 5 \dots \quad (1)$$

$$\theta_{P,Total} = \frac{\pi}{2} \cdot n, n = 2, 4, 6 \dots \quad (2)$$

3 Design and simulation

In this paper, a novel three-device DPA based on the aforementioned strategy is designed using three identical 10-W Cree CGH40010F GaN HEMT devices, to verify the proposed bandwidth enhancement method. ADS Simulations are conducted based on the model provided by the supplier. The carrier amplifier is biased at $V_{GS} = -2.7\text{ V}$ and $V_{DS} = 28\text{ V}$, corresponding to class-AB mode. On the other hand, the two peaking amplifiers are biased at $V_{GS} = -5.5\text{ V}$ and $V_{DS} = 32\text{ V}$, corresponding to the class-C mode. The design uses asymmetrical power supplies that make the output currents of sub-amplifiers equal at saturation. It should be emphasized that a precise large-signal model of the selected device is required to conduct valuable simulations. A reliable model containing the parasitic network that reported in [13] is used, as shown in Fig. 5.

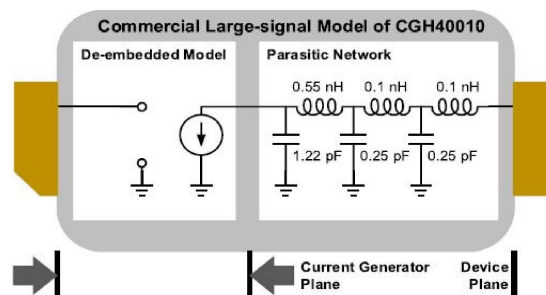


Fig. 5. A commercial large-signal model of Cree CGH40010F

In order to achieve the desired behavior in the proposed design, the OMNs of the carrier and peaking amplifiers must be properly designed. In the conventional carrier amplifier OMN_C design, $Z_{C,H}$ is usually matched to $Z_{opt,C,H}$, and then an offset line is added to the behind OMN_C. And $Z_{C,L}$ is matched to the impedance that make the carrier amplifier achieve higher efficiency in the back-off power by carefully setting the electrical length and characteristic impedance of the offset line. When $Z_{opt,C,H}$ and $Z_{opt,C,L}$ are both determined, the output matching network and the offset line can be designed together. These two elements are judiciously designed as a whole to make the overall structure compact in size and small in electrical length. This helps to facilitate the output matching network for broadband design, enhancing the operating bandwidth of the Doherty power amplifier. The parameters of the output part of the carrier amplifier in this particular design is shown in Fig. 6. $Z_{opt,C,H}$ and $Z_{opt,C,L}$ are load impedances of the carrier's transistor at saturation and back-off obtained by load-pull, respectively. A very simple stepped impedance configuration is used to fulfill the function of impedance matching and phase adjustment.

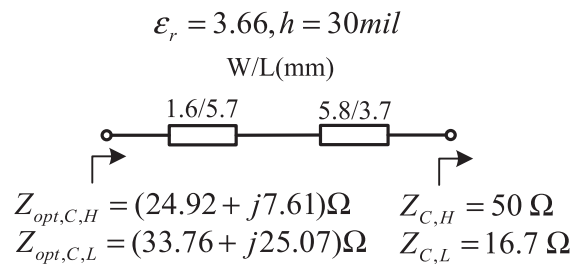


Fig. 6. The optimized carrier amplifier output matching network

Similarly, the longer length of the offset line in the peaking amplifier, the more limitation to the bandwidth of the Doherty PA. To reduce bandwidth constraints of the peaking offset line, the peaking offset line is optimized with a shortest electrical length. The optimized peaking amplifier output matching network parameters shown in Fig. 7. The peaking output network can match $Z_{P,H}$ to $Z_{opt,P,H}$, while the output impedance can be converted to a impedance larger than 500Ω in the low-power region. Therefore, it can effectively reduce the power leakage in the low-power region. $Z_{opt,P,H}$ is peaking's load impedance of transistors obtained by load-pull.

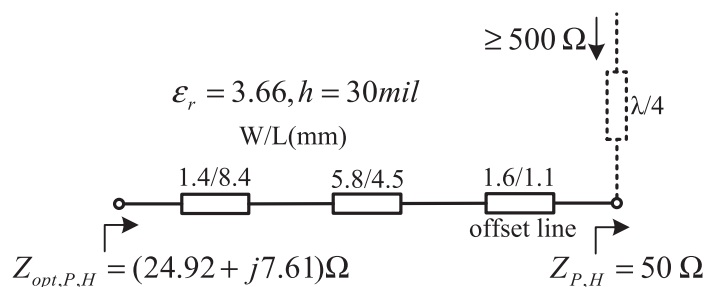


Fig. 7. The optimized peaking amplifier output matching network

The final completed schematic of the proposed three-device DPA is shown in Fig. 8. A wideband three-way equal power splitter is designed to systematically enhance the bandwidth. Fig. 9 shows the simulated drain efficiency and output power of the proposed three-device DPA versus frequency. It can be observed that the saturated power is around 45 dBm, and the drain efficiency is more than 56% over the entire frequency range from 1.45 to 2.35 GHz. The minimum drain efficiency values within the entire absolute frequency band of 900 MHz are 42% and 41% at 6- and 9-dB back-off powers, respectively.

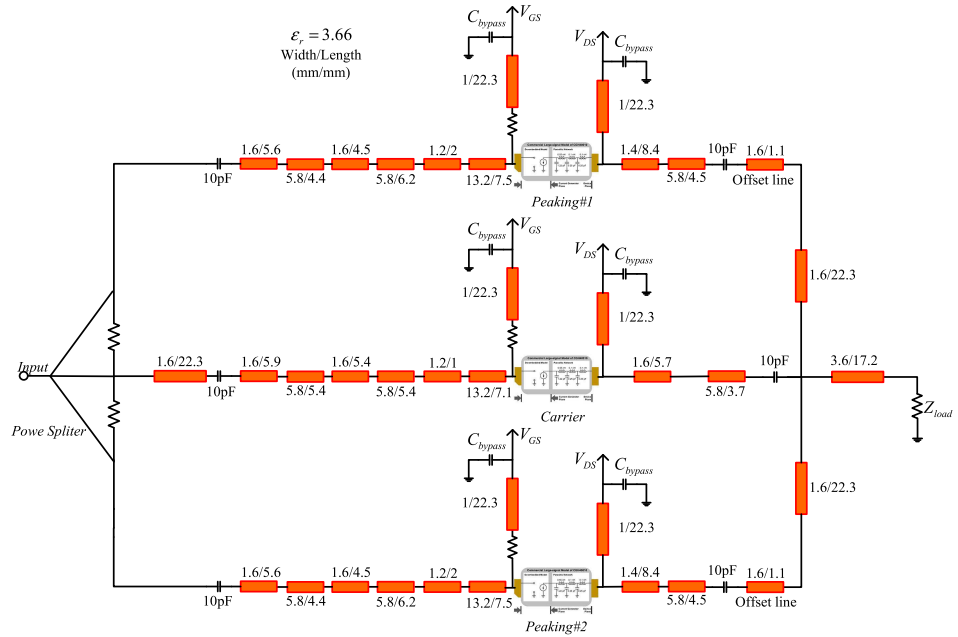


Fig. 8. Complete schematic of the proposed three-device DPA

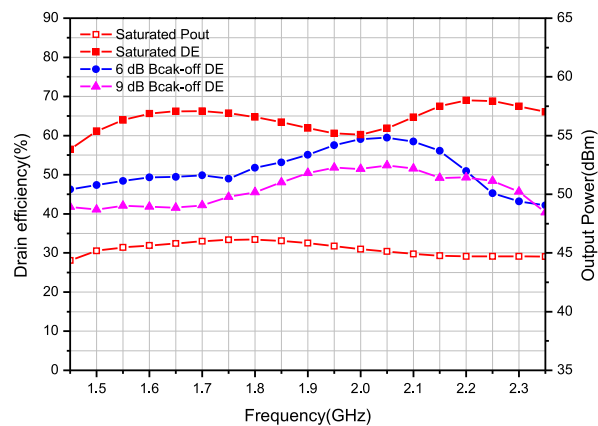


Fig. 9. Simulated drain efficiencies and saturated output power of the proposed three-device DPA versus frequency

4 Implementation and measurement results

In order to further validate the proposed design strategy, a broadband three-device DPA is implemented using three Cree 10-W GaN HEMTs CGH40010F on a Rogers RO4350B substrate of thickness 30 mils, dielectric constant of 3.48. To

achieve good heat dissipation, grounding performance and suppressing the thermal memory effect, the circuit board and transistor is welded to the copper substrate by the solder paste. The photograph of the fabricated broadband three-device DPA is shown in Fig. 10.

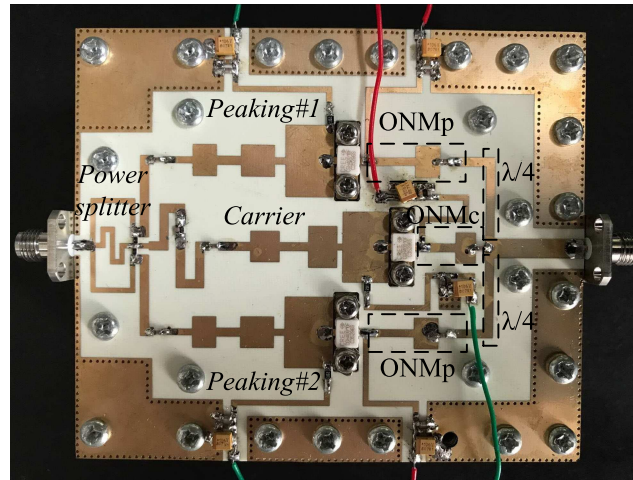


Fig. 10. Photograph of the fabricated circuit

Fig. 11 gives the measurement results under continuous wave (CW) signal in terms of output powers, drain efficiencies and gains at saturation in the frequency band from 1.45 to 2.35 GHz. As can be seen, the proposed DPA achieves a drain efficiency of 58–70%, output powers of 44.3–46.8 dBm, at saturation. The saturated gains are more than 8 dB. In addition, higher than 40% efficiency is obtained at 9-dB back-off power over the 900 MHz band, accounting for 46% fractional bandwidth. The measurement results are consistent with the simulation results. These mean that the simulated model and characteristics of the practical transistor are in good agreement. The simulation load-pull values $Z_{opt,C,H}$, $Z_{opt,C,L}$ and $Z_{opt,P,H}$ are close to load impedances by the designed circuit, respectively. The measured drain efficiency profiles versus the output power at different frequency points are depicted in Fig. 12. It can be clear observed that the proposed three-device DPA

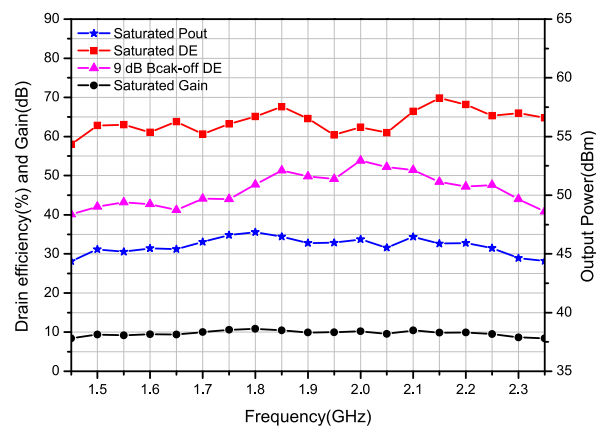


Fig. 11. Measured drain efficiencies, gains, and saturated powers of the proposed three-device DPA versus frequency

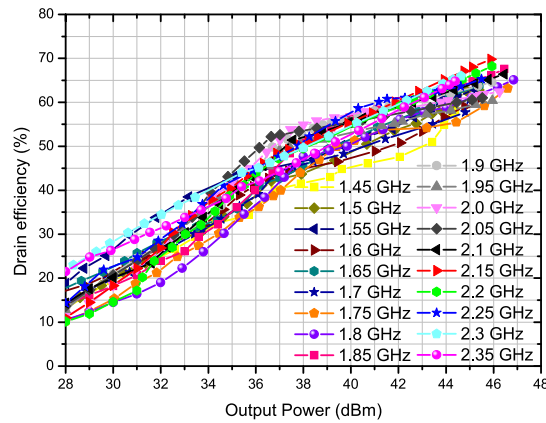


Fig. 12. Measured drain efficiency profiles versus the output power.

Table I. Performance comparison of broadband Doherty PAs

Ref	Frequency (GHz)	Bandwidth (%)	DE@ saturation	DE@ back-off	Pout (dBm)
[10]	0.73–0.98	29	43–67	49–64 @9 dB	42.7–44.6
[11]	0.7–0.95	30.3	60–78	50–67 @9.5 dB	42.9–44.7
[12]	2–2.6	26	53–76	≥40 @8 dB	43.6–45.4
This Work	1.45–2.35	46	58–70	40–54 @9 dB	44.3–46.8

approximately follows the classic Doherty type efficiency profiles at all the frequencies. Table I lists the comparison of some published broadband three-device DPA performance and this work.

5 Conclusion

A method for bandwidth enhancement of three-device DPA based on symmetric devices has been proposed in this work. A $\lambda/4$ transmission line is inserted at each peak amplifier output to compensate the load impedance of the carrier amplifier. For demonstration, a DPA prototype was fabricated based on the proposed configuration, and 46% fractional bandwidth has been achieved with drain efficiency higher than 40% at 9-dB back-off power.

Acknowledgments

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