Bridging the Gap Between Nanowires and Josephson Junctions: A Superconducting Device Based on Controlled Fluxon Transfer

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The basis for superconducting electronics can broadly be divided between two technologies: the Josephson junction and the superconducting nanowire. While the Josephson junction (JJ) remains the dominant technology due to its high speed and low power dissipation, recently proposed nanowire devices offer improvements such as gain, high fanout, and compatibility with CMOS circuits. Despite these benefits, nanowire-based electronics have largely been limited to binary operations, with devices switching between the superconducting state and a high-impedance resistive state dominated by uncontrolled hotspot dynamics. Unlike the JJ, they cannot increment an output through successive switching and their operation speeds are limited by their slow thermal-reset times. Thus, there is a need for an intermediate device with the interfacing capabilities of a nanowire but a faster, moderated response allowing for modulation of the output. We present a nanowire device based on controlled fluxon transport. We show that the device is capable of responding proportionally to the strength of its input, unlike other nanowire technologies. The device can be operated to produce a multilevel output with distinguishable states, the number of which can be tuned by circuit parameters. Agreement between experimental results and electrothermal circuit simulations demonstrates that the device is classical and may be readily engineered for applications including use as a multilevel memory.

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I. INTRODUCTION

Superconducting devices have played critical roles in technologies such as quantum computing [1], astronomical imaging [2–4], magnetometry [5,6], and digital logic [7–10]. Past superconducting electronics have largely been based on the Josephson junction (JJ) due to its desirable characteristics such as rapid operation speeds >100 GHz and power dissipation on the order of 10^{-19} J per switch [11]. Recently, however, superconducting nanowires have emerged as an alternative platform for new electronics. Unlike JJs, superconducting nanowires are dominated by thermal dissipation and a loss of phase coherence, switching from a superconducting state to a high-impedance resistive state when triggered by an external signal, such as a photon or current pulse. This functionality has enabled nanowires to be used in applications where JJs fall short—for instance, the nanocryotron (nTron) is a three-terminal comparatorlike nanowire device that can support high impedances and large fanout [12], whereas JJs lack intrinsic device gain and compatibility with high-impedance environments. The nTron can also be triggered by single flux quantum (SFQ) pulses to interface between JJs and CMOS circuits [13,14], demonstrating that nanowire electronics have a unique place in computing architectures. Other advantages of nanowires, including their single-layer fabrication, high-output voltages, and scalability, have prompted the development of new devices for use in readout, memory, and sensing.

Despite the growth of nanowire electronics, further advancement into new applications is currently hindered by characteristics that are inherent to nanowires. By switching from the superconducting domain to the resistive domain in response to an external input, nanowires are limited to operations of two states, with the resistive state expelling nearly all current from the high-impedance hotspot and generating a single large output. For the nTron, in which an input gate current triggers the growth of a high-impedance normal domain in the channel, this means that the output voltage is fixed and is only dependent on the gate current exceeding a critical threshold. Similarly, a recently reported superconducting nanowire memory based on persistent current was limited to binary operations of either "0," no current stored in the superconducting loop, or "1," a maximum amount of current stored in the loop [15]. By breaking coherence, hotspot

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formation also prevents incrementation of the output by successive device switching, as can be done with JJs. Another disadvantage of nanowire devices is that the operation speeds are slow due to the long thermal healing time of the resistive domain, which is often made slower by the electrical time constants of the biasing circuit.

These limitations leave a gap in the family of superconducting electronics for a device that offers the robust interfacing capabilities of a traditional nanowire, but with a more moderated response that allows for modulation of the output, analogous (but not identical) to incrementing in a JJ. Past approaches to creating such a device have focused on Dayem bridge weak links [16,17], where the dimensions of a nanowire in relation to the material's coherence length allow for preservation of phase coherence over a temporary phase-slip center. However, there have been very few experimental demonstrations of these devices in real circuit operations, and the primary goal has largely been to achieve true Josephson behavior in a nanowire rather than to demonstrate a device with the intermediate characteristics of both technologies.

Here, we report on a superconducting-nanowire device based on thermal principles that demonstrates a controlled output. Unlike other nanowire technologies, the device responds proportionally to the magnitude of an input signal and can be operated to achieve multiple discrete states. By using local resistive shunting and a high-inductance superconducting loop, we are able modulate the expulsion of current in an ultranarrow superconducting constriction and to controllably trap flux [18] in quantities of $n\Phi_0$, where n is an integer less than 10, and Φ_0 is the magnetic flux quantum. We experimentally show that the amount of flux per event n is dictated by circuit parameters and validate these results with electrothermal simulations. The results show that the device may be designed to achieve different $n\Phi_0$ outputs depending on the desired application. We anticipate that this device will serve as a foundation for new nanowire technologies such as a multilevel memory or multilevel-logic-circuit elements.

II. METHODS

A. Device fabrication

The devices presented in this work are fabricated using a multistep lithography process. The shunt resistors and alignment marks are first patterned using electron-beam lithography (Elionix F125). A bilayer resist process is employed by first spinning the polymethyl methacrylate (PMMA) copolymer EL6 (6% in ethyl lactate) at 5 krpm for 60 s, then spinning the positive-tone resist gL2000 (Gluon Lab LLC) at 6 krpm for 60 s. The resist is developed in o-xylene and MIBK:IPA in a 1:3 ratio. A 10-nm Ti + 25-nm Au metal bilayer is evaporated, and lift off is achieved in N-Methyl-2-pyrrolidone (NMP) heated to 60 °C for 1 h. An approximately 20-nm-thick NbN film is then deposited in an AJA sputtering system following the procedure described in Ref. [19]. The resulting sheet resistance is 150 Ω/sq and the critical temperature is 8.5 K. The nanowire structures are then patterned with electron-beam lithography using gL2000, followed by cold development in o-xylene at 5 °C and reactive ion etching in CF_4 (Plasmatherm, rf power of 50 W, chamber pressure of 10 mTorr). The structure is imaged using a scanning electron microcrope (Zeiss) to check for proper alignment. The full process flow may be found in the Supplemental Material [20].

B. Experimental setup

All measurements are performed with the devices submerged in liquid helium at 4.2 K. The devices are adhered to a printed circuit board (PCB), and electrical connections between the devices and gold PCB pads are made using aluminum wire bonds. The PCB ports are connected to room-temperature electronics outside of the liquid helium dewar through CMP cables. Current-voltage characteristics are measured by applying a sinusoidal bias current from an arbitrary waveform generator (Agilent AWG33622A) at a sweep frequency of 10–20 Hz with a 10-kΩ series resistor. The dc output voltage is read by a 2-GHz, real-time oscilloscope (LeCroy 620Zi) after amplification through a low-noise preamplifier (Stanford Research Systems SRS560). The switching current of the readout device (the yTron) is measured by applying a voltage pulse through a 30-dB attenuator to the device and measuring the skew between the oscilloscope trigger rising edge and the time at which a voltage output from the yTron is recorded, signifying a switching event. The bias pulse has a frequency of 500 Hz, width of 650 μs, rising edge of 400 μs, and height of 560 mV. The yTron output is sent through a pulse splitter and a low-noise amplifier (RF Bay LNA-2000, bandwidth: 10 kHz–2000 MHz, gain: 26 dB) before being read by the oscilloscope. The skew is then converted to units of switching current based on the slope of the bias waveform. To apply a dc bias to the constriction, a dc battery source (Stanford Research Systems SIM928) is connected to the constriction through a 100-kΩ series resistor and a dc 1.9-MHz coaxial low-pass filter (MiniCircuits). To apply a pulse to the constriction, a pulsed-voltage waveform of widths ranging from 5 ns to 100 μs and heights ranging from 50 to 550 mV is sent to the constriction input through a 30-dB attenuator. Details of the complete measurement setup may be found in the Supplemental Material [20].

C. Simulation details

The circuit simulator employed in this work uses a superconducting nanowire model implemented in MATLAB that includes thermoelectric dynamics of hotspot formation and decay [21]. Physical parameters for the material stack are derived from prior literature [22] and

are adjusted to match the experimental results. Flux quantization in the superconducting loop is enforced following each transient, which is found to be sufficient in explaining behavior in the absence of coherent transport events.

III. RESULTS AND DISCUSSION

A. Device characterization

Figure 1 summarizes the device architecture and its basic characteristics. The device is comprised of three superconducting nanowire elements: a narrow 60-nm-wide constriction, a storage loop, and a nanoscale readout tool known as the yTron [23]. All three elements are fabricated together on an approximately 20-nm-thick niobium nitride (NbN) film on a silicon oxide substrate using electron-beam lithography. In addition to the nanowire components, a resistive metal shunt is patterned in parallel with the constriction to reduce Joule heating and provide damping, similar to the purpose served in resistively shunted JJs. Initial efforts to fabricate the resistor on top of the NbN film failed due to contact resistance, requiring us to place the resistor layer beneath the NbN film, as was done in similar work on Nb nanowires [24]. Previous attempts to shunt nanowires have found that series inductance between the shunt and the constriction plays a critical role in the effectiveness of the damping; high series inductance produces relaxation oscillations, while increasing the inductance even further makes the resistor completely ineffective [25]. To reduce this effect, the shunt is patterned as close to the constriction as possible and the leads are made wide to reduce the number of squares of material.

A simple circuit model for the device is shown in Fig. 1(b). To trap flux in the loop, a bias write current I_{write} is inductively split to the nanowire in the amount of αI_{write}, where $\alpha = L_{\text{loop}}/(L_{\text{constriction}} + L_{\text{loop}})$. In this case, $L_{\text{constriction}} = 284$ pH and $L_{\text{loop}} = 1.87$ nH, leading to $\alpha = 0.87$. Once the sum of αI_{write} and any existing current circulating in the loop surpasses the critical current of the constriction, the nanowire switches and the bias current is diverted away from the constriction to the shunt resistor and the righthand side of the loop. By shunting the majority of the bias current, the resistor allows the nanowire to recover the superconducting state more quickly and limits the amount of current that charges L_{loop}, thus controlling the amount of flux that is trapped once the constriction heals. After the constriction heals, a persistent current circulates in the superconducting loop in quantized units of $n\Phi_0/L$, where n is an integer, Φ_0 is the magnetic flux quantum, and L is the total loop inductance. Since the geometric inductance of this device is <0.33 fH, the total loop inductance is dominated by the kinetic inductance of the superconducting nanowires. In this device, persistent current is estimated to be quantized as approximately 0.95 μA/fluxon.

The amount of circulating current in the loop can be nondestructively read out using the yTron. As described by McCaughan *et al.* [23], the yTron is a three-terminal nanoscale device with two adjoining arms whose switching currents depend on one another as a result of current crowding around the intersection point. In our device, the left arm of the yTron forms part of the superconducting loop so that the switching current of the right arm

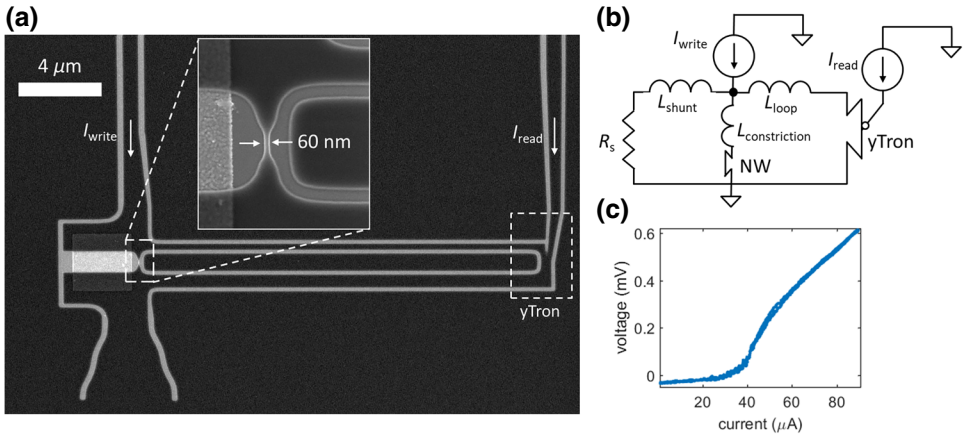

FIG. 1. Device design and characterization. (a) Scanning electron micrograph of the device. The dark area is the NbN film, while the light outlines are the underlying substrate. The inset shows an enlarged view of the 60-nm-wide constriction in parallel with the resistive shunt. The shunt dimensions are 1×3 μm^2. The righthand side of the loop is connected to a yTron with arm widths equal to 300 nm. (b) Circuit representation of the device. In this particular design, $R_s = 5$ Ω, $L_{\text{shunt}} = 50$ pH, $L_{\text{constriction}} = 284$ pH, and $L_{\text{loop}} = 1.87$ nH. I_{write} is the bias current that switches the nanowire constriction (NW) and changes the state of the loop. I_{read} is the bias current applied to the right arm of the yTron in order to sense the amount of circulating current in the loop. (c) Current-voltage characteristics of an isolated shunted nanowire of width = 60 nm, $R_s = 5$ Ω. The absence of hysteresis implies that Joule heating through the nanowire has been significantly reduced by the presence of a shunt resistor. Comparison to the characteristics of an unshunted nanowire may be found in the Supplemental Material [20].

I_{switch} is a function of the amount of circulating current—a higher circulating current in the clockwise direction flowing through the yTron's left arm will result in a higher switching current in the yTron's right arm. Since the two arms of the yTron are electrically disconnected from one another, switching the right arm does not break superconductivity in the left. As a result, the state of the loop is undisturbed by the reading process in which I_{switch} is measured by applying a bias current I_{read} to the yTron's right arm until it switches and generates a voltage, allowing us to nondestructively sense the amount of circulating current in the loop.

Figure 1(c) shows the current-voltage characteristics of an isolated shunted nanowire patterned alongside the device with dimensions identical to those of the constriction. The absence of hysteresis, as shown by the lack of separation between the switching and retrapping currents, indicates that the shunt resistor is able to reduce Joule heating through the constriction by effectively diverting the bias current, thereby reducing power dissipation in the nanowire and allowing it to regain the superconducting state more quickly [26]. Observation of the amplified rf output of the device within a bandwidth of 2 GHz does not reveal any relaxation oscillations, suggesting that the shunt inductance is low enough to prevent stable relaxation oscillations at least within the limits of our measurement capabilities [25].

B. Demonstration of controlled dynamics

Figure 2 shows the response of the device to an input voltage pulse of varying amplitude and width; the response is compared to that of an otherwise identical device lacking a resistive shunt. For these measurements, an input voltage of widths ranging from 5 ns to 100 μs and heights ranging from 50 to 550 mV is sent to the constriction through a -30 dB attenuator. The change in the amount of stored current in the loop is inferred by measuring the switching current of the yTron readout arm. Before each positive input pulse, a large negative pulse (width $= 10$ μs, height $= -1.3$ V) is sent to the constriction to reset the superconducting loop.

As shown in Fig. 2(a), the amount of stored current in the unshunted device sharply increases with increasing input voltage, but then abruptly drops off, suggesting instability. This response was also observed in the device reported in Ref. [27], and was speculated to be due to overheating of the constriction, causing flux to be lost. In contrast, the response of the shunted device in Fig. 2(b) shows that the amount of flux stored in the loop increases proportionally with input voltage. Unlike the unshunted constriction, in the shunted device there was no sudden loss of stored flux or signatures of unstable oscillations, implying that heating in the constriction is moderated by the presence of the resistive shunt.

To demonstrate the flux-shuttling capabilities of the shunted device, we measure its dependence on the previously written state by ramping a dc bias current on the constriction without resetting the loop and recording the switching current of the yTron at every bias point. As shown in Fig. 3(a), ramping the bias current to the constriction produces either increasing or decreasing steps in the switching current output of the yTron, signifying a sudden addition or subtraction in the amount of trapped flux.

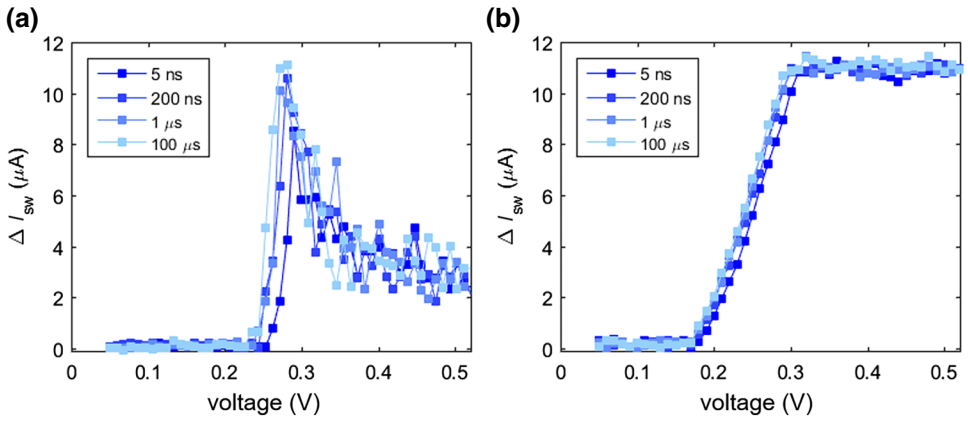

FIG. 2. Response to the voltage and pulse width of the write input. (a) Switching current of the right yTron arm as a function of the input write voltage for a superconducting loop with an unshunted constriction. The input pulse widths range from 5 ns to 100 μs. The switching currents are plotted in terms of $\Delta I_{sw} = I_{sw} - I_{sw}(v = 0)$, where v is the voltage height of the input pulse. The decrease in ΔI_{sw} suggests that some flux has been lost in the loop at high input voltages, potentially due to overheating of the constriction. Each point represents the mean of 10 sequential measurements of the yTron switching current. (b) Results from the same measurement repeated on a superconducting loop with a shunted constriction, $R_s = 5$ Ω. The proportional increase in switching current with increasing input voltage implies that the dynamics of the constriction are controlled by the presence of the shunt resistor. Logarithmic colormaps showing the complete range of input pulse widths and voltages for both devices may be found in the Supplemental Material (see Fig. S7) [20].

The horizontal lines in Fig. 3(a) show that the steps can be categorized into seven distinguishable states, revealing that successive switching of the constriction produces controlled, incremental changes in the amount of circulating current in the loop, rather than storing the maximum amount of current every time. The slight variation in the position of the seven states occurs due to instability in the plateaus, representing when the loop current is nearly maximized (approximately $|I_{c,\mathrm{NW}}|$) and may have lost a small amount of flux (1–$2\Phi_0$) to achieve stability. Despite the small shifts at the plateaus, the seven states have well-separated mean values including consideration of their standard deviations (see Fig. S8 within the Supplemental Material [20]). In contrast, Fig. 3(b) displays the results from repeating the measurement on an unshunted device of the same geometry. In this case, no intermediate states are observed, and the loop traps nearly its maximum amount of circulating current whenever the nanowire switches. Thus, it is not possible to achieve distinguishable intermediate states without the presence of a resistive shunt.

While the yTron is an effective tool for sensing when there is a change in circulating current, it can be imprecise for extracting the exact amount of circulating current in the loop. Depending on the geometry of the yTron, there may be a nonlinear relationship between the amount of circulating current and the induced change in switching current (see Fig. S6 within the Supplemental Material [20]). Additionally, the sensitivity of the yTron depends on the intersection point between its two arms, which has a radius of curvature <5 nm, leaving room for fabrication variability and thus differences in sensitivity between yTrons of identical design.

To bypass this shortcoming, we use the yTron only to sense when a change in trapped flux occurs and examine the corresponding bias current at each of the points of change in order to infer the magnitude of the loop current. Figure 3(c) shows the bias current at each of the first 14 steps of the plot in Fig. 3(a). The bias current at each step can be used to estimate the amount of circulating current remaining in the loop, given that the transition occurs when the nanowire switches, or when $|\alpha I_{\mathrm{write}} + I_{\mathrm{loop}}| > |I_{c,\mathrm{NW}}|$. The average zero flux state ($I_{\mathrm{loop}} \approx 0$) occurs at $I_{c,\mathrm{NW}} \approx 20.48 \pm 1.45\ \mu$A over a set of eight bias ramps. While the seven levels in the yTron switching current of Fig. 3(a) are spaced unevenly, the steps in terms of bias current occur at nearly equal intervals of approximately 5 μA, or roughly 5 Φ_0 of circulating current. As a result, it is possible to infer that the loop gains or loses aproximately 5 Φ_0 of trapped flux every time the constriction switches. Repeating this measurement over eight ramping cycles with a finer sweep produces an average of 4.77 Φ_0 per step in circulating current, with variation from an integer amount ($n \approx 5$) expected to be caused by noise in the measurement setup. A discussion of the experimental noise may be found in the Supplemental Material [20].

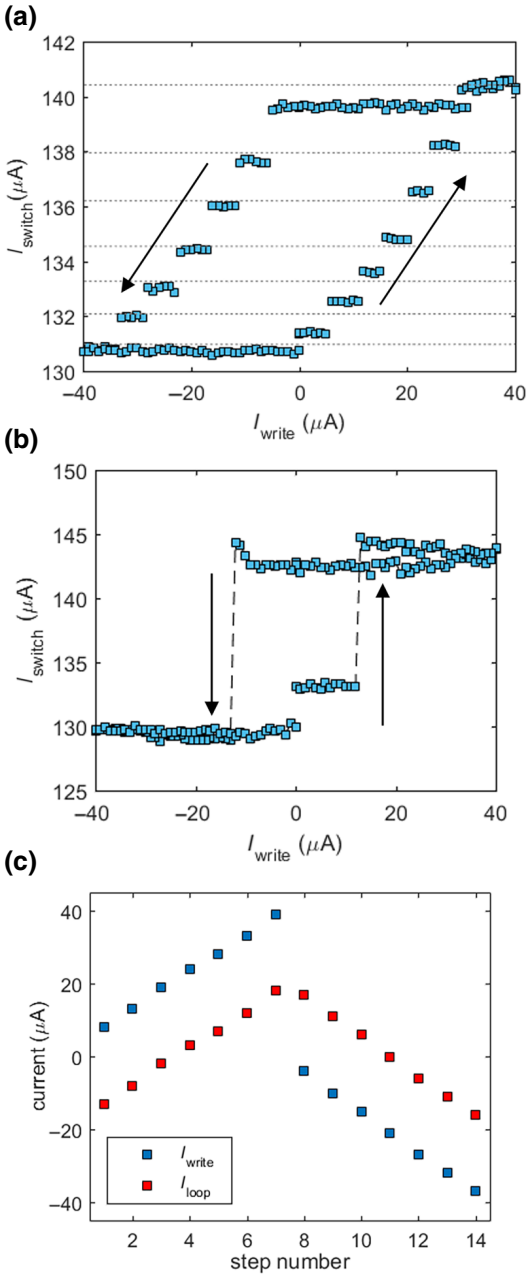

FIG. 3. Demonstration of controlled flux shuttling. (a) Switching current of the right arm of the yTron on the shunted device in response to a dc bias ramp of $\pm 40\ \mu$A applied to I_{write} of the constriction. Each point is the mean of 10 measurements of the yTron switching current. Each bias current step in I_{write} is applied to the constriction for 100 ms before being turned off during the reading operation. (b) Repetition of the same measurement on a device with an unshunted constriction. In comparison to the shunted device, no repeatable intermediate states are observed, and nearly the maximum amount of current is trapped every time the constriction switches. (c) Blue squares represent I_{write} at the initial point of each of the first 14 steps of the yTron switching current in (a). The approximate circulating loop current I_{loop} (red squares) is also calculated using $I_c = 21\ \mu$A. The data shows that the amount of circulating loop current can be incremented in nearly even steps of approximately 5 μA.

TABLE I. Mean change in circulating current per switching event, represented in terms of flux.

Device	L_{loop}	R_s	No. of states	μ	σ
Device 1	1.87 nH	5 Ω	7	4.77 Φ_0	1.23 Φ_0
Device 2	1.87 nH	7.8 Ω	5	7.63 Φ_0	1.5 Φ_0
Device 3	0.66 nH	7.8 Ω	3	5.87 Φ_0	1.02 Φ_0

Thus, despite the nonlinear response of the yTron, movement of a controlled $n\Phi_0$ of flux per step can be validated by examining the bias current at which each of the steps occurs.

Table I summarizes the results of repeating this measurement on two other devices with varying circuit parameters. Device 2 has $R_s = 7.8\ \Omega$ and $L_{loop} = 1.87$ nH, and Device 3 has $R_s = 7.8\ \Omega$ and $L_{loop} = 0.66$ nH. All other geometries and parameters are kept the same. For each device, the bias write current I_{write} is ramped to $\pm 40\ \mu$A as before in increments of about 10% of the amount of current per fluxoid, or $0.1\Phi_0 L$, where L is the total inductance of the loop. For $L_{loop} = 1.87$ nH, $\Delta I_{write} = 0.1\ \mu$A, and for $L_{loop} = 0.66$ nH, $\Delta I_{write} = 0.25\ \mu$A. At each bias point, the write current is applied for 100 ms and subsequently turned off. The device is allowed to rest for 100 ms before 10 readings of the yTron switching current are measured. Eight complete ramping cycles are recorded for each device. The write current at the first point of each step in switching current is recorded and the difference between sequential steps is calculated. The results from Table I show that increasing R_s decreases the number of consistent states and increases the average number of fluxons trapped

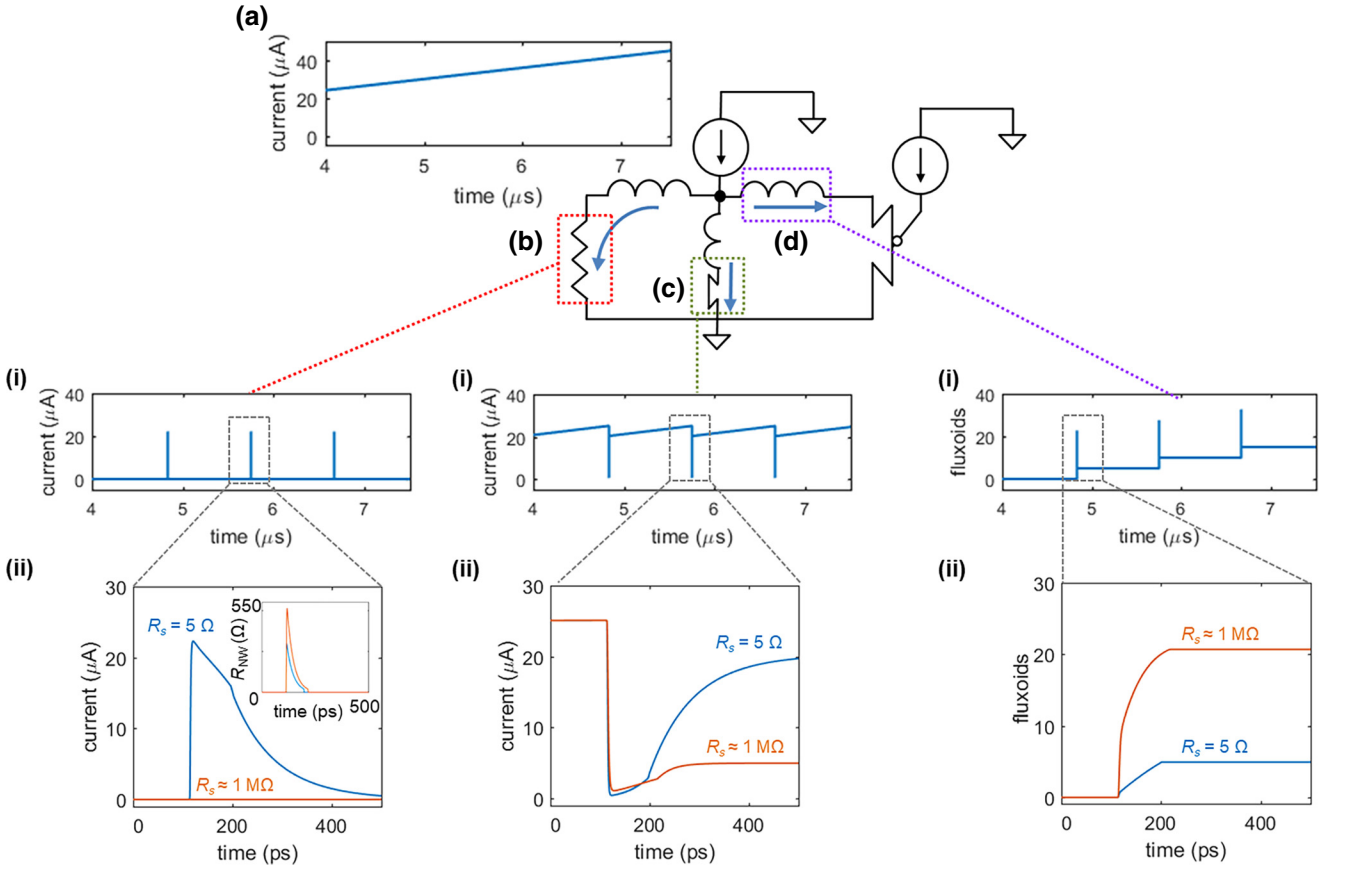

FIG. 4. Time domain simulations of the circuit highlighting the three branches through which the bias writing current is diverted. (a) Bias current ramp delivered to the device. (b) Current through the shunt resistor. (i) Simulation over a long-time domain. (ii) Simulation over a single switching event. Time on the x axis has been shifted to start from $t = 0$. In the 1-MΩ case, essentially no current is diverted to the resistor, and the maximum amount of current is stored in the loop. When $R_s = 5\ \Omega$, nearly all of the current is diverted to the resistor, reducing the amount of trapped flux. Inset shows that the low shunt resistor also reduces the hotspot resistance and allows it to collapse more quickly. (c) Current through the constriction. (i) Simulation over a long-time domain. (ii) Simulation over a single switching event. (d) Current through the inductor, represented in terms of trapped fluxoids. (i) Simulation over a long-time domain. The amount of flux trapped in the loop increases by 5 Φ_0 every time the constriction switches. (ii) Simulation over a single switching event, showing that the maximum amount of flux is trapped for the device shunted with 1 MΩ. For all of these simulations, $L_{shunt} = 50$ pH and $L_{loop} = 1.87$ nH.

per switching event, while decreasing the loop inductance may slightly reduce the amount. Plots showing the states of yTron outputs for Devices 2 and 3 may be found in the Supplemental Material [20].

C. Electrothermal simulations

To better understand how the device parameters influence the amount of flux n trapped per switching event, we model the dynamics of the system using circuit simulations that include the electrothermal dynamics of the resistive hotspot [21] and material-specific physical parameters [22]. Figure 4 shows the basic circuit, highlighting the main branches through which current is divided after the constriction switches: the shunt resistor [Fig. 4(b)], the constriction itself [Fig. 4(c)], and the loop inductor [Fig. 4(d)]. In a device with an unshunted constriction (represented here as $R_s = 1$ MΩ for consistency), nearly all of the bias current is diverted to the loop inductor after a switching event, causing the maximum amount of persistent current approximately equal to I_c to be stored in the loop once the hotspot collapses and the constriction regains the superconducting state. In contrast, shunting the constriction with $R_s = 5$ Ω allows the majority of the bias current to be diverted instead to the resistor, minimizing the amount of flux trapped through the loop inductor. Figures 4b(i)–4d(i) show the results over a longer timescale, where continuous switching of the shunted constriction brought on by a steadily increasing bias current ramp adds flux to the loop in increments of 5 Φ_0, thus confirming the experimental observations displayed in Fig. 3 for Device 1.

Figure 5 displays the amount of flux per switching event resulting from simulating devices of varying circuit parameters. Figure 5(a) shows that the amount of flux increases proportionally with increasing shunt resistance and shunt inductance, which agrees with the experimentally observed shift caused by increasing R_s. Figure 5(b) suggests a slightly more complex relationship between R_s and L_{loop}, with plateaus occurring due to limitations on the maximum loop current with respect to the critical current of the constriction—for example, if $I_c = 20$ μA, a loop inductance leading to a ratio of 2 μA of circulating current per fluxon cannot have more than 10 fluxons per switching event. While both of these results rely on the electrothermal dynamics included in the simulation, their general shapes stem from current division between the shunt impedance and the loop impedance after the nanowire switches. Details on this relationship may be found in the Supplemental Material [20]. In Fig. 5(c), the simulated trends for varying R_s with $L_{\text{loop}} = 1.85$ nH or $L_{\text{loop}} = 0.65$ nH are compared to the experimental results for the three devices listed in Table I. Data points representing the three measured devices show that the electrothermal simulations are in good agreement with the experimental measurements.

D. Discussion on applications

The results of our experiments and correspondence with simulations demonstrate that the device output may be tuned through simple circuit parameters and tailored to meet specific design requirements. As a result, the device is a promising platform for the development of a multilevel memory, with the number of states dictated by the critical current of the constriction and the amount of flux per event. While we demonstrate a maximum of seven states in the case of Fig. 3, the simulations of Fig. 5 show that the number could be increased by changes that reduce the number of fluxons per event, such as

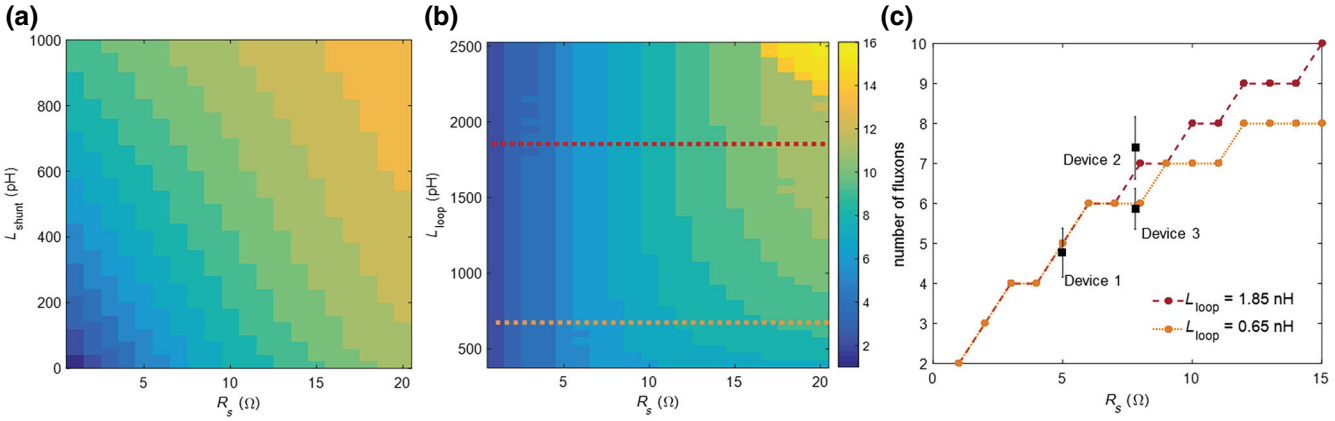

FIG. 5. Simulated effect of circuit parameters on amount of trapped flux. (a) Number of fluxons per switching event as a function of varying R_s and L_{shunt}. R_s is swept in increments of 1 Ω and L_{shunt} is swept in increments of 50 pH. L_{loop} is held constant at 1.87 nH. (b) Number of fluxons per switching event as a function of varying R_s and L_{loop}. R_s is swept in increments of 1 Ω, and L_{loop} is swept in increments of 50 pH. L_{shunt} is held constant at 50 pH. (c) Comparison of the simulated number of fluxons per switching event with the three experimentally measured devices. The orange curve represents the trend for $L_{\text{loop}} = 0.65$ nH, and the red curve represents the trend for $L_{\text{loop}} = 1.85$ nH. Experimental mean values are represented as black squares. The error bars are $\pm 0.5\sigma$.

further reducing R_s. This multilevel operation is significantly different from previously reported superconducting nanowire-based memories, which have thus far been predominantly binary devices [15,27,28]. It has recently been argued that multilevel memory may compensate for the large power consumption of peripheral circuits in superconducting memory arrays by providing a higher information capacity per cell given the same peripheral circuitry; additionally, multilevel memories may allow for increased memory density as the limits of physically shrinking a memory unit are approached [29]. Thus, future investigation of the device presented here as a multilevel memory may advance the scaling of superconducting memory arrays. Other potential applications of the device include use in multilevel logic or integration with other superconducting elements such as photon detectors. While the proof-of-concept device reported here has a rather large size ($3 \times 25\ \mu m^2$), the device can be scaled down by introducing a high-kinetic-inductance wiring layer for the loop, given that the geometric inductance is inconsequential. Further scaling improvements could be made by fabricating the loop as a stacked structure, as was suggested with previous nanowire-based memories [15].

IV. CONCLUSIONS

In summary, we develop a superconducting nanowire-based device capable of generating a response that is proportional to the strength of its input. By introducing local resistive shunting through on-chip fabrication, we are able to control the dynamics of a shunted constriction with a high-inductance superconducting loop and display behavior vastly different from its unshunted counterpart. When subjected to a dc bias current ramp, the device produces seven distinguishable states as a result of controlled flux trapping, illustrating that it may be able to be used as a multilevel memory. Through electrothermal circuit simulations and experimental measurements of devices with different circuit parameters, we show how the amount of flux added or subtracted per event—and thus the number of distinguishable states—can be adjusted through device design. We envision that this device can be used as a tunable element for proportional and multilevel operations.

CODE AVAILABILITY

The code that supports the plots within this paper and the electrothermal simulations used to confirm the findings of this study are available from the corresponding author upon reasonable request.

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E.T. designed the device. E.T. and M.C. fabricated the devices. M.C. deposited the superconducting film. M.O. designed and performed the simulations. E.T., A.M., and K.K.B. conceived the experiments. E.T. performed the measurements with assistance from B.B. and M.C., and E.T. analyzed the data. E.T. wrote the manuscript with input from all of the authors. K.K.B. supervised the project. All of the authors contributed to discussions and improved understanding of the results.

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