

Research Article

Three Microwave Frequency Dividers Using Current Source/Sink and Modified Current Source Inverters

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In a preceding paper Carlos E. Saavedra, 2005, established that frequency division can be achieved with the use of inverter rings and transmission gates. In this paper, we suggest three modified circuits which obtain the similar function, namely, using Current Sink Inverter, Current Source Inverter, and Modified Current Source Inverter. The performances of the proposed circuits are examined using Cadence and the model parameters of a 45 nm CMOS process. The simulation results of the three circuits are presented and are compared. We also present the results of a simple but effective novel technique to reduce clock skew between real and complementary clock signals and the corresponding improvement achieved in maximum frequency of operation. One of the proposed circuits can operate at up to 8.2 GHz input while performing a divide-by-4 operation.

1. Introduction

A frequency divider, also called, a prescaler, is a circuit that takes an input signal of a frequency, f_{in} , and generates an output signal of a frequency, f_{out} , such that $f_{out} = f_{in}/n$, where n is an integer. Thus when a periodic signal is given as input, frequency dividers generate a periodic signal as output at a frequency that is a fraction of the input signal.

Frequency dividers are a combination of RF IC and microwave circuits. They are of particular importance to phase locked loops (PLLs). PLLs employ frequency dividers in their feedback path which divide the output frequency down to a fraction. This divided frequency is then compared with the reference frequency obtained from a crystal oscillator in a phase detector. Finally, this output phase difference tunes the VCO output voltage [1, 2]. Besides PLLs, frequency dividers are used in frequency synthesizers, phase shift keying demodulators, and so forth. One of the most recent applications of frequency dividers is applied on high speed Serializers/Deserializers (SerDes) and high frequency Local Multipoint Distribution Service (LMDS) technology.

Frequency dividers can be devised with both analog and digital circuits. But as of now most of the analog frequency dividers are solely employed for EHF (>30 GHz) band. The use of digital circuits suffices for lower frequencies. Interestingly these can support both analog, and digital inputs. But digital circuits do have the drawback of increased circuit delay and speed degradation as the supply voltage is reduced and operating speed is increased. This is attributed by an increase in output RC time constant due to a reduction in gate to source driving voltage [3].

The analog approach involves several methods. The very first method used is regenerative feedback frequency dividers and was suggested by Miller in 1939 [4]. Its main element is a nonlinear feedback circuit consisting of a mixer and a loop filter. Although this method has an added advantage of having a simple steady state operation, it suffers from complicated start-up and transient operations [5]. A related approach uses injection-locked frequency dividers (ILFDs). ILFDs function similar to injection-locked oscillators and operate in a free-running mode. This is in contrast to regenerative methods which do not have free run and require

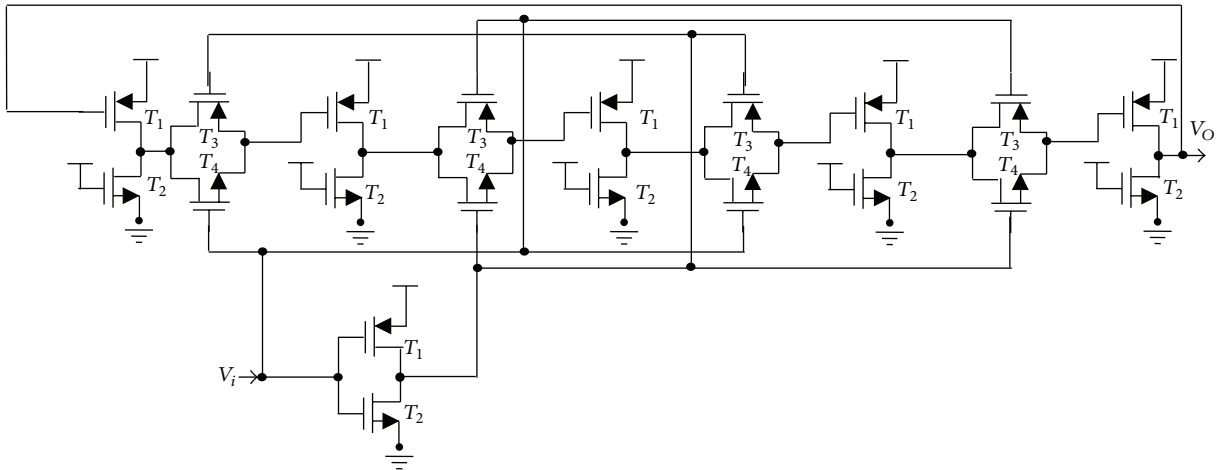


FIGURE 1: Device level presentation of Current Sink Inverter.

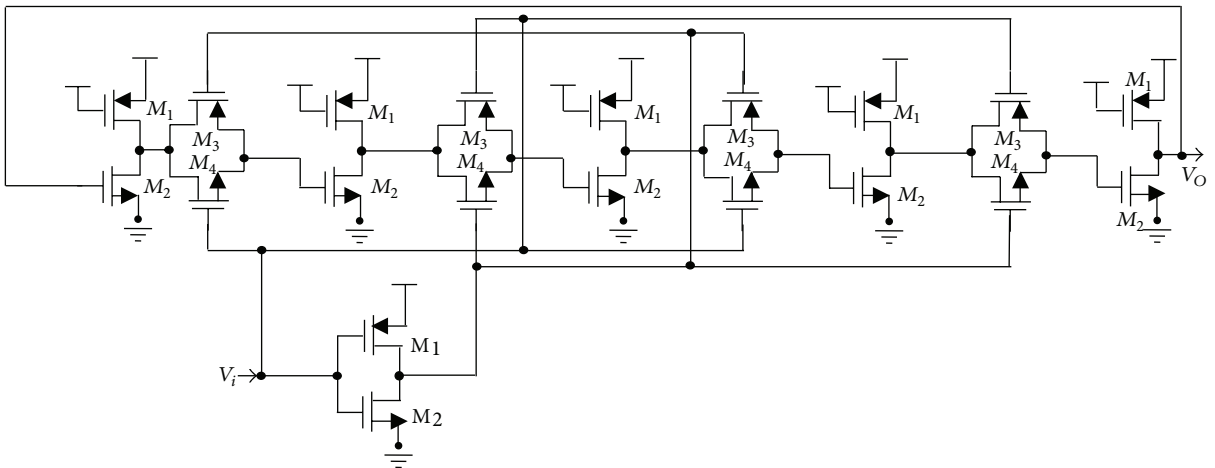


FIGURE 2: Device level presentation of Current Source Inverter.

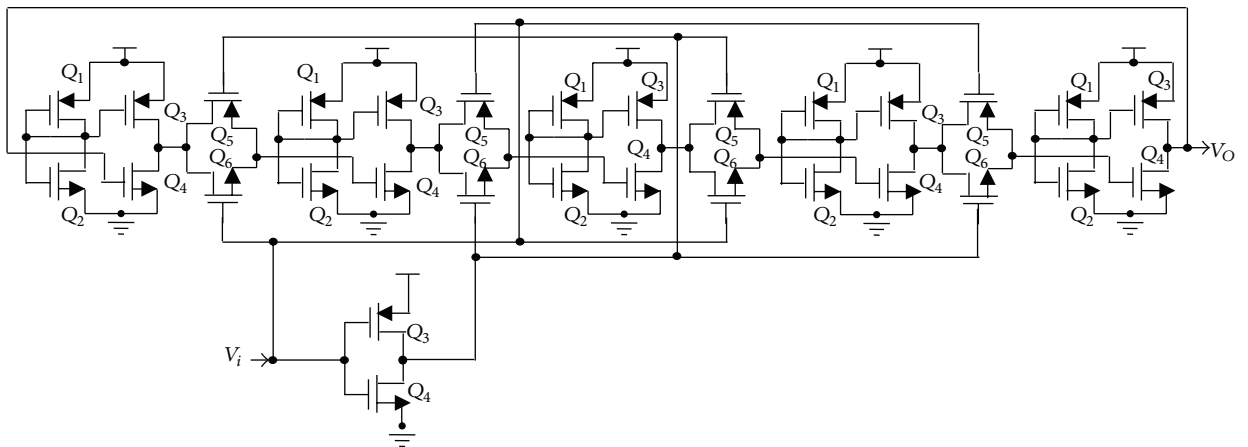


FIGURE 3: Device level presentation of Modified Current Source Inverter.

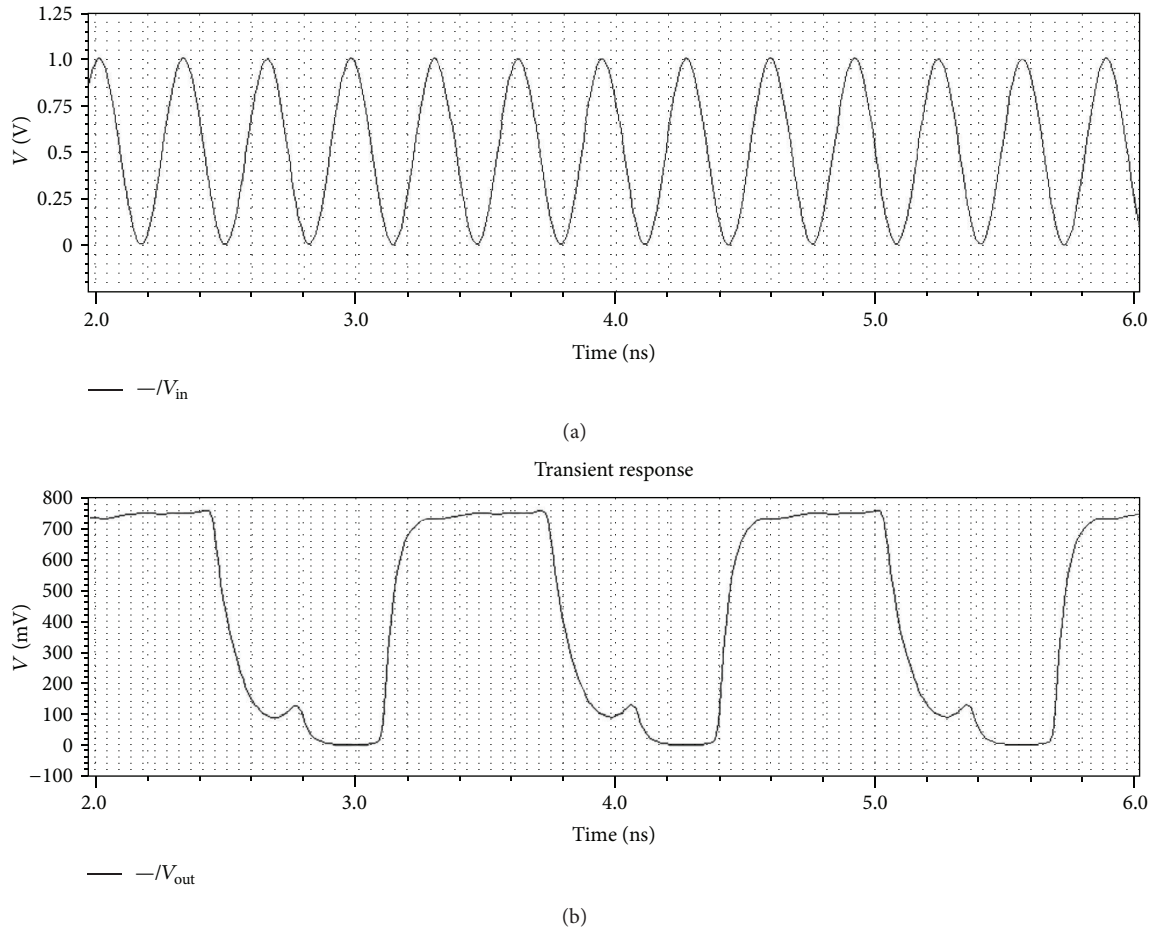


FIGURE 4: Sine input at 3.1 GHz and resulting output.

an injected signal to produce an output [6]. ILFDs have the advantage of having lower power dissipation compared to several digital implementations of frequency dividers, but this is negated by a limited locking bandwidth. A third analog method is introduced by adopting parametric frequency division. This method offers broader bandwidths and simpler configurations, overtaking the previous two methods [7].

Similarly, there exist several digital approaches on designing a frequency divider. Static frequency dividers are made to use flip-flops and are composed of two D-latches in cascade with a negative feedback configuration [2]. These circuits are called Source Coupled Logic (SCL) when implemented in CMOS. This configuration provides a divide-by-2 function. Higher division ratios are obtained by cascading this block. The two latches can be duals of each other, thus requiring only a single-phase clock to drive both the latches. This is particularly of great use as the frequency of operation increases, since there is no clock skew associated with this design, or the latches can be identical, which would require two clock signals, the true clock and its complement [8]. A second approach involves dynamic logic, as described in [9]. This has the advantage of reduced power consumption on account of lesser capacitive loads which is achieved by minimizing the aspect ratios (W/L). This design also leads

TABLE 1: Sine input parameters.

DC amplitude	0.5 V
AC amplitude	0.5 V
Delay time	1 fs
Amplitude	0.5 V

to a reduction in the number of transistors. But dynamic logic involved has the drawback of increased instability and reduced tolerance to process and temperature variation. Other implementations incorporated have both static logic and dynamic logic in the same circuit [10]. These tend to use the dynamic logic in the input block to take advantage of their capability of operating at a higher frequency. This is then followed by a static logic block, which is optimized for low power consumption.

An alternative method used to achieve frequency division is the use of cascaded inverters. These circuits can work with both analog and digital input signals. This is described in [11, 12]. The work in [1] by Saavedra is based upon the previous two papers and suggests a more compact CMOS inverter ring topology. In [1], the circuit consists of a chain of odd numbers of cascaded inverters with the output of the last inverter being

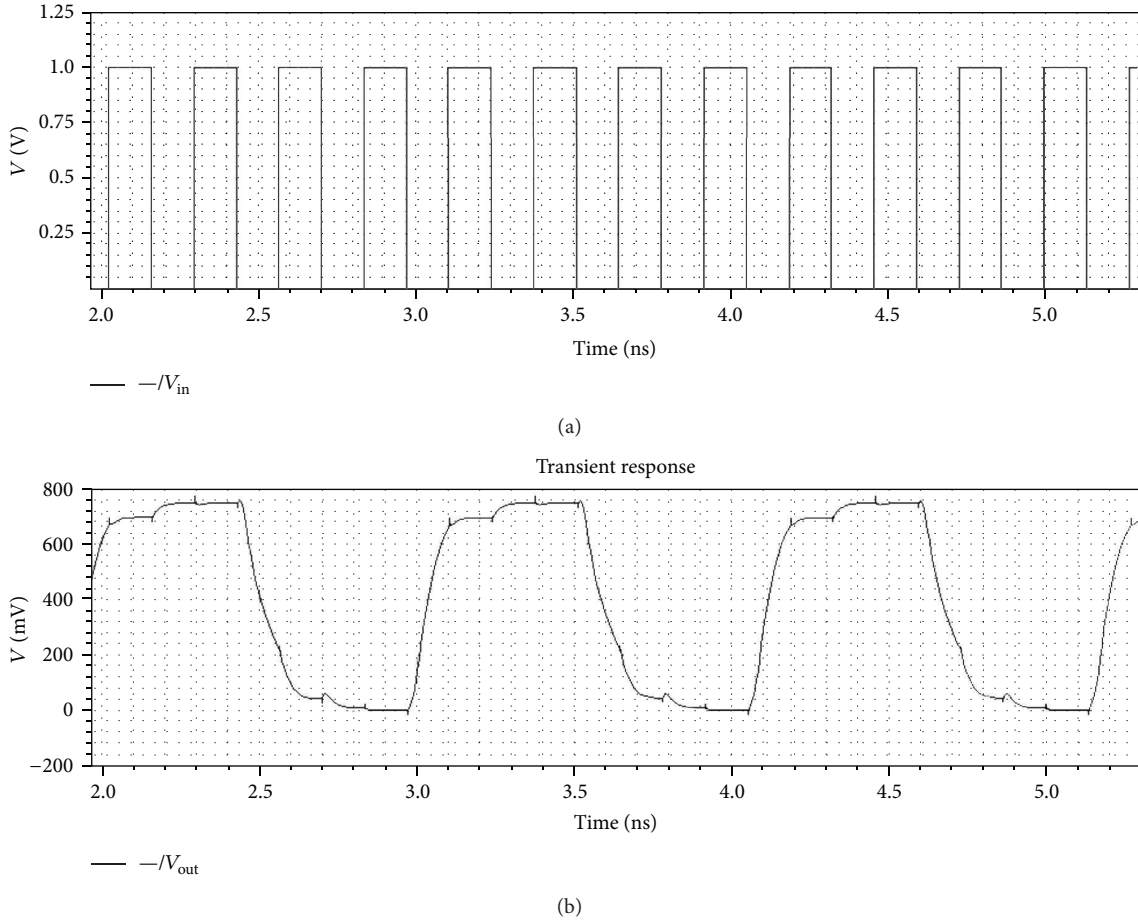


FIGURE 5: Square wave input at 3.7 GHz and resulting output.

TABLE 2: Square wave input parameters.

Voltage 1	1 V
Voltage 2	0 V
Delay time	1 fs
Rise time	2 fs
Fall time	2 fs
Duty cycle	50%

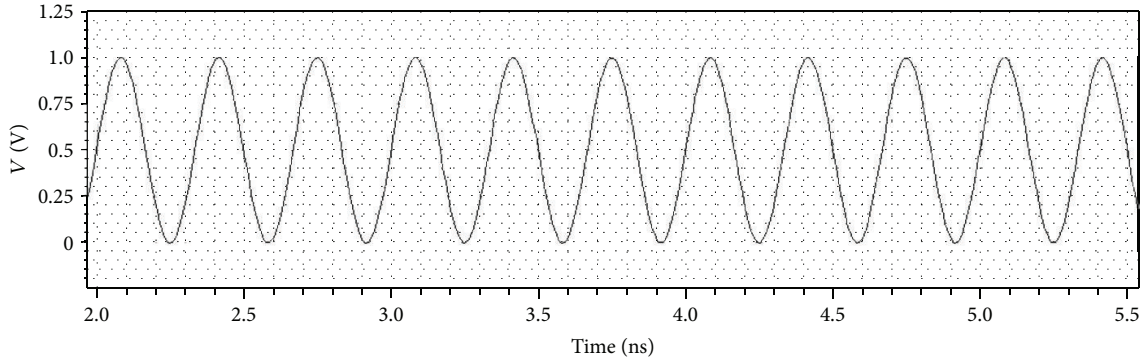
feedback to the first inverter to form a closed loop. It is a well-known fact that a chain of odd numbers of inverters in a loop tends to oscillate due to its inherent instability. This oscillation is however controlled by using transmission Gates (TGs) operating in between two adjacent inverters. These transmission gates are clocked by Clk and $\sim\text{Clk}$. Also the TGs are clocked such that two consecutive TGs are clocked with a complementary signal, which means only one of any two consecutive TGs will be conducting at any time. The overall implication of this clocking scheme is that the feedback loop would be broken and effectively controlled and rely upon the frequency of the clocking signal.

To understand the divide-by-four operation, it is sufficient to grasp the timing description of the circuit. Supposing

that the TGs were not present then any change in the output of the first inverter INV_1 would have propagated throughout the chain of inverters and has been fed back to INV_1 with a delay equal to the sum of the propagation delays through each of the inverters. But the presence of the TGs means that the signal propagation from any INV_n to the next INV_{n+1} only after the intervening TG is switched on.

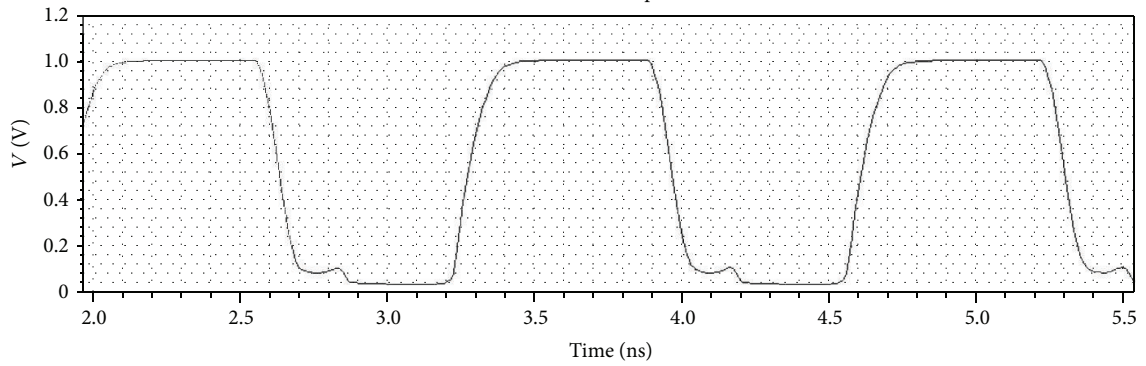
The purpose of this paper is to modify the circuit in [1] in terms of the logic implementation of the inverter used. These modified circuits were simulated and the results observed are analyzed in terms of a maximum frequency of operation, frequency locking range, power dissipation, figure of merit, and output voltage swing. In addition, we proposed an additional circuit component to improve upon the performance of the original circuit by reducing the skew between the true and complementary clock signals. This leads to an enhanced maximum frequency of operation.

The organization of the remaining sections is as follows. All the circuit's descriptions are described in Section 2. The simulation specifications and results obtained are described in Section 3. Several methods to optimize the proposed circuits and the results of their implementation are considered in Section 4. Finally, this is followed by the conclusion in Section 5.



(a)

Transient response



(b)

FIGURE 6: Sine input at 3 GHz and resulting output.

TABLE 3: Measured operating parameters of the proposed circuits.

Inverter type	Input type	V_{bias}	Max freq.	Min freq.	Range of operation	$P_{\text{dissipation}}$	Figure of merit	Voltage swing		Figure no.
								Min	Max	
Current sink	Sine	490 mV	3.1 GHz	0.3 GHz	2.80 GHz	$40.58 \mu\text{W}$	76.39	0	750 mV	Figure 4
	Square	490 mV	3.7 GHz	≤ 10 MHz	3.69 GHz	$33.61 \mu\text{W}$	110.08	0	750 mV	Figure 5
Current source	Sine	325 mV	3.0 GHz	0.22 GHz	2.78 GHz	$27.05 \mu\text{W}$	110.09	35 mV	1 V	Figure 6
	Square	325 mV	3.268 GHz	≤ 10 MHz	3.258 GHz	$18.21 \mu\text{W}$	179.46	32 mV	1 V	Figure 7
Modified current source	Sine	n/a	5.55 GHz	0.22 GHz	5.33 GHz	$63.44 \mu\text{W}$	87.48	100 mV	1 V	Figure 8
	Square	n/a	6.135 GHz	≤ 10 MHz	6.125 GHz	$45.52 \mu\text{W}$	134.77	100 mV	1 V	Figure 9

TABLE 4: Measured operating parameters of the optimized circuits.

Inverter type	Input type	V_{bias}	Max input frequency	$P_{\text{dissipation}}$	Figure of merit	Voltage swing		Remarks/possible usage mode
						Min	Max	
Current sink with V_{bias} optimization	Sine	450 mV	2.55 GHz	$31.29 \mu\text{W}$	81.49	0	815 mV	Reduced output voltage swing as V_{bias} is increased limits practical implementation
		600 mV	3.75 GHz	$71.26 \mu\text{W}$	52.62	80 mV	500 mV	
	Square	450 mV	3.0 GHz	$25.46 \mu\text{W}$	117.83	0	810 mV	
Current source with V_{bias} optimization	Sine	250 mV	5.7 GHz	$55.12 \mu\text{W}$	103.41	64 mV	1 V	High speed mode
		415 mV	3.65 GHz	$33.42 \mu\text{W}$	109.21	37 mV	1 V	Low power mode
	Square	250 mV	6.17 GHz	$37.71 \mu\text{W}$	163.61	62 mV	1 V	High speed mode
		415 mV	4 GHz	$20.75 \mu\text{W}$	192.77	37 mV	1 V	Low power mode

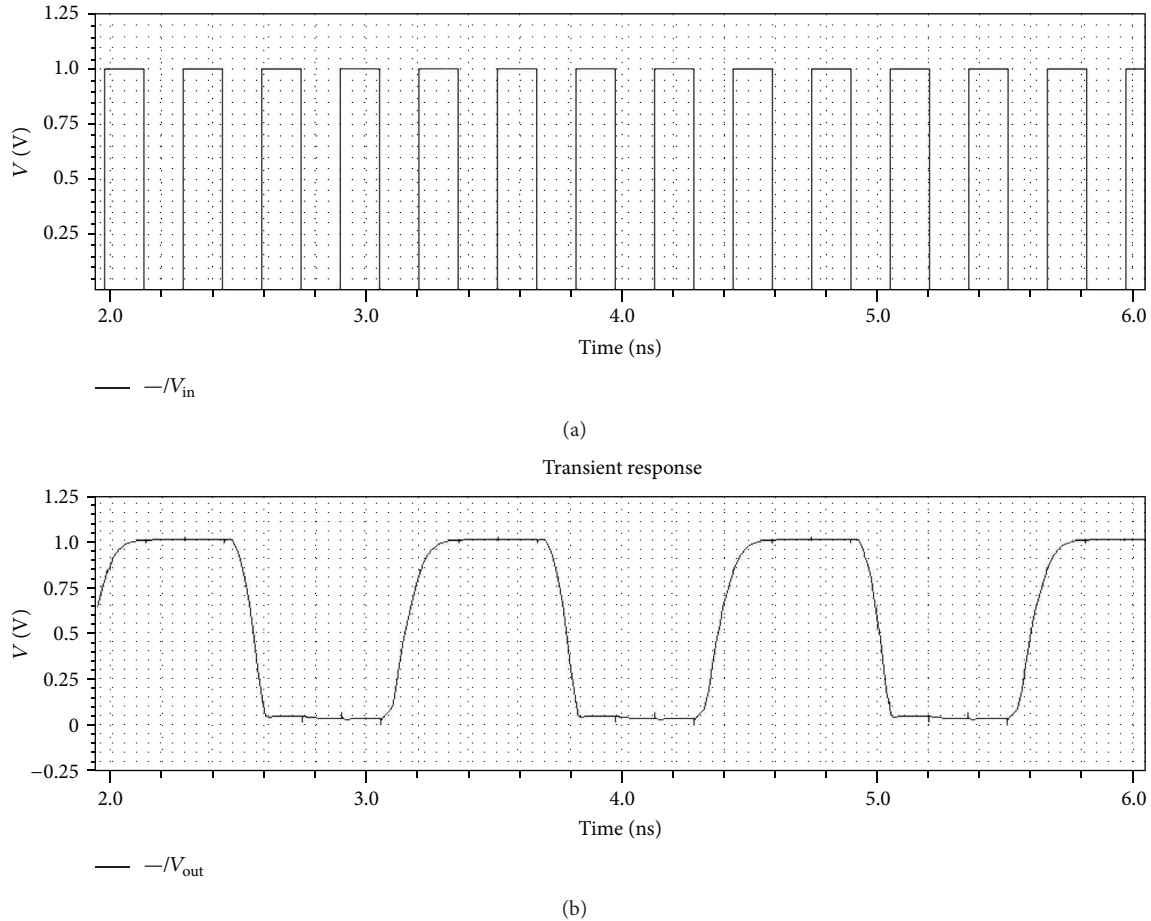


FIGURE 7: Square wave input at 3.268 GHz and resulting output.

TABLE 5: Measured operating parameters of proposed circuits with skew reduction block.

Inverter type	Input type	V_{bias}	Max input freq. with skew reduction block	Max input freq. without skew reduction block	Increase in maximum input frequency	$P_{\text{dissipation}}$ (with skew reduction block)	Figure of merit (with skew reduction block)
Current sink	Sine	490 mV	3.6 GHz	3.1 GHz	16.13%	134.43 μW	26.77
	Square	490 mV	3.717 GHz	3.7 GHz	0.46%	33.68 μW	110.36
Current source	Sine	325 mV	4.9 GHz	3.0 GHz	63.34%	138.74 μW	35.32
	Square	325 mV	3.448 GHz	3.268 GHz	5.50%	30.07 μW	114.66
Modified current source	Sine	n/a	8.2 GHz	5.55 GHz	47.75%	197.77 μW	41.46
	Square	n/a	8.163 GHz	6.135 GHz	33.05%	76.01 μW	107.39

2. Circuits Description

The original circuit in [1] proposes the use of standard CMOS inverters which is inherently optimized for low power operation. In [13], this is modified to use PMOS load inverters, which is especially suited for the high frequency input stages. A related approach using cascaded inverters by Razavi is given in [14] and therein used dynamic (or clocked) latches and is suited for a low distortion output.

In order to achieve better output and a higher capability of maximum frequency of operation while ensuring minimal power dissipation, different types of inverters were tried out

for implementation of the inverter stages in the frequency divider. The various modifications tried out on the circuit in this paper are Current Source Inverter, Current Sink Inverter and Modified Current Source Inverter.

2.1. Current Sink Inverter. In a Current Sink Inverter stage a current sink load is used. The current sink (Figure 1) is implemented using a common gate configuration and employs an n-channel transistor with its gate connected to a fixed bias supply of $V_{\text{bias}} = 490$ mV, while the PMOS transistor serves as a pull, up network. It is observed that

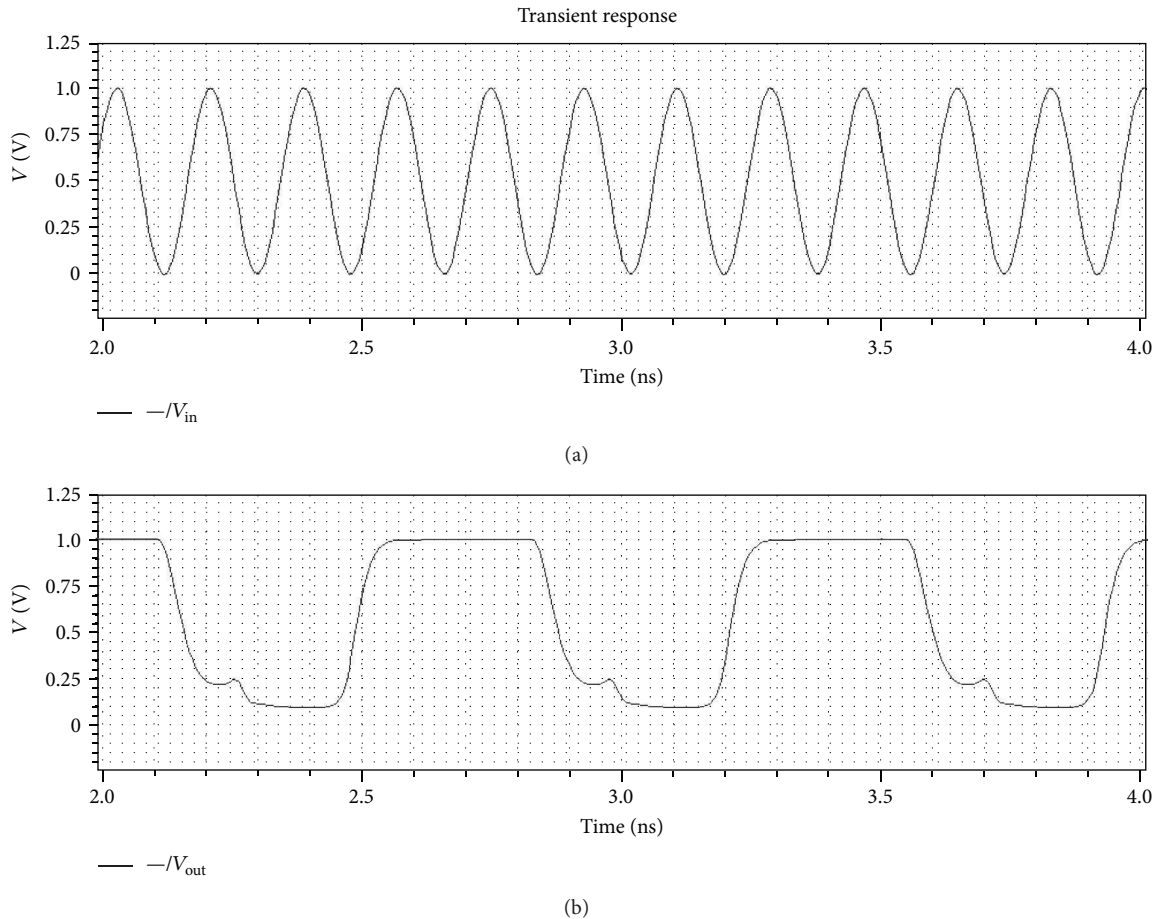


FIGURE 8: Sine input at 5.55 GHz.

decreasing this biasing voltage increases circuit performance especially the maximum frequency of operation at the cost of increased current drawn and higher power dissipation. Hence, a compromise must be made between the two while deciding V_{bias} .

2.2. Current Source Inverter. In a Current Source Inverter stage, a current source load is used [15–17]. The current source (Figure 2) is implemented using a common gate configuration and employs a p-channel transistor with its gate connected to a fixed bias supply of $V_{bias} = 325$ mV, while the NMOS serves as a pull-down network. Once again, the dependence of circuit performance on the biasing voltage was observed. Overall performance of this circuit achieved has much lower power dissipation than the other two. It was felt that there was room to push the circuit for it to operate at higher frequencies at the cost of increased power dissipation. Hence, the circuit operation was analyzed for several values of V_{bias} to evaluate its impact on the power dissipation of the circuit.

2.3. Modified Current Source Inverter. The current source circuit described above suffers from the drawback that it requires an on-chip battery, which is difficult to incorporate

in a typical portable embedded device. So a voltage divider CMOS circuit (Figure 3) is used to give the dc voltage supply required to bias the gate of the p-channel transistor and a modified current source inverter is opted for. The device ratios were chosen with primarily least delay and maximum possible frequency of operation in mind. Hence this circuit was able to operate at a much higher frequency than the other circuits proposed, but this is at the cost of increased static power dissipation.

3. Simulation Results

3.1. Objective. We discuss the design specifications of the frequency divider and its modifications in this section. We also deal with the experiments performed to analyze the circuit behavior of the proposed frequency divider circuit. The performances of the proposed circuits are examined using Cadence and the model parameters of a 45 nm CMOS process. The main objective of the simulation was to get the maximum frequency of operation of the various modified circuits and to calculate the power dissipation of the circuit.

3.2. Specifications. The circuit was simulated using a DC supply rail voltage of +1V and employed corresponding

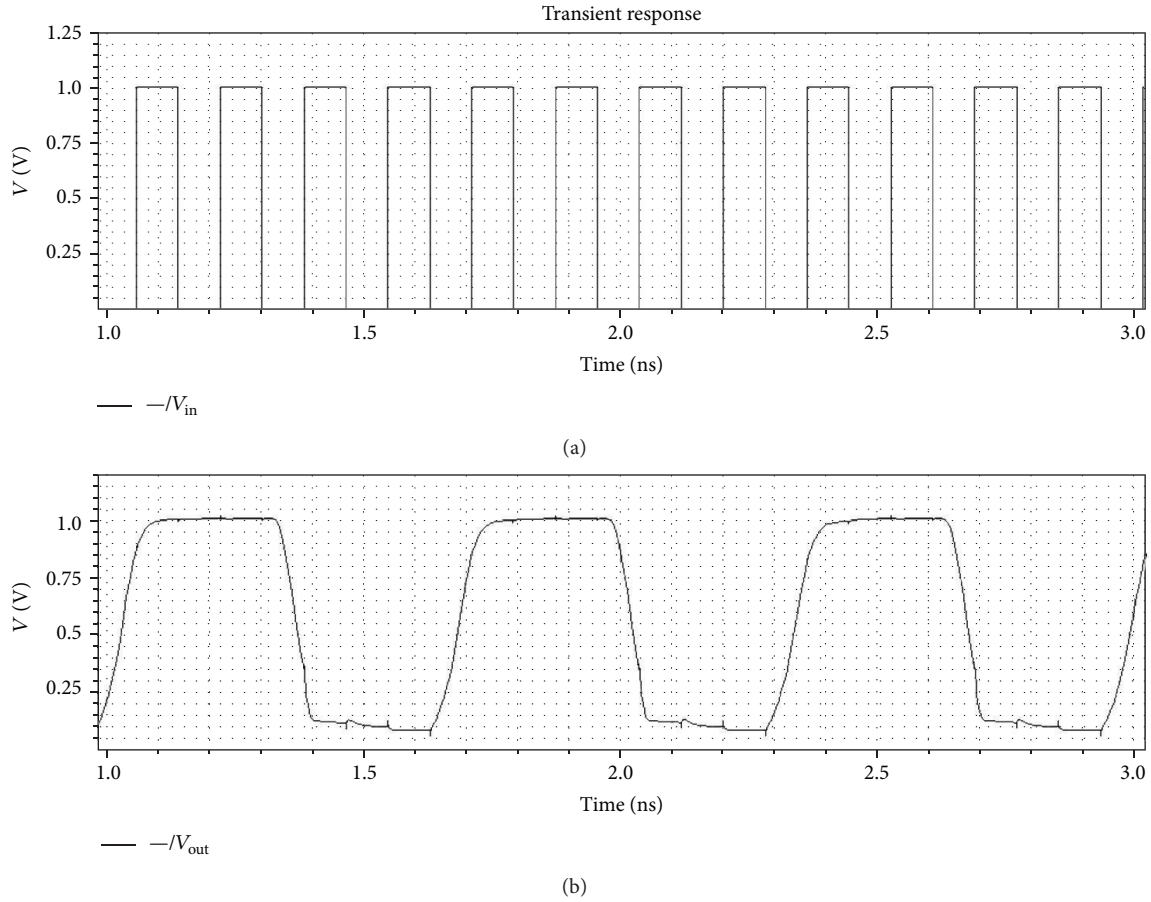


FIGURE 9: Square wave input at 6.135 GHz.

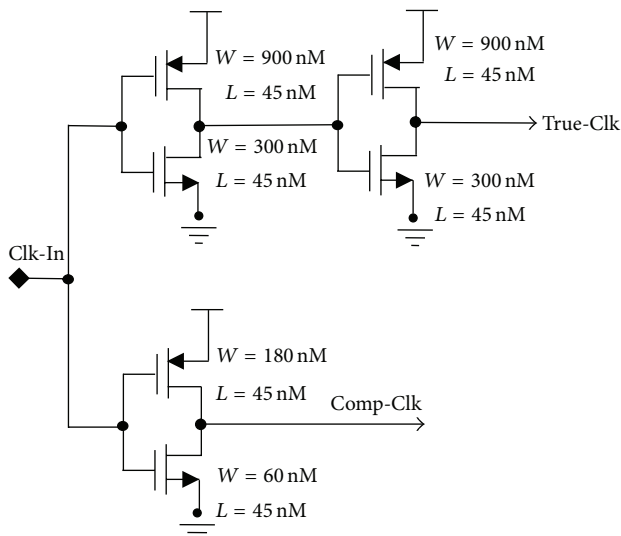


FIGURE 10: Skew reduction block with aspect ratios.

+1V PMOS and +1V NMOS transistors from the 45 nm gpdk library in Cadence. Initially, a sinusoidal input was applied as stimuli; this was followed by square wave input

stimuli. The parameters for these inputs are given in Tables 1 and 2. Frequency of input was varied from a minimum of 2 GHz to the highest frequency limit possible for each of the given circuits. The limits of operation were modeled as the requirement that the rise time in the output waveform is to be at the most 0.7 times the corresponding bit period (half of the time period). Alternatively, at the higher end this frequency is the limit beyond which the circuit no longer can keep up with the input causing the output to show a divide-by-four operation which is either unstable or totally absent.

Power dissipation was calculated using the average DC current consumed from the DC voltage sources. From these values, the figure of merit (FOM) for each of the circuits was estimated, where it is defined as

$$\text{FOM} = \frac{\text{Maximum Frequency of Operation (in GHz)}}{\text{Power Dissipation (in mW)}}. \quad (1)$$

3.3. Device Sizing. The complementary input signal was generated uniformly in all circuits by using an inverter of aspect ratio W_P/L_P : 180 nm/45 nm and W_N/L_N : 60 nm/45 nm for the PMOS and NMOS, respectively. On the other hand, the transistor sizing of the inverter stages in the actual circuit was optimized in each of the modifications in an effort to improve

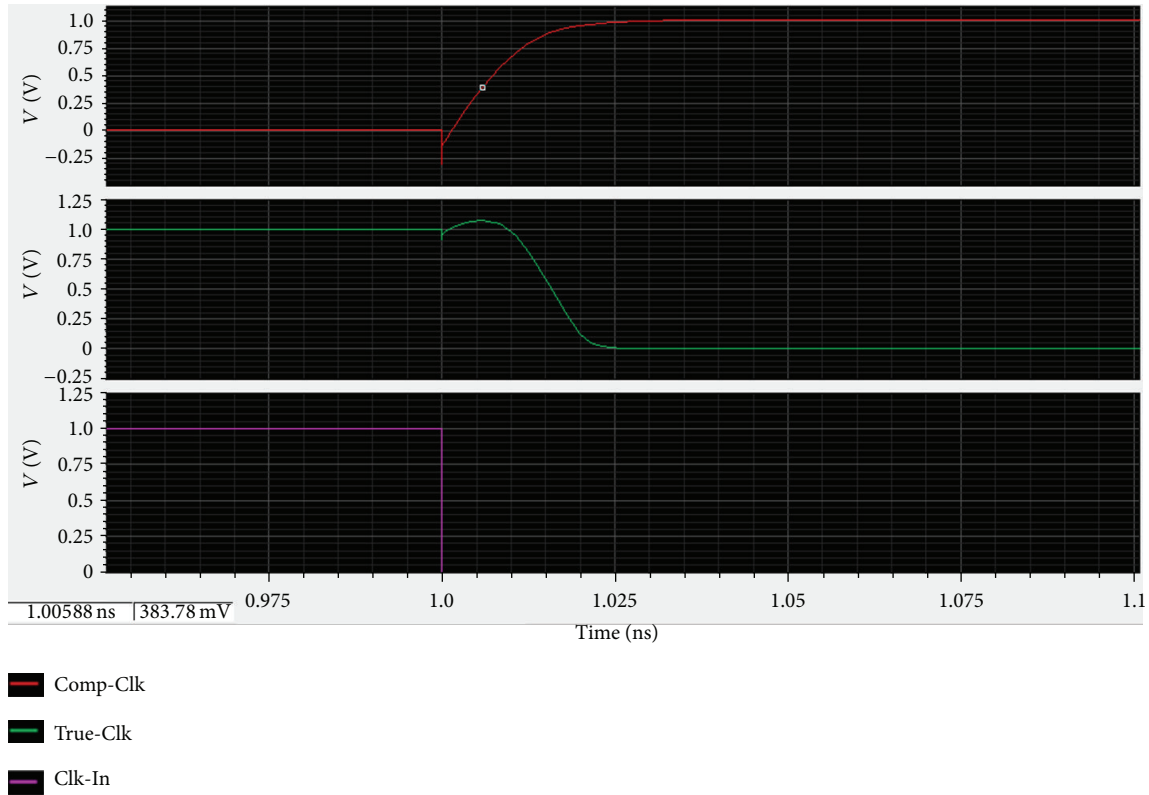


FIGURE 11: Skew reduction block output-transition from high to low.

the slew rate and minimize distortion in the output signal. The channel length of the TGs was chosen as the minimum possible length, that is, 45 nm in order to minimize the RC delay. This effectively improved the maximum frequency of operation over the nonoptimized circuit.

For the Current Sink Inverter circuit, the aspect ratios of T_1 , T_2 , T_3 , and T_4 were taken as 60 nm/45 nm, 60 nm/45 nm, 180 nm/45 nm, and 60 nm/45 nm.

For the Current Source Inverter circuit, the aspect ratios of M_1 , M_2 , M_3 , and M_4 were taken as 60 nm/45 nm, 60 nm/45 nm, 180 nm/45 nm, and 60 nm/45 nm.

For the Modified Current Source inverter circuit, the aspect ratios of Q_1 , Q_2 , Q_3 , Q_4 , Q_5 , and Q_6 were taken as 60 nm/180 nm, 180 nm/45 nm, 135 nm/45 nm, 60 nm/45 nm, 180 nm/45 nm, and 60 nm/45 nm.

3.4. Simulation Results. The results for all the three modified circuits, both sinusoidal and square wave inputs along with the operating parameters observed during simulation such as maximum and minimum frequency operations, power dissipation, figure of merit, and voltage swing are tabulated in Table 3. The low DC rail voltage imposes a serious limitation on the upper frequency of operation, but at the same time helps to keep the power dissipation down to a minimum level. The Current Sink Inverter based circuit has power dissipation in between those of the other two circuits but has the least FOM compared to the others. The Current Source Inverter requires the least amount of power but also has a limited

frequency range of operation. It also has the best FOM among the three. Finally, the Modified Current Source Inverter has a much higher maximum frequency of operation, while dissipating the most power and partly sacrificing the FOM.

The input and corresponding output waveforms for both sine and square wave input are shown in Figures 4 and 5 for Current Sink Inverter circuit (Figure 1), Figures 6 and 7 for Current Source Inverter circuit (Figure 2), and Figures 8 and 9 for Modified Current Source Inverter circuit (Figure 3).

4. Optimizations in the Proposed Circuit

The first set of optimizations involves changing the bias voltage of the Current Sink Inverter and Current Source Inverter based circuits. The corresponding simulation results in terms of variation of maximum frequency of operations and power dissipation are measured and tabulated (see Table 4).

For the Current Sink Inverter based circuit, it is observed that as power dissipation increases, V_{bias} is increased. The maximum frequency of operation ranges from 2.55 GHz to 3.75 GHz for sinusoidal input and from 3 GHz to 4.54 GHz for square wave input. V_{bias} is varied from 490 mV to 600 mV in both cases. The disadvantage is that the output voltage swing reduces progressively as the bias voltage is increased.

For the Current Source Inverter based circuit, it is observed that when power dissipation decreases, V_{bias} is increased. The maximum frequency of operation ranges from

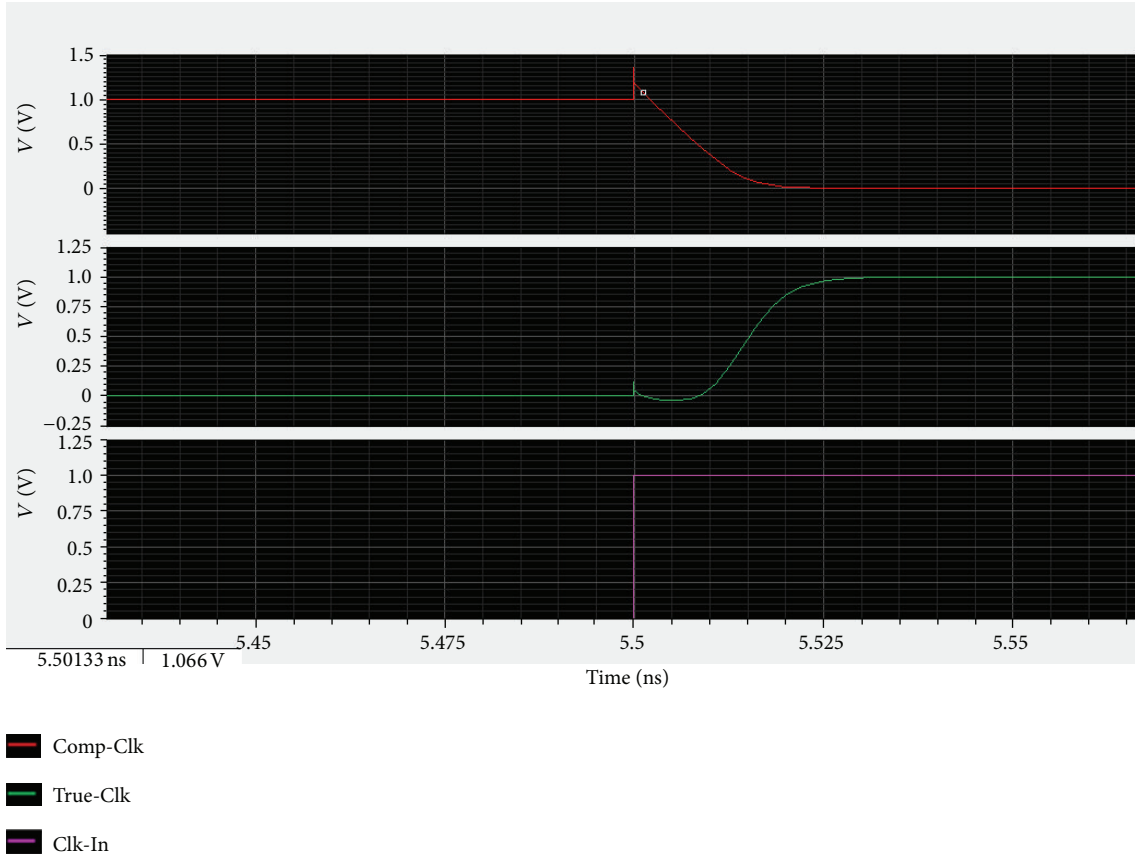


FIGURE 12: Skew reduction block output-transition from low to high.

3.65 GHz to 5.7 GHz for sinusoidal input and from 4 GHz to 6.17 GHz for square wave input as V_{bias} is varied from 250 mV to 415 mV. The output voltage swing is relatively stable as the bias voltage is varied.

If an additional external circuit is developed, such that the V_{bias} is dynamically varied as per requirement, then the Current Source Inverter based frequency divider can be used to operate in a variety of modes: a low power mode with lower frequency of operation or a high speed mode for higher operational frequencies.

The second set of optimizations involves attempts to reduce the clock skew between the true and complementary clock signals in an effort to increase the maximum frequency of operation possible for the frequency divider circuit.

One of the methods suggested by Razavi in [8] is to introduce a transmission gate in the path of the true clock signal in a bid to delay it almost equally as the delay faced by the signal while being passed through the inverter. Though this method is effective, it has the drawback of inducing distortion of the clocking signal as supply voltage is scaled, and hence reducing its effectiveness.

We proposed another method, wherein two back to back inverters with minimum dimensions on the true signal path, while the complementary clock is obtained through a single inverter with nonminimal dimensions.

Overall dimensions are optimized to balance out skew between true and complementary clock signals. The circuit for this is presented in Figure 10, and the results (Figures 11 and 12) of the simulation using this skew reduction block are given in Table 5.

This method of clock skew reduction is very effective in decreasing skew between the two clocking signals to an order of 5–7 ps and thereby increasing the maximum frequency of operation. Large improvements are obtained for circuits with sinusoidal inputs at the cost of increased power dissipation. The modified current source inverter can operate at up to 8.2 GHz for sinusoidal input and 8.16 GHz for square wave input with this optimization. This is an improvement of almost 48% over the unoptimized circuit in terms of highest possible frequency of operation.

5. Conclusion

We have presented a set of modifications to an inverter ring based microwave frequency divider circuit. These modifications are in terms of the topology of the inverter used. The topologies used are Current Source Inverter, Current Sink Inverter, and Modified Current Source Inverter. The results of the modified circuits have been tabulated and compared.

Amongst them the Current Source Inverter based circuit has the least power dissipation while the Modified Current Source Inverter has the highest frequency of operation.

We have also presented a set of optimizations which includes varying the bias voltage and also introducing a skew reduction block. The use of the skew reduction block gives significant improvement in the highest possible frequency of operation. Among the circuits proposed by us, the best performance is given by the Modified Current Source Inverter based circuit with a skew reduction block, which can operate at up to 8.2 GHz for sine and 8.163 GHz for square input. The FOM is 41.46 for sine input and 107.39 for square input.

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