Research Article

Full-Wave Analysis of Traveling-Wave Field-Effect Transistors Using Finite-Difference Time-Domain Method

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Nonlinear transmission lines, which define transmission lines periodically loaded with nonlinear devices such as varactors, diodes, and transistors, are modeled in the framework of finite-difference time-domain (FDTD) method. Originally, some root-finding routine is needed to evaluate the contributions of nonlinear device currents appropriately to the temporally advanced electrical fields. Arbitrary nonlinear transmission lines contain large amount of nonlinear devices; therefore, it costs too much time to complete calculations. To reduce the calculation time, we recently developed a simple model of diodes to eliminate root-finding routines in an FDTD solver. Approximating the diode current-voltage relation by a piecewise-linear function, an extended Ampere's law is solved in a closed form for the time-advanced electrical fields. In this paper, we newly develop an FDTD model of field-effect transistors (FETs), together with several numerical examples that demonstrate pulse-shortening phenomena in a traveling-wave FET.

1. Introduction

The generation of a short electrical pulse with picosecond duration is one of the keys to producing a breakthrough in high-speed electronics. The applications of short pulses include measurement systems with picosecond temporal resolution, over-100-Gbit/s communication systems, and submillimeter-to-teraherz imaging systems [1]. We recently found that a transmission line periodically loaded with resonant tunneling diodes (RTDs) greatly compresses the temporal width of the pulse input to it [2]. Once the input pulse crosses the peak voltage of the loaded RTDs, the exponential wave is developed at voltages smaller than the peak voltage, and the sinusoidal wave is coupled to it at larger voltages, whose wave number becomes much larger than that of the input; therefore, the input pulse experiences significant shortening. The similar pulse shortening can be realized in traveling-wave field-effect transistors (TWFETs). A TWFET is a special type of FET whose electrodes are employed not only as electrical contacts but also as transmission lines [3]. We consider the case where a decreasing voltage pulse is applied to the gate line and an increasing one is simultaneously applied to the drain line. By properly designing the top and bottom levels of the applied pulses, every FET simulates an electronic switch (the switch is open for voltages greater than some fixed threshold, and closed otherwise). This arrangement guarantees the pulse shortening owing to the development of the exponential-sinusoidal waves as observed in an RTD line [4].

In order to evaluate the above-mentioned results in monolithically integrated devices, we have to develop the models of nonlinear devices such as RTDs and FETs for use in a finite-difference time-domain (FDTD) electromagnetic solver [5]. In FDTD-based solvers of Maxwell's equations, a circuit element such as a capacitor, an inductor, or a nonlinear device, is usually implemented in an extended Ampere's law as a field-dependent conductance/capacitance in a single Yee cell [6]. Unfortunately, it requires some root-finding routine such as the Newton-Raphson method to solve it to obtain the temporal advanced electrical fields for numerical stability [7]. The situation becomes more cumbersome, when the physical extent of devices cannot be ignored. Because we have to evaluate several adjacent cells for the terminal voltages that determine the device operation, a root-finder for multiple-variable functions is needed, which is very time-consuming. Moreover, we consider nonlinear

transmission lines, which generally include numerous non-linear devices.

Recently, we developed a concise model of nonlinear devices that contributes to eliminating the time-consuming root-finding procedures mentioned above. It approximates the voltage dependence of the device current by a piecewise-linear function and solves an extended Ampere's law in a closed form. Actually, we successfully demonstrated an FDTD calculation of the pulse shortening in an RTD line [8]. The similar modeling can be applied not only for diodes but also for three-terminal devices such as FETs. Based on our strategy, we first discuss an FDTD model of FETs after giving brief reviews and then show the results of full-wave calculations that demonstrate the pulse compression in a TWFET.

2. Diode Model in FDTD

When the conduction current density flowing in the device is denoted by $\mathbf{J}_L$, the temporal evolution of the electromagnetic fields is calculated on the basis of an extended Ampere's law as

$$\frac{\partial \mathbf{E}}{\partial t} = \frac{1}{\epsilon} \nabla \times \mathbf{H} - \frac{1}{\epsilon} \mathbf{J}_L, \tag{1}$$

where $\mathbf{E}$, $\mathbf{H}$, and ϵ are the electric field, magnetic field, and dielectric constant, respectively. By the single-cell implementation of the lumped device, (1) is converted as follows:

$$E_y^n = E_y^{n-1} + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}\right)_y - \frac{\Delta t}{\epsilon \Delta x \Delta z} I_L(V_L)^{n-1/2}, \tag{2}$$

where Δx, Δz, and Δt show the cell size in x, z, and t directions, respectively. The superscripts show the temporal positions, by which we represent the alternative evaluations of electrical and magnetic fields in FDTD. Moreover, I_L and V_L show the device current and terminal voltage, respectively. The current is assumed to flow in the y direction and is equal to $|\mathbf{J}_L|\Delta x \Delta z$. Moreover, V_L is given by $E_y \Delta y$ at the cell corresponding to the device. Thus, (2) becomes

$$E_y^n = E_y^{n-1} + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}\right)_y - \frac{\Delta t}{\epsilon \Delta x \Delta z} I_L^{n-1/2}\left(E_y^n\right). \tag{3}$$

As mentioned above, the argument of I_L is evaluated at time n for numerical stability. When a device occupies N adjacent cells, the difference equations to be solved become

$$E_y^n[i] = E_y^{n-1}[i] + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}[i]\right)_y$$
$$- \frac{\Delta t}{\epsilon \Delta x \Delta z} I_L^{n-1/2}\left(E_y^n[1], E_y^n[2], \ldots, E_y^n[N]\right) \tag{4}$$
$$(i = 1, 2, \ldots, N),$$

where $X[i]$ ($X = E_y, \mathbf{H}$) represents the field at the ith cell occupied by the device.

To solve (4) explicitly, we approximate the voltage dependence of the device current by a piecewise-linear function. The key is the fact that $E_y^n[i]$ is solved by hand in (4), when

$I_L^{n-1/2}$ is a linear function of the arguments. Setting $I_j \equiv I_L(V_j)$ for M different voltages V_j, ($j = 1, \ldots, M$), I_L is approximated by the following piecewise-linear function:

$$I_L(V) = \frac{I_{j+1} - I_j}{V_{j+1} - V_j}\left(V - V_j\right) + I_j, \tag{5}$$

where $V \in (V_j, V_{j+1}]$ for $j = 1, \ldots M - 1$. Substituting (5) into I_L in (4) and setting $V = \Delta y \sum_{k=1}^N E_y^n[k]$, we obtain

$$E_y^n[i] = E_y^{n-1}[i] + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}[i]\right)_y - \alpha_j \sum_{k=1}^N E_y^n[k] - \beta_j, \tag{6}$$

where

$$\alpha_j = \frac{\Delta t \Delta y}{\epsilon \Delta x \Delta z}\frac{I_{j+1} - I_j}{V_{j+1} - V_j},$$
$$\beta_j = \frac{\Delta t}{\epsilon \Delta x \Delta z}\frac{I_j V_{j+1} - I_{j+1} V_j}{V_{j+1} - V_j}. \tag{7}$$

By straightforward calculations, (6) is solved with respect to $E_y^n[i]$ to give

$$\mathbf{E}_y^n = \mathbf{A}[j]^{-1}\mathbf{S}[j], \tag{8}$$

$$A[j]_{kl} = \delta_{kl} + \alpha_j, \tag{9}$$

$$S[j]_k = E_y^{n-1}[k] + \frac{\Delta t}{\epsilon}(\nabla \times \mathbf{H}[k])_y - \beta_j, \tag{10}$$

where $\mathbf{E}_y^n$ shows the column vector $(E_y^n[1], E_y^n[2], \ldots, E_y^n[N])^T$. Moreover, $A[j]_{kl}$, ($k, l = 1, 2, \ldots, N$) and $S[j]_k$, ($k = 1, 2, \ldots, N$) show the (k, l)th entry of $\mathbf{A}[j]$ and the kth component of $\mathbf{S}[j]$, respectively. Note that $\mathbf{A}[j]^{-1}$ is obtained in a closed form as

$$A[j]_{kl}^{-1} = \delta_{kl} - \frac{\alpha_j}{1 + N\alpha_j}. \tag{11}$$

After obtaining $E_y^n[i]$ using (8), we have to check if the terminal voltage V is really in the range $(V_j, V_{j+1}]$ with $V = \Delta y \sum_{i=1}^N E_y^n[i]$. If not, the procedure is repeated with other j values, until $V \in (V_j, V_{j+1}]$. The presented diode model successfully demonstrated the wave properties traveling in an RTD transmission line [8, 9].

3. FET Model in FDTD

There are many different equivalent circuits of an FET, depending on the accuracy and the application to use. For clarity, we first consider the simplest representation: an FET is represented only by the drain-source current I_{DS} as a function of both the gate-source and drain-source voltages. Then, an extended Ampere's law is given by

$$E_y^n = E_y^{n-1} + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}\right)_y$$
$$- \frac{\Delta t}{\epsilon \Delta x \Delta z} I_{DS}^{n-1/2}(V_{GS}, V_{DS}), \tag{12}$$
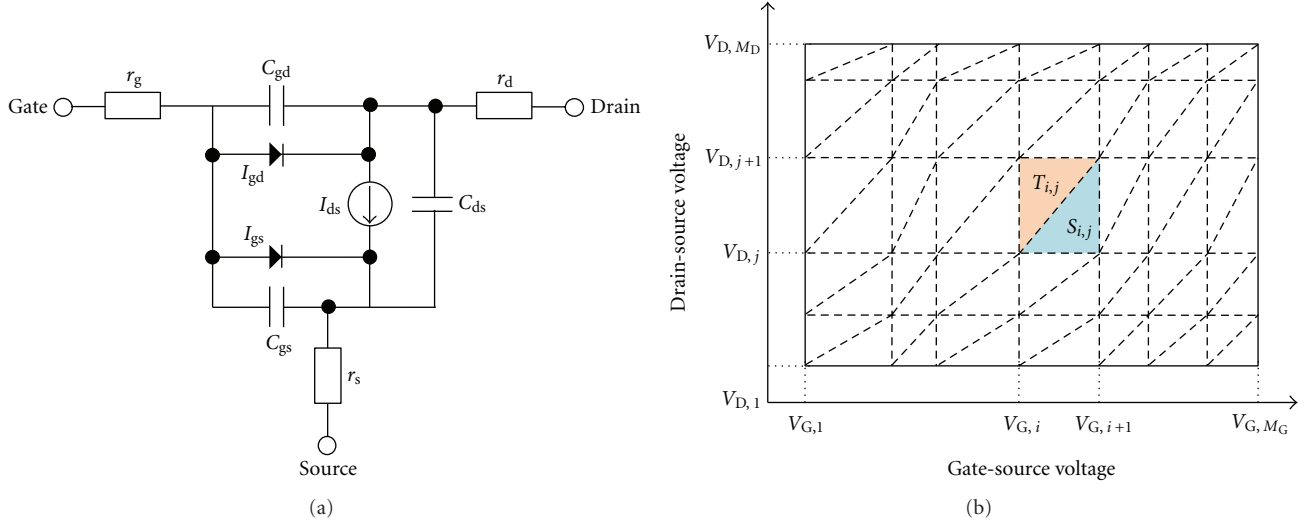
(a)

(b)

FIGURE 1: FET model in FDTD. (a) The Statz model and (b) A triangulation of $V_{GS} - V_{DS}$ plane.

where V_{GS} and V_{DS} represent the gate-source and drain-source voltages, respectively. Again, the current is assumed to flow in the y direction. The adjacent M_D cells are used for calculating V_{DS}. Moreover, the electrical field components used for V_{DS} are denoted by $E_y[1], \ldots, E_y[M_D]$. The difference equations to be solved become

$$E_y^n[i] = E_y^{n-1}[i] + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}[i]\right)_y$$
$$- \frac{\Delta t}{\epsilon \Delta x \Delta z}I_{DS}^{n-1/2}\left(V_{GS}, \Delta y \sum_{k=1}^{M_D} E_y^n[k]\right) \quad (13)$$
$$(i = 1, 2, \ldots, M_D).$$

At this point, we approximate the voltage dependence of I_{DS} by a piecewise-linear function and solve algebraically (13) with respect to $E_y^n[i]$ ($i = 1, \ldots, M_D$). The procedure is similar to the above-mentioned diode case, except that V_{GS} must be upgraded by corresponding electrical field components at time n.

Next, we consider more practical FET models shown in Figure 1(a), called the Statz model [10]. The model takes the gate-source, gate-drain currents together with the drain-source current into consideration. Moreover, the parasitic resistances and capacitances are also modeled. The device current-voltage relationships are given by

$$I_G^{n-1/2} = \frac{-r_s\left(V_{DS}^n - x_{ds}^n\right) + (r_s + r_d)\left(V_{GS}^n - x_{gs}^n\right)}{r_g r_s + r_s r_d + r_d r_g},$$
$$I_D^{n-1/2} = \frac{\left(r_s + r_g\right)\left(V_{DS}^n - x_{ds}^n\right) - r_s\left(V_{GS}^n - x_{gs}^n\right)}{r_g r_s + r_s r_d + r_d r_g}, \quad (14)$$
$$I_S^{n-1/2} = I_G^{n-1/2} + I_D^{n-1/2},$$

where I_G, I_D, and I_S represent the gate, drain, and source currents, respectively. The auxiliary voltage variables x_{gs} and

x_{ds} are solved with respect to V_{GS} and V_{DS} by the following expressions resulting from Kirchhoff's law:

$$I_S^{n-1/2} = I_{DS}\left(x_{gs}^n, x_{ds}^n\right) + C_{DS}\frac{x_{ds}^n - x_{ds}^{n-1}}{\Delta t} + I_{GS}\left(x_{gs}^n\right)$$
$$+ C_{GS}\left(x_{gs}^n\right)\frac{x_{gs}^n - x_{gs}^{n-1}}{\Delta t},$$
$$I_D^{n-1/2} = I_{DS}\left(x_{gs}^n, x_{ds}^n\right) + C_{DS}\frac{x_{ds}^n - x_{ds}^{n-1}}{\Delta t} - I_{GD}\left(x_{gs}^n, x_{ds}^n\right)$$
$$+ C_{GD}\left(x_{gs}^n, x_{ds}^n\right)\frac{x_{ds}^n - x_{gs}^n - x_{ds}^{n-1} + x_{gs}^{n-1}}{\Delta t}.$$
$$(15)$$

For definiteness, we assume that the adjacent M_G cells are used to evaluate V_{GS} and adjacent M_D cells are for V_{DS}. Moreover, the gate and drain currents are assumed to flow the former M_G and the latter M_D cells, respectively. Then, we denote the electrical field components used for V_{GS} as $E_y[1], \ldots, E_y[M_G]$, and the symbols $E_y[M_G+1], \ldots, E_y[M_G+M_D]$ are reserved for those representing V_{DS}. The difference equations to be solved become

$$E_y^n[i] = E_y^{n-1}[i] + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}[i]\right)_y$$
$$- \frac{\Delta t}{\epsilon \Delta x \Delta z}I_X^{n-1/2}(V_{GS}, V_{DS}), \quad (16)$$

where I_X represents $I_G(I_D)$ for $i = 1, \ldots, M_G$ ($i = M_G + 1, \ldots, M_G + M_D$).

To obtain a piecewise-linear function that approximates the device currents, we triangulate the $V_{GS} - V_{DS}$ plane. For the present device currents, a simple triangulation shown in Figure 1(b) suffices. Setting $I_{G(D),i,j} \equiv I_{G(D)}(V_{GS,i}, V_{DS,j})$ for

$M_G \times M_D$ different voltages $(V_{GS,i}, V_{DS,j})$, $(i = 1, \ldots, M_G, j = 1, \ldots, M_D)$, I_X $(X = G, D)$ is approximated by the following piecewise-linear function for $(V_{GS}, V_{DS}) \in S_{i,j}$ in Figure 1(b):

$$I_X(V_{GS}, V_{DS}) = \frac{I_{X,i+1,j} - I_{X,i,j}}{V_{GS,i+1} - V_{GS,i}}(V_{GS} - V_{GS,i})$$

$$+ \frac{I_{X,i,j+1} - I_{X,i,j}}{V_{DS,j+1} - V_{DS,j}}\left(V_{DS} - V_{DS,j+1}\right) \quad (17)$$

$$+ I_{X,i,j+1}.$$

On the other hand, for $(V_{GS}, V_{DS}) \in T_{i,j}$ in Figure 1(b), it is

$$I_X(V_{GS}, V_{DS}) = \frac{I_{X,i+1,j} - I_{X,i,j}}{V_{GS,i+1} - V_{GS,i}}(V_{GS} - V_{GS,i+1})$$

$$+ \frac{I_{X,i,j+1} - I_{X,i,j}}{V_{DS,j+1} - V_{DS,j}}\left(V_{DS} - V_{DS,j}\right) + I_{X,i+1,j}.$$

$$(18)$$

Hereafter, we denote the piecewise-linear counterparts of $I_{D(G)}$ as $I_{D(G)} = a_{D(G),ij}V_{GS} + b_{D(G),ij}V_{DS} + c_{D(G),ij}$ for convenience. Substituting them into $I_{D,G}$ in (16), we obtain

$$E_y^n[i] = E_y^{n-1}[i] + \frac{\Delta t}{\epsilon}\left(\nabla \times \mathbf{H}^{n-1/2}[i]\right)_y - \frac{\Delta t}{\epsilon \Delta x \Delta z}$$

$$\times \left(a_{X,jk}\Delta y \sum_{l=1}^{M_G} E_y^n[l] + b_{X,jk}\Delta y \sum_{l=M_G}^{M_G+M_D} E_y^n[l] + c_{X,jk}\right),$$

$$(19)$$

where X has to set to G and D for $i = [1, \ldots, M_G]$ and $i = M_G + 1, \ldots, M_G + M_D$, respectively.

We again obtain the column vector $\mathbf{E}_y^n = (E_y^n[1], \ldots, E_y^n[M_G], E_y^n[M_G+1], \ldots, E_y^n[M_G+M_D])^T$ in the form of $\mathbf{E}_y^n = \mathbf{A}[jk]^{-1}\mathbf{S}[jk]$. The lth component of $\mathbf{S}[jk]$ is given by

$$S[jk]_l = E_y^{n-1}[l] + \frac{\Delta t}{\epsilon}(\nabla \times \mathbf{H}[l])_y - \gamma_{X,jk}, \quad (20)$$

where $\gamma_{X,jk}$ represents $c_{G,jk}\,\Delta t/\epsilon\Delta x\Delta z$ for $i = 1, \ldots, M_G$, and $c_{D,jk}\,\Delta t/\epsilon\,\Delta x\,\Delta z$ for $i = M_G+1, \ldots, M_G+M_D$. Moreover, the matrix $\mathbf{A}[jk]$ is given by

$$A[jk]_{lm}$$

$$= \begin{cases} \delta_{lm} + \alpha_{G,jk}, & (l, m) \in [1, M_G], \\ \delta_{lm} + \beta_{D,jk}, & (l, m) \in [M_G + 1, M_G + M_D], \\ \beta_{G,jk}, & l \in [1, M_G], \ m \in [M_G + 1, M_G + M_D], \\ \alpha_{D,jk}, & l \in [M_G + 1, M_G + M_D], \ m \in [1, M_G], \end{cases}$$

$$(21)$$

where $\alpha_{G,D,jk} \equiv a_{G,D,jk}\Delta t\Delta y/\epsilon\Delta x\Delta z$ and $\beta_{G,D,jk} \equiv b_{G,D,jk}\Delta t\Delta y/\epsilon\Delta x\Delta z$. For the present case, $\mathbf{A}[jk]^{-1}$ is explicitly given as

$$h_{lm}A[jk]_{lm}^{-1} = \begin{cases} \left[\left(1 + M_D\beta_{D,jk}\right)\left(1 + M_G\alpha_{G,jk}\right) - M_G M_D \alpha_{D,jk}\beta_{G,jk}\right]\delta_{lm} \\ \quad -\left(1 + M_D\beta_{D,jk}\right)\alpha_{G,jk} + M_D\beta_{G,jk}\alpha_{D,jk}, & (l, m) \in [1, M_G], \\ \left[\left(1 + M_D\beta_{D,jk}\right)\left(1 + M_G\alpha_{G,jk}\right) - M_G M_D \alpha_{D,jk}\beta_{G,jk}\right]\delta_{lm} \\ \quad -\left(1 + M_G\alpha_{G,jk}\right)\beta_{D,jk} + M_G\alpha_{D,jk}\beta_{G,jk}, & (l, m) \in [M_G + 1, M_G + M_D], \\ -\beta_{G,jk}, & l \in [1, M_G], \ m \in [M_G + 1, M_G + M_D], \\ -\alpha_{D,jk}, & l \in [M_G + 1, M_G + M_D], \ m \in [1, M_G], \end{cases}$$

$$(22)$$

where $h_{lm} = (1 + M_D\beta_{D,lm})(1 + M_G\alpha_{G,lm}) - M_G M_D \beta_{G,lm}\alpha_{D,lm}$. After obtaining $E_y^n[i]$, we have to check if the terminal voltages V_{GS} and V_{DS} are really in the range we presume. Otherwise, the procedure is repeated with coefficients corresponding to another triangularized regions in $V_{GS} - V_{DS}$ plane. Moreover, when the device model includes capacitors such as C_{GS} and C_{GD}, these terminal voltages must be recorded, which are required for evaluating x_{ds}^{n-1} and x_{gs}^{n-1} in (15).

In the following, we demonstrate the pulse shortening in TWFETs by FDTD calculations. Although the line structure we set up is rather impractical, we successfully observed the shortening of the pulse traveling along a TWFET. It is observed, only when the nonlinear operations of a large amount of FETs are properly simulated. We thus believe that this example calculation clarifies the validity of our models. Before showing calculation results, we briefly review the mechanism of the pulse shortening in TWFETs.

4. Pulse Shortening in TWFETs

Figure 2(a) shows the equivalent representation of a TWFET. One end of each electrode line labeled as $V_{gin}(V_{din})$ is for signal applications. Figure 2(b) shows the required pulse
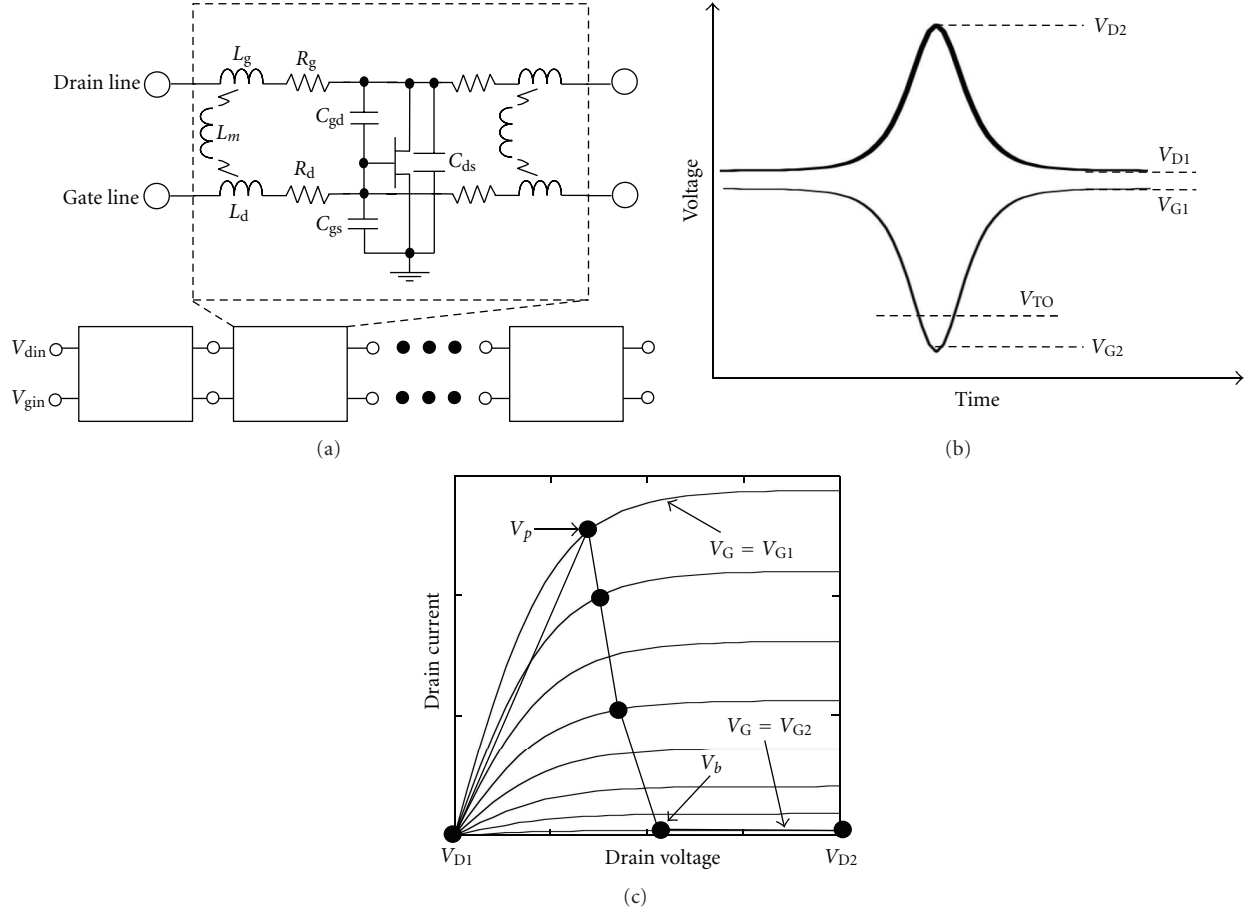
(a)

(b)

(c)

FIGURE 2: Setup of TWFETs for shortening traveling pulses. (a) A representation of a TWFET, (b) the signal application to a TWFET and (c) the equivalent current-voltage relationship of an FET for a pulse traveling in the drain line.

shapes applied at $V_{gin}(V_{din})$. The voltages biasing the gate and drain lines are denoted by V_{G1} and V_{D1}, respectively. The drain pulse has the opposite parity to the gate pulse. Moreover, the top and bottom voltage levels of the drain (gate) pulse are set to V_{D2} (V_{G1}) and V_{D1} (V_{G2}), respectively. At this point, V_{G2} is set below the FET threshold voltage V_{TO}, and both of V_{D1} and V_{G1} are set to approximately 0 V. The thin curves in Figure 2(c) show the drain current-voltage relationships for several different gate bias voltages. The uppermost and lowermost curves correspond to the relationships for V_{G1} and V_{G2}, respectively. Because of the presence of electromagnetic couplings between the gate and drain lines, two different propagation modes, called the c mode and the π mode [11], are developed on a TWFET. We can design a TWFET to amplify only the pulses carried by one of the two modes and attenuate the pulses carried by the other mode [4]. The conditions are given by simple inequalities using three variables u_s, u_c, and u_π defined as

$$u_s = \sqrt{\frac{L_m}{C_{gd}\left(L_g L_d - L_m^2\right)}}$$

$$u_{c,\pi} = \sqrt{\frac{X_1 \pm \sqrt{X_1^2 - 2X_2}}{X_2}},$$

(23)

where the upper (lower) signs are for c (π) mode. Moreover, we used two variables $X_{1,2}$ for brevity: $X_1 = C_{gs}L_g + C_{ds}L_d + C_{gd}(L_g + L_d) - 2C_{gd}L_m$ and $X_2 = 2(C_{gs}C_{ds} + C_{gs}C_{gd} + C_{ds}C_{gd})(L_g L_d - L_m^2)$. It is then found that the c-mode pulse is generically amplified when $u_s > u_c$, while the π-mode pulse is amplified when $u_s < u_\pi$. Because u_c is always greater than u_π, we can see that when the characteristic velocity u_s is less than both u_c and u_π, the slower mode is the unique amplified mode; in contrast, when u_s is greater than both u_c and u_π, the faster mode is the unique amplified mode.

When the TWFET succeeds in amplifying the unique mode, we can assume the simultaneous propagation of the leading edges of the gate and drain pulses. At this point, every FET operates as an electronic switch that is open for $V_{din} > V_b$, and closed for $V_{din} < V_p$ as shown in Figure 2(c). As a result, the pulse is influenced by finite shunt conductance for voltages less than V_p and is otherwise loss-free. Owing to this nonlinearity, a short-wavelength sinusoidal wave supported
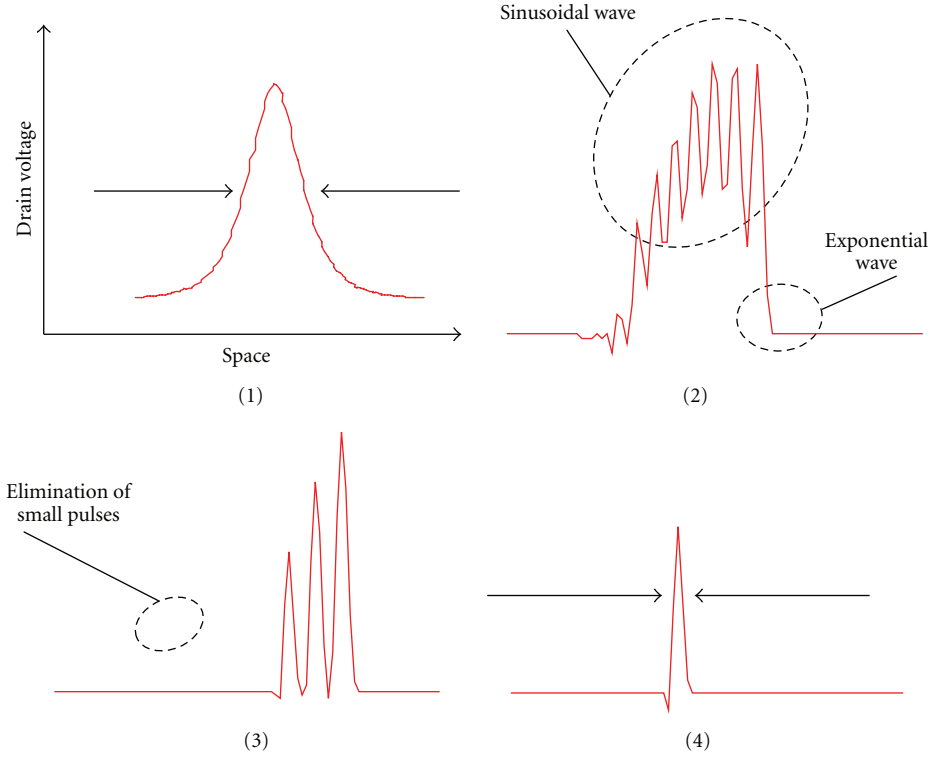
FIGURE 3: Operation principle of pulse shortening in TWFETs.

by an exponential edge develops [4]. **Figure 3** schematically explains the mechanism of pulse-shortening phenomena. When a pulse of width l_{init} is input to the drain line ((1) of **Figure 3**), the above-mentioned short-wavelength sinusoidal wave is shown in (2). Because the drain line attenuates voltage waves only below V_{p}, the small-amplitude parts of the wave disappear with the shorter propagation than the large-amplitude ones ((3) in **Figure 3**). Finally, a short pulse is obtained at the output ((4) in **Figure 3**).

5. Demonstration of Pulse Shortening in TWFETs

Three-dimensional FDTD calculations were carried out for demonstrating nonlinear pulse propagation along a TWFET. The total number of cells was $400 \times 150 \times 100$. The spatial increments in the x, y, and z orientations were set to 10, 2, and 10 μm, respectively. The calculation setup is illustrated in **Figure 4(a)**. The gate and drain lines were aligned in the x direction. At one of the ends of the lines, the inputs were applied with the hyperbolic secant pulses with the opposite parity. To maximize the coupling between the gate and drain lines, the spacing between two lines was set small and no ground plane was placed except the source. The dielectric constant of the substrate was set to 13.6. Moreover, a Mur's 2nd-order absorbing boundary condition (ABC) was employed. FETs are placed every 30 μm along the electrode

lines, whose widths were all set to 10 μm. Each FET was modeled as the drain-source current I_{DS}:

$$I_{\text{DS}}(V_{\text{GS}}, V_{\text{DS}})$$
$$= \begin{cases} \beta(V_{\text{GS}} - V_{\text{TO}})^2 \tanh(\alpha V_{\text{DS}}), & V_{\text{GS}} > V_{\text{TO}}, \\ 0, & V_{\text{GS}} < V_{\text{TO}}, \end{cases} \tag{24}$$

where we set β, V_{TO}, and α to 20.0 mA/V^2, -1.0 V, and 2.0 V^{-1}, respectively. We ignore the influences caused by the gate-source current with the parasitic capacitors and resistors for clear observations of the nonlinear properties of a TWFET. We modeled I_{DS} as a piecewise-linear function with respect to V_{DS} with 2000 segments. The cross-section of electrodes is shown in **Figure 4(b)**. For V_{GS}, we summed up the y components of the electrical fields of the nine subsequent cells connecting the gate line and the source (the cells labeled by "G" in **Figure 4(b)**). Similarly, neighboring fifteen cells were used for evaluating V_{DS} (the cells labeled by "D" in **Figure 4(b)**).

To obtain a rough estimation of the model TWFET, we carried out the quasi-TEM analysis [11]. The 2×2 capacitance matrix **C** and inductance matrix **L** are obtained by the numerical estimation of electrical charges stored in the electrode lines. By solving the Poisson equation for the case where V_{GS} and V_{DS} are set to 1.0 and 0.0 V, respectively,
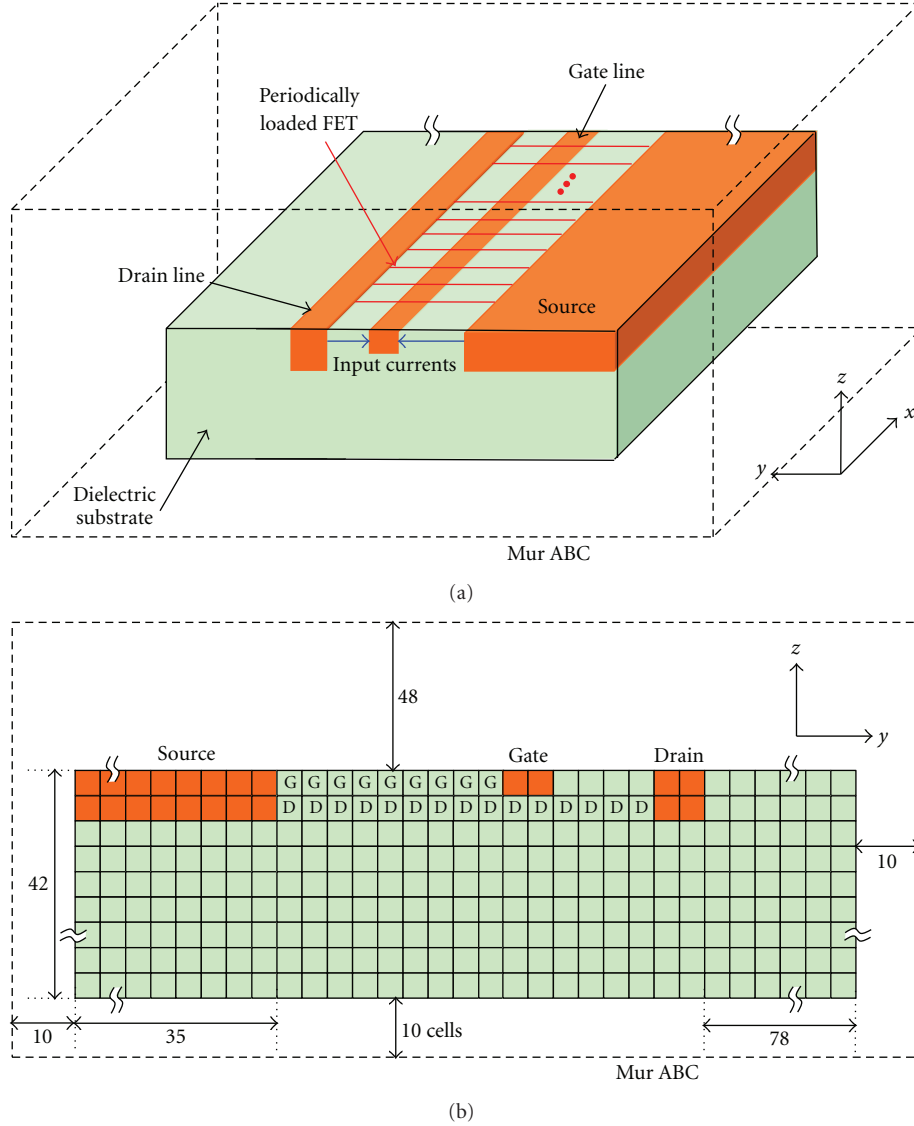
(a)

(b)

FIGURE 4: Setup of FDTD calculations. (a) The longitudinal and (b) the transverse structure of the calculated TWFET.

TABLE 1: Line parameters of test TWFET.

C_{gs}	0.10 pF/mm	L_g	0.73 nH/mm
C_{gd}	0.17 pF/mm	L_d	0.70 nH/mm
C_{ds}	0.09 pF/mm	L_m	0.42 nH/mm

we can obtain the electrical charges stored in the gate and drain lines: Q_{11} and Q_{21}. Those for the case where V_{GS} and V_{DS} are, respectively, set to 0.0 and 1.0 V, called Q_{12} and Q_{22} are similarly obtained. Then, the 2×2 matrix **Q**, whose components are given by Q_{ij} ($i, j = 1,2$), gives **C**. On the other hand, we consider the case where the electrodes are in vacuum; that is, the dielectric constant of each cell is set to unity for **L**. To obtain **L**, it is required to evaluate the capacitance matrix $\mathbf{C}_0$ in vacuum by the same procedure as obtained **C**, because **L** has to be equal to $c^{-2}\mathbf{C}_0^{-1}$ (c: the light

velocity). As a result, we obtain the line parameters as listed in Table 1. Using them, u_π and u_c are calculated to be 0.29 c and 0.32 c, respectively. Moreover, u_s satisfies the condition, $u_s < u_\pi$, so that the π-mode pulse is expected to be uniquely amplified; therefore, the pulse shortening can be observed in the one carried by the slower π mode. The black curves in Figure 5 show the results from numerical integration of the transmission equations of a TWFET using the parameters listed in Table 1. Hyperbolic secant waveforms shown in Figure 5(a) are applied. The temporal waveforms monitored at five different FET cells, each separated by twelve FET cells, are shown. The thin and thick waveforms represent the pulse on the gate and drain lines, respectively. Because the discrepancy between the c- and π-mode velocities is small, the pulse carried by the π mode is still overlapped with that carried by the c mode even in Figure 5(f). However, it is observed that the pulse carried by the slower mode
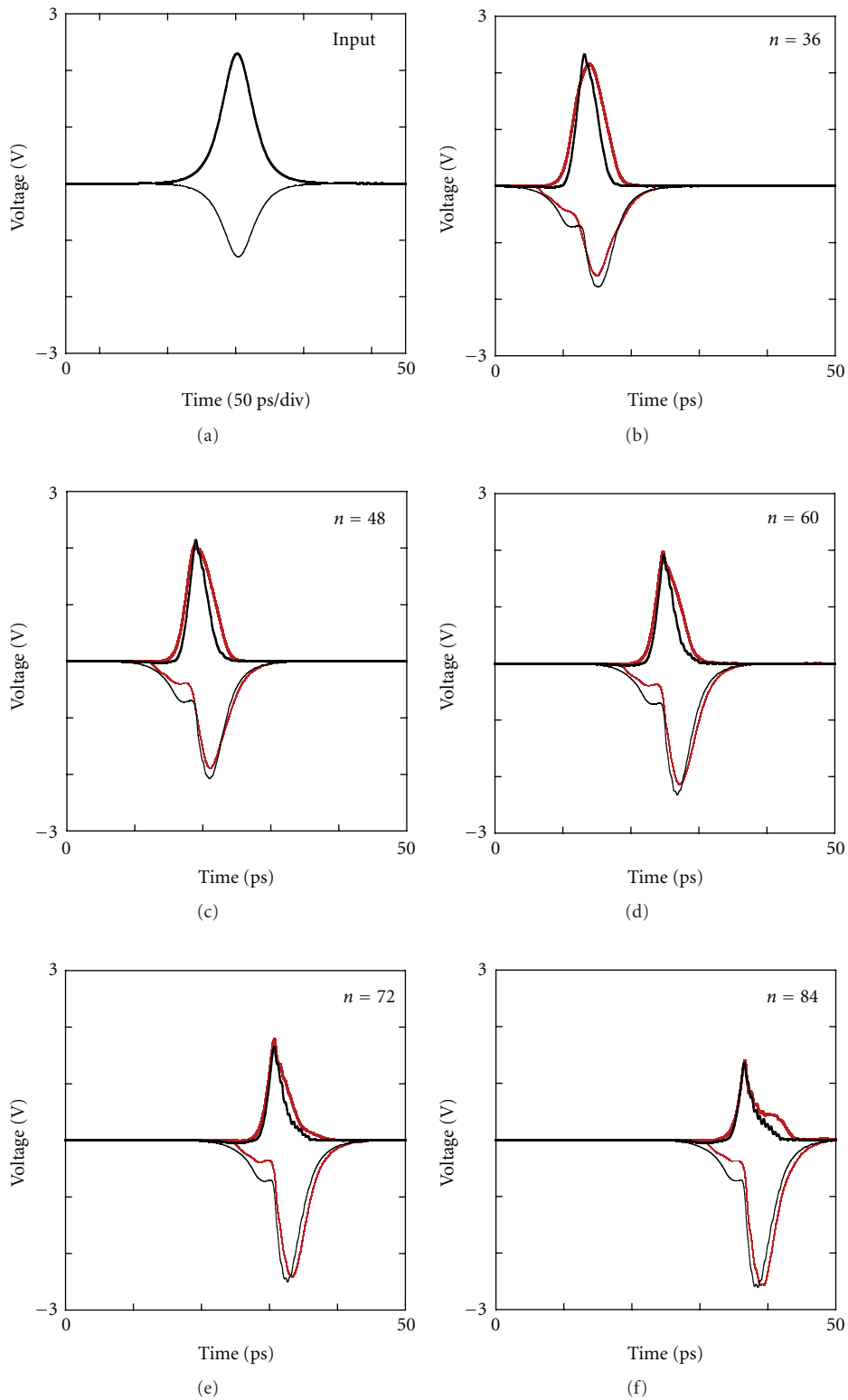
FIGURE 5: Wave propagation on test TWFET. The waveforms on the gate and drain lines are shown by the thin and thick curves, respectively. The black and red curves correspond to the quasi-TEM and FDTD calculations, respectively. (a) shows the input waveforms. Waveforms recorded at the nth FET cell are shown. (b), (c), (d), (e), and (f) represent the waveforms at n = 36, 48, 60, 72, and 84, respectively.
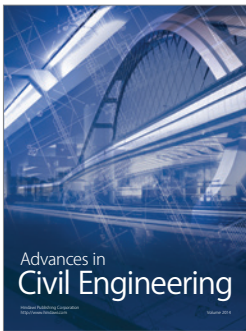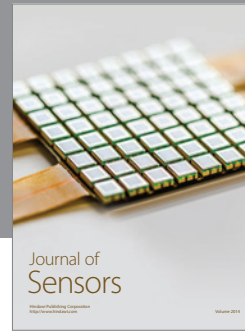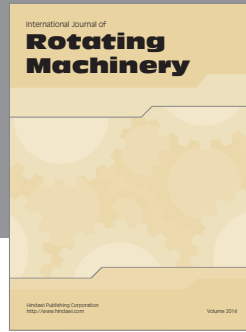
experiences shortening. On the other hand, the results from FDTD calculations are shown by the red curves in Figure 5. Five temporal waveforms are plotted and recorded at $480\,\mu$m intervals along the line in Figures 5(b)–5(f). Qualitatively, the waveform transients have good resemblance with those obtained by quasi-TEM calculations. The steep exponential edge is developed and the pulse starts to exhibit an oscillatory behavior and then is shortened. We have found that even a TWFET with practical FET properties succeeds in pulse shortening in the framework of the transmission line theory. Moreover, we experimentally confirmed the pulse shortening using actual FETs at low frequencies [12]. We believe that the FDTD calculations may contribute to the design of the monolithically integrated TWFETs as pulse compressor, when they are solved with a practical FET model.

6. Conclusions

We demonstrated full-wave calculations that illustrate the pulse propagation characteristics of a TWFET. The pulse shortening in a TWFET was properly observed in the full-wave calculations. By using piecewise-linear modeling, FETs were characterized in FDTD without significant computational costs.

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