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Silicon Carbide Junction Field Effect Transistor Integrated Circuits for Hostile Environments

By

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Abstract

Silicon carbide (SiC), in particular its 4H polytype, has long been recognised as an appropriate semiconductor for producing hostile environment electronics due to its wide energy band gap, large chemical bond strength and high mechanical hardness. A strong research foundation has facilitated the development of numerous sensor structures capable of operating at high temperatures and in corrosive atmospheres. Front-end electronics suitable for *in situ* signal conditioning are however lacking.

Junction field effect transistors (JFETs) circumvent the pitfalls of contemporary alternative SiC transistor variants and have been found to operate predictably and consistently under such extreme conditions. This thesis demonstrates for the first time the capability of producing the necessary stable and high-performance interface circuits from n-channel lateral depletion-mode (NLDM) JFETs.

The temperature dependence of pertinent bulk 4H–SiC material parameters relevant for describing the operation of macroscopic JFETs were initially studied. An accurate phenomenological model was developed to account for the variation of the thermal equilibrium free carrier concentrations. The position of the electrochemical potential and the distribution of free electron energies were found to change markedly when conduction band non-parabolicity, higher energy intrinsic bands and extrinsic effects were accounted for. These in turn were found to influence the determination of p-n junction contact potentials.

The worst case error introduced through use of the Boltzmann approximation when applied to the channel and gate regions of the JFETs under study, having nominal doping concentrations of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $2 \times 10^{19}\,\mathrm{cm}^{-3}$, respectively, were approximately $0.1\,\%$ and $2\,\%$, respectively. A set of efficient and well behaved closed form expressions were subsequently developed for the free carrier concentrations in the framework of the Joyce-Dixon approximation (JDA) which are ideally suited for use in circuit simulations.

Expressions for the electron conductively effective mass and an appropriate weighting function for the momentum relaxation time were subsequently identified. While the conductivity effective mass along the basal plane remained almost independent of temperature the non-parabolic band dispersion in the direction of principle axis introduced a temperature variation of 19% and 21% between 25 °C and 400 °C in the first and second conduction bands, respectively.

Monolithically integrated 4H–SiC signal-level homo-epitaxial NLDM JFETs, p-n junction diodes and resistors were electrically characterised between room temperature and 400 °C and their static and dynamic properties studied. Their behaviours were found to be well represented by macroscopic drift-diffusion models and were in agreement with predictions based on the bulk material properties. The intrinsic voltage gain of the fabricated JFET structures with nominal 9 µm gate length, 300 nm channel depth and 250 µm gate width, under typical bias conditions, was roughly 100. As a consequence of the finite doping concentration in the buffer layer beneath the active device channel, with an experimentally

determined value of approximately $3 \times 10^{15}\,\mathrm{cm}^{-3}$, the devices under study were found to exhibit a strong body-effect.

The thermal performance of the utilised tungsten capped annealed nickel-titanium and aluminium-titanium contacts, on highly doped n- and p-type regions, respectively, were investigated and appropriate methods for their characterisation described. The lowest recorded value of specific contact resistance was $1.90(50) \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ with a corresponding sheet resistance of $7.89(9) \times 10^2\,\Omega/\square$. Lateral current flow through the contact side wall and the difference in sheet resistance under the contact were found to increase the value of the specific contact resistance determined from transfer length method (TLM) test structures by as much as 10% for n-type contacts. While exhibiting much larger contact resistance, the p-type contacts were found to have negligible impact on device performance due to the high impedance of the gate-channel and body-channel p-n junctions under typical operation.

Physics based, Simulation Program with Integrated Circuit Emphasis (SPICE) compatible, integrated circuit (IC) consistent compact models were developed that are congruent with experimental measurements over the aforementioned range of temperature and across all essential bias levels. Most notably, a self-contained, asymmetric double-gated, non-self-aligned JFET model was developed that accurately accounts for the body-effect, voltage dependent mobility and temperature. An accurate yet efficient solver of the charge neutrality equation within each region of the device is utilised to account for incomplete ionisation of dopants and the temperature dependence of the p-n junction contact potentials. Meticulous agreement with experimental measurements was attained from a minimal number of input parameters.

The modelled devices were used to simulate pertinent IC building blocks, including single stage and differential amplifiers, level-shifters and voltage buffers. The finite body-transconductance of active load transistors were identified as a major degrading factor for the voltage gain. Practical methods to circumvent this are discussed with the aid of appropriate small-signal equivalent models. Finally, a design was presented for a two-stage 4H–SiC operational amplifier (op-amp) with direct current (DC) stability over the entire temperature range of study. Low-frequency small-signal voltage gains of 80 dB and 70 dB were achieved at 25 °C and 400 °C, respectively when utilising a ±30 V supply. A closed-loop non-inverting op-amp configuration with an ideal gain of 11 was then simulated and found to vary by just 1 % between 25 °C and 400 °C. Such amplifiers are of great utility and form the cornerstone of numerous useful and important electronic systems.

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List of Acronyms

AC	alternating current
ADA	abrupt depletion approximation
AFM	atomic force microscopy
AJA	abrupt junction approximation
ASTRO	Active Sensor Structures for Extreme Environments
BEEM	ballistic-electron emission microscopy
BJT	bipolar junction transistor
CD	common drain
CG	common gate
CLM	channel length modulation
CMRR	common-mode rejection ratio
CR	cyclotron resonance
CS	common source
CV	capacitance-voltage
CWRU	Case Western Reserve University
DC	direct current
DFT	density functional theory
DM	depletion mode
DOS	density of states
ECSCRM	European Conference on Silicon Carbide and Related Materials
EDA	electronic design automation
EPR	electron paramagnetic resonance
ETM	Emerging Technologies and Materials
expop	extrapolation pinch-off point
FET	field effect transistor
GCA	gradual channel approximation
GRC	Glenn Research Center

LIST OF ACRONYMS

IC	integrated circuit
ICSCRM	International Conference on Silicon Carbide and Related Materials
JDA	Joyce-Dixon approximation
JFET	junction field effect transistor
LDA	local density approximation
LMA	Levenberg-Marquardt algorithm
LOPC	longitudinal optical phonon plasma-coupled
MESFET	metal-semiconductor field effect transistor
MIS	metal-insulator-semiconductor
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field effect transistor
NASA	National Aeronautics and Space Administration
NLDM	n-channel lateral depletion-mode
NMR	nuclear magnetic resonance
NR	Newton-Raphson
NU	Newcastle University
ODCR	optically detected cyclotron resonance
OP	operating point
op-amp	operational amplifier
PSRR	power supply rejection ratio
RIE	reactive ion etching
RMS	root mean square
RTA	rapid thermal anneal
SI	semi-insulating
SIMS	secondary ion mass spectroscopy
SNR	signal-to-noise ratio
SOI	silicon-on-insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SRH	Shockley-Read-Hall
SRIM	Stopping Range of Ions in Matter
TCAD	technology computer aided design
tempco	temperature coefficient
TFE	thermionic field emission
THD	total harmonic distortion
TLM	transfer length method
VCCS	voltage-controlled current-source
VCVS	voltage-controlled voltage-source

VTC	voltage transfer characteristic
WKB	Wentzel-Kramers-Brillouin

List of Symbols

A	first-order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameter cross-sectional area closed-loop gain
A^{**}	effective Richardson constant
a'_0	effective Bohr radius
a	direct lattice constant device channel depth
$\boldsymbol{a}$	direct lattice primitive vector
a^*	reciprocal lattice constant
$\boldsymbol{a}^*$	reciprocal lattice primitive vector
A_{i}	small-signal current gain
A_{is}	small-signal short-circuit current gain
A_{o}	open-loop gain
A_{v}	small-signal voltage gain
A_{vc}	small signal common-mode voltage gain
A_{vd}	small-signal differential voltage gain
A_{vo}	small-signal open-circuit voltage gain
B	feedback gain
b	undepleted device channel depth
C	capacitance
c	direct lattice constant first-order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameter
$\boldsymbol{c}$	direct lattice primitive vector
c^*	reciprocal lattice constant
$\boldsymbol{c}^*$	reciprocal lattice primitive vector
C_{bd}	body-drain capacitance
C_{bs}	body-source capacitance

C_d	diffusion capacitance
C_gd	gate-drain capacitance
C_gs	gate-source capacitance
C_j	depletion capacitance
$C_\mathrm{j,0}$	depletion capacitance at zero bias
D	diffusion coefficient
d	contact separation
E	energy
e	elementary charge
E_{00}	characteristic energy
E_a	acceptor level
E_b	impurity energy bandwidth
E_c	conduction band minimum
E_cf	crystal-field interaction
E_d	donor level
E_F	Fermi-level
E_g	fundamental band gap
E_so	spin-orbit interaction
E_v	valence band maximum
E_vo	valley-orbit interaction
F	Fermi transform Gaussian weighting function
f	linear frequency distribution function
f_0	Fermi-Dirac distribution function
f_i	modified Fermi-Dirac distribution function
G	standard deviation
$\boldsymbol{G}$	reciprocal lattice translation vector
g	Joyce-Dixon coefficient small-signal conductance
g_bd	small-signal body-drain conductance
g_bs	small-signal body-source conductance
g_ds	small-signal drain-source conductance
g_gd	small-signal gate-drain conductance
g_gs	small-signal gate-source conductance
G_m	small-signal short-circuit transconductance
g_m	small-signal transconductance

g_{mb}	small-signal body-transconductance
h	local hexagonal environment
h	Miller index Planck constant
$\hbar$	reduced Planck constant
i_{BD}	instantaneous body-drain current
i_{bd}	body-drain signal current
i_{BS}	instantaneous body-source current
i_{bs}	body-source signal current
i_{D}	instantaneous drain current
i_{d}	drain signal current
I_{DS}	drain-source bias current
i_{DS}	instantaneous drain-source current
i_{ds}	drain-source signal current
i_{DSS}	instantaneous drain-source current with gate-source short
I_{eff}	vertical current flow into contact
i_{G}	instantaneous gate current
i_{GD}	instantaneous gate-drain current
i_{gd}	gate-drain signal current
i_{GS}	instantaneous gate-source current
i_{gs}	gate-source signal current
I_{I}	input bias current
i_{I}	instantaneous input current
i_{i}	input signal current
i_{O}	instantaneous output current
I_{O}	output bias current
i_{o}	output signal current
I_{s}	ideal diode reverse saturation current
$\boldsymbol{J}, J$	electric current density
K	compensation ratio
k	local cubic environment
k	Miller index wave number
$\boldsymbol{k}$	wave vector
k_{B}	Boltzmann constant
L	device channel length contact length carrier diffusion length

l	Miller index
	direction cosine
L_T	transfer length
m^*	effective mass
M_c	number of equivalent conduction bands
m_e	electron rest mass
m_e^c	conduction band conductivity effective mass
m_e^d	conduction band density of states effective mass
m_h^c	valence band conductivity effective mass
m_h^d	valence band density of states effective mass
m^t	tunnelling effective mass
N	intrinsic density of states
n	conduction band electron concentration
n_0	equilibrium conduction band electron concentration
N_a	active acceptor concentration
	net acceptor concentration in gate epilayer
N_a^-	ionised acceptor concentration
N_b	net acceptor concentration in body epilayer
N_c	conduction band effective density of states
N_d	active donor concentration
	net donor concentration in channel epilayer
N_d^+	ionised donor concentration
n_I	apparent intrinsic carrier concentration
n_i	intrinsic carrier concentration
n_{n0}	n-region equilibrium conduction band electron concentration
N_v	valence band effective density of states
p	valence band hole concentration
p_0	equilibrium valence band hole concentration
p_{p0}	p-region equilibrium valence band hole concentration
q_{BD}	instantaneous body-drain charge
q_{bd}	body-drain signal charge
q_{BS}	instantaneous body-source charge
q_{bs}	body-source signal charge
q_{GD}	instantaneous gate-drain charge
q_{gd}	gate-drain signal charge
q_{GS}	instantaneous gate-source charge
q_{gs}	gate-source signal charge

$\boldsymbol{r}$	direct–space vector
R	resistance impurity separation
$\boldsymbol{R}$	direct lattice translation vector
R_{B}	static body series resistance
r_{b}	dynamic body series resistance
R_{bulk}	semiconductor bulk resistance
R_{c}	contact front resistance
R_{D}	static drain series resistance
r_{d}	dynamic drain series resistance
R_{G}	static gate series resistance
r_{g}	dynamic gate series resistance
R_{i}	static input resistance
r_{i}	dynamic input resistance
R_{imp}	implanted epilayer resistance
R_{l}	load resistance
R_{m}	small-signal open-circuit transresistance
R_{o}	static output resistance
r_{o}	dynamic output resistance
R_{pn}	p-n junction depletion resistance
R_{S}	static source series resistance
r_{s}	dynamic source series resistance
R_{sh}	sheet resistance
R_{sk}	sheet resistance under contact
R_{sw}	contact side wall resistance
R_{tot}	total resistance
T	temperature
t	time contact sidewall thickness
T_{n}	nominal temperature
u	Miller index
V	potential difference electrostatic potential energy
$\boldsymbol{v}$	velocity
v	Miller index velocity
V_{b}	p-n junction reverse bias breakdown voltage
v_{BD}	instantaneous body-drain voltage

v_{bd} body-drain signal voltage
V_{BS} body-source bias voltage
v_{BS} instantaneous body-source voltage
v_{bs} body-source signal voltage
$v_{\mathrm{BS,off}}$ device turn-off body voltage
v_{D} instantaneous drain voltage
v_{d} drift velocity
drain signal voltage
V_{DD} positive DC supply voltage
V_{DS} drain-source bias voltage
v_{DS} instantaneous drain-source voltage
v_{ds} drain-source signal voltage
$v_{\mathrm{d,sat}}$ saturation drift velocity
$v_{\mathrm{DS,sat}}$ expop drain-source voltage
v_{g} gate signal voltage
v_{GD} instantaneous gate-drain voltage
v_{gd} gate-drain signal voltage
V_{GG} gate bias DC supply voltage
V_{GS} gate-source bias voltage
v_{GS} instantaneous gate-source voltage
v_{gs} gate-source signal voltage
$v_{\mathrm{GS,off}}$ device turn-off gate voltage
V_{I} input bias voltage
v_{I} instantaneous input voltage
v_{i} input signal voltage
v_{ic} common-mode input signal voltage
v_{id} differential input signal voltage
V_{O} output bias voltage
v_{O} instantaneous output voltage
v_{o} output signal voltage
v_{od} differential output signal voltage
V_{SS} negative DC supply voltage
W mesa width
w Miller index
W_{n} n-region depletion width
W_{p} p-region depletion width
$\hat{x}_{\mathrm{d}}$ relative non-self alignment length between channel and drain

$\hat{x}_{\mathrm{s}}$	relative non-self alignment length between channel and source
$\hat{y}_{\mathrm{ds}}$	relative epilayer depth either side of channel
Z	device channel width contact width impedance
$\boldsymbol{\mathscr{E}}$, $\mathscr{E}$	electric field
$\mathscr{E}_{\mathrm{c}}$	critical electric field
$\mathscr{F}$	Fermi integral
$\mathscr{G}$	normalised Joyce-Dixon coefficient
$\mathscr{L}$	Laplace transform
ϕ_{p}	channel pinch-off voltage
α	normalised first order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameter fitting parameter
β	inverse electron wave function degeneracy factor fitting parameter
χ	expop smoothing factor
δ	modified Dirac delta function difference between contact and mesa width
ε_{s}	semiconductor permittivity
ϵ	normalised energy
ϵ_{a}	normalised acceptor level
ϵ_{b}	normalised impurity energy bandwidth
ϵ_{c}	normalised conduction band minimum
ϵ_{d}	normalised donor level
ϵ_{F}	normalised Fermi energy
ϵ_{v}	normalised valence band maximum
η	Miller-Bravais index
γ	normalised standard deviation channel length modulation coefficient
ι	Miller-Bravais index
κ	Miller-Bravais index effective wave number
$\boldsymbol{\kappa}$	effective wave vector
λ	Miller-Bravais index wavelength screening length channel length modulation coefficient
λ_{e}	electron screening length

λ_h	hole screening length
λ_i	impurity screening length
μ_e	electron drift mobility
$\mu_\mathrm{e,0}$	low-field drift mobility
μ_H	Hall mobility
ν	Miller-Bravais index normalised electric potential energy
Ω	direct–space volume
ω	Miller-Bravais index
ϕ	electric potential
ϕ_0	contact potential
ϕ_B	barrier height potential
ϕ_b	bottom-gate junction potential at source end of channel
ϕ_g	band gap voltage
ϕ_T	thermal voltage
ϕ_t	top-gate junction potential at source end of channel
ρ	electrical resistivity volume charge density normalised impurity separation distance
ρ_c	specific contact resistance
σ	electrical conductivity
τ	Miller-Bravais index
τ_m	momentum relaxation time
υ	Miller-Bravais index
Ξ	electric field dependent mobility

CHAPTER 1

Introduction

The development of resilient sensors will not only facilitate existing hostile environment monitoring schemes but will enable deployment within regions that conventional technologies would otherwise be impractical or impossible to be implemented. Self-contained circuitry will reduce the need for remote electronics, coolant systems and shielding. This will allow for a reduction in system size, weight and complexity and eliminate potential failure mechanisms. Envisaged applications for such systems include process control in high-temperature manufacturing and energy-production industries, such as in nuclear installations and deep well drilling; detection of gas species within combustion engines, in order to improve fuel efficiency and reduce harmful emissions; monitoring of active volcanoes, allowing for real time tracking and provision of early warning systems; for medical and ecological electronics, where chemical inactivity is paramount; and in the exploration of extra terrestrial planets, where weight and reliability are pivotal [1, 2].

The maturity of growth and processing techniques are primary limits for any device technology. Si integrated circuit (IC) technologies are highly mature; unfortunately, even silicon-on-insulator (SOI) devices remain unsuitable at temperatures exceeding 300 °C, under high radiation dose and within chemically aggressive surroundings [2–4]. Conversely, SiC exhibits relatively strong atomic bonding, high chemical inertness and excellent radiation resilience. Additionally, it possesses excellent mechanical properties, including a Mohs hardness of 9* and a wear resistance of 9.15.† While comparatively immature, it is by far the most advanced contemporary wide band gap semiconductor technology. While other emerging technologies, such as group–III nitrides and diamond, profess comparable or improved performance [5] these are presently less attractive due to cost metrics, growth challenges, process limitations and reduced thermal stability [4]. Further advantages of using SiC are that it can be processed with existing IC tools and that is has SiO_2 as a native oxide.

SiC has received significant attention from power electronic device designers due to its high breakdown electric field, thermal conductivity and carrier saturation velocity, enabling increased power densities and allowing for a considerable reduction in the size and weight of electronic systems [5]. Its prevalence within the field of hostile environment electronics continues to grow alongside the emergence of higher quality commercial wafers and an ex-

*Comparative to 10 for diamond

†Favourable to Al_2O_3 having a value of 9.00.

panding research foundation; however, significant investigation is still demanded in order to achieve long term stability of devices and optimisation of circuits.

SiC bipolar junction transistors (BJTs) have recently been realised [6]. However, being minority carrier devices they are less predicable at high temperatures and under radiation exposure, necessitate low resistance contacts to all terminals and require high quality emitter junction passivation [4]. Additionally, incomplete ionisation of dopants, particularly in the p-type base region of a n-p-n transistor, can cause significant variation in current gain with temperature [6, 7].

Despite great efforts, the present quality of SiO_2 on and its interface with SiC results in undesirably high concentrations of fixed oxide charge and interface states, causing a reduction of inversion layer mobility and threshold voltage instability in metal-oxide-semiconductor field effect transistors (MOSFETs) [5]. The best reported* field effect mobilities fall short of $200\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, with the majority below $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Additionally, the wide band gap of SiC results in lower potential barriers with SiO_2 for both electrons and holes, significantly increasing the leakage current through the oxide film compared with Si metal-oxide-semiconductor (MOS) variants [5].

Excessive thermionic emission also restricts the usefulness of SiC metal-semiconductor field effect transistors (MESFETs), limiting their operating temperatures to below 400 °C [3]. Additionally, thermal degradation of the gate contact metallisation makes it a poor choice for long term use at elevated temperatures [4].

SiC junction field effect transistors (JFETs) offer the most promising near term solution for producing stable harsh environment electronics and benefit from a strong existing research foundation [4, 8]. Current flow involves predominantly majority carriers with the positive consequences of maintaining performance and stability across a wide temperature range and remaining relatively insensitive to radiation [9,10]. The p-n junction also provides excellent electrical isolation from the gate and substrate regions with considerable opportunity for forward biasing. Depletion mode (DM) device operation imposes a number of restriction on circuit topologies, although a number of techniques exist that take advantage of these constraints. Regrettably, p-channel JFETs are burdened by excessively large contact resistances, low dopant ionisation and inferior majority carrier mobilities compared to n-channel devices. Process limitation also make their inclusion very costly. For these reasons n-channel devices are the focus of this thesis.

4H-SiC metal-insulator-semiconductor (MIS) gas sensor arrays are in development within the Emerging Technologies and Materials (ETM) research group at Newcastle University. Monolithic integration of JFET amplifiers is proposed to further improve the signal-to-noise ratio (SNR), reduce interconnect parasitics, provide a smaller footprint and lower production costs [11]. Demand will be placed on circuits to accommodate an extended temperature range and detriment from exposure to radiation and harsh chemicals, while accounting for intrinsic and extrinsic material peculiarities and process variations [4].

The remainder of this thesis is organised as follows:

*Numerous reports are presented biennially at the International Conference on Silicon Carbide and Related Materials (ICSCRM) and European Conference on Silicon Carbide and Related Materials (ECSCRM) and published in their proceedings.

Chapter 2 provides a review of the current literature relating to the various aspects of interest for this project. A overview of the physical structure and electrical properties of 4H–SiC is initially presented. Pertinent experimental and theoretical data are identified and discussed. Notable areas of omission are subsequently identified. The physical operation of the JFET is covered and existing computational models introduced. The thermal properties of published SiC JFETs are then given and key performance values examined. Design strategies for n-channel lateral depletion-mode (NLDM) JFETs are finally outlined and published SiC JFET circuits critiqued.

Chapter 3 presents a set of phenomenological models describing carrier statistics and transport properties as a function of temperature and doping concentration which are suitable for describing the operation of macroscopic JFETs. Computationally efficient models and techniques are subsequently developed that are ideally suited for use by circuit simulators. The influence of multiple non-parabolic conduction bands is discussed is detail and a closed-form expressions is developed for the electron thermal density of states effective mass. A discussion of the temperature dependence of the electron conductivity effective mass and its influence on anisotropy of electron mobility is lastly presented.

Chapter 4 starts by providing a outline of the process flow used to fabricate the monolithically integrated 4H–SiC lateral signal-level JFETs and test structures used in this work. Areas influencing device behaviour are discussed. The impact of contact resistance on device performance is studied with the aid of a modified transfer length method (TLM) model. The derivation and validation of a set of novel temperature dependent compact models is presented and validated against experimental electrical measurements between 25 °C and 400 °C.

Chapter 5 implements the compact model developed in the chapter 4 using parameters matched to a fabricated device in order to simulate a number of pertinent amplifier circuits, including single stage common source (CS) amplifiers, differential amplifiers and voltage level-shifters. The influence of the body-effect on circuit performance is studied in great detail. Lastly, a high gain and temperature stable operational amplifier (op-amp) is demonstrated in both open- and closed-loop configurations.

Chapter 6 summarises the conclusions of the preceding chapters and identisies areas of future work.

CHAPTER

2

Literature Review

2.1 Introduction

An understanding of electronic circuits first requires an appreciation of the devices of which they are comprised. These in turn require knowledge of the relevant electronic properties of the contributing materials and their dependence on external stimuli. Suitable models are required in each case which provide an appropriate level of abstraction.

The ability to precisely control the conductivity of a semiconductor through the introduction of impurities and the manipulation of electric fields has allowed a variety of high performance solid-state devices to be conceived and realised. The robustness of the junction field effect transistor (JFET) and its relative ease of fabrication makes for a highly appropriate pairing with SiC for hostile environment applications. The general theory for their operation is well understood; however, the behaviour of specific structures can vary greatly and will depend on the details of their fabrication and the conditions of their operation.

A quantum mechanical treatment is warranted to account for SiC's electronic properties which present with distinct dependence on direction, electric field strength and temperature. Such information is required to assess the impact on device performance and to establish appropriate mathematical descriptions for their operation.

The first purpose of this chapter is to introduce the nomenclature and known concepts influencing the operation of 4H–SiC JFETs under envisaged conditions. The second purpose is to present a discussion of the pertinent published work on devices and circuits and to identify gaps in the literature with relevance to this work.

2.2 Silicon Carbide

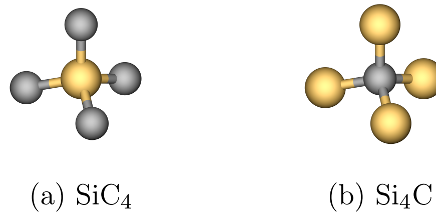
2.2.1 Crystal Structure

SiC is a IV–IV* compound semiconductor comprised of a balanced stoichiometry of Si and C atoms, sp^3 hybrid orbitally bonded† to four dissimilar nearest neighbour atoms; the spatial arrangement of atoms form tetrahedral cells, as are illustrated in Figure 2.1‡ [12]. The short

*C and Si are isoelectronic [9].

†An electron from the 3s (2s) shell of Si (C) is promoted to its 3p (2p) shell.

‡Minor deviations from the ideal tetrahedra structure occur.



(a) SiC_4 (b) Si_4C

Figure 2.1
Ball and stick models depicting the tetrahedral bonding of Si (gold) and C (grey) atoms as would occur in bulk SiC.

inter-atomic distances develop a wide fundamental band gap, high chemical bond strength and excellent mechanical hardness [7]. The difference in the electronegativity of Si and C atoms, 1.90 and 2.55 in Pauling units, respectively, results in polarised covalent bonds, whereby electrons are more strongly attracted to the C atoms [13]; the intrinsic polarisation introduces effects not present in non-polar semiconductors, such as Si or Ge.

While SiC is the only chemically stable bulk compound of Si and C, disturbances in the growth nucleus facilitate the formation of numerous polytypes* with distinct electrical and mechanical properties. The underlying mechanism by which this occurs is not clear, but is believed to be a result of either the thermodynamic stability of small-period polytypes within longer-order structures, the influence of screw dislocations during growth, or a combination of both of these effects [14, 15].

A hexagonal basis can be defined for each SiC polytype and replicated at each site of a respective simple hexagonal lattice† defined by the direct lattice translation vector

$$\boldsymbol{R} = u\boldsymbol{a}_1 + v\boldsymbol{a}_2 + w\boldsymbol{c}, \tag{2.1a}$$

wherein u, v and w are integers and $\boldsymbol{a}_1$, $\boldsymbol{a}_2$ and $\boldsymbol{c}$ are the non-coplaner primitive vectors for the direct lattice which can be given in terms of primitive lattice constants, a and c, and cartesian unit vectors, $\hat{\boldsymbol{x}}$, $\hat{\boldsymbol{y}}$ and $\hat{\boldsymbol{z}}$, as‡

$$\boldsymbol{a}_1 = a\hat{\boldsymbol{x}}, \quad \boldsymbol{a}_2 = -\frac{a}{2}\hat{\boldsymbol{x}} + \frac{\sqrt{3}a}{2}\hat{\boldsymbol{y}}, \quad \boldsymbol{c} = c\hat{\boldsymbol{z}}. \tag{2.1b}$$

Only the lattice constant along the direction of the principle-axis varies markedly between polytypes, being dependent on the number of bilayers§ in the stacking sequence. The lattice constants for intrinsic 4H and 6H at 300 K¶ are given in Table 2.1 [19]. Al and N are the preferred acceptor and donor dopants in both polytypes. Due to the relative difference in atomic size these values are understandably found to increase slightly with Al concentration and decrease slightly with N concentration, although by negligible amounts compared with that due to thermal expansion.

*Polytypism is a special case of polymorphism, varying in one direction [14].
†Other choices conflict with the conventional notation for directions and planes ubiquitous in literature.
‡Another common choice has the x-axis bisect the angle between $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$ [16–18].
§Bilayers are neighbouring layers of dissimilar atoms aligned along the principle axis.
¶The kelvin, symbol K, is the SI unit of thermodynamic temperature.

Table 2.1
The primitive lattice constants of intrinsic 4H– and 6H–SiC at 300 K.

Polytype	a (Å)	c (Å)
4H	3.0798	10.0820
6H	3.0805	15.1151

The corresponding translation vector for the reciprocal lattice is defined as

$$\boldsymbol{G} = h\boldsymbol{a}_1^* + k\boldsymbol{a}_2^* + l\boldsymbol{c}^*, \tag{2.2a}$$

where h, k and l are integers and $\boldsymbol{a}_1^*$, $\boldsymbol{a}_2^*$ and $\boldsymbol{c}^*$ are the non-coplanar primitive vectors for the reciprocal lattice, which given Equation 2.1b are determined as

$$\boldsymbol{a}_1^* = \frac{2\pi}{a}\left(\frac{\sqrt{3}\hat{\boldsymbol{x}} + \hat{\boldsymbol{y}}}{\sqrt{3}}\right), \quad \boldsymbol{a}_2^* = \frac{2\pi}{a}\left(\frac{2}{\sqrt{3}}\hat{\boldsymbol{y}}\right), \quad \boldsymbol{c}^* = \frac{2\pi}{c}\hat{\boldsymbol{z}}. \tag{2.2b}$$

Crystal directions are conventionally expressed using Miller indices, defined by the smallest integer multiple of u, v and w to denote a collinear value of $\boldsymbol{R}$ [16]. Conversely, crystal planes are defined as being orthogonal to reciprocal lattice vectors with Miller indices equal to the lowest integer multiples of h, k and l to specify a collinear value of $\boldsymbol{G}$ [16]. Given the hexagonal symmetry present in all SiC polytypes Miller-Bravais indices become more appropriate as they highlight the presence of equivalent directions and planes; analogous to the case of Miller indices in cubic systems a plane tangental to a direction shares the same values for their indices. Miller-Bravais planes, $(\eta, \kappa, \iota, \lambda)$, and directions, $[\upsilon, \nu, \tau, \omega]$, each require four indices which are related to their respective Miller indices by [20]

$$\eta = h \tag{2.3a}$$

$$\kappa = k \tag{2.3b}$$

$$\iota = -(\eta + \kappa) \tag{2.3c}$$

$$\lambda = l \tag{2.3d}$$

and

$$\upsilon = \tfrac{1}{3}(2u - v) \tag{2.4a}$$

$$\nu = \tfrac{1}{3}(2v - u) \tag{2.4b}$$

$$\tau = -(\upsilon + \nu) \tag{2.4c}$$

$$\omega = w \tag{2.4d}$$

respectively.

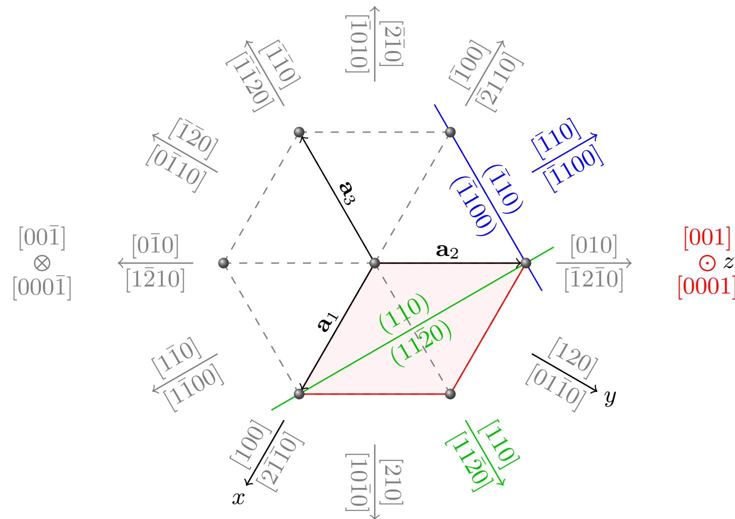


Figure 2.2

A graphical summary of the high symmetry directions and planes in SiC, projected along the basal plane, using both Miller and Miller-Bravais notation. Commonly referenced planes include the M–face (blue), A–face (green) and Si–face (red). Corresponding directions are similarly coloured.

Pertinent directions and planes are presented in Figure 2.2 in terms of both Miller and Miller-Bravais indices. The centre of each of the six basal plane faces and each of its six corners constitute equivalent directions [21] which are collectively identified by

$$\langle 11\bar{2}0\rangle \equiv [11\bar{2}0]\,,\ [\bar{2}110]\,,\ [1\bar{2}10]\,,\ [\bar{1}\bar{1}20]\,,\ [2\bar{1}\bar{1}0]\,,\ [\bar{1}2\bar{1}0]$$

and

$$\langle 10\bar{1}0\rangle \equiv [10\bar{1}0]\,,\ [01\bar{1}0]\,,\ [\bar{1}100]\,,\ [\bar{1}010]\,,\ [0\bar{1}10]\,,\ [1\bar{1}00]\,,$$

respectively. Commonly used face definitions include the A–faces

$$\{11\bar{2}0\} \equiv (11\bar{2}0)\,,\ (\bar{2}110)\,,\ (1\bar{2}10)\,,\ (\bar{1}\bar{1}20)\,,\ (2\bar{1}\bar{1}0)\,,\ (\bar{1}2\bar{1}0)\,,$$

the M–faces

$$\{1\bar{1}00\} \equiv (10\bar{1}0)\,,\ (01\bar{1}0)\,,\ (\bar{1}100)\,,\ (\bar{1}010)\,,\ (0\bar{1}10)\,,\ (1\bar{1}00)\,,$$

the Si–face (0001) and the C–face $(000\bar{1})$.

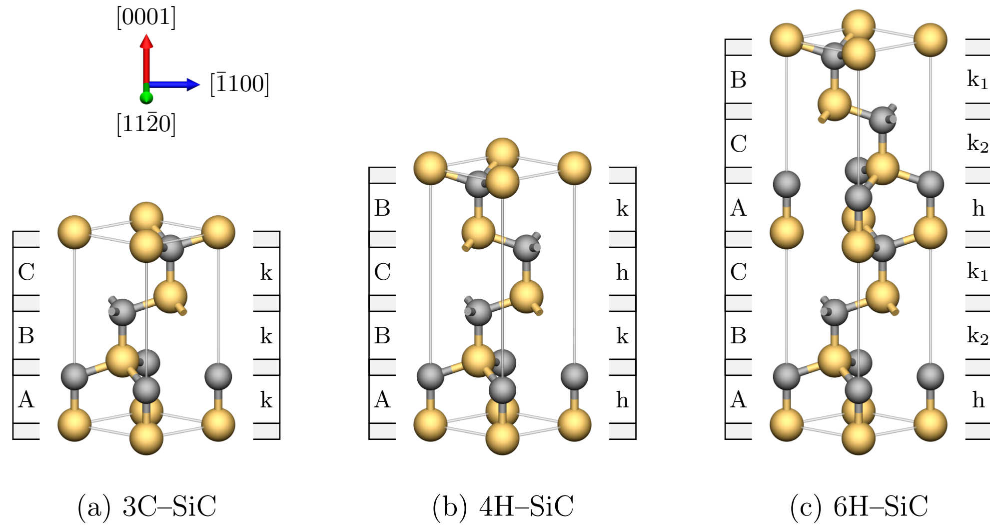
All polytypes may be characterised by a repeated close packed bilayer stacking sequence of local Zinc Blende (ABCABC...) and Wurtzite (ABAB...) crystal structures along the principle-axis* [15]. Ramsdell notation offers a terse alternative and is the most commonly utilised SiC polytype descriptor, whereby an integer denotes the number of bilayers in the repeated stacking sequence and a letter symbolises the crystal structure as having cubic (C),

*These may be written in terms of individual atoms using AA', BB' and CC' in place of A, B and C [9].

Table 2.2

A comparison of the commonly utilised descriptors for prevalent SiC polytypes [22, 26].

ABC	Ramsdell	Jagodzinski	Hägg	Zhdonov
AB	2H	$(h)_2$	$+-$	(11)
ABC	3C	(k)	$+++$	(∞)
ABAC	4H	$(hk)_2$	$++--$	(22)
ABCACB	6H	$(hkk)_2$	$+++---$	(33)
ABACBCACBABCBAC	15R	$(hkhkk)_3$	$(+++--)_3$	$(32)_3$



(a) 3C–SiC (b) 4H–SiC (c) 6H–SiC

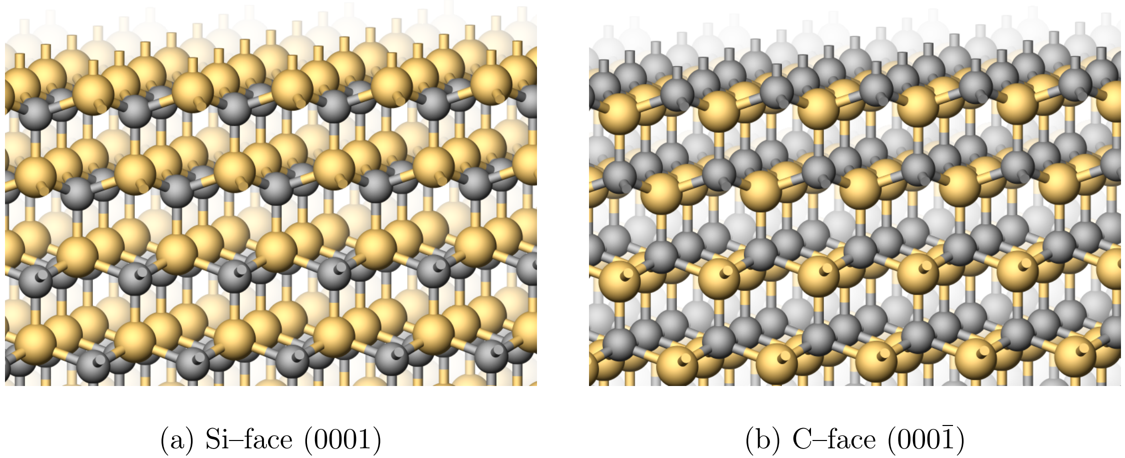
Figure 2.3

Ball and stick models of the hexagonal bases for three pertinent SiC polytypes, depicting [0001] stacking of Si (gold) and C (grey) atoms about the $(11\bar{2}0)$ plane. Local cubic (k), local hexagonal (h) and closed-packed (A, B and C) bilayer locations, are indicated.

rhombohedral (R) or hexagonal (H) symmetry [22,23]. In Jagodzinski notation a bilayer may be described as being cubic (k)* or hexagonal (h) with respect to its principle-axis nearest neighbour centroids [25]. In h layers equivalent sub-lattice positions are present in the layers above and below (local Wurtzite), while for k layers the positions are different (local Zinc Blende); as such, k sites describe bilayer translation only while h sites exhibit both bilayer translation and 180° rotation about the principle-axis [15, 22]. Less utilised notations also exist that provide a comparable level of abstraction. A comparison of most used notations is provided in Table 2.2 for the commonly studied polytypes [22, 26].

Polytype favourability is strongly dependent on growth metrics and only the 3C, 4H and 6H variants are reproducible enough for large single crystal wafer manufacture [7, 27]. The bases for these polytype are depicted in Figure 2.3 which indicates the closed-packed, local cubic and local hexagonal bilayer positions. Theoretical studies suggest that 3C is the most

*From the German word, kubisch [24].



(a) Si–face (0001) (b) C–face (000$\bar{1}$)

Figure 2.4
Ball and stick models of on-axis non-passivated bulk 4H–SiC crystals for both Si (gold) and C (grey) terminated surfaces.

stable polytype in its intrinsic form; however, C and Si vacancies were found to improve the favourability of 4H and 6H, respectively. The results suggest a qualitative agreement with experiment, whereby 4H and 6H are favoured at high growth temperatures due to enhanced vacancy formation. 6H–SiC has historically been prevalent in the development of SiC devices due to the earlier availability of commercial wafers. 4H–SiC is currently regarded as the most advantageous of the reproducible polytypes, offering the widest energy band gap, shallower dopant energy levels, lower parameter anisotropy and, overall, higher carrier mobilities [7].

A crystal of 4H–SiC is produced by replicating the basis of atoms illustrated in Figure 2.3b at each point in a corresponding simple hexagonal lattice. For crystals grown along the direction of the principle axis the possibility exists for both Si and C terminated surfaces, as illustrated in Figure 2.4, which are termed the Si–face and C–face, respectively. The majority of 4H–SiC crystals are in fact grown between 4° and 8° off-axis. The motivation for this is to introduce closely spaced terraces that provide preferential nucleation points during crystal growth so as to prevent spurious nucleation [26].

Up to four distinct local bilayer environments are possible as a consequence of non-equivalent distant neighbours, two of which are local h and two of which are local k. The eight corresponding atomic sites have been observed in nuclear magnetic resonance (NMR) spectroscopy measurements [28]. 4H–SiC in particular provides one unique h and one unique k bilayer; an impurity substituting for one of either Si or C when localised can be in one of two unique energy states depending on its location.

2.2.2 Electronic Band Structure

The electron wave vector, $\boldsymbol{k}$, denotes the expected value for an electron wave packet and can be represented as a point in reciprocal space. The boundary conditions imposed by the periodicity of the reciprocal lattice in a crystalline solid require values of $\boldsymbol{k}$ to become quantised, with all unique values located within one reciprocal lattice unit cell [29]. The

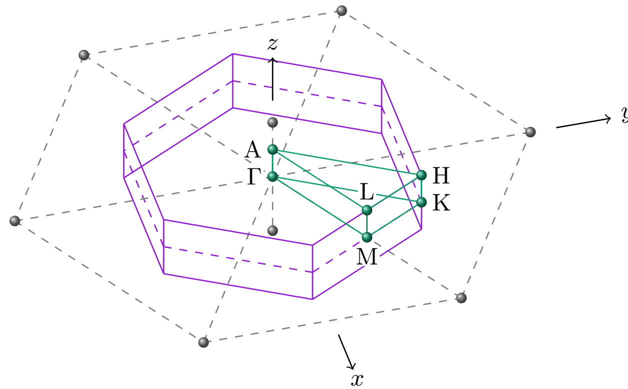


Figure 2.5

An illustration of the first Brillouin zone in 4H–SiC. Grey spheres denote reciprocal lattice points with nearest neighbours joined by dashed lines. Purple lines represent the Wigner-Seitz cell of the reciprocal lattice, termed the first Brillouin zone. Green spheres represent high symmetry points in the Brillouin zone, whose bounding volume denotes the reduced zone containing all unique states.

energy associated with each $\boldsymbol{k}$ deviates from that of a free electron and includes large regions of forbidden energy. The highest band of closely spaced levels that is fully occupied at absolute zero temperature is referred to as the first valence band with the next unoccupied band called the first conduction band. The region of energy between the bottom of the first conduction band, $E_{\mathrm{c},1}$, and the top of the first valence band, $E_{\mathrm{v},1}$ is termed the fundamental band gap [29]

$$E_{\mathrm{g}} = E_{\mathrm{c},1} - E_{\mathrm{v},1}. \tag{2.5}$$

The reciprocal lattice of a hexagonal direct lattice is itself hexagonal* with corresponding lattice constants $a^* = 4\pi/(\sqrt{3}a)$ and $c^* = 2\pi/c$. The Wigner-Seitz cell represents a valid unit cell of a reciprocal lattice and is termed the first Brillouin zone. For a hexagonal reciprocal lattice the Brillouin zone is also hexagonal, as illustrated in Figure 2.5. An important consequence of the symmetry in the Brillouin zone is that wave vectors at equivalent points have identical corresponding electronic energies. Unlike the lowest three valence bands which are located at the Γ–point, the minima of the two lowest conduction bands of interest are located at each of the six equivalent M–points, located at the Brillouin zone boundary [30].

In quantum mechanics a particle is described by its wave function. Solving the Schrödinger equation for a single electron in a periodic potential (a Bloch electron) results in a wave function similar to that of a free electron but multiplied by a function with equal periodicity as the Bravais lattice [16]. It is therefore often justifiable to characterise the behaviour of such electrons using a semiclassical model wherein their masses are modified to account for the interaction with the crystal potential [31]. The absence of an electron may equally well be represented by a quasi-particle called a hole exhibiting a positive charge and an appropriate effective mass [12].

Cyclotron resonance (CR) provides an accurate and direct means of determining the

*The reciprocal lattice is rotated by 30° with respect to the direct lattice.

effective masses of carriers in semiconductors about lowest energy band extrema provided sufficiently high quality samples can be obtained [21]. Volm *et al.* performed optically detected cyclotron resonance (ODCR) measurements* at 1.6 K and 36 GHz at magnetics fields up to 4 T to determine the individual components of the electron effective mass tensor at the bottom of the first conduction band of 4H–SiC, obtaining values of 0.33(1), 0.58(1) and 0.31(1) in units of free electron mass in the M–L, M–Γ and M–K directions, respectively [21]. Son *et al.*, using ODCR performed at 9.23 GHz and 4.4 K, were able to identify the transverse† and longitudinal hole effective mass relative to the principle axis about the extremum of the first valence band as 0.66(2) and 1.75(2), respectively, in units of free electron mass [32]. The slight underestimates of the effective masses determined via theoretical calculations by groups such as Persson *et al.* [33, 34] can be attributed to the neglecting of the polaron effect‡ as well as the assumptions made in their calculations [21, 32].

For small changes in $\boldsymbol{k}$ around a conduction band minimum the increase in energy is approximately quadratic, as it is for free electron [12]; however, for larger values an electron wave will interact more strongly with the lattice causing the effective mass to increase [9]. A mobile electron in a practical bulk semiconductor in the presence of an electric field will be scattered after only a small change in $\boldsymbol{k}$, meaning only a narrow range of energy need be considered§ being dependent on the maximum temperature and doping concentration of interest [9].

$\boldsymbol{k}\cdot\boldsymbol{p}$ theory¶ allows approximate analytical expressions for band dispersion around high symmetry points to be defined. From density functional theory (DFT) band theory calculations under the local density approximation (LDA), Wellenhofer and Rössler discovered that the dispersion in the M–K and M–Γ directions for the lowest two conduction bands are essentially parabolic, and that the hyperbolic model given by‖ [30]

$$E(k_z) = E_\mathrm{c} - \frac{c_z}{2} + \left(\frac{c_z^2}{4} + \frac{c_z \hbar^2 k_z^2}{2m_{zz}^*}\right)^{1/2} \tag{2.6}$$

could accurately account for the dispersion along the M–L direction up to 300 meV above the first conduction band minimum, wherein E_c is the energy of the respective conduction band minimum and k_z, m_{zz}^* and c_z are, respectively, the component of $\boldsymbol{k}$, the effective mass and the first-order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameter, in the M–L direction in reciprocal space. It will later be shown that this represents the appropriate energy range of interest for high temperature 4H–SiC JFETs. A comparison of this model with the parabolic band model and the theoretically calculated values of Wellenhofer and Rössler using the DFT-LDA method is given in Figure 2.6a.

As the rate of increase of energy becomes progressively smaller than the square of the

*The short carrier scattering times, particularly for holes, for samples produced during this period demanded high frequencies and the photo-neutralisation of ionised impurities provided by ODCR for successful cyclotron resonance CR measurements [32].

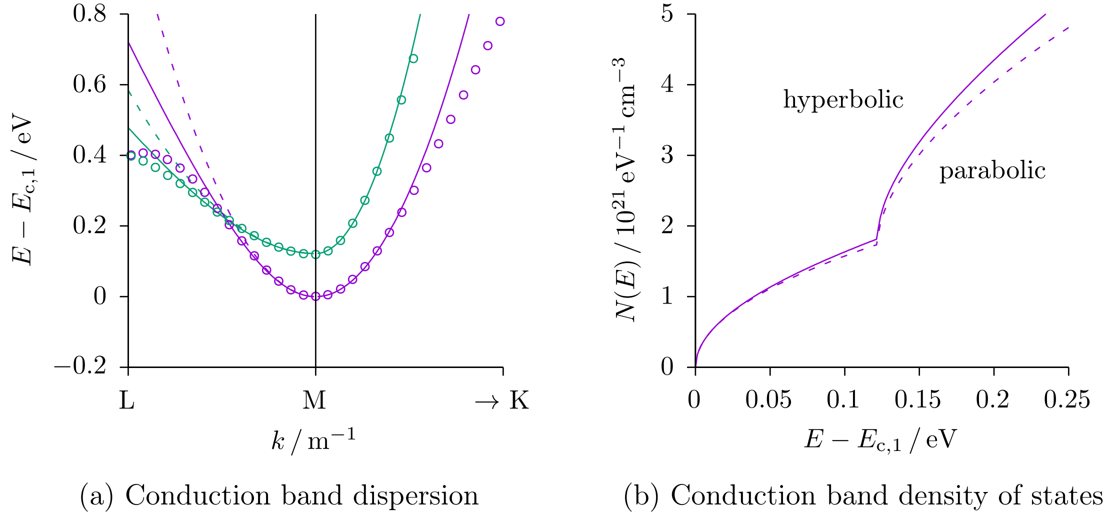
†The transverse value is an appropriate average of the two basal plane principle tensor components.

‡A polaron describes an electron or hole coupled to an optical phonon in polar semiconductor.

§This is not the case when ballistic effects or injection of high energy electrons are present.

¶The $\boldsymbol{k}\cdot\boldsymbol{p}$ relation is an approximate solution of the one electron wave equation for a Block wave [35].

‖A derivation is given by Smith [36].



(a) Conduction band dispersion

(b) Conduction band density of states

Figure 2.6

A comparison between (a) the DFT-LDA calculations (points), parabolic dispersion approximation (dashed lines) and hyperbolic $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion model (solid lines), for the first two conduction bands in 4H–SiC along M–L and M–K close to the band minima and (b) the combined density of states from each bands determined using the parabolic (dashed lines) and hyperbolic $\boldsymbol{k}\cdot\boldsymbol{p}$ (solid lines) models. Reprinted [adapted] from [30].

wave number the effective mass increases, resulting in a greater number of $\boldsymbol{k}$–space states within a given energy interval [35, 37], as illustrated by the density of states (DOS) plot presented in Figure 2.6b. These theoretical results have been confirmed by ballistic-electron emission microscopy (BEEM) experiments [38].

The difference in energy between the first and second set of equivalent conduction bands is small enough to cause appreciable occupation of the second set at modest temperature and thereby influence the electron transport properties. As the DFT-LDA effective masses for the first set agree well with experiment, the values determined for the second set are also likely to be accurate [30, 39]. This information can thus be used within phenomenological models and applied to problems concerned with carrier statistics and transport theory [36].

Spin-orbit interaction* and the internal crystal field result in three closely spaced two-fold spin degenerate valence bands each located at the Γ point in the Brillouin zone [38]. The two uppermost (heavy-hole and light-hole) valence band edges are split due to spin-orbit interaction, by an amount $E_{\mathrm{so}} = 8.6\,\mathrm{meV}$. The third band is separated by the crystal field by an amount $E_{\mathrm{cf}} = 73\,\mathrm{meV}$. While the third band has been found to be essentially parabolic the lowest two interact rather strongly [30]. Appropriate $\boldsymbol{k}\cdot\boldsymbol{p}$ theory models for their dispersions have been reported and represented as corrections to the parabolic DOS [40]; however, while the individual valence bands are not parabolic, the total DOS provided by all three can be closely approximated by three appropriately chosen parabolic valence bands [30].

*The spin-orbit interaction results from the coupling between the magnetic dipole field of a spinning electron and the magnetic field as a consequence of its orbital motion [37].

2.2.3 Carrier Statistics

Electrons and holes are Fermions and so are subject to the Pauli exclusion principle. Their expected thermal equilibrium distributions of energies in a region of a semiconductor can be appropriately determined from Fermi-Dirac statistics* and the DOS in the conduction and valence bands [12, 41]. Integrating over all states within a set of equivalent parabolic bands provides expressions for the electron and hole concentrations of

$$n_0 = N_\mathrm{c} \mathscr{F}_{1/2}\left(\frac{E_\mathrm{F} - E_\mathrm{c}}{k_\mathrm{B}T}\right) \tag{2.7a}$$

$$p_0 = N_\mathrm{v} \mathscr{F}_{1/2}\left(\frac{E_\mathrm{v} - E_\mathrm{F}}{k_\mathrm{B}T}\right), \tag{2.7b}$$

respectively, where

$$N_\mathrm{c} = 2\left(\frac{2\pi m_\mathrm{e}^\mathrm{d} k_\mathrm{B} T}{h^2}\right)^{3/2} \tag{2.8a}$$

and

$$N_\mathrm{v} = 2\left(\frac{2\pi m_\mathrm{h}^\mathrm{d} k_\mathrm{B} T}{h^2}\right)^{3/2} \tag{2.8b}$$

are termed the effective DOS in the conduction band and valence band, respectively, wherein m_e^d and m_h^d represent appropriately averaged DOS effective masses†, k_B is the Boltzmann constant, h is the Planck constant and T is the absolute thermodynamic temperature; $\mathscr{F}_{1/2}$ is the Fermi integral of order one-half; E_F is the electrochemical potential, more commonly referred to as the Fermi level‡, denoting the chemical potential of the electrons; and E_v is the energy of the respective valence band maximum. When the concentration of free carriers within a band is low enough that the exclusion principle becomes unimportant, the Fermi integral can be replaced by an exponential,

$$\mathscr{F}_{1/2}(\eta) \approx \mathrm{e}^{\eta}, \quad \text{for } \eta \ll 0. \tag{2.9}$$

Equation 2.9 is termed the Boltzmann approximation and remains valid provided E_F appears in the fundamental band gap far away from the band edges.

The intrinsic carrier concentration can be attained by applying Equation 2.9 to Equation 2.7 as [12]

$$n_\mathrm{i} = \sqrt{n_0 p_0} = \sqrt{N_\mathrm{c} N_\mathrm{v}}\, \mathrm{e}^{-\frac{E_\mathrm{g}}{2k_\mathrm{B}T}}, \quad \text{for } E_{\mathrm{v},1} \ll E_\mathrm{F} \ll E_{\mathrm{c},1}. \tag{2.10}$$

*This is the most probable distribution for carriers in thermal equilibrium, defined as the arrangement which can be obtained in the greatest number of ways [31].

†Geometric mean averaged over all equivalent extrema in the Brillouin zone.

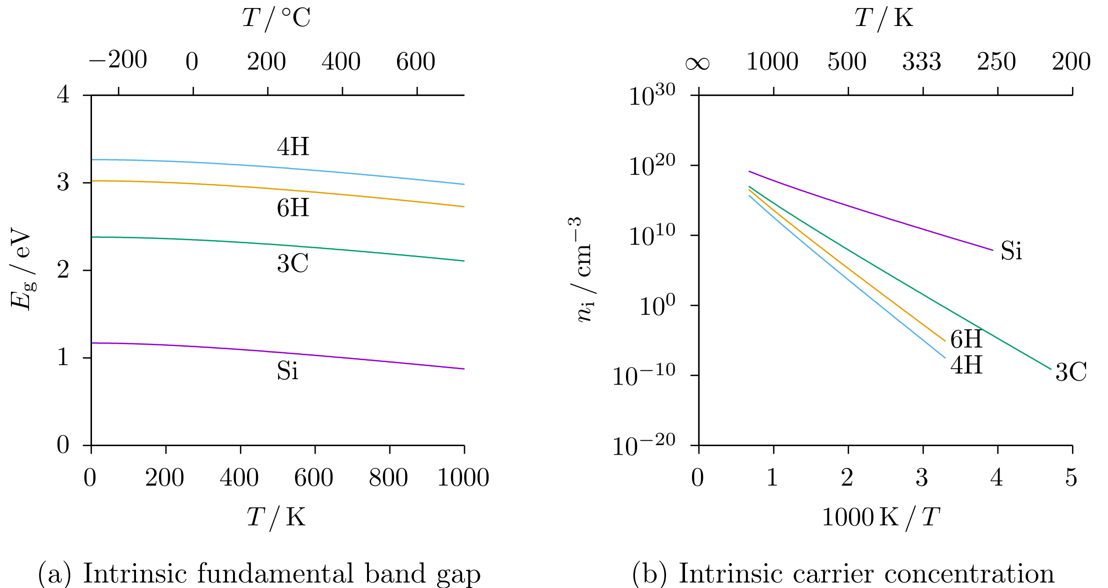
‡In non-engineering texts the symbol E_F is often strictly used to represent the Fermi-energy, denoting the highest occupied state at absolute zero, while the symbol μ_e is used to denote the electrochemical potential. As μ_e is used ubiquitously in engineering texts to denote electron mobility the convention of using the symbol E_F in both instances has been adopted.

Under the condition of non-degeneracy, the n_0p_0 product remains independent of the doping concentration [36]; however, the Boltzmann approximation is strictly valid for parabolic semiconductors. It is possible to derive approximate expressions for non-parabolic and degenerate semiconductors by using DOS functions derived from $\boldsymbol{k}\cdot\boldsymbol{p}$ theory within the framework of the Joyce-Dixon approximation (JDA) [42]. The results are polynomial corrections to the Boltzmann approximation were the coefficients can be determined using a mixture of analytical and numerical techniques.

The band gap energy is the dominant term in Equation 2.10 which is itself a function of temperature due to lattice dilation and increased electron-lattice interactions [16, 37, 43]. For 4H–SiC this variation can be approximated by the empirical expression [43, 44]

$$E_\mathrm{g}\,/\,\mathrm{eV} \approx 3.265 - \frac{6.5\times10^{-4}\,T^2}{T+1300}. \tag{2.11}$$

A comparison of the intrinsic band gap energy and and intrinsic carrier concentration in Si and 3C–, 4H– and 6H–SiC as a function of temperature, assuming singular sets of parabolic conduction and valence bands, is illustrated in Figure 2.7 and demonstrates 4H–SiC's superiority and suitability for use at high temperatures* [44].



(a) Intrinsic fundamental band gap

(b) Intrinsic carrier concentration

Figure 2.7

Variation of (a) the intrinsic fundamental band gap energy, E_g, and (b) the intrinsic carrier concentration, n_i, with temperature, T, for three pertinent SiC polytypes and Si, assuming singular sets of parabolic conduction and valence bands. Reprinted [adapted] from [44].

Monovalent impurities in SiC† are coerced to share the same tetrahedrally bonding arrangement as the host lattice. In the case of donors this forces one of their five valence

*The non-parabolic nature of band edges causes this simple assessment to break down at elevated temperatures.

†Monovalent acceptors and donors are located in group III and V of the periodic table, respectively.

electrons to occupy a higher energy anti-bonding state that would otherwise represent a conduction band state. The occupation, however, lowers this state's energy slightly such that it appears as a localised level below the conduction band edge [45]. Such a donor level is described as being neutral if filled by an electron and positively charged if empty [12]. An analogous situation exists for monovalent acceptors. An acceptor level is, conversely, neutral if empty and negatively charged if filled by an electron [12]. At finite temperatures the system is dynamic with excitation from and capture by impurities continuously taking place [9, 37]. The concentrations of donor electrons in the conduction band and acceptor holes in the valence band can, however, be statistically determined.

Substitutional* N and Al provide relatively shallow monovalent donor and acceptor levels in 4H–SiC, replacing C and Si atoms, respectively, each having two non-equivalent sites. Consequently two ground-state energies should be observed for each impurity† [48]. Strong evidence exists that support site occupancy being evenly weighted between the non-equivalent sites [49]. The situation for donors is further complicated by the presence of multiple equivalent conduction bands whose combined 1s like ground-state wave function is comprised of the wave functions of six separate electron states. Valley-orbit coupling‡ raises the energy of the four non-symmetric electron states [50] resulting in two ionisation energies for each non-equivalent donor site. Notably, as the wave function associated with each non-interacting impurity is highly localised only one of the six states can be occupied at any instance [46]; thus, the higher energy states are analogous to excited states.

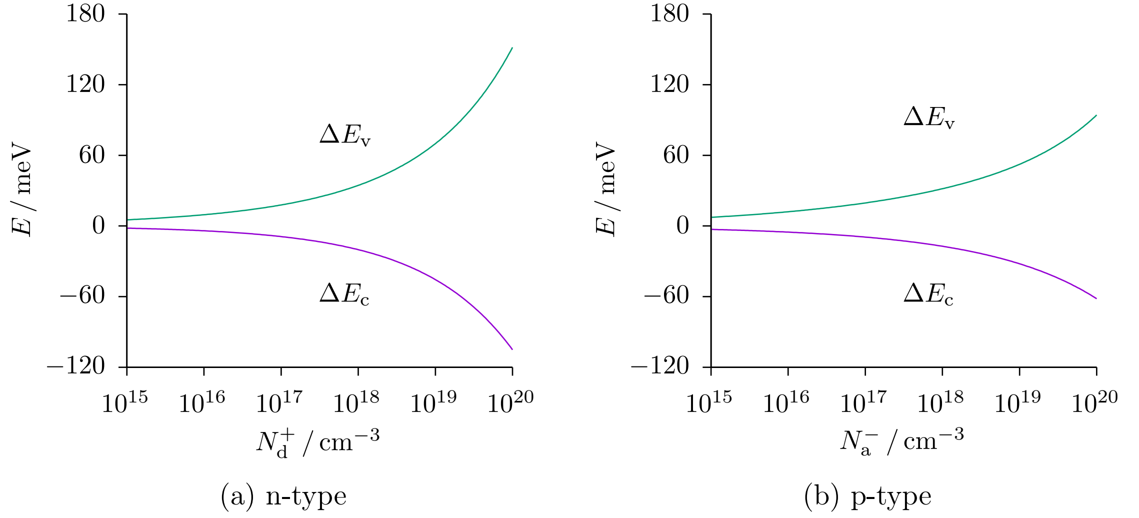
The wide range of reported ionisation energies for N and Al in the literature for 4H–SiC can be attributed to varying crystal quality and the underlying assumptions made in their determination [49]. The most reliable values for the ground-state energies of N on h sites is provided by Ivanov *et al.* attained through the matching of excited states from photo-thermal ionisation and infrared absorption spectra with values predicted by the effective mass approximation. These provide values for $E_{\mathrm{d,h}}(\mathrm{A_1})$ and $E_{\mathrm{d,h}}(\mathrm{E})$ of 61.4(5) meV and 54.0 meV below the conduction band, respectively [51]. A follow-up study using donor-acceptor pair luminescence measurements on high quality N and Al samples provided a k site energy, $E_{\mathrm{d,k}}(\mathrm{A_1})$, of 125.5(1) meV and acceptor energies, $E_{\mathrm{a,h}}$ and $E_{\mathrm{a,k}}$, of 197.9(1) meV and 201.3(1) meV, for h and k sites, respectively [52]. The ground-state separation of $E_{\mathrm{d,k}}(\mathrm{E})$ from $E_{\mathrm{d,k}}(\mathrm{A_1})$ has been reported elsewhere to be 11 meV [26].

Interactions between the free carriers and the ionised impurities as well as those between these carriers and optical phonons, present with a decrease and increase of the conduction band and valence band edges, respectively [53]. The change in the conduction band and valence band edges with increasing doping concentrations have been studied by Persson *et al.* accounting for the various interactions between the majority carriers, minority carriers and impurity atoms [53]. A set of parameterised closed form expressions were determined

*The ionisation energy of interstitial impurities are typically far greater than the band gap energy [36].

†The site dependence on ionisation energies is a consequence of the Kohn-Luttinger effect [46, 47].

‡The portion of a defect potential localised within a unit cell is known as a central cell correction. This produce an interaction between the degenerate conduction band valleys known as the valley-orbit coupling.



(a) n-type

(b) p-type

Figure 2.8

Empirical fit to band theory calculations of the variation in the conduction band minimum, ΔE_c, and valance band maximum, ΔE_v, in 4H–SiC due to (a) ionised donors, N_d^+, and (b) ionised acceptors, N_a^-. Reprinted [adapted] from [53].

as

$$\Delta E_\mathrm{c} \,/\, \mathrm{meV} = -17.91 \left(\frac{N_\mathrm{d}^+}{10^{18}}\right)^{1/3} - 2.20 \left(\frac{N_\mathrm{d}^+}{10^{18}}\right)^{1/2} \tag{2.12a}$$

$$\Delta E_\mathrm{v} \,/\, \mathrm{meV} = 28.23 \left(\frac{N_\mathrm{d}^+}{10^{18}}\right)^{1/4} + 6.24 \left(\frac{N_\mathrm{d}^+}{10^{18}}\right)^{1/2} \tag{2.12b}$$

and

$$\Delta E_\mathrm{c} \,/\, \mathrm{meV} = -16.15 \left(\frac{N_\mathrm{a}^-}{10^{18}}\right)^{1/4} - 1.07 \left(\frac{N_\mathrm{a}^-}{10^{18}}\right)^{1/2} \tag{2.12c}$$

$$\Delta E_\mathrm{v} \,/\, \mathrm{meV} = -35.07 \left(\frac{N_\mathrm{a}^-}{10^{18}}\right)^{1/3} + 6.74 \left(\frac{N_\mathrm{a}^-}{10^{18}}\right)^{1/2} + 56.96 \left(\frac{N_\mathrm{a}^-}{10^{18}}\right)^{1/4} \tag{2.12d}$$

for n-type and p-type 4H–SiC, respectively, where N_d^+ and N_a^- represent the ionised donor and acceptor concentration, respectively, with units of cm^{-3} [53]. Plots of Equation 2.12 are presented in Figure 2.8. The band gap narrowing effects are essentially insensitive to the dopant species and therefore can be treated as depending on concentration only [9]. While these expressions are strictly valid for doping concentrations above $10^{18}\,\mathrm{cm}^{-3}$ and at low temperatures they are suggested to be suitable outside of these limits [53]. Due to the interdependence of the extrinsic band gap and ionised impurity concentration self-consistently calculations are required.

2.2.4 Carrier Mobility

The electron transport properties within the channel region of a macroscopic n-channel JFET will closely follow the behaviour of the underlying bulk semiconductor. The electron drift current density is proportional to the average drift velocity of the electron charge density, v_d, whose value is related to the applied electric field, $\mathscr{E}$, by a proportionality factor termed the electron drift mobility, μ_e, according to the expression [54]

$$\langle v_\mathrm{d} \rangle = -\mu_\mathrm{e} \mathscr{E}. \tag{2.13}$$

An electron in a perfect crystal, accelerated by an applied electric field will pass successively between corresponding edges of the Brillouin zone. In practice, however, the electric field established by changes in the periodic lattice potential by imperfections can alter the momentum of electrons after small changes in their wave vector [9]. The rapidly varying potential requires a quantum mechanical treatment to determine the resulting distribution of carrier momentum and energy which in turn depend on the density of unoccupied quantum states and the requirements of conservation of momentum and energy [35].

In the context of the relaxation-time approximation (RTA) of the Boltzmann equation the momentum relaxation time, τ_m, represents the time required to randomise the carrier momentum*. An effective momentum relaxation time is attained by combining the influence of each scattering mechanism using Matthiessen's rule [55],

$$\tau_\mathrm{m}^{-1} = \sum_i \tau_{\mathrm{m},i}^{-1}. \tag{2.14}$$

Using measurements of Hall mobility, μ_H, Pernot *et al.* were subsequently able to approximately quantify the influence of the pertinent scattering mechanisms in extrinsic 4H–SiC for various impurity concentrations and temperatures. The results corresponding to typical doping concentrations used for the n-type channel and p^+-type gate regions of a homoepitaxial JFET are presented in Figure 2.9 and consider the influence of intra-valley longitudinal† acoustic phonon‡ (ac), ionised impurity (ii), neutral impurity (ni), polar optical phonon (pop), non-polar optical phonon (npo) and inter-valley phonon (iph) scattering mechanisms [20, 57].

The characteristic behaviour in Figure 2.9a for the moderately doped ($10^{17}\,\mathrm{cm}^{-3}$) n-type sample is consistent with the stepwise power law model presented by Scozzie *et al.* for a similarly doped sample which found mobility to vary as $T^{-1.2}$ between 100 K and 200 K, $T^{-1.7}$ between 200 K and 300 K and $T^{-2.4}$ between 300 K and 600 K [58]. In the temperature range of interest in this study, approximately 300 K to 700 K, it is seen that intra-valley polar optical, intra-valley acoustic and inter-valley phonon scattering have appreciable influence on the measured electron Hall mobility, each accelerating the decrease in mobility from approximately $480\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ to $70\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$.

For the highly doped p-type sample in Figure 2.9b the mobility is dominated at low

*In the specific case of isotropic scattering this is equivalent to the mean time between collisions.
†Referring to the direction of displacement with respect to the direction of propagation of energy.
‡A phonon is a quantised lattice vibrational mode [56].

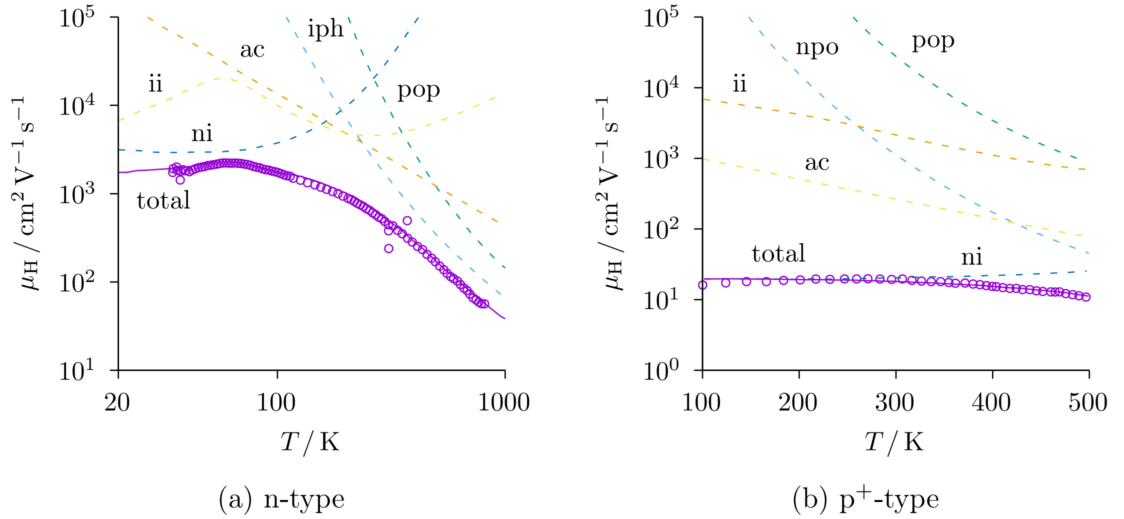


Figure 2.9

Experimental Hall mobility, μ_H, (points) for (a) moderately N doped (10^{17} cm^{-3}) and (b) highly Al doped (10^{19} cm^{-3}) 4H–SiC samples as a function of absolute thermodynamic temperature, T, alongside theoretical fits (solid lines) determined from approximate solutions to the Boltzmann equation with the relaxation time approximation, considering contributions from to intra-valley longitudinal acoustic phonon (ac), ionised impurity (ii), neutral impurity (ni), polar optical phonon (pop), non-polar optical phonon (npo) and inter-valley phonon (iph) scattering mechanisms (dashed lines). Reprinted [adapted] from [20, 57].

temperatures by neutral impurity scattering on account of the high degree of incomplete ionisation of acceptors. At higher temperature acoustic phonons and non-polar optical phonons have a stronger influence on the mobility. At 300 K the hole Hall mobility was measure to be around 20 cm^2 V^{-1} s^{-1} which drops to about 10 cm^2 V^{-1} s^{-1} at 500 K.

At low electric fields the increase in drift velocity is roughly proportional. High electric fields impart more energy to the electrons which can be described as having an electron temperature higher than that of the lattice. For sufficiently large electric field strengths the drift mobility will depart appreciably from its low-field value [36]. Using the conductance technique Khan and Cooper calculated the electron drift velocity as a function of electric field strength for a 10^{17} cm^{-3} N doped 4H–SiC sample cut 8° off-axis from the basal plane [59]. Self-heating was mitigated through appropriately timed pulse measurements. Additional corrections were made to account for spreading resistance and the varying encroachment of the depletion layer between the active channel and the low acceptor-doped buffer epilayer. The measured values at 296 K and 593 K are presented in Figure 2.10.

The experimental high-field carrier velocity can be expediently modelled by the semi-empirical expression [35, 59]

$$v_{\mathrm{d}}(\mathscr{E}) = \frac{\mu_{\mathrm{e},0}\,\mathscr{E}}{[1 + (\mu_{\mathrm{e},0}\,\mathscr{E}/v_{\mathrm{d,sat}})^{\beta}]^{1/\beta}}, \tag{2.15}$$

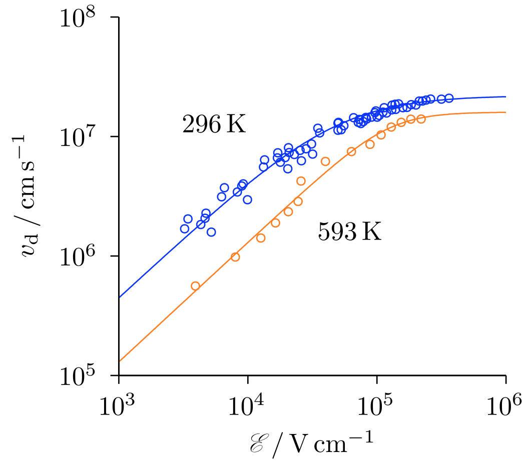


Figure 2.10

Experimental electron drift velocity, v_d, as a function of electric field strength, $\mathscr{E}$, for a $10^{17}\,\mathrm{cm^{-3}}$ N doped 4H–SiC sample 8° off-axis from the basal plane (points) and semi-empirical model fits for Equation 2.15 (lines) at 296 K and 593 K. Reprinted [adapted] from [59].

where $\mu_{\mathrm{e},0}$ represents the low field mobility, $v_{\mathrm{d,sat}}$ is the electron saturation velocity* and β is a fitting parameter. Some uncertainty is introduced into the result with the assumption of a unity Hall-factor, although this is expected to be a reasonable approximation for this sample [61]. An additional uncertainty comes from the $\pm 10\,\%$ accuracy in patterning the constricted channel region. A best fit to the data shows that at 296 K the velocity should approach a maximum value of $2.2 \times 10^7\,\mathrm{cm\,s^{-1}}$ for an electric field strength slightly above $3.5 \times 10^5\,\mathrm{V\,cm^{-1}}$, reducing to $1.6 \times 10^7\,\mathrm{cm\,s^{-1}}$ at 593 K for a field strength of approximately $2 \times 10^5\,\mathrm{V\,cm^{-1}}$. The low-field mobility at each temperature was determined to be $450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $130\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, respectively. The fitting parameter was found to be 1.2 and 2.2, respectively [59]. The electric field necessary to introduce a $1\,\%$ and $5\,\%$ reduction in mobility at room temperature should therefore be expected to be around $8.7 \times 10^3\,\mathrm{V\,cm^{-1}}$ and $1.86 \times 10^4\,\mathrm{V\,cm^{-1}}$, respectively [59].

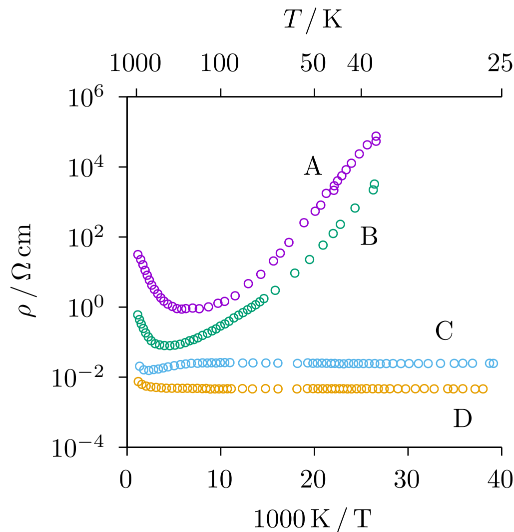
The field-dependent mobility model is also suitable for low to medium frequency large-signal analysis, as the time required for a steady-state to be achieved between the electrons and the lattice is far shorter than the periods of signals under consideration and the distance travelled by carriers in this time is far shorter than the dimension of the device channels [35].

2.2.5 Resistivity

The resistivity†, ρ, of an n-type semiconductor varies with temperature. Using a semi-classic treatment its value depends on the concentration of free electrons, n, and their drift mobility,

*Monte-Carlo calculations employing DFT derived conduction band DOS values indicate that in 4H–SiC velocity saturation at high electric field strengths is not maintained [60]; however, these values are well above those experienced by electrons under consideration in this study.

†The reciprocal of the conductivity.



Sample	Doping / cm^{-3}	Thickness / µm
A	3.5×10^{15}	2.4
B	2.2×10^{17}	0.6
C	1×10^{19}	0.15
D	4×10^{19}	0.4

Figure 2.11

Van der Pauw resistivity, ρ, measurements as a function of absolute thermodynamic temperature, T, for a range of N doped 4H–SiC samples, as deduced from Hall effect measurements. Reprinted [adapted] from [48].

μ_e, according to the equation [12]

$$\rho = \frac{1}{en\mu_e}. \tag{2.16}$$

Using mesa-etched van der Pauw structures, Ferreira da Silva *et al.* measured the resistivity of a collection of N doped 4H–SiC samples with electrically active impurity concentrations, as deduced from Hall effect measurements, between $3.5 \times 10^{15}\,cm^{-3}$ and $4 \times 10^{19}\,cm^{-3}$ in the temperature range 6 K to 900 K. The results of the various samples are presented in Figure 2.11 [48].

Sample A and B, representing low and moderate doped conditions, respectively, show a wide variation of resistivity with temperature. At very low temperatures the increase in carrier concentration, due predominantly to dopant ionisation and the resulting decrease of neutral impurity scattering, provides a decrease in resistivity with increasing temperature. The exhaustion of unionised donors and the increased influence of the various phonon scattering mechanisms eventually cause the resistivity to increase, with the turning point dependent upon the doping concentration.

The highly doped samples, C and D, are representative of the ion implanted regions formed prior to ohmic contact formation. At these concentrations the individual donor levels have spread markedly to form a band due to a strong overlap of their wave functions. The approximate constancy of the resistivity in the low temperature regime for these samples is indicative of impurity delocalisation and metal-nonmetal transitions* [48]. An electron paramagnetic resonance (EPR) study on net $1 \times 10^{19}\,cm^{-3}$ N doped 4H–SiC supports the notion of a delocalisation of donor band states. A finite energy separation of roughly 40 meV between delocalised donor states and the conduction band was, however, still observed at

*The variation of mobility with temperature at these doping concentrations shows little temperature dependence either.

around 100 K [62], suggesting that the band for donors on the k sites has not yet merged with the conduction band and that these levels remain moderately localised. This is consistent with the decrease in resistivity for sample C at high temperature due to thermal excitation to the conduction band. Sample D, however, demonstrates a strong metal to non-metal transition.

2.3 Junction Field Effect Transistors

2.3.1 Introduction

In a JFET, the flow of majority carriers from the *source* to the *drain* end of a region of extrinsic semiconductor, termed the channel, correlates with the modulation of the channel resistance by a p-n junction depletion region whose complementary terminal is called the *gate* [12]. The shared region of semiconductor on which integrated circuit (IC) devices are formed provide a second p-n junction which can be controlled via an additional *body* terminal and subsequently acts as a second gate*. A schematic cross-section for a typical lateral JFET is illustrated in Figure 2.12.

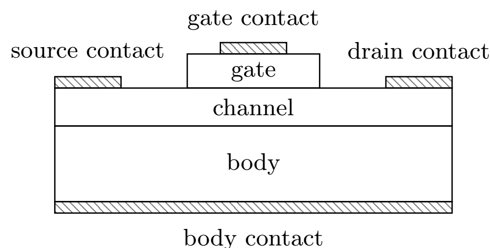


Figure 2.12
A schematic cross-section for a simple lateral junction field effect transistor. Majority carriers flow from the source along the channel to the drain. The channel resistivity is modulated by the gate-channel and body-channel p-n junctions.

The concept for the JFET was proposed by William Shockley† in 1952‡ [63]. An approximate one-dimensional treatment was utilised to predict the electric potential along and thus the current through a device channel under external bias. Dacey and Ross fabricated the first devices the following year and identified the importance of field-dependent mobility on device operation [64]. The 1960's provided discussions of more general device structures, but predominantly relied on the assumptions originally proposed by Shockley [65–67]. In 1970 Kennedy and O'Brien [68] and Kim and Yang [69] performed numerical two-dimensional calculations for various device geometries to ascertain the conditions leading to channel pinch-off and the impact and consequences of velocity saturation in Si devices.

*This is often referred to as a back-gate and the process by which a JFET in influenced by this junction is termed the body-effect.

†Shockley became a Nobel laureate in 1956 for his contribution to the development of the bipolar junction transistor (BJT) which he invented eight years prior.

‡This is the origin of the field effect transistor (FET) terminal names: drain, gate, source.

While the adoption of the JFET has been thwarted by the success of the metal-oxide-semiconductor field effect transistor (MOSFET) and the BJT, it has continued to find use in a number of high performance application, most notably within analogue front-end amplifiers. An expanding interest into hostile environment electronics is generating renewed interest with wide band gap semiconductors such as SiC proving to be an apt pairing.

2.3.2 Theory

Shockley's solution to describing current flow within a JFET was to separate the channel into many thin slices that could justifiably be analysed in one-dimension [63]. This simplification, termed the gradual channel approximation (GCA), requires that the potential contours in the channel be roughly perpendicular to the direction of current flow while those in the depletion region should lie parallel to it. These conditions can be justified in certain device structures under a specific range of bias conditions, but becomes increasingly invalid for rapidly changing space charge widths. Due to the depletion of carriers within the space charge region its resistance is significantly larger than the quasi-neutral bulk regions, allowing the gate epilayer and body epilayers to be treated as equipotential surfaces [70]. The potential at each point along the channel can then be determined from the solution of a separable first-order non-linear homogeneous ordinary differential equation.

The principle of detailed balance requires the Fermi level to be constant across a p-n junction in thermal equilibrium [9]. Majority carriers in the vicinity of the p-n junction diffuse across it, thereby uncovering a region of ionic space charge in its vicinity. The resulting electric field, directed from ionised donors to ionised acceptors, raises the potential of the n-type region with respect to the p-type region, with the resulting contact potential bringing the net movement of each carrier type to zero [9, 31].

Gauss' law provides a relationship between the volume charge density, ρ, and electric field, $\mathscr{E}$. When written in terms of electric potential, ϕ, it is commonly referred to as the Poisson equation. The one-dimensional Poisson equation applied to a bulk semiconductor yields the expression

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = -\frac{\mathrm{d}\mathscr{E}}{\mathrm{d}x} = -\frac{\rho}{\varepsilon_\mathrm{s}} = \frac{e(n - p + N_\mathrm{a}^- - N_\mathrm{d}^+)}{\varepsilon_\mathrm{s}}, \tag{2.17}$$

where ε_s represents the semiconductor permittivity and e the elementary charge. A p-n junction formed between homogeneous epilayers may be accurately described using the abrupt junction approximation (AJA). Setting the reference position to the metallurgical junction, extending the n-region in the positive direction and choosing the reference potential at minus infinity, the free hole and electron concentrations under the Boltzmann approximation may be appropriately expressed as [36, 71]

$$p(x) = p_\mathrm{p0}\,\mathrm{e}^{-\frac{e\phi(x)}{k_\mathrm{B}T}} \tag{2.18a}$$

and

$$n(x) = n_\mathrm{n0}\,\mathrm{e}^{-\frac{e[\phi_0 - \phi(x)]}{k_\mathrm{B}T}}, \tag{2.18b}$$

respectively, where p_{p0} and n_{n0} represent the equilibrium majority carrier hole and electron concentrations in the quasi-neutral regions and ϕ_0 is the contact potential. As the Fermi level in the depletion region is, except close to the quasi-neutral regions, well below and above the donor and acceptor levels, respectively, all impurities here can be assumed ionised.

Even when applying the AJA the second-order non-linear differential equation of Equation 2.17 cannot be solved analytically. From Equation 2.18, the compensating effect of the mobile carriers is limited to approximately a Debye length at each end of the depletion region and constitute a potential difference of the order of the thermal voltage, ϕ_{T} [12]. Due to the relative size of ϕ_{T} compared with ϕ_0 in 4H–SiC the abrupt depletion approximation (ADA) may be conveniently adopted to achieve an approximate analytic solution*. Taking x equal to zero at the metallurgical junction and setting n and p equal within the depletion region provides the related expressions [65]

$$\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} \approx \begin{cases} eN_{\mathrm{a}}/\varepsilon_{\mathrm{s}} & \text{for } -W_{\mathrm{p}} \leq x \leq 0 \\ -eN_{\mathrm{d}}/\varepsilon_{\mathrm{s}} & \text{for } \quad 0 \leq x \leq W_{\mathrm{n}} \end{cases} \tag{2.19a}$$

$$\mathscr{E}(x) = \begin{cases} -eN_{\mathrm{a}}(x+W_{\mathrm{p}})/\varepsilon_{\mathrm{s}} & \text{for } -W_{\mathrm{p}} \leq x \leq 0 \\ -eN_{\mathrm{d}}(W_{\mathrm{n}}-x)/\varepsilon_{\mathrm{s}} & \text{for } \quad 0 \leq x \leq W_{\mathrm{n}} \end{cases} \tag{2.19b}$$

$$\phi(x) = \begin{cases} eN_{\mathrm{a}}(x+W_{\mathrm{p}})^2/(2\varepsilon_{\mathrm{s}}) & \text{for } -W_{\mathrm{p}} \leq x \leq 0 \\ \phi(0) + eN_{\mathrm{d}}(W_{\mathrm{n}}-x/2)x/\varepsilon_{\mathrm{s}} & \text{for } \quad 0 \leq x \leq W_{\mathrm{n}} \end{cases} \tag{2.19c}$$

where W_{p} and W_{n} are the depletion widths into the p- and n-type region, respectively. A qualitative illustration of the effect of applying the ADA on the charge density across for a p^+-n junction is given in Figure 2.13.

*Numerical techniques are required for almost all other impurity profiles.

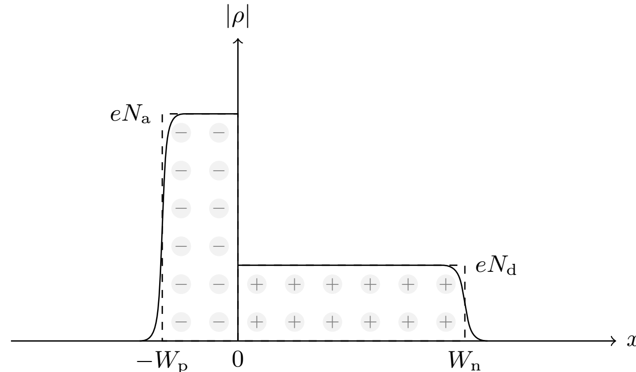
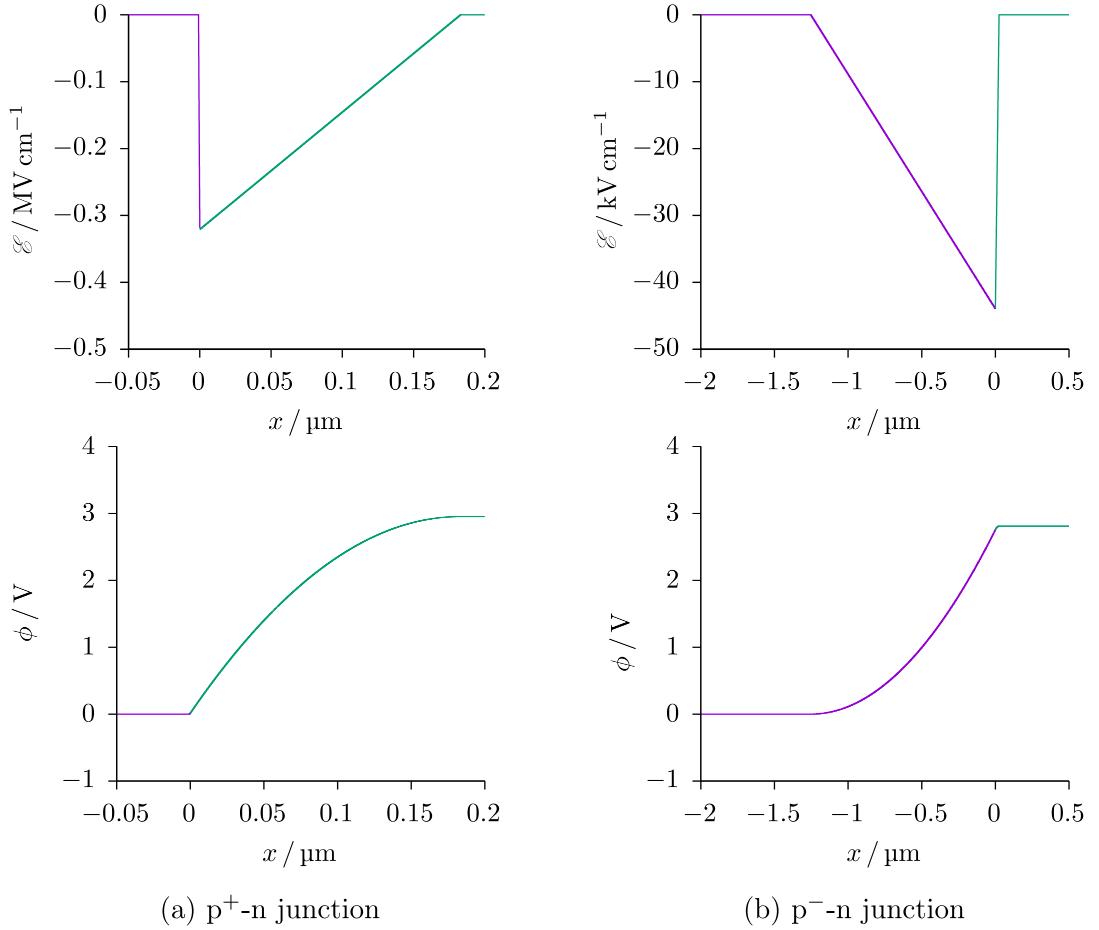


Figure 2.13

A qualitative illustration of the net charge distributions though an abrupt p^+-n junction, including electron and hole concentrations (solid lines) and using the abrupt depletion approximation (dashed lines) [12].

For the net dipole charge to equal zero the depletion region must extend further into the lower doped side of a p-n junction [63]. For homogenous epilayers with $N_\mathrm{a} > N_\mathrm{d}$ the charge density will resemble that shown in Figure 2.13. Plots of Equations 2.19b and 2.19c are presented in Figure 2.14 using typical device doping concentrations for a gate-channel junction ($N_\mathrm{a} = 2 \times 10^{19}\,\mathrm{cm}^{-3}$, $N_\mathrm{d} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $\phi_0 = 2.95\,\mathrm{V}$) and a body-channel junction ($N_\mathrm{a} = 2 \times 10^{15}\,\mathrm{cm}^{-3}$, $N_\mathrm{d} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $\phi_0 = 2.81\,\mathrm{V}$) of an n-channel JFET [72]. By choosing N_a to be 200 times larger than N_d almost all of the potential in Figure 2.14a is seen to appear over the channel region. Similarly, in Figure 2.14b the majority of the potential is dropped over the low doped body epilayer; however, the absolute value of the depletion width extending into the channel seen here is comparable to that produced by the gate-channel junction and thus would have a noticeable influence on channel resistivity.



(a) p$^+$-n junction

(b) p$^-$-n junction

Figure 2.14

Calculated electric field, $\mathscr{E}$, and electric potential, ϕ, of an abrupt p-n junction, using the abrupt depletion approximation, for (a) $N_\mathrm{a} = 2 \times 10^{19}\,\mathrm{cm}^{-3}$ and $N_\mathrm{d} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ with $\phi_0 = 2.95\,\mathrm{V}$ and (b) $N_\mathrm{a} = 2 \times 10^{15}\,\mathrm{cm}^{-3}$ and $N_\mathrm{d} = 1 \times 10^{17}\,\mathrm{cm}^{-3}$ with $\phi_0 = 2.81\,\mathrm{V}$. The reference position has been set to the metallurgical junction and the reference potential has been set to minus infinity. Purple and green indicate p and n regions, respectively.

For a step junction, any externally applied voltage will be similarly distributed across the junction [41]; the variation of depletion width into the channel epilayer can therefore be suitably described by the expression [12],

$$W_{\mathrm{n}} = \left[\frac{2\varepsilon_{\mathrm{s}} N_{\mathrm{a}}}{e N_{\mathrm{d}}(N_{\mathrm{a}} + N_{\mathrm{d}})}(\phi_0 - V)\right]^{1/2} \tag{2.20a}$$

$$\approx \left[\frac{2\varepsilon_{\mathrm{s}}}{e N_{\mathrm{d}}}(\phi_0 - V)\right]^{1/2}, \quad \text{for } N_{\mathrm{a}} \gg N_{\mathrm{d}}, \tag{2.20b}$$

where V represents the voltage applied to the p side with respect to the n side of the junction*. The maximum forward bias applied to the gate with respect to the channel is limited to the value of the contact potential for the junction, although this is not strictly achievable due to excessive leakage current prior to reaching this value [12].

Using the expression for the depletion width given in Equation 2.20b the instantaneous channel current in a n-channel JFET under the assumption of the GCA for a single gated device operating below the extrapolation pinch-off point (expop) can be expressed as [12,63]

$$i_{\mathrm{DS}} = \frac{en\mu_{\mathrm{e}} Za}{L}\left\{v_{\mathrm{DS}} - \frac{2}{3a}\left(\frac{2\varepsilon_{\mathrm{s}}}{eN_{\mathrm{d}}}\right)^{1/2}\left[(\phi_0 - v_{\mathrm{GS}} + v_{\mathrm{DS}})^{3/2} - (\phi_0 - v_{\mathrm{GS}})^{3/2}\right]\right\}, \tag{2.21}$$

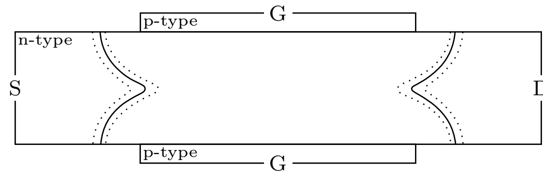
where Z denotes the channel width, L is the channel length, a is the channel depth and v_{DS} and v_{GS} are the instantaneous drain-source and gate-source voltages, respectively. The instantaneous drain-source and gate-source voltages can be separated into bias voltages V_{DS} and V_{GS}, respectively, and signal voltages, v_{ds} and v_{gs}, respectively. Similarly, the instantaneous channel current is comprised of a bias current, I_{DS}, and a signal current, i_{ds}.

Simultaneous solutions to both the continuity and Poisson equations in two-dimensions have been numerically performed by Kennedy and O'Brian using finite difference methods for a range of Si n-channel JFET structures [68]. Figures 2.15 to 2.19 present the results of their calculations for a short channel device with a gate length 2.5 times greater than its channel depth. The drain, gate and source terminals in the following channel cross-sections are denoted by the letters D, G, and S, respectively. In Figures 2.15 to 2.17 the solid lines within the n-type channel region represent 50% depletion of the majority carriers, while the dotted lines correspond with 10% and 90% depletion contours. In Figure 2.18 the solid line in the n-type channel again represents 50% depletion of the majority carriers, while the dotted lines represent contours of constant potential.

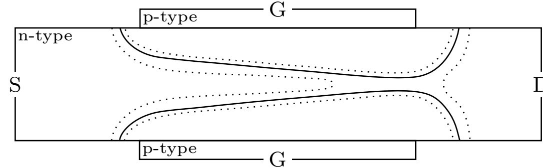
Figure 2.15a shows the expected shape of the channel depletion region under the assumption of constant electron mobility for equal gate-source and gate-drain voltages sufficient to achieve strong channel pinch-off. Figure 2.15b provides the distribution after the removal of the gate-source voltage while maintaining the gate-drain voltage and identifies that for an applied drain-source potential close to the expop† value an appreciable conductive channel remains between the source and drain ends of the device, albeit depleted by between 50%

*The resistance of the depletion region is assumed to be much larger than the quasi-neutral regions.

†The point of channel pinch-off determined after extending the gradual channel approximation past its range of validity is termed the extrapolated pinch-off point.



(a) $V_{\mathrm{DS}} = 0\,\mathrm{V}$, $V_{\mathrm{GD}} = -5\,\mathrm{V}$, $V_{\mathrm{GS}} = -5\,\mathrm{V}$



(b) $V_{\mathrm{DS}} = 5\,\mathrm{V}$, $V_{\mathrm{GD}} = -5\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$

Figure 2.15

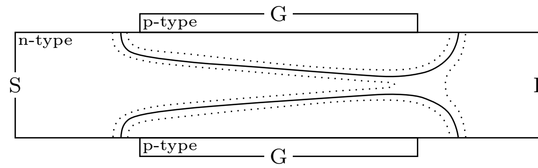
Simulated mobile electron distributions in the n-type channel of a Si JFET with gate a length 2.5 times greater than its channel depth, calculated from simultaneous solutions to both the continuity and Poisson equations in two-dimensions for a range of drain-source, gate-drain and gate-source bias voltages, V_{DS}, V_{GD} and V_{GS}, respectively, assuming constant electron mobility. Solid lines within the channel represent 50% depletion of the majority carriers while the dotted lines correspond with 10% and 90% depletion contours. Reprinted [adapted] from [68].

and 90% [68]. Notably, under the assumption of constant mobility the electron concentration in the channel was only ever found to be below the equilibrium value, as allowing transport at any speed prevents charge accumulation from taking place.

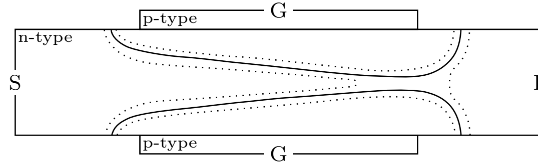
From Figures 2.16a–c it can be seen that increasing the drain-source voltage beyond the expop expands the depletion region towards the source. The continued presence of a finite channel allows further increase in channel current with channel voltage. In Figures 2.16d–e it is then seen how a negative gate-source voltage further depletes the channel.

Figure 2.17 present the corresponding results after including the influence of field-dependent mobility. Before the previous pinch-off condition is achieved the mobile carriers were found to reach their saturation velocity, whence further increase in channel voltage was unable to provide an increase in current density. Additionally, accumulation and depletion of carriers at the source and drain sides of the pinch-off region, respectfully, was found to establish a potential altering dipole layer in such a way as to ensure current continuity along the channel. The carrier accumulation was also found to impair the encroachment of the depletion region towards the source. In situations where the gate length is kept sufficiently long so as to ensure the electric field remains below the critical value these effects will be absent; however, the average electric field is still expected to have an impact on carrier mobility and thus the magnitude of the channel current [12].

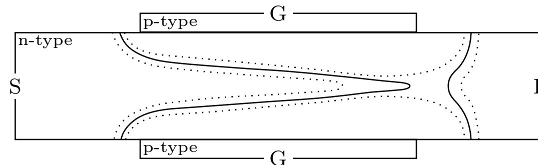
The calculated electric potential contours for the same structure under the assumption



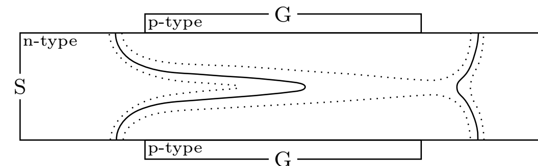
(a) $V_{\mathrm{DS}} = 4\,\mathrm{V}$, $V_{\mathrm{GD}} = -4\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



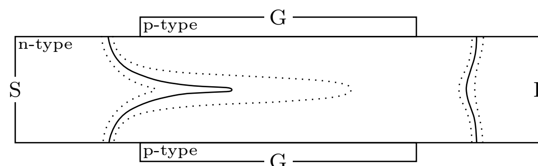
(b) $V_{\mathrm{DS}} = 5\,\mathrm{V}$, $V_{\mathrm{GD}} = -5\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



(c) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -7\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



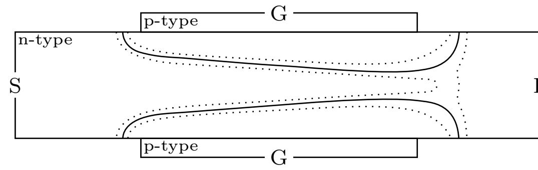
(d) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -8.21\,\mathrm{V}$, $V_{\mathrm{GS}} = -1.21\,\mathrm{V}$



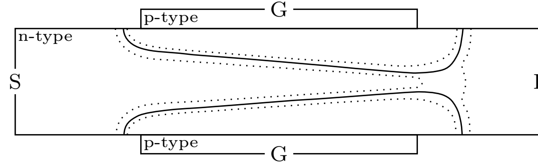
(e) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -9.42\,\mathrm{V}$, $V_{\mathrm{GS}} = -2.42\,\mathrm{V}$

Figure 2.16

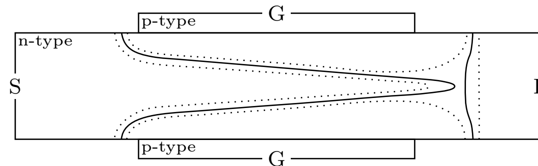
Simulated mobile electron distributions in the n-type channel of a Si JFET with gate a length 2.5 times greater than its channel depth, calculated from simultaneous solutions to both the continuity and Poisson equations in two-dimensions for a range of drain-source, gate-drain and gate-source bias voltages, V_{DS}, V_{GD} and V_{GS}, respectively, assuming constant electron mobility. Solid lines within the channel represent 50% depletion of the majority carriers while the dotted lines correspond with 10% and 90% depletion contours. Reprinted [adapted] from [68].



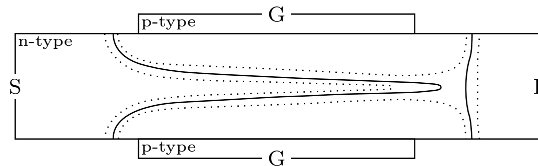
(a) $V_{\mathrm{DS}} = 3\,\mathrm{V}$, $V_{\mathrm{GD}} = -3\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



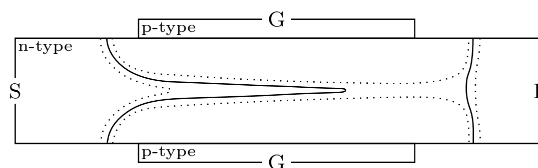
(b) $V_{\mathrm{DS}} = 5\,\mathrm{V}$, $V_{\mathrm{GD}} = -5\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



(c) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -7\,\mathrm{V}$, $V_{\mathrm{GS}} = 0\,\mathrm{V}$



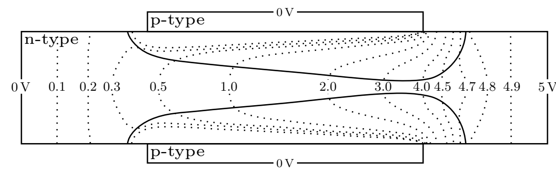
(d) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -8.21\,\mathrm{V}$, $V_{\mathrm{GS}} = -1.21\,\mathrm{V}$



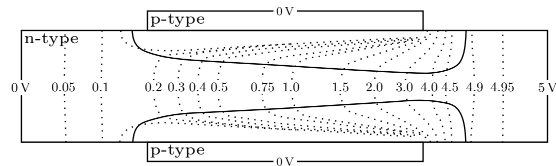
(e) $V_{\mathrm{DS}} = 7\,\mathrm{V}$, $V_{\mathrm{GD}} = -9.42\,\mathrm{V}$, $V_{\mathrm{GS}} = -2.42\,\mathrm{V}$

Figure 2.17

Simulated mobile electron distributions in the n-type channel of a Si JFET with gate a length 2.5 times greater than its channel depth, calculated from simultaneous solutions to both the continuity and Poisson equations in two-dimensions for a range of drain-source, gate-drain and gate-source bias voltages, V_{DS}, V_{GD} and V_{GS}, respectively, assuming field-dependent electron mobility. Solid lines within the channel represent 50% depletion of the majority carriers while the dotted lines correspond with 10% and 90% depletion contours. Reprinted [adapted] from [68].



(a) constant mobility



(b) field-dependent mobility

Figure 2.18

Simulated potential distribution in the n-type channel of a Si JFET with gate a length 2.5 times greater than its channel depth, calculated from simultaneous solutions to both the continuity and Poisson equations in two-dimensions for gate-source and drain-source bias voltages of $V_{\mathrm{GS}} = 0\,\mathrm{V}$ and $V_{\mathrm{DS}} = 5\,\mathrm{V}$, respectively, assuming (a) constant and (b) field-dependent electron mobility. Solid lines within the channel represent 50% depletion of the majority carriers while the dotted lines represent contours of constant potential. Reprinted [adapted] from [68].

of constant or field-dependent mobility and biased with gate-source and drain-source of 0 Vand 5 V, respectively, are presented in Figure 2.18. Despite the wider channel opening in Figure 2.18b a larger proportion of the voltage was found to appear in the region between the gates. This is a consequence of the lower carrier mobilities and translates into a higher channel resistance. Towards the centre of the channel, up to approximately half the length of the channel depth from the ends of the gate, the contours in both cases were found to satisfy the GCA, consistent with the prediction by Shockley. Strictly, the condition can be given by [73]

$$\left(\frac{\mathrm{d}b}{\mathrm{d}x}\right)^2 \ll \frac{1}{2} \tag{2.22}$$

where b represents the depth of the active channel region calculated using the ADA. The breakdown in the GCA at either end of the gate resulted in depletion layer widths there that are substantially smaller than that predicted by a one-dimensional analysis.

A comparison of Kennedy and O'Brian's numerically calculated channel current as a function of channel voltage with Shockley's approximate analytic analysis, assuming constant electron mobility, is presented in Figure 2.19. A key observation is that the GCA appears reliable at low voltages, but predicts a non-physical transition into saturation. As pinch-off is approached, the electric field along the channel becomes comparable to that in the space charge region, and the GCA loses its validity [69]. The approximate two-dimensional model

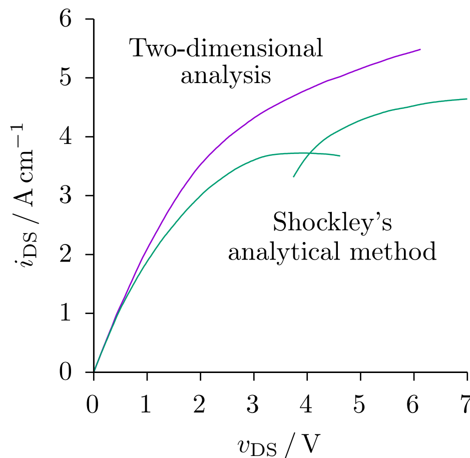


Figure 2.19

Simulated volt-ampere characteristics for a n-channel Si JFET with gate a length 2.5 times greater than its channel depth, calculated from simultaneous solutions to both the continuity and Poisson equations in two-dimensions (purple line) and using Shockley's approximate analytic 1-dimensional (below expop) and 2-dimension (above expop) techniques, for a gate-source bias voltage of 0 V and assuming constant electron mobility. Reprinted [adapted] from [68].

provided by Shockley, valid in strong saturation only, shows qualitative agreement with the numeric calculations with the current continuing to increase in a non-linear manner beyond the expop [68].

When an analytic expression is required the GCA can prove suitable prior to current saturation, but is physically unsuitable above pinch-off. A commonly employed approach is to use the drain-source voltage corresponding to the expop, termed the drain-source saturation voltage, in place of drain-source voltage when larger than this value [74]; this has the effect of maintaining the channel current at its expop value. Unfortunately, this approach fails to account for the finite output resistance in this region. Wu [75] has been successful in eliminating the discontinuities seen in two-part Shockley's analytical model through a curve fitting process; however, the solutions are very complicated and non-physical.

An accurate description of the channel potential beyond pinch-off requires that the Poisson equation be solved in two dimensions subject to complicated boundary conditions. In order to provide a continuous closed form solution Grebene and Ghandhi made use of the depletion approximation and the simplifying condition that beyond pinch-off the channel current is confined to a narrow region of depth

$$b_{\mathrm{min}} = \lim_{v_{\mathrm{d}} \to v_{\mathrm{d,sat}}} b(x) = \frac{i_{\mathrm{DS}}}{env_{\mathrm{d,sat}} Z}, \tag{2.23}$$

where the carriers are assumed to travel at their saturation velocity, $v_{\mathrm{d,sat}}$ [74]. While the free carrier concentrations in the high field region was shown to deviate form the equilibrium value they showed that this did not greatly affect the calculations. An immediate consequence is that the voltage needed to achieve pinch-off at the drain is reduced below that of the expop;

however, because the value of $b_{\min}$ is typically very small in comparison to the channel depth this will have little impact on the discussion. The region between the source end of the channel and the pinch-off point, with length L_1, is appropriately calculated under the framework of the GCA while the remaining channel length, L_2, is solved using the two-dimensional Poisson equation with boundary conditions chosen to ensure continuity of the potential across the two regions.

In the specific case of a two gated symmetric device the narrow channel region will experience no net flow of charge across the line of symmetry. Splitting the device in half along this line the allows it to be treated as two separate single gate devices; the schematic cross-section for one device half is illustrated in Figure 2.20.

An approximate solution to the two-dimensional Poisson equation subject to the chosen boundary conditions provided a pinch-off length of

$$L_2 \approx \frac{2a}{\pi} \sinh^{-1} \frac{(v_{\mathrm{DS}} - v_{\mathrm{DS,sat}})\pi}{2\mathscr{E}_{\mathrm{c}} a} \tag{2.24}$$

where $v_{\mathrm{DS,sat}}$ is the instantaneous drain-source saturation voltage and the critical electric field, $\mathscr{E}_{\mathrm{c}}$, was defined the point of which the velocity attains 95% of $v_{\mathrm{d,sat}}$. Subsequently, the output resistance was approximately determined as

$$r_{\mathrm{o}} \approx \frac{L\mathscr{E}_{\mathrm{c}}}{i_{\mathrm{DS}}} \left\{ 1 + \left[\frac{(v_{\mathrm{DS}} - v_{\mathrm{DS,sat}})\pi}{2\mathscr{E}_{\mathrm{c}} a} \right]^2 \right\}^{1/2}. \tag{2.25}$$

which is found to increase with $v_{\mathrm{DS}} - v_{\mathrm{DS,sat}}$ in a non-linear manner. A investigation of the

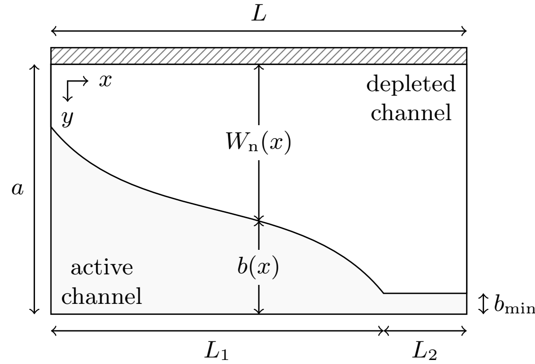


Figure 2.20

An illustration of the two part channel depletion model of Grebene and Ghandhi beyond channel pinch-off, developed in the framework of the abrupt depletion approximation, where L is the channel length, a is the channel depth, W_{n} is the depletion width in the n-type channel and b is the active channel depth. The depletion width in region 1, of length L_1, is calculated in the framework of the gradual channel approximation, while in region 2, of length L_2, it is solved using the two-dimensional Poisson equation with boundary conditions chosen to ensure continuity of the potential across the two regions. Reprinted [adapted] from [74].

temperature dependence of the output resistance, confirmed by experimental measurements, showed it to increase approximately linearly with temperature [74].

Very few JFET compact models have been presented, none of which are sufficiently comprehensive enough to accurately model the integrated circuit devices of interest to this work. While not the first to outline a model for an asymmetric dual gate JFET in the framework of the GCA, Van Halen appears to have been the first to address the mathematics specific for independent biasing [76]. The description of operation is analogous to that proposed by Shockley, but includes an additional term in the separable first-order non-linear homogeneous ordinary differential equation to account for the reduction in active channel depth by a second independent gate. While identifying its suitability for use in Simulation Program with Integrated Circuit Emphasis (SPICE) models the focus of his first paper was on a manual sequential parameter extraction methodology. This relied on major simplifications of the model equations and special characterisation techniques to be performed [76]. The simplification did enable him to outline how a voltage-controlled voltage-source (VCVS), when connected to the gate of the single gate SPICE JFET primitive, could account for the influence of a second gate potential, although this came at the expense of five experimentally determined fitting parameters.

These inadequacies were addressed in a subsequent paper which identified that an entirely new model, devoid of the restrictions of the primitive SPICE JFET model, was needed [77]. He was however unable to achieve a closed form solution for channel voltage at the expop point when field-dependent mobility was included [77].

Applying to Van Halen's model the same simplifications as performed in deriving the SPICE primitive JFET model from Shockley's model [78] Ding was able to derive a closed form two-part piecewise model that included independently controlled top and bottom gates that also accounted for field-dependent mobility when using an approximate drift velocity expression of the form

$$v_\mathrm{d} = \frac{\mu_{\mathrm{e},0}\mathscr{E}}{1 - \mathscr{E}/\mathscr{E}_\mathrm{c}}, \tag{2.26}$$

where $\mathscr{E}_\mathrm{c} = v_{\mathrm{d,sat}}/\mu_{\mathrm{e},0}$ represents the critical electric field at which the free-carrier velocity becomes saturated [79]. Specifically, he found that by expanding the square root terms of W_n for both gates and retaining the first two terms prior to integrating along the channel that the resulting form provided a explicit solution for the drain-source saturation voltage. The drain-source current and saturation voltage* were determined as

$$i_\mathrm{DS} = \frac{enZ\mu_{\mathrm{e},0}}{L}\left(1 + \frac{v_\mathrm{DS}}{\mathscr{E}_\mathrm{c}L}\right)^{-1}\left(M\,v_\mathrm{DS} - \frac{N}{2}\,v_\mathrm{DS}^2\right) \tag{2.27}$$

and

$$v_\mathrm{DS,sat} = \frac{1}{N}\left[\sqrt{(N\mathscr{E}_\mathrm{c}L)^2 + 2MN\mathscr{E}_\mathrm{c}L} - N\mathscr{E}_\mathrm{c}L\right], \tag{2.28}$$

*The error in the original paper has been corrected here.

respectively, where

$$M = a - \sqrt{K_\mathrm{t}(\phi_{0,\mathrm{t}} - v_\mathrm{GS})} - \sqrt{K_\mathrm{b}(\phi_{0,\mathrm{b}} - v_\mathrm{BS})}, \tag{2.29a}$$

$$N = \frac{1}{2}\left(\sqrt{\frac{K_\mathrm{t}}{\phi_{0,\mathrm{t}} - v_\mathrm{GS}}} + \sqrt{\frac{K_\mathrm{b}}{\phi_{0,\mathrm{b}} - v_\mathrm{BS}}}\right), \tag{2.29b}$$

$$K_\mathrm{t} = \frac{2\varepsilon_\mathrm{s} N_\mathrm{a}}{e N_\mathrm{d}(N_\mathrm{d} + N_\mathrm{a})} \tag{2.29c}$$

and

$$K_\mathrm{b} = \frac{2\varepsilon_\mathrm{s} N_\mathrm{b}}{e N_\mathrm{d}(N_\mathrm{d} + N_\mathrm{b})}, \tag{2.29d}$$

wherein $\phi_{0,\mathrm{t}}$ and $\phi_{0,\mathrm{b}}$ are the top and bottom gate contact potentials; v_BS denote the instantaneous bottom-gate voltage with respect to the source potential, comprised of bias and singnal voltages V_BS and v_bs, respectively; and N_a and N_b are the top-gate and bottom-gate net doping concentrations, respectively.

The turn-off voltage can be subsequently determined by setting the channel height at the source end to zero which provides the expression

$$v_\mathrm{GS,off} = \phi_{0,\mathrm{t}} - \frac{a^2}{K_\mathrm{t}}\left(1 - \frac{\sqrt{K_\mathrm{b}}}{a}\sqrt{\phi_{0,\mathrm{b}} - v_\mathrm{BS}}\right)^2. \tag{2.30}$$

The series expansions unfortunately have the undesirable effect of progressively underestimating the channel current as the gate-source voltage is increased above the turn-off voltage. Reasonable accuracy was achieved when applied to devices with gate lengths a low as 4 µm, although this will have invariably resulted in non-physical parameter values. Much like the SPICE primitive, this model becomes unsuitable for medium and long channel devices, increasingly so for those with large negative turn of voltages.

2.3.3 Experiment

The impracticality of diffusing dopants to form sufficiently deep gate and channel regions and the poor quality of those formed through ion implantation has prompted the ubiquitous adoption of epilayers for producing SiC JFETs. The low current and voltage requirement of signal level JFETs circumvent the need for complex structures typically adopted for power devices [80] and allows channel and gate regions to be formed from single homogenous epilayers. Devices intended for use in IC applications are subsequently required to have lateral channels and top mounted contacts. Unsurprisingly, the typical structure of n-channel lateral depletion-mode (NLDM) JFETs found in the literature closely resembles Figure 2.12. Variations in electrical characteristics do arise however on account of the device dimension and the choice of epilayer doping concentrations.

Acceptable quality SiC wafers became commercially available toward the end of the twentieth century. Subsequently, Scozzie *et al.* were some of the first to publish experimental

characteristics of 4H–SiC JFETs, reaching temperatures as high as 400 °C [58, 81, 82]. While their choice a buried gate structure is not compatible with IC fabrication the device operation is comparable to top gated variants. The nominal channel length, width and depth adopted were 5 µm, 1 mm and 0.2 µm, respectively. The buried gate epilayer was determined to have a net active Al acceptor doping concentration of $1.6 \times 10^{18}\,\mathrm{cm^{-3}}$ while the N donor concentration in the channel was found to be $2.4 \times 10^{17}\,\mathrm{cm^{-3}}$.

The quoted graphically extracted turn-off voltages measured approximately −6.5 V which agrees well with the one-dimension p-n junction theory for a step junction previously discussed [58]. A pertinent observation, however, is that ratio of the gate and channel doping concentrations will result in a large portion of the applied voltage not appearing on the channel side of the junction, thereby degrading the intrinsic gain of the device. They were successful in attributing the non-linear variation of the channel current with temperature to the combined influence of dopant ionisation, electron mobility and gate-channel p-n junction contact potential. The resulting saturation currents for zero applied gate-source bias, i_{DSS}, are presented in Figure 2.21. Using the observed value of i_{DSS} at room temperature, a corresponding value for the Hall effect mobility and a basic two level donor model they were able to estimate the donor ionisation as approximately 69 %.

While long identified as being suitable for use at high temperature and in environments exposed to high doses of radiation, attention for many years following became largely focused on exploiting SiC for high voltage power electronics applications. The maturity of growth and processing techniques and the emergence of a niche yet high profile market for resilient electronics has caused a resurgent interest by a small number of groups. The longest standing and most high profile contributors have been Neudeck *et al.* at the National Aeronautics and Space Administration (NASA) Glenn Research Center (GRC), who first presented SiC JFETs back in 2000 [83]. Case Western Reserve University (CWRU) have collaborated

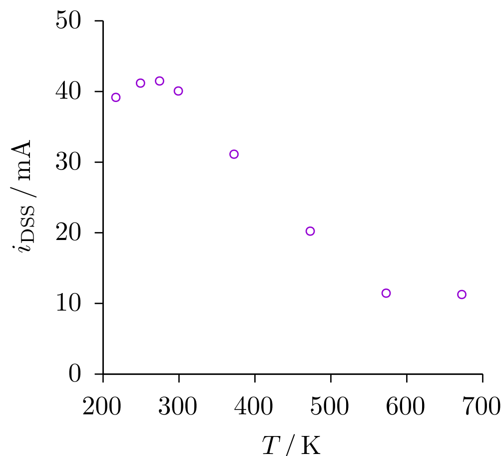


Figure 2.21

Experimental channel drain-source saturation current at zero applied gate-source voltage, i_{DSS}, for a n-channel buried gate JFET with Al doped gate concentration of $1.6 \times 10^{18}\,\mathrm{cm^{-3}}$, N doped channel concentration of $2.4 \times 10^{17}\,\mathrm{cm^{-3}}$, and channel length, width and depth of 5 µm, 1 mm and 0.2 µm, respectively. Reprinted [adapted] from [58].

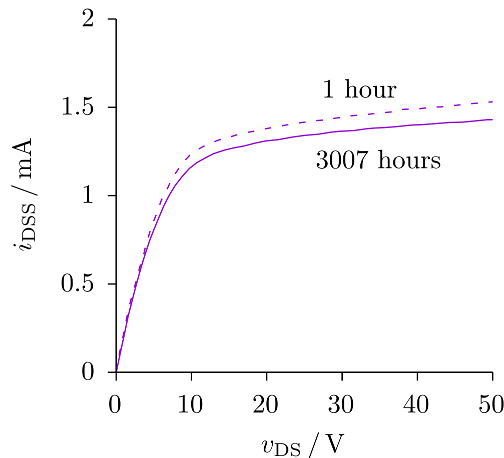


Figure 2.22

Drain current for zero applied gate-source bias, i_{DSS}, of a packaged 6H–SiC n-channel lateral depletion mode JFET with 200 µm wide and 10 µm long gate, measured during the 1st and 3007th hour of continuous operation at 500 °C. Reprinted [adapted] from [84].

with NASA GRC since 2005 with the goal of developing SiC ICs for remote sensing in high temperature systems. The perceived superiority of 6H–SiC during this time led to its adoption by both groups, although more recently they have made the switch to 4H–SiC [2]. The NLDM devices produced by each group closely resemble Figure 2.12 with gate, channel and body epilayers having nominal doping concentrations of $2\text{–}5 \times 10^{19}\,\mathrm{cm}^{-3}$, $1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $2 \times 10^{15}\,\mathrm{cm}^{-3}$, respectively, with thicknesses of 200 nm, 300 nm and 7 µm, respectively. Drain and source contact implants ($> 10^{19}\,\mathrm{cm}^{-3}$) were included to achieve low resistance ohmic contacts and reduce the series resistance.

Their most notable achievement to date is a demonstration of 10 000 hours of continuous operation at 500 °C [4,84]. During this time critical device parameters were shown to degrade by less than 10%. The channel current for a 6H–SiC JFET after a 1 hour burn-in and 3007 hours (approximately 4 months) of exposure is presented in Figure 2.22 [84]. Such changes, while small, can significantly impact circuit operation and so should be accounted for in any proposed circuit designs.

While their experimental results have proved the suitability of SiC JFETs for high temperature applications, little effort has been placed on developing accurate mathematical models suitable for implementation in circuit simulators. Each group continues to rely on either the primitive model provided by SPICE or a crudely modified version of Shockley's original analysis [83, 85, 86]. Figure 2.23 demonstrates the noticeable discrepancy between the simulated and experimental values. More recently NASA GRC have identified the importance of body bias on channel current and have provided analogies with a long channel MOSFET SPICE primitive model; however, this still remains less useful than the Ding model previously described, is highly non-physical and can only achieve agreement with experiment over narrow region of operation. In the latter case an attempt was made to indirectly account for the effect of substrate biasing through use of a modulated channel thickness. This however fails to account for the influence of channel potential on the bottom gate. In both

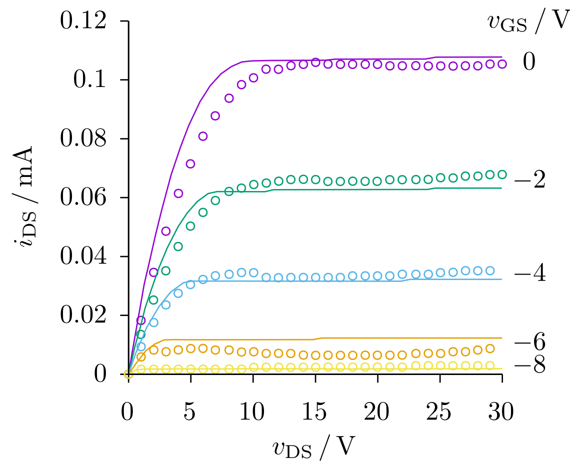


Figure 2.23
A comparison of experimental 6H–SiC n-channel lateral depletion mode JFET characteristics (points) and simulations with the SPICE primitive compact model (lines). Reprinted [adapted] from [83].

cases the absence of suitable thermal parameter models requires that separate device models be created for use at each temperature, thereby greatly inconveniencing the user and limiting the range of analysis that can be performed.

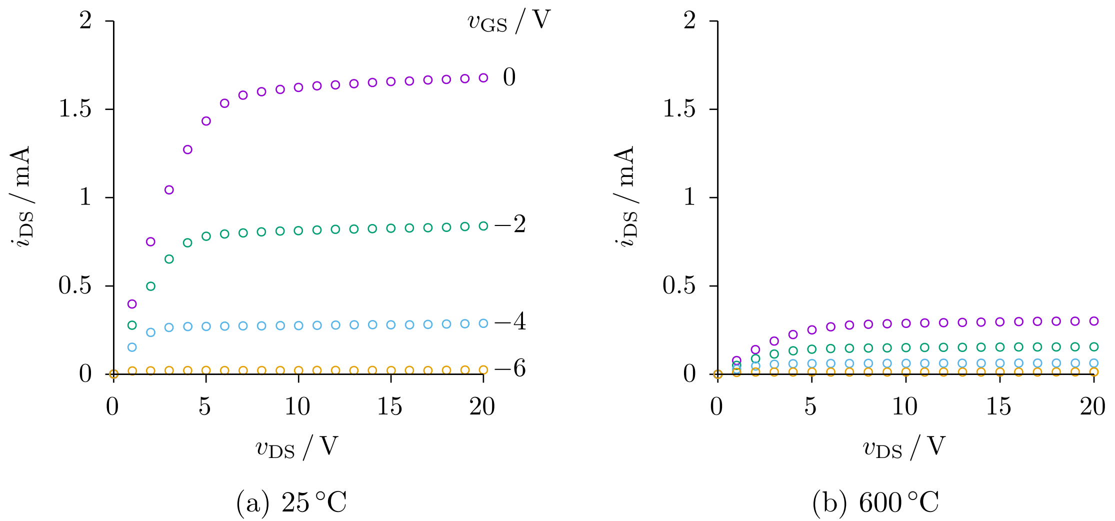
Their 6H–SiC devices have also been proven stable for over 4600 hours (approximately 6 months) of testing within low-earth-orbit on the international space station [87].

Active development of signal level SiC JFETs for hostile environment applications has up until recently been limited to NASA GRC, CWRU and Newcastle University (NU)'s Active Sensor Structures for Extreme Environments (ASTRO) group. Lately, however, Lien *et al.* have fabricated their own version of devices based on the specification outlined by NASA GRC and CWRU but using 4H–SiC. Their work so far has been limited to demonstrating single working devices but have achieved successful short term operation at 600 °C in air [8].

Example output characteristics for a device with gate width and length of 100 µm and 10 µm, respectively, at 25 °C and 600 °C are presented in Figure 2.24, exhibiting a maximum change in channel current in excess of 80 %. Unfortunately, the lack of data at intermediate temperatures provides limited insight into the direct current (DC) properties of the devices.

The product of a device's transconductance, g_m, and its output resistance, r_o, is termed the intrinsic voltage gain, $g_m r_o$ and is a transistor figure of merit defining the maximum achievable voltage gain for a given bias. An illustration of the observed transconductance at zero gate-source voltage, normalised to channel width, and the corresponding intrinsic voltage gain are presented in Figure 2.25 [8], where the average value of output resistance in saturation is believed to have been used. For the chosen device dimensions they observed the intrinsic voltage gain drop from 81.5 to 57.2 between 25 °C to 600 °C, representing a decrease of 30 %.

A reliability study showed that the transconductance changed by 3 % over an 90 hour period at 540 °C; however, a similar test at 600 °C resulted in a 30% change after only 1 hour [8]. It is likely that contact degradation is responsible for this drastic change with oxygen



(a) 25 °C

(b) 600 °C

Figure 2.24

Experimental output characteristics of a 4H–SiC n-channel lateral depletion mode JFET with gate width and length of 100 µm and 10 µm, respectively, measured at (a) 25 °C and (b) 600 °C. Reprinted [adapted] from [8].

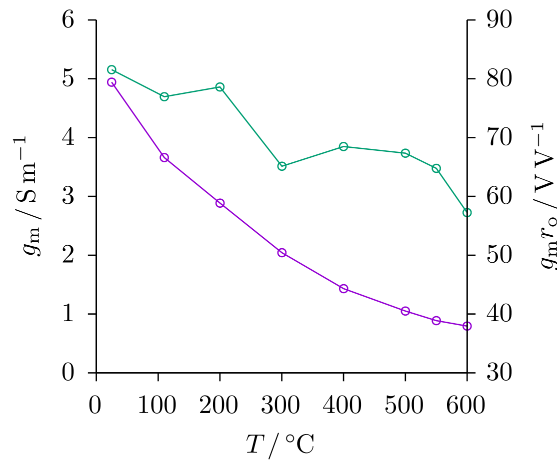


Figure 2.25

Experimental transconductance, g_m, and corresponding intrinsic gain, $g_m r_o$ of a 4H–SiC n-channel lateral depletion mode JFET with gate width and length of 100 µm and 10 µm, respectively, as a function of temperature, T. Reprinted [adapted] from [8].

from the atmosphere diffusing through the metal to the metal-semiconductor interface. The results suggest practical limits are placed on SiC devices that have not been properly designed to withstand high temperatures. The reported off-state current at a gate-source voltage of −9 V was found to increase from 6.31×10^{-9} A to 1.97×10^{-7} A in the same temperature range [8]. While small in comparison to convention semiconductors they remain far in excess of theoretical values achievable by 4H–SiC.

2.4 Integrated Circuit Amplifiers

2.4.1 Introduction

An electronic amplifier is intended to produce at its output port scaled versions of the voltage and current signals appearing at its input port. Voltage and current amplification is quantified by a system's voltage gain,

$$A_{\mathrm{v}} = \frac{\mathrm{d}v_{\mathrm{O}}}{\mathrm{d}v_{\mathrm{I}}} \tag{2.31a}$$

and current gain,

$$A_{\mathrm{i}} = \frac{\mathrm{d}i_{\mathrm{O}}}{\mathrm{d}i_{\mathrm{I}}}, \tag{2.31b}$$

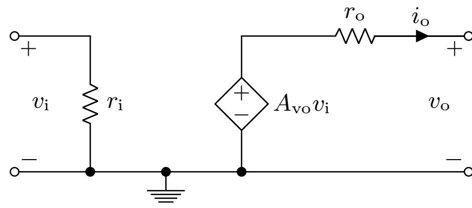
respectively, where v_{O} is the instantaneous output voltage which is the sum of the output bias voltage V_{O} and output signal voltage, v_{o}; v_{I} is the instantaneous input voltage which is the sum of the input bias voltage V_{I} and input signal voltage, v_{i}; i_{O} is the instantaneous output current which is the sum of the output bias current I_{O} and output signal current, i_{o}; and i_{I} is the instantaneous input current which is the sum of the input bias current I_{I} and input signal voltage, i_{i} [88]. In the majority of cases the amount of amplification is desirably independent of the input signal magnitude; such amplifiers are said to be linear. At low frequencies amplifiers may be broadly represented by any of the four related linear equivalent circuit models illustrated in Figure 2.26, where r_{i} and r_{o} represent corresponding small-signal Thévenin or Norton equivalent resistances looking into the input and output port, respectively, and the open-circuit voltage gain, A_{vo}, short-circuit current gain, A_{is}, short-circuit transconductance, G_{m}, and open-circuit transresistance, R_{m}, are defined by Equation 2.32; the ideal values for each of these parameters, however, depends on the input and output signals of interest.

Electronic circuits can be classified as being discrete or integrated (monolithic). Discrete circuit are comprised of separately sourced components*. In contrast an IC has its components and interconnections formed systematically on a common substrate via a shared fabrication process. The smaller dimensions afforded by this approach and the opportunity for simultaneous circuit fabrication provide strong economic benefits, whilst the inherent matching between devices formed in close proximity and the reduction of parasitics provide crucial performance advantages [17].

The functionality and versatility of operational amplifiers (op-amps) make them extremely attractive for use in all kinds of high performance circuits†. The topologies required to achieve the desirable properties can realistically only be achieved in specially designed and fabricated ICs due to the close tolerances demanded. Consequently, a number of practical restrictions are imposed on their design and construction. It is the goal of this section therefore to introduce the pertinent design topologies for NLDM FETs in addition to reviewing the designs and results published for SiC JFET amplifiers.

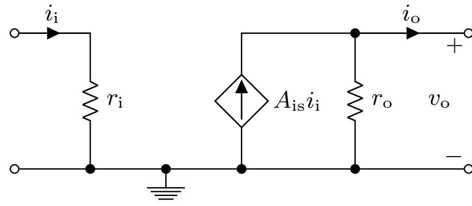
*Hybrid circuits are discrete circuit containing one or more integrated circuit components.

†The term operational amplifier was originally coined by Ragazzini *et al.* back in 1947 on account of their ability to perform useful mathematical operations such as addition and multiplication [89].



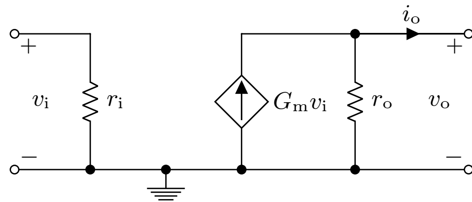
(a) Voltage

$$A_{vo} = \left.\frac{v_o}{v_i}\right|_{i_o=0} \tag{2.32a}$$



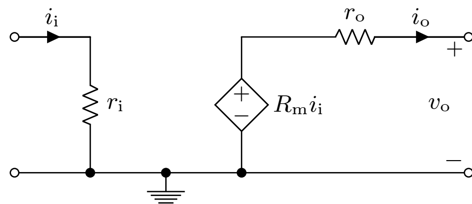
(b) Current

$$A_{is} = \left.\frac{i_o}{i_i}\right|_{v_o=0} \tag{2.32b}$$



(c) Transconductance

$$G_m = \left.\frac{i_o}{v_i}\right|_{v_o=0} \tag{2.32c}$$



(d) Transresistance

$$R_m = \left.\frac{v_o}{i_i}\right|_{i_o=0} \tag{2.32d}$$

Figure 2.26

Low-frequency small-signal amplifier equivalent circuits. Expression for the open-circuit voltage gain, A_{vo}; short-circuit current gain, A_{is}; short-circuit transconductance, G_m; and open-circuit transresistance, R_m, are defined in terms of input and output signal voltages, v_i and v_o, respectively, and input and output signal currents, i_i and i_o, respectively. Small-signal input and output resistances, r_i and r_o, respectively, are the Thévenin or Norton equivalent values seen looking into the input and output port, respectively. Reprinted [adapted] from [88].

2.4.2 Legacy Designs

Much of the existing body of work for NLDM FET IC amplifiers, such as those developed for GaAs metal-semiconductor field effect transistors (MESFETs) are directly applicable to SiC JFETs, provided the necessary conditions for their validity are met, while contextually relevant modifications are understandably required to accommodate the behaviour of SiC devices over their intended range of operation.

One of the simplest IC compatible NLDM FET amplifier designs is presented in Figure 2.27 [90]. Transistor J_1 operates as a common source (CS) amplifier with transistor J_2 acting both as a means of biasing and as a relatively high impedance load for J_1. J_3 acts as a common drain (CD) amplifier biased by J_4 providing a voltage buffer form the output of the first stage. R_3 provides a DC level-shift with minimal alternating current (AC) attenuation, provided its resistance value is much smaller than the output resistance of J_3 and J_4. Resistor R_1 and R_2 form an inverting amplifier configuration through use of negative voltage feedback; a discussion of which may be found any standard textbook [90, 91].

The simple circuit is fundamentally limited in a number of ways. The gain of the CS stage in the absence of the body-effect is limited to half the intrinsic gain of J_1. The condition by which the closed-loop voltage gain is independent of the open-loop voltage gain would require impractically large devices drawing extremely large bias currents. A bigger issue is that the DC level-shift across R_3 will depend both on its resistance and the bias current established by J_4; the variation of DC resistance between J_4 and R_3 with temperature will thus not provide a consistent voltage drop. The moderately high output resistance will also result in significant attenuation if a low resistance load is connected. It is also worth noting that the output signal in this case will be out of phase with the input signal.

The circuit proposed by Larson and Martin for use with GaAs MESFETs, as shown in Figure 2.28, includes a number of performance enhancement techniques [92]. Transistors

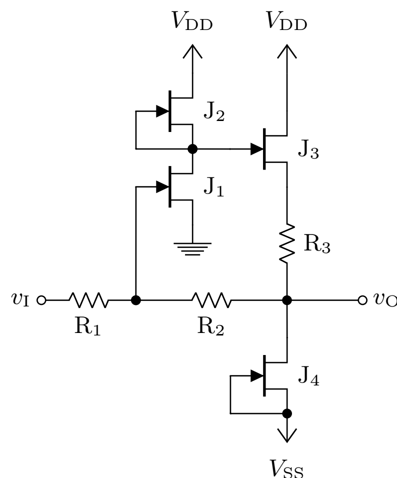


Figure 2.27

Basic single stage n-channel depletion mode FET inverting voltage amplifier with resistor based voltage level-shift and negative voltage feedback. Instantaneous input and output signals are denoted by v_I and v_O, respectively. Reprinted [adapted] from [90].

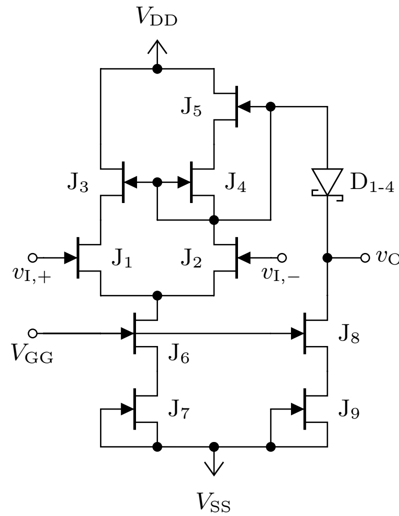


Figure 2.28
Single-stage n-channel lateral depletion-mode FET differential voltage amplifier with bootstrapped differential current-source load with voltage-follower, cascode current-sinks and diode level-shifting. Reprinted [adapted] from [92].

J_1 and J_2 form a differential pair with its common-mode point connected to a current-sink comprised of self-biased transistor J_7 and common-gate transistor J_6 included to provide current buffering and increase the output resistance of the sink [91]. The bias voltage, V_{GG}, could potentially be provided through use of a current mirror stage. The bootstrapping* source-follower transistor J_3 provides positive feedback from the amplifier output to the to corresponding side of the differential pair. A DC voltage drop is achieved using series connected diodes biased by a current-sink formed by cascode transistor pair J_8 and J_9. While suitable for fixed temperature and voltage supply operation the mutability of the voltage drop will result in poor output bias stability. The output impedance of the active-load transistor J_4, and thus the voltage gain, is enhanced by the bootstrap transistor J_5 which acts as a voltage-follower† [93].

An idealisation for the gain stage is shown in Figure 2.29 which can most simply be explained by first grounding the negative input and applying an input voltage to the positive terminal [93]. As the output is in phase with the input, applying a positive voltage to the gate of J_1 will cause the voltage at the drain of J_2 to increase. J_3 will thus force the drain of J_1 to increase by almost the same amount for an ideally unity gain voltage buffer. The voltage common-mode point is consequently forced to increase by an amount

$$\frac{v_s}{v_i} \approx g_{m,1}\, r_{o,1} \frac{1 + g_{m,3}\, r_{o,3}}{1 + g_{m,2}\, r_{o,2}} \tag{2.33}$$

where g_m and r_o represent a JFET's transconductance and output resistance, respectively, with subscripts denoting the corresponding numbered devices. The gain developed at the

*Bootstrapping involves feeding back the output to earlier parts of the circuits with the intention of providing increasing gain or impedance.

†This method is, however, only effective provided the influence of the body-effect is small.

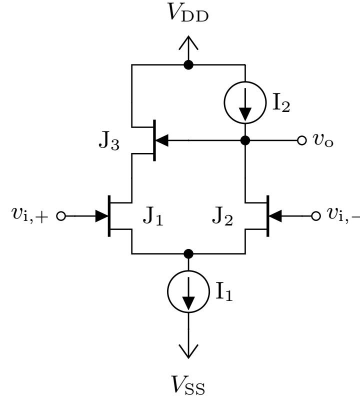


Figure 2.29

Gain enhanced differential pair using positive feedback. Reprinted [adapted] from [93].

common-mode point is subsequently enhanced by the intrinsic gain of J_2 to provide a total voltage gain of

$$\frac{v_o}{v_i} \approx g_{m,1} r_{o,1} (1 + g_{m,3}\, r_{o,3}). \tag{2.34}$$

which is roughly the differential voltage gain of two cascaded differential amplifiers. In the more realistic case where the FETs are subject to the body-effect and limited by non-ideal current-source and sink

$$\frac{v_o}{v_i} = \frac{g_{m,1} r_{o,1} \left[1 + (g_{m,2} + g_{mb})\, r_{o,2}\right]}{\left[1 + (g_{m,1} + g_{mb} + g_1)\, r_{o,1}\right](1 + g_1\, r_{o,2}) - (\alpha - g_2\, r_{o,1})\left[1 + (g_{m,2} + g_{mb})\, r_{o,2}\right]}, \tag{2.35a}$$

where

$$\alpha = \frac{g_{m,3}}{g_{m,3} + g_{mb,3} + r_{o,3}^{-1} + g_1 + g_2} \tag{2.36}$$

is the gain of the source-follower comprising J_3, g_1 and g_2 are the output conductances of the sink and source, respectively, and g_{mb} is the body transconductance. Importantly, the output resistance of the source must include the degrading influence of the body-effect on the FETs of which it is comprised. This can be represented by a parallel resistance following application of the source-absorption theorem [90]. When J_1 and J_2 are matched, $\alpha \approx 1$ and $g_m \gg g_1$, Equation 2.35 reduces to

$$\frac{v_o}{v_i} \approx \frac{g_m}{2g_2} \tag{2.37}$$

which indicates the dependence of the gain enhancement on the output impedance of the current-source load formed by J_4 and J_5 in Figure 2.28.

A two-stage op-amp proposed by Bayruns is illustrated in Figure 2.30. J_1 and J_2 act as a differential pair and J_3 acting as a biasing current-sink. J_4 provides positive feedback in the manner discussed previously. From Equation 2.37 the voltage gain enhancement is limited by the output resistance of active-load transistor J_5, although the arrangement does continue to provide differential to single-ended output conversion. J_6 and J_7 along with R_1 provide a DC level-shift similar to that used in Figure 2.27. The appropriate bias current is achieved

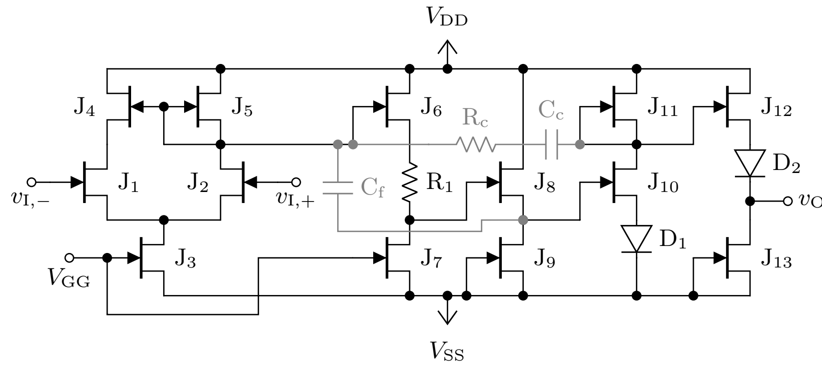


Figure 2.30

Two-stage n-channel lateral depletion-mode FET op-amp with bootstrapped differential current-source load both resistor and diode level-shifting and Miller compensation. Reprinted [adapted] from [94].

through use of a bias voltage; while not discussed the appropriate value was suggested to be attained from the output of a current mirror. J_8 and J_9 produce close to unity gain voltage buffering. Transistors J_{10} and J_{11} form a cascaded CS gain stage. The diode D_1 is included to provide a voltage level-shift sufficient to maintain J_9, in the preceding source-follower stage, in saturation. Lastly, transistors J_{12} and J_{13} form a class A output stage which includes a voltage drop through D_2 to correct for that due to D_1. Miller compensation is provided through capacitor C_c and and resistor R_c [94].

The final circuit of interest to this work was proposed by Scheinberg and is shown in Figure 2.31 [95]. The design utilises many of the features of the preceding examples alongside some additional ones. Many of the performance advantages discussed are afforded by the use of a semi-insulating (SI) substrate in order to mitigate the body-effect. In the design the positive common-mode range was increased to its maximum, at the expense of negative common-mode range, by clamping $v_{DS,4}$ close the minimum value possible to hold J_4 in saturation. The role of the level-shifter was to maintain this value independent of the supply voltages used while provide a DC voltage level-shift between the output of the differential amplifier, comprising of transistors J_1 to J_6, to the input of the proceeding CS amplifier stage at the gate of J_{17}.

The level-shifter design is based around a depletion mode (DM) FET current-mirror. For matched devices operating in saturation the current into the drain of J_{10} and J_{11} will be equal. The cascoding of J_7 with J_{10} and J_8 with J_{11} was performed to increase the output resistance of the current-sinks. Diodes D_1 and D_2 provide the necessary voltage level-shift to maintain current-sink transistor J_{12} in saturation, while D_3 to D_6 fulfil a similar role for J_7, J_8 and J_{10}. The dimensions of J_7, J_8, J_{10} and J_{11} were selected to operate at $v_{GS} = 0\,\mathrm{V}$ when operated using nominal supply voltages. The equivalent resistors labelled R_1 accommodate the majority of the voltage level-shift. The symmetry of the mirror results in the bias voltage at the gate of J_{17} being equal to the value of the gate of J_7 which for $v_{GS,7} = 0\,\mathrm{V}$ equals the voltage drop across $D_{1,2}$. The CS transistor at the start of the second stage can subsequently be biased to $v_{GS,17} = 0\,\mathrm{V}$ by setting the voltage at its source to $D_{1,2}$ voltage drop above

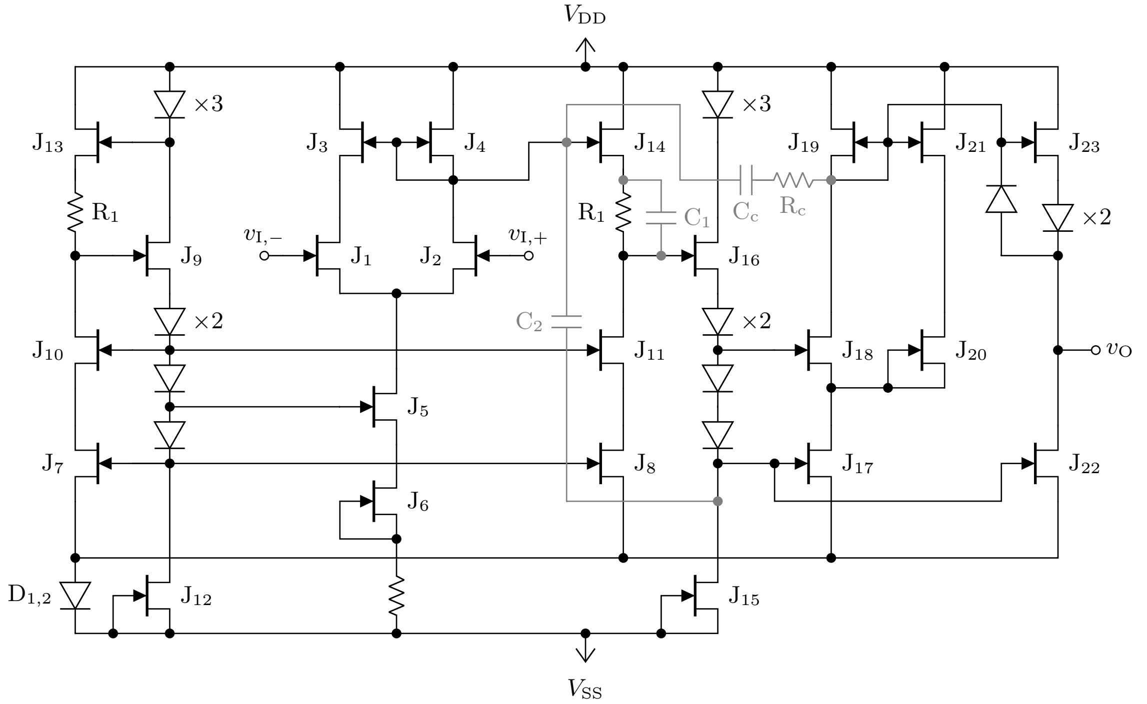


Figure 2.31
Two-stage n-channel lateral depletion-mode FET op-amp with bootstrapped differential current-source load, both resistor and diode level-shifting, current mirror biasing, bootstrapped current bleeder and Miller compensation. Reprinted [adapted] from [95].

the negative supply, V_{SS}. The mirroring action also results in the quiescent voltage $v_{DS,4}$ being equal to the voltage dropped across three diodes between V_{DD} and the gate of J_{13}. If the supply voltages are changed then $v_{GS,7}$, and thus $v_{DS,6}$, will change. As $v_{DS,4}$ tracks $v_{DS,6}$, it will vary by an amount equal to $v_{GS,7}$; however, $v_{DS,4}$ will vary by only a small amount in comparison to the power supply variation. The circuit is therefore able to achieve a high power supply rejection ratio (PSRR) and an almost temperature insensitive bias for the proceeding CS stage.

The second gain stage uses a current bleeder with positive feedback, via transistors J_{20} and J_{21}, respectively, to provide two degrees of voltage gain enhancement. Transistors J_{17} to J_{19} form a cascoded CS amplifier with gain $A_v \approx g_{m,17}\, r_{o,19}$ on account of the buffering effect of J_{18}. The bleeder circuit J_{20} allows the width of J_{18} and J_{19} to be reduced and thus $r_{o,19}$ to be increased without reducing $g_{m,17}$. The gain is further increased by using J_{21} to apply positive feedback to provide a total voltage gain of

$$A_v = \frac{g_{m,17}\, r_{o,19}}{1 - r_{o,19}/r_{o,20}}. \tag{2.38}$$

The current through the bleeder transistor J_{20} is controlled by the positive feedback provided by J_{21} which would otherwise remain fairly constant. Large voltage gain improvement is therefore achieved by selecting the widths for J_{20} and J_{21} to be less than or equal to J_{19}. The arrangement requires that J_{18} and J_{19} are matched, J_{20} and J_{21} are also matched and

Table 2.3
Experimental benchmark results for the circuit for the GaAs MESFET op-amp illustrated in in Figure 2.31 [95].

DC characteristics	
Common-mode range	$\pm 4\,\mathrm{V}$ from power rails
Output swing	$\pm 3\,\mathrm{V}$ from power rails
Common-mode rejection ratio	50 dB (100 kHz)
Open-loop gain	60 dB (100 kHz)
Power supply rejection ratio	1 MV/V
Output current	$\pm 25\,\mathrm{mA}$
AC characteristics ($C_\mathrm{l} = 5\,\mathrm{pF}$, $R_\mathrm{l} = 500\,\Omega$)	
Gain-bandwidth product	500 MHz ($C_\mathrm{c} = 0.5\,\mathrm{pF}$)
Phase margin	35° ($C_\mathrm{c} = 0.5\,\mathrm{pF}$)
Gain-bandwidth product	320 MHz ($C_\mathrm{c} = 1\,\mathrm{pF}$)
Phase margin	60° ($C_\mathrm{c} = 1\,\mathrm{pF}$)
Power bandwidth	100 MHz ($5\,\mathrm{V_{pp}}$ output, $C_\mathrm{c} = 1\,\mathrm{pF}$)
Slew rate	1500 V/µs ($C_\mathrm{c} = 1\,\mathrm{pF}$)
Output resistance	$25\,\Omega$
Power requirements	
power range	$\pm 5\,\mathrm{V}$ to $\pm 9\,\mathrm{V}$
supply current	47 mA

the width of J_{17} be the sum of the widths of J_{18} and J_{20}. A proviso is that the infinite gain alluded to by Equation 2.38 by matching J_{19} and J_{20} is not safely achievable due to the risk of $r_{o,19}$ becoming larger than J_{20} and causing the output to latch*.

The stability criteria was met by including $\mathrm{C_c}$ and $\mathrm{C_2}$ to provide Miller compensation, with $\mathrm{R_c}$ is included to limit the amount of signal feeding through the capacitor $\mathrm{C_c}$ to the output at high frequencies.

The reported properties for one such fabricated amplifier comprised of GaAs MESFETs are listed in Table 2.3 [95].

The fixed voltage drops provided by the diodes will be a strong function of temperature. While the diodes have a positive temperature coefficient (tempco), the voltage required to saturate the drain current of a FET will typically increase on account of the lowering of the threshold voltage and the increase of the series resistances. Another issue is change in bias current, supplied by the current-sink devices, with temperature. Placing a forward biased diodes in series with a epitaxial resistor having a negative tempco could provide sufficient stability. A specially designed active circuit may instead be required.

*Scheinberg opted for a ratio of 2:1.

2.4.3 Silicon Carbide Designs

Despite there being a large existing body of literature on SiC devices very little has been published on DM FET amplifiers for hostile environments. Relevant work has almost entirely originated from the collaborative effort of NASA GRC and CWRU. Preliminary circuits have been constructed by both groups with CWRU's focus being primarily on maximising voltage gain at high temperatures whilst NASA GRC have placed emphasis on lifetime studies for operation under extreme conditions. Pertinent developments from each group are discussed below.

NASA Glenn Research Center

NASA GRC have focused predominantly on investigating the mutability of the low-frequency voltage gain of passive-loaded 6H–SiC JFET CS amplifiers operated at elevated temperatures or under high dose radiation exposure [4, 84].

Figure 2.32a illustrates the results of a packaged CS amplifier comprised of a 6H–SiC JFET with gate width and length of 80 µm and 10 µm, respectively, and epitaxial resistor load at 25 °C and 500 °C for a positive, negative and substrate bias of 40 V, 0 V and 0 V, respectively. The results demonstrate absolute voltage gains in excess of 10 at 500 °C with very little variation down to room temperature. The low bandwidth is likely a result of parasitic capacitances introduced by the cabling used to perform the measurements. The corresponding variation in gain when operating at 500 °C, normalised to the value attained following a 100 hour burn-in period, is shown in Figure 2.32b. The circuit was found to survive continuous operation approaching 4000 hours (approximately 5 months) before failing,

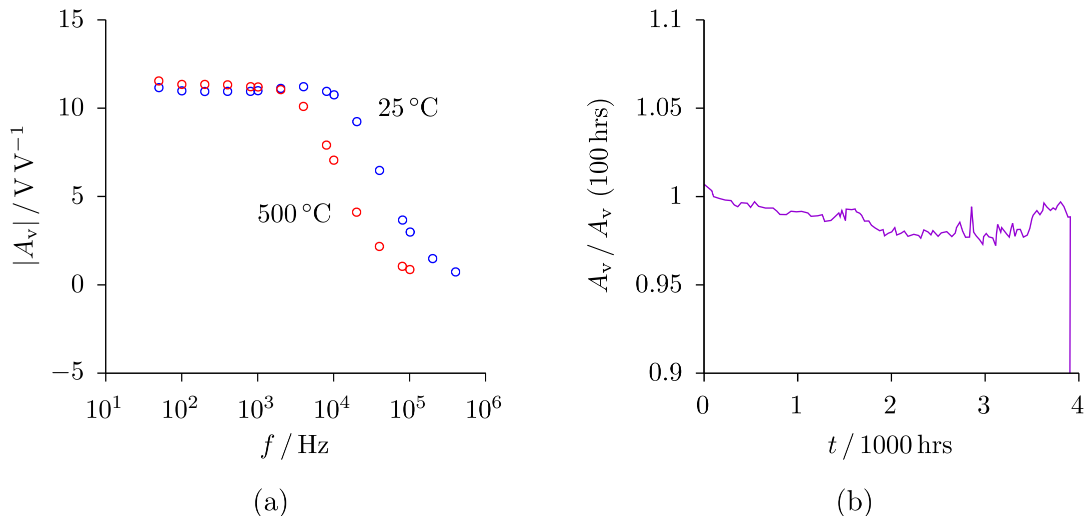
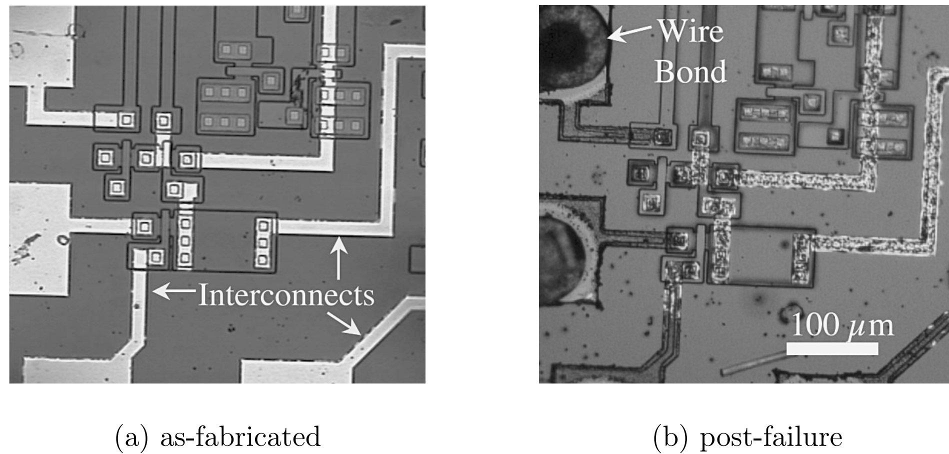


Figure 2.32

Prototype 6H–SiC integrated circuit common-source amplifier (a) gain-frequency characteristics at 25 °C (blue) and 500 °C (red) and (b) normalised low-frequency voltage gain variation over time for 500 °C operation following a 100 hour burn-in period. Reprinted [adapted] from [4].



(a) as-fabricated (b) post-failure

Figure 2.33
Optical micrographs a region of an 6H–SiC IC chip (a) as-fabricated and (b) following failure after thousands of hours operating at 500 °C while exposed to air. Reprinted [adapted] from [4].

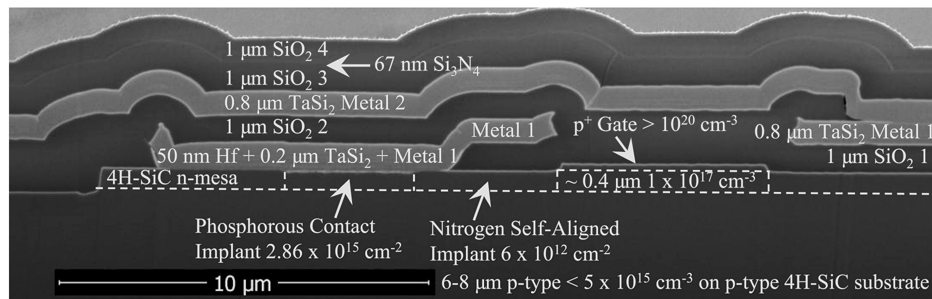


Figure 2.34
Annotated cross-sectional micrograph of a 4H–SiC JFET and passivated two-layer interconnect and dielectric stack. Reprinted [adapted] from [2].

while exhibiting a deviation of less than 3 %.

Failure during the initial lifetime studies were a result of a breakdown of the interconnects and contacts due to their exposure to oxygen [4]. Figure 2.33 provides a before and after optical micrographs for a set of contact and interconnects.

More recently they have successfully demonstrated a two layers $TaSi_2$ metallisation scheme using SiO_2 and Si_3N_4 for both isolation and protection from oxidation. Figure 2.34 is a cross-sectional micrograph showing a JFET and its connections.

With the aid of the two-layer metallisation scheme they have recently demonstrated a two-stage op-amp comprising of ten 4H–SiC JFETs each with 6 µm long and 200 µm wide gates. The variation of the op-amp's voltage gain for several thousand hours of continuous operation at 500 °C is presented in Figure 2.35 alongside the results for a single differential amplifier stage with and without a DC level-shifter [2]. While relatively stable the open-loop voltage gain is undesirably low on account of the intrinsic voltage gain of the JFETs. After 534 hours the op-amp was re-configured to operate as an inverting amplifier with an ideal

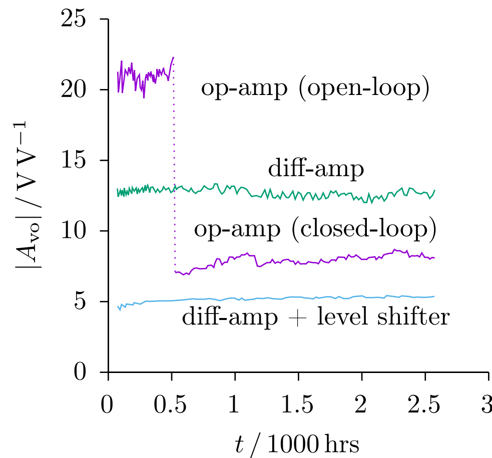


Figure 2.35

Measured differential small-signal voltage gain as a function of time for 4H–SiC voltage amplifiers operating at 500 °C, with supply voltages set to $V_{DD} = 45$ V and $V_{SS} = -15$ V. Reprinted [adapted] from [2].

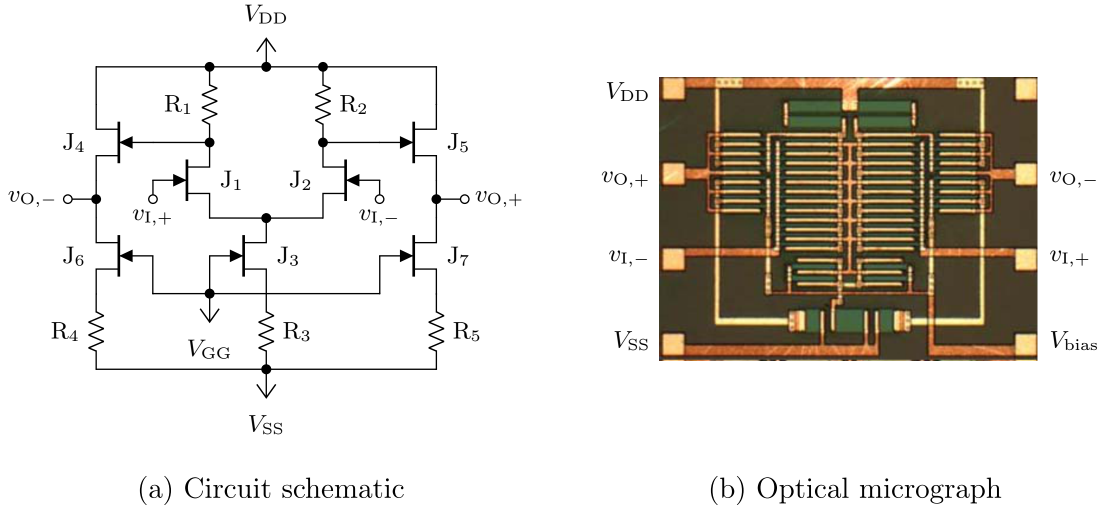
close-loop gain of roughly 8. The gain was however seen to vary by as much as 15 % over the remaining 2000 hours (approximately 3 months) of testing. Due to the low value of open-loop voltage gain the variation in the closed-loop gain will not be dominated by the feedback network [90]. Provided a larger open-loop gain can be achieved a passive feedback network comprising of a pair of resistors degrading evenly over time should have little impact on the closed-loop gain stability.

The variation in gain between the independent differential amplifiers with and without DC level-shifting suggests that the biasing arrangement is having a significant loading effect on the signal. The absence of a circuit schematic prevents further discussion. Providing this can be addressed the voltage gain of the two stage op-amp could be potentially increased by an order of magnitude for the same devices and supply voltages.

Case Western Reserve University

CWRU have designed and fabricated a variety of packaged fully monolithic 6H–SiC NLDM JFET differential amplifiers and have demonstrated successful operation between 25 °C and 576 °C. The transistors used had gate lengths as low as 10 µm. During the experimental testing of each circuit a positive supply voltages of 45 V was used with both the negative supply and gate bias voltages set to 0 V [96].

The simplest example demonstrated was a single-stage symmetric differential amplifier with resistive loads and source-follower outputs. A schematic for this circuit is presented in Figure 2.36 alongside an optical micrograph of a fabricated circuit. The load and bias resistors were formed from the same epilayer as the JFET channel and thus share a similar temperature dependence. The low-frequency differential voltage gain in this example is given



(a) Circuit schematic (b) Optical micrograph

Figure 2.36

Monolithic single-stage 6H-SiC differential voltage amplifier with resistor loads. Reprinted [adapted] from [96].

by the expression [96]

$$|A_{\mathrm{vd}}| \approx g_{\mathrm{m,1}} \left(r_{\mathrm{o,1}} \parallel R_1\right) \frac{g_{\mathrm{m,4}}}{g_{\mathrm{m,4}} + g_{\mathrm{mb,4}}} \tag{2.39a}$$

$$\approx g_{\mathrm{m,1}} R_1 \quad \text{for } r_{\mathrm{o,1}} >> R_1 \text{ and } g_{\mathrm{m,4}} >> g_{\mathrm{mb,4}}. \tag{2.39b}$$

The gain-bandwidth was measured as 3.6 MHz at 25 °C and 2.8 MHz at 600 °C which in the absence of frequency compensation is set by the dominant pole around $(r_{\mathrm{o,1}} \parallel R_1)(C_{\mathrm{gd,1}} + C_{\mathrm{gd,4}})$. The low-frequency common-mode rejection ratio (CMRR) and PSRR at 25 °C were found to be 74 dB above 80 dB, respectively. The low-frequency differential voltage gain determined as 35.8 dB at 25 °C and showed less than 1 dB reduction up to 600 °C. While not mentioned explicitly, the large values quoted are believed to result from the use of multi-finger devices, as evidenced by the shown in Figure 2.36b.

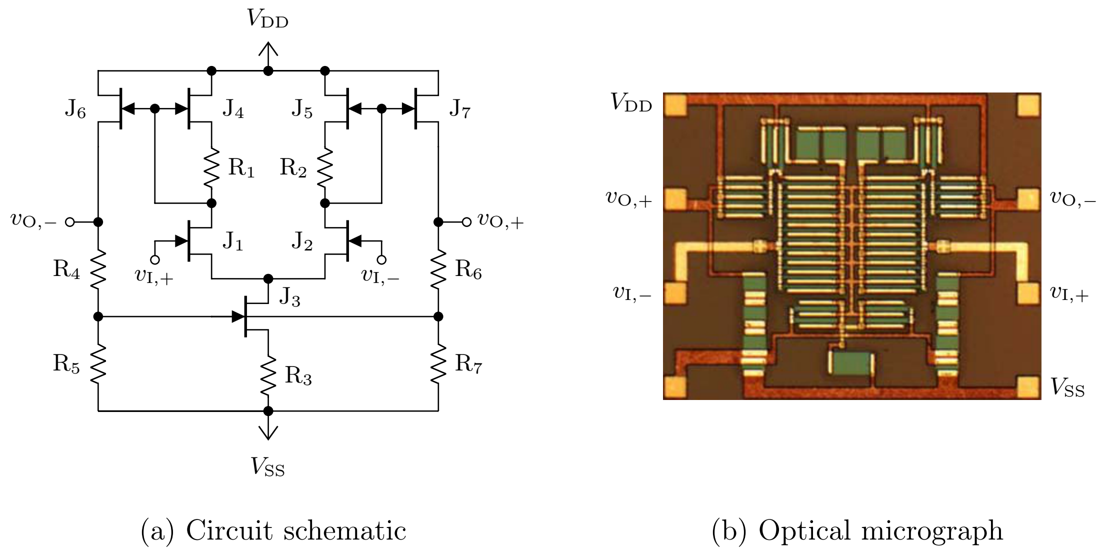
The next example given is a single stage differential amplifier with active-loads and common-mode voltage feedback. A schematic for this circuit is presented in Figure 2.37 alongside a corresponding optical micrograph of a fabricated circuit [96]. The differential voltage gain in the absence of the body-effect should be

$$|A_{\mathrm{vd}}| \approx g_{\mathrm{m,1}} \left(r_{\mathrm{o,1}} \parallel g_{\mathrm{m,4}}\, r_{\mathrm{o,4}}\, R_1\right) \tag{2.40a}$$

$$\approx g_{\mathrm{m,1}}\, r_{\mathrm{o,1}}. \tag{2.40b}$$

The observed low-frequency differential gain at 25 °C was found to be 44 dB and provided a gain-bandwidth of 4.7 MHz [96]. Common-mode feedback to the gate of the current-sink was provided via resistors R_4 to R_7 in order to improve the CMRR.

In the third example a pair of transistors were cascoded with the differential pair as illustrated in Figure 2.38. Common-mode feedback was also added to the cascode transistors.



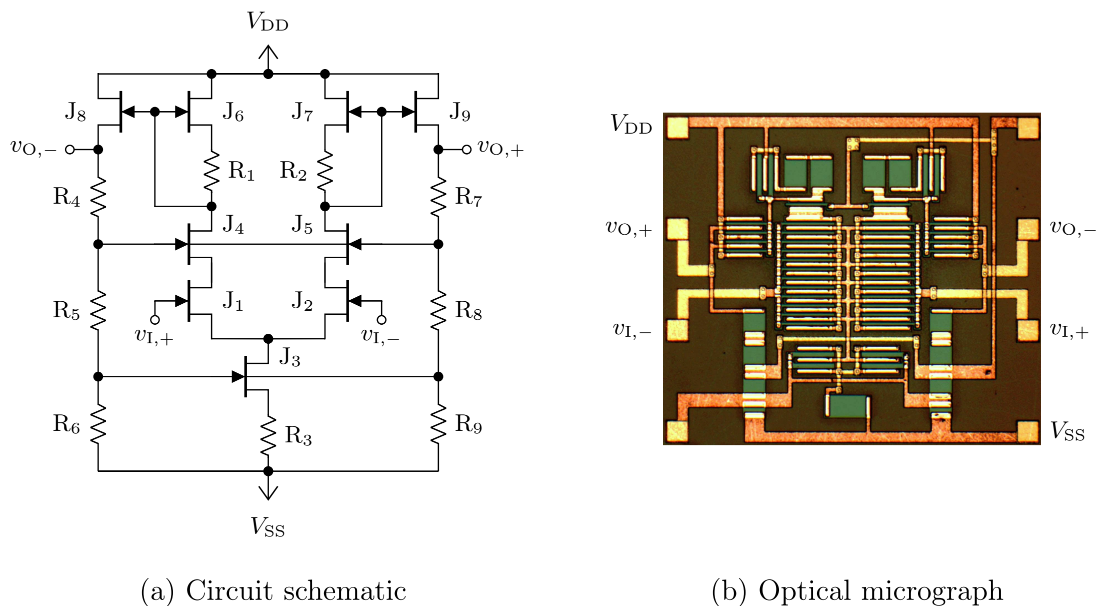
(a) Circuit schematic (b) Optical micrograph

Figure 2.37
Monolithic single-stage 6H-SiC differential voltage amplifier current-source loads and common-mode voltage feedback. Reprinted [adapted] from [96].

The low-frequency voltage gain is then given by the expression

$$|A_{\mathrm{vd}}| = g_{\mathrm{m},1}\,(g_{\mathrm{m},4}\,r_{\mathrm{o},4}\,r_{\mathrm{o},1} \parallel g_{\mathrm{m},6}\,r_{\mathrm{o},6}\,R_1)\,. \tag{2.41}$$

The last example involves a cascade of the active-load and passive-load stages previously mentions, although, without intermediate level-shifting. Voltage gains of 73.2 dB and 69.2 dB



(a) Circuit schematic (b) Optical micrograph

Figure 2.38
Monolithic single-stage 6H-SiC differential voltage amplifier current-source loads, common-mode voltage feedback and cascoded drivers. Reprinted [adapted] from [96].

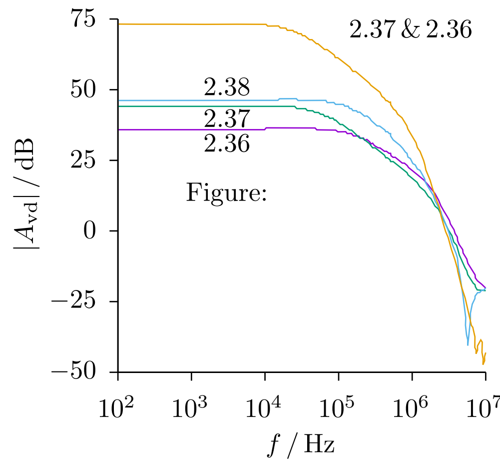
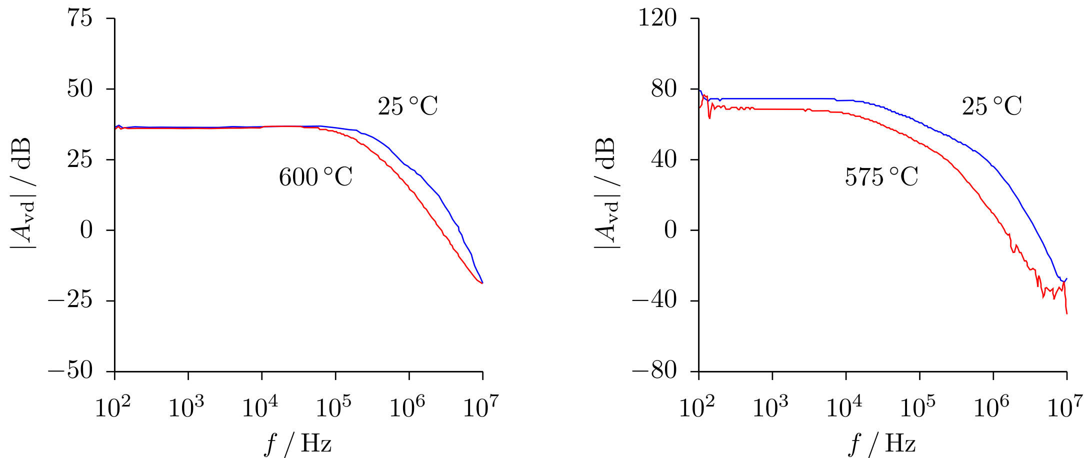


Figure 2.39

Measured differential voltage gains at room temperature with $V_{\mathrm{DD}} = 45\,\mathrm{V}$, $V_{\mathrm{SS}} = V_{\mathrm{GG}} = 0\,\mathrm{V}$ for each of the various amplifier configurations. Reprinted [adapted] from [96].

at 25 °C and 576 °C, respectively, were achieved with this arrangement, which would be considered suitable for the vast majority of applications requiring op-amps [96].

A comparison of the magnitude responses for each of these circuits at 25 °C is presented in Figure 2.39. High and low temperature plots for the circuit in Figure 2.36 and a cascode of the circuits Figure 2.38 are also present in Figure 2.40a and Figure 2.40b, respectively. The results clearly demonstrate the suitability of SiC JFETs for constructing high temperature op-amps; however, the major issue of bias point stability still needs to be addressed.



(a) Single-stage with passive-load.

(b) Two-stage with passive- and active-loads.

Figure 2.40

Measured differential small-signal voltage gains at room temperature with $V_{\mathrm{DD}} = 45\,\mathrm{V}$, $V_{\mathrm{SS}} = V_{\mathrm{GG}} = 0\,\mathrm{V}$ for (a) the passive-loaded amplifier in Figure 2.36 and (b) a cascade of the circuit in Figure 2.37, without voltage level-shifting, with that in Figure 2.36, at 25 °C and 600 °C. Reprinted [adapted] from [96].

One continuing problem does appear to be the low circuit yield. A yield of just 54% from a total 46 single-stage differential amplifiers has been reported more recently by the same group [83].

CHAPTER

3

Carrier Models

3.1 Introduction

A quantum mechanical treatment is warranted to account for the electronic properties of crystalline solids [35]. The associated energies of permissible electron states is encapsulated in a materials electronic band structure and depend heavily on the underlying crystal structure and atomic composition. Pertinent information gleaned from experiment and band theory calculations of 4H–SiC may be subsequently incorporated into simpler and more exoteric semiclassical models which are well suited for describing the operation of conventional semiconductor devices. Moreover, this approach provides the means for suitable analytical expressions to be derived that are ideally suited for use by circuit simulators.

This chapter first derives an appropriate analytical expression for the intrinsic density of states (DOS) as a function of energy, $N(E)$, suitable for the two lowest conduction bands in 4H–SiC close to their respective minima. Post hoc modifications are then applied to better represent the extrinsic DOS. The significance of impurity band formation is briefly discussed. Self-consistent calculations are subsequently performed to determine the equilibrium majority carrier concentration, Fermi level and band gap energy as a function of temperature for device pertinent N and Al doping concentrations. The results are used to develop and validate more computationally efficient approximate models suitable for use in circuit simulations.

The second part of this chapter is concerned with the effect of multiple anisotropic and non-parabolic conduction bands on the low-field electron mobility in 4H–SiC. A semiclassical electron conductivity model based on a solution to the Boltzmann equation in the relaxation-time approximation was developed and appropriate weighting functions for the scattering time and conductivity effective mass are identified. A complete high-temperature n-type 4H–SiC semiclassical conductivity model is subsequently produced.

3.2 Intrinsic Conduction Band Density of States

In a crystalline solid of finite size a limited number of discrete states are available within any given volume of $\boldsymbol{k}$–space [37], where $\boldsymbol{k}$ denotes the electron wave vector whose magnitude is

inversely proportional to the electron wavelength, λ, according to

$$k = \frac{2\pi}{\lambda}. \tag{3.1}$$

While $\boldsymbol{k}$–space states are uniformly distributed, their associated energies, $E(\boldsymbol{k})$, are not. An analytical expression for $N(E)$ first requires an analytic expression for these dispersions [35] which must be accurate for all energies up to those where the applicable electron occupancy probability, $f(E)$, becomes negligible [37]. Cyclotron resonance provide an accurate and direct means of experimentally determining the curvature about the lowest band minimum [21] while band theory calculations can be used to provide information about the higher energy variation [30, 40].

With the reference energy set to the respective conduction band minimum, E_c; the $\boldsymbol{k}$–space axes centred at an M–point in the Brillouin zone; and k_x, k_y and k_z directed along the M–Γ, M–K and M–L directions, respectively, an appropriate expression for the band dispersion in one of the M_c equivalent bands suitable for all energies of interest for either of the two lowest conduction bands in 4H–SiC is given by

$$E(\boldsymbol{k}) = \frac{\hbar^2}{2}\left[\frac{k_x^2}{m_{xx}^*} + \frac{k_y^2}{m_{yy}^*} + \frac{k_z^2}{m_{zz}^*\,(1+AE)}\right], \tag{3.2}$$

where m_{xx}^*, m_{yy}^* and m_{zz}^* are the principle axis components of the effective mass* tensor and A is a first order dispersion parameter derived from $\boldsymbol{k}\cdot\boldsymbol{p}$ theory [30]. Constant energy surfaces in $\boldsymbol{k}$–space are therefore ellipsoids that become progressively prolate along the direction of k_z as E increases above E_c.

The change of variables

$$\kappa_x = k_x\left(\frac{m^*}{m_{xx}^*}\right)^{1/2}, \tag{3.3a}$$

$$\kappa_y = k_y\left(\frac{m^*}{m_{yy}^*}\right)^{1/2} \tag{3.3b}$$

and

$$\kappa_z = k_z\left[\frac{m^*}{m_{zz}^*(1+AE)}\right]^{1/2} \tag{3.3c}$$

defines a related $\boldsymbol{\kappa}$–space, wherein the dispersion,

$$E(\boldsymbol{\kappa}) = \frac{(\hbar\kappa)^2}{2m^*}, \tag{3.4}$$

*The effect of the periodic potential in the Schrödinger equation on carrier motion is encapsulated in an effective mass [35].

is conveniently both parabolic and isotropic. The relationship between the incremental $\boldsymbol{k}$–space and $\boldsymbol{\kappa}$–space volumes, $\mathrm{d}\boldsymbol{k} = \mathrm{d}k_x\mathrm{d}k_y\mathrm{d}k_z$ and $\mathrm{d}\boldsymbol{\kappa} = \mathrm{d}\kappa_x\mathrm{d}\kappa_y\mathrm{d}\kappa_z$, respectively, is

$$\mathrm{d}\boldsymbol{k} = (m^*)^{-3/2}\left(m^*_{xx}m^*_{yy}m^*_{zz}\right)^{1/2}(1+AE)^{1/2}\,\mathrm{d}\boldsymbol{\kappa}. \tag{3.5}$$

The Brillouin zone contains the same number of $\boldsymbol{k}$–space states as the crystal contains unit cells; the large number present in a macroscopic crystal allows a sum over $\boldsymbol{k}$–space to be replaced by an integral without perceptible error. The transformation is given by [29]

$$\sum_{\boldsymbol{k}} \equiv \frac{\Omega}{(2\pi)^3}\int_{\boldsymbol{k}} \mathrm{d}\boldsymbol{k}, \tag{3.6}$$

where $\Omega/(2\pi)^3$ is the unit $\boldsymbol{k}$–space volume wherein Ω is the direct–space volume.

In accordance with the Pauli exclusion principle each $\boldsymbol{k}$–space state can simultaneously accept two electrons with opposite spin directions*, meaning the density of electron states is twice as large as the density of $\boldsymbol{k}$–space states [29, 37]. The number of electron states per unit volume of direct–space within a differential energy range $\mathrm{d}E$ is therefore given by

$$N(E)\mathrm{d}E = \frac{1}{4\pi^3}\int_{\boldsymbol{k}} \mathrm{d}\boldsymbol{k} \tag{3.7}$$

where the volume integral is taken over the region of $\boldsymbol{k}$–space bounded by energy contours E and $E + \mathrm{d}E$ [97]. Substituting Equation 3.5 into Equation 3.7, recognising from spherical symmetry that

$$\int_{\boldsymbol{\kappa}} \mathrm{d}\boldsymbol{\kappa} = 4\pi\kappa^2\mathrm{d}\kappa \tag{3.8}$$

and accounting for the M_c equivalent conduction band minima gives

$$N(E)\mathrm{d}E = M_\mathrm{c}\frac{\kappa^2}{\pi^2}(m^*)^{-3/2}\left(m^*_{xx}m^*_{yy}m^*_{zz}\right)^{1/2}(1+AE)^{1/2}\,\mathrm{d}\kappa. \tag{3.9}$$

After rearranging a substituting for Equation 3.4 and its derivative,

$$\mathrm{d}\kappa = \left(\frac{m^*}{2\hbar^2 E}\right)^{1/2}\mathrm{d}E, \tag{3.10}$$

into Equation 3.9 provides a corresponding energy-space definition

$$N(E)\mathrm{d}E = M_\mathrm{c}\frac{8\sqrt{2}\pi}{h^3}\left(m^*_{xx}m^*_{yy}m^*_{zz}\right)^{1/2}\left(E + AE^2\right)^{1/2}\mathrm{d}E. \tag{3.11}$$

The form of Equation 3.11 differs from that for a band with parabolic dispersion due to the inclusion of a $(1 + AE)^{1/2}$ term. This improved model appropriately predicts progressively higher $N(E)$ with increasing E. This will influence dopant ionisation and carrier transport properties, particularly at high temperatures which are of interest for this work.

*In units of $\hbar$, the spin angular momentum for an electron can be plus or minus one half [18].

Alternatively, each conduction band can be treated as having a DOS effective mass

$$m_{\mathrm{e}}^{\mathrm{d}}(E) = M_{\mathrm{c}}^{2/3}\left(m_{xx}^{*}m_{yy}^{*}m_{zz}^{*}\right)^{1/3}(1+AE)^{1/3} \tag{3.12a}$$

$$= m_{\mathrm{e}}^{\mathrm{d}}(0)\,(1+AE)^{1/3}, \tag{3.12b}$$

where

$$m_{\mathrm{e}}^{\mathrm{d}}(0) = M_{\mathrm{c}}^{2/3}\left(m_{xx}^{*}m_{yy}^{*}m_{zz}^{*}\right)^{1/3} \tag{3.12c}$$

denotes the DOS effective mass at the bottom of the conduction band.

High frequency cyclotron resonance measurements provide principle axis tensor components for each equivalent minimum of the first conduction band of $m_{xx}^{*} = 0.58(1)\,m_{\mathrm{e}}$, $m_{yy}^{*} = 0.31(1)\,m_{\mathrm{e}}$ and $m_{zz}^{*} = 0.33(1)\,m_{\mathrm{e}}$, where m_{e} is the free electron rest mass. [21]. Intrinsic band structure calculations provide values for the first and second conduction band dispersion parameters of $A_1 = 0.77\,\mathrm{eV}^{-1}$ and $A_2 = 0.83\,\mathrm{eV}^{-1}$, respectively, and principle axis effective mass tensor components for each of the three equivalent minima of the second conduction band of $m_{xx}^{*} = 0.74\,m_{\mathrm{e}}$, $m_{yy}^{*} = 0.17\,m_{\mathrm{e}}$ and $m_{zz}^{*} = 0.80\,m_{\mathrm{e}}$ [30]; the strong agreement with experimentally determined values in the first conduction band provides strong support for those in the higher energy band.

3.3 Electron Concentration

The arrangement of electrons in phase–space* can be described by the distribution function $f(\boldsymbol{r}, \boldsymbol{k}, t)$, where $\boldsymbol{r}$ is the direct–space vector and t the time. The total conduction electron concentration is determined from the sum of electrons over all conduction band states in the first Brillouin zone [35]

$$n(\boldsymbol{r}, t) = \frac{1}{\Omega}\sum_{\boldsymbol{k}} f(\boldsymbol{r}, \boldsymbol{k}, t) \tag{3.13a}$$

$$= \frac{1}{4\pi^3}\int_{\boldsymbol{k}} f(\boldsymbol{r}, \boldsymbol{k}, t)\mathrm{d}\boldsymbol{k} \tag{3.13b}$$

$$= \int_{E_{\mathrm{c}}}^{\infty} N(E) f(\boldsymbol{r}, E, t)\mathrm{d}E. \tag{3.13c}$$

The distribution function can be approximately determined from solutions to the semiclassical Boltzmann equation, although in the specific case of a homogeneous semiconductor in thermodynamic equilibrium this reduces to the the Fermi-Dirac distribution [97],

$$f_0(E) = \frac{1}{1+\mathrm{e}^{(E-E_{\mathrm{F}})/(k_{\mathrm{B}}T)}}, \tag{3.14}$$

where E_{F} is the Fermi level, k_{B} the Boltzmann constant and T the absolute thermodynamic temperature.

*Six-dimensional position–momentum–space.

A high concentration of majority carriers will modify the lattice periodic potential and alter the DOS as determined for an intrinsic semiconductor [9]. Band theory calculations however suggest the influence to be small for the doping concentrations of interest [39].

Random spatial variation of the electrostatic potential energy, $V(\boldsymbol{r})$, realistically occurs in bulk semiconductors due to charge inhomogeneity. The macroscopic statistical average effect of the locally varying DOS can be pragmatically accounted for by averaging over all values of V [98, 99]. The thermodynamic equilibrium electron concentration in an n-type semiconductor can subsequently be expressed as [100]

$$n_0 = \int_{-\infty}^{\infty} \int_{-\infty}^{E-E_\mathrm{c}} N(E-V)\, F(V)\, f_0(E) \mathrm{d}V \mathrm{d}E \tag{3.15a}$$

where

$$F(V) = (\sqrt{\pi} G)^{-1} \mathrm{e}^{-\frac{V^2}{G^2}} \tag{3.15b}$$

is an appropriate Gaussian weighting function, with normalised standard deviation,

$$G = \left(\frac{N_\mathrm{d}^+ + N_\mathrm{a}^-}{4\pi^2 \varepsilon_\mathrm{s}^2} e^4 \lambda \right)^{1/2}, \tag{3.15c}$$

wherein N_d^+ and N_a^- are ionised donor and acceptor concentrations, respectively, and λ is an appropriate screening length. The Coulomb potential of a donor impurity will be modified by the presence of nearby free electrons and ionised impurities and the total screening length [100]

$$\lambda = \left(\lambda_\mathrm{e}^{-2} + \lambda_i^{-2} \right)^{-1/2}, \tag{3.15d}$$

is comprised of an electron screening length, which for a non-degenerate semiconductor may be expressed as [100]

$$\lambda_\mathrm{e} = \left(\frac{\varepsilon_\mathrm{s} k_\mathrm{B} T}{e^2 n} \right)^{1/2}, \tag{3.15e}$$

and an impurity screening length [100]

$$\lambda_i = \left[\frac{\varepsilon_\mathrm{s} k_\mathrm{B} T}{e^2 N_\mathrm{d}^+ \left(1 - N_\mathrm{d}^+ / N_\mathrm{d}\right)} \right]^{1/2} + \Gamma\left(\tfrac{4}{3}\right) \left[\frac{4\pi \left(N_\mathrm{d} + N_\mathrm{a}\right)}{3} \right]^{-1/3}, \tag{3.15f}$$

where Γ is the gamma function.

While the optical band gap energy will remain unchanged the covariant movement of E_c and E_v with respect to E_F produces a tailing of both the conduction band and valence band DOS into the band gap, causing the experimental electrical band gap energy, E_g, to be lowered [9]. The movement of states to lower energies will also influence the location of E_F, and hence demand a self-consistent treatment.

To correctly account for the distribution of permissible states below E_c Equation 3.15

should be expressed as

$$n_0 = \frac{8\sqrt{2\pi}}{h^3 G}\left(m_{\mathrm{e}}^{\mathrm{d}}\right)^{3/2}\int_{-\infty}^{\infty}\int_{-\infty}^{E-E_{\mathrm{c}}}\frac{\left[\left(E-E_{\mathrm{c}}-V\right)\left(1+A\left|E-E_{\mathrm{c}}-V\right|\right)\right]^{1/2}}{\left[1+\mathrm{e}^{(E-E_{\mathrm{F}})/k_{\mathrm{B}}T}\right]\mathrm{e}^{(V/G)^2}}\mathrm{d}V\mathrm{d}E. \quad (3.16)$$

The modulus of the energy term in the square-root function is required to remove the symmetry in the resulting DOS expression.

The double integral in Equation 3.16 needs to be solved numerically and therefore must be transformed into a tractable form. Making the substitutions $E = E_{\mathrm{c}} + k_{\mathrm{B}}T\epsilon$ and $V = G\nu$ the double integral can be written as

$$\int_{-\infty}^{\infty}\int_{-\infty}^{k_{\mathrm{B}}T\epsilon/G}\frac{\left[\left(k_{\mathrm{B}}T\epsilon-G\nu\right)\left(1+A\left|k_{\mathrm{B}}T\epsilon-G\nu\right|\right)\right]^{1/2}}{\left[1+\mathrm{e}^{\epsilon-(E_{\mathrm{F}}-E_{\mathrm{c}})/k_{\mathrm{B}}T}\right]\mathrm{e}^{\nu^2}}\left|\frac{\partial\left(V,E\right)}{\partial\left(\nu,\epsilon\right)}\right|\mathrm{d}\nu\mathrm{d}\epsilon. \quad (3.17)$$

Substituting for the value of the Jacobian determinant

$$\left|\frac{\partial\left(V,E\right)}{\partial\left(\nu,\epsilon\right)}\right| = \begin{vmatrix}\frac{\partial V}{\partial\nu} & \frac{\partial V}{\partial\epsilon}\\ \frac{\partial E}{\partial\nu} & \frac{\partial E}{\partial\epsilon}\end{vmatrix} = \begin{vmatrix}G & 0\\ 0 & k_{\mathrm{B}}T\end{vmatrix} = Gk_{\mathrm{B}}T, \quad (3.18)$$

and applying the additional parameter normalising substitutions, $E_{\mathrm{F}} = k_{\mathrm{B}}T\epsilon_{\mathrm{F}}$, $E_{\mathrm{c}} = k_{\mathrm{B}}T\epsilon_{\mathrm{c}}$, $A = \left(k_{\mathrm{B}}T\right)^{-1}\alpha$ and $G = k_{\mathrm{B}}T\gamma$, produces

$$n_0 = N_{\mathrm{c}}\frac{2}{\pi}\int_{-\infty}^{\infty}\int_{-\infty}^{\epsilon/\gamma}\frac{\left[\left(\epsilon-\gamma\nu\right)\left(1+\alpha\left|\epsilon-\gamma\nu\right|\right)\right]^{1/2}}{\left(1+\mathrm{e}^{\epsilon-\epsilon_{\mathrm{F}}+\epsilon_{\mathrm{c}}}\right)\mathrm{e}^{\nu^2}}\mathrm{d}\nu\mathrm{d}\epsilon, \quad (3.19a)$$

where

$$N_{\mathrm{c}} = 2\left(\frac{2\pi m_{\mathrm{e}}^{\mathrm{d}}k_{\mathrm{B}}T}{h^2}\right)^{3/2} \quad (3.19b)$$

is the conduction band effective density of states and $m_{\mathrm{e}}^{\mathrm{d}}$ the DOS effective mass at E_{c}.

While Equation 3.19 predicts an exponentially decreasing DOS into the band gap an Anderson transition will eventually occur [100]. The energy at which the DOS switches from a state of non-localisation to a state of localisation depends on the nature of wave functions involved, but can be taken to be approximately $E_{\mathrm{c}} - 2G$ [100].

The expression for the extrinsic DOS,

$$N'(\epsilon) = N_{\mathrm{c}}\frac{2}{\pi}\int_{-\infty}^{\epsilon/\gamma}\left[\left(\epsilon-\gamma\nu\right)\left(1+\alpha\left|\epsilon-\gamma\nu\right|\right)\right]^{1/2}\mathrm{e}^{-\nu^2}\mathrm{d}\nu \quad (3.20)$$

cannot be represented in terms of existing functions and so must be solved using generalised numerical techniques. The long computation times associated with the resulting double integral in Equation 3.19a can be avoided by observing that γ is independent of ϵ. Equation 3.20 therefore need only be calculated once for each T, after which the tabulated values may be used by the outer integral with intermediate values of ϵ determined through interpolation.

For low to moderate doping concentrations or at low temperatures γ will be small and Equation 3.19a can be appropriately approximated by

$$n_0 \approx N_\mathrm{c}\frac{2}{\sqrt{\pi}}\int_0^\infty \frac{\left(\epsilon+\alpha\epsilon^2\right)^{1/2}}{1+\mathrm{e}^{\epsilon-\epsilon_\mathrm{F}+\epsilon_\mathrm{c}}}\mathrm{d}\epsilon. \tag{3.21}$$

Typical junction field effect transistor (JFET) channel doping concentrations will satisfy this requirement, although the implanted drain and source contact regions will not. The integral in Equation 3.21 is similar in form to the Fermi transform, $F_{1/2}(\epsilon_\mathrm{F}-\epsilon_\mathrm{c})$, but includes an additional $(1+\alpha\epsilon)^{1/2}$ term in the numerator. This integral will hereafter be referred to as the modified Fermi transform of order one-half.

In 4H–SiC appreciable occupation of the second conduction band occurs at relatively modest temperatures. For a given f_0 the total n_0 is subsequently determined from the arithmetic sum of the concentrations in both bands [17, 35]

$$n_0 = \sum_{x=1}^{2} n_{0,x} = n_{0,1} + n_{0,2}. \tag{3.22}$$

In carrier transport calculations it is however required that each band be treated separately, albeit with the possibility of scattering taking between them. This is due to the fact that the kinetic energy, $E-E_\mathrm{c}$, and transport properties for an electron in the second conduction band will be different than in the first for a given E.

3.4 Hole Concentration

An expression for the equilibrium free hole concentration in each valence band, justifiably approximated as being parabolic, may be equivocally determined, *mutatis mutandis*, to be

$$p_0 = N_\mathrm{v}\frac{2}{\pi}\int_{-\infty}^{\infty}\int_{-\infty}^{\epsilon/\gamma}\frac{(\epsilon-\gamma\nu)^{1/2}}{(1+\mathrm{e}^{\epsilon+\epsilon_\mathrm{F}-\epsilon_\mathrm{v}})\mathrm{e}^{\nu^2}}\mathrm{d}\nu\mathrm{d}\epsilon \tag{3.23a}$$

where $\epsilon_\mathrm{v} = E_\mathrm{v}/k_\mathrm{B}T$ denoted the normalised valence band maximum and

$$N_\mathrm{v} = 2\left(\frac{2\pi m_\mathrm{h}^\mathrm{d} k_\mathrm{B} T}{h^2}\right)^{3/2} \tag{3.23b}$$

is the effective DOS for the valence band, wherein m_h^d is the appropriate scalar DOS effective mass. Equation 3.23a can be satisfactorily simplified at low temperature or for moderately doped samples to

$$p_0 = N_\mathrm{v}\frac{2}{\sqrt{\pi}}\int_0^\infty \frac{\epsilon^{1/2}}{1+\mathrm{e}^{\epsilon+\epsilon_\mathrm{F}-\epsilon_\mathrm{v}}}\mathrm{d}\epsilon. \tag{3.23c}$$

For Equation 3.23a the total screening length used in Equation 3.15c becomes

$$\lambda = \left(\lambda_\mathrm{h}^{-2}+\lambda_i^{-2}\right)^{-1/2}, \tag{3.24a}$$

where

$$\lambda_{\mathrm{h}} = \left(\frac{\varepsilon_{\mathrm{s}} k_{\mathrm{B}} T}{e^2 p} \right)^{1/2}, \tag{3.24b}$$

is the hole screening length and the impurity screening length becomes

$$\lambda_i = \left[\frac{\varepsilon_{\mathrm{s}} k_{\mathrm{B}} T}{e^2 N_{\mathrm{a}}^- \left(1 - N_{\mathrm{a}}^- / N_{\mathrm{a}}\right)} \right]^{1/2} + \Gamma\left(\tfrac{4}{3}\right) \left[\frac{4\pi \left(N_{\mathrm{d}} + N_{\mathrm{a}}\right)}{3} \right]^{-1/3}. \tag{3.24c}$$

3.5 Donor Ionisation

Imperfections in the crystal structure have a strong impact on the conductivity of a semiconductor. The ground-state of the non-bonding electron of an isolated monovalent substitutional donor impurity will take the place of an otherwise intrinsic conduction band state, but will have a localised wave function at an energy, $E_{\mathrm{d}} < E_{\mathrm{c},1}$ [45]. As the separation is typically much smaller than the band gap, doping is used ubiquitously to predictably control the conductivity in different regions of semiconductor devices.

N acts as a relatively shallow monovalent donor in 4H–SiC; unfortunately, under normal conditions the separation of E_{d} from from E_{c} is large enough to cause an appreciable portion of the donors to remain unionised at room temperature. This in turn influences the temperature dependence of the conductivity in the active channel region of the JFETs and in other related structures studied in this work.

As the wave functions of intrinsic band states extend throughout a crystal two electrons of opposite spin can be associated with the same value of $\boldsymbol{k}$ without appreciable electrostatic interaction between them. Conversely, the resulting charge density of a single electron occupying a localised defect state significantly raises the energy of the remaining degenerate states preventing further occupation [29, 37]. The modified Fermi-Dirac distribution

$$f_i(E) = \frac{1}{1 + \beta \mathrm{e}^{(E - E_{\mathrm{F}})/k_{\mathrm{B}} T}} \tag{3.25}$$

describes the most probable arrangement of electrons subject to this restriction. While there are β^{-1} similar wave functions to describe a possible ground state of an set of isolated donor levels, only one can be occupied at any one time [37].

The 1s type wave function of a monovalent donor in 4H–SiC is a combination of the wave functions of six electron states, comprised of three states each with two fold spin degeneracy. Four of these states are not individually symmetric due to the influence of the crystal field and consequently have higher ground state energies than the remaining two symmetric states [37]. The effective degeneracy factor can be conveniently expressed as

$$\beta_1^{-1} = \beta_{A_1}^{-1} + \beta_E^{-1} \mathrm{e}^{-\frac{E_{\mathrm{vo}}}{k_{\mathrm{B}} T}}, \tag{3.26}$$

where $\beta_{A_1}^{-1}$ and β_E^{-1} are 2 and 4, respectively [27]. Experimentally determined values of E_{vo} for N donors occupying hexagonal and cubic sites are 7.6 meV and 11 meV, respectively [26].

It is also true that an electron can be trapped in one of its many excited states [27, 101]; however, these states all lie very close to the conduction band edge and are readily merged with it for the moderate doping concentrations and temperatures of interest and may thus be omitted from the discussion and analysis [37].

At low doping concentrations, N_d, the impurities are far enough apart in direct–space such that their interaction is negligible and their wave functions remain highly localised on the atomic scale. Under such conditions it is appropriate to approximate $N_\mathrm{d}(E)$ as N_d degenerate levels located at E_d. Given that the probability of hole occupation at E_d is $1 - f_i(E_\mathrm{d})$ the concentration of ionised donors, N_d^+, can be written as

$$N_\mathrm{d}^+ = N_\mathrm{d}\left[1 - f_i(E_\mathrm{d})\right] \tag{3.27a}$$

$$= \frac{N_\mathrm{d}}{1 + \beta^{-1}\mathrm{e}^{(E_\mathrm{F}-E_\mathrm{d})/k_\mathrm{B}T}}. \tag{3.27b}$$

Impurities may be treated as non-interacting only under low concentrations. At higher concentrations the wave functions interact and form a band of levels. The tight binding approximation offers an appropriate model for such systems as the spacing between donor atoms is large enough for the overlap of their electron wave functions to remain sufficiently small [46]. Monovalent donors and acceptors can be treated as having hydrogenic ground state orbitals, therefore forming a 1s type band of levels. The solution to the appropriate energy transfer integral for a collection of hydrogenic impurities separated by a distance, R, is given by [46]

$$E(R) = \frac{e^2\xi}{4\pi\varepsilon_\mathrm{s}}\left(1 + \xi R\right)\mathrm{e}^{-\xi R}, \tag{3.28a}$$

where,

$$\xi = \hbar^{-1}\left[2m_\mathrm{e}^\mathrm{c}\left(E_\mathrm{c} - E_\mathrm{d}\right)\right]^{1/2}, \tag{3.28b}$$

wherein m_e^c is an appropriate conductivity effect mass. Notably, Equation 3.28a shows an exponential dependence on the separation distance between donors.

A random distribution of impurities suggests R should realistically follow a Poisson distribution. The average value of the transfer integral should therefore be approximately [46]

$$\langle E(R)\rangle = \int_0^\infty E(R)\,4\pi N_\mathrm{d}R^2\,\mathrm{e}^{-\frac{4}{3}\pi N_\mathrm{d}R^3}\,\mathrm{d}R. \tag{3.29}$$

Using the substitutions

$$R = \rho\,\xi^{-1} \tag{3.30a}$$

and

$$\zeta = -\frac{4}{3}\pi N_\mathrm{d}\xi^{-3} \tag{3.30b}$$

provides the computationally tractable result

$$\langle E(R)\rangle = \frac{e^2 N_\mathrm{d}}{\varepsilon_\mathrm{s}\xi^2}\int_0^\infty (1+\rho)\,\rho^2 \mathrm{e}^{\zeta\rho^2}\,\mathrm{d}\rho \tag{3.30c}$$

The total bandwidth is subsequently given by [46]

$$E_\mathrm{b} = 2\left|\langle E(R)\rangle\right|. \tag{3.31}$$

Solutions to Equation 3.31 are presented Figure 3.1 for typical values for N and Al. The results suggest that for $N_\mathrm{d} \leq 10^{17}\,\mathrm{cm}^{-3}$ or $N_\mathrm{a} \leq 10^{18}\,\mathrm{cm}^{-3}$ the band of levels is small enough to be adequately represented as occupying an N_d degenerate level at E_d; however, due to the exponential dependance of the bandwidth, higher concentrations require a energy dependent DOS to be used.

While the overlap of wave functions gives rise to a band of levels, for the doping concentrations of interest, the states will remain sufficiently localised. Metallic behaviour will not take place unless the average interatomic spacing is of the order of a few effective Bohr radii. If such states were to become delocalised then electrons would move to unpaired states at lower energy causing some atoms to have two non-bonding electrons while others to have none. A simple argument why this does not happen is that an ionised electron can only move to another ionised donor if the distance between the two impurities is small enough such that the other conduction electrons do not sufficiently screen the charge of the destination ion to the point at which the electron cannot be bound [29]. Observations of low temperature hopping conduction indicate the remaining presence of localised donor bands, with the activation energy of 3 to 5 meV relating to a slightly more delocalised region at the band centre [102, 103]. The localisation for the concentrations of interest are also confirmed by the experimental temperature dependence of bulk resistivity in N and Al doped

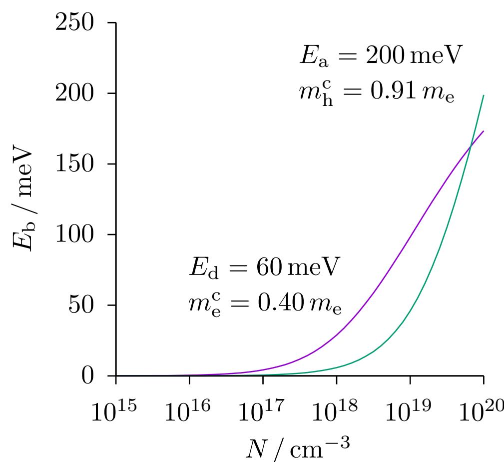


Figure 3.1

Theoretical monovalent ground-state impurity bandwidths calculated in framework of the tight binding approximation using approximate values applicable for N donors (purple) and Al acceptors (green) in 4H–SiC [46].

samples [48, 104–106].

While the exact distribution will be quite complicated one can approximate it as a uniform distribution such that [100]

$$N_\mathrm{d}(E) = \begin{cases} N_\mathrm{d}/E_\mathrm{b} & E_\mathrm{d} - \frac{1}{2}E_\mathrm{b} \le E \le E_\mathrm{d} + \frac{1}{2}E_\mathrm{b} \\ 0 & \text{otherwise} \end{cases} \tag{3.32a}$$

$$= N_\mathrm{d}\,\delta(E - E_\mathrm{d} + \tfrac{1}{2}E_\mathrm{b}, E_\mathrm{b}), \tag{3.32b}$$

with the modified Dirac delta function defined as,

$$\delta(a, b) = \begin{cases} b^{-1} & 0 \le a \le b \\ 0 & \text{otherwise} \end{cases}. \tag{3.33}$$

For a band of closely spaced levels a summation can again be expediently replaced by an integral and N_d^+ can thus be determined using

$$N_\mathrm{d}^+ = \int_{-\infty}^{\infty} \frac{N_\mathrm{d}(E)}{1 + \beta^{-1}\mathrm{e}^{(E_\mathrm{F}-E)/k_\mathrm{B}T}}\mathrm{d}E \tag{3.34a}$$

$$= \frac{N_\mathrm{d}}{E_\mathrm{b}} \int_{E_\mathrm{d}-\frac{1}{2}E_\mathrm{b}}^{E_\mathrm{d}+\frac{1}{2}E_\mathrm{b}} \frac{\mathrm{d}E}{1 + \beta^{-1}\mathrm{e}^{(E_\mathrm{F}-E)/k_\mathrm{B}T}}, \tag{3.34b}$$

which on making the substitutions $E = E_\mathrm{d} - \frac{1}{2}E_\mathrm{b} + k_\mathrm{B}T\epsilon$, $E_\mathrm{d} = k_\mathrm{B}T\epsilon_\mathrm{d}$ and $E_\mathrm{b} = k_\mathrm{B}T\epsilon_\mathrm{b}$ may be written in terms of normalised quantities as

$$= \frac{N_\mathrm{d}}{\epsilon_\mathrm{b}} \int_0^{\epsilon_\mathrm{b}} \frac{\mathrm{d}\epsilon}{1 + \beta^{-1}\mathrm{e}^{\epsilon_\mathrm{F}-\epsilon_\mathrm{d}+\frac{1}{2}\epsilon_\mathrm{b}-\epsilon}}. \tag{3.34c}$$

If $\epsilon > \epsilon_\mathrm{c} - \epsilon_\mathrm{d} + \epsilon_\mathrm{b}/2$ there is an overlap of the impurity band with the conduction band. In this situation the donors with $E_\mathrm{d} \ge E_\mathrm{c}$ cease to be localised and are able to readily donate an electron to the conduction band [9]; this is accounted for by an increase in the Fermi level.

Additionally, the donor ground state will follow the potential fluctuations due to the aforementioned charge inhomogeneity, causing a further spread of energy. Equation 3.15b can be used to modify Equation 3.34a to include the influence of the random variation, providing

$$N_\mathrm{d}^+ = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{N_\mathrm{d}(E-V)F(V)}{1 + \beta^{-1}\mathrm{e}^{(E_\mathrm{F}-E)/k_\mathrm{B}T}}\mathrm{d}V\mathrm{d}E \tag{3.35a}$$

$$= \frac{N_\mathrm{d}}{\sqrt{\pi}G} \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{\delta\left(E - E_\mathrm{d} + \frac{1}{2}E_\mathrm{b} - V, E_\mathrm{b}\right)}{[1 + \beta^{-1}\mathrm{e}^{(E_\mathrm{F}-E)/k_\mathrm{B}T}]\mathrm{e}^{(V/G)^2}}\mathrm{d}V\mathrm{d}E. \tag{3.35b}$$

Applying a change of variables and using the Jacobian determinant

$$\left|\frac{\partial (V, E)}{\partial (\nu, \epsilon)}\right| = G k_{\mathrm{B}} T, \tag{3.36}$$

provides

$$N_{\mathrm{d}}^{+} = \frac{N_{\mathrm{d}}}{\sqrt{\pi}} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{\delta(\epsilon - \gamma\nu, \epsilon_{\mathrm{b}}) \mathrm{e}^{-\nu^2}}{1 + \beta^{-1} \mathrm{e}^{\epsilon_{\mathrm{F}} - \epsilon_{\mathrm{d}} + \frac{1}{2}\epsilon_{\mathrm{b}} - \epsilon}} \mathrm{d}\nu \mathrm{d}\epsilon \tag{3.37a}$$

$$= \frac{N_{\mathrm{d}}}{2\epsilon_{\mathrm{b}}} \int_{-\infty}^{\infty} \frac{\mathrm{erf}\,(\epsilon/\gamma) - \mathrm{erf}\,[(\epsilon - \epsilon_{\mathrm{b}})/\gamma]}{1 + \beta^{-1} \mathrm{e}^{\epsilon_{\mathrm{F}} - \epsilon_{\mathrm{d}} + \frac{1}{2}\epsilon_{\mathrm{b}} - \epsilon}} \mathrm{d}\epsilon. \tag{3.37b}$$

A number of additional extrinsic effects will also act to reduce the energy separation between individual donors levels and the conduction band. The interaction between a neutral donor ion and its bound electron, for example, will in part be screened by the presence of the conduction electrons. In the case of a non-degenerate n-type semiconductor an estimate of this effect can be attained from [100]

$$\Delta E_{\mathrm{d}} = \frac{q^2}{4\pi\varepsilon_{\mathrm{s}} a_0'} \left\{ \frac{3}{8} - \frac{2\lambda_{\mathrm{e}}}{a_0'} \sin\left[\frac{a_0'}{2\lambda_{\mathrm{e}}} + 2\tan^{-1}\left(\frac{a_0'}{8\lambda_{\mathrm{e}}}\right)\right] \left(4 + \frac{a_0'^2}{16\lambda_{\mathrm{e}}^2}\right)^{-1} \right\} \tag{3.38a}$$

where

$$a_0' = \frac{4\pi\varepsilon_{\mathrm{s}}\hbar^2}{m_{\mathrm{e}}^{\mathrm{c}} e^2} \tag{3.38b}$$

is the effective Bohr radius of the hydrogenic donor impurity. A plot of Equation 3.38 at 25 °C and 400 °C are given in Figure 3.2. In light of the anisotropic nature of 4H–SiC the geometric mean of the conductivity effective mass principle components and dielectric constant were used in place of isotropic values. The results suggest that unless very high

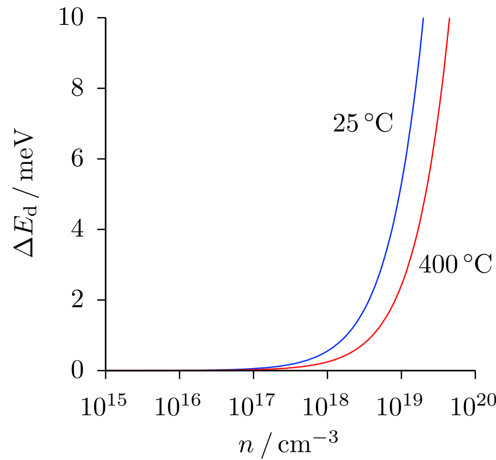


Figure 3.2

Theoretical shift of donor ground-state energy, E_{d}, due to screening by conduction electron, n, calculated under the assumption of non-degeneracy, calculated at 25 °C and 400 °C.

doping and temperature are considered their influence will be negligible, more so at elevated temperatures. A consequence of this effect is, however, that the greater the number of free electrons the greater the influence of electron-electron interactions and subsequently the easier it it for remaining electrons to be ionised [29]; such an effect thereby must be treated self-consistently.

For an anisotropic semiconductor such as 4H–SiC, it should also arise that E_d will vary somewhat with temperature due to inequivalent lattice expansion in different directions, causing the impurity state wave function to be modified [37]. Fundamental studies are required to assess such subtleties but are expected to have little influence in comparison to those effects already mentioned.

The mutability of the intrinsic bands and donors levels subsequently allow for a donor or acceptor energy to reside in the conduction band and valence band, respectively, as indicated by Equation 2.12. In such cases the atoms are again permanently ionised with the liberated electrons becoming free to take part in conduction [97]. Experimental results for N doped 4H–SiC presented in Figure 2.11 [48] identified a critical concentration close to $10^{19}\,\mathrm{cm}^{-3}$.

3.6 Acceptor Ionisation

Similarly, the concentration of ionised acceptors can be determined from a set of analogous equations. At low doping concentrations the interaction between acceptors impurities is again sufficiently small that they may be treated as N_a degenerate levels at energy E_a,

$$N_\mathrm{a}^- = \frac{N_\mathrm{a}}{1+\beta \mathrm{e}^{(E_\mathrm{a}-E_\mathrm{F})/k_\mathrm{B}T}}, \tag{3.39}$$

where $\beta = 2$ for each non-degenerate valence band in 4H–SiC.

Approximating the acceptor DOS by a uniform distribution,

$$N_\mathrm{a}(E) = N_\mathrm{a}\,\delta(E - E_\mathrm{a} + \tfrac{1}{2}E_\mathrm{b}, E_\mathrm{b}), \tag{3.40}$$

the ionised acceptor concentration can be expressed as

$$N_\mathrm{a}^- = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{N_\mathrm{a}(E-V)\,F(V)}{1+\beta \mathrm{e}^{(E-E_\mathrm{F})/k_\mathrm{B}T}}\mathrm{d}V\mathrm{d}E \tag{3.41}$$

$$= \frac{N_\mathrm{a}}{\sqrt{\pi}G}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \frac{\delta\left(E - E_\mathrm{a} + \frac{1}{2}E_\mathrm{b} - V, E_\mathrm{b}\right)}{[1+\beta \mathrm{e}^{(E-E_\mathrm{F})/k_\mathrm{B}T}]\mathrm{e}^{(V/G)^2}}\mathrm{d}V\mathrm{d}E \tag{3.42}$$

which on making the substitutions $E = E_\mathrm{a} - \frac{1}{2}E_\mathrm{b} + k_\mathrm{B}T\epsilon$, $E_\mathrm{a} = k_\mathrm{B}T\epsilon_\mathrm{a}$ and $E_\mathrm{b} = k_\mathrm{B}T\epsilon_\mathrm{b}$ may be written in terms of normalised quantities as

$$= \frac{N_\mathrm{a}}{2\epsilon_\mathrm{b}}\int_{-\infty}^{\infty} \frac{\mathrm{erf}\,(\epsilon/\gamma) - \mathrm{erf}\,[(\epsilon-\epsilon_\mathrm{b})/\gamma]}{1+\beta \mathrm{e}^{\epsilon+\epsilon_\mathrm{a}-\frac{1}{2}\epsilon_\mathrm{b}-\epsilon_\mathrm{F}}}\mathrm{d}\epsilon. \tag{3.43}$$

In contrast with N doped 4H–SiC, the predicted metal-insulator transition for Al dopants is experimentally observed taking place between $6.4\,\mathrm{cm}^{-3}$ and $8.7\times10^{20}\,\mathrm{cm}^{-3}$ [107–109].

Similar expressions to those derived in §3.5 can also be used for acceptors, and therefore for brevity are not repeated.

3.7 Charge Neutrality Equation

The equilibrium value of E_{F} used in the preceding equations is required to satisfy the charge neutrality condition [29]

$$n - p = N_{\mathrm{d}}^{+} - N_{\mathrm{a}}^{-}. \tag{3.44}$$

The problem requires a self-consistent numerical calculation which at high doping concentrations demands up to 10 iterations to achieve convergence of E_{F} to 0.1% tolerance.

The calculated results for the normalised free carrier concentrations, reduced Fermi level and extrinsic band gap for relevant device doping concentrations with zero compensation are presented in Figure 3.3 wherein variation of E_{c} and E_{v} with N_{d}^{+} and N_{a}^{-} is performed using the parameterised models of Persson *et al.*[*] [39], change in the intrinsic band gap is accounted for using the expression in [44] and screening of donors and acceptors by free carriers is included following the suggestions by Lee [100].

A visual illustration of the solution for 4H–SiC in thermal equilibrium is presented in Figure 3.4 for an intrinsic sample at 673 K, a moderately n-type sample at 300 K and a highly doped p-type sample at 300 K. A closer look at the total extrinsic conduction band DOS for moderate doping at high temperature is given in Figure 3.5 and is seen to differ greatly from that for a single parabolic band both at high and low energies. Presented alongside is the resulting distribution of electron energies which are also found differ greatly. As the transport properties vary between bands a two band model should strictly be used at high temperatures.

From the room temperature shift of the Raman longitudinal optical phonon plasma-coupled (LOPC) mode, Cuia *et al.* found that for a $5 \times 10^{17}\,\mathrm{cm}^{-3}$ nitrogen doped 4H–SiC sample, as determined by secondary ion mass spectroscopy (SIMS), the free electron concentration was approximately $2 \times 10^{17}\,\mathrm{cm}^{-3}$ ($N_{\mathrm{d}}^{+}/N_{\mathrm{d}} \approx 40\%$), which is in close agreement with these calculations, assuming a realistic partial inactivation of donors [110].

Compensation will influence the determined values which can understood from Figure 3.6. The compensation ratio [111],

$$K = \begin{cases} N_{\mathrm{a}}/N_{\mathrm{d}} & \text{for } N_{\mathrm{a}} < N_{\mathrm{d}} \\ N_{\mathrm{d}}/N_{\mathrm{a}} & \text{for } N_{\mathrm{d}} < N_{\mathrm{a}} \end{cases}, \tag{3.45}$$

should only be considered important for values above 5% [111]. The two common process induced intrinsic defects are the $\mathrm{Z}_{1/2}$ and $\mathrm{EH}_{6/7}$ centres, providing two acceptor levels and one donor level, respectively. Their concentrations are, however, much too small to influence the channel of gate epilayers, but could make a difference in lower doped buffer layers [112]. Interestingly, the electrons ionised from hexagonal donor sites due to compensation will act to screen the electrons on the k sites and facilitate their ionisation [48] which for low

[*]The expressions for these models were given in Equation 2.12.

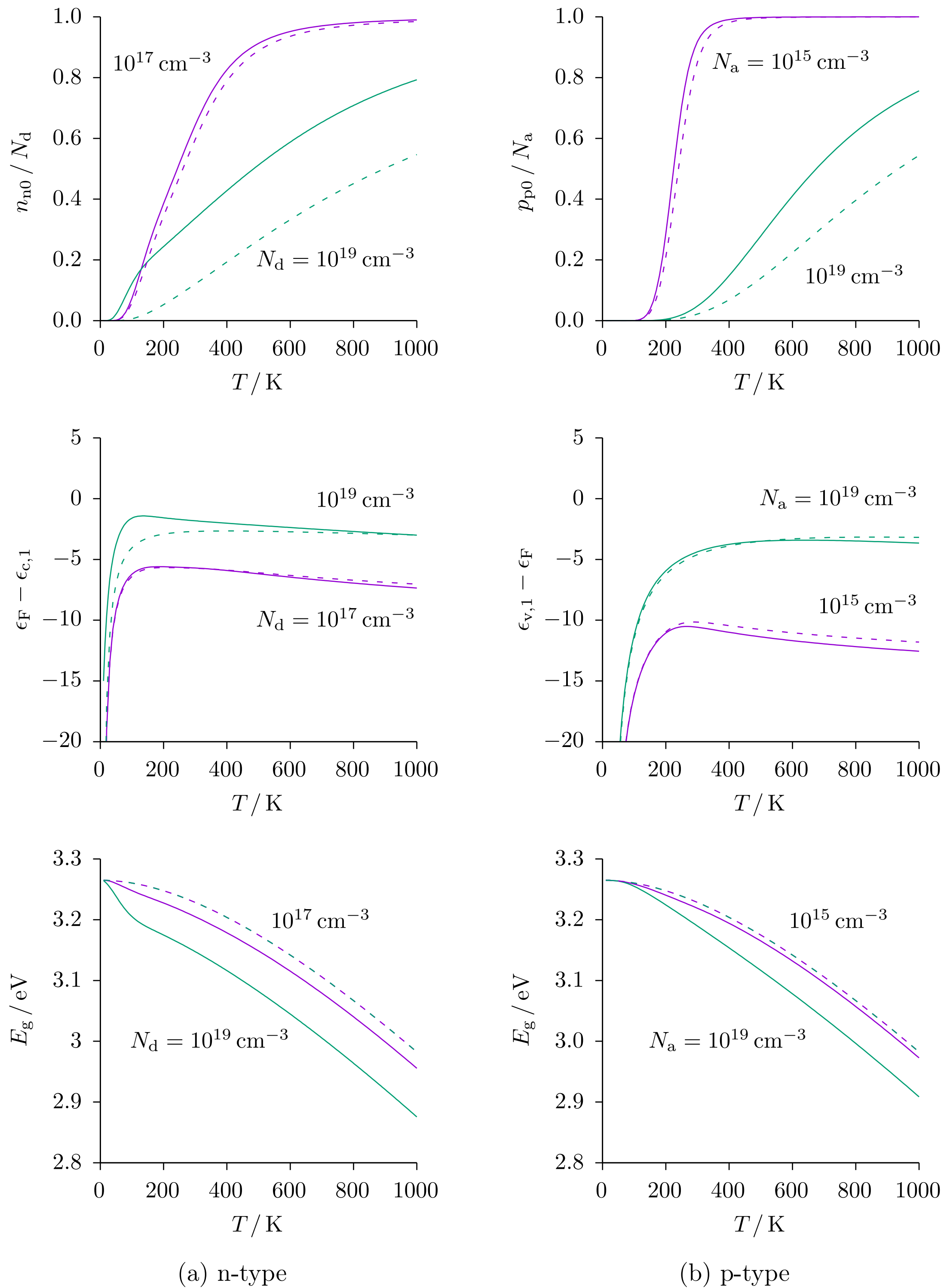
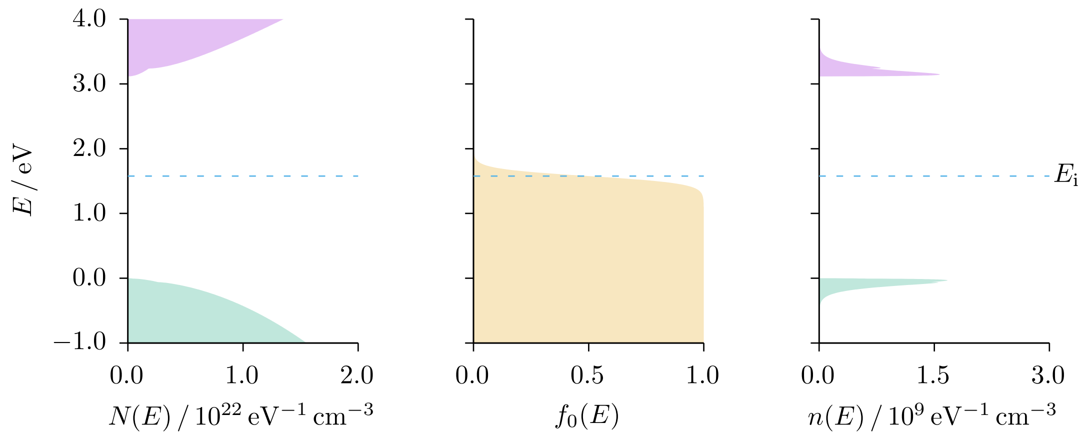
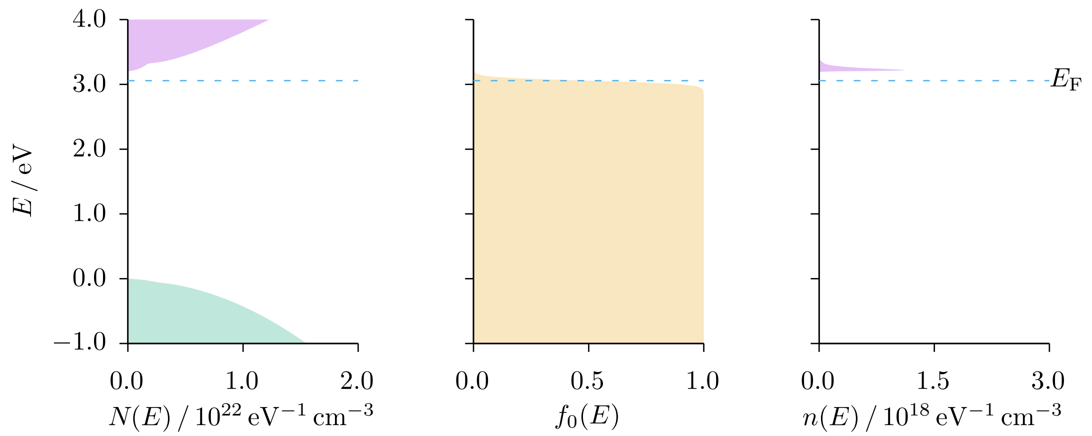


Figure 3.3

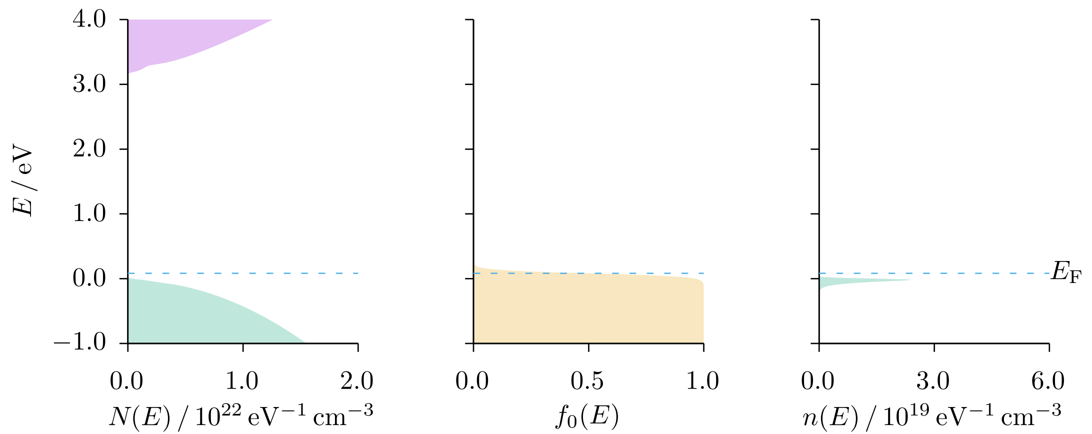
Calculated majority carrier concentrations, reduced Fermi level relative to the conduction band edge and fundamental band gap in nitrogen and aluminium doped 4H–SiC for relevant n-channel JFET doping concentrations assuming no compensation. Values are determined from numerical solutions to the charge neutrality equation. Solid lines represent full models while dashed lines assume single intrinsic bands with extrinsic effects omitted.



(a) $N_d = 0$, $N_a = 0$, $T = 673.15\,K$



(b) $N_d = 1 \times 10^{17}\,cm^{-3}$, $N_a = 0$, $T = 300\,K$



(c) $N_d = 0$, $N_a = 5 \times 10^{19}\,cm^{-3}$, $T = 300\,K$

Figure 3.4

Illustrative density of states and carrier energy distributions in the conduction and valence bands of (a) intrinsic, (b) n-type and (c) p^+-type 4H–SiC at various temperatures, T. The valence band minimum is selected as the reference energy. The Fermi level is indicated by blue dashed lines.

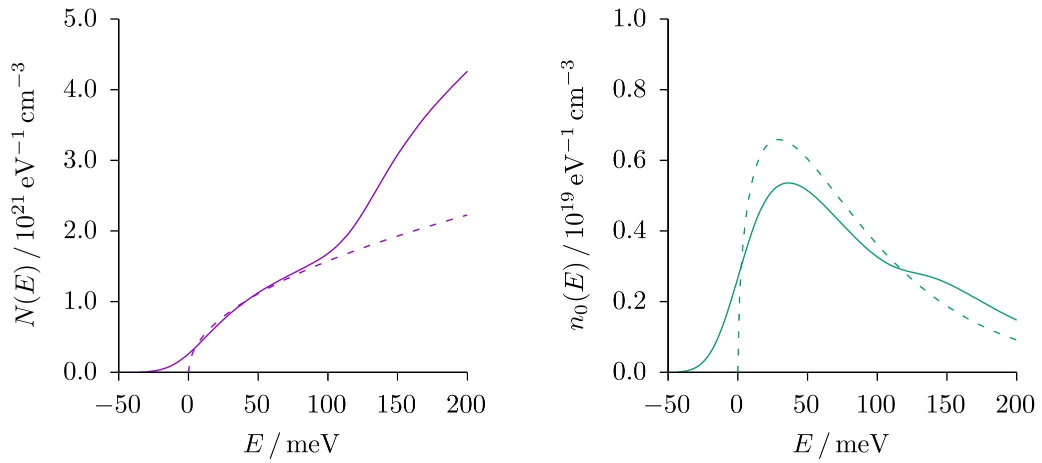
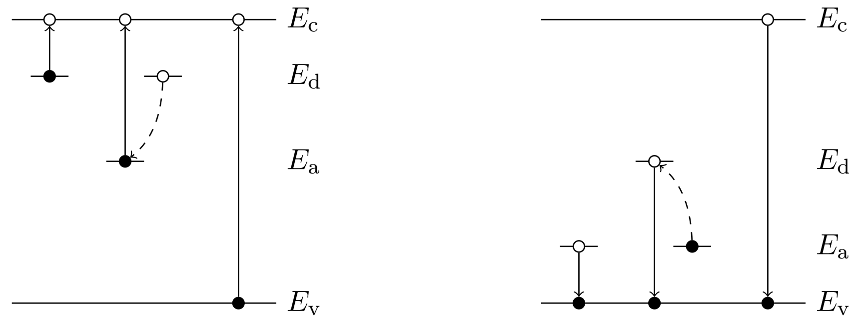


Figure 3.5

Equilibrium distribution of conduction band density of states and free electron concentrations determined for a singular intrinsic parabolic conduction and valence bands without impurity induced effects (dashed lines) and using the proposed model including non-parabolicity, multiple non-equivalent conduction and valence bands and impurity induced effects for a N donor concentration of $1 \times 10^{18}\,\mathrm{cm}^{-3}$ with compensation concentration $N_\mathrm{a} = 1 \times 10^{15}\,\mathrm{cm}^{-3}$ at $T = 673\,\mathrm{K}$. The intrinsic first conduction band minimum is taken as the reference energy.

compensation can actually increase the degree of ionisation in the usable temperature range. Compensation will also increase disorder and the fluctuations of the impurity potential, but given the level of doping control and the moderate doping concentrations required for JFETs the effect will be negligible.



(a) n-type: compensating acceptors

(b) p-type: compensating donors

Figure 3.6

Illustration of the effect of compensation in doped semiconductors. Electrons and holes are represented by filled and empty circles, respectively. Dashed arrows indicated a previous lowering in energy of a majority carrier to fill a compensating state. Solid lines represent subsequent possible majority carrier transitions into the conduction or valence band for n-type and p-type semiconductors, respectively.

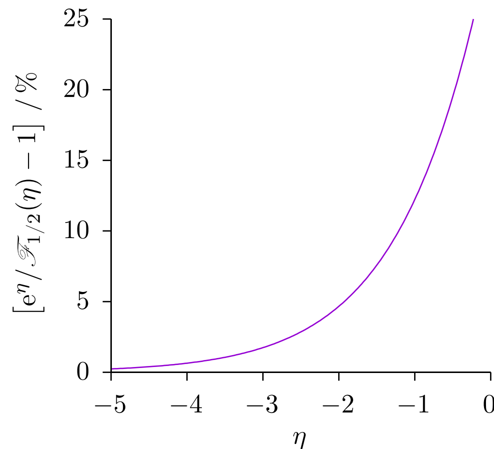


Figure 3.7
Percentage error introduced through use of the Boltzmann approximation to the Fermi integral of order one-half.

Given the values for the reduced Fermi level in Figure 3.3a and the relative plot for the Fermi integral in Figure 3.7* the worst case error introduced through use of the Boltzmann approximation for a typical n-type JFET channel and gate epilayer are approximately 0.1% and 2%, respectively.

3.8 SPICE Models

The degree of ionisation and the position of the Fermi level are extremely useful parameters for use in compact models. While feasible to incorporate, the iterative methods through which Simulation Program with Integrated Circuit Emphasis (SPICE) operates would become burdened by the models presented in the preceding sections. Using their results for guidance and validation, the proceeding section presents a set of efficient approximations for modelling the carrier concentrations in non-parabolic and highly doped bands. An appropriate procedure for using the highly efficient Newton-Raphson (NR) root finding algorithm to find E_{F} for both n- and p-type samples is also given.

3.8.1 Free Carrier Concentration

At high temperatures or doping concentrations the use of the parabolic single band approximation and Maxwell-Boltzmann statistics can become untenable. It has already been demonstrated how analytic approximations for the free carrier concentrations may be achieved where the DOS has been derived from $\boldsymbol{k}\cdot\boldsymbol{p}$ perturbation theory [113]. To calculate the electron concentration in each conduction band the modified Fermi transform of order one-half

$$F_{1/2}(\eta,\alpha) = \int_0^\infty \frac{\epsilon^{1/2}(1+\alpha\epsilon)^{1/2}}{1+\mathrm{e}^{\epsilon-\eta}}\mathrm{d}\epsilon \tag{3.46a}$$

*The Fermi integral pertains to parabolic bands.

must be solved. A typical n-channel JFET has a doping concentration of approximately $10^{17}\,\mathrm{cm}^{-3}$. Figure 3.3a suggests that for a N doping concentration of $10^{17}\,\mathrm{cm}^{-3}$ $\eta < -5$ at all temperatures, allowing the Fermi transform to be appropriately approximated by

$$\approx \mathscr{L}\{\epsilon^{1/2}(1+\alpha\epsilon)^{1/2}\}(1)\mathrm{e}^{\eta}, \tag{3.46b}$$

where

$$\mathscr{L}\{f(\epsilon)\}(s) = \int_0^\infty \mathrm{e}^{-s\epsilon} f(\epsilon)\,\mathrm{d}\epsilon \tag{3.46c}$$

is the Laplace transform of $f(\epsilon)$ at s. The integral can be solved piecemeal after expanding the term $(1+\alpha\epsilon)^{1/2}$ in a Binomial series, to give

$$F_{1/2} = \sum_{x=0}^{\infty} \binom{1/2}{x} \mathscr{L}\{\epsilon^{1/2+x}\}(1)\,\alpha^x \mathrm{e}^{\eta} \tag{3.46d}$$

$$= g_1 \mathrm{e}^{\eta}, \tag{3.46e}$$

where

$$\binom{n}{k} = \frac{n!}{k!\,(n-k)!} \tag{3.46f}$$

is the binomial coefficient. As the relationship between the Fermi integral and transform of order one-half is

$$\mathscr{F}_{1/2} = 2\pi^{-1/2} F_{1/2} \tag{3.47}$$

it is convenient to define

$$\mathscr{G}_1 = 2\pi^{-1/2} g_1 \tag{3.48}$$

whose value can be approximated by the truncated series

$$\mathscr{G}_1(\alpha) \approx \mathscr{G}_{1,0} + \mathscr{G}_{1,1}\alpha + \mathscr{G}_{1,2}\alpha^2 + \mathscr{G}_{1,3}\alpha^3 + \mathscr{G}_{1,4}\alpha^4. \tag{3.49}$$

whose scalar coefficients can be numerically calculated as 1.00*, 0.750, −0.469, 0.820 and −2.31, to 3 significant figures.

The DOS of overlapping bands should be summed together [97], as illustrated in Figures 2.6b and 3.5. Using the variables and syntax derived in §3.3, the total electron concentration in the two lowest conduction bands is given as

$$n_0 = N_{\mathrm{c},1}\mathscr{F}_{1/2}(\epsilon_\mathrm{F} - \epsilon_{\mathrm{c},1}, \alpha_1) + N_{\mathrm{c},2}\mathscr{F}_{1/2}(\epsilon_\mathrm{F} - \epsilon_{\mathrm{c},2}, \alpha_2) \tag{3.50a}$$

$$\approx N_{\mathrm{c},1}\mathscr{G}_1(\alpha_1)\mathrm{e}^{\epsilon_\mathrm{F}-\epsilon_{\mathrm{c},1}} + N_{\mathrm{c},2}\mathscr{G}_1(\alpha_2)\mathrm{e}^{\epsilon_\mathrm{F}-\epsilon_{\mathrm{c},2}} \tag{3.50b}$$

*This value is exact, and equates to the Boltzmann approximation for a parabolic band.

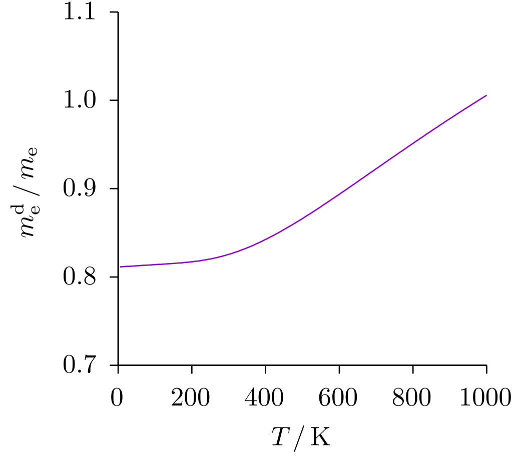


Figure 3.8

Calculated thermal conduction band density of states effective mass, m_e^d, including all six bands of interest, as a function of absolute thermodynamic temperature, T, as determined by Equation 3.51 using first-order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameters $0.77\,\mathrm{eV}^{-1}$ and $0.83\,\mathrm{eV}^{-1}$ for the first and second conduction bands, respectively.

$$= \left[N_{c,1}\mathscr{G}_1(\alpha_1) + N_{c,2}\mathscr{G}_1(\alpha_2)e^{\epsilon_{c,1}-\epsilon_{c,2}}\right]e^{\epsilon_F-\epsilon_{c,1}} \tag{3.50c}$$

$$= N_c e^{\epsilon_F-\epsilon_{c,1}}, \tag{3.50d}$$

where secondary subscript numbers 1 and 2 refer to the first and second conduction band, respectively. The latter form given by Equation 3.50d demonstrates that the two bands can be represented as a single effective band with combined conduction band effective DOS, N_c, with a thermal DOS effective mass [114] of

$$m_e^d(T) = \left\{\mathscr{G}_1(\alpha_1)[m_{e,1}^d(\epsilon_{c,1})]^{3/2} + \mathscr{G}_1(\alpha_2)[m_{e,2}^d(\epsilon_{c,2})]^{3/2}e^{\epsilon_{c,1}-\epsilon_{c,2}}\right\}^{2/3} \tag{3.51}$$

as plotted in Figure 3.8, assuming the same first-order $\boldsymbol{k}\cdot\boldsymbol{p}$ dispersion parameters $0.77\,\mathrm{eV}^{-1}$ and $0.83\,\mathrm{eV}^{-1}$, for the first and second bands, respectively. The closed-form expression is in close agreement with numerically determined values of $m_e^d(T)$ obtained from band structure calculations by Wellenhofer and Rössler [30].

Closed form analytic solutions can be attained for the n_0 and E_F in a compensated semiconductor that contains a single monovalent donor impurity. Unfortunately, for two inequivalent levels, as in the case of 4H–SiC, no real solutions exist. It has been suggested that the hexagonal and cubic donor levels can be approximated by an effective donor level [115]; unfortunately, a single static level provides a poor fit and its value and variation with temperature and compensation are difficult to account for.

Approximate solutions to E_F, and thus n_0, in n-type 4H–SiC can be determined from the simplified charge neutrality equation [12]

$$n_0 - N_{d,h}^+ - N_{d,k}^+ + N_a = 0, \quad \text{for } \{N_{d,h}^+, N_{d,k}^+\} \gg N_a, \tag{3.52}$$

where $N_{\mathrm{d,h}}^{+}$ and $N_{\mathrm{d,k}}^{+}$ represent the concentrations of ionised donors on hexagonal and cubic sites, respectively, and $N_{\mathrm{a}} \approx N_{\mathrm{a}}^{-}$ is the net concentration of compensating acceptors which can be safely be assumed to be completely ionised [37]. Equation 3.50 and its derivatives are well behaved and simple to calculate [116], making it ideal for use in efficient derivative based root finding methods such as the NR algorithm. An appropriate initial estimate comes from noting that at absolute zero n_0 is zero and E_{F} coincides with the highest donor level with remaining unionised donors [37]. Using this approach it is also possible to use intermediately determined values for n_0 and N_{d}^{+} to simultaneously update dependent parameters and thereby significantly reduce the total number of iterations required to achieve convergence.

A similar procedures can be followed for calculating the free hole concentration in the gate epilayer; although, additional high doping effects need to be included. In the case of valence band tailing, γ and ϵ are closely linked and a simple closed form analytic solution is not possible. The proposed solution, suitable for Verilog-A implemented SPICE models, employs the Joyce-Dixon approximation (JDA) [42, 116]

$$\mathscr{F}_{1/2}(x) \approx \mathscr{G}_1 \mathrm{e}^{x} - \mathscr{G}_2 \mathrm{e}^{2x}, \quad \text{for } x < -1 \tag{3.53a}$$

with a two-dimensional lookup table for the values of

$$\mathscr{G}_s(\gamma) = \frac{2}{\pi^{1/2}} \mathscr{L}\left\{ \int_{-\infty}^{\epsilon/\gamma} (\epsilon - \gamma\nu)^{1/2} \mathrm{e}^{-\nu^2} \mathrm{d}\nu \right\}(s), \quad s \in \{1, 2\} \tag{3.53b}$$

at different values of γ for each s. Including the three highest energy valence bands,

$$p_0 = \sum_{x=1}^{3} N_{\mathrm{v},x} \mathscr{F}_{1/2}(\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}}, \gamma) \tag{3.54a}$$

$$\approx \sum_{x=1}^{3} N_{\mathrm{v},x} \left[\mathscr{G}_1(\gamma) \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}}} - \mathscr{G}_2(\gamma) \mathrm{e}^{2(\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}})} \right] \tag{3.54b}$$

$$= \sum_{x=1}^{3} N_{\mathrm{v},x} \left[\mathscr{G}_1(\gamma) - \mathscr{G}_2(\gamma) \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}}} \right] \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}}} \tag{3.54c}$$

$$= N_{\mathrm{v}} \mathrm{e}^{\epsilon_{\mathrm{v},1} - \epsilon_{\mathrm{F}}}, \tag{3.54d}$$

where N_{v} represents the combined valence band effective DOS, with degenerate thermal DOS effective mass,

$$m_{\mathrm{h}}^{\mathrm{d}}(T) = \left\{ \sum_{x=1}^{3} \left[\mathscr{G}_1(\gamma) - \mathscr{G}_2(\gamma) \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{F}}} \right] (m_{\mathrm{h},x}^{\mathrm{d}})^{3/2} \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{v},1}} \right\}^{2/3}. \tag{3.55a}$$

In the non-degenerate limit, this may be simplified to give

$$m_{\mathrm{h}}^{\mathrm{d}}(T) = \left\{ \sum_{x=1}^{3} (m_{\mathrm{h},x}^{\mathrm{d}})^{3/2} \mathrm{e}^{\epsilon_{\mathrm{v},x} - \epsilon_{\mathrm{v},1}} \right\}^{2/3}. \tag{3.55b}$$

3.8.2 Intrinsic Carrier Concentration

The intrinsic carrier concentration, n_i, has a strong temperature dependence which can be most appropriately expressed as

$$n_\mathrm{i}(T) = n_\mathrm{i}(T_\mathrm{n})\frac{n_\mathrm{i}(T)}{n_\mathrm{i}(T_\mathrm{n})} \tag{3.56a}$$

$$= n_\mathrm{i}(T_\mathrm{n})\left[\frac{m_\mathrm{e}^\mathrm{d}(T)}{m_\mathrm{e}^\mathrm{d}(T_\mathrm{n})}\frac{m_\mathrm{h}^\mathrm{d}(T)}{m_\mathrm{h}^\mathrm{d}(T_\mathrm{n})}\right]^{3/4}\left(\frac{T}{T_\mathrm{n}}\right)^{3/2}\mathrm{e}^{\frac{1}{2k_\mathrm{B}}\left[\frac{E_\mathrm{g}(T_\mathrm{n})}{T_\mathrm{n}}-\frac{E_\mathrm{g}(T)}{T}\right]} \tag{3.56b}$$

$$= n_\mathrm{i}(T_\mathrm{n})\left[\frac{m^\mathrm{d}(T)}{m^\mathrm{d}(T_\mathrm{n})}\frac{T}{T_\mathrm{n}}\right]^{3/2}\mathrm{e}^{\frac{1}{2}\left[\frac{\phi_g(T_\mathrm{n})}{\phi_\mathrm{T}(T_\mathrm{n})}-\frac{\phi_g(T)}{\phi_\mathrm{T}(T)}\right]}, \tag{3.56c}$$

where $\phi_g = eE_\mathrm{g}$ is the band gap voltage and $m^\mathrm{d} = (m_\mathrm{e}^\mathrm{d}\, m_\mathrm{h}^\mathrm{d})^{1/2}$, with m_h^d by definition given by Equation 3.55b.

The mass action law is valid for non-degenerate semiconductors in thermal equilibrium [17]. For the gate epilayer used in the JFET structures in thus study, the acceptor concentration is large enough to be considered as degenerate. The identity

$$p_0\, n_0 = n_\mathrm{I}^2 \tag{3.57}$$

is however valid, where n_I is an apparent intrinsic carrier concentration and differs from n_i only in its use of Equation 3.55a in Equation 4.34 [9].

3.9 Conductivity

This section is concerned with investigating the temperature dependence of the bulk low-field* electron conductivity in 4H–SiC which is of interest in describing the operation of JFETs. A suitable model for the low-field electron mobility is developed in the framework of the relaxation time approximation of the Boltzmann equation and includes the influence of multiple non-parabolic and anisotropic conduction bands. Appropriate expressions for the scattering time and conductivity effective mass are identified. Thermal averages of the electron conductivity effective mass calculated for the two lowest non-equivalent conduction bands are lastly determined.

3.9.1 Scattering time

The electron current density in a semiconductor,

$$\boldsymbol{J} = -e\int_{\boldsymbol{k}} N\boldsymbol{v}f\,\mathrm{d}\boldsymbol{k}, \tag{3.58}$$

requires knowledge of the distribution of electrons and their velocities, $\boldsymbol{v}$ [117]. In the presence of a weak external electric field, $\mathscr{E}$, the Boltzmann equation in the framework of

*The low-field assumption is approximately valid for $\mathscr{E}$ less than $1\times10^3\,\mathrm{V\,cm^{-1}}$ [36].

the relaxation time approximation* provides a closed form expression for the distribution function, f, for electrons as

$$f = f_0 + e\tau_{\mathrm{m}}\mathscr{E}\cdot\boldsymbol{v}\frac{\partial f_0}{\partial E}, \tag{3.59}$$

where τ_{m} denotes the momentum relaxation time and is strongly dependent on the wave vector. Equation 3.59 suggests that the shape of the equilibrium distribution will be maintained, but will have its $\boldsymbol{k}$–space origin shifted in the direction of the electric field. The Pauli exclusion principle places limits on the motion of electrons in response to an applied electric field. The current density will be zero for f_0 as the carrier velocity, $\boldsymbol{v}$, is antisymmetric, $\boldsymbol{v}(\boldsymbol{k}) = -\boldsymbol{v}(-\boldsymbol{k})$, and f_0 is symmetric, $f_0(\boldsymbol{k}) = f_0(-\boldsymbol{k})$ [35]. It is therefore the case that only electrons in the region of energy where $-\partial f_0/\partial E$ is significant are available to take part in conduction. Substituting in the remaining anti-symmetric portion and changing to a sum over energy space provides

$$\boldsymbol{J} = -e^2\int_{E_{\mathrm{c}}}^{\infty}\tau_{\mathrm{m}}N\boldsymbol{v}(\mathscr{E}\cdot\boldsymbol{v})\frac{\partial f_0}{\partial E}\mathrm{d}E. \tag{3.60}$$

A wave vector denotes the state in which an electron wave packet, representing a localised electron, would be most concentrated. Wave theory defines the group velocity of a wave packet, representing the expectation value for the velocity of an electron centred at a given point in $\boldsymbol{k}$–space, as being proportional to the gradient of the dispersion and directed normal to the constant energy surface at that point. From Equation 3.2 the $\boldsymbol{k}$–space group velocity,

$$\boldsymbol{v}(\boldsymbol{k}) = \hbar^{-1}\nabla_{\boldsymbol{k}}E(\boldsymbol{k}) \tag{3.61a}$$

$$= \frac{\hbar k_x}{m_x^*}\hat{\boldsymbol{x}} + \frac{\hbar k_y}{m_y^*}\hat{\boldsymbol{y}} + \frac{\hbar k_z}{m_z^*[1+2\alpha E(k_z)]}\hat{\boldsymbol{z}}, \tag{3.61b}$$

is found to be direction and energy dependent. The $\boldsymbol{\kappa}$–space velocity,

$$\boldsymbol{v}(\boldsymbol{\kappa}) = \hbar^{-1}\nabla_{\boldsymbol{\kappa}}E(\boldsymbol{\kappa}) = \frac{\hbar\boldsymbol{\kappa}}{m^*} \tag{3.62}$$

attained through the change of variables in Equation 3.3, is however a scalar. For weak electric fields the drift velocity is much smaller than the thermal velocity and can be ignored in the following analysis. Given the electron kinetic energy,

$$E = \tfrac{1}{2}m^*v^2, \tag{3.63}$$

of an electron and observing the $\boldsymbol{\kappa}$–space symmetry, it is found that

$$v_iv_j = \frac{v^2}{3} = \frac{2E}{3m^*}, \quad (i,j)\in\{x,y,z\}, \tag{3.64}$$

*The relaxation time approximation is valid for low-field strengths and when the scattering mechanisms are elastic, isotropic, or both [35].

allowing Equation 3.60 to be written as

$$\boldsymbol{J} = -\frac{2e^2\mathscr{E}}{3m^*}\int_{E_\mathrm{c}}^{\infty} EN(E)\frac{\partial f_0}{\partial E}\tau_\mathrm{m}\mathrm{d}E \tag{3.65}$$

In the case of non-degenerate semiconductors the centre of $\partial f/\partial E$ will be far below the bottom of the conduction band and only the upper tail of the distribution will overlap it [29]. In such cases Equation 3.65 can therefore be simplified to

$$\boldsymbol{J} \approx \frac{2e^2\mathscr{E}}{3k_\mathrm{B}Tm^*}\int_{E_\mathrm{c}}^{\infty} EN\mathrm{e}^{-\frac{E}{k_\mathrm{B}T}}\tau_\mathrm{m}\mathrm{d}E \tag{3.66}$$

Written in a form analogous to the classical conductivity model

$$\boldsymbol{J} = \frac{ne^2\overline{\tau_\mathrm{m}}}{m^*}\mathscr{E}, \tag{3.67}$$

it is seen that an appropriate average scattering time, $\overline{\tau_\mathrm{m}}$, is required. The low-field condition allows the equilibrium DOS to be used [118] which after substituting for $N(E)$ provides

$$\overline{\tau_\mathrm{m}} = \frac{2}{3k_\mathrm{B}T}\frac{\int_{E_\mathrm{c}}^{\infty} E(E+AE^2)^{1/2}\,\mathrm{e}^{-E/k_\mathrm{B}T}\tau_\mathrm{m}\,\mathrm{d}E}{\int_{E_\mathrm{c}}^{\infty}(E+AE^2)^{1/2}\,\mathrm{e}^{-E/k_\mathrm{B}T}\,\mathrm{d}E} \tag{3.68a}$$

$$= \frac{2\langle E\tau_\mathrm{m}\rangle}{3k_\mathrm{B}T}, \tag{3.68b}$$

where $\langle E\tau_\mathrm{m}\rangle$ is the expectation value of $E\tau_\mathrm{m}$ normalised by the probability density function, $(E+AE^2)^{1/2}\,\mathrm{e}^{-E/k_\mathrm{B}T}$. Equation 3.68 differs from the case of a standard band in the inclusion of a $(1+AE)^{1/2}$ term in both of the integrals.

It is expediently assumed that τ_m depends only on the magnitude of the electron velocity so that $\overline{\tau_\mathrm{m}}$ can be used for all directions. More generally τ_m will be tensorial and one should use the quotient with the corresponding effective mass component [36]. The error introduced will however be small in the temperature range of interest where the dominant scattering mechanisms are isotropic.

3.9.2 Conductivity Effective Mass

When dealing with carrier transport it is important to remember that the effective mass is a function of energy, such that carriers appreciably above their respective band extremum, referred to as hot electrons, will have different transport properties to those located at the extremum [35]. The equations of motion for an electron due to the force of an electric field in a semiconductor without spherical symmetry requires an appropriate effective mass in the direction of electron motion to be used [36].

The components of $\boldsymbol{J}$ in terms of the real coordinates for a given ellipsoid are given by

$$J_i = \sum_j \sigma_{ij}\mathscr{E}_j = \sum_j \frac{ne^2\overline{\tau_\mathrm{m}}}{\langle m_{ij}^*\rangle}\mathscr{E}_j, \quad (i,j)\in\{x,y,z\}, \tag{3.69}$$

where σ_{ij} and m^*_{ij} are the conductivity and effective mass tensors, respectively; J_i and $\mathscr{E}_j$ are the current density and electric field vector components in the i and j directions, respectively; n is the total concentration of electrons in the given conduction band; and $\overline{\tau_{\mathrm{m}}}$ is given by Equation 3.68 [36]. In an anisotropic conductor, $\boldsymbol{J}$ and $\mathscr{E}$ will not be parallel except along axes of symmetry which for ellipsoidal constant energy surfaces are the directions of the principle axes of the tensor; i.e., for $i = j$ [36].

The conductivity effective mass, also referred to as the inertial effective mass, accounts for the quantum mechanical aspects of electron motion inside the classical equation [9]. Analogising the time rate of change of a wave packet's group velocity with the acceleration of a classical particle allows the notion of an effective mass to develop, which in general will be tensorial [36]

$$m^*_{ij} = \hbar^2 \left[\frac{\partial^2 E(\boldsymbol{k})}{\partial k_i \partial k_j} \right]^{-1}, \quad (i,j) \in \{x, y, z\}. \tag{3.70}$$

Both m^*_{xx} and m^*_{yy}, as so far implied, can be satisfactorily be treated as being scalar values that are independent of E. Conversely, the thermal average of the conductivity effective mass in the direction of the principle axis,

$$\langle m^*_{zz} \rangle = \frac{\sum_{\boldsymbol{k}} f(\boldsymbol{k})}{\sum_{\boldsymbol{k}} f(\boldsymbol{k}) / m^*_{zz}(\boldsymbol{k})}. \tag{3.71a}$$

should be used in Equation 3.69* [119]. Equation 3.71a may be readily solved in E–space using the techniques previously discussed; restricting the discussion to non-degenerate semiconductors under low electric fields and setting the reference energy to the the conduction band minimum allows the expectation value of to be determined from

$$\langle m^*_{zz} \rangle = \frac{\int_{E_{\mathrm{c}}}^{\infty} (E + AE^2)^{1/2} \mathrm{e}^{-E/k_{\mathrm{B}}T} \mathrm{d}E}{\int_{E_{\mathrm{c}}}^{\infty} (E + AE^2)^{1/2} \mathrm{e}^{-E/k_{\mathrm{B}}T} / m^*_{zz}(E) \mathrm{d}E}, \tag{3.71b}$$

where from Equation 3.70,

$$m^*_{zz}(E) = m^*_{zz}(0)[1 + 4A(E + AE^2)]^{3/2}. \tag{3.71c}$$

In terms of the normalised variables previously stated this becomes,

$$\langle m^*_{zz} \rangle = \frac{\int_0^{\infty} (\epsilon + \alpha\epsilon^2)^{1/2} \mathrm{e}^{-\epsilon} \mathrm{d}\epsilon}{\int_0^{\infty} (\epsilon + \alpha\epsilon^2)^{1/2} \mathrm{e}^{-\epsilon} / m^*_{zz}(\epsilon) \mathrm{d}\epsilon}, \tag{3.71d}$$

wherein

$$m^*_{zz}(\epsilon) = m^*_{zz}(0)[1 + 4\alpha(\epsilon + \alpha\epsilon^2)]^{3/2}. \tag{3.71e}$$

The total contribution is the sum for the individual ellipsoids. Close to equilibrium it can

*The effective mass will also reduce very slightly as temperature is increased on account of interactions with lattice vibrations; however, this will not greatly influence results [55].

be noted that the carriers will be evenly distributed between all of the equivalent ellipsoids [35]. In 4H-SiC, the constant-energy ellipsoids lie along the six symmetrically equivalent $\langle 10\bar{1}0\rangle$ directions. As the band minima for both the first and second conduction band occur at the M–points in the Brillouin zone, the problem may be mathematically considered in each case as three equivalent ellipsoids along the three unique sets of axes* [57, 120].

The effective mass tensor can be written in principle axis form as

$$\langle m^*_{ij}\rangle = \begin{bmatrix} m^*_{xx} & 0 & 0 \\ 0 & m^*_{yy} & 0 \\ 0 & 0 & \langle m^*_{zz}\rangle \end{bmatrix}. \tag{3.72}$$

The tensors of each equivalent conduction band minima must, however, be related to a unique set of orthogonal axes which can be achieved through use of the second rank tensor transformation law [121],

$$m^{*\prime}_{ij} = l_{ip}\, l_{jq}\, m_{pq}, \tag{3.73}$$

where l_{ip} and l_{jq} denote direction cosines. The directions in the new coordinate system are given in terms of direction cosines from the original coordinate system axes contained in a set transformation matrix† [36]. The transformation matrix for counter clockwise rotation about the principle axis is given by [35],

$$l_{ip} = \begin{bmatrix} l_{xx} & l_{xy} & l_{zz} \\ l_{yx} & l_{yy} & l_{yz} \\ l_{zx} & l_{zy} & l_{zz} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3.74a}$$

For rotation $\theta = 60^\circ$ and 120° relative to a reference direction about the basal plane the transformation matrixes become

$$l_{ip} = \begin{bmatrix} \frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad \text{for } \theta = 60^\circ \tag{3.74b}$$

and

$$l_{ip} = \begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad \text{for } \theta = 120^\circ, \tag{3.74c}$$

respectively. Thus, for rotation of the co-ordinate system about the principle axis, the following transformations are performed,

*Two opposite facing half ellipsoids constitutes one full ellipsoid [37].

†A transformation matrix relates two sets of axes.

$$m^{*}_{xx}{}' = l^2_{xx} m^{*}_{xx} + l^2_{xy} m^{*}_{yy} \tag{3.75a}$$

$$m^{*}_{xy}{}' = m^{*}_{yx}{}' = l_{xx} l_{yx} m^{*}_{xx} + l_{xy} l_{yy} m^{*}_{yy} \tag{3.75b}$$

$$m^{*}_{yy}{}' = l^2_{yx} m^{*}_{xx} + l^2_{yy} m^{*}_{yy} \tag{3.75c}$$

$$m^{*}_{xz}{}' = m^{*}_{zx}{}' = m^{*}_{yz}{}' = m^{*}_{zy}{}' = 0 \tag{3.75d}$$

$$m^{*}_{zz}{}' = m^{*}_{zz}. \tag{3.75e}$$

Choosing the reference axis to line up with the principle axis of one of the ellipsoids and transforming the remaining two to the same set provides the direction averaged conductivity effective mass in either of the two lowest conduction band as [36]

$$m^{\mathrm{c}}_{\mathrm{e}} = \frac{1}{3}\begin{bmatrix} m^{*}_{xx} & 0 & 0 \\ 0 & m^{*}_{yy} & 0 \\ 0 & 0 & \langle m^{*}_{zz}\rangle \end{bmatrix} \cdots$$

$$+ \frac{1}{3}\begin{bmatrix} (m^{*}_{xx} + 3m^{*}_{yy})/4 & (\sqrt{3}m^{*}_{xx} - \sqrt{3}m^{*}_{yy})/4 & 0 \\ (\sqrt{3}m^{*}_{xx} - \sqrt{3}m^{*}_{yy})/4 & (3m^{*}_{xx} + m^{*}_{yy})/4 & 0 \\ 0 & 0 & \langle m^{*}_{zz}\rangle \end{bmatrix} \cdots$$

$$+ \frac{1}{3}\begin{bmatrix} (m^{*}_{xx} + 3m^{*}_{yy})/4 & (\sqrt{3}m^{*}_{yy} - \sqrt{3}m^{*}_{xx})/4 & 0 \\ (\sqrt{3}m^{*}_{yy} - \sqrt{3}m^{*}_{xx})/4 & (3m^{*}_{xx} + m^{*}_{yy})/4 & 0 \\ 0 & 0 & \langle m^{*}_{zz}\rangle \end{bmatrix} \tag{3.76a}$$

$$= \begin{bmatrix} (m^{*}_{xx} + m^{*}_{yy})/2 & 0 & 0 \\ 0 & (m^{*}_{xx} + m^{*}_{yy})/2 & 0 \\ 0 & 0 & \langle m^{*}_{zz}\rangle \end{bmatrix} \tag{3.76b}$$

$$= \begin{bmatrix} m^{\mathrm{c}}_{\mathrm{e,a}} & 0 & 0 \\ 0 & m^{\mathrm{c}}_{\mathrm{e,a}} & 0 \\ 0 & 0 & m^{\mathrm{c}}_{\mathrm{e,c}} \end{bmatrix} \tag{3.76c}$$

Thus, while transport within each ellipsoid is anisotropic, if the electric field in any direction of the basal plane is sufficiently low such that each equivalent valley is equally populated the resulting value averages out to the same value each time [35].

The conductivity in the direction of current flow can be alternatively expressed as

$$\sigma = \frac{\boldsymbol{J}^2}{\boldsymbol{J} \cdot \boldsymbol{\mathscr{E}}}. \tag{3.77}$$

In the case of crystals with hexagonal symmetry previously identified we have a single axis of symmetry along the [0001] direction. The perpendicular and parallel components of $\boldsymbol{J}$

can be expressed as

$$J_{\perp} = \sigma_{\perp}\mathscr{E}_{\perp} = J\sin\theta \tag{3.78a}$$

and

$$J_{\parallel} = \sigma_{\parallel}\mathscr{E}_{\parallel} = J\cos\theta, \tag{3.78b}$$

respectively [97]. Substituting these expressions into Equation 3.77, it is subsequently found that

$$\boldsymbol{J}\cdot\mathscr{E} = \frac{J_{\parallel}^2}{\sigma_{\parallel}} + \frac{J_{\perp}^2}{\sigma_{\perp}} = J^2\left(\frac{\cos^2\theta}{\sigma_{\parallel}} + \frac{\sin^2\theta}{\sigma_{\perp}}\right). \tag{3.79}$$

As each basal plane direction is equivalent the change in effective mass in any direction can be represented in terms of an arbitrary angle subtended from the principle axis [36]

$$m_{\mathrm{e}}^{\mathrm{c}} = m_{\mathrm{e,a}}^{\mathrm{c}}\sin^2\theta + m_{\mathrm{e,c}}^{\mathrm{c}}\cos^2\theta. \tag{3.80}$$

The resulting range for the conductivity effective mass of an electron at the bottom of the first and second conduction band will vary with direction between $0.33\,m_{\mathrm{e}} \leq m_{\mathrm{e,1}}^{\mathrm{c}} \leq 0.45\,m_{\mathrm{e}}$ and $0.45\,m_{\mathrm{e}} \leq m_{\mathrm{e,2}}^{\mathrm{c}} \leq 0.80\,m_{\mathrm{e}}$, respectively, as illustrated in Figure 3.9a. SiC is typically grown between 4° and 8° off axis, although Equation 3.80 and Figure 3.9a suggest little difference is expected from the on-axis coordinate systems. Additionally, the orientation of

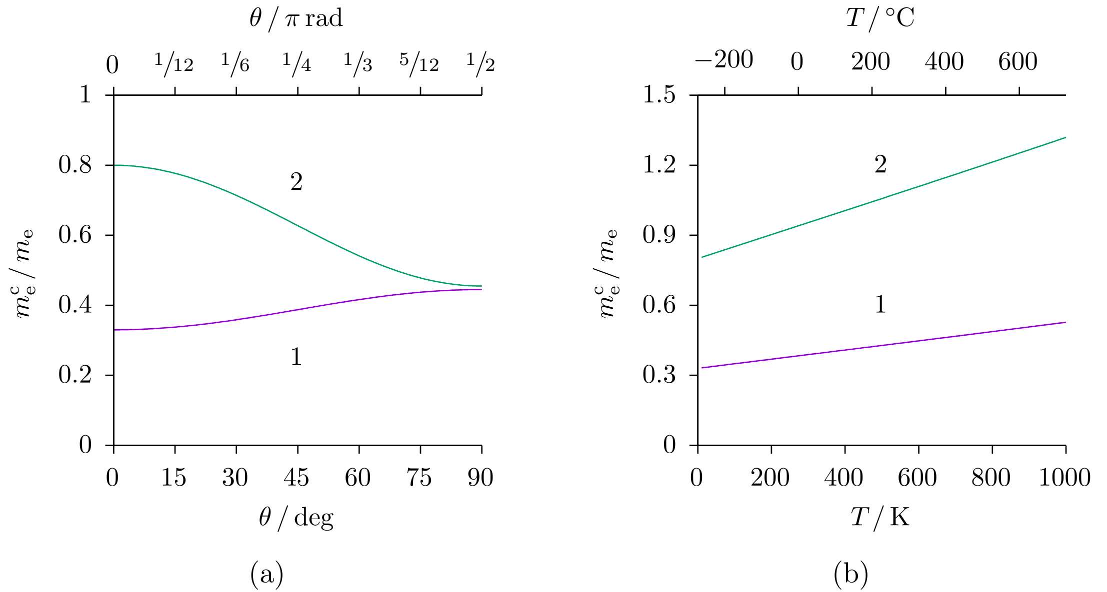


Figure 3.9

Electron conductivity effective mass in bulk 4H–SiC in the first and second conduction bands, denoted by 1 and 2, respectively, for (a) variation with angle, θ, subtended from the principle axis at their respective minimum and (b) variation with temperature, T, for motion along the principle axis.

a device on the wafer for an ideal crystal bears no effect on the conductivity.

Equation 3.76c shows that the effective mass perpendicular to the basal plane is equal to the thermal average of the principle axis effective mass tensor components for a single band along the principle axis as described by Equation 3.71; numerically determined value for the first and second conduction band are given in Figure 3.9b as a function of temperature. The increase is fairly linear, changing by approximately 19% and 21% between 25 °C and 400 °C in the first and second conduction bands, respectively. Consequently the calculated room temperature values are noticeable larger than the values determined at the band minima.

The appropriate average for use in other contexts may differ. For example, the appropriate value for use in the Richardson constant [122] can be a much larger value as the lower mass carriers with energy less than the barrier height will not contribute to the average.

A two band conductivity model is subsequently given as [97].

$$\sigma = e^2 \left(\frac{n_1 \overline{\tau_{\mathrm{m},1}}}{m^{\mathrm{c}}_{\mathrm{e},1}} + \frac{n_2 \overline{\tau_{\mathrm{m},2}}}{m^{\mathrm{c}}_{\mathrm{e},2}} \right), \tag{3.81}$$

with each non-equivalent band having a corresponding values for n, $\overline{\tau_{\mathrm{m}}}$ and $m^{\mathrm{c}}_{\mathrm{e}}$. The equilibrium distribution of electrons between the different conduction bands will be determined by the ratio of the DOS of each band at a given energy [18]. Appropriate weighted averages are required for both effective mass and relaxation time in both of the conduction bands [31]. It should be apparent that without precise knowledge for $\overline{\tau_{\mathrm{m}}}$ in each band an average thermal conductivity effective mass cannot be defined [123]. Methods for achieving this are well known and therefore are not covered here. Expressions for each τ_{m} component derived under the assumption of single parabolic bands remain valid provided Equation 3.51 is used in place of $m^{\mathrm{d}}_{\mathrm{e}}$.

3.10 Summary

An analytic expression for the DOS suitable for the two lowest non-equivalent conduction bands in 4H–SiC has been developed based on a $\boldsymbol{k}\cdot\boldsymbol{p}$ approximation of the dispersion near their respective minimum. Appropriate expressions for the thermal equilibrium electron and hole concentrations in extrinsic samples have been subsequently found which include the influence of the random spacial variation of impurities. Computationally efficient models to represent the DOS of donors and acceptors impurities were also discussed.

Numeric solutions for the Fermi level in n- and p-type 4H–SiC that satisfy the charge neutrally equation were subsequently calculated. The combined influence of multiple non-parabolic conduction bands, multiple valence bands and impurity induced variation in the DOS for intrinsic and impurity bands were shown to have a marked effect on the determined free carrier concentrations, Fermi level and band gap energy, especially for degenerately doped samples. The worst case error introduced through use of the Boltzmann approximation for $10^{17}\,\mathrm{cm}^{-3}$ N and $10^{19}\,\mathrm{cm}^{-3}$ Al doped samples were found to be approximately 0.1 % and 2 %, respectively. The self-consistent calculations also identified a reduction of the intrinsic band gap at 400 °C in each case of 27 meV and 79 meV, respectively.

Based on the solutions to the aforementioned models a set of efficient well behaved closed form expressions were developed for the free carrier concentrations in the framework of the JDA which are ideally suited for use in circuit simulations. Convenient expressions for the thermal density of states effective masses were simultaneously developed that can be utilised in expressions derived for singular parabolic bands. The conditions by which solutions to the charge neutrality equation can be achieved using the efficient NR algorithm were also identified.

The effect of multiple non-parabolic conduction bands on the low-field electron conductivity in 4H–SiC was lastly discussed. Appropriate weighting functions for the momentum relaxation time and conductivity effective mass were identified. The effective mass in each band for all directions on the basal plane was found to be the arithmetic mean of the principle axis effective mass tensor components parallel to the plane. Under the assumption of parabolic dispersion these values will be almost independent of temperature. The similarity of the conductivity effective mass along the basal plane in each conduction band also indicates that the distribution of carriers in each band will have little effect on the low-field electron mobility. The effective mass perpendicular to the basal plane was found to be simply equal to the principle axis effective mass tensor components for a single band in that direction. The non-parabolic dispersion in this direction was found to introduce a temperature dependence to the effective mass, causing the expectation value to increase by 19% and 21% between 25 °C and 400 °C in the first and second conduction bands, respectively. The derived expressions in context with a two band conductivity model provide much needed insight it the temperature dependence of the transport properties of 4H–SiC.

CHAPTER

4 Devices

4.1 Introduction

The modern electronics industry provides a rich catalogue of solid-state devices to suit a wide range of applications, wherein topologies and materials are selected based on their combined merits and manufacturability. Harsh environment sensors utilising SiC continue to receive much attention, creating a demand for accompanying signal conditioning electronics. High quality and process tolerant SiC junction field effect transistors (JFETs) are relatively simple to fabricate using conventional equipment and techniques, and circumvent many of the pitfalls experienced by other SiC transistor variants. Their suitability for long term operation under such conditions have been demonstrated by a number of groups [4, 8, 96].

Computer simulations are of great utility in the development of electronic systems, providing an efficient and relatively inexpensive method of validating and optimising devices and circuits. Circuit simulators make use of high level device models, commonly referred to as compact models, that employ a combination of physical and empirical expressions to achieve fast convergence, even for complex circuits with numerous devices. The validity of these simulations, however, depend on how accurately the models are able to reflect real device behaviour. Material specific models are often also demanded to account for changes in stimuli, such as temperature and electric field. Historically the JFET has been overshadowed by other field effect transistor (FET) structures and the need for integrated circuit (IC) compatible compact models has not previously arisen, presenting a stumbling block for many contemporary SiC IC designers.

This chapter continues by first outlining the process steps followed to produce the n-channel lateral depletion-mode (NLDM) JFETs and related devices developed for this project. Contact performance and influence on device operation is then briefly discussed. Two novel IC compatible compact models, developed in the framework of the gradual channel approximation (GCA), that include the influence of the body-effect and electric field dependent mobility are then presented; the first is proposed for users requiring closed form solutions while the second employs an efficient numerical method to calculate the extrapolation pinch-off point (expop) but more accurately describes channel modulation. Validation and optimisation of model parameters against experimental data is then presented. Appropriate SiC thermal models are lasted covered and successfully incorporated.

4.2 Fabrication

The second generation of Newcastle University (NU) SiC JFETs used in this study were designed and fabricated by Dr. Konstantin Vasilevskiy and are based on the first generation devices developed by Dr. Rupert Stevens [124]. A concise account of the process flow followed to create the 4H–SiC JFETs and other related devices is given in Table 4.1, with accompanying JFET cross sectional schematics in Figure 4.1*†. The mask references listed in the third column of Table 4.1 relate to the layout images provided in §A.

The starting sample at step 1 was taken from a commercial 4H–SiC n-type wafer with three layers of epitaxy, obtained from Cree, Inc. A *body* epilayer with nominal p-type doping concentration and thickness of $2 \times 10^{15}\,\mathrm{cm}^{-3}$ and 7 µm, respectively, acts as a buffer layer and provides isolation from the n-type substrate. A n-type epilayer with nominal doping concentration and thickness of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ and 300 nm, respectively, acts as the device *channel*. Lastly, a p-type *gate* epilayer with nominal doping concentration and thickness of $2 \times 10^{19}\,\mathrm{cm}^{-3}$ and 200 nm, respectively, is included as the primary means of modulating the active device channel. Importantly, Cree specify tolerances of ±10% for epilayer thickness and ±25% and ±50% for n- and p-type dopant concentrations, respectively [125].

The initial reactive ion etching (RIE) in step 5 was performed in stages, in-between which electrical measurements were taken to test for isolation between the gate and channel epilayers. Using this method the gate epilayer thickness was determined to be 177.5 nm. Approximately 50 nm of the channel region was additionally removed to insure adequate electrical isolation at the expense of increasing the series resistance at the source and drain ends of the channel.

The N implant in step 7 was intended to provide a box profile extending approximately 200 nm into the n-type epilayer with a peak concentration of $2 \times 10^{19}\,\mathrm{cm}^{-3}$. The implant energies and fluxes used are listed in Table 4.2. The results of SIMS measurements shown in Figure 4.2 provide confirmation and agree with the SRIM simulations presented alongside. While the sensitivity of SIMS is capable of detecting densities as low as $10^{14}\,\mathrm{cm}^{-3}$, the dynamic range is very poor and discrepancies occur when transitioning from high to lower doped regions‡ and are due to a cascading of impurities from the crater wall of the preceding highly doped region [126]. It should also be noted that SIMS provides the total rather than activated concentration. The 1700 °C rapid thermal anneal (RTA) in step 10 was performed to activate the implant and repair related damage. Post-anneal room temperature Hall-effect measurements provided a free electron concentration and Hall mobility of $4.01 \times 10^{18}\,\mathrm{cm}^{-3}$ and $103.5\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, respectively; using the model presented in §3.7, and noting that the solubility of N at 1700 °C is expected to be notably less than $2 \times 10^{19}\,\mathrm{cm}^{-3}$ [127], the activated donor concentration can be approximately determined to be $1.2 \times 10^{19}\,\mathrm{cm}^{-3}$.

During thermal oxidation a fresh oxide-semiconductor interface is created which transitions into the semiconductor [17]. The oxidation performed in step 17 removed approximately 22.7 nm from the surface of the n- and p-type epilayers and is the sum of two successive oxida-

*Images not drawn to scale.
†Colours used reflect observation [20].
‡The so called SIMS tail.

Table 4.1
A simplified version of the process flow, developed by Dr. Konstantin Vasilevskiy of Newcastle University, used to fabricate the 4H–SiC JFETs and related devices used in this study.

No.	Description	Notes
1	Clean	
2	Photolithography	Mask: GATE (see §A)
3	Deposit Ti/Ni	5/80 nm
4	Lift off	
5	RIE	
6	Photolithography	Mask: NIMPL (see §A)
7	N implantation	200 nm at 2×10^{19} cm^{-3}
8	Clean	
9	Etch Ni/Ti	
10	Deposit protective layer and anneal	1700 °C RTA
11	Clean	
12	Photolithography	Mask: MESA (see §A)
13	Deposit Ti/Al	5/230 nm
14	Lift off	
15	RIE	
16	Etch Al/Ti	
17	Oxidation	47 nm SiO_2 (−22.7 nm SiC)
18	Photolithography	Mask: NCONT (see §A)
19	Etch SiO_2	
20	Deposit Ti/Ni	5/70 nm
21	Lift off and anneal	1040 °C, 210 s
22	Photolithography	Mask: PCONT (see §A)
23	Etch SiO_2	
24	Deposit Ti/Al/Ti/Al/Ti/Ni	3/15/6/30/25/30 nm
25	Lift off and anneal	1000 °C, 20 s
26	Photolithography	Mask: TOPUP (see §A)
27	Deposit Cr/W/Pt/Au	10/11/20/220 nm
28	Lift off	
29	Deposit Si_3N_4	1030 nm
30	Photolithography	Mask: PROTE (see §A)
31	Deposit Al	40 nm
32	Lift off	
33	RIE	
34	Etch Al	

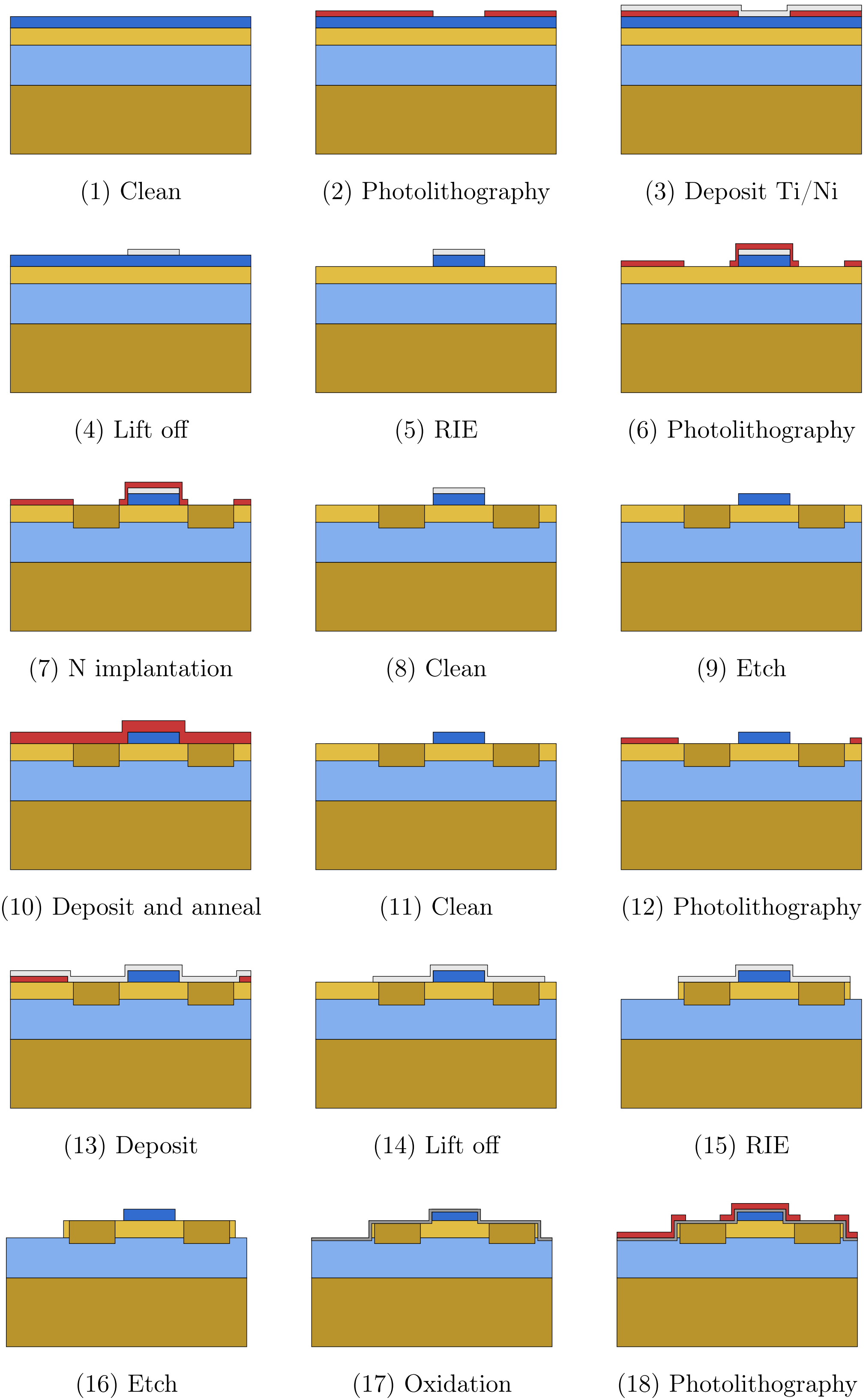


Figure 4.1
Cross section view during a JFET process flow.

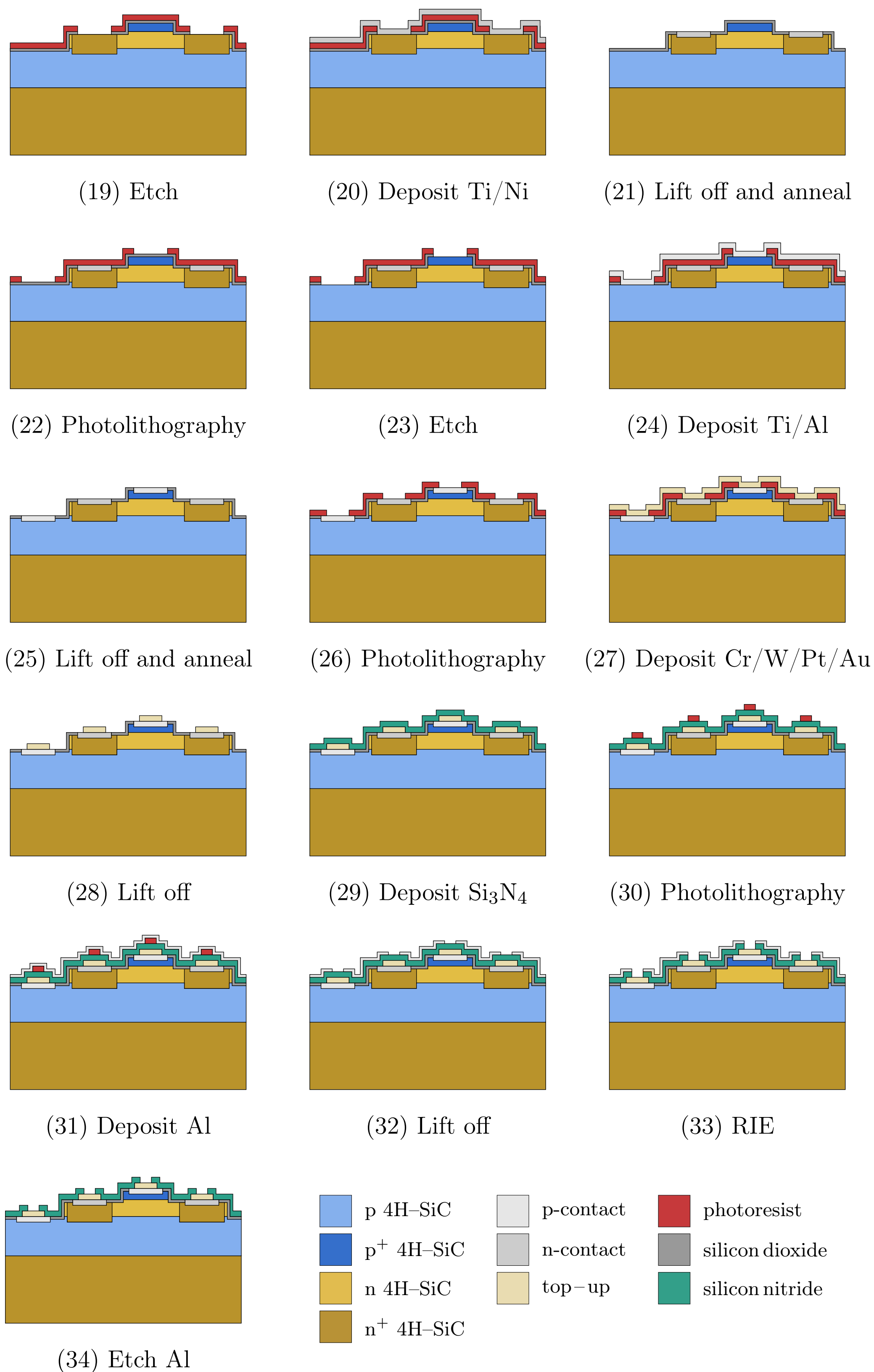


Figure 4.1
Cross section view during a JFET process flow. (cont.)

Table 4.2
N implant energies and fluxes used to form a $2 \times 10^{19}\,\mathrm{cm}^{-3}$ box profile to facilitate low resistance n-type contacts.

Energy / keV	Flux / cm^{-2}
110	1.5×10^{14}
60	6.0×10^{13}
80	5.5×10^{13}
40	5.5×10^{13}
20	5.0×10^{13}

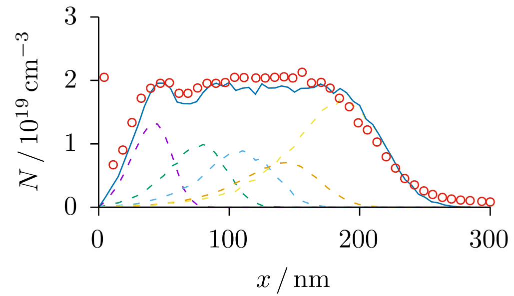
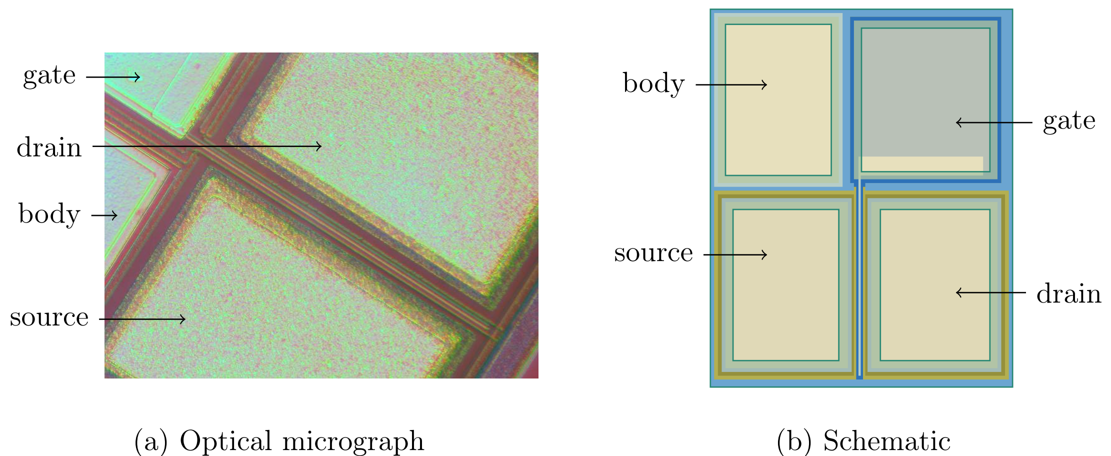


Figure 4.2
SIMS measurements (points) alongside SRIM simulation results for individual implant steps listed in Table 4.2 (dashed lines) and their total (solid line).

tion steps with intermediate removal taking place due to reprocessing. Lateral oxide growth also reduces the gate length by about twice this value, while simultaneously increasing the non-self alignment distance between the active channel and its contacts by the same amount.

Previous atomic force microscopy (AFM) measurements within the Active Sensor Structures for Extreme Environments (ASTRO) project at NU have shown that in forming Ni_2Si contacts Ni is consumed at approximately twice the rate of SiC [128]; for the 70 nm of Ni used in this study approximately 35(5) nm of SiC is expected to be consumed. This is notably beneficial for n-type contacts as the peak implant concentration is located approximately this distance below the post RIE surface, although will understandably increase the sheet resistance under the contact.



(a) Optical micrograph

(b) Schematic

Figure 4.3
An aerial view photomicrograph of a fabricated SiC n-channel lateral depletion-mode (NLDM) JFET with 9 µm gate length and 250 µm gate width and a corresponding schematic diagram with colours corresponding to those used in Figure 4.1; with nitride and top-up layer opacity has been reduced to preventt the visual obstruction of the lower layers.

The additional metallisation described in step 27 is intended to ensure thermal stability, by restricting diffusion into and away from the contact, and prevent damage from probing during electrical characterisation.

A magnified aerial-view photomicrograph of a completed JFET with 9 µm gate length and 250 µm gate width is shown in Figure 4.3 alongside a schematic illustration for comparison.

4.3 Ohmic Contacts

Ohmic contacts must be capable of providing the necessary current to a device with a voltage drop that is small compared with its active regions [126]. Unfortunately, it is very difficult to make low resistance ohmic contacts on wide band gap semiconductors, particularly to n- and p-type regions simultaneously, making it important to assess their impact on device performance [12]. Unlike in the case of a p-n junction, where both regions constitute a single crystal, the contact between a metal and a semiconductor gives rise to interface states. The act of forming the contact will influence the interface properties, thereby altering the distribution, nature and concentration of traps that act to pin the Fermi level and ultimately determine the barrier height [36]. Annealing of Ni/Ti and Al/Ti contacts on n- and p-type 4H–SiC, respectively, have been show to provide sufficiently low specific contact resistance to realise JFETs [129–133], and were thus adopted for this study.

Due to the low doping of the body epilayer and the omission of a pre-deposition implant, the contacts displayed rectifying characteristics, albeit with large leakage currents. When used as a JFET body contact any voltage with respect to the channel will be split across three series resistance components, those being the contact resistance, R_{c}, the bulk semiconductor resistance, R_{bulk}, and the p-n junction depletion layer resistance, R_{pn}. In normal device operation the body contact is always forward biased while the body-channel p-n junction is always reverse biased which given the thickness of the epilayer suggests $R_{\mathrm{c}} + R_{\mathrm{bulk}} \ll R_{\mathrm{pn}}$. As a result, any applied voltage will appear almost entirely across R_{pn}, allowing the body to be treated as a equipotential surface. Experimental JFET characteristics show this to be the case, making it unnecessary to consider the influence of these contacts further.

Conversely, R_{c} for channel contacts is required to be low to prevent gain reduction and limit the voltage burden. Also, as the gate contact can receive both positive and negative voltages under normal operation, R_{c} can noticeably affect device performance in cases where the gate-channel p-n junction shows excessive leakage.

The specific contact resistance,

$$\rho_{\mathrm{c}} = \lim_{V \to 0} \left(\frac{\mathrm{d}J}{\mathrm{d}V} \right)^{-1}, \tag{4.1}$$

represents the per unit area resistance of the contact and is typically specified in the limit of $V \to 0$. For back-to-back contacts the dynamic resistance is highest at this point, thereby providing a worst case value and thus a figure of merit. As current flow into lateral contacts is non-uniform, transfer length method (TLM) measurements were performed to determine the specific contact resistance for the gate and channel contacts. The TLM method also

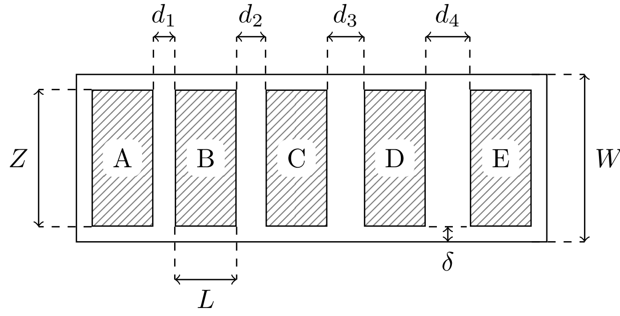


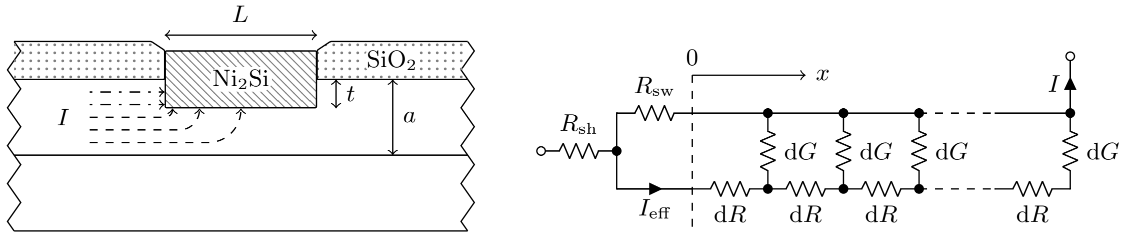
Figure 4.4
An aerial view schematics illustration of a transfer length method (TLM) test structure with mesa width W, contact width $Z = W - \delta$, contact length L and contact spacings d.

enables the sheet resistance,

$$R_{\mathrm{sh}} = \left[\int_0^a \sigma(y)\mathrm{d}y\right]^{-1}, \tag{4.2}$$

of the gate epilayer and implanted channel regions to be determined which denote the average resistivity over a sample of thickness a [126]. Figure 4.4 illustrates an aerial view of a TLM test structure, where W represents the mesa width and Z, L and d represent contact width, length and separation, respectively. For the wide contacts considered in this study (see Figures A.3 and A.4) the contact and mesa widths are approximately the same and the influence of lateral current flow around the contact sides on the calculated contact resistance will be insignificant [126, 134].

Finetti *et al.* suggested a suitable model for annealed contacts, as outlined in Figure 4.5. Horizontal current flow through the contact sidewall of thickness t is accounted for by a



(a) Cross sectional illustration. (b) Modified 2-D transmission line model.

Figure 4.5
Cross section of a transfer length method (TLM) test structure with annealed contacts, with mesa depth a, contact length L and contact depth into semiconductor t. I_{eff} represents the proportion of the current flowing vertically into the contact (dashed lines) with the remainder (dot-dash line) passing horizontal through the contact sidewall of resistance R_{sw}. R_{sh} is the semiconductor sheet resistance either side of the contact. dR and dG are transmission line model elements described in Equation 4.4.

shunt resistance

$$R_{\mathrm{sw}} = \frac{\rho_{\mathrm{c}}}{Zt}, \tag{4.3}$$

while vertical current flow,

$$I_{\mathrm{eff}} = I \frac{R_{\mathrm{sw}}}{R_{\mathrm{sw}} + R_{\mathrm{c,eff}}} \tag{4.4a}$$

is determined by a two-dimensional transmission line model with parameters,

$$\mathrm{d}R = \frac{R_{\mathrm{sk}}\mathrm{d}x}{Z}, \tag{4.4b}$$

with $R_{\mathrm{sk}} > R_{\mathrm{sh}}$ the sheet resistance under the contact and

$$\mathrm{d}G = \frac{Z\mathrm{d}x}{\rho_{\mathrm{c}}}, \tag{4.4c}$$

as illustrated in Figure 4.5b. Due to the high doping concentration being used for both the implanted channel and gate epilayers the influence of epilayer modulation by the back gate can be ignored. Accounting for the doping profile near the epilayer surface, the difference between R_{sk} and R_{sh} for n-type contacts, where 35(5) nm of SiC is consumed during contact formation, will be close to 10%. The experimental R_{c} is the parallel combination of R_{sw} and vertical contact resistance $R_{\mathrm{c,eff}}$. As R_{sw} is finite, $R_{\mathrm{c,eff}}$ is larger than R_{c}, and the calculated value of ρ_{c} will be higher than when expediently assuming R_{sw} is infinite.

Provided that the metal can be treated as an equipotential surface, the solution to the two-dimensional transmission line model reveals that the potential along the length of the channel reduces almost exponentially with distance as [126]

$$V(x) = \frac{I_{\mathrm{eff}}\sqrt{R_{\mathrm{sk}}\rho_{\mathrm{c}}}}{Z} \frac{\cosh[(L-x)/L_{\mathrm{T}}]}{\sinh(L/L_{\mathrm{T}})}, \tag{4.5a}$$

where L_{T} is termed the transfer length, defined as

$$L_{\mathrm{T}} = \sqrt{\rho_{\mathrm{c}}/R_{\mathrm{sk}}}, \tag{4.5b}$$

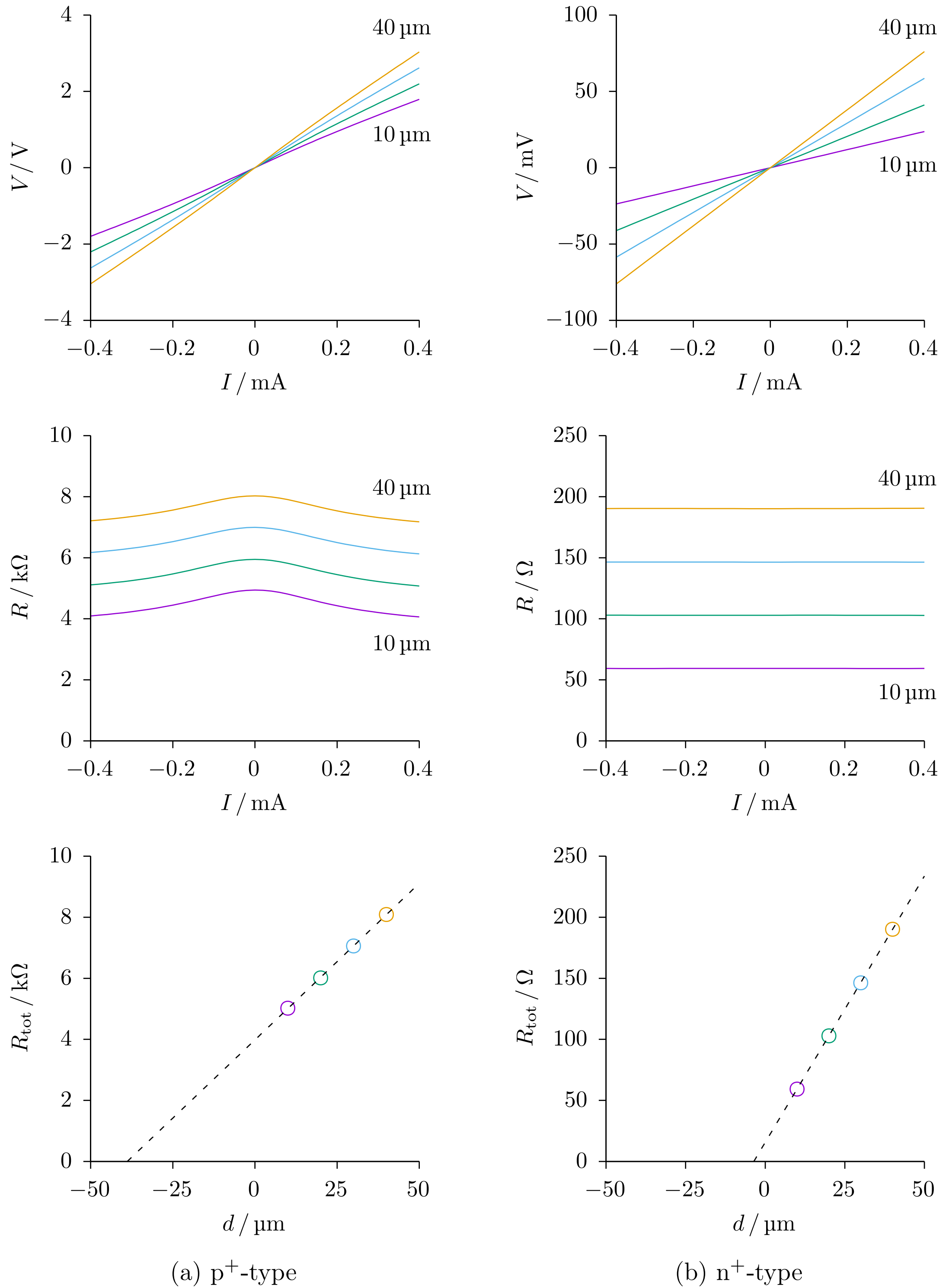
and represents the distance over which a significant proportion of I_{eff} is transferred between the semiconductor and the metal [126]. At the contact's front edge [126]

$$R_{\mathrm{c,eff}} = \frac{V(0)}{I_{\mathrm{eff}}} = \frac{\sqrt{R_{\mathrm{sk}}\rho_{\mathrm{c}}}}{Z} \coth(L/L_{\mathrm{T}}). \tag{4.5c}$$

As $L \gg L_{\mathrm{T}}$ (see Figure A.3 and Figure A.4) then $\coth(L/L_{\mathrm{T}}) \approx 1$ and the total resistance between pairs of TLM contacts is approximately [126]

$$R_{\mathrm{tot}} = \frac{R_{\mathrm{sh}}d}{Z} + 2R_{\mathrm{c}} \approx \frac{R_{\mathrm{sh}}}{Z}\left(d + 2L_{\mathrm{T}}\frac{R_{\mathrm{sk}}}{R_{\mathrm{sh}}}\right). \tag{4.6}$$

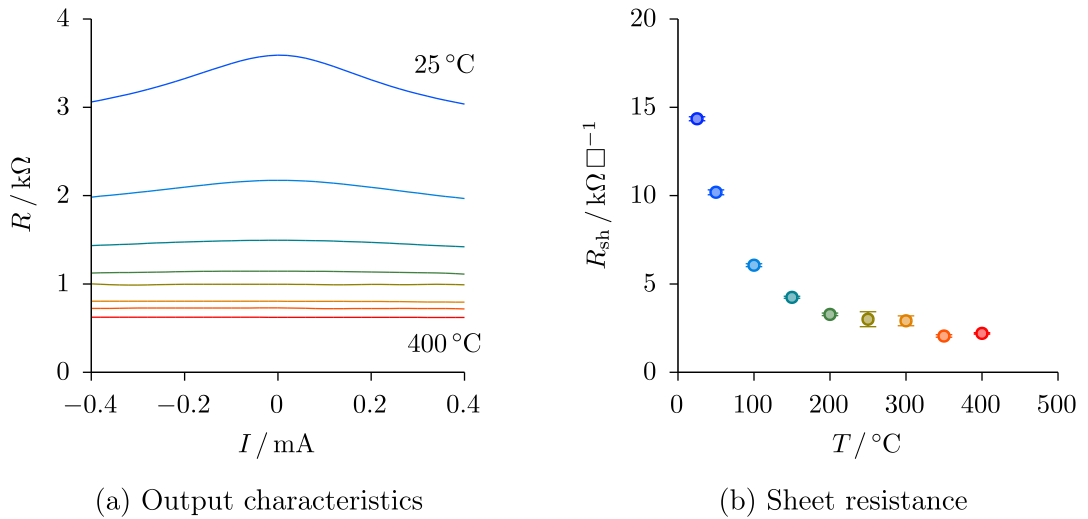
Equation 4.6 suggests a plot of total resistance as a function contact spacing will produce



(a) p$^+$-type (b) n$^+$-type

Figure 4.6

Room temperature transfer length method (TLM) measurements of annealed Al/Ti and Ni/Ti contacts on highly Al (2×10^{19} cm^{-3}) and N (2×10^{19} cm^{-3}) doped 4H-SiC, respectively. The utilised structures had contacts widths, Z, of 160 µm, nominal mesa depths, a, of 200 nm and 300 nm, respectively, utilised four contact spacings, d, each and displayed long contact behaviour.



(a) Output characteristics

(b) Sheet resistance

Figure 4.7

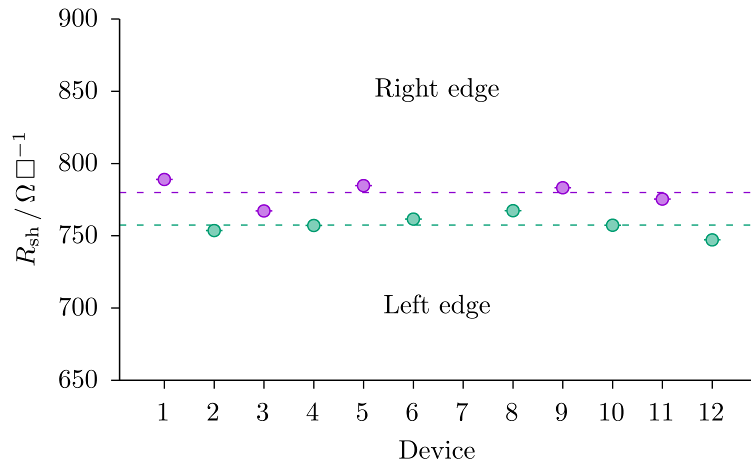
Variation in the total resistance, R_{tot}, between pairs of contacts 10 µm apart and the determined variation of sheet resistance, R_{sh}, with temperature.

a straight line with slope R_{sh}/Z and y-intercept of $2R_{\mathrm{c}}$, from which ρ_{c} can be determined provide Z is know [126]. As R_{sw} depends on ρ_{c} a self consistent approach is required.

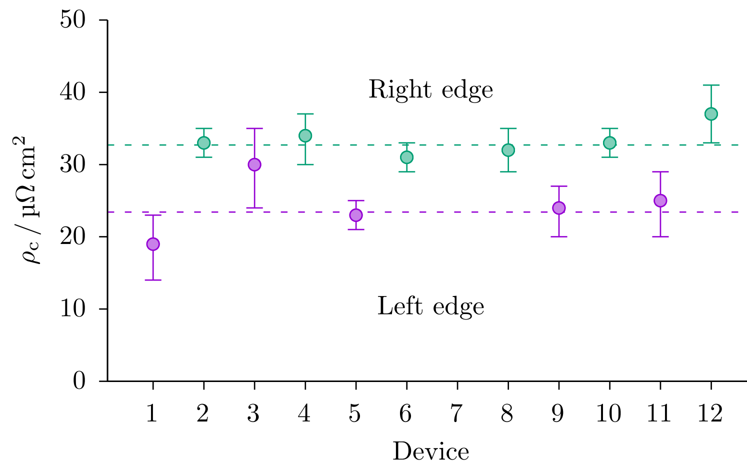
Figure 4.6 outlines the intermediate steps followed to obtain ρ_{c} and R_{sh} for both p- and n-type contacts at room temperature. R_{tot} values were determined from the dynamic resistances at zero volts, calculated using the second-order accurate central difference method [135] for four sets of contact spacings. Linear regression provided the best estimates for the slope and y-intercept in addition to their uncertainties [56]. The results of the regression were used to determine values for ρ_{c} and R_{sh} as well as their uncertainties. The determined room temperature values for ρ_{c} in each case were 42(4) mΩ cm^2 and 23(2) µΩ cm^2 for p- and n-type contacts, respectively.

From Figure 4.7 it is apparent that for p-type contacts both the sheet and contact resistances reduce with temperature between 25 °C and 400 °C, the former due to the dominant effect of dopant ionisation and the later due to increasing thermionic emission. Figure 4.7b explicitly illustrates the reduction of sheet resistance as determined by TLM measurements. These results suggest that p-type contacts will not impose a limit for high temperature device operation.

Twelve identically fabricated n-type TLM structure at evenly spaced points along left and right edges of a 10 mm by 10 mm sample were characterised, with the extracted room temperature sheet resistances and specific contact resistance values presented in Figure 4.8. Structure 7 was omitted due to process related damage. The left side of the sample provided on average lower specific contact resistance and higher sheet resistance than the right side, with two-sample t-tests indicating statistically significant differences with above 99% confidence. These differences are believed to stem from a combination of three effects. Firstly, the chosen process has been shown to be sensitive to the thickness of the Ti diffusion layer in the contact stack [136]. The sputtering process used for fabrication will result in appreciable



(a) Sheet resistance

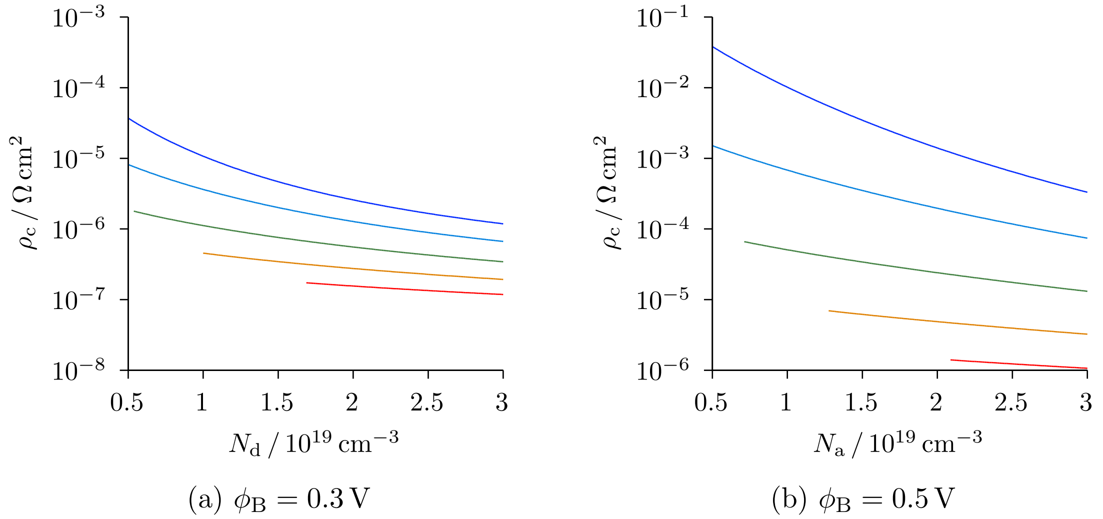


(b) Specific contact resistance

Figure 4.8

A comparison of sheet resistance, R_{sh}, and specific contact resistance, ρ_c, values for two columns of transfer length method (TLM) structures along the left (purple) and right (green) edges of a 10 mm by 10 mm 4H–SiC sample with N implanted ($2 \times 10^{19}\,\text{cm}^3$) epilayer as described in Figure 4.2. Error bars denote the standard error and the dashed lines represent weighted mean values for each group of values.

non-uniformity in deposition thickness for such thin layers. Secondly, the sample was annealed in a 25 mm by 40 mm ceramic heater with a circular heating element. The difference in temperature between the centre and the sides of the element during operation is evidenced by the varying intensity of light produced, suggesting the sample edge furtherest from the centre experienced a lower temperature anneal. Thirdly, a build up of photoresist occurs at the edge of the sample after spinning due to surface tension and the approach of spraying solvent to remove this excess cannot be used on small samples. This edge bead may have caused the photomasks to sit further from the surface at one edge, resulting in a variable



(a) $\phi_B = 0.3\,V$ (b) $\phi_B = 0.5\,V$

Figure 4.9

Plots of the WKB derived specific contact resistance expression in Equation 4.7 in the thermionic emission regime, at 25 °C, 100 °C, 200 °C, 300 °C and 400 °C at two different barrier heights, ϕ_B.

shortening of d. All three issues are controllable in large scale fabrication and are not cause for concern.

Comparable values for specific contact resistance were reported by Sundaramoorthy *et al.* for similar contacts, although no uncertainties were provided [136].

An approximate analytic expression for ρ_c where thermionic field emission (TFE) is the dominant transport mechanism can be derived in the framework of the Wentzel-Kramers-Brillouin (WKB) approximation to be [12]

$$\rho_{c,TFE} = \frac{k_B\sqrt{E_{00}}}{A^{**}Te\sqrt{\pi e(\phi_{B,n} - \phi_n)}} \cosh\left(\frac{E_{00}}{k_BT}\right) \coth\left(\frac{E_{00}}{k_BT}\right) e^{\frac{e(\phi_{B,n}-\phi_n)}{E_{00}\coth(E_{00}/k_BT)} + \frac{e\phi_n}{k_BT}} \tag{4.7a}$$

where the characteristic energy

$$E_{00} = \frac{e\hbar}{2}\left(\frac{N}{m^t\varepsilon_s}\right)^{1/2} \tag{4.7b}$$

is a function of the tunnelling effective mass, m^t, and for an n-type semiconductor

$$\phi_n = \frac{E_c - E_F}{e}, \tag{4.7c}$$

as measured in the bulk. Appropriate barrier heights for n- and p-type contacts were determined to be roughly 0.3 V and 0.5 V, respectively, and are in agreement with other published works [137, 138]. The predicted variations with temperature are presented in Figure 4.9 and indicate that contact resistance also will not limit device operation at high temperatures.

4.4 Compact Models

4.4.1 Introduction

The term compact models refers to the mathematical descriptions of electronic components used in circuit simulators [139]. Occam's razor is a guiding principle of rejecting unnecessary complexity. In the development of compact models the simplest approach that adequately represents experiment in all regions of interest should be viewed as the most desirable, both in terms of computational efficiency and usability. The primary objective is to account for any important electrical properties to within a small enough fraction of the process variation [140]. Aspects of device behaviour unimportant for intended operation include subthreshold conduction [141] and self-heating [142] and are therefore omitted. It is desirable to employ physical parameters where possible to provide greater insight into device behaviour and guidance during fabrication; however, empirical terms constitute an important strategy for achieving a balance between accuracy and efficiency [143].

Simulation Program with Integrated Circuit Emphasis (SPICE) simulators work by numerically solving for a consistent set of nodal voltages at the connection points between circuit elements, whose terminal behaviour will in general be described by a collection of non-linear differential equations [139]. Compact models must form conservative systems, whereby either or both of Kirchoff's flow and potential laws are satisfied*. Iterative techniques are employed whereby approximate solutions to the true nodal values are sought with convergence being achieved when sequential estimations differ by less than the chosen tolerances. This process requires that models be robust enough to accept any, potentially non-physical, values as initial or intermediate estimates. Models need also adhere to the restrictions imposed by the numerical techniques utilised, with the most important for SPICE simulators being that branch expressions and their first derivatives† should be continuous across their domains in order to accommodate the Newton-Raphson (NR) algorithm‡.

The proposed IC NLDM JFET compact models are represented by a collection of lumped elements describing different regions of the device. The quasi-static§ elements are first discussed. The primary component is a voltage-controlled current-source (VCCS) which is used to model current flow along the JFET channel in terms of¶ drain-source voltage, v_{DS}, gate-source voltage, v_{GS} and body-source voltage, v_{BS}. Dynamic model components are subsequently added to account for high frequency effects. Lastly, equations are introduced that correctly scale user and internal model parameters in response to changes in temperature.

4.4.2 Quasi-static models

Macroscopic devices can be adequately described in terms of spatially averaged quantities. In the linear region of operation the GCA is valid suggesting current transport along the channel

*The sum of all flows out of a node and the sum of branch potentials around all loops at any instance are zero.

†Some analysis techniques require higher order derivatives to be continuous also.

‡Small-signal analyses make strict use of linear models but rely of non-linear models for prior determination of bias points.

§A quasi-static model is valid for both static and low frequency large signal analysis.

¶The standard convention for signal variables is followed.

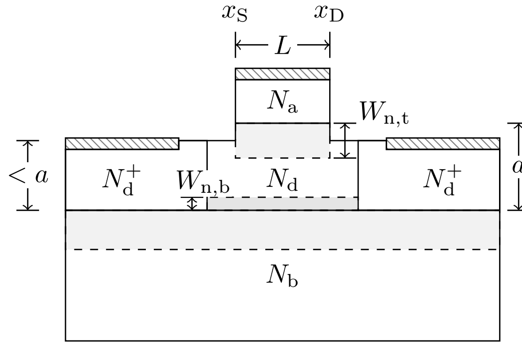


Figure 4.10
Cross sectional schematic structure for the JFET model being developed, indicating doping concentrations as well as pertinent dimensions and positions, where L is the channel length; a is the channel depth; $W_{d,t}$ and $W_{d,b}$ are the top and bottom gate depletion widths into the channel, respectively; N_a and N_b are the net acceptor doping concentrations in top and bottom gate epilayers; N_d is the net donor concentration in the device channel; N_d^+ is the implanted donor concentration at the source and drain contacts; and x_D and x_S are the drain and source ends of the channel, respectively.

(x-direction) and modulation of the depletion regions at the top and bottom of the channel (y-direction) are dominated by the electric field components $\mathscr{E}_x$ and $\mathscr{E}_y$, respectively. For a channel with depth a, width Z and top and bottom gate channel depletion widths of $W_{n,t}$ and $W_{n,b}$, respectively, as illustrated in Figure 4.10, the conduction electron charge in a slice of a homogeneous channel of length $\mathrm{d}x$ with electron density n is $enZ(a - W_{n,t} - W_{n,b})\mathrm{d}x$. For a spatially dependent mean drift velocity, v_d, of the form $\mu_{e,0}\mathscr{E}_x(1+\mathscr{E}_x/\mathscr{E}_c)^{-1}$, where $\mu_{e,0}$ is the low-field electron mobility and $\mathscr{E}_c$ is a critical field, the instantaneous drain-source current, i_{DS}, along the channel can be described by the separable first-order non-linear homogeneous ordinary differential equation

$$i_{DS} = en\mu_e Za\left(1 - \frac{W_{n,t}}{a} - \frac{W_{n,b}}{a}\right)\frac{\mathrm{d}\phi}{\mathrm{d}x}\left(1 + \frac{1}{\mathscr{E}_c}\frac{\mathrm{d}\phi}{\mathrm{d}x}\right)^{-1}, \tag{4.8a}$$

where ϕ is the position dependent potential along the channel.

Two models are introduced which differ only in the representation of $W_{n,b}$; model 1 assumes control by the body-source voltage only, while model 2 takes into account the potential distribution along the length of the channel. In the following descriptions it is assumed that the drain is at a higher potential than the source; reverse operation is achieved with appropriate changes in sign and branch notation [139].

The following convenient definitions are made. The open-channel conductance is defined as

$$G_0 = \frac{en\mu_e Za}{L}. \tag{4.9a}$$

The gate-channel and body-channel junction potentials at the source end of the channel are denoted by

$$\phi_{\mathrm{t}} = \phi_{0,\mathrm{t}} - v_{\mathrm{GS}} \tag{4.9b}$$

and

$$\phi_{\mathrm{b}} = \phi_{0,\mathrm{b}} - v_{\mathrm{BS}}, \tag{4.9c}$$

respectively, where $\phi_{0,\mathrm{t}}$ and $\phi_{0,\mathrm{b}}$ are the gate-channel and body-channel built-in potentials. The independent pinch-off voltages for the gate-channel and body-channel junctions are

$$\phi_{\mathrm{p,t}} = \frac{eN_{\mathrm{d,t}}a^2}{2\varepsilon_{\mathrm{s}}} \tag{4.9d}$$

and

$$\phi_{\mathrm{p,b}} = \frac{eN_{\mathrm{d,b}}a^2}{2\varepsilon_{\mathrm{s}}}, \tag{4.9e}$$

respectively, where ε_{s} is the semiconductor permittivity,

$$N_{\mathrm{d,t}} = \frac{N_{\mathrm{d}}\left(N_{\mathrm{a}} + N_{\mathrm{d}}\right)}{N_{\mathrm{a}}} \tag{4.9f}$$

and

$$N_{\mathrm{d,b}} = \frac{N_{\mathrm{d}}\left(N_{\mathrm{b}} + N_{\mathrm{d}}\right)}{N_{\mathrm{b}}}, \tag{4.9g}$$

wherein N_{a}, N_{d} and N_{b} represent the net active gate, channel and body epilayer doping concentrations, respectively. Lastly, a field dependent mobility parameter is defined by

$$\Xi = \left(L\mathscr{E}_{\mathrm{c}}\right)^{-1}, \tag{4.9h}$$

where L is the top gate length.

Model 1

Applying the GCA and assuming body-channel junction potential along the entire channel is not influenced by v_{DS},

$$i_{\mathrm{DS}} \int_{x_{\mathrm{S}}}^{x_{\mathrm{D}}} \left(1 + \frac{1}{\mathscr{E}_{\mathrm{c}}}\frac{\mathrm{d}\phi}{\mathrm{d}x}\right)\mathrm{d}x = en\mu_{\mathrm{e}}Za \int_{v_{\mathrm{S}}}^{v_{\mathrm{D}}} \left[1 - \left(\frac{\phi_{\mathrm{t}} - v_{\mathrm{S}} + \phi}{\phi_{\mathrm{p,t}}}\right)^{1/2} - \left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2}\right]\mathrm{d}\phi \tag{4.10a}$$

$$i_{\mathrm{DS}} + \frac{i_{\mathrm{DS}}v_{\mathrm{DS}}}{L\mathscr{E}_{\mathrm{c}}} = \frac{en\mu_{\mathrm{e}}Za}{L}\left[v_{\mathrm{DS}} - \phi_{\mathrm{p,t}}^{-1/2}\int_{\phi_{\mathrm{t}}}^{\phi_{\mathrm{t}}+v_{\mathrm{DS}}} u^{1/2}\mathrm{d}u - \left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2} v_{\mathrm{DS}}\right], \tag{4.10b}$$

providing the result

$$i_{\mathrm{DS}} = \frac{G_0}{1+\Xi v_{\mathrm{DS}}}\left\{v_{\mathrm{DS}} - \frac{2}{3}\phi_{\mathrm{p,t}}^{-1/2}\left[(\phi_{\mathrm{t}}+v_{\mathrm{DS}})^{3/2} - \phi_{\mathrm{t}}^{3/2}\right] - \left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2} v_{\mathrm{DS}}\right\}. \tag{4.10c}$$

Employing the abrupt depletion approximation (ADA) [12], the drain-source saturation voltage, $v_{\mathrm{DS,sat}}$, corresponding to the expop, occurs when

$$\frac{\mathrm{d}i_{\mathrm{DS}}}{\mathrm{d}v_{\mathrm{DS}}} = \left\{G_0\left[1 - \left(\frac{\phi_{\mathrm{t}}+v_{\mathrm{DS}}}{\phi_{\mathrm{p,t}}}\right)^{1/2} - \left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2}\right] - i_{\mathrm{DS}}\Xi\right\}(1+\Xi v_{\mathrm{DS}})^{-1} = 0. \tag{4.11a}$$

For the physical case where $\Xi > 0$,

$$v_{\mathrm{DS,sat}} = \left[\left(\Xi^{-1}-\phi_{\mathrm{t}}\right)\Upsilon_2^{-1} - \Upsilon_2\right]^2 - \phi_{\mathrm{t}}, \tag{4.11b}$$

where

$$\Upsilon_2 = \left\{\Upsilon_1 + \left[\Upsilon_1^2 + \left(\Xi^{-1}-\phi_{\mathrm{t}}\right)^3\right]^{1/2}\right\}^{1/3} \tag{4.11c}$$

and

$$\Upsilon_1 = \frac{3}{2}\phi_{\mathrm{p,t}}^{1/2}\Xi^{-1}\left[1 - \left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2}\right] - \phi_{\mathrm{t}}^{3/2}. \tag{4.11d}$$

For very long-channel devices it may be assumed that $\Xi = 0$, providing the simpler result

$$v_{\mathrm{DS,sat}} = \phi_{\mathrm{p,t}}\left[1 - 2\left(\frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right)^{1/2} + \frac{\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}}}\right] - \phi_{\mathrm{t}}. \tag{4.11e}$$

A real FET has no uniquely definable turn-off voltage* [126]. In the framework of the ADA the gate-source turn-off voltage, $v_{\mathrm{GS,off}}$, is defined as the potential applied to the top gate with respect to the source to reduce the channel width at the source to zero and is a function of the bottom gate potential. Equating the effective channel width at the source end of the channel to zero provides

$$a - \left[\frac{2\varepsilon_{\mathrm{s}}}{qN_{\mathrm{d,t}}}\left(\phi_{0,\mathrm{t}} - v_{\mathrm{GS,off}}\right)\right]^{1/2} - \left[\frac{2\varepsilon_{\mathrm{s}}}{qN_{\mathrm{d,b}}}\left(\phi_{0,\mathrm{b}} - v_{\mathrm{BS}}\right)\right]^{1/2} = 0 \tag{4.12a}$$

which on solving for $v_{\mathrm{GS,off}}$ gives

$$v_{\mathrm{GS,off}} = \phi_{0,\mathrm{t}} - \phi_{\mathrm{p,t}}\left[1 - \left(\phi_{\mathrm{p,b}}^{-1}\phi_{\mathrm{b}}\right)^{1/2}\right]^2. \tag{4.12b}$$

*This is more often referred to, somewhat ambiguously, as the threshold voltage.

An analogous expression can also be defined for the bottom gate turn-off voltage as

$$v_{\mathrm{BS,off}} = \phi_{0,\mathrm{b}} - \phi_{\mathrm{p,b}} \left[1 - \left(\phi_{\mathrm{p,t}}^{-1}\phi_{\mathrm{t}}\right)^{1/2}\right]^2 . \tag{4.13}$$

Model 2

Including the influence of v_{DS} on the body-channel junction potential,

$$i_{\mathrm{DS}} \int_{x_{\mathrm{S}}}^{x_{\mathrm{D}}} \left(1 + \frac{1}{\mathscr{E}_{\mathrm{c}}}\frac{\mathrm{d}\phi}{\mathrm{d}x}\right) \mathrm{d}x = en\mu_{\mathrm{e}}Za \int_{v_{\mathrm{S}}}^{v_{\mathrm{D}}} \left[1 - \sum_{s\in\{\mathrm{t,b}\}} \left(\frac{\phi_s - v_{\mathrm{S}} + \phi}{\phi_{\mathrm{p},s}}\right)^{1/2}\right] \mathrm{d}\phi \tag{4.14a}$$

$$i_{\mathrm{DS}}L + \frac{i_{\mathrm{DS}}}{\mathscr{E}_{\mathrm{c}}} \int_{v_{\mathrm{S}}}^{v_{\mathrm{D}}} \mathrm{d}\phi = en\mu_{\mathrm{e}}Za \left[\int_{v_{\mathrm{S}}}^{v_{\mathrm{D}}} \mathrm{d}\phi - \sum_{s\in\{\mathrm{t,b}\}} \int_{v_{\mathrm{S}}}^{v_{\mathrm{D}}} \left(\frac{\phi_s - v_{\mathrm{S}} + \phi}{\phi_{\mathrm{p},s}}\right)^{1/2} \mathrm{d}\phi\right] \tag{4.14b}$$

$$i_{\mathrm{DS}} + \frac{i_{\mathrm{DS}}v_{\mathrm{DS}}}{L\mathscr{E}_{\mathrm{c}}} = \frac{en\mu_{\mathrm{e}}Za}{L} \left[v_{\mathrm{DS}} - \sum_{s\in\{\mathrm{t,b}\}} \phi_{\mathrm{p},s}^{-1/2} \int_{\phi_s}^{\phi_s + v_{\mathrm{DS}}} u^{1/2}\mathrm{d}u\right] \tag{4.14c}$$

from which it is determined that

$$i_{\mathrm{DS}} = \frac{G_0}{1 + \Xi v_{\mathrm{DS}}} \left\{v_{\mathrm{DS}} - \frac{2}{3} \sum_{s\in\{\mathrm{t,b}\}} \phi_{\mathrm{p},s}^{-1/2} \left[(\phi_s + v_{\mathrm{DS}})^{3/2} - \phi_s^{3/2}\right]\right\}. \tag{4.14d}$$

In the limiting case of $\Xi = 0$,

$$\frac{\mathrm{d}i_{\mathrm{DS}}}{\mathrm{d}v_{\mathrm{DS}}} = G_0 \left[1 - \left(\frac{\phi_{\mathrm{t}} + v_{\mathrm{DS}}}{\phi_{\mathrm{p,t}}}\right)^{1/2} - \left(\frac{\phi_{\mathrm{b}} + v_{\mathrm{DS}}}{\phi_{\mathrm{p,b}}}\right)^{1/2}\right], \tag{4.15a}$$

giving a channel saturation voltage of

$$v_{\mathrm{DS,sat}} = \frac{\phi_{\mathrm{p,b}}\phi_{\mathrm{p,t}} - \phi_{\mathrm{p,b}}\phi_{\mathrm{t}} + \phi_{\mathrm{p,t}}\phi_{\mathrm{b}}}{\phi_{\mathrm{p,b}} - \phi_{\mathrm{p,t}}} \cdots$$

$$\cdots + \frac{2\phi_{\mathrm{p,b}}\phi_{\mathrm{p,t}} \left\{\phi_{\mathrm{p,t}} - \left[\phi_{\mathrm{p,b}}\phi_{\mathrm{p,t}} + (\phi_{\mathrm{t}} - \phi_{\mathrm{b}})(\phi_{\mathrm{p,t}} - \phi_{\mathrm{p,b}})\right]^{1/2}\right\}}{(\phi_{\mathrm{p,b}} - \phi_{\mathrm{p,t}})^2}. \tag{4.15b}$$

For $\Xi > 0$, an explicit solution for $v_{\mathrm{DS,sat}}$ is not possible; however, numerical methods can be employed to attain a suitable approximation to the true value. The NR method is a fast converging iterative technique whereby an increasingly better approximation to the root of a function of one dependent variable, $f(x)$, can be attained after each successive iteration subject to an appropriate initial estimate, x_0. The approximate solution to the root of $f(x)$ after n iterations is

$$x_n = x_0 - \sum_{k=0}^{n} \frac{f(x_k)}{f'(x_k)}. \tag{4.16}$$

An implicit requirement for this approach is that $f(x)$ and its first derivative, $f'(x)$, are

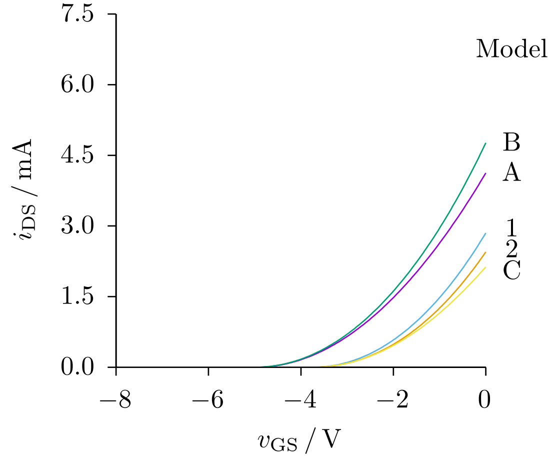


Figure 4.11

A comparison of the proposed JFET channel models, 1 and 2, with the conventional SPICE primitive (A), the Shockley model (B) and the Ding model (C), using the nominal parameters listed in Table 4.3, for $v_{BS} = 0\,V$, $v_{DS} = v_{DS,sat}$ and $\Xi = 0\,V^{-1}$.

continuous along the path of convergence*. As the root of the first derivative of i_{DS} with respect of v_{DS} is of interest, both the first and second derivative are required. Appropriate expressions for f and f' are therefore

$$\left\{1 - \Xi i_{DS} G_0^{-1} - \sum_{s \in \{t,b\}} \left[\phi_{p,s}^{-1}\left(\phi_s + v_{DS}\right)\right]^{1/2}\right\}\left(1 + \Xi v_{DS}\right)^{-1} \tag{4.17a}$$

and

$$\left\{ - 2\Xi f - \frac{1}{2} \sum_{s \in \{t,b\}} \left[\phi_{p,s}\left(\phi_s + v_{DS}\right)\right]^{-1/2}\right\}\left(1 + \Xi v_{DS}\right)^{-1}, \tag{4.17b}$$

respectively.

The value of $v_{GS,off}$ suitable for this model is equivalent to the result determined for model 1.

Comparison

A comparison of the aforementioned models with the SPICE primitive [144] (A), Shockley model [63] (B) and Ding model [79] (C), is presented in Figure 4.11 using the parameter values listed in Table 4.3; these values where calculated based on the envisaged device channel dimensions of 9 µm by 250 µm, the nominal epilayer thicknesses and doping concentrations quoted by the wafer manufacturer, the measured Hall-effect electron mobility and the results of the model presented in §3.7 assuming uncompensated homogeneous epilayers.

The single-gated models, A and B, predict a lower $v_{GS,off}$ than the remaining double-gate models. This can be overcome though use of an effective channel depth and would cause

*Such functions are said to be well behaved.

Table 4.3

Theoretically calculated nominal material specific compact model parameter values applicable to the fabricated devices under study, determined using the specifications from the wafer manufacturer and simulated conductivity values.

Parameter	G_0	$\phi_{0,\mathrm{t}}$	$\phi_{0,\mathrm{b}}$	$\phi_{\mathrm{p,t}}$	$\phi_{\mathrm{p,b}}$
Value	5.27 mS	2.94 V	2.81 V	7.93 V	402 V

models 1 and B as well as models C and A to overlap for $\Xi = 0\,\mathrm{V}^{-1}$. Normalisation be used to demonstrate that model 1 provides a closer approximation to model 2 than does model C, increasingly so for modest Ξ or decreasing N_b. The relationship between models C and 2 is analogous to the relationship between models A and B, affirming that model C will poorly represent changes in current for medium gate length JFETs when v_GS is appreciably larger than $v_\mathrm{GS,off}$.

A visual illustration of the position dependent modulation of the channel is presented in Figure 4.12 for models B and 2. Solutions to the channel position, x, as a function of the proportion of drain-source potential at x, $\phi_{x\mathrm{S}}$, are readily achieved through indefinite integration [63]. Assuming a constant low-field electron mobility along the entire channel to simplify the mathematics in this demonstration,

$$i_\mathrm{DS} = Zen\mu_\mathrm{e}\left\{a - \sum_{s\in S} W_{\mathrm{n},s}\right\}\frac{\mathrm{d}\phi_{x\mathrm{S}}}{\mathrm{d}x} \tag{4.18a}$$

$$= Zen\mu_\mathrm{e}\left\{a - \sum_{s\in S}\left[\frac{2\varepsilon_\mathrm{s}}{eN_{\mathrm{d},s}}\left(\phi_s + \phi_{x\mathrm{S}}\right)\right]^{1/2}\right\}\frac{\mathrm{d}\phi_{x\mathrm{S}}}{\mathrm{d}x} \tag{4.18b}$$

$$= G_0 L\left\{1 - \sum_{s\in S}\left[\frac{\phi_s + \phi_{x\mathrm{S}}}{\phi_{\mathrm{p},s}}\right]^{1/2}\right\}\frac{\mathrm{d}\phi_{x\mathrm{S}}}{\mathrm{d}x} \tag{4.18c}$$

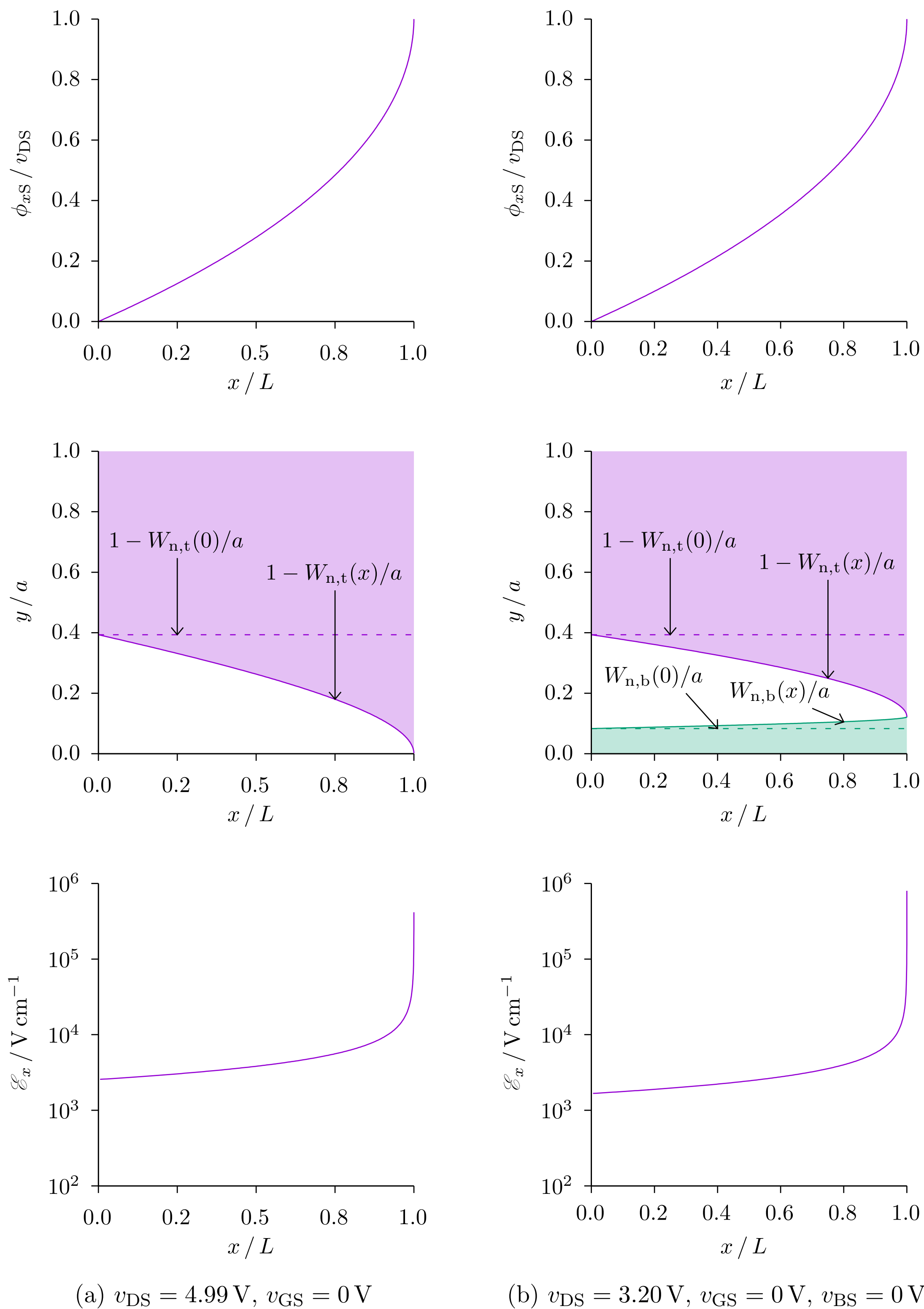
$$i_\mathrm{DS}\int \mathrm{d}x = G_0 L\left\{\int \mathrm{d}\phi_{x\mathrm{S}} - \sum_{s\in S}\int\left[\frac{\phi_s + \phi_{x\mathrm{S}}}{\phi_{\mathrm{p},s}}\right]^{1/2}\mathrm{d}\phi_{x\mathrm{S}}\right\}, \tag{4.18d}$$

providing the general solution

$$x = \frac{G_0 L}{i_\mathrm{DS}}\left\{\phi_{x\mathrm{S}} - \frac{2}{3}\sum_{s\in S}\phi_{\mathrm{p},s}^{-1/2}\left(\phi_s + \phi_{x\mathrm{S}}\right)^{3/2}\right\} - \frac{C}{i_\mathrm{DS}}. \tag{4.18e}$$

Applying the boundary condition $\phi_{x\mathrm{S}} = 0$ at $x = 0$, the particular value for the integration constant becomes,

$$C = -G_0 L\left\{\frac{2}{3}\sum_{s\in S}\phi_{\mathrm{p},s}^{-1/2}\phi_s^{3/2}\right\}, \tag{4.18f}$$



(a) $v_{DS} = 4.99\,\mathrm{V}$, $v_{GS} = 0\,\mathrm{V}$ (b) $v_{DS} = 3.20\,\mathrm{V}$, $v_{GS} = 0\,\mathrm{V}$, $v_{BS} = 0\,\mathrm{V}$

Figure 4.12

Comparison of the channel potential, depletion and electric field profiles between the Shockley (B) and the proposed JFET model (2) assuming constant mobility for a 9 µm gate length device with 300 nm channel depth, using nominal parameters listed in Table 4.3.

giving a particular solution

$$x = \frac{G_0 L}{i_{\mathrm{DS}}} \left\{ \phi_{x\mathrm{S}} - \frac{2}{3} \sum_{s \in S} \phi_{\mathrm{p},s}^{-1/2} \left[(\phi_s + \phi_{x\mathrm{S}})^{3/2} - \phi_s^{3/2} \right] \right\}. \tag{4.18g}$$

After substituting for i_{DS}, the explicit solution for the relative position along the channel, $0 \leq x/L \leq 1$, as a function of $\phi_{x\mathrm{S}}$ becomes

$$\frac{x}{L} = \frac{\phi_{x\mathrm{S}} - \frac{2}{3} \sum_{s \in S} \phi_{\mathrm{p},s}^{-1/2} \left[(\phi_s + \phi_{x\mathrm{S}})^{3/2} - {\phi_s}^{3/2} \right]}{v_{\mathrm{DS}} - \frac{2}{3} \sum_{s \in S} \phi_{\mathrm{p},s}^{-1/2} \left[(\phi_s + v_{\mathrm{DS}})^{3/2} - {\phi_s}^{3/2} \right]}, \quad \text{for } 0 \geq \phi_{x\mathrm{S}} \geq v_{\mathrm{DS}}. \tag{4.18h}$$

where S equals {t} and {t,b} for model B and 2, respectively.

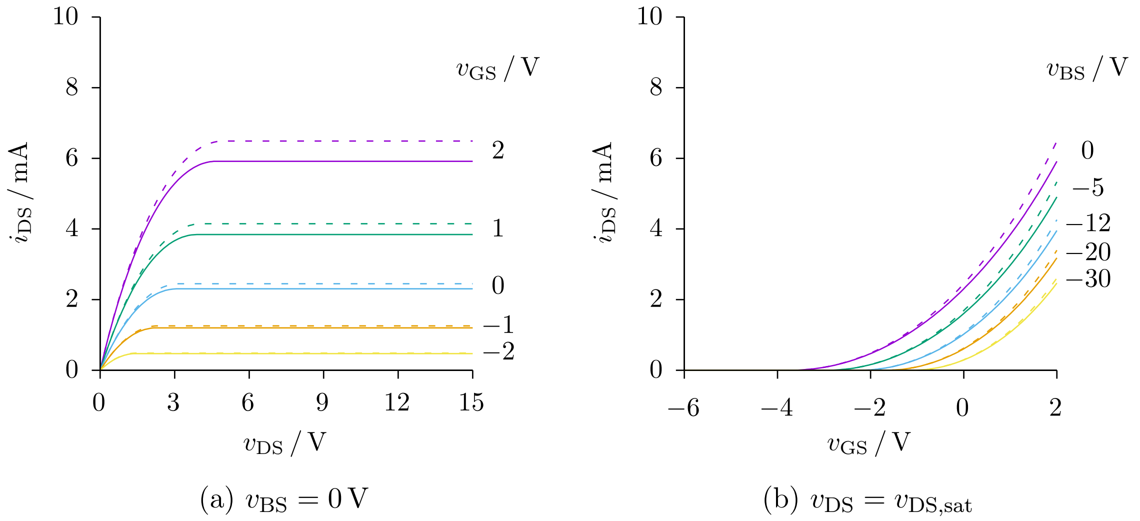
Figure 4.12b shows that encroachment of $W_{\mathrm{n,b}}$ into the channel epilayer due to $\phi_{0,\mathrm{b}}$ results in modest reduction of the active channel depth and is the reason for the difference in $v_{\mathrm{GS,off}}$ between the single- and double-gated models. $\phi_{x\mathrm{S}}$ is also seen to noticeably increase $W_{\mathrm{n,b}}$ above its equilibrium value, although to a much lesser extent than for $W_{\mathrm{n,t}}$, thereby further lowering i_{DS} and $v_{\mathrm{DS,sat}}$ compared with model 1. As N_{b} reduces this effect will become less apparent and model 1 will become a better approximation of model 2. Model B can be seen as a limiting case of both models 1 and 2 valid when the buffer epilayer is semi-insulating.

Mobility

The average electric fields seen in Figure 4.12 are large enough to noticeably reduce the average channel mobility, and more so as v_{GS} is increased. The images also highlight the breakdown of the GCA and the non-physical nature of the expop which predicts an unrealistic asymptotic increase in $\mathscr{E}$ to infinity at $x = L$; however, as this region is small compared to L it will not have a significant impact on the average value.

Figure 4.13 presents output and transfer characteristics for channel model 2 simulated using the nominal parameter values listed in Table 4.3. The effect of Ξ may be assessed by comparing the dashed and solid lines, denoting constant low-field mobility and field dependent mobility, respectively. For small v_{DS} the average $\mathscr{E}$ remains low enough to maintain the constant mobility approximation for all values of v_{GS}. Also, for v_{GS} close to $v_{\mathrm{GS,off}}$ the channel is already close to pinch-off causing $v_{\mathrm{DS,sat}}$ to be small and hence the average $\mathscr{E}$ to remain relatively low, too. As v_{GS} increases so does $v_{\mathrm{DS,sat}}$, allowing higher average values of $\mathscr{E}$ to be achieved and causing a more pronounced reduction in i_{DS}.

Figure 4.13b predicts large increases in $v_{\mathrm{GS,off}}$ with decreasing v_{BS}, with subsequent reductions in i_{DS} for fixed v_{GS}. This influence is extremely relevant for IC applications where devices are forced to share a common buffer epilayer. In the highly relevant case of an active loaded differential pair with shared current-sink, the bias dependent differences in v_{BS} between the amplifier loads and the sink require their aspect ratios to be carefully chosen to achieve a desire bias conditions. Such issues are discussed in detail in §5.3.



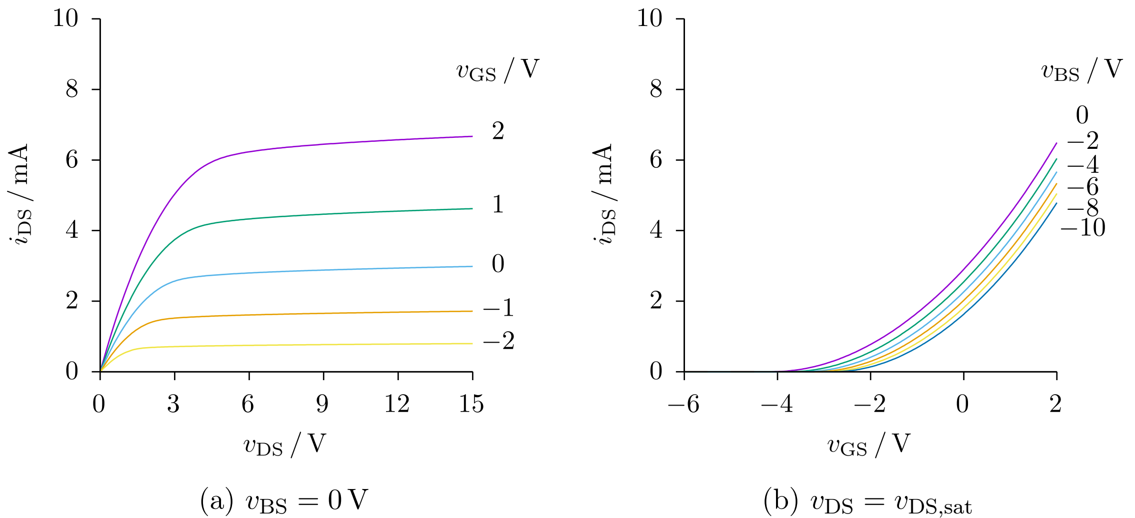
(a) $v_{BS} = 0\,\mathrm{V}$ (b) $v_{DS} = v_{DS,sat}$

Figure 4.13

Comparison output conductance and transconductance characteristics, emphasising the effect of terminal bias and electric field dependent mobility, using the nominal parameter values listed in Table 4.3 for $\Xi = 20\,\mathrm{mV}^{-1}$ (solid lines) and $\Xi = 0\,\mathrm{V}^{-1}$ (dashed lines).

Output Resistance

Two-dimensional technology computer aided design (TCAD) simulations were performed by Dr. Amit Tiwari of NU using representative material and geometric parameters for the fabricated devices in order to assess the validity of the GCA. The results presented in Figure 4.14 are in close agreement Figure 4.13 for v_{DS} smaller than $v_{DS,sat}$; however, as expected, the underlying assumptions break down in saturation.



(a) $v_{BS} = 0\,\mathrm{V}$ (b) $v_{DS} = v_{DS,sat}$

Figure 4.14

Technology computer aided design (TCAD) simulations for representative material and geometric parameters for the fabricated devices. Data courtesy of Dr. Amit Tiwari.

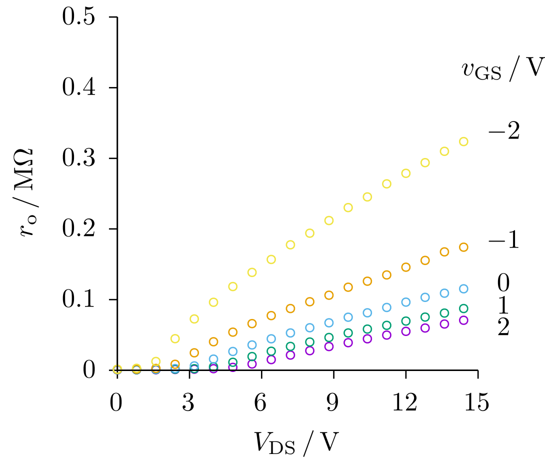


Figure 4.15

Room temperature experimental dynamic channel output resistance, r_o, as a function of drain-source voltage, V_{DS}, for pertinent gate-source voltages, V_{GS}.

As in other SPICE-like FET models a channel length modulation (CLM) parameter, λ, is included with the proposed compact model*. Experimental output resistance, r_o, results presented in Figure 4.15 demonstrate that unlike the conventional SPICE CLM model the resistance increases with v_{DS} above $v_{DS,sat}$ in a non-linear manner. Use of an effective voltage dependent CLM parameter

$$\lambda' = \frac{\lambda}{1 + \gamma \max\left(v_{DS} - v_{DS,sat}, 0\right)} \tag{4.19}$$

*The origin of this symbol in SPICE likely stems from the fact that the parameter has units of reciprocal voltage and the corresponding capital letter Λ looks like an upside down V.

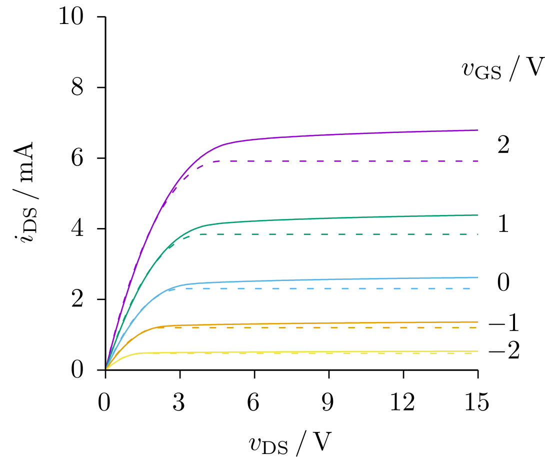


Figure 4.16

Comparison of the level 2 compact model with and without channel length modulation and expop smoothing expressions, using the channel length modulation parameters $\lambda = 2 \times 10^{-2}$ and $\gamma = 0.1$ and expop smoothing parameter value of $\chi = 0.1$.

was found to provide good agreement with experiment, where γ is an additional empirical CLM parameter.

While circuit simulators demand that i_{DS} and channel conductance, g_{ds}, be continuous while transitioning between the linear and saturation, the breakdown of the GCA within this region means the predicted behaviour is non-physical. The unnatural harshness of the transition can be reduced through use of a smoothing function that asymptotically limits the value of v_{DS} to below $v_{\mathrm{DS,sat}}$, producing an effective v_{DS} of

$$v_{\mathrm{DS,eff}} = \frac{2v_{\mathrm{DS}}}{\left[(1 - v_{\mathrm{DS}}/v_{\mathrm{DS,sat}})^2 + \chi\right]^{1/2} + \left[(1 + v_{\mathrm{DS}}/v_{\mathrm{DS,sat}})^2 + \chi\right]^{1/2}}, \tag{4.20}$$

where the empirical parameter $\chi \geq 0$ denotes the degree of softening, with a value around 0.1 providing suitable for agreement with experiment. Additional benefits of this approach is the reduced memory requirement during simulation as well as eliminating the potential discontinuity in the transition into saturation entirely which is particularly important while performing Fourier analysis in SPICE to determine an amplifier's total harmonic distortion (THD) [145]. Also, being odd symmetric, this function benefits from being suitable for forward and reverse mode of operation without modification [146].

A comparison JFET output characteristics with and without the further inclusion of the channel length modulation and expop smoothing expressions of the given by Equation 4.19 and Equation 4.20, respectively, is given in Figure 4.16; the dotted lines correspond with the solid lines shown in Figure 4.13. The characteristics closely follow those of the TCAD calculations shown in Figure 4.14.

Series Resistance

With reference to Figure 4.10, the series resistance appearing at the source and drain ends of the active channel are the sum of three independent parts.

The first the the contact resistance. A typical room temperature value of contact resistance, determined by the TLM for a 160 µm contact width was found to be 8 Ω. Scaling this value to match the width of the JFETs under study provides an estimated value of

$$8\,\Omega \times \frac{160\,\mu\mathrm{m}}{230\,\mu\mathrm{m}} = 5.6\,\Omega. \tag{4.21}$$

The second component is the series resistance of the implanted region of the channel epilayer extending past the contact edge. Using an average sheet resistance from Figure 4.8a and photomask information provides an estimate of

$$775\,\Omega\square^{-1} \times \frac{3}{250}\square = 9.3\,\Omega. \tag{4.22}$$

Total contact series resistance can therefore be estimate as

$$9.3\,\Omega + 5.6\,\Omega = 14.9\,\Omega. \tag{4.23}$$

The last is the resistances of the remaining non-self aligned regions either side of the channel. Accounting for the influence of oxidation on the lengths of the gate epilayer and the lengths of the non-self alignment regions defined in the photomasks, the nominal length of these regions, normalised by the length of the device channel will be approximately 0.34 and will be denoted by $\hat{x}_\mathrm{d}$ and $\hat{x}_\mathrm{s}$ between the drain and source, respectively. The process of isolating the gate and channel epilayers using a RIE step can result in varying amounts of vertical channel being removal. The relative depth of the channel epilayer either side of the remaining gate epilayer, normalised by the active channel depth, $\hat{y}_\mathrm{ds}$, is expected to be in the range $0.7 \leq y_\mathrm{ds} \leq 0.9$ based on the specifications provided by the wafer manufacturer, with a nominal value of 0.87. The volume of semiconductor described by these relative lengths constitutes additional voltage dependent series resistances either side of the channel and may be determined using the value of G_0, $\phi_{0,\mathrm{b}}$ and $\phi_{\mathrm{p,b}}$.

The coupling of these parameters is highly desirable as the temperature coefficients can also be shared between the three regions. This imposes constraints to the model and helps to provide more physical values model parameters derived through curve fitting.

Leakage

The forward and reverse bias characteristics of a p-n diode structure are depicted in Figure 4.17 and highlight two unideal leakage mechanisms not accounted for by the ideal diode equation. In forward bias an additional leakage mechanism results in non-negligible current to flow as low as 1.5 V. The series resistance is initially very large, suggesting an effective area that is much smaller than the total junction area is contributing. Such characteristics have been linked to barrier height inhomogeneities caused by deep level interface traps [147]. Excess reverse bias leakage currents exhibiting a power law behaviour with exponents above

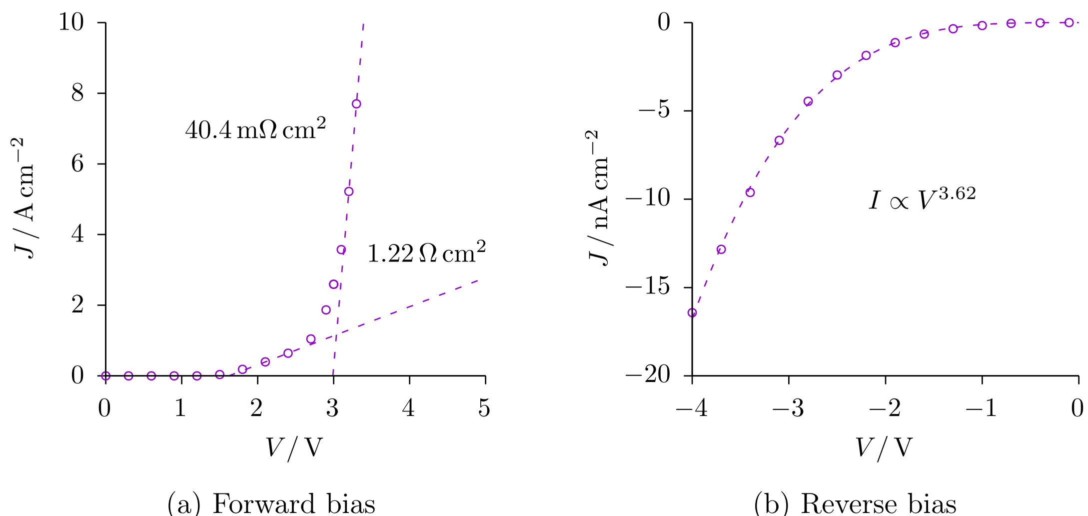


Figure 4.17
Experimental static p-n diode characteristics (points) and model fits (dashed lines) for a structure with cross sectional area $4.59 \times 10^{-4}\,\mathrm{cm}^2$.

unity* have previously been linked to impurity precipitates† [148–151]. This can occur when dopants are introduced in excess of their solid solubility limit‡ following which they agglomerate about existing defects and subsequently produce localised regions of enhanced electric field strength and hence an increase in the ionisation coefficients. Current is thus preferentially funnelled along discrete channels at these points known as microplasmas [9], with screw dislocations in the 4H–SiC having been identified as one such prominent cause [151].

For wide band gap semiconductors, in reverse bias either the recombination or pre-breakdown avalanche current will dominate at any given bias and temperature; a log-log plot enables the power law dependence to be determined from the slopes of the characteristics [152]. At room temperature an average value of 3.62 was determined for the device in Figure 4.17b at all points, suggesting its dominance over the Shockley-Read-Hall (SRH) process.

An empirical model commonly used to describe the reverse bias avalanche breakdown effect in p-n junctions is given by [12]

$$i_{\mathrm{st}} = \frac{I_{\mathrm{s}}}{1 - (v_{\mathrm{D}}/V_{\mathrm{b}})^{\beta}}, \quad \text{for } v_{\mathrm{D}} < 0, \tag{4.24}$$

was found to provide excellent agreement with the experimental data, where V_{b} and β are fitting parameters, I_{s} is the reverse saturation current derived from the ideal diode equation and v_{D} is the applied junction bias.

The experimental JFET characteristics exhibit the same characteristics as Figure 4.17b. The small junctions result in low currents which at room temperature are sub pA down to turn off and thereby have negligible influence on device performance. The extent of the

*Referred to as "soft" breakdown.

†Precipitates are agglomerations of intrinsic or extrinsic defects that expand about a nucleation point.

‡Supersaturation.

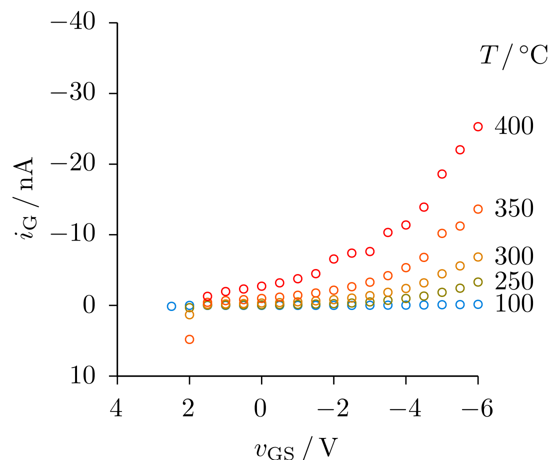


Figure 4.18

Experimental gate current, i_{G}, measured from a fabricated JFET with 9 µm gate length and 250 µm gate width, under drain-source bias, $v_{\mathrm{DS}} = 10\,\mathrm{V}$, body-source bias, $v_{\mathrm{BS}} = 0\,\mathrm{V}$ between 100 °C and 400 °C.

leakage current varied markedly between devices, suggesting an underlying material quality as opposed to a processing issue. Even at 400 °C the reverse bias leakage remains in the low nA range as shown in Figure 4.18. The increasing current offset at $v_{\mathrm{GS}} = 0\,\mathrm{V}$ suggests that the critical field for tunnelling reduces with temperature. As v_{GS} increases the maximum field across the junction reduces below the critical field and the current reduces. The onset of forward bias diffusion current can be observed around 2 V at 400 °C, which can be taken as an upper limit for device operation.

Validation

A complete large-signal quasi-static JFET model, including static drain, gate, source and bulk series resistances, R_{D}, R_{G}, R_{S}, and R_{B}, respectively*, and instantaneous gate-drain, gate-source, body-drain and body-source junction leakage currents, i_{GD}, i_{GS}, i_{BD}, i_{BS}, respectively, is presented in Figure 4.19. The minor discrepancies are largely due to inconsistencies in the collected data for equivalent bias points taken from different sweeps; as measurement were performed simultaneously using the same equipment it is believed that self-heating is responsible for the differences.

The model was implemented in Synopsys HSPICE wherein a modified Levenberg-Marquardt algorithm (LMA)† was used to optimise the model parameters against experimental data. A comparison between simulated and experimental data for a JFET with $L = 9\,\mu\mathrm{m}$ at 25 °C is shown in Figure 4.20 after the final optimisation stage. The data used in the fits were limited to regions of negligible leakage current so that the channel parameters could be optimised in isolation. The initial, intermediate and final parameter values determined by the fit are listed in Table 4.4. The initial estimate were selected based on calculated nominal values.

*The large-signal resistance will differ the static resistances on account of the non-linear dependence of current with respect to applied voltage.

†Non-linear functions require iterative methods to approximately determine the minimum point of the multi-dimensional error surface to within a given tolerance. The LMA is a robust and efficient method that harnesses the benefits of both the gradient-decent and Gauss-Newton methods [56].

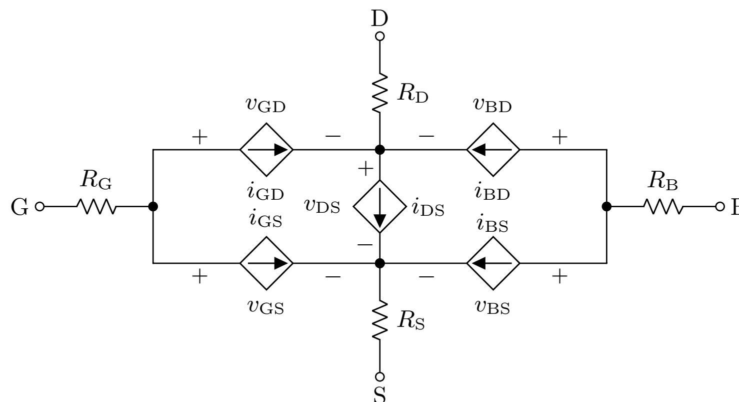
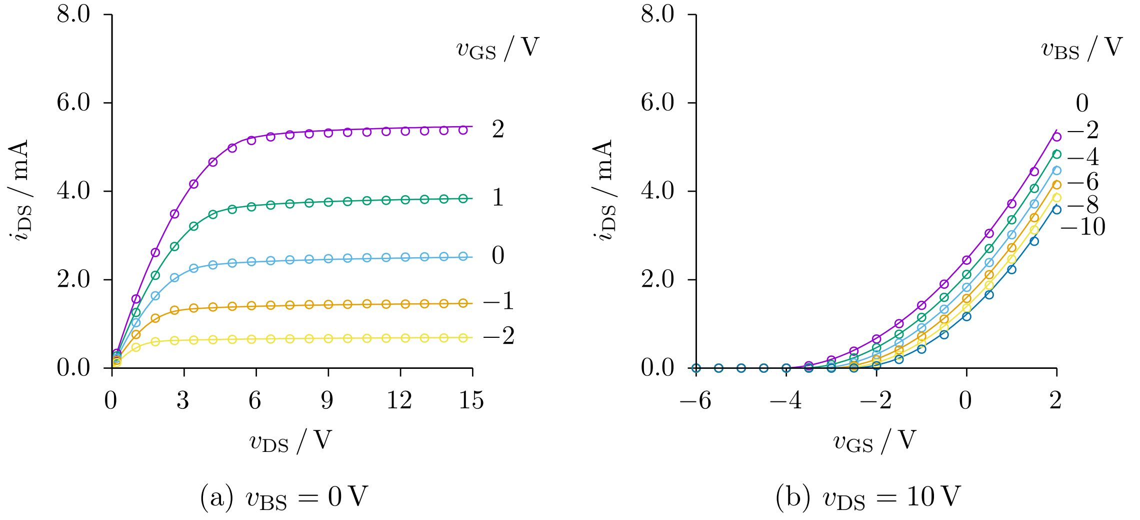


Figure 4.19

Schematic illustration of the proposed quasi-static JFET compact model, including series resistances and junction leakage currents.



(a) $v_{BS} = 0$ V (b) $v_{DS} = 10$ V

Figure 4.20

A comparison between experimental JFET measurements (points) and the complete proposed compact model (CM) with optimised parameters (lines) under various bias conditions at 25 °C. The utilised model parameters are listed in Table 4.4.

Table 4.4

Process steps used to optimise the compact model parameters for a n-channel lateral depletion model JFET at 25 °C. Initial estimates were selected based on experimental measurements and theoretical calculations. The first optimisation stages was used to update the first-order parameters, G_0, $\phi_{p,t}$ and $\phi_{p,b}$ only, with a second stage included the second-order effects. Parameters $\phi_{0,t}$, $\phi_{0,b}$, $\hat{x}_d$, $\hat{x}_s$ and R_c were initialised to accurately determined values and held constant throughout the optimisation.

Parameter	Units	Value		
		Initial	Update 1	Update 2
G_0	mS	5.27	5.09	5.07
$\phi_{0,t}$	V	2.92	-	-
$\phi_{0,b}$	V	2.81	-	-
$\phi_{p,t}$	V	7.93	8.62	8.61
$\phi_{p,b}$	V	402	340	321
Ξ	mV^{-1}	20	-	38.9
λ	mV^{-1}	20	-	45.6
γ	mV^{-1}	100	-	153
χ	10^{-1}	1	-	1.89
R_c	Ω	15	-	-
$\hat{x}_d$, $\hat{x}_s$	1	0.34	-	-
$\hat{y}_{ds}$	1	0.87	-	0.9

The range input for each parameter was limited to physically significant values; for example, the uncertainty in the channel depth and the epilayer doping concentrations provide value ranges for the top and bottom gate pinch-off voltages of [6.45 : 9.58] and [219 : 964], respectively. To avoid conflict between parameters appropriate values for $\phi_{0,\mathrm{t}}$, $\phi_{0,\mathrm{b}}$, $\hat{x}_{\mathrm{d}}$, $\hat{x}_{\mathrm{s}}$ and R_{c}, determined experimentally or theoretically, were fixed during the entire optimisation process. To to their dominant role in the model equations and their large uncertainty an initial optimisation was performed where the parameters G_0, $\phi_{\mathrm{p,t}}$ and $\phi_{\mathrm{p,b}}$ due simultaneously updated (Update 1). These values were subsequently as the initial estimates in the second and final optimisation (Update 2), that included the second-order effect parameters.

4.4.3 Large-signal model

A complete large-signal model extends the quasi-static model to include parasitic capacitances as illustrated schematically in Figure 4.21. As the impedance of a capacitor is frequency dependent they introduce a limit on the bandwidth of a FET amplifier.

Capacitance is defined as the differential flow of charge with applied voltage. In a p-n junction both the change in depletion width and the change in minority carrier densities contribute to the total capacitance, and are referred to as junction and diffusion capacitances, C_{j} and C_{d}, respectively [31]. For typically device operation C_{d} will contribute negligibly to the total and can be ignored [17].

The C_{j} model originally proposed by Statz can be used to overcome the shortcomings of the diode-like models used in the SPICE primitive [144, 153], but requires careful treatment to incorporate it into a compact model. Following the approaches proposed by Divekar and Smith [154–156] the instantaneous gate-source and gate-drain charges, q_{GD} and q_{GS},

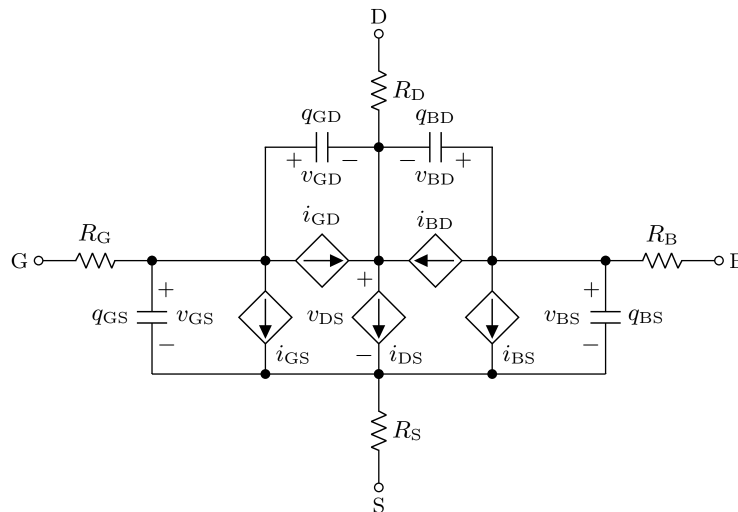


Figure 4.21
Schematic illustration of the proposed large-signal JFET compact model, including series resistances, junction leakage currents and charge storage.

respectively, can be represented by

$$q_{\mathrm{GS}} = \begin{cases} C_{\mathrm{gs}}(0)\left[2\phi_{0,\mathrm{t}}\left(1-\sqrt{1-\dfrac{V_{\mathrm{max}}}{\phi_{0,\mathrm{t}}}}\right)+\dfrac{v_{\mathrm{new}}-V_{\mathrm{max}}}{\sqrt{1-V_{\mathrm{max}}/\phi_{0,\mathrm{t}}}}\right], & \text{for } v_{\mathrm{new}} > \mathrm{FC}\phi_{0,\mathrm{t}} \\ 2C_{\mathrm{gs}}(0)\phi_{0,\mathrm{t}}\left(1-\sqrt{1-\dfrac{v_{\mathrm{new}}}{\phi_{0,\mathrm{t}}}}\right), & \text{for } v_{\mathrm{new}} \le \mathrm{FC}\phi_{0,\mathrm{t}} \end{cases} \tag{4.25a}$$

and

$$q_{\mathrm{GD}} = C_{\mathrm{gd}}(0)v_{\mathrm{eff},2}, \tag{4.25b}$$

where $C_{\mathrm{gd}}(0)$ and $C_{\mathrm{gs}}(0)$ are the equilibrium gate-drain and gate-source capacitances, respectively,

$$v_{\mathrm{eff},1} = \frac{1}{2}\left(v_{\mathrm{GS}}+v_{\mathrm{GD}}+\sqrt{\left(v_{\mathrm{GS}}-v_{\mathrm{GD}}\right)^2+\Delta_1^2}\right), \tag{4.25c}$$

$$v_{\mathrm{eff},2} = \frac{1}{2}\left(v_{\mathrm{GS}}+v_{\mathrm{GD}}-\sqrt{\left(v_{\mathrm{GS}}-v_{\mathrm{GD}}\right)^2+\Delta_1^2}\right) \tag{4.25d}$$

$$v_{\mathrm{new}} = \frac{1}{2}\left(v_{\mathrm{eff},1}+v_{\mathrm{GS,off}}+\sqrt{\left(v_{\mathrm{eff},1}-v_{\mathrm{GS,off}}\right)^2+\Delta_2^2}\right), \tag{4.25e}$$

and

$$V_{\mathrm{max}} = \min(\mathrm{FC}\phi_{0,\mathrm{t}}, V_{\mathrm{max}}). \tag{4.25f}$$

In reverse mode* the values of q_{GS} and q_{GD} or should be swapped. Similar expressions can be attained for the bottom gate charges, q_{BD} and q_{BS}, by replacing the voltages v_{GD}, v_{GS} and $v_{\mathrm{GS,off}}$ with v_{BD}, v_{BS} and $v_{\mathrm{BS,off}}$, respectively, and zero bias capacitances C_{gd} (0) and C_{gs} (0) withC_{bd} (0) and C_{bs} (0), respectively.

The fitting parameters Δ_1 and Δ_2 described the drop in capacitance close to channel turn-off. These values will be temperature dependent, but suitable values to provide agreement with experimental measurements at room temperature are approximately 0.5 V and 0.2 V, respectively.

4.4.4 Small-signal model

Circuit simulators construct small-signal models automatically by linearising the quasi-static or large-signal models at the predetermined operating point. The quasi-static small-signal model assuming no leakage is presented in Figure 4.22.

The transconductance,

$$g_{\mathrm{m}} = \left.\frac{\partial i_{\mathrm{DS}}}{\partial v_{\mathrm{GS}}}\right|_{\mathrm{OP}} = G_0\left[\frac{\sqrt{\phi_{0,\mathrm{t}}-V_{\mathrm{GS}}+V_{\mathrm{DS}}}-\sqrt{\phi_{0,\mathrm{t}}-V_{\mathrm{GS}}}}{\sqrt{\phi_{\mathrm{p,t}}}\left(1+\Xi V_{\mathrm{DS}}\right)}\right] \tag{4.26a}$$

*In reverse mode operation the source terminal is held at a higher potential than the source.

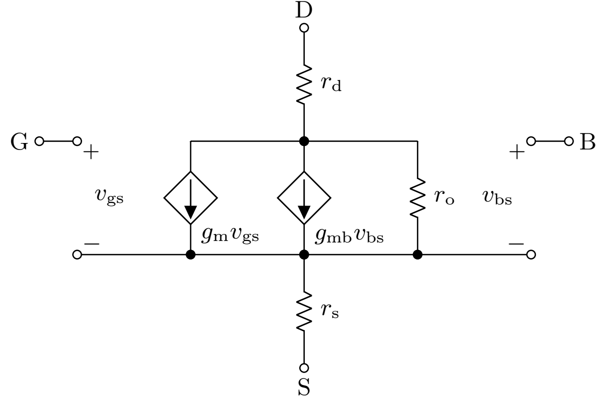


Figure 4.22
Schematic illustration of the low-leakage quasi-static small-signal model for the proposed JFET compact model, where r_d and r_s are the dynamic drain and source series resistances, respectively, r_o is the dynamic output resistance, v_gs and v_bs are the gate-source and body-source signal voltages, respectively, and g_m and g_mb are the transconductance and body-transconductance, respectively.

and body-transconductance,

$$g_\mathrm{mb} = \left.\frac{\partial i_\mathrm{DS}}{\partial v_\mathrm{BS}}\right|_\mathrm{OP} = G_0 \left[\frac{\sqrt{\phi_{0,\mathrm{b}} - V_\mathrm{BS} + V_\mathrm{DS}} - \sqrt{\phi_{0,\mathrm{b}} - V_\mathrm{BS}}}{\sqrt{\phi_{\mathrm{p,b}}}\,(1 + \Xi V_\mathrm{DS})} \right], \tag{4.26b}$$

expressed here for model 2, are the small-signal parameters that quantify the ability of a FET to act as amplifier [145]. Plots of Equations 4.26a and 4.26b using the nominal parameters values listed in Table 4.3 are presented in Figure 4.23 as functions of gate-source and body-source bias voltages V_GS and V_BS, respectively. The results evidence the importance of using a model capable of accurately describing the body-effect.

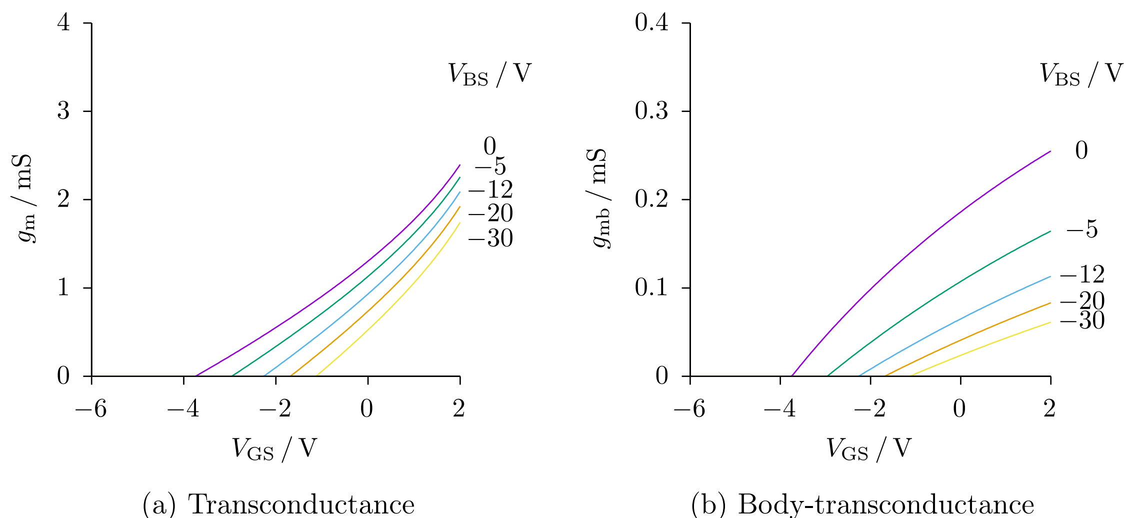
The product of a FET's transconductance and output resistance,

$$r_\mathrm{o} = g_\mathrm{ds}^{-1} = \left.\frac{\partial v_\mathrm{DS}}{\partial i_\mathrm{DS}}\right|_\mathrm{OP} \tag{4.27}$$

is a figure of merit representing an upper limit for voltage gain. Experimental room temperature values for r_o for a range of bias conditions were given in Figure 4.15. Under typical operation g_m and r_o are of the order of 1 mS and 100 kΩ, suggesting intrinsic gains in the region of 100.

To maintain the reverse bias of the body-channel p-n junction the substrate is usually connected to the most negative supply voltage in the circuit [90]. Unfortunately, this will result in an unwanted reduction in g_m. Conversely, in §5.3 it will be shown that if the buffer layer is shared by all devices the voltage gain can be increased when depletion mode (DM) load devices with lower g_mb are used, and in cases where this is the limiting factor its reduction with v_BS can outweigh the reduction in g_m of the amplifying transistor.

The intrinsic values of g_ds, g_m and g_mb, described by Equations 4.26 and 4.27, are affected



(a) Transconductance (b) Body-transconductance

Figure 4.23
Intrinsic transconductance and body-transconductance for channel model 2 using the nominal parameter values listed in Table 4.3 for $\Xi = 0\,\mathrm{V}^{-1}$.

by the parasitic resistances. Externally observed values become [144]

$$g_{\mathrm{ds,obs}} \approx \frac{g_{\mathrm{ds}}}{1 + (r_{\mathrm{s}} + r_{\mathrm{d}})\, g_{\mathrm{ds}}}, \tag{4.28a}$$

$$g_{\mathrm{m,obs}} \approx \frac{g_{\mathrm{m}}}{1 + r_{\mathrm{s}} g_{\mathrm{m}}} \tag{4.28b}$$

and

$$g_{\mathrm{mb,obs}} \approx \frac{g_{\mathrm{mb}}}{1 + r_{\mathrm{s}} g_{\mathrm{mb}}}, \tag{4.28c}$$

assuming the leakage current is small. A more detailed treated reveals that, for example,

$$\begin{aligned}
g_{\mathrm{m,obs}} &= \frac{\partial i_{\mathrm{DS}}}{\partial (v_{\mathrm{GS}} + v_{R_{\mathrm{G}}} + v_{R_{\mathrm{S}}})} && (4.29\mathrm{a})\\
&= \left[\frac{\partial v_{\mathrm{GS}}}{\partial i_{\mathrm{DS}}} + \frac{\partial v_{R_{\mathrm{G}}}}{\partial i_{\mathrm{DS}}} + \frac{\partial v_{R_{\mathrm{S}}}}{\partial i_{\mathrm{DS}}}\right]^{-1} && (4.29\mathrm{b})\\
&= \left[g_{\mathrm{m}}^{-1} + \frac{\partial v_{R_{\mathrm{G}}}}{\partial i_{R_{\mathrm{G}}}}\frac{\partial i_{R_{\mathrm{G}}}}{\partial i_{\mathrm{DS}}} + \frac{\partial v_{R_{\mathrm{S}}}}{\partial i_{R_{\mathrm{S}}}}\frac{\partial i_{R_{\mathrm{S}}}}{\partial i_{\mathrm{DS}}}\right]^{-1} && (4.29\mathrm{c})\\
&= g_{\mathrm{m}}\left[1 + g_{\mathrm{m}} r_{\mathrm{g}}\frac{\partial i_{R_{\mathrm{G}}}}{\partial i_{\mathrm{DS}}} + g_{\mathrm{m}} r_{\mathrm{s}}\frac{\partial i_{R_{\mathrm{S}}}}{\partial i_{\mathrm{DS}}}\right]^{-1} && (4.29\mathrm{d})\\
&\approx g_{\mathrm{m}}\left[1 + g_{\mathrm{m}} r_{\mathrm{s}}\right]^{-1}, \quad \text{for } i_{R_{\mathrm{G}}} \to 0, i_{R_{\mathrm{S}}} \to i_{\mathrm{DS}} && (4.29\mathrm{e})
\end{aligned}$$

which in the more general form must be solved numerically.

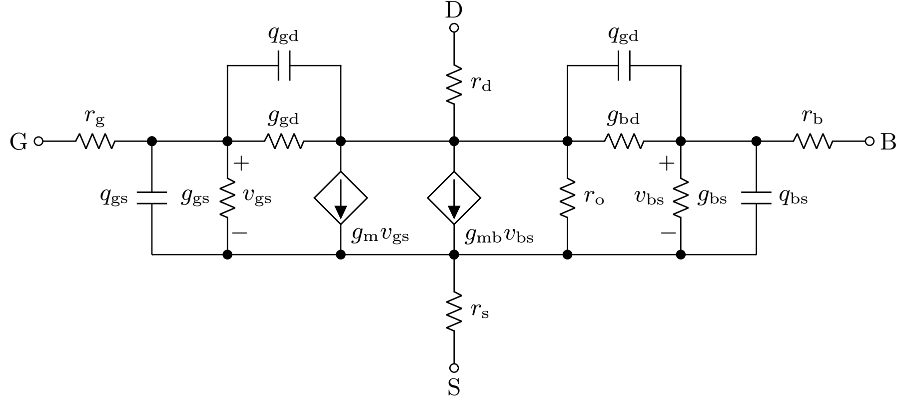


Figure 4.24

Schematic illustration of the low-leakage high-frequency small-signal model for the proposed JFET compact model, where $r_{\rm d}$, $r_{\rm g}$, $r_{\rm s}$ and $r_{\rm b}$ are the dynamic drain, gate, source and bulk series resistances, respectively, $r_{\rm o}$ is the dynamic output resistance, $v_{\rm gs}$ and $v_{\rm bs}$ are the gate-source and body-source signal voltages, respectively, $g_{\rm m}$ and $g_{\rm mb}$ are the transconductance and body-transconductance, respectively, $g_{\rm gd}$, $g_{\rm gs}$, $g_{\rm bd}$ and $g_{\rm bs}$ are small-signal conductances and $q_{\rm gd}$, $q_{\rm gs}$, $q_{\rm bd}$ and $q_{\rm bs}$ are signal charges.

The gate-drain and gate-source conductances,

$$g_{\rm gd} = \frac{i_{\rm gd}}{v_{\rm gd}} = \left.\frac{\partial i_{\rm GD}}{\partial v_{\rm GD}}\right|_{\rm OP} \tag{4.30}$$

and

$$g_{\rm gs} = \frac{i_{\rm gs}}{v_{\rm gs}} = \left.\frac{\partial i_{\rm GS}}{\partial v_{\rm GS}}\right|_{\rm OP} \tag{4.31}$$

are expected to be small on account of the very high resistance of the gate-channel depletion region, as will the body-channel conductances, $g_{\rm bd}$ and $g_{\rm bs}$. The impedance of these junctions will reduce as the applied signal frequency is increased. The complete high-frequency small-signal model including dynamic series resistances is given in Figure 4.24 where $q_{\rm gd}$, $q_{\rm gs}$, $q_{\rm bd}$ and $q_{\rm bs}$ define the lumped signal charges for the top and gate p-n junctions at the drain and source end of the channel and $g_{\rm gd}$, $g_{\rm gs}$, $g_{\rm bd}$ and $g_{\rm bs}$ are corresponding junction conductances.

4.4.5 Thermal models

Semiconductor devices are highly sensitive to changes in temperature. The influence is exemplified for the NLDM JFETs under investigation by the experimental data (points) presented in Figure 4.25 which are presented alongside the corresponding optimised simulation results (lines) using the completed thermal model developed in this section; the parameters used are given in Table B.1. It is worth noting that the discrepancies in the model are primarily a result of inconsistency of the experimental data taken from different sweeps.

An expedient and commonly adopted approach to account for model variation with temperature is to independently model the device at every temperature of interest. One

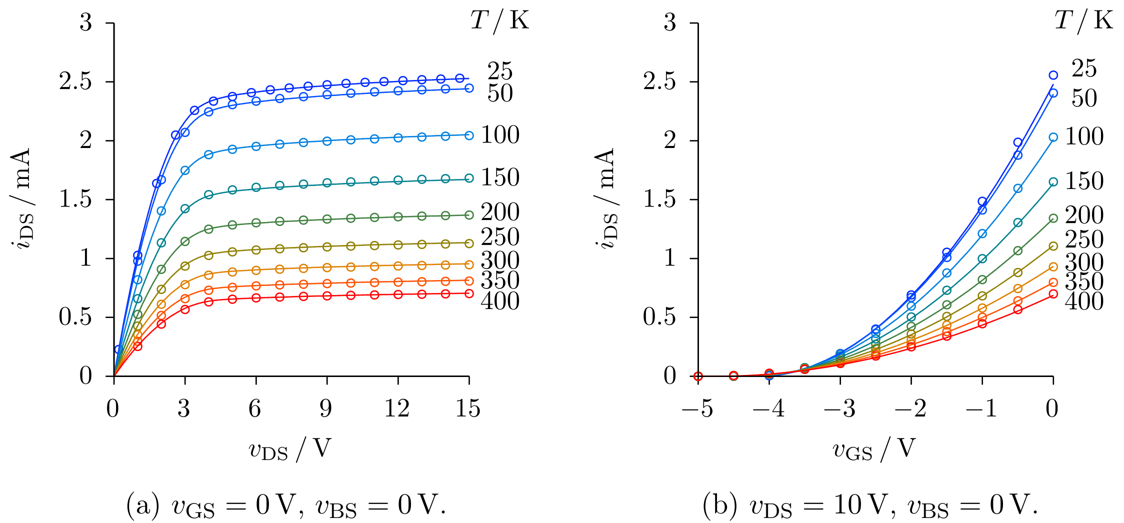


Figure 4.25

Experimental variation in drain-source current, i_{DS}, with temperature, T, between 25 °C and 400 °C at various bias conditions (points) and the optimised compact model simulation results determined using a multi-step modified Levenberg-Marquardt optimisation algormithms within HSPICE, following the process described in §4.4.2, for a nominal temperature, T_n, of 25 °C (lines), whose parameters listed in Table B.1.

perceived benefit of this method is that each model parameter can be varied independently of one another; although, this can result in non-physical values being determined when performing global optimisation. Other downsides are the inflexibility for the user, the need for duplicate models and additional characterisation steps. In contrast, SPICE facilitates temperature variation by scaling pertinent model parameters based on deviation from the nominal temperature, T_n, at which they were specified; accordingly, the equations used to achieve this must be written in terms of these variables.

The remainder of this chapter is concerned with developing a set of appropriate equations and techniques to accurately account for material and device specific temperature effects observed in the SiC JFETs under study. Appropriate values in each case are presented in Table B.1. Modified values may arguably be used for IC resistors formed monolithically with the JFETs which utilise the channel epilayer.

Open-Channel Conductance

The product of n and $\mu_{e,0}$ in the channel region determines the temperature dependence of G_0*. At high temperatures, where phonon scattering dominates in non-degenerate samples, a simple power law is usually sufficient to describe the variation of $\mu_{e,0}$ [36]. This method is adopted in many SPICE models due to its computational efficiency, including the JFET primitive. A single power law dependence is, however, unsuitable for the wide temperature range of interest due to the varying significance of the different scattering mechanisms de-

*While the channel volume will change due to thermal expansion the variables Z, a and L the amount will be small and have a negligible effect on the calculation.

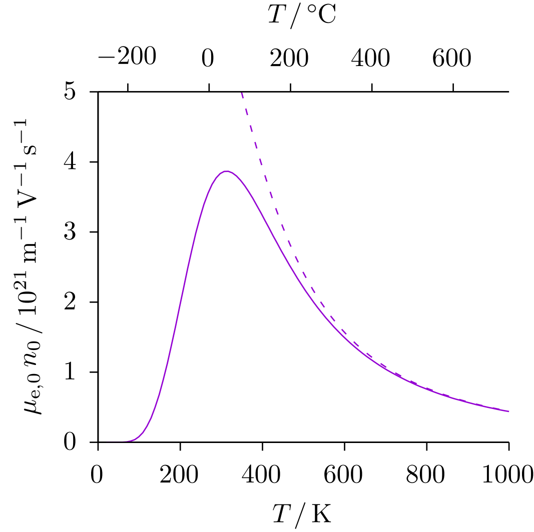


Figure 4.26

Open-channel conductance thermal models: SPICE power law model (dashed line) and twin power law model with incomplete ionisation (solid line), given $N_\mathrm{d} = 10^{17}\,\mathrm{cm}^{-3}$, $T_\mathrm{n} = 300\,\mathrm{K}$, $\mu_{\mathrm{e},0}(T_\mathrm{n}) = 6 \times 10^{-2}\,\mathrm{m}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, $\alpha = -2.5$, $\beta = 2.5$ and $M = 0.5$.

picted in Figure 2.9a. A two part power law model has been found suitable for bulk SiC devices which avoids the complex calculations of Equation 3.68 [58, 157]. Incomplete ionisation of donors in SiC also has a noticeable effect in the temperature range of interest, as exemplified by Figure 3.3a. Combining both effects the relative change in G_0 can be expressed as

$$G_0(T) = G_0(T_\mathrm{n}) \frac{n(T)}{n(T_\mathrm{n})} \frac{(1+M)(T/T_\mathrm{n})^\alpha}{1 + M(T/T_\mathrm{n})^{\alpha-\beta}}, \tag{4.32}$$

where $\alpha < 0$, $\beta > 0$ and $M = \mu_1(T_\mathrm{n})/\mu_2(T_\mathrm{n})$ are a fitting parameter and $n(T)$ and $n(T_\mathrm{n})$ are calculated numerically for a set of donor and acceptor concentrations, N_d and N_a, respectively, using the computationally efficient methods developed in §3.8.

The dashed and solid lines in Figure 4.26 illustrate the standard SPICE model and the proposed model, respectively. Unlike the SPICE primitive JFET model, the proposed model is able to accurately predict G_0 across a wide temperature range in a manner appropriate for SiC.

Built-in Potentials

A general method for determining ϕ_0 in a step junction is to find the distance between the equilibrium Fermi levels on each side of the junction,

$$\phi_0 = e(E_\mathrm{F,n} - E_\mathrm{F,p}). \tag{4.33}$$

The standard approach adopted by SPICE relies on the assumptions of complete ionisation, standard bands and that both regions are non-degenerate. While this model can be modified to adequately account for the first two points, the predictions become less accurate the more

the law of mass action is violated. A computationally efficient method for determining $E_{F,n}$ and $E_{F,p}$ that satisfies Equation 4.33 was proposed in §3.8 and is the approach adopted here; however, a modified version of the closed form expression used by SPICE does have the benefit of identifying the salient factors contributing the the variation and as such is briefly discussed.

Extending the SPICE model to account for incomplete ionisation, the SiC band structure and doping induced band gap variation [12, 144],

$$\phi_{0,t}(T) = \phi_T(T) \ln\left[\frac{p_{p0}(T)n_{n0}(T)}{n_{i,p}(T)n_{i,n}(T)}\right] \tag{4.34a}$$

$$= \phi_T(T)\left\{\ln\left[\frac{p_{p0}(T_n)n_{n0}(T_n)}{n_{i,p}(T_n)n_{i,n}(T_n)}\right] + \ln\left[\frac{p_{p0}(T)n_{n0}(T)}{n_{i,p}(T)n_{i,n}(T)}\frac{n_{i,p}(T_n)n_{i,n}(T_n)}{p_{p0}(T_n)n_{n0}(T_n)}\right]\right\} \tag{4.34b}$$

$$= \phi_0(T_n)\left(\frac{T}{T_n}\right) - \phi_T(T)\ln\left[\frac{n_{i,p}(T)}{n_{i,p}(T_n)}\frac{n_{i,n}(T)}{n_{i,n}(T_n)}\right] + \phi_T(T)\ln\left[\frac{p_{p0}(T)}{p_{p0}(T_n)}\frac{n_{n0}(T)}{n_{n0}(T_n)}\right] \tag{4.34c}$$

which after substituting in Equation 3.56c provides

$$= \phi_0(T_n)\left(\frac{T}{T_n}\right) - 3\phi_T(T)\ln\left(\frac{m^d(T)}{m^d(T_n)}\frac{T}{T_n}\right) - \phi_g(T_n)\left(\frac{T}{T_n}\right) + \phi_g(T)\cdots$$

$$\cdots + \phi_T(T)\ln\left[\frac{p_{p0}(T)}{p_{p0}(T_n)}\frac{n_{n0}(T)}{n_{n0}(T_n)}\right], \tag{4.34d}$$

where $n_{i,n}$ and $n_{i,p}$ are the intrinsic carrier concentrations in the n- and p-type regions and $\phi_g = \frac{1}{2}(\phi_{g,p} + \phi_{g,n})$ is the arithmetic mean band gap voltage calculated from the self-consistently determined band gap voltages, $\phi_{g,n}$ and $\phi_{g,p}$, in the n- and p-type regions, respectively, $m^d = \left(m_e^d m_h^d\right)^{1/2}$ is the arithmetic mean density of states effective mass determined from the electron and hole density of states effective masses, m_e^d and m_h^d, respectively.

Equation 4.34c differs from that used by SPICE in three areas. The first is the inclusion of the thermal density of states effective mass ratio, the second is the implicit inclusion of doping induced band gap narrowing and the third is the logarithmically varying ratio of free carrier concentrations. In the case of a non-degeneracy being considered here the third and fourth arithmetic terms in Equation 4.34c will over balance the first to provide a significant portion of the reduction in ϕ_0 at low to moderate temperatures. Importantly, if the determined value for $\phi_g(T_n)$ is incongruent with $\phi_0(T_n)$ the model becomes erratic and unusable, thereby affirming the importance of doping on calculating ϕ_g. The second term in Equation 4.34c has only a small influence at low temperature but becomes more important at high temperatures, enhanced by the influence of high energy bands and non-parabolicity expressed through the temperature dependence of m_e^d and m_h^d in Equation 3.51 and Equation 3.55, respectively. The last term is important across the entire temperature range and provides comparable influence as the other factors, thereby warranting its inclusion.

As the method by which the free carrier concentrations are calculated rely on the knowledge of $E_{F,p}$ and $E_{F,n}$ Equation 4.33 is a more suitable option than Equation 4.34. The alternative method proposed here solves Equation 4.33 numerically using the intermediate

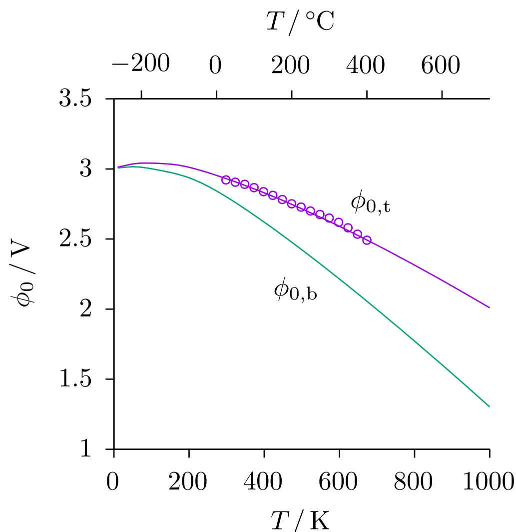


Figure 4.27

Experimental (points) and simulated (lines) p-n junction built-in potentials for top and bottom gates, $\phi_{0,\mathrm{t}}$ and $\phi_{0,\mathrm{b}}$, respectively, as a function of absolute temperature. Simulated values were achieved through by numerically solving a simplified charge neutrality equation using the Newton-Raphson method, assuming nominal doping concentrations and zero compensation.

values obtain during the calculation of the dopant ionisations using the NR method. The simulated results are presented in Figure 4.27 for both $\phi_{0,\mathrm{t}}$ and $\phi_{0,\mathrm{b}}$ assuming nominal doping concentrations and zero compensation.

Capacitance-voltage (CV) measurements performed on a lateral diode structure [17,126] provide validation of the contact potential model. Figure 4.28a presents a CV characteristic of the diode structure at room temperature. Under the condition of channel homogeneity, the quantity $\phi_{0,\mathrm{t}} - 2\phi_{\mathrm{T}}$ can be deduced from the root of a linear fit line applied to C^{-2} vs. V data, as illustrated in Figure 4.28b [12]. The depletion region quickly encloses the epilayer with increasing reverse bias, causing the the narrow channel contributing a significant series resistance close to pinch-off. The minima seen around $-3.5\,\mathrm{V}$ is a consequence of this and these artificial values in Figure 4.28b are correctly ignored [126]. Accordingly, it was determined that $\phi_{0,\mathrm{t}} = 2.92(1)\,\mathrm{V}$ which is in excellent agreement with theory. The results of this experimental analysis are presented by points in Figure 4.27 and show excellent agreement with the theoretical model.

The slope can also be used to deduce the effective channel doping concentration

$$N_{\mathrm{d,t}} = -\frac{2}{e\varepsilon_{\mathrm{s}}}\left(\frac{\mathrm{d}C_{\mathrm{j}}^{-2}}{\mathrm{d}V}\right)^{-1} \tag{4.35a}$$

which given a uniformly doped gate epilayer of concentration N_{a} suggests

$$N_{\mathrm{d}} = \frac{\sqrt{4N_{\mathrm{a}}N_{\mathrm{d,t}} + N_{\mathrm{a}}^2} - N_{\mathrm{a}}}{2}. \tag{4.35b}$$

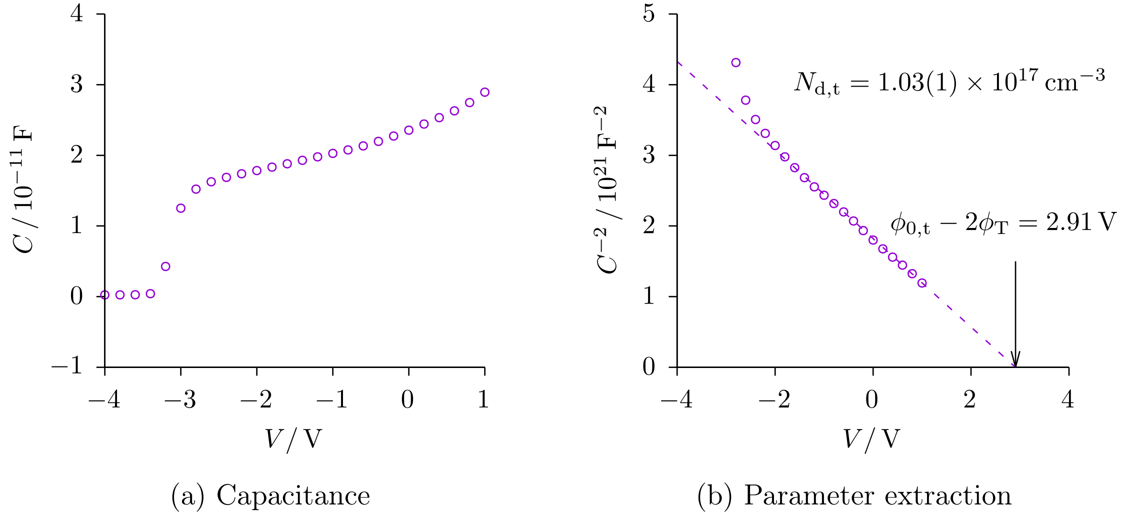


Figure 4.28

Room temperature capacitance-voltage measurements for a lateral 4H–SiC step p^{+}-n junction diode with cross sectional area $4.59 \times 10^{-4}\,\mathrm{cm}^2$. Experimentally extracted values for the contact potential and effective channel doping concentration, as determined from the root and slope of the linear fit of the inverse squared capacitance against voltage measurements, respectively, are included.

Accounting for the manufacturer specified uncertainty in N_{a} it was determined that $N_{\mathrm{d}} = 1.03(2) \times 10^{17}\,\mathrm{cm}^{-3}$ which is very close to the quoted nominal value of $1 \times 10^{17}\,\mathrm{cm}^{-3}$.

Pinch-off Voltages

Both $\phi_{\mathrm{p,t}}$ and $\phi_{\mathrm{p,b}}$ will vary with temperature predominantly on account of variation in the semiconductor permittivity, ε_{s}. Published work suggests that ε_{s} will increase with temperature in 4H–SiC in the temperature range of interest [158, 159]. The relative change in $\phi_{\mathrm{p,t}}$ and $\phi_{\mathrm{p,b}}$ may be attained experimentally by applying Equation 4.35a to a one-sided abrupt junction diode at different temperatures. As $\phi_{\mathrm{p,t}}$ and $\phi_{\mathrm{p,b}}$ are both inversely proportional to ε_{s},

$$\frac{\phi_{\mathrm{p,t}}(T)}{\phi_{\mathrm{p,t}}(T_{\mathrm{n}})} = \frac{\phi_{\mathrm{p,b}}(T)}{\phi_{\mathrm{p,b}}(T_{\mathrm{n}})} = \frac{(\mathrm{d}C^{-2}/\mathrm{d}V)(T)}{(\mathrm{d}C^{-2}/\mathrm{d}V)(T_{\mathrm{n}})} \approx \frac{\varepsilon_{\mathrm{s}}(T_{\mathrm{n}})}{\varepsilon_{\mathrm{s}}(T)}, \tag{4.36}$$

suggesting they should share a temperature coefficient. The true variation of ε_{s} will depend on thermal expansion and will be influenced by ionisation; however, the small variation observed, as presented in Figure 4.29, can be adequately modelled using a first order polynomial fit to experimental data given by the equation

$$\phi_{\mathrm{p}}(T) = \phi_{\mathrm{p}}(0) + \phi_{\mathrm{p}}(T_{\mathrm{n}})mT = \phi_{\mathrm{p}}(T_{\mathrm{n}})\left[1 + m(T - T_{\mathrm{n}})\right]. \tag{4.37}$$

The later form is concordant with the linear SPICE temperature model, wherein the temperature independent temperature coefficient is identified as the gradient of the line, m.

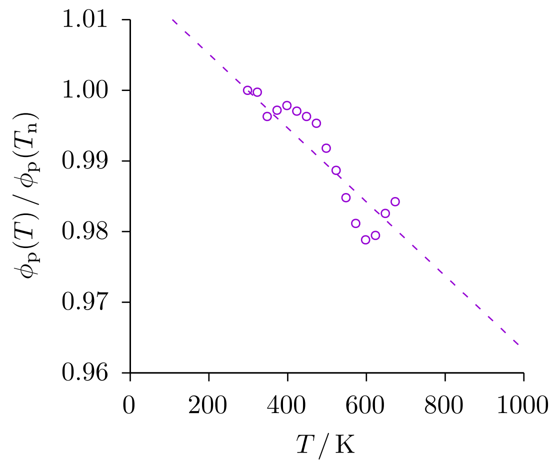


Figure 4.29
Relative change in measured pinch-off voltages with temperature, determined from the slopes of linear fits to experimental inverse squared capacitance against voltage measurements for a lateral 4H–SiC p^+-n junction. The dashed line represents a linear fit to the experimental data.

Mobility-degradation

In the chosen velocity saturation model $v_{sat} = \mu_{e,0}\mathscr{E}_c = \mu_{e,0}(L\Xi)^{-1}$ and it may be expected that a reduction in $v_{d,sat}$ would require an increase in Ξ. Closer observation of the published experimental data of Khan *et al.* presented in Figure 2.10 reveals that at higher temperatures the field required to cause noticeable deviation from the constant mobility approximation increases with temperature [59]. As the devices under study experience only moderate fields the model being used is satisfied by a decrease in Ξ that can be appropriately modelled by a power law model as

$$\Xi(T) = \Xi(T_n)\left(\frac{T}{T_n}\right)^{\alpha}, \quad \alpha < 0. \tag{4.38}$$

where α is a fitting parameter.

Channel-length Modulation

The default SPICE model takes no account of the temperature dependence of λ; however, first-order polynomial models for λ [74], γ and χ, similar in form to Equation 4.37, were found to improve agreement over the extended temperature range of interest.

Saturation Current

The ideal diode model makes several assumptions [144] although these are suitably valid for modelling gate-channel and body-channel leakage currents. Despite the large difference in

doping concentration between the gate and epilayers, due to the low degree of ionisation for Al acceptors in the gate epilayer, both electron and hole diffusion currents will both contribute noticeably to current density flowing across the gate-channel junction

$$J_{\mathrm{s}} = J_{\mathrm{s,n}} + J_{\mathrm{s,p}} = \left[\frac{eD_{\mathrm{n}}n_{\mathrm{I,p}}^2}{L_{\mathrm{n}}p_{\mathrm{p0}}} + \frac{eD_{\mathrm{p}}n_{\mathrm{i,n}}^2}{L_{\mathrm{p}}n_{\mathrm{n0}}}\right]\left(\mathrm{e}^{\frac{eV}{k_{\mathrm{B}}T}} - 1\right). \tag{4.39a}$$

The hole current injected from the gate will, however, be the larger of the two for the doping concentrations of interest here. Also, the slight difference in band gaps in the two epilayers due to band gap narrowing causes the junction to behave similarly to an ideal anisotype heterojunction, introducing an additional exponential dependence to the ratio of current components such that [9, 12]

$$\frac{J_{\mathrm{s,n}}}{J_{\mathrm{s,p}}} \approx \frac{n_{\mathrm{n0}}}{p_{\mathrm{p0}}}\mathrm{e}^{-\Delta\phi_{\mathrm{g}}}. \tag{4.39b}$$

Although Equation 4.39a has a number of temperature dependent terms, the intrinsic carrier concentration tends to dominate, more so as the ionisation fractions approach unity [12].

The default SPICE thermal model for describing the reverse saturation current in a p-n junction is given by [144]

$$I_{\mathrm{s}}(T) = I_{\mathrm{s}}(T_{\mathrm{n}})\left(\frac{T}{T_{\mathrm{n}}}\right)^{\mathrm{XTI/N}} \mathrm{e}^{\frac{\phi_{\mathrm{g}}}{\mathrm{N}k_{\mathrm{B}}}(T_{\mathrm{n}}^{-1} - T^{-1})}, \tag{4.40}$$

where XTI and N are fitting parameters. It is not entirely suitable for 4H-SiC devices due to the untenable assumptions of complete ionisation, non-degeneracy and single carrier type. A improved model is given by

$$I_{\mathrm{s}}(T) = I_{\mathrm{s}}(T_{\mathrm{n}})\frac{n_{\mathrm{i,n}}^2(T)\,n_{\mathrm{n}}^{-1}(T) + \alpha\, n_{\mathrm{I,p}}^2(T)\,p_{\mathrm{p}}^{-1}(T)}{n_{\mathrm{i,n}}^2(T_{\mathrm{n}})\,n_{\mathrm{n}}^{-1}(T_{\mathrm{n}}) + \alpha\, n_{\mathrm{I,p}}^2(T_{\mathrm{n}})\,p_{\mathrm{p}}^{-1}(T_{\mathrm{n}})}, \tag{4.41}$$

where $n_{\mathrm{I,p}}$ the the effective intrinsic carrier concentration in the gate epilayer and $\alpha = (D_{\mathrm{n}}L_{\mathrm{p}})/(D_{\mathrm{p}}L_{\mathrm{n}})$, provides and additional weighting factor.

Series Resistance

In SPICE the temperature dependence of the series resistances are modelled as first order polynomials, whose parameters have units of $^{\circ}\mathrm{C}^{-1}$ [144]. This provides a suitable arrangement for the contact resistances and is also adopted in the proposed thermal model. It should be noted that the gate and body series resistances will typically be much smaller than the resistance of the p-n junctions, provided they are biased at less than 2 V, and so accurate values are not critical.

The temperature dependence of the additional channel series resistances, formed by the non-implanted non-self alignment regions, will be strongly temperature dependent. It's variation will, however, be implicitly included through the thermal models for the open-channel conductance and the bottom gate pinch-off and contact voltages used in its calculation. The

use of relative lengths also accounts for the change in channel volume due to thermal expansion. As such no additional model parameters are required for these regions. This has the additional benefit of providing appropriate parameter constraint during optimisation.

Capacitance

The zero bias capacitance used in both the SPICE diode model and the modified Statz model can be suitably scaled using the existing SPICE thermal model

$$C_{j0}(T) = C_{j0}(T_n) \left[1 + \alpha m (T - T_n) + m \left(1 - \frac{\phi_0(T)}{\phi_0(T_n)} \right) \right], \tag{4.42}$$

where the grading coefficient, m, equals 0.5 for homogenous epilayers and α is an additional fitting parameter. Its variation is only moderate as exemplified by Figure 4.30, showing experimental C_{gs} at different values of V_{GS} at 25 °C and 400 °C.

The variation the the slope of the data around the turn-off points suggest that when the modified Statz capacitance model is used the values of Δ_1 and Δ_2 should be made temperature dependent. At the time of writing this feature is not currently implemented.

4.5 Summary

NLDM JFETs with gate lengths of 9 µm and gate widths of 250 µm have been realised using a commercial n-type 4H–SiC wafer with three layers of homo epitaxy and conventional planer processing techniques. The fabricated device displayed excellent long channel device characteristics with turn-off voltages and current densities consistent with bulk semiconductor theory. The output resistance in saturation showed strong non-linear channel and gate voltage dependence. Such characteristics are not accounted for the in the primitive SPICE

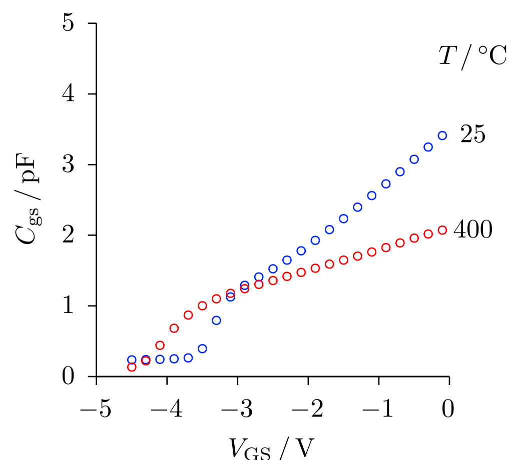


Figure 4.30

Experimental JFET gate-source capacitance, C_{gs}, as a function of gate-source bias, V_{GS} at 25 °C and 400 °C, using a measurement frequency of 100 kHz. Drain and body terminals were guarded (set to AC ground).

JFET compact model. The intrinsic voltage gain within the typical region of operation was determined as roughly 100. Non-ideal p-n junction leakage currents in forward and reverse bias were also identified and attributed to high field regions in the vicinity of defect agglomerations. The gate-channel reverse bias current was found to increase exponentially with temperature reaching a few nano amps at 400 °C under typical operating conditions. Operation at 400 °C was found to limit device operation for forward bias gate-source voltages of less than 2 V.

Annealed Ni/Ti contacts on $2 \times 10^{19}\,\mathrm{cm}^{-3}$ doped N implanted layers provided sufficiently low contact resistance to the channel epilayer. Horizontal current flow through the contact side wall and the difference in sheet resistance under the contact were found to increase the determined value of the specific contact resistance determined from TLM test structures by as much as 10%. The lowest recorded value of specific contact resistance was $1.90(50) \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ with a corresponding sheet resistance of $7.89(9) \times 10^2\,\Omega/\square$. Inhomogeneity in sheet resistance and specific contact resistance was attributed to known processes variations that could be mitigated for large scale production.

Stacked annealed Al/Ti contacts on the $2 \times 10^{19}\,\mathrm{cm}^{-3}$ Al doped epilayer provided an typical room temperature specific contact resistance of $42(4)\,\mathrm{m}\Omega\,\mathrm{cm}^2$ and exhibited a strong thermionic emission component. While the contact resistances were relatively large at low temperature, the low leakage current under normal operation resulted in a negligible effect on device operation.

An accurate compact model has been developed in the framework of the GCA that is suitable for describing the electronic characteristics of the NLDM JFETs under study. Notable features include electric field dependent mobility, asymmetric twin gate operation and SiC specific thermal models. Efficient empirical corrections to the GCA near to and above pinch-off capable of providing close agreement with experiment were presented. A two part power law mobility model in combination with the efficient donor ionisation model presented in §3 was successful in modelling the resistivity of the channel epilayer between 25 °C and 400 °C using a minimal number of parameters. The gate-channel contact potential was experimentally determined between 25 °C and 400 °C and found to agree closely with the proposed theoretical model. A small but finite reduction in relative permittivity of 4H–SiC with temperature of about 2 % was simultaneously observed. The proposed compact model was implemented in Synopsys HSPICE wherein a modified LMA was used to optimise the model parameters against experimental data between 25 °C and 400 °C. Comparisons with experimental results demonstrate excellent agreement for a wide range of gate, body and channel biasing and temperatures.

CHAPTER

5

Integrated Circuits

5.1 Introduction

An integrated circuit (IC) is a collection of electronic circuits formed on a small piece of semiconductor. The resulting reduction of interface parasitics and the inherent consistency between devices formed in close proximity provide crucial performance advantages over circuits constructed from discrete components. The reduced dimensions and the ready means of simultaneous fabrication provide further practical and economic benefits [17].

A number of constraints are unfortunately imposed on the analogue IC designer. Large value coupling capacitors, for example, are not practically realisable and consequently direct coupling between amplifier stages is demanded. The temperature dependence of output bias voltages are therefore of significant importance in amplifier designs. Connections to shared regions of semiconductor can also undesirably alter device characteristics based on their position in the circuit and can be highly process and temperature sensitive. The fabrication process also restricts the type and behaviour of devices that can be implemented together, thereby limiting the scope of usable circuit topologies.

A number of difficulties also arise during development. A major inconvenience is that signals within ICs are impractical to measure, with current measurements proving to be extremely difficult. Importantly, circuit modification at the IC level require new photomask designs and repeat fabrication in-between testing which is costly and can take many months to complete.

Computer simulations provide a cost effective and time efficient method for validating a circuit topology prior to fabrication. Simulation Program with Integrated Circuit Emphasis (SPICE), originally developed in the early seventies* at University California at Berkley by Professor D. O. Pederson and his students, is the *de facto* class of electronic design automation (EDA) software employed for this task [144]. Its strength lies in applying suitably accurate device models in order to validate hand designed circuits [145]. The more detailed analysis can additionaly be used for efficient circuit optimisation of component values and model parameters based on experimental data. As with most EDA based software, however, SPICE is concordant with the adage '*garbage in, garbage out*'.

*During this time programmes were stored on punch cards and even now the archaic terms *deck* and *card* are still used to denote a netlist file and statement, respectively.

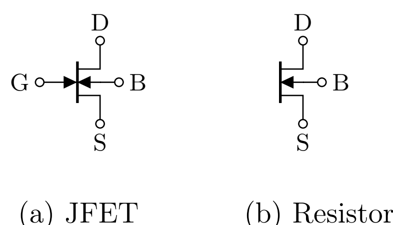
The functionality and versatility of operational amplifiers (op-amps) make them an extremely desirable component for use in various kinds of high performance circuits. Utilising the accurate IC compatible junction field effect transistor (JFET) compact model developed in §4 this chapter outlines a design for a stable monolithic 4H–SiC high temperature op-amp. The discussion is broken into three parts, specifically common source (CS) amplifiers, differential amplifiers and voltage buffers with and without direct current (DC) level shifting. Techniques for achieving stable operation across a wide temperature range are identified. Particular attention is given to influence of the body-effect on voltage gain and operating point (OP) stability.

In the remainder of this chapter the standard convention used for symbolising voltages and currents has been adopted. An instantaneous value is denoted by a lower case letter, v and i, respectively, with upper case subscripts and represents the sum of a DC bias value, denoted by a corresponding uppercase letter and subscripts, and an alternating current (AC) signal, represented by a lowercase letter and subscripts; e.g., the instantaneous voltage between the gate and source terminals of a JFET, v_{GS}, is the sum of the bias voltage, V_{GS} and signal voltage, v_{gs} [88].

5.2 Devices

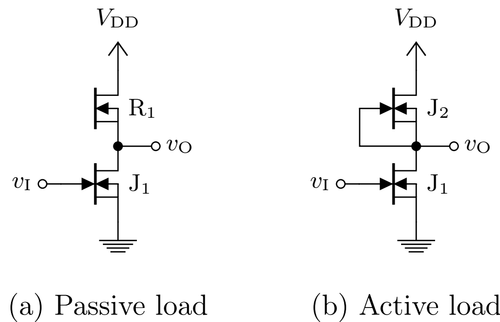
The adopted component symbols for the IC n-channel lateral depletion-mode (NLDM) JFET and resistor used in the circuit schematics throughout the remainder of this chapter are depicted in Figure 5.1. The drain, gate, source and body terminals denoted by the letters D, G, S, and B, respectively. The IC resistor differs from the JFET only in the omission of the top gate and the channel geometry and therefore related parameter sets based on fits to experimental data of a 9 µm by 250 µm JFET were adopted for the simulations. All length and width scaling is performed relative to these values with dependent parameters updated accordingly.

It is important to note that transistors and resistors sharing a common buffer epilayer without electrical isolation have a common body potential that must be chosen to ensure the channel-body junction of all devices remain reverse biased [145]. This value is limited both by supply availability and the apparent voltage dependence of the reverse bias leakage current.



(a) JFET (b) Resistor

Figure 5.1
N-channel integrated circuit component symbols. Drain, gate, source and body terminals are denoted by D, G, S and B, respectively.



(a) Passive load (b) Active load

Figure 5.2

Single-supply JFET common-source amplifier with (a) passive and (b) active load configuration, with body-source voltage fixed at 0 V.

5.3 Common-Source Amplifier and the Body Effect

An instantaneous input voltage, v_I, applied to the gate of a JFET will modulate the current through its channel*. This effect is quantified for small changes by the transistor's transconductance, g_m. It was shown in §4.4.4 that this value depends strongly on the biasing conditions and will in general be limited by power dissipation, supply voltage availability and the ability to maintain a high impedance gate-channel junction [161].

Passing the resulting current through a resistance attached between the JFET's drain terminal and a positive DC supply voltage, V_{DD}, as illustrated in Figure 5.2a†, produces a corresponding instantaneous output voltage, v_O. This arrangement describes the CS amplifier configuration‡. The choice of resistance is important for achieving adequate voltage gain,

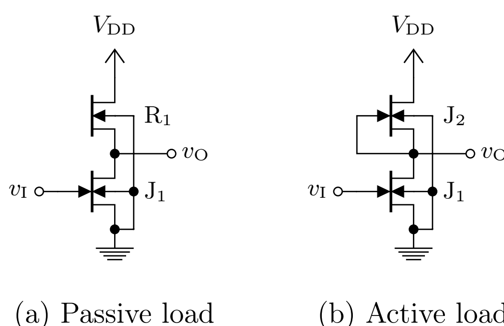
$$A_v = \frac{dv_O}{dv_I} = \lim_{v_i \to 0} \frac{v_o}{v_i} \tag{5.1}$$

whilst establishing a suitable OP. A resistor, when used for the task of current-to-voltage conversion, is referred to as a *passive* load. Ohm's law suggests a high value should be used to maximise the change in output voltage; however, finite supply voltages and the need to maintain an appropriate OP limit the range of suitable values in any given design. Specifically, the resistor's static resistance must allow the JFET to remain in saturation ($v_{DS} > v_{DS,sat}$) in addition to providing sufficient output signal swing. A second depletion mode (DM) JFET can replace the resistor, as illustrated in Figure 5.2b, and is appropriately referred to as an *active* load. A major benefit is that if biased in saturation its dynamic resistance, important for small-signal analysis, can be much larger than the static resistance which is important for establishing the DC OP. One distinct consequence of using active loads, however, is the introduction of an additional voltage burden with the undesirable effect of reducing the positive output voltage swing.

*Despite the relatively large ionisation energies for Al and N dopants, the quasi-static approximation for the depletion width has been found experimentally to be a suitable for SiC for frequencies up to several hundred MHz [160].

†The convention of using arrowheads to denote DC supplies has been adopted [90].

‡The source terminal appears as a signal ground to both input and output signals.



(a) Passive load (b) Active load

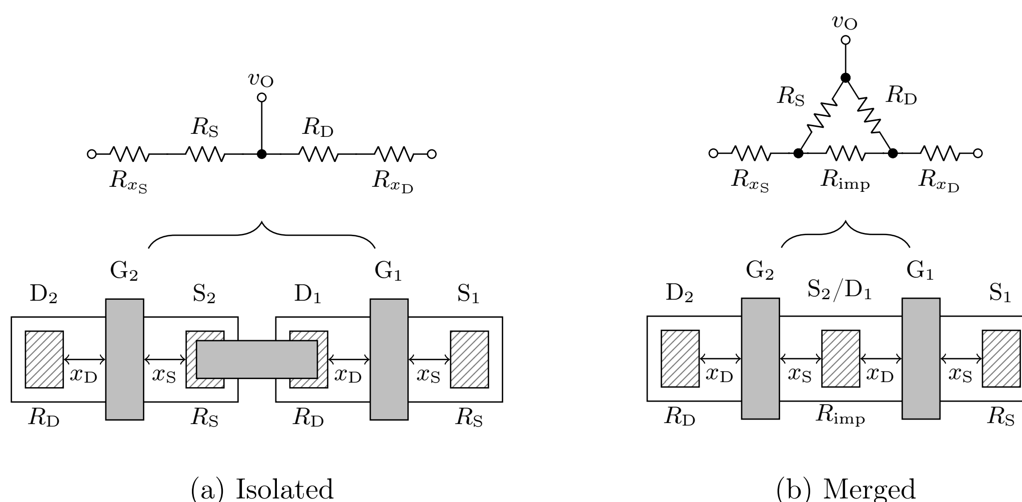
Figure 5.3

Single-supply JFET common-source amplifier with (a) passive and (b) active load configuration, for body coupled devices.

When an electrically common body epilayer is adopted the configurations in Figure 5.2 must be changed to those in Figure 5.3. The single consequence of this change is that a finite body-source voltage, v_{BS}, is introduced to the load transistor and is equal to the negative of the output voltage. The detrimental influence of this change on the OP stability and voltage gain will be discussed in detail.

It is necessary to first discuss the methods and consequences for establishing connections between devices. All resistor and JFET channels are fabricated from the same epilayer and thus connections can be performed in one of two ways, as illustrated in Figure 5.4 for a pair of drain-source-coupled JFETs. An equivalent circuit for each configuration between the active channel edges is included, wherein R_D and R_S denote drain and source contact resistances, respectively, while R_{x_D} and R_{x_S} denote the resistance of the non-self alignment regions at the drain and source end of an active device channel, respectively.

In Figure 5.4a each device channel is electrically isolated and an interconnect is placed between the contacts of the adjacent devices. The resistance and temperature dependence



(a) Isolated (b) Merged

Figure 5.4

Interconnect configurations and equivalent circuits for drain-source coupled JFETs.

of the interconnecting metal should be negligible in comparison and is omitted from the equivalent circuit model. Directly connecting the device channels will remove the voltage burden of R_{D} and R_{S}; however, if a voltage sensing contact is placed between the devices, as in Figure 5.4b, an additional resistance, R_{imp}, is introduced on account of the resistivity of the implanted region under it. Assuming that the input impedance for all of the devices sensing v_{O} remain large and the transfer length for current flow into the contact is much smaller than the contact length this will appear in parallel with the series combination of R_{D} and R_{S}. In Figures 5.2b and 5.3b the effective resistance appears in the voltage feedback path of the load transistor, J_2. As the combined temperature dependence differs from that of R_{S} alone a disparity between the source degradation of the two transistors is created and will thereby constitute a drift of bias voltage, V_{O}, in response to a change in temperature. To circumvent this the arrangement in Figure 5.4a is adopted in the following simulations.

Goal based optimisation of the load device was performed at 400 °C for each circuit in Figure 5.2 and Figure 5.3 with the intent of maximising the open-circuit voltage gain, A_{vo}, while simultaneously maintaining sufficient large-signal swing. The values were subsequently used to calculate A_{vo} and V_{O} as a function of temperature, T, between 25 °C at 400 °C. The results of the SPICE simulations for each circuit in Figure 5.2 and Figure 5.3 are presented in Figure 5.5 by dashed and solid lines, respectively. Low-frequency* large-signal voltage transfer characteristics (VTCs) at 25 °C and 400 °C, denoted by blue and red lines, respectively, are included to illustrate the input and output signal ranges and linearity at the temperature extremes.

For the circuit in Figure 5.2a the appropriate open-channel resistance for R_1 was determined to be approximately 2 kΩ, providing a maximum value of $|A_{\mathrm{vo}}|$ of around 3.10† at 400 °C with a minimum of 2.86 at about 70 °C. Slightly higher values were achievable by using of larger values for R_1 but came at the expense of compromising the negative output voltage swing.

Following the bias point calculations, large-signal equivalent circuits can be replaced with their representative small-signal equivalent circuit. Linear element values‡ are subsequently used within an incremental linear model where standard frequency domain analysis techniques can be applied [144, 145]. The low values of $|A_{\mathrm{vo}}|$ for the CS amplifier with passive load can be understood from the familiar small-signal expression§

$$A_{\mathrm{vo}} = -g_{\mathrm{m,1}}(r_{\mathrm{o,1}} \parallel r_{\mathrm{o,2}}) \approx -g_{\mathrm{m,1}} r_{\mathrm{o,2}}, \tag{5.2}$$

where $g_{\mathrm{m,1}}$ represents the transconductance of the JFET, $r_{\mathrm{o,1}}$ the output resistance of the JFET and $r_{\mathrm{o,2}}$ the output resistance of the load resistor.

A benefit of using on chip resistors is that their resistivity follows the same temperature dependence of a JFET channel. This has been previously exploited in similar fixed biased CS SiC JFET amplifiers to provide a relatively stable low-frequency voltage gain for tem-

*During DC analysis all physical and equivalent circuit capacitors are removed from the circuit [144].

†The output signal is 180° out of phase with the input, thereby providing a negative voltage gain.

‡The linearisation of the non-linear functions is achieved via a first order truncated Taylor series expansion about the OP.

§The total of the resistors in parallel is the reciprocal of the sum of the reciprocals.

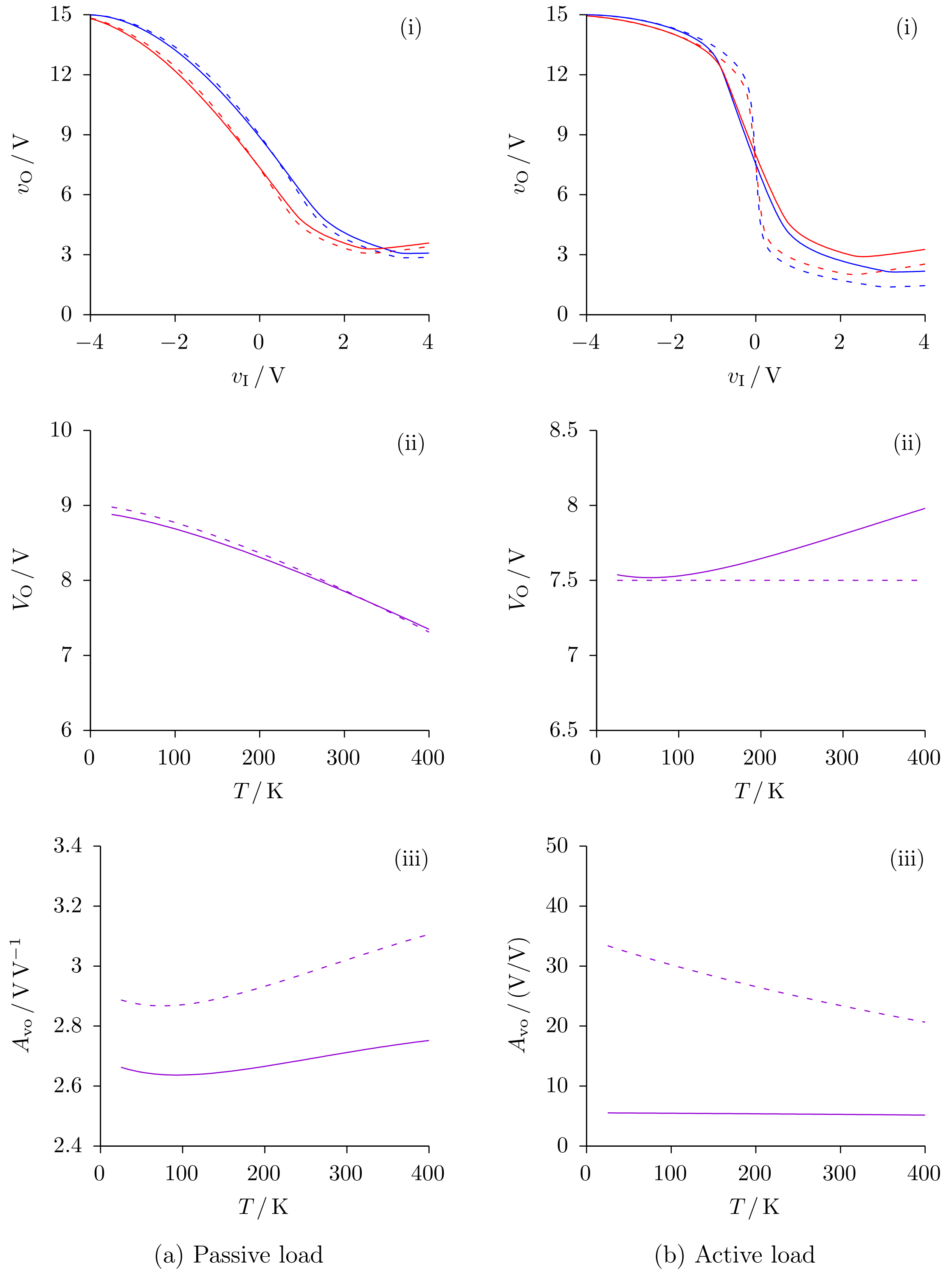
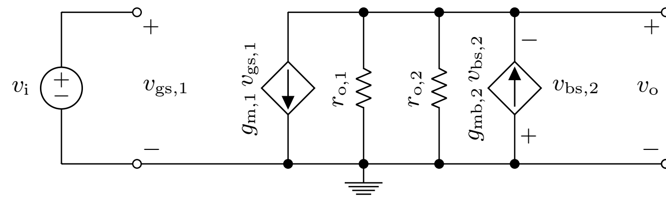
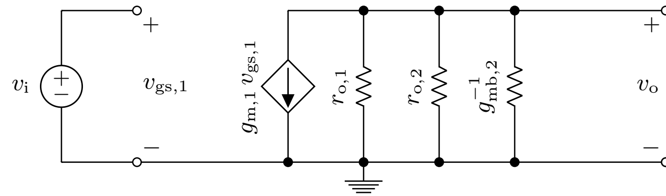


Figure 5.5

(i) Voltage transfer characteristics at 25 °C (blue) and 400 °C (red), (ii) DC output voltage, V_O, for $V_I = 0$ V and (iii) low-frequency open-circuit voltage gain, A_{vo} for the (a) passive and (b) active common-source amplifier configurations in Figure 5.2 (dashed lines) and Figure 5.3 (solid lines).



(a) before source absorption



(b) after source absorption

Figure 5.6

Small-signal model for the circuits in Figures 5.3a and 5.3b (a) before and (b) after applying the source absorption theorem.

peratures between 25 °C and 500 °C [4,84]. The reason this consistency is that $r_{o,2}$ increases with temperature at approximately the same rate that the transistors g_m decreases. The reported values of gain are comparable to the present simulations which is to be expected based on the similarity of the device structures.

The amplification of AC signals demands that the OP of each amplifier stage maintains sufficient signal swing*. Direct-coupled amplifiers are more challenging and require that the output bias voltage remains independent of temperature. While the gain of the passive loaded CS amplifier was found to remain relatively stable the output is seen to undesirably deviate by almost 1.7 V between 25 °C and 400 °C.

IC resistors on a shared region of semiconductor are subject to the body-effect. Considering the fixed bias CS amplifier with passive load in Figure 5.3a, the resistor will again operate analogous to a three terminal JFET, however, in this case with its gate tied to ground [90]. While the body-source voltage, v_{BS}, of J_1 remains zero the v_{BS} of R_1 will equal $-v_O$, resulting in a continuous altering of the OP in response to input signal, v_i [145].

The low-frequency small-signal equivalent model for Figure 5.3a is given in Figure 5.6a wherein subscripts 1 and 2 relate to J_1 and R_1, respectively. A signal voltage $v_{bs,2}$ is present which results in an additional change in drain current $g_{mb,2}\, v_{bs,2}$, where $g_{mb,2}$ is the body-transconductance of the load [90]. The source absorption theorem states that during small-signal analysis a voltage controlled current source, whose control voltage appears across its terminals, can be replaced by an equivalent impedance, $g_{mb,2}^{-1}$, as in Figure 5.32 [90]. From

*Linear amplification, devoid of distortion, requires also that the variation of the output voltage be linear.

Figure 5.6b expressions for the output and input signals can be identified as Figure 5.6b.

$$v_\mathrm{o} = -g_{\mathrm{m},1} v_{\mathrm{gs},1} \left(g_{\mathrm{mb},2}^{-1} \parallel r_{\mathrm{o},1} \parallel r_{\mathrm{o},2} \right) \tag{5.3a}$$

and

$$v_\mathrm{i} = v_{\mathrm{gs},1}, \tag{5.3b}$$

respectively, producing a small-signal open-circuit voltage gain of

$$A_\mathrm{vo} = \frac{v_\mathrm{o}}{v_\mathrm{i}} \tag{5.3c}$$

$$= -\, g_{\mathrm{m},1} \left(g_{\mathrm{mb},2}^{-1} \parallel r_{\mathrm{o},1} \parallel r_{\mathrm{o},2} \right) \tag{5.3d}$$

$$= -\, \frac{g_{\mathrm{m},1}}{g_{\mathrm{mb},2} + r_{\mathrm{o},1}^{-1} + r_{\mathrm{o},2}^{-1}} \tag{5.3e}$$

As a consequence of the body-effect the optimised value for the open channel resistance for $\mathrm{R_1}$ was recalculated as the lower value of $1.70\,\mathrm{k\Omega}$. This can be understood to result from the additional encroachment of the body-channel depletion region, $W_{\mathrm{n,b}}$, into the channel which thereby reduces the active channel volume. Due to the presence of the small-signal resistance $g_{\mathrm{mb},2}^{-1}$ the optimised value of $|A_\mathrm{vo}|$ was found to reduce to 2.75 at 400 °C with a minimum of 2.64 around 100 °C. The minor discrepancy between these values and the similarly between the dashed and solid lines in Figure 5.5a suggests that $r_{\mathrm{o},2}$ is still the dominant factor for achieving a large voltage gain.

The deviation of V_O, as seen in Figure 5.5a, was not strongly affected by the body-effect in this arrangement which remains undesirably large.

It should be noted that the increase in v_O for v_I above 2 V in the VTC is due to excessive leakage current through the gate of $\mathrm{J_1}$ after becoming sufficiently forward biased. This restricts the bias voltage that may be placed on the source of $\mathrm{J_1}$ to larger than −2 V above that of the gate.

The low gain and strong OP temperature dependence, with and without body-effect present, suggests that passive loads are not a suitable option for use in high temperature SiC IC op-amps, despite the suggestions made by Patil *et al.* [162].

When an active load used, as in Figure 5.2b, the symmetry of the circuit dictates the optimal choice is to use matched JFETs in order to maximise voltage gain and signal swing. With reference to Figure 5.5b, while $|A_\mathrm{vo}|$ was found to vary between 33.4 and 20.7 between the low and high temperature extremes, respectively, V_O remained insensitive to temperature, fixed at $V_\mathrm{DD}/2 = 7.5\,\mathrm{V}$. This is an extremely desirable result.

The magnitudes of the gains are consistent with the small-signal expression

$$A_\mathrm{vo} = -g_{\mathrm{m},1} (r_{\mathrm{o},1} \parallel r_{\mathrm{o},2}) \tag{5.4a}$$

$$= -\tfrac{1}{2} g_{\mathrm{m},1} r_{\mathrm{o},1}, \quad \text{for } \mathrm{J_1} \equiv \mathrm{J_2}, \tag{5.4b}$$

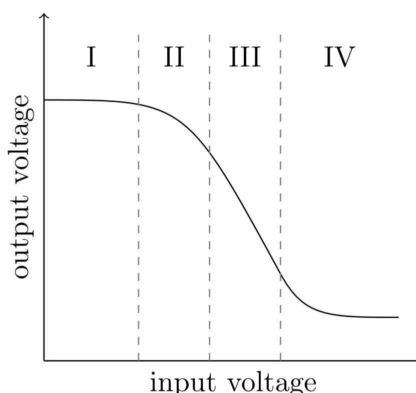


Figure 5.7
Qualitative voltage transfer characteristic of a common-source JFET amplifier with active depletion mode JFET load. The numbered regions refer to the operating state of each device, as described in [90], with region III the desired operating point for achieving high gain linear amplification.

where subscripts 1 and 2 relate to J_1 and J_2, respectively. This is found to be half of the intrinsic gain of the J_1*.

An important observation is that the output voltage swing is limited in both the positive and negative directions. Moving from a negative to a positive value of v_I the four distinct regions of operations are [90]

Region I J_1 is off, J_2 in linear region,

Region II J_1 in saturation region, J_2 in linear region,

Region III J_1 & J_2 in saturation region,

Region IV J_1 in linear region, J_2 in saturation region.

which are qualitatively illustrated in Figure 5.7.

High gain, linear amplification is attained only in Region III where both transistors are in saturation [90]. The total output range therefore is restricted to at most $V_{DD} - 2v_{DS,sat}$. From the circuit in Figure 5.5b with the single supply voltage of 15 V the maximum output voltage swing at 400 °C for achieving linear amplification is only ±2.5 V. This can be improved through use of a larger supply voltage, use of self-aligned devices or operating the transistors in reverse bias. The primary issue in each of these cases is availability, fabrication limitations and reduction in $g_{m,1}$, respectively. The influence of $r_{o,2}$ on A_{vo} can be reduced by using a cascoded transistor as a current buffer; however, this would introduce an additional voltage burden and hence demand a larger supply to achieve a reasonable output voltage swing.

In contrast to Figure 5.2b the finite $v_{BS,2}$ present in Figure 5.3b will alter the active channel resistance of J_2 analogous to the case of the passive load. In order to maintain both J_1 and J_2 in saturation J_2 can be scaled to decrease its open-channel resistance. Importantly, the resistance R_S and R_{x_S} will both reduce if the width, Z, is increased. This would again

*The intrinsic voltage gain represents the maximum voltage gain achievable from a single transistor

introduce a temperature coefficient to V_{O} through the alteration of the v_{GS} degeneration of J_2. The correct volume of active channel to provide the correct resistance and hence current to achieve the desired OP can instead be attained by reducing the channel length, L, of J_2. The downside of this is that Ξ is expected to be inversely proportional to L, thereby introducing an alternative, although smaller, temperature dependence to V_{O}.

An appropriate gate length scaling to maximise voltage gain and signal swing at 400 °C was determined to be 0.512, providing an absolute gate length of 4.61 µm. In this case, the maximum value for $|A_{\mathrm{vo}}|$ at 400 °C was determined as only 5.13, approximately a quarter of the result for isolated devices at this temperature and comparable to the value attained when utilising a passive load. The value at 25 °C provided only a marginal increase to 5.53, roughly one sixth of the value for isolated devices at this temperature. More importantly the V_{O} range was determined as approximately 460 mV. This is far in excess of typical DC signals of interest for amplification and therefore not directly suitable for use in an IC op-amp intended to operate across a wide temperature range.

On account of $v_{\mathrm{GS,2}}$ and $v_{\mathrm{BS,1}}$ being zero in Figure 5.3b its small-signal model is identical to Figure 5.6 as previously derived for the resistive load with body-effective included. In this case, however, the value of $r_{\mathrm{o,2}}$ for the active load is much larger. The ideal voltage gain of Equation 5.4b is no longer achieved and instead Equation 5.3e must again be used. Comparing the VTCs in Figure 5.5b it is clear that for the current device specification $g_{\mathrm{mb,2}}^{-1} \ll (r_{\mathrm{o,1}} \parallel r_{\mathrm{o,2}})$ with the result that $A_{\mathrm{vo}} \approx -g_{\mathrm{m,1}}/g_{\mathrm{mb,2}}$. Consequently, in order to sizeably increase $|A_{\mathrm{vo}}|$ it is required that $g_{\mathrm{mb,2}}$ be first reduced.

Provided the body-effect can be sufficiently reduced and accounted for, the relatively high, moderately stable voltage gain and a temperature independence of V_{O} suggest that a CS amplifier with an active load is a highly suitable option for use in IC op-amps. Two solutions have been identified to simultaneously overcome the issues imposed by the body-effect. The first is to mitigate the influence of the common epilayer by making it intrinsic, as is done in silicon-on-insulator (SOI) technology. This adds extra costs to the fabrication and can introduce additional complications if the quality of the intrinsic epilayer and its interface with the channel epilayer is poor [163]. Also, while semi-insulating substrate provides reasonable isolation between devices, those in close proximity are susceptible to cross talk [95]. The better solution is to electrically isolate the devices by performing a reactive ion etching (RIE) through the body epilayer to the substrate. This can be achieved using traditional RIE techniques. Each device or group of devices would subsequently remain electrically isolated from the substrate via the body-substrate p-n junction and suitably electrically isolated from one another by back-to-back body-substrate p-n junctions, effectively eliminating the issue of cross-talk. The body and source contacts of each device can then be tied together if so desired and so long as the substrate is connected to the lowest potential in the circuit each isolating junction will remain in reverse bias.

The proposed arrangement can be further exploited through placement of a p^{+} epilayer between the body and the channel epilayers to create a more efficient second gate. This can subsequently be coupled to the top gate, thereby enhancing the transconductance and thus intrinsic voltage gain of each device.

Both options introduce additional costs to the fabrication process. It is therefore prudent

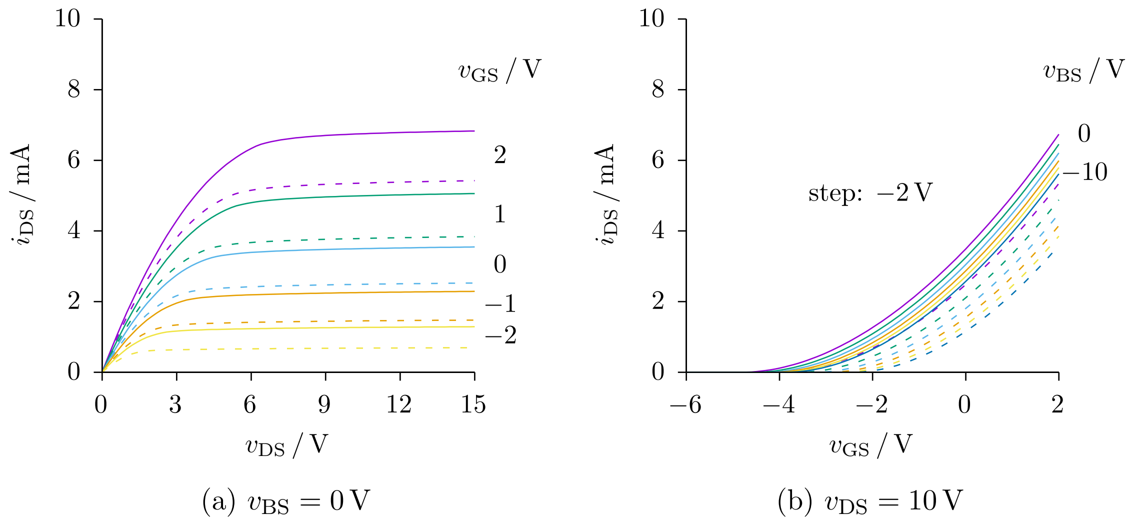


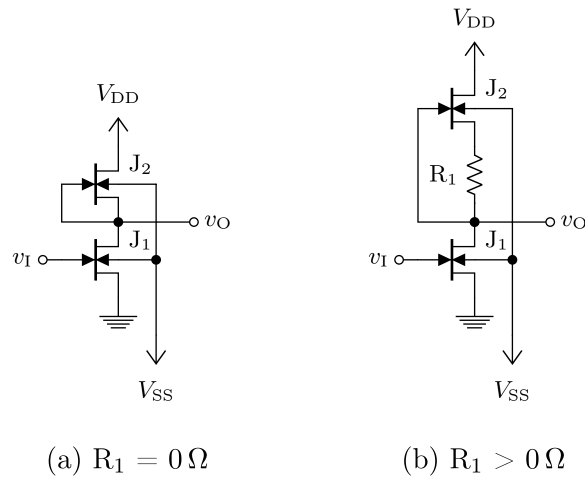
Figure 5.8

SPICE simulated device characteristics for a 9 µm by 250 µm SiC JFET using the experimentally determined value of bottom gate pinch-off voltage (dashed lines) and the maximum nominal value 1 kV (solid lines) for various values of v_{DS}, v_{GS} and v_{BS}.

to first assess the influence of the body-effect after the body epilayer doping concentration has been reduced to the lowest value offered by Cree for its standard epilayer specification, which at the time of writing is $9 \times 10^{14}\,\mathrm{cm}^{-3}$ [125].

The reduction of the body doping concentration, N_b, will have the effect of increasing the pinch-off voltage for the bottom gate, $\phi_{p,b}$, to roughly 1 kV. The value of $\phi_{0,b}$ will also change slightly but will have far less of an influence. The simulated device characteristics for the previously optimised 9 µm by 250 µm JFET before and after increasing $\phi_{p,b}$ is given in Figure 5.8 for various biasing conditions. By increasing $\phi_{p,b}$ the encroachment of the body-channel depletion region into the channel decreases, having the effect of making the turn-off voltage applied to the gate, $v_{GS,off}$, more negative and increasing the channel current, i_{DS}. The influence of v_{BS} on i_{DS}, in the absolute sense, is also significantly reduced. The non-linear dependence of i_{DS} on v_{BS} allows its sensitivity to now be decreased to more acceptable levels using only modest negative v_{BS}. If V_O is selected as 7.5 V and an additional supply voltage, $V_{SS} = -15$ V, is attached to the body epilayer, as in Figure 5.9a, the resulting V_{BS} of an active load transistor will increase to −22.5 V. Not only does this help stabilise V_O, it also provides a significant reduction in the g_{mb} of an load device J_2, thereby resulting in an increase of $|A_{vo}|$ in an active loaded CS amplifier with body-coupling.

The previous SPICE simulations were repeated for the circuit in Figure 5.9a assuming the new value for $\phi_{p,b}$. The optimised channel length scaling for the load at 400 °C was found to increase to 0.822, or around 7.4 µm in absolute value. The subsequent analyses are presented in Figure 5.10a. The VTCs are found to more closely follow the results for the isolated active loaded CS amplifier at both 25 °C and 400 °C with $|A_{vo}|$ increasing to 14.3 at 25 °C and 11.9 at 400 °C. While the range of V_O was also found to reduce to 363 mV this remains inadequate for most DC applications.



(a) $R_1 = 0\,\Omega$ (b) $R_1 > 0\,\Omega$

Figure 5.9
Active loaded common-source amplifier with negative body bias (a) without and (b) with load degradation.

The temperature dependence of the two devices are not the same due to the difference in sensitivity of the top and bottom depletion widths, $W_{n,t}$ and $W_{n,b}$, respectively, between devices, in addition to the slight influence of field dependent mobility through Ξ. It is possible though, through careful choice of channel length scaling and load degeneration using R_{x_S}, to reduce the the temperature drift of V_O to an acceptable level. The additional resistance is explicitly included in the circuit in Figure 5.9b.

The users for these amplifiers will expect stable operation in the temperature range of 300 °C to 400 °C with consistent performance at 25 °C for the purpose of testing. A new optimisation routine was established requiring V_O at 25 °C and 400 °C to be equal to $V_{DD}/2 = 7.5\,\text{V}$, chosen to achieve adequate gain and signal swing, while minimising V_O drift between 300 °C and 400 °C. The optimised values for the channel length and the updated non-self alignment scaling at the source, with respect to the nominal channel length of the modelled device, where determined as 0.733 and 0.558, respectively. The results from the subsequent SPICE simulations are given in Figure 5.10b. The magnitude of the resulting voltage gain showed only small increases to 14.7 and 12.1 at 25 °C to 400 °C, respectively; however, the subsequent range for V_O was reduced to just 6.15 mV across the temperature range of 300 °C and 400 °C, with only a 2.25 mV difference between the values attained at 25 °C and 400 °C. While these achievements are imperfect they should prove adequate for most application requiring a large and wide temperature range.

The previous analysis has shown that in the simple case of a CS amplifier it is possible to compensate most of the influence of the body-effect. The required compensation will however be strongly dependent on the tolerances of the doping concentrations of all three epilayers and the thicknesses of the channel epilayer; as these values can vary by as much as ±50 % and ±10 %, respectively [125], this method is far from an ideal solution. While some improvement was attained the maximum achievable voltage gain was still far below that attained for electrically isolated devices. As the gain enhancement techniques discussed in

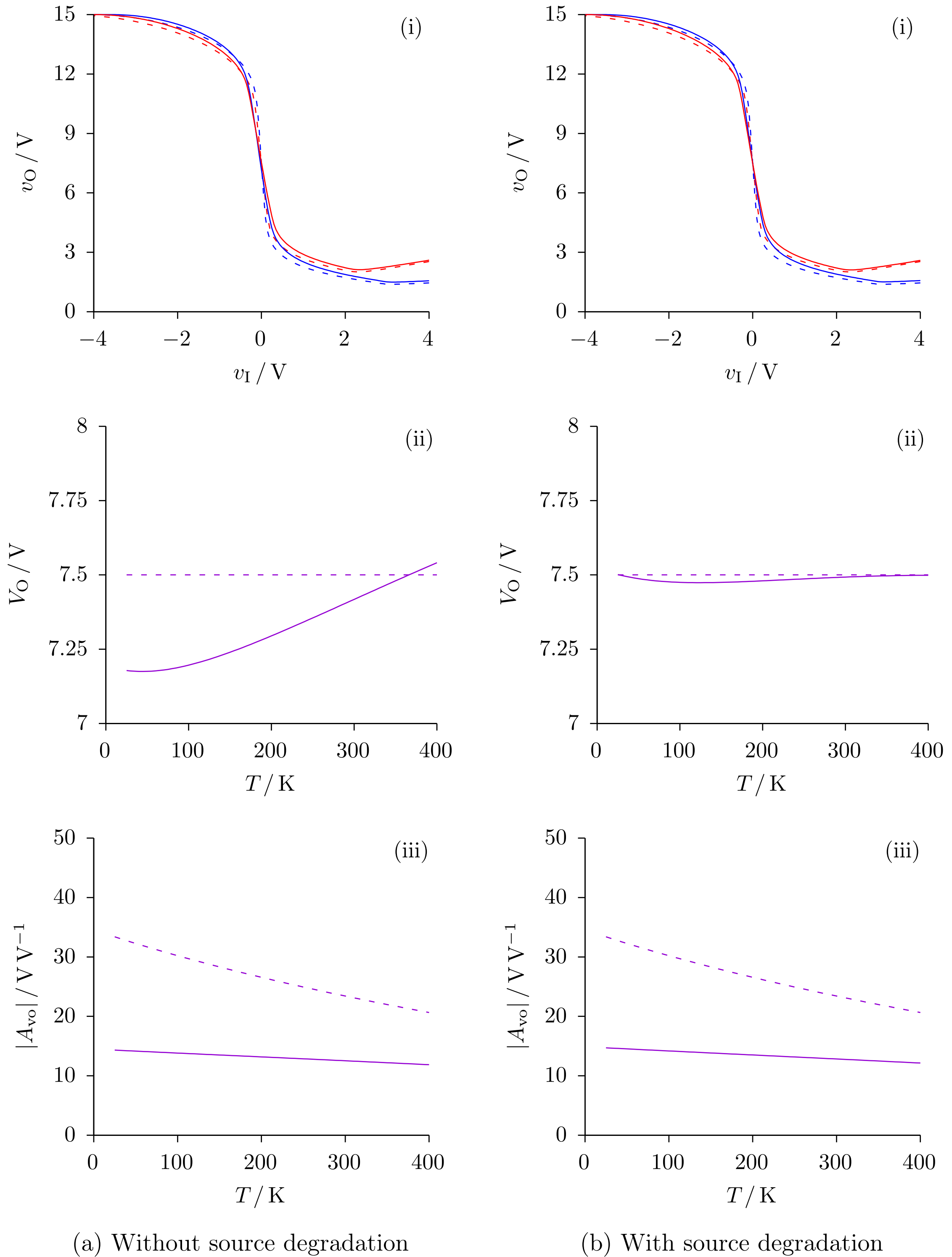
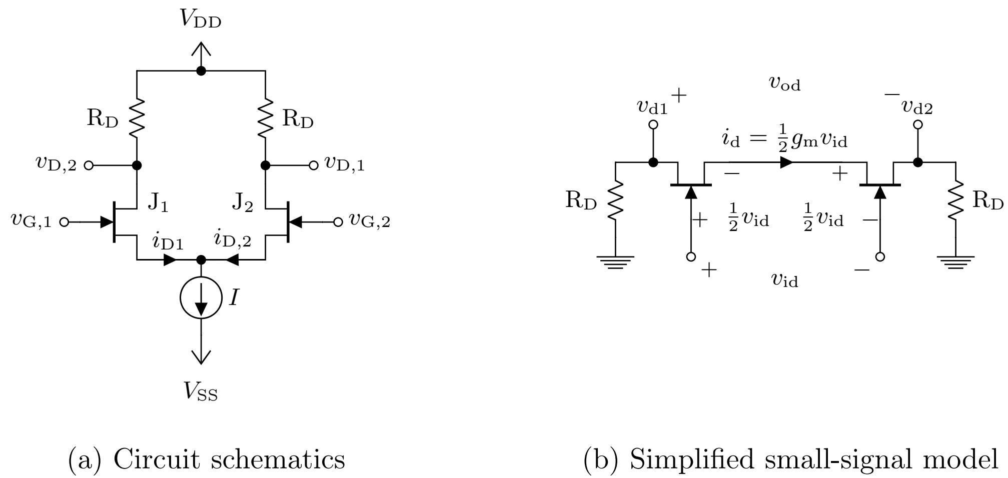


Figure 5.10

(i) Voltage transfer characteristics at 25 °C and 400 °C, (ii) DC output voltage, V_O, for input voltage, $V_I = 0$ V and (iii) low-frequency open-circuit voltage gain, A_{vo}, for the common-source amplifier configurations in (a) Figure 5.9a and (b) Figure 5.9b, with the results from Figure 5.2b (dashed lines) included for reference.



(a) Circuit schematics

(b) Simplified small-signal model

Figure 5.11
(a) A basic differential amplifier with passive loads and constant current-sink bias and (b) its simplified small-signal model. Ideal current-sink.

§2.4.2 are also greatly compromised by the body-effect the gain reduction is hard to recover. For these reasons device isolation should utilised and will be adopted in the simulations for the remainder of this chapter.

5.4 Differential Amplifier

The differential pair is a ubiquitous building block in analogue ICs. Their principle function is to amplify the voltage difference between two inputs irrespective of the common signal [145]. A basic differential amplifier design is presented in Figure 5.11a. Transistors J_1 and J_2 each work in a similar manner to CS amplifiers but with the important distinction that their source terminals are coupled to a common current-sink.

The load devices and the current-sink work together to set the OP for the amplifier. Kirchhoff's first law requires that the sum of currents through each branches must equal that of the sink; this requirement is expressible algebraically as

$$I = i_{D,1} + i_{D,2}, \tag{5.5}$$

where $i_{D,1}$ and $i_{D,2}$ are the drain currents for J_1 and J_2, respectively*. The differential configuration operates through steering the current between either branch in response to the differential input voltage [145, 164].

$$v_{id} = v_{g,1} - v_{g,2} \tag{5.6}$$

Current-to-voltage conversion is again achieved through use of the resistive load elements.

An important feature when an ideal current source is employed is that a signal ground appears at the coupled source terminals [90]. The small-signal equivalent circuit for each half

*Transistors J_1 and J_2 are assumed to have infinite input impedances such that $i_D = i_S$.

of the differential amplifier circuit is then equivalent to that of a single-stage CS amplifier having out-of-phase input voltages equal to half of v_{id}. A corresponding simplified small-signal model is given in Figure 5.11b. The small-signal output voltages can subsequently be deduced as [90]

$$v_{\mathrm{d1}} = -i_{\mathrm{d}} R_{\mathrm{D}} \tag{5.7a}$$

$$= -\tfrac{1}{2} g_{\mathrm{m}} v_{\mathrm{id}} (R_{\mathrm{D}} \parallel r_{\mathrm{o}}) \tag{5.7b}$$

$$v_{\mathrm{d2}} = +i_{\mathrm{d}} R_{\mathrm{D}} \tag{5.7c}$$

$$= +\tfrac{1}{2} g_{\mathrm{m}} v_{\mathrm{id}} (R_{\mathrm{D}} \parallel r_{\mathrm{o}}), \tag{5.7d}$$

with a resulting small-signal differential output voltage of

$$v_{\mathrm{od}} = v_{\mathrm{d1}} - v_{\mathrm{d2}} \tag{5.7e}$$

$$= -g_{\mathrm{m}} v_{\mathrm{id}} (R_{\mathrm{D}} \parallel r_{\mathrm{o}}) \tag{5.7f}$$

$$= A_{\mathrm{vd}} v_{\mathrm{id}} \tag{5.7g}$$

and differential voltage gain of

$$A_{\mathrm{vd}} = \frac{v_{\mathrm{od}}}{v_{\mathrm{id}}} = -g_{\mathrm{m}} (R_{\mathrm{D}} \parallel r_{\mathrm{o}}) \approx -g_{\mathrm{m}} R_{\mathrm{D}}. \tag{5.7h}$$

For any real differential amplifier the current-sink will provide a finite output impedance. This value of the output signal, v_{o}, is then a function of both differential input voltage, v_{id}, and common-mode input voltage, v_{ic}, and the corresponding differential and common-mode voltage gains, A_{vd} and A_{vc}, respectively, whereby A_{vc} relates the change in v_{o} with v_{ic}. The combined influence may be succinctly expressed as

$$v_{\mathrm{od}} = A_{\mathrm{vd}} v_{\mathrm{id}} + A_{\mathrm{vc}} v_{\mathrm{ic}}, \tag{5.8}$$

where, most generally,

$$v_{\mathrm{ic}} = \frac{v_{\mathrm{g,1}} + v_{\mathrm{g,2}}}{2}. \tag{5.9}$$

A suitable SPICE sub-circuit utilised in this section that is capable of simultaneously supplying a differential and common-mode input signal during differential amplifier simulations is shown in Figure 5.12* [145].

An important figure of merit for differential amplifiers is their common-mode rejection ratio (CMRR) which quantifies their ability to reject common-mode signals and is in general frequency dependent [90]. This is determined from the ratio of the differential and common-

* While the large-signal operation using this arrangement is correct, a proviso is that the small-signal input impedance of the amplifier will alway appear to be the token value of the resistor $\mathrm{R_{id}}$.

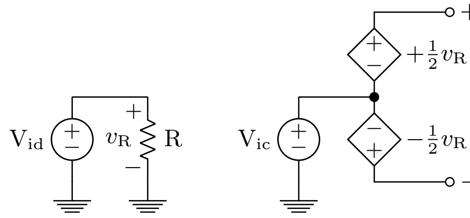


Figure 5.12
A SPICE sub-circuit capable of simultaneously supplying differential and common-mode voltage signals [145].

mode voltage gains as

$$\mathrm{CMRR} = \frac{|A_{\mathrm{vd}}|}{|A_{\mathrm{vc}}|}, \tag{5.10a}$$

and is most often expressed in decibels using the equation*

$$\mathrm{CMRR/dB} = 20\log_{10}\frac{|A_{\mathrm{vd}}|}{|A_{\mathrm{vc}}|}. \tag{5.10b}$$

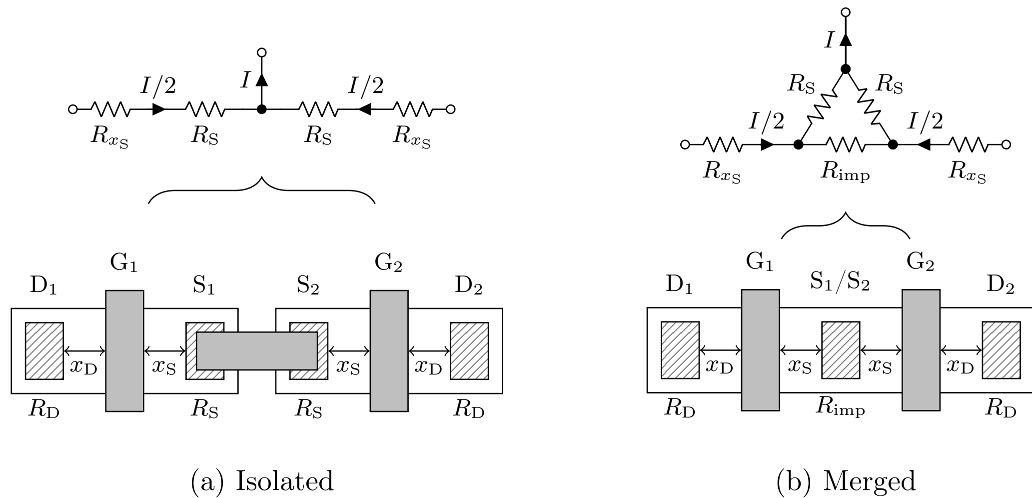
The common-mode voltage gain should ideally be zero [145]. A finite value results from a combination of any asymmetry of the differential pair and the finite small-signal output resistance of the biasing current-sink [145]. In SPICE simulations the former can be readily eliminated and thereby such simulations represent the upper limit for the CMRR for a given circuit topology.

Further consideration can be given to the connections between devices for the differential amplifier. Figure 5.13 presents the case of two source-coupled differential JFETs, i.e., the *tail* point of the differential pair. Providing the source contact lengths in both Figure 5.13a and Figure 5.13b are much larger than the transfer length for current flowing into them, the bias current, I, can in each case be viewed as passing into the tail from each side through a resistance R_{S}. Both arrangements are therefore equivalent for OP analysis and will provide the same value of V_{O}. Conversely, assuming an ideal current-source sink, none of the small-signal current will pass through the tail but will instead pass through the parallel combination of R_{imp} and $2R_{\mathrm{S}}$. While the value will depend on the length of the implanted region and its resistivity it will be lower than the series combination of the contact resistances and therefore a suitable option.

While this chapter focuses primarily on the low-frequency performance of the circuit, an additional benefit of Figure 5.13b is the decrease in capacitance due to the reduction of contact area. If the shared body region is connected to the source of each transistor then an appreciable common-mode parasitic capacitance will unfortunately still exist; however, if the body is tied to ground then this can be significantly reduced at the expense of reintroducing the body-effect. Further discussion is outside the scope of this work.

The conclusions drawn from the discussion of the CS amplifier identify the suitability of

*The conversion to dB require either that the input and output signals be of the same form, i.e. sinusoids, or that root mean square (RMS) values are used [91].



(a) Isolated (b) Merged

Figure 5.13

Interconnection configurations and equivalent circuits for two source-coupled JFETs.

active loads for achieving high voltage gain with minimal output bias voltage drift. Similar measures have been previously adopted by Patil *et al.* while developing SiC differential amplifiers [96]. A viable differential amplifier with differential outputs is presented in Figure 5.14a.

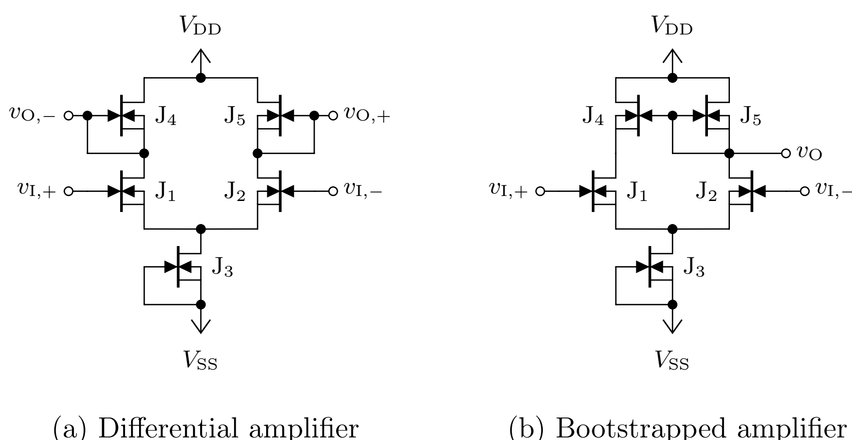
An alternative arrangement employing a current-mirror load more commonly utilised in IC designs is shown in Figure 5.14b [165]. While similar in appearance to Figure 5.14a its underlying operation is very different*. An advantage of this arrangement is increased voltage gain when taking a single ended output which is more appropriate when constructing multi-stage amplifiers such as op-amps; however, the finite small-signal output resistance of J_5 limits the value of $g_{m,1}(r_{o,1} \parallel r_{o,5})$.

In each of the circuits in Figure 5.14 a rudimentary current-sink has been formed using a single DM JFET biased to operate in saturation to provide a relatively voltage insensitive current of $i_{DSS,3}$ [165]. Two unideal features are the voltage burden to ensure it operates in the saturation and the finite output resistance. A suitable negative supply, V_{SS}, is therefore required to accommodate the voltage drop while maintaining $v_{GS,1}$ at approximately zero volts. With J_1, J_2, J_4 and J_5 matched, J_3 set to twice the width of the other transistors†, and V_{DD} set to $|2V_{SS}|$ then V_O will be fixed at half of V_{DD} at all temperatures. The finite resistance will unfortunately allow the coupled source voltage to change in response to common mode signals, thereby introducing a finite common-mode gain, A_{vc}, even for a perfectly matched differential pair.

The proposed design ensures $v_{GS,1}$ and $v_{GS,2}$ at equilibrium will be zero, in harmony with the source and sink transistors. J_1 and J_2 can conceivably be forward biased as much as 2 V, provided the common-mode input is not excessive, in an effort to increase their transconductance; however, the corresponding decrease in output resistance and the ap-

*The useful benefits and limitations of positive feedback were discussed in §2.4.2.

†The equilibrium current through the sink is twice as large as through the other transistors causing the voltage dropped across its contacts to be twice as large for a given contact width.



(a) Differential amplifier (b) Bootstrapped amplifier

Figure 5.14

Differential amplifier configurations with (a) independent depletion-mode JFET active loads and (b) current-mirror load providing differential to single-ended output conversion.

preciable difference in temperature coefficients identify this as a unsuitable option for this configuration.

When using active loads in a differential amplifier with a shared current-sink bias, caution must be taken to ensure the bias currents create the appropriate conditions for each of the five JFETs, as small deviations in i_{DS} can result in rather large changes in v_{DS} of the load devices which could potentially cause the amplifier's OP to leave region III. The presence of the body-effect is therefore also problematic for the differential amplifier. In this section the body-effect is assumed to have been mitigated through appropriate electrical isolation of devices as explained in the preceding section. If body-coupled transistors were to be used then the increased substrate encroachment in the active load devices compared with the sink device would mean that the correct geometrical ratio of dimensions to satisfy the current-sinking requirement differs from the case for isolated devices [90]. Even if scaling was performed in order to correctly bias all of the devices, the resulting difference in temperature dependences between devices on account $W_{n,t}$ and $W_{n,b}$ would introduce an appreciable drift in V_O. In such cases it may be possible to combat this through the combined use of a floating voltage reference and current-mirroring in order to clamp V_O in a similar manner as was utilised in Figure 2.31 [95, 166].

In the following SPICE simulations supply voltages of 15 V and −7.5 V were chosen to establish a temperature insensitive value for V_O of 7.5 V. Due to the large values for $v_{DS,sat}$ these chosen values represent a reasonable lower limit for the current device specification. Given the underlying symmetry of the circuit and the fact that the transconductance is a function of v_{DS}, provided V_{DD} and V_{SS} are scaled proportionally the voltage gain can be increased. This is not possible, however, if the body-effect is present. The voltage gain could also be improved through increasing of the width-length ratio of each device at the expense of increase power dissipation.

Differential input VTCs in the absence of common-mode input for each circuit in Figure 5.14 are presented in Figure 5.15. The behaviour of the circuits can be understood further

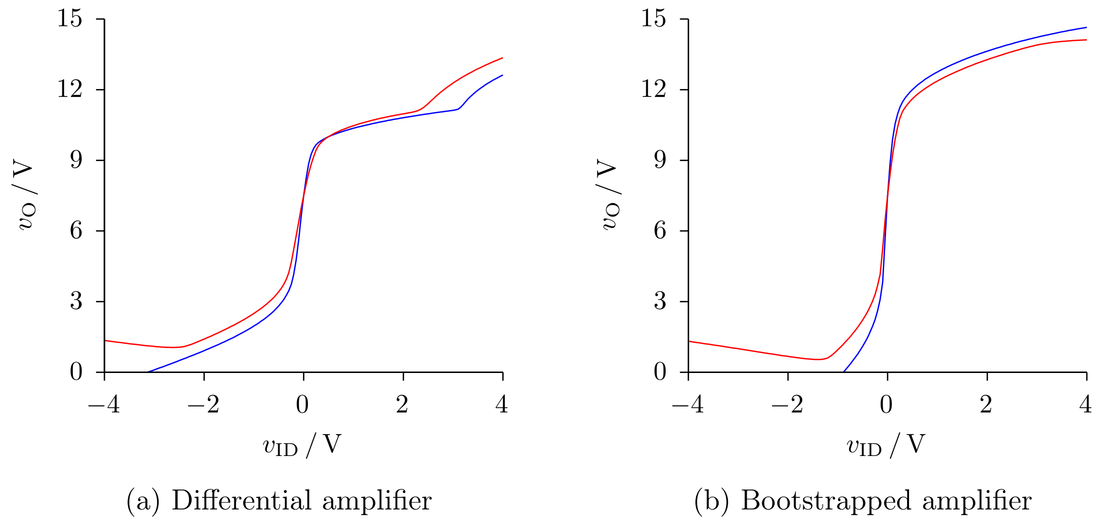


Figure 5.15

Large-signal single-ended output voltage transfer characteristics at 25 °C (blue) and 400 °C (red) for the circuits in (a) Figure 5.14a and (b) Figure 5.14b.

from observing the individual transistor currents and voltages as shown in Figure 5.15. Both circuits steer current in response to a differential input which to maintain correct operation is limited of approximately ±100 mV in each case. Sharper transitions of channel current, i_{DS}, appear in Figure 5.16b on account of the bootstrapping active of J_4, which explains the increase in differential voltage gain when taking a single ended output. The circuit in Figure 5.14a behaves much the same as two CS amplifiers; however, unlike the fixed biased CS amplifier the voltage at the coupled-source node of the differential pair can float in response to input voltages, giving rise to differences in the VTCs outside of the intended operating region. When using a current-mirror as a load, as in Figure 5.14b, the behaviour is very different. When all transistors are in saturation $v_{DS,1}$ will follow $v_{DS,2}$ and be very almost equal in value regardless of the input. By extension $v_{DS,1}$ will follow $v_{DS,2}$. The differing v_{GS}'s due to the input facilitate the steering of current. The asymmetry in Figure 5.16b about the equilibrium point is a consequence of the current-mirror which is driven from one side only.

The small-signal values for $|A_{vd}|$ and $|A_{vc}|$ as a function of temperature for each circuit in Figure 5.14 are presented in Figure 5.17 alongside their resulting CMRRs. The values of $|A_{vd}|$ and $|A_{vc}|$ at 25 °C for the circuit in Figure 5.14a were found to be 33.4 (30.5 dB) and 1.91 (5.64 dB), respectively, when a differential output was taken. As expected, these values go down with temperature, reaching 20.7 (26.3 dB) and 1.91 (5.41 dB) at 400 °C.

Similar figures are presented in Figure 5.17b for the circuit in Figure 5.14b. The values of $|A_{vd}|$ and $|A_{vc}|$ at 25 °C were determined to be 32.4 (25.9 dB) and 0.96 (−0.61 dB), respectively. The slightly lower values for $|A_{vd}|$ compared with the differential output value from Figure 5.14 can be understood from the sub-unity gain of the bootstrapped voltage buffering transistor J_4; with body-effect included for the same selection of devices the voltage buffering action of J_4 is significantly compromised and the benefits of the bootstrapping are lost.

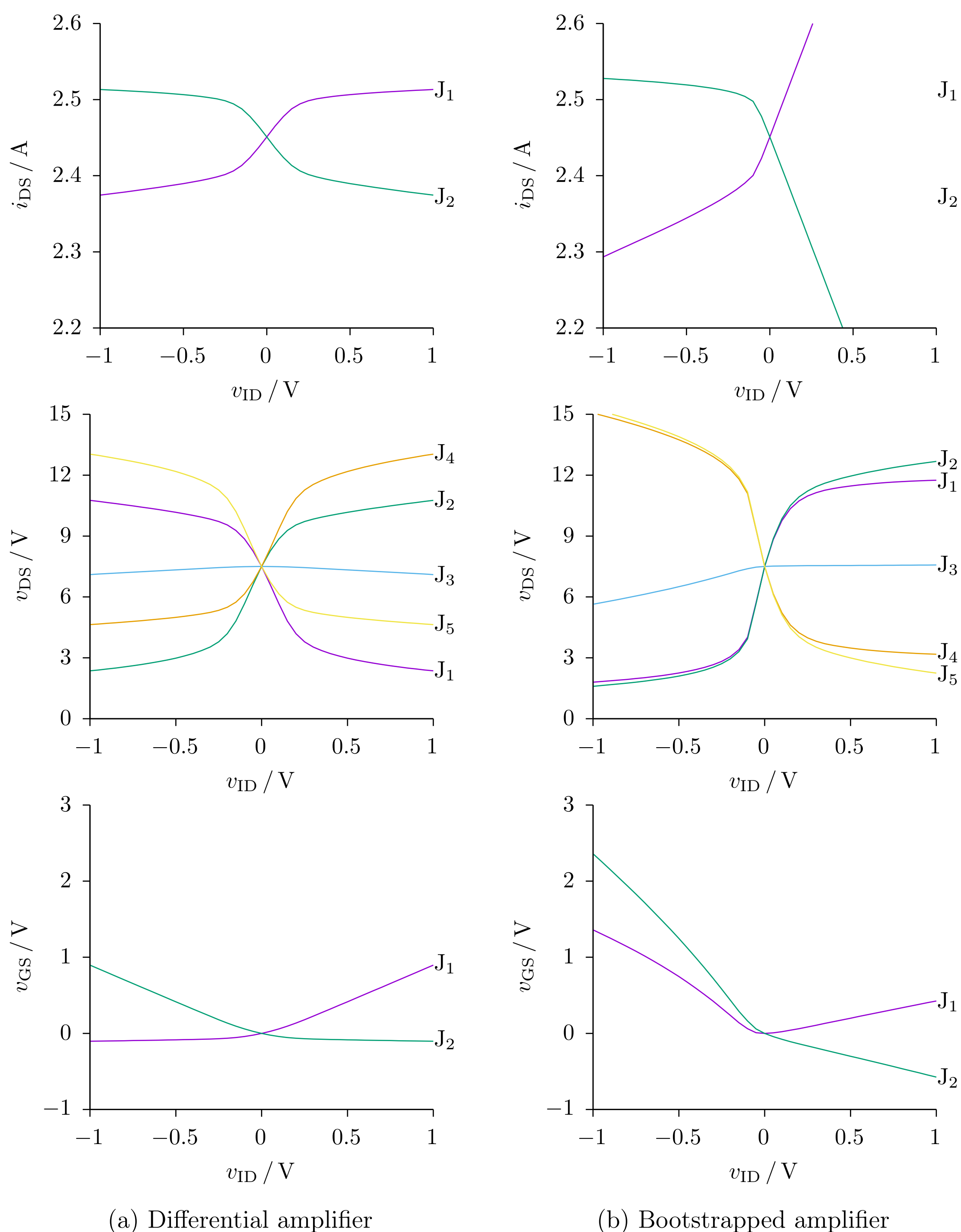


Figure 5.16

SPICE simulations of the differential input large-signal branch currents and voltages for the circuits in (a) Figure 5.14a and (b) Figure 5.14b in the absence of common-mode input using supply voltages of 15 V and −7.5 V.

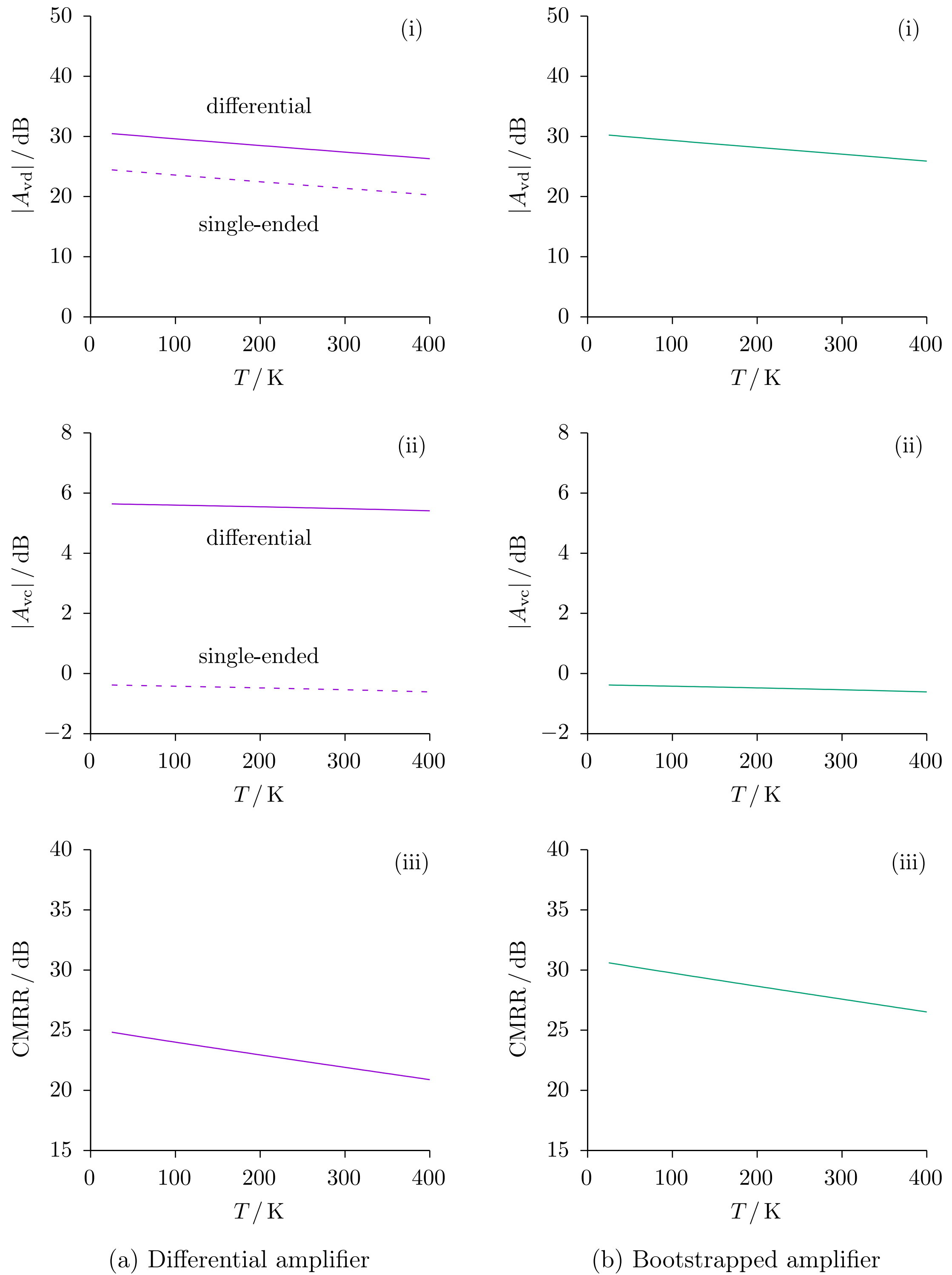
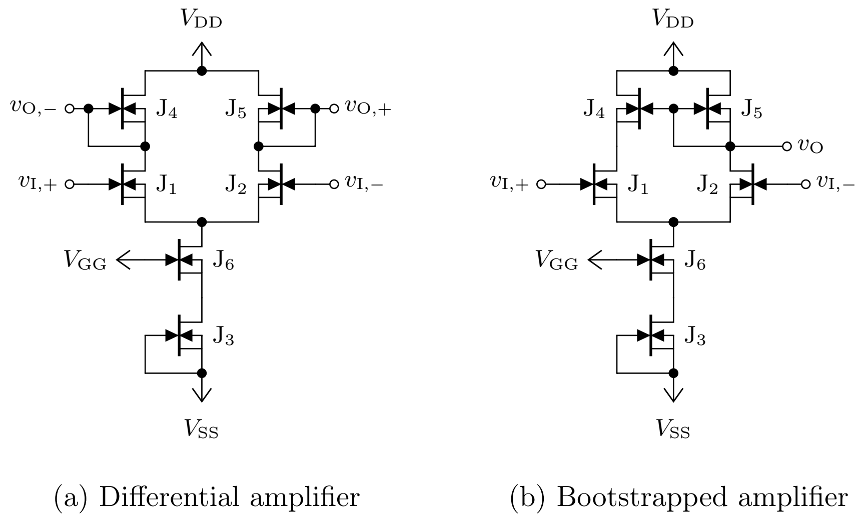


Figure 5.17

Small-signal (i) differential and (ii) common-mode voltage gains and (iii) corresponding common-mode rejection ratios for the circuits in (a) Figure 5.14a and (b) Figure 5.14b.



(a) Differential amplifier (b) Bootstrapped amplifier

Figure 5.18
Differential amplifier configurations with (a) independent depletion-mode JFET active loads and (b) current-mirror load providing differential to single-ended output conversion, including a current buffer to reduce the common-mode voltage gain.

While the gain of both circuits are comparable, the benefit found from using Figure 5.14b is that a single ended output can be taken, reducing the need for further differential stages or a subsequent differential to single-ended conversion stage to be included.

The corresponding values of CMRR are acceptable for many applications but far from ideal. It is possible to use an additional transistor in a common gate (CG) configuration as a current buffer for the sink transistor, a process known as cascoding*, in order to stabilise $v_{DS,5}$ [164, 165], as shown in Figure 5.18. The additional voltage burden and the desire to maintain a temperature independent OP requires that V_{SS} be increased to -15 V and a gate voltage, V_{GG}, on J_6 to be -7.5 V†.

SPICE simulations for the large-signal VTCs were repeated for the circuits in Figure 5.18 with the results presented in Figure 5.19. These are, as expected, almost indistinguishable from those in Figure 5.15. The differential small-signal voltage gains given in Figure 5.20 also closely resemble the results of the previous analysis. Now, however, the common-mode voltage gain is significantly reduced due to the ability of J_6 to stabilise $v_{DS,3}$. For Figure 5.18a and Figure 5.14b the maximum value for $|A_{vc}|$ at 400 °C was found to be 0.03 (-30.86 dB) and 0.02 (-32.95 dB), respectively. This resulted in significant improvement in the CMRR of each amplifier, increasing to 721.13 (57.16 dB) and 895.66 (59.04 dB), respectively, at 400 °C.

The only notable published work on SiC JFET differential amplifiers comes from Patil *et al.* whose key results were presented in §2.4.3 [96,162]. Their devices and circuit arrangement share similarity to those developed and utilised in this work with the only major distinction

*A similar procedure could in fact be used on the active loads to enhance voltage gain, but only if a larger positive supply voltage is utilised.

†The supply voltage could be derived from the existing supply voltages; however, this is outside the scope of the current discussion.

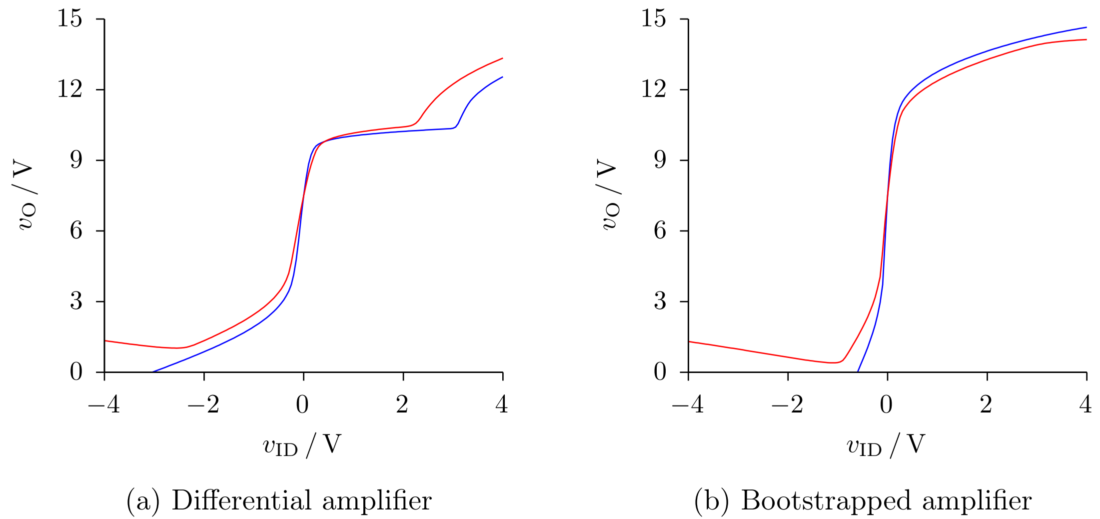


Figure 5.19
Large-signal single-ended output voltage transfer characteristics at 25 °C (blue) and 400 °C (red) for the circuits in (a) Figure 5.18a and (b) Figure 5.18b.

being their choice of 6H–SiC over 4H–SiC [162]. In their work no mention was given to the body-effect or that steps were taken to electrically isolate the devices. One possibility is that the large supply voltage of 45 V used was able to mitigate its influence through the introduction of a large negative v_{BS} on the load devices, such that the gain reducing effect of g_{mb} was sufficiently diminished, while simultaneously increasing the output resistance and transconductance of the differential pair. They were able to achieve large differential voltage gains of roughly 160 (44 dB) for an active loaded amplifier. Their accompanying figures suggest both increase of load resistance by source degradation and the use of many parallel devices to increase the effective device channel width are the reasons behind the large voltage gain. Similar conditions applied to the SPICE simulations were able to provide comparable and improved results. Their inability to maintain a stable DC output voltage is a major limitation for their work which has been successfully eliminated in the circuit presented in this chapter.

5.5 Level Shifter and Voltage Buffer

While both the JFET CS and differential amplifier boasts a large input impedance, at least at low frequencies, their output impedances leave much to be desired, particularly when active loads are utilised. The output for each amplifier stage can be modelled as either a Norton or Thévenin equivalent circuit, as are illustrated in Figure 5.21, where I_{No} and R_{No} are the Norton equivalent current source and resistance, respectively, and V_{Th} and R_{Th} are the Thévenin equivalent voltage source and resistance, respectively*.

When a finite load is coupled to the output of a voltage amplifier the output signal is split between the amplifier's Thévenin equivalent output resistance, R_o, and the load resistance,

*By definition $R_{No} = R_{Th}$

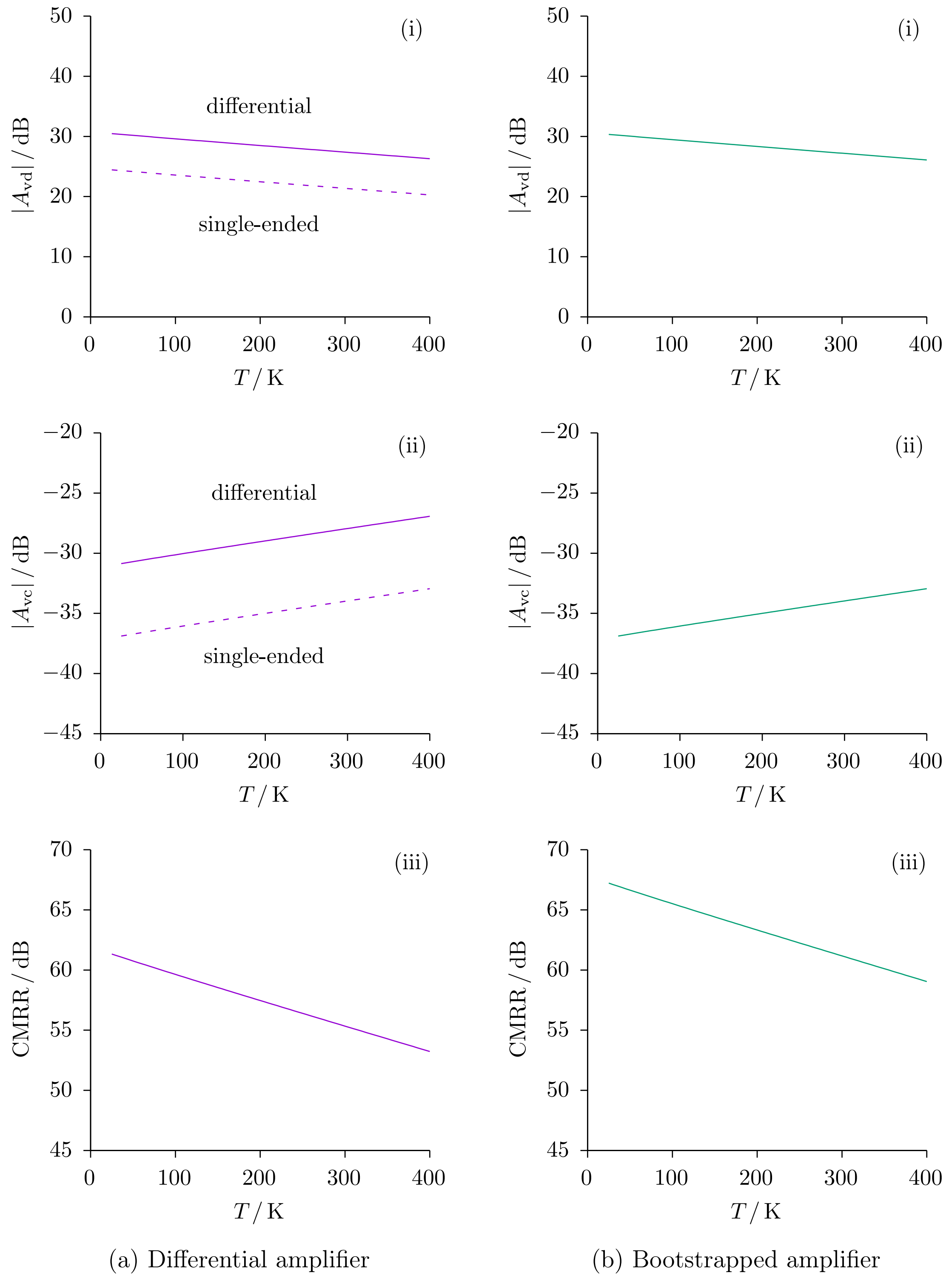
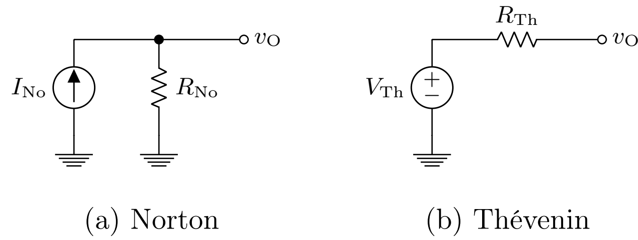


Figure 5.20

Small-signal (i) differential and (ii) common-mode voltage gains and (iii) corresponding common-mode rejection ratios for the circuits in (a) Figure 5.18a and (b) Figure 5.18b.



(a) Norton (b) Thévenin

Figure 5.21
Norton and Thévenin equivalent circuits.

R_l. The voltage appearing across the load is thereby found from [90]

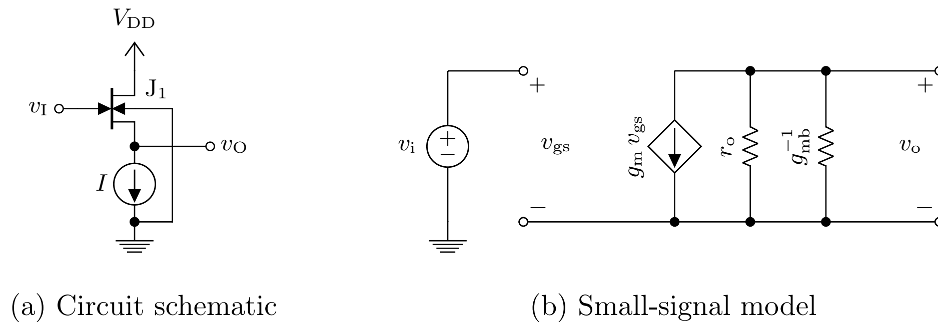
$$v_o = A_{vo} v_i \frac{R_l}{R_l + R_o} = A_v v_i. \tag{5.11}$$

To maximise voltage transfer it is therefore desirable for the output impedance of the amplifier to have a much lower impedance than the load.

A circuit which can accept a signal from a voltage amplifier with moderately high output impedance and reproduce it at its low impedance output is referred to as a voltage buffer*. This process can be achieved using the common drain (CD) amplifier topology, also know as a source-follower, whose general IC configuration is given in Figure 5.22a. The corresponding small-signal model of the CD amplifier with body-effect included is given in Figure 5.22b. Here g_{mb}^{-1} represents the equivalent resistance between source and body, looking into the source† [90]. Provided R_i remains very large, v_g will equal the input voltage, v_i. From Figure 5.22b the output and input voltages can be deduced as

$$v_o = g_m v_{gs} (r_o \parallel g_{mb}^{-1}) \tag{5.12}$$

*A voltage buffer is needed only if the amplifier is driving a resistive load.
†The input resistance looking into the gate is still ∞.



(a) Circuit schematic (b) Small-signal model

Figure 5.22
The general source-follower configuration (a) circuit schematic and (b) its small-signal model, assuming an infinite input impedance, an ideal current source bias and the influence of the body-effect.

and

$$v_{\mathrm{i}} = v_{\mathrm{gs}} + v_{\mathrm{o}} \tag{5.13a}$$

$$= v_{\mathrm{gs}} + g_{\mathrm{m}} v_{\mathrm{gs}} (r_{\mathrm{o}} \parallel g_{\mathrm{mb}}^{-1}). \tag{5.13b}$$

respectively, from which it can be determined,

$$A_{\mathrm{vo}} = \frac{v_{\mathrm{o}}}{v_{\mathrm{i}}} \tag{5.14a}$$

$$= \frac{(g_{\mathrm{mb}}^{-1} \parallel r_{\mathrm{o}})}{g_{\mathrm{m}}^{-1} + (g_{\mathrm{mb}}^{-1} \parallel r_{\mathrm{o}})} \tag{5.14b}$$

$$\approx \left. \frac{g_{\mathrm{m}}}{g_{\mathrm{m}} + g_{\mathrm{mb}}} \right|_{r_{\mathrm{o}} \gg g_{\mathrm{mb}}^{-1}} \tag{5.14c}$$

and the buffer output resistance as

$$R_{\mathrm{o}} = \left[g_{\mathrm{m}}^{-1} \parallel g_{\mathrm{mb}}^{-1} \parallel r_{\mathrm{o}} \right]. \tag{5.15}$$

From Equations 5.14 and 5.15 it is clear that the body-effect will have a drastic negative influence on the performance of the voltage buffer, thereby strengthening the argument for electrically isolating the bodies. For the devices under study, the influence of the finite output resistances of J_1 and the current-sink will only minimally degrade the buffering capability.

The simplest approach for achieving the current-sink is again to use a matching DM JFET as configured in Figure 5.23. If no current is drawn from the input then the current through each transistor is the same. When both devices are in saturation $v_{\mathrm{GS,2}}$ is held at zero causing v_{O} will follow v_{I}. This is suitable for the output stage of an op-amp, but requires first that the DC input voltage be level-shifted to zero.

The large-signal VTC for the circuit in Figure 5.23 determined using SPICE is presented in Figure 5.24 (solid line) alongside the ideal unity gain characteristic (dashed line). The low-frequency small-signal voltage gain at 25 °C and 400 °C where found to be 0.99 and 0.98, respectively, which are very close to the ideal value.

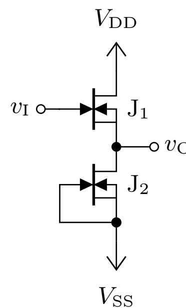


Figure 5.23
Common-drain amplifier with depletion-mode JFET current-sink bias.

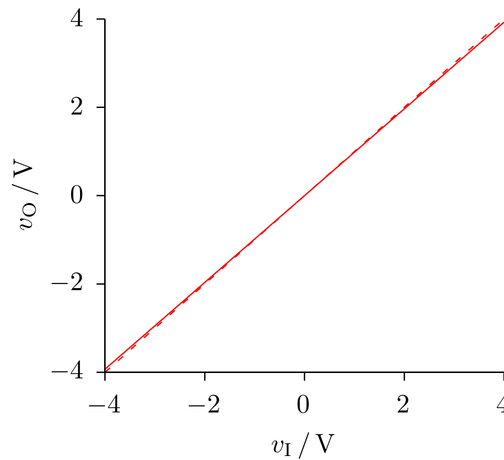
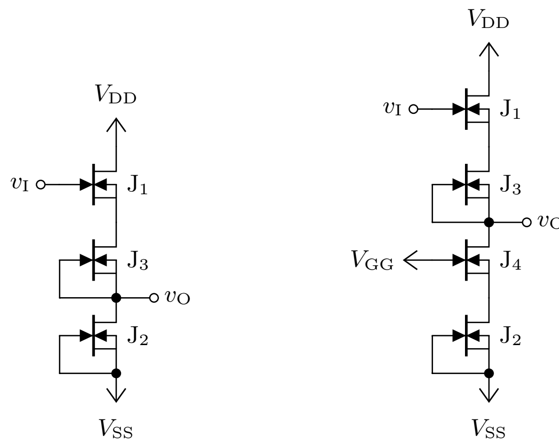


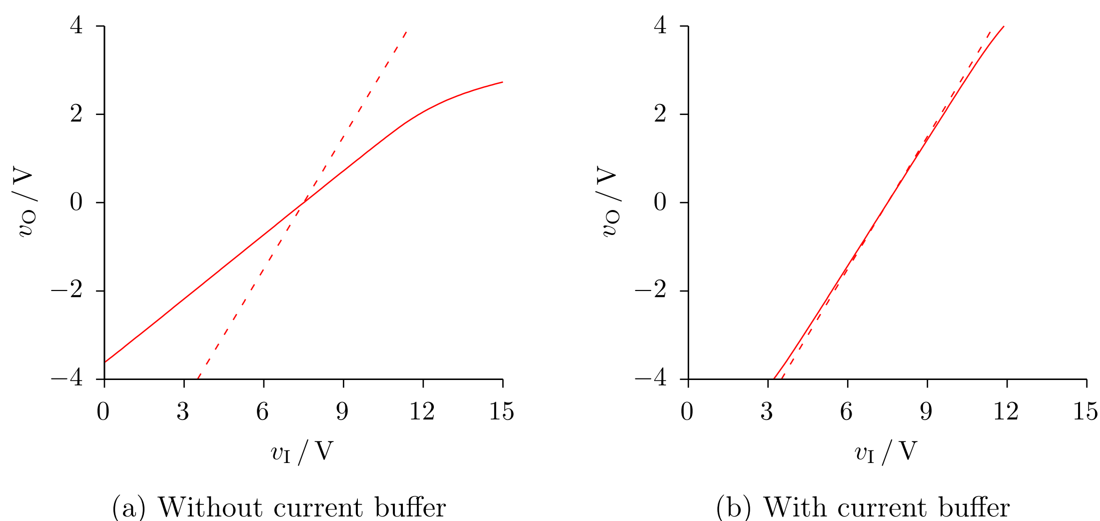
Figure 5.24
Voltage transfer characteristic for the source-follower circuit in Figure 5.23 at 400 °C (solid line) in comparison with the ideal voltage buffer (dashed line).

The source-follower configuration can also be used to achieve voltage shifts; this is demanded to establishing appropriate bias conditions at the input of successive stages. This can be achieved in one of two basic ways [164]. The first method requires that J_2 in Figure 5.23 sources a current appropriate to introduce a finite v_{GS} for J_1. It is more often required that the level at V_O be lower than V_I, thereby requiring a positive v_{GS} for J_1. The reduction of the input impedance of J_1 limits that amount of voltage that can be dropped in any one stage and is therefore inconvenient. The resulting asymmetry between transistors also introduces a temperature dependence suggesting its unsuitability. The second commonly utilised option is to place a resistor between J_1 and J_2 over which a voltage may be dropped. An issue with this is that the resistance will likely have a different temperature dependence than the JFETs.



(a) Without current buffer (b) With current buffer

Figure 5.25
Voltage level-shifter (a) without and (b) with current buffering.



(a) Without current buffer

(b) With current buffer

Figure 5.26
Voltage transfer characteristics for the voltage level-shifter depicted in (a) Figure 5.25a and (b) Figure 5.25b.

A simple solution to this problem is the circuit in Figure 5.25a which replaces the resistor with a JFET. Taking V_I from the previous stage as half V_{DD}; making all three JFETs identical, including their contact resistances; and choosing the supplies such $V_{DD} = |2V_{SS}|$, then from Ohm's law V_O will equal 0 V. Provided that V_I remains half of V_{DD}, which has been shown possible, then V_O will hold steady regardless of temperature. This value is suitable both for the input of a subsequent gain stage and the output stage. This arrangement is highly process insensitive as the ratio of all three devices will remain the same. It will also be insensitive to supply variation, i.e., maintain a large power supply rejection ratio (PSRR), provided the ratio is adequately maintained and their values are large enough to ensure all devices remain in saturation.

A VTC at 400 °C is given in Figure 5.26a. The major issue is that the output signal will undergo voltage division, splitting equally between J_3 and J_4. The voltage gain at 25 °C and 400 °C expectedly reduces to 0.49 and 0.48, respectively. The circuit in Figure 5.25b overcomes this by casoding a CG transistor to act as a current buffer between the output and the sink. To maintain the appropriate bias conditions and temperature insensitivity V_{SS} must be increased to −15 V and a V_{GG} of −7.5 V should again be used. The corresponding VTC at 400 °C is given in Figure 5.26b and shows that the voltage gain is almost entirely recovered, achieving and $|A_{vo}|$ of 0.97 and 0.95 at 25 °C and 400 °C, respectively.

5.6 Operational Amplifier

An ideal op-amp senses the voltage difference across its two inputs and produces a frequency independent amplified version at its output, irrespective of the connected load and without drawing any current from the signal source. Other important features are an infinite CMRR and zero voltage offsets [90].

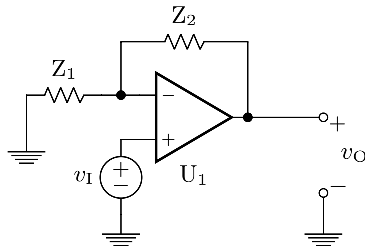


Figure 5.27
Non-inverting operational amplifier configuration.

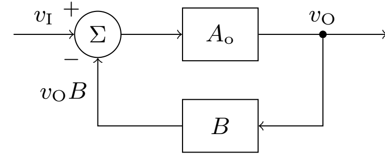


Figure 5.28
Block model for a negative feedback voltage amplifier.

The preceding findings suggest these requirements can be sufficiently satisfied through combining the aforementioned circuit topologies, using a differential amplifier stage with single-ended output as the input stage, a level-shifter, a cascaded CS amplifier to enhance the gain, a second level-shifter and lastly an output buffer to provide a low impedance output.

While it has been shown that the temperature dependence of the DC output drift can be effectively eliminated through a careful selection of device geometries and supply voltages the simulated voltage gain was found to vary noticeably. Inconsistencies in the material and fabrication process can also introduce gain inconsistencies between batches. An inherent and extremely useful property of an op-amp is that it may utilise negative feedback to stabilise the gain close to a desired value.

The non-inverting amplifier configuration presented in Figure 5.27 provides an example of negative feedback applied to op-amp $\mathrm{U_1}$*. With reference to the corresponding block diagram in Figure 5.28 a proportion of v_O appears at the negative input of $\mathrm{U_1}$ through the voltage divider network established using impedances $\mathrm{Z_1}$ and $\mathrm{Z_2}$, providing a feedback factor

$$B = \frac{Z_1}{Z_1 + Z_2}. \tag{5.16}$$

Noting that

$$v_\mathrm{O} = A_\mathrm{o}(v_+ - v_-) \tag{5.17a}$$

$$= A_\mathrm{o}\left(v_\mathrm{I} - v_\mathrm{O}B\right) \tag{5.17b}$$

the resulting closed-loop voltage gain, assuming an op-amp with finite open-loop voltage gain, A_o, is subsequently determined as [88]

$$\frac{v_\mathrm{O}}{v_\mathrm{I}} = \frac{A_\mathrm{o}}{1 + A_\mathrm{o}B} \tag{5.18a}$$

which in the limit of large open-loop voltage gain reduces to

$$A = \lim_{A_\mathrm{o}\to\infty} 1 + \frac{Z_2}{Z_1} = B^{-1}. \tag{5.18b}$$

*Supply connections are omitted for conciseness.

This analysis suggests that provided the open-loop gain can be made sufficiently large then the closed-loop voltage gain will approximately equal to a fixed value determined by the choice of external impedances. If Z_1 and Z_2 are made resistors having comparable temperature coefficients then the gain can be made almost independent of temperature. It's worth noting that while the ratio of the two feedback resistors is the significant factor in determining the gain, larger values will have a smaller loading effect on the amplifier and are thus more desirable. It is therefore sensible to select resistance values at least twenty times larger than the output impedance of the op-amp.

The input impedance of the non-inverting amplifier remains high, equaling that of the non-inverting input. In the limiting case where the feedback impedances are replaced by short circuits one attains a buffer amplifier with output voltage determined as

$$v_{\mathrm{O}} = \frac{A_{\mathrm{o}}}{1 + A_{\mathrm{o}}} v_{\mathrm{I}} = \lim_{A_{\mathrm{o}} \to \infty} v_{\mathrm{I}}. \tag{5.19}$$

The influence of the amplifier's open-loop voltage gain also has the affect of massively reducing the output impedance of the amplifier providing an extremely high quality voltage buffer suitable for use alongside very low resistance loads.

The circuit schematics for the proposed 4H–SiC NLDM JFET op-amp is presented in Figure 5.29. SPICE simulation were performed using both ±15 V and ±30 V supplies for comparison. The open-loop VTC using ±15 V supplies is presented in Figure 5.30a for 25 °C and 400 °C, assuming a common-mode input of 0 V. The corresponding low-frequency small-signal differential voltage gain as a function of temperature between 25 °C and 400 °C is given in Figure 5.30b. When using the ±15 V supplies theses values were found to vary between 1024.6 (60.2 dB) and 372.6 (51.4 dB) between the low and high temperature extremes. Repeating the simulations using ±30 V supplies revealed an increase in gain at 25 °C and 400 °C to 9554.9 (79.6 dB) and 3179.4 (70.0 dB), respectively. The non-linear dependency of voltage gain on supply voltage is due to the cascading of the gain stages.

A plot of the closed-loop gain, A, given by Equation 5.18a normalised by the ideal

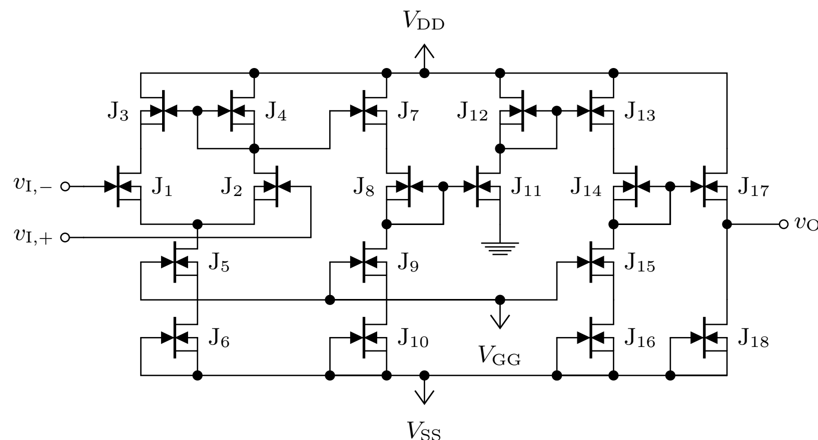


Figure 5.29

Schematic for the proposed 4H–SiC n-channel lateral depletion-mode JFET amplifier.

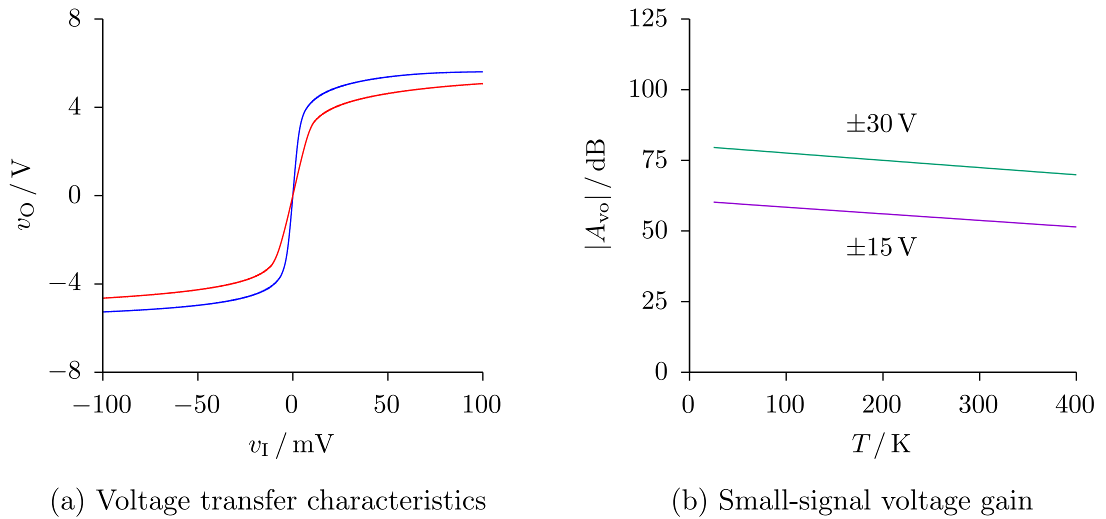


Figure 5.30

(a) Open-loop voltage transfer characteristic of the proposed 4H–SiC operational amplifier at 25 °C (blue line) and 400 °C (red line) using ±15 V supplies and (b) the corresponding low-frequency small-signal differential voltage gain between 25 °C and 400 °C using ±15 V or ±30 V supplies.

closed-loop gain of Equation 5.18b is given in Figure 5.31, from which it can be observed that Equation 5.18b is a reasonable approximation of Equation 5.18a, provided A_o can be made two orders of magnitude larger than B^{-1} at the highest temperature of interest. From Figure 5.30b it can be concluded that to maintain a relatively temperature insensitive closed-loop voltage gain up to 400 °C when using ±15 V or ±30 V supplies its value must be limited to approximately 5 and 30, respectively. If higher closed-loop voltage gains are required either an additional gain stage or one or more of the bootstrapping techniques presented in

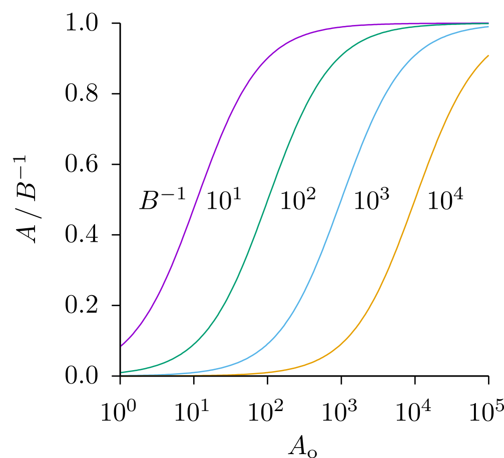
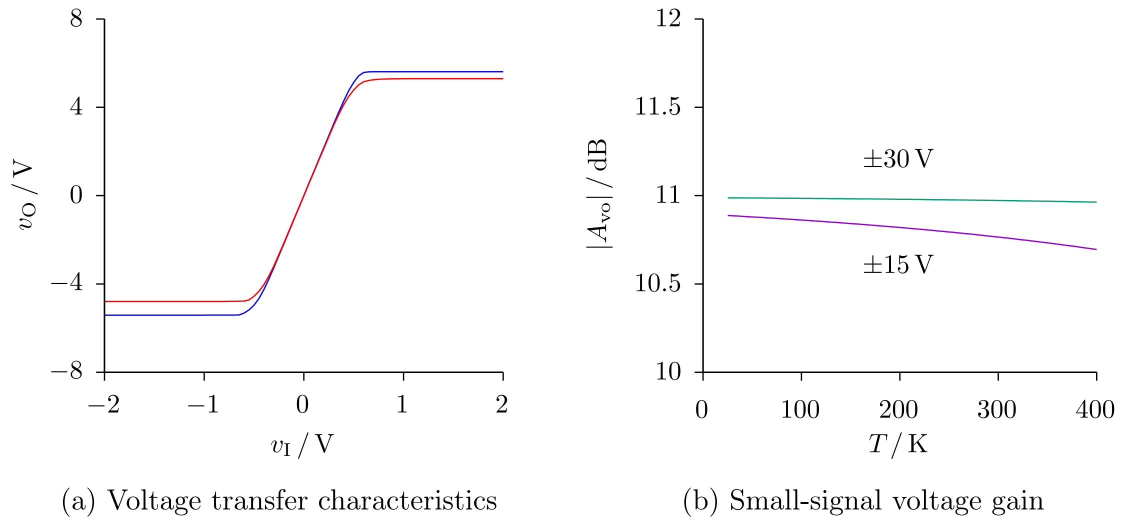


Figure 5.31

Closed-loop voltage gain, A, normalised by the feedback factor, B, as a function of open-loop voltage gain, A_o, and reciprocal feedback factor.



(a) Voltage transfer characteristics

(b) Small-signal voltage gain

Figure 5.32

(a) Closed-loop voltage transfer characteristic of the proposed 4H–SiC operational amplifier at 25 °C (blue line) and 400 °C (red line) using ±15 V supplies and (b) the corresponding low-frequency small-signal differential voltage gain between 25 °C and 400 °C using ±15 V or ±30 V supplies, for a reciprocal feedback factor of 11.

§2.4.2 can be included.

The op-amp circuit was subsequently configured into the close-loop arrangement of Figure 5.27 which in practice may be achieved through use of on chip epitaxial resistors. Resistance values where chosen to establish an ideal closed-loop voltage gain of 11. The simulated large-signal VTCs for 25 °C and 400 °C are presented in Figure 5.32a. The variation in voltage gain between the two temperature extremes is shown to be significantly reduced. The dependence on input single is also improved by the negative feedback, significantly increasing the linearity of the amplifier. The usable output swing at 400 °C is limited to approximately ±4 V, required for maintaining all devices in saturation. This may be improved by using higher voltage supplies, by reducing the amount of series resistance and though biasing the CS amplifier in the second gain stage to incorporate the negative supply range; the latter solution has the additional advantage of increasing the voltage gain. A comparison of the closed-loop small-signal voltage gain between 25 °C and 400 °C whilst using ±15 V and 30 V supplies is given in Figure 5.32b for an ideal gain of 11. The order of magnitude difference in open-loop gain at 400 °C when using these supply voltages is reflected in the amplifiers ability to established a constant value. The results suggest that the variation between 25 °C and 400 °C could be made much less than 1 %.

5.7 Summary

Pertinent IC compatible voltage amplifiers have been investigated using SPICE, employing the custom asymmetric twin-gated JFET compact model developed in §4.4, with model parameters matched to an experimental data set for a 4H–SiC 9 µm by 250 µm device. In

each case the DC output voltage, low-frequency small-signal voltage gain and output signal swing have be calculated in the temperature range 25 °C and 400 °C and qualified by their static and small-signal models. Reasonable and consistent supply voltages were adopted so as to achieve realistic values and facilitate comparison between topologies.

The influence of the body-effect was found to have devastating effect on the voltage gain and DC voltage stability of the circuits studied. Use of a lower doped body epilayer and large body-source reverse bias were found to reduce its impact; however, its degrading influence was noticeably present even for a simultaneous doping concentration and body-source bias as low as $9 \times 10^{14}\,\mathrm{cm}^{-3}$ and $-22.5\,\mathrm{V}$, respectively. Using device scaling and voltage feedback it was shown that a reasonable degree of OP stability could be achieved across a wide temperature range for the case of a CS amplifier. This design was, however, sensitive to process variations and continued to exhibit significantly reduced voltage gains compared with electrically isolated devices. More complex structures provided less favourable results. It was concluded that electrical isolation of devices using RIE was the most appropriate solution.

While passive loads were found to provide a relatively constant voltage gain over the full temperature range the low resistances required to achieve suitable OPs imposed serious restrictions on the values that could be attained; in the specific case of a CS amplifier with a 15 V supply the achieved value was close to −3. A 1.7 V variation in output bias further identifies them as an unsuitable choice for use in direct coupled op-amps. Conversely, replacing the resistor with an isolated DM JFET provided an open-circuit voltage gain of 33.4 (30.5 dB) and 20.7 (26.3 dB) at 25 °C and 400 °C, respectively, whilst maintaining a temperature invariant output bias of $V_{\mathrm{DD}}/2$. Inclusion of the body-effect was found to reduce the gain at 25 °C and 400 °C to just 5.53 and 5.13, respectively, with the additional consequence of introducing a 460 mV variation in DC output bias. The voltage gain was found to be approximately proportional to the ratio of the amplifying transistors transconductance and the active load's body-transconductance, preventing device scaling from being used to increase its value. Setting the body doping concentration and body-source bias to $9 \times 10^{14}\,\mathrm{cm}^{-3}$ and $-22.5\,\mathrm{V}$, respectively, and introducing negative voltage feedback to the load increased the gain to 14.7 and 12.1 at 25 °C and 400 °C, respectively, and reduce the bias variation to roughly 2 mV.

A differential amplifier with current-mirror load and DM JFET current-sink, formed from electrically isolated devices, was similarly able to provided differential voltage gains of 32.9 (30.3 dB) and 20.2 (26.1 dB) at 25 °C and 400 °C, respectively, from a ±15 V supply, while simultaneously providing differential to single-ended conversion. Current buffering was utilised to mitigate the finite output resistance of the the current-sink to provide corresponding CMRRs of 2296.39 (67.22 dB) and 895.66 (59.04 dB) at 25 °C and 400 °C, respectively. Thermal stability of the DC output voltage was achieved by ensuring identical bias voltages for each device through the appropriate selection of supply voltages.

A temperature and supply insensitive voltage level-shifter was also demonstrated, exhibiting low-freqency small-signal voltage gains of 0.97 and 0.95 at 25 °C and 400 °C, respectively. Bias point stability was again achieved by matching the biasing and thus temperature coefficients for each device.

Subsequently, a design was presented for a two-stage 4H–SiC op-amp comprised solely of NLDM JFETs. Low-frequency small-signal voltage gains of 9554.9 (79.6 dB) and 3179.4 (70.0 dB) were achieved at 25 °C and 400 °C, respectively, from a ±30 V supply. The close-loop voltage gain was shown to be essentially independent of temperature provided the open-loop voltage gain at the maximum temperature of interest is at least two orders of magnitude larger.

Configuring the op-amp as a non-inverting amplifier with an ideal closed-loop gain of 11 the value was found to change by just 1 % between 25 °C and 400 °C whilst significantly increasing the amplifier's linearity. Larger supply voltages, wider channel widths, shorter gate lengths, reduced series resistance and bootstrapping techniques where identified as means of further increasing the voltage gain.

CHAPTER

6

Final Remarks

6.1 Conclusions

This thesis has been concerned with addressing the demand for monolithically integrated signal conditioning electronics for hostile environment sensors systems utilising 4H–SiC. The junction field effect transistor (JFET) has been identified as the most suitable candidate for achieving this goal due to the relative stability of their majority carrier current with temperature, their insensitivity to radiation and their excellent junction isolation. Whilst a moderate body of pertinent research information exists the literature was found to be deficient in several key areas. The most important of these have be covered in this thesis, namely the electrical properties of 4H–SiC at high temperature, the development of a suitable compact model for integrated circuit (IC) 4H–SiC JFETs and the necessary requirements for circuits to operate consistently across a wide temperature range.

A discussion of the electronic band structure of 4H–SiC has identified the need for suitable material specific models for the purposes of carrier statistics and transport calculations. An analytic expression for the density of states (DOS) suitable for each of the relevant conduction bands has been developed based on a $\boldsymbol{k}\cdot\boldsymbol{p}$ approximation of the dispersion near their minima. This was subsequently used to provide appropriate expressions for the thermal equilibrium electron and hole concentrations in N and Al doped 4H–SiC subject to pertinent extrinsic effects. From these results a set of computationally efficient models have been developed that are suitable for use in Simulation Program with Integrated Circuit Emphasis (SPICE) compact models. Such models are of great utility for describing important electronic properties of 4H–SiC, including the free carrier concentrations and p-n junction built-in potentials, in areas where low computational overhead are important. The scope of the approximation do, however, extends far beyond use in SPICE. Appropriate expression for the DOS effective mass have also been developed that allow the influence of band non-parabolicity and occupation of high energy bands to be accounted for in many of the existing expressions developed under the assumption of single parabolic bands.

The influence of multiple non-parabolic conduction bands on the low-field transport properties of electrons in 4H–SiC has also been covered. Appropriate weighting functions for the momentum relaxation time and conductivity effective mass have been identified and should replace those currently found in 4H–SiC literature that assume parabolic bands. A

key finding was that the effective mass in each conduction band for all directions on the basal plane is the arithmetic mean of the principle axis effective mass tensor components parallel to the plane. The similarity of this value in the lowest two bands means the statistical average value at any temperature should remain fairly constant irrespective of temperature and electric field strength. Conversely, the non-parabolic conduction band dispersion in the direction of the principle axis was found to introduce a temperature dependence to the effective mass, causing its expectation value to increase roughly linearly by 19% and 21% between 25 °C and 400 °C in the first and second conduction bands, respectively. The derived expressions in context with a two band conductivity model provide much needed insight into the temperature dependence of the electron transport properties in 4H–SiC currently overlooked in the literature.

N-channel lateral depletion-mode (NLDM) JFETs with gate lengths of 9 µm and gate widths of 250 µm have been realised using a commercial n-type 4H–SiC wafer with three layers of homo epitaxy and conventional planer processing techniques. The fabricated devices displayed excellent long channel device characteristics with turn-off voltages and current densities consistent with bulk theory. The experimental measurements strongly support the suitability of 4H–SiC NLDM JFETs for developing IC analogue amplifiers suitable of operation at temperatures as high as 400 °C.

Annealed Ni/Ti contacts on $2 \times 10^{19}\,\mathrm{cm}^{-3}$ doped N implanted layers provided sufficiently low contact resistance to the channel epilayer. Horizontal current flow through the contact side wall and the difference in sheet resistance under the contact were found to increase the calculated values of the specific contact resistance determined from transfer length method (TLM) test structures by as much as 10%. The lowest recorded value of specific contact resistance was $1.90(50) \times 10^{-5}\,\Omega\,\mathrm{cm}^2$ with a corresponding sheet resistance of $7.89(9) \times 10^2\,\Omega/\square$. Inhomogeneity in sheet resistance and specific contact resistivity across the sample was attributed to known processes variations that can be mitigated in large scale production.

An accurate compact model has been developed in the framework of the gradual channel approximation (GCA) that is suitable for describing the electronic characteristics of the NLDM JFETs under study. Notable features include electric field dependent mobility, asymmetric twin gate operation and SiC specific parameter thermal models. Efficient empirical corrections to the GCA near to and above pinch-off capable of close agreement with experiment were presented that are highly suitable for compact modelling. The compact model was successful in quantitatively accounting for the large variation of the channel current cause by the body-effect present in both experimental measurements and technology computer aided design (TCAD) simulations. A number of 4H–SiC material parameters pertinent to describing the operation of bulk devices have studied and suitable mathematical thermal models have been presented that are suitable over the full range of temperatures between 25 °C and 400 °C. Comparisons with experimental results have demonstrated excellent agreement for a wide range of gate, body and channel biasing and temperatures.

SPICE simulations employing the aforementioned compact model with model parameters matched to an experimental data set for a 4H–SiC non-self aligned 9 µm long by 250 µm wide gate length device have been performed with measurements of the direct current (DC) output voltage, low-frequency small-signal voltage gain and output signal swing in the tem-

perature range 25 °C and 400 °C reported. The influence of the body-effect was found to have devastating effects on the voltage gain and DC voltage stability of all circuits studied. Low body epilayer doping and large body-channel reverse biases were proposed to limit its impact; however, further SPICE simulations predicted a significant influence even for concentrations and junction bias as low as $9 \times 10^{14}\,\mathrm{cm}^{-3}$ and $-22.5\,\mathrm{V}$, respectively. Current-mirroring circuits were suggested as a suitable option for attaining DC stability in the presence of the body-effect providing stable voltage references can be developed. Unfortunately, this will fail to account for the prominent reduction in gain and the effectiveness of gain enhancing bootstrapping techniques. Electrical isolation of devices by reactive ion etching (RIE) was suggested as a practical option for elimination all of the resulting effects.

Passive loads were found to provide a relatively constant voltage gain over the full temperature range. Unfortunately, their values are too low for the majority or desired applications and resulted in larger variation in the DC bias point at the output. Matched depletion mode (DM) JFETs were shown to be suitable for providing suitably high voltage gain equal to half the intrinsic JFET gain of either device, while achieving a stable output bias voltage at all temperatures of interest. A differential amplifier with positive feedback was shown to provide the necessary differential to single-ended output conversion, with the resulting differential voltage gain in close agreement with theory.

A design for a two-stage 4H–SiC operational amplifier (op-amp) using a culmination of the individual circuits previously covered was lastly presented. Low-frequency small-signal voltage gains of 9554.9 (79.6 dB) and 3179.4 (70.0 dB) were achieved at 25 °C and 400 °C, respectively, from a ±30 V supply. By selecting an ideal value of closed-loop gain at least two orders of magnitude lower than the op-amp's open-loop gain at the maximum temperature of interest a gain variation of less than 1 % was achieved between 25 °C and 400 °C. Larger supply voltages, wider channel widths, shorter gate lengths and smaller non-self alignment resistance where identified as means of further increasing the voltage gain without the need for redesigning the circuit.

6.2 Future Work

This work has been highly successful in addressing the major barriers for the development of hostile environment electronics based on SiC JFETs. It also provides a excellent framework for further work. A few pertinent areas where extended study should be made are described below.

The proposed JFET compact model has so far been very successful in describing the electrical properties of the fabricated NLDM devices. While efficient, the use empirical parameters to describe the output current and dynamic resistance in saturation does unfortunately place a large emphasis on curve fitting techniques which provides little insight in device behaviour in this region. Such values cannot be accurately determined *a priori* and thus requires that devices first be fabricated and characterised before appropriate values can be determined. Further study of the two-dimensional effects close to and above pinch-off is therefore desirable provided sufficiently efficient models can be derived.

Circuit performance depends greatly on the device specifications. For example the chan-

nel depth plays a major role in determining the channel voltage to achieve current saturation. Voltage burdens significantly limit the output voltage swing of an amplifier and imposes a minimum supply range on a circuit. Device designs should thereby be selected to better corresponding with their intended application. The voltage burden can be further minimised through reduction of the non-self alignment resistances; ideally a self-aligned process should be used.

While the models developed can account for dynamic effects the discussion has so far been limited to low-frequencies. The motivation for this decision was that bias point stability was one of the primary points of interest. The effect of parasitic capacitance and the inclusion of Miller compensation are discussed in great detail in related textbooks.

In order to attain a fundamental understanding of the device behaviour the applications and discussions have been limited to few simple examples. While meeting the necessary criteria for low-frequency operation over a wide temperature range more work should be performed to optimise op-amp voltage gain. Many of the bootstrapped topologies capable of enhancing voltage gain can be adopted for this purpose whilst still maintaining thermal stability. One criticism of the proposed op-amp design, that can be corrected for, is that the swing of the last gain stage does not utilise the negative supply voltage. This has the effect of significantly reducing the signal swing and voltage gain. In reality the the DC input to the common source (CS) amplifier can be brought very close to the negative rail, provided negative common-mode voltage is not of interest. This can be done through the use of current mirroring, but first requires stable voltage level-shifter circuits to be developed.

Lastly, process variability is known to have a significant effect on the performance of SiC ICs, in large part due to the inconsistencies of the semiconductor epilayers. Following a dedicated study of this variability, it will be possible to included these influences in future circuit simulations in order to assess their impact of proposed designs.

APPENDIX

A

Device Photomask Outlines

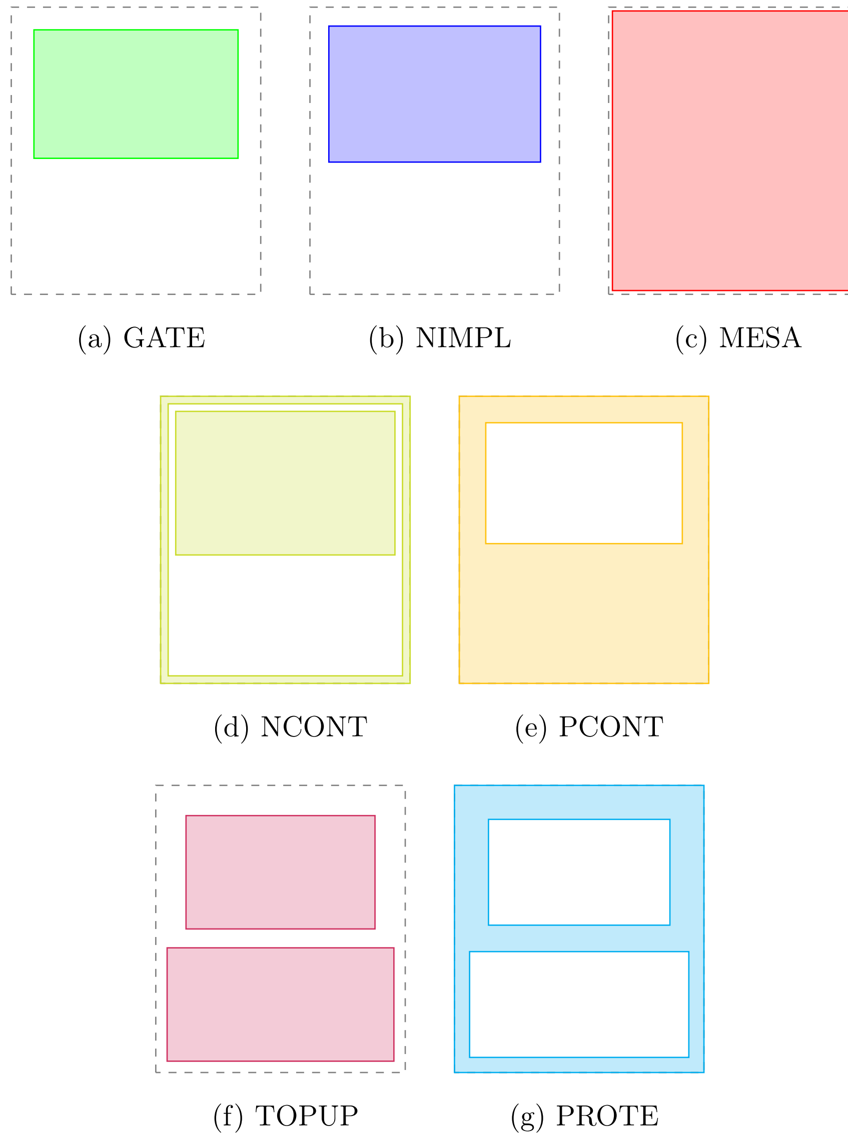


Figure A.1
Photomask outline for the lateral p-n junction diode used in this study (1:100 scale).

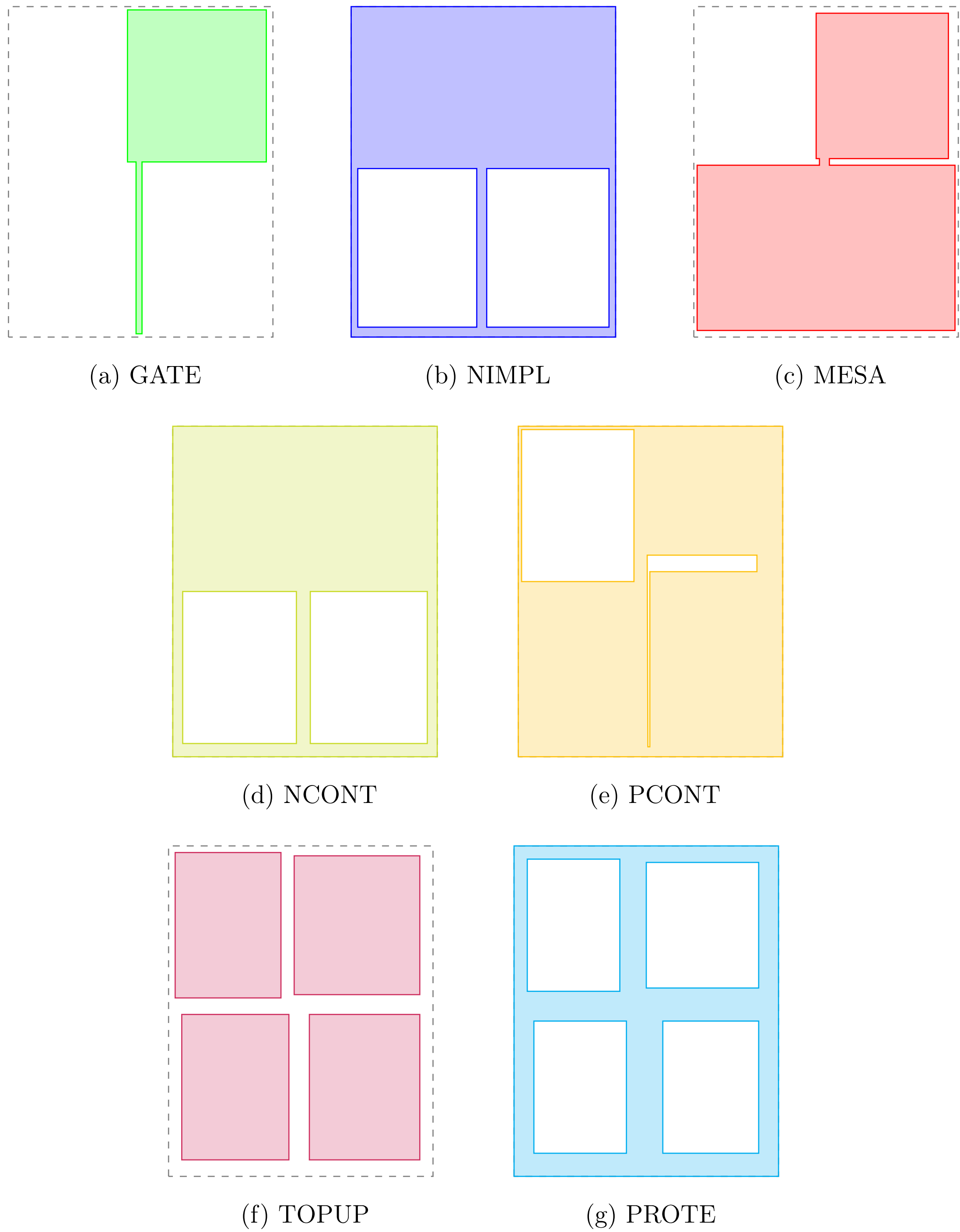


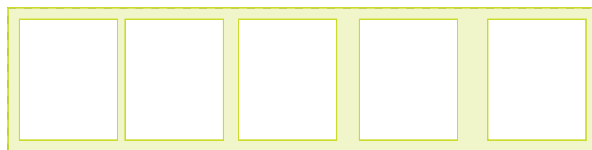
Figure A.2

Photomask outline for the non-self aligned JFET with 9 µm gate length and 250 µm gate width used in this study (1:100 scale).

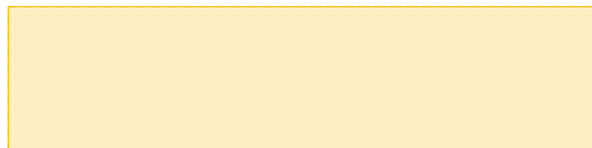
(a) GATE

(b) NIMPL

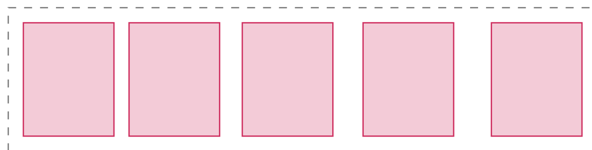
(c) MESA



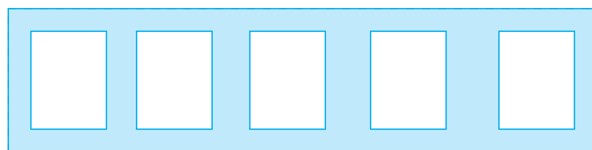
(d) NCONT



(e) PCONT

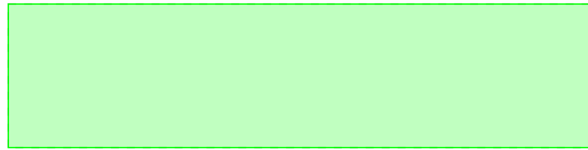


(f) TOPUP



(g) PROTE

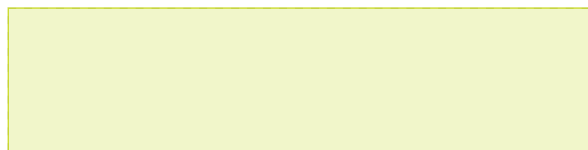
Figure A.3
Photomask outline for the channel implant TLM structure used in this study (1:100 scale).



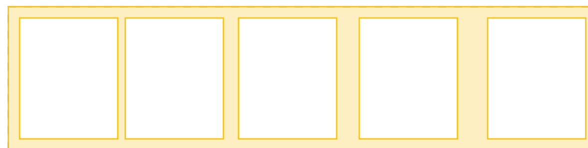
(a) GATE

(b) NIMPL

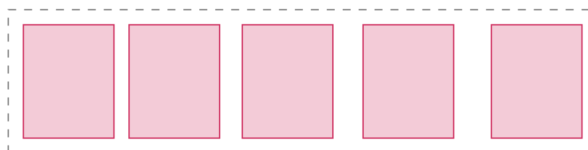
(c) MESA



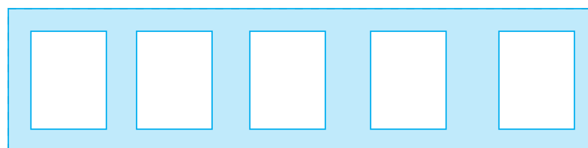
(d) NCONT



(e) PCONT



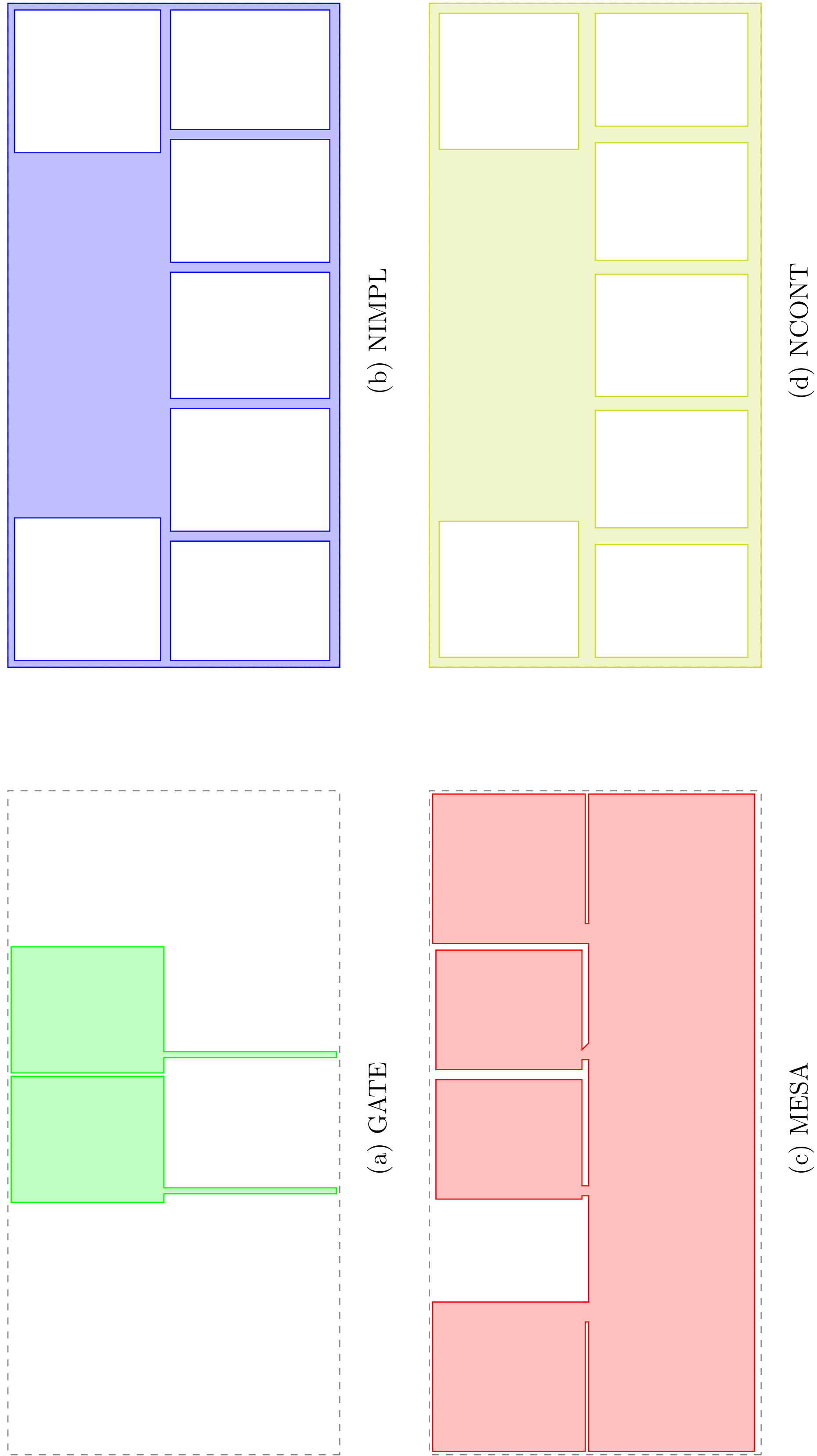
(f) TOPUP



(g) PROTE

Figure A.4

Photomask outline for the gate epilayer TLM structure used in this study (1:100 scale).



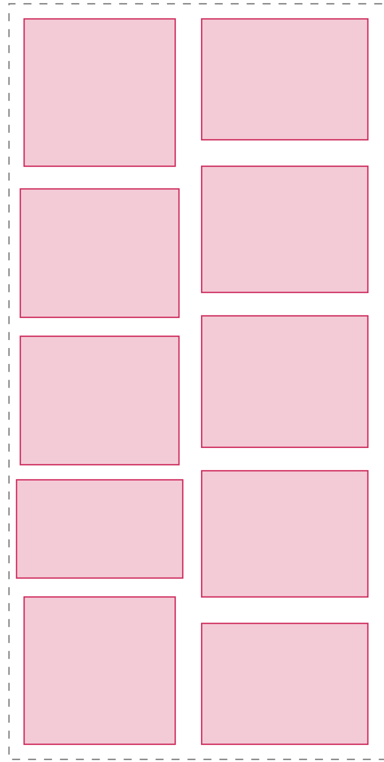
(a) GATE

(b) NIMPL

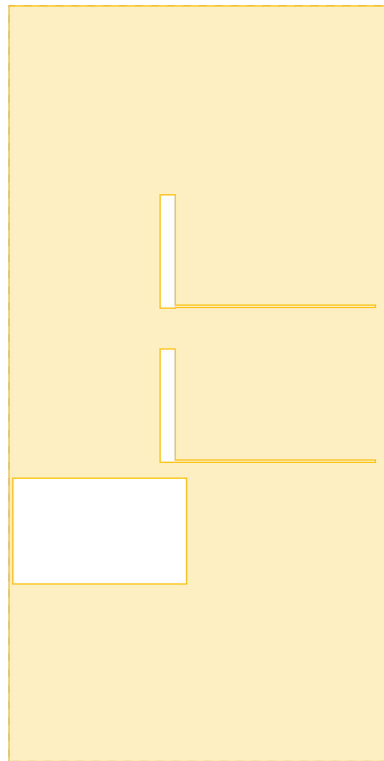
(c) MESA

(d) NCONT

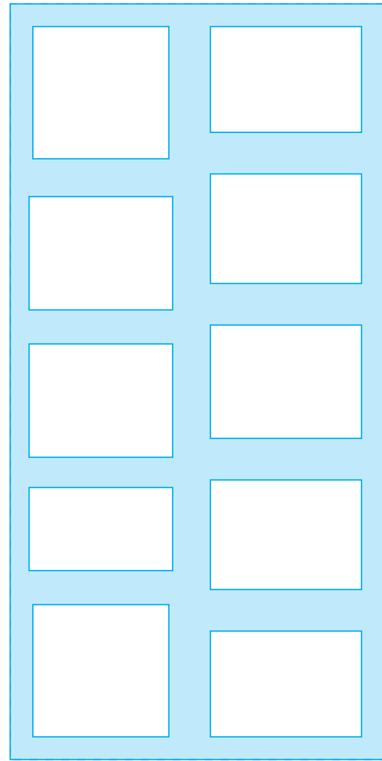
Figure A.5
Photomask outline for a JFET differential pair with passive loads used in this study (1:100 scale).



(f) TOPUP



(e) PCONT



(g) PROTE

Figure A.5

Photomask outline for a JFET differential pair with passive loads used in this study (1:100 scale) (cont.).

APPENDIX

B

SPICE Model Parameters

Table B.1

Model parameters for the proposed JFET compact model, including pertinent extracted values determined form curve fits to experimental data between 25 °C and 400 °C.

Parameter	Symbol	Description	Unit	Value
`level`		channel model	1	2
`capop`		capacitance model	1	1
`tref`		reference temperature	°C	25.0
`lscale`		channel length scale	1	1.0
`wscale`		channel width scale	1	1.0
`g0`	G_0	open-channel conductance	S	5.65×10^{-3}
`phi0t`	$\phi_{0,\mathrm{t}}$	gate-channel contact potential	V	2.92
`phi0b`	$\phi_{0,\mathrm{b}}$	bulk-channel contact potential	V	2.82
`phipt`	$\phi_{\mathrm{p,t}}$	gate-channel pinch-off voltage	V	8.67
`phipb`	$\phi_{\mathrm{p,b}}$	body-channel pinch-off voltage	V	279
`xi`	Ξ	field dependent mobility factor	V^{-1}	3.13×10^{-2}
`lambda`	λ	channel-length modulation factor	V^{-1}	2.51×10^{-2}
`gamma`	γ	channel-length modulation factor	V^{-1}	9.68×10^{-2}
`chi`	χ	expop smoothing factor	1	2.33×10^{-1}
`rd`	R_c	drain contact resistance	Ω	42.7
`rg`	R_c	gate contact resistance	Ω	
`rs`	R_c	source contact resistance	Ω	42.7
`rb`	R_c	body contact resistance	Ω	
`xd`	$\hat{x}_\mathrm{d}$	drain non-self alignment relative length	1	3.85×10^{-1}
`xs`	$\hat{x}_\mathrm{s}$	source non-self alignment relative length	1	3.85×10^{-1}
`yds`	$\hat{y}_\mathrm{ds}$	non-self alignment relative depth	1	0 9
`ist`	I_s	gate-channel reverse saturation current	A	
`isb`	I_s	body-channel reverse saturation current	A	

Table B.1

Model parameters for the proposed JFET compact model, including pertinent extracted values determined form curve fits to experimental data between 25 °C and 400 °C. (cont.)

Parameter	Symbol	Description	Unit	Value
alphat	α	gate-channel carrier injection ratio	1	
alphab	α	body-channel carrier injection ratio	1	
cj0t	$C_{\mathrm{j,0}}$	gate-channel zero-bias capacitance	F	
cj0b	$C_{\mathrm{j,0}}$	body-channel zero-bias capacitance	F	
fc	FC	forward bias capacitance coefficient	1	
delta1	Δ_1	capacitance smoothing factor	V	
delta2	Δ_1	capacitance smoothing factor	V	
g0_tc1		open-channel conductance tempco	1	-2.59
g0_tc2		open-channel conductance tempco	1	7.24
g0_tc3		open-channel conductance tempco	1	1.87×10^{-1}
na	N_{a}	gate epilayer dopant concentration	m^{-3}	2.10×10^{25}
nac	N_{d}	gate epilayer dopant compensation	m^{-3}	1.00×10^{23}
nd	N_{d}	channel epilayer dopant concentration	m^{-3}	1.05×10^{23}
ndc	N_{a}	channel epilayer dopant compensation	m^{-3}	2.00×10^{21}
nb	N_{a}	body epilayer dopant concentration	m^{-3}	4.00×10^{21}
nbc	N_{d}	body epilayer dopant compensation	m^{-3}	1.00×10^{21}
phip_tc		pinch-off voltage tempco	$°\mathrm{C}^{-1}$	-2.96×10^{-5}
xi_tc		field dependent mobility factor tempco	1	-8.78×10^{-2}
lambda_tc		channel-length modulation factor tempco	$°\mathrm{C}^{-1}$	3.39×10^{-4}
gamma_tc		channel-length modulation factor tempco	$°\mathrm{C}^{-1}$	-4.40×10^{-4}
chi_tc		expop smoothing factor tempco	$°\mathrm{C}^{-1}$	-1.51×10^{-3}
rd_tc		drain contact resistance tempco	$°\mathrm{C}^{-1}$	1.25×10^{-2}
rg_tc		gate contact resistance tempco	$°\mathrm{C}^{-1}$	
rs_tc		source contact resistance tempco	$°\mathrm{C}^{-1}$	1.25×10^{-2}
rb_tc		body contact resistance tempco	$°\mathrm{C}^{-1}$	

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