Power Quality Improvements of Single-phase Grid-connected Photovoltaic Systems

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A thesis submitted for the degree of

Doctor of Philosophy

May, 2017

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To my Father, and my Mother

الى الوالد والوالدة أطال الله في عمرهما

Abstract

The number of distributed power generation systems (DPGSs), mostly based on photovoltaic (PV) energy sources is increasing exponentially. These systems must conform to grid codes to ensure appropriate power quality and to contribute to grid stability. A robust and reliable synchronization to the grid is an important consideration in such systems. This is due to the fact that, fast and accurate detection of the grid voltage parameters is essential in order to implement stable control strategies under a broad range of grid conditions. The second-order generalized integrator (SOGI) based phase-locked loop (PLL) is widely used for grid synchronization of single-phase power converters. This is because it offers a simple, robust and flexible solution for grid synchronization. However, the SOGI-PLL is affected by the presence of a dc offset in the measured grid voltage. This dc voltage offset is typically introduced by the measurements and data conversion process, and causes fundamental-frequency ripple in the estimated parameters of the grid voltage (i.e. voltage amplitude, phase angle and frequency). In addition to this ripple, the unit amplitude sine and cosine signals of the estimated phase angle (i.e. unit vectors), that are used to generate reference signals in the closed-loop control of grid-connected PV converters will contain dc offset. This is highly undesirable since it can cause dc current injection to the grid, and as a consequence, the quality of the power provided by the DPGSs can be degraded. To overcome this drawback, a modified SOGI-PLL with dc offset rejection capability is proposed. The steady-state, transient and harmonic attenuation performance of the proposed PLL scheme are validated through simulation and experimental tests. The overall performance demonstrates the capability of the proposed PLL to fully reject such dc current injection as well as to provide a superior harmonic attenuation when compared with the SOGI-PLL and two other existing offset rejection approaches. It is shown that, the proposed PLL scheme can enhance the overall total harmonic distortion (THD%) of the injected power by 15% when compared to the conventional SOGI-PLL.

In addition to the synchronization, grid-connected PV systems require a current control scheme to regulate the output current. Due to the simple implementation, proportional-integral (PI) controllers in the stationary reference frame are commonly used for current controlled inverters. However, these PI-controllers exhibit a major drawback of failure to track a sinusoidal reference

without steady-state error, which may result in low-order harmonics. This drawback can be overcome if the PI-controllers are implemented in direct-quadrature (*dq*) rotating reference frame. In single-phase systems, the common approach is to create a synthesized phase signal orthogonal to the fundamental of the real single-phase system so as to obtain dc quantities by means of a stationary-to-rotating reference frame. The orthogonal synthesized signal in conventional approaches is obtained by phase shifting the real signal by a quarter of the fundamental period. The introduction of such delay in the system deteriorates the dynamic response, which becomes slower and oscillatory. This thesis proposes an alternative way of implementing such PI-controllers in the *dq* reference frame without the need of creating such orthogonal signals. The proposed approach, effectively improves the poor dynamic of the conventional approaches while not adding excessive complexity to the controller structure. The results show that, in addition to its ability to regulate the current and achieve zero steady-state error, the proposed approach shows superior dynamic response when compared with that of conventional delay-based approach.

Acknowledgements

First and foremost, Praise is to God (Allah), the most merciful and the most gracious, who gives me wisdom, strength and patience to complete this work. The author would like to take this chance to express sincere gratitude to those who have made this thesis possible.

I would like to thank the Libyan Government, as without their funding this work would not have been carried out. I am always indebted to my country Libya.

I acknowledge with deepest appreciation; the outstanding guidance, intellectual support and encouragement provided by my supervisor, Dr. David Atkinson, whose knowledge, and patience, added considerably to my research project. It was such a pleasant experience to work with Dave and learn from his expertise and experience in the field of control of grid-connected power converters which helped me through many difficulties.

Very special thanks are due to Dr Mohamed Dahidah for his valuable advice and consistent encouragement. His constructive notes always resulted in improvements to my work.

I would also like to acknowledge the significant contribution of Darren Mackie throughout the project; for his considerable help with the assembly of the electronic hardware. Also, special acknowledgement must also go to Gill Webber, the postgraduate research coordinator, for her support and great help.

Many thanks also go to my valuable friends in the UG lab, for their friendship and help throughout and in particular for the great time we have spent together.

My heartfelt appreciation goes to my first ever teachers in this life, my parents for their support and encouragement throughout my life. Without their constant assistance, prayers and blessings, I would not have reached this level of education.

Finally, the warmest thanks go to my wife, for her quiet patience, daily devotion and unwavering love. I am also indebted to my children; Moody, Jody, and little one Abdul for their warm hugs and lovely smiles every morning. I would like to say to them that from now on, we will enjoy more time together.

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Symbols

Symbol	Definition
AC	Alternating Current
A/D	Analogue to Digital Conversion
ADC	Analogue to Digital Converter
APOD	Alternative Phase Opposition Disposition
AI	Anti-islanding
BPF	Band-pass Filter
CHB	Cascaded H-Bridge
CLPF	Cascaded Low-pass Filter
CLTF	Closed-loop Transfer Function
DPGSs	Distributed Power Generation Systems
DQ	Direct-quadrature
DFAC	Double-frequency and Amplitude Compensation
DC	Direct Current
DSP	Digital Signal Processor
DAC	Digital to Analogue Converter
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interface
FC	Flying Capacitor
GUI	Graphical User Interface
IPD	In-phase Disposition
LPF	Low-pass Filter
LS-PWM	Multi-carrier Level-shifted PWM
LF	Loop Filter
MPPT	Maximum Power Point Tracing
MMPD	Modified Mixer Phase Detector
MOSFET	Metal Oxide Field Effect Transistor
NPC	Neutral Point Clamped
OLTF	Open-loop Transfer Function
OSG	Orthogonal Signal Generator

PCB	Printed Circuit Board
PQ	Active and Reactive Power Controller
POD	Phase Opposition Disposition
PV	Photovoltaic
PCC	Point of Common Coupling
PI	Proportional-Integral
PR	Proportional–Resonant
PLL	Phase-locked Loop
PWM	Pulse Width Modulation
pPLL	power-based phase-locked loop
PS-PWM	Multi-carrier Phase-shifted PWM
PD	Phase Detector
PVD	Peak Voltage Detection
PM	Phase Margin
RRF	Rotating Reference Frame
S_tRF	Stationary Reference Frame
SRF	Synchronous Reference Frame
SPWM	Multi-carrier Based Pulse Width Modulation
SHE-PWM	Selective Harmonic Elimination
SVM	Multilevel Space Vector Modulation
SPGC	Single-phase Grid-connected Converter
SOGI	Second-order Generalized Integrator
SO	Symmetrical Optimum
SPI	Serial Peripheral Interface
THD	Total Harmonic Distortion
T-PDs	Transformation-based Phase Detectors
VSC	Voltage-source Converter
VSI	Voltage-source Inverter
VCO	Voltage-controlled Oscillator
WD	Window Detector
ZCD	Zero-crossing Detection

CHAPTER 1

INTRODUCTION

1.1 Introduction

During the last decade, renewable energy sources have attracted most of the attention as a promising means to tackle the energy, sustainability and environmental concerns being faced today worldwide [1, 2]. Among these energy sources, the photovoltaic (PV) technology has been regarded as an environmentally friendly alternative energy source and has advanced considerably in recent years. As depicted in Figure. 1.1, over the past decade, the number of PV installations with the majority being grid-connected has experienced extraordinary growth. For example, the total installed global capacity grew from 177 GW installed in 2014 to reach 227.1 GW by the end of 2015 [3].

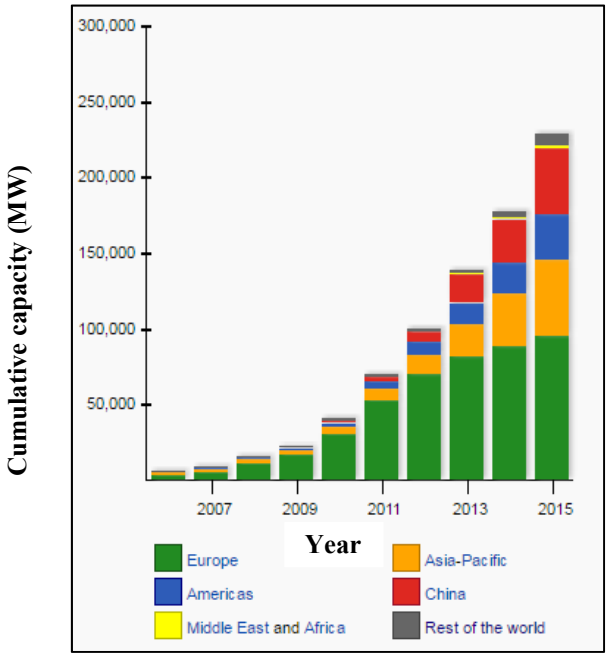


Figure 1.1. The worldwide cumulative installed PV power in MW according to IEA [3]

Nowadays, and due to the necessity of producing and delivering more reliable, flexible and clean energy technologies, the electrical power providers are turning toward distributed power generation systems (DPGSs). In such systems, a large number of small-scale electricity generation units mostly from renewable energy resources such as, roof-mounted photovoltaic

and wind generation systems are integrated into power systems at distribution level [1, 2, 4]. Recently, the number of distributed power generation systems (DPGSs) has reached significant penetration levels and are expected to become increasingly predominant in the near future [2, 5-7]. In such systems, the enabling technology of power electronic converters and associated control are utilized to perform different tasks. In addition to providing high-quality power to the electricity network, these systems should actively contribute to grid stability by supporting voltage/frequency under different grid conditions [8-10]. However, the action of interfacing such systems to the utility grid, can seriously affect the grid stability, power-quality and safety conditions if these systems are not appropriately controlled [2, 7, 11]. This issue has become of great concern to electricity supply companies, and as a consequence, new and more stringent standards have been in force. This is in respect of how these power sources interact with the grid, to ensure the power quality of the network is not compromised [11-14]. Accordingly, more attention should be given on ways of advancing the control strategy used in grid-connected power converters. Such a control strategy should be able to ensure that power extracted from renewable energy sources and transmitted to the grid-side does not violate the modern grid codes and standards [15]. Generally, this control strategy consists of, a synchronization unit to ensure fast and precise grid synchronization, and a current controller to enable a high-quality current injection [2, 7].

Synchronization is one of the most important aspects to be considered in the control of power converters interfacing renewable energy sources to the utility grid [16-19]. Grid-connected converters should be appropriately synchronized with the network and stay actively connected, supporting the grid services and maintaining the generation up under many different grid conditions [10, 20]. In such conditions, an accurate and fast detection of phase angle, frequency and amplitude of the grid voltage is an essential requirement for effective operation and control of the grid-connected converters [21]. Thus, grid voltage variables should be continuously monitored at the point of common coupling (PCC). This is to confirm the suitability of the network state for a correct operation of power converters, also to set the energy transfer between the power converter and the utility grid accordingly [11]. In addition to the synchronisation issue, regulating the current injected into the utility grid using advanced current control strategies is another very important feature to be investigated. Typically, the performance of such a current controller relies heavily on the estimated amplitude and phase-angle of the grid voltage, thus, it is greatly affected by the response of the synchronization algorithm. As a

consequence, the quality of the injected power from renewable energy sources under different grid disturbances, can be effectively enhanced by adopting a more robust synchronization method.

1.2 Project Motivation

This thesis is concerned with research into grid-connected photovoltaic (PV) systems, specifically low-power single-phase PV 'roof-mounted' systems. In such systems, the synchronization is normally performed using phase-locked loop (PLL) algorithms. The PLL as a key component in grid-connected systems will impact the power quality, stability and reliability of the power conversion system. Accordingly, the PLL used in the synchronization of PV inverters with the grid should be carefully designed to achieve optimal steady-state and transient response. Most of the previous studies have dealt with the performance developments of PLL algorithms under various disturbances in the grid voltage such as harmonics, voltage dip, frequency deviations and phase-angle jumps. However, errors generated from the grid voltage measurement circuits e.g. DC offset, can seriously affect the response of the PLL, and as a consequence, the entire performance of the grid-connected PV system may be degraded. For this reason, there is obviously considerable motivation to enhance grid-connected PV inverter performance through the use of more robust PLL algorithm that can estimate the grid voltage variables more accurately under different grid disturbance conditions including the presence of such a dc offset.

In addition to the synchronization algorithm, grid-connected PV inverter systems generally require a current control scheme to regulate their output current as well as to provide a high-quality power exchange with the utility grid. Owing to their simple structure and digital implementation, PI-controllers in the stationary reference frame are considered as the most conventional approaches used for current controlled inverters. However, because of the time-varying nature of the quantity being controlled, these PI-controllers have a major drawback of the inability to track a sinusoidal reference without steady-state error [22, 23]. This drawback can be overcome if the PI-controller is implemented in the synchronous reference frame (SRF) instead. In an SRF, usually referred to as a *dq* frame, ac (time varying) quantities appear as dc (time invariant) quantities. This allows the controller to be designed as would be for dc–dc converters, presenting infinite control gain at the steady-state operating point, and leading to zero steady-state error [24, 25]. The *dq*-controller has been very effectively used for the current

control of three-phase systems to obtain zero steady-state [25-28]. However, they encounter shortcomings when utilized in single-phase systems. In such systems, the use of a *dq*-controller is not possible unless a fictitious quadrature signal is produced to form a two-axis environment (i.e.,$\alpha\beta$) [24, 29]. Thus, in this regard, a new way of implementing such PI-controllers in the *dq* reference frame without the need for creating such a fictitious quadrature signal is proposed.

To assess where photovoltaic system performance can be improved, however, it is necessary to understand the typical operation of a grid-connected PV inverter system. This will therefore be the focus of the following discussion.

1.3 Typical Operation of a Grid Connected PV Inverter System

As illustrated in Figure.1.2, a grid-connected photovoltaic power system can be defined as the interface between the PV array and the utility grid system through two power stages. In the first stage, a DC/DC boost converter is employed to step up the relatively low PV array output DC voltage to a convenient level accepted by the DC/AC inverter. A maximum power point tracking (MPPT) controller is normally implemented in this stage, for maximizing the energy capture. While in the second stage, a power inverter that operates in a current controlled mode is involved to efficiently and reliably inject unity power factor sinusoidal current into the utility grid. A low-pass filter (LPF) is placed at the output of the inverter to attenuate any high frequency harmonics can be generated by the pulse width modulation (PWM) used to control the inverter. Finally, a 50Hz isolation transformer is typically presented at the inverter output to primarily provide an isolation barrier between the grid-connected PV inverter and the utility grid. It also serves to exclude DC current injection into the grid. It is worth mentioning that, different grid-connected PV system configuration such as centralized, string and multi-string have been described in the literature [6].

Throughout this thesis, the DC link voltage V_{dc} of the DC/AC converter is assumed to be fixed at a desired level, thus, the first power stage described above will not be considered in the real time implementation of the grid-connected PV system. Therefore, the main focus of this research is more on the AC side of the grid-connected PV inverter system.

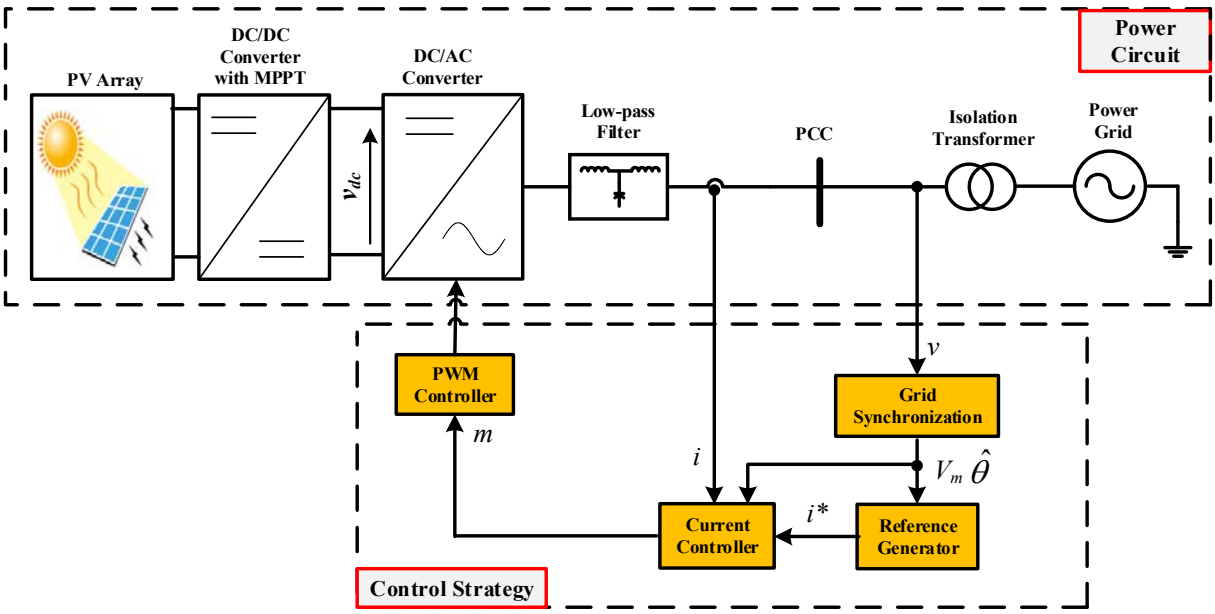


Figure 1.2.Typical Grid Connected Photovoltaic Inverter System along with its associated control strategy

where: v, V_m, $\hat{\theta}$,i, i^* and m are the measured grid voltage, estimated grid voltage amplitude, estimated phase-angle, measured grid current, demand current and modulation index respectively.

1.3.1 The choice of the DC/AC Inverter

In single-phase grid-connected PV systems, two-level voltage-source inverters (VSIs) are commonly used as a key element that converts DC power generated by PV arrays into grid-synchronized AC power. Typically, VSIs operate with relatively high PWM switching frequency, generating voltage waveforms with harmonic content around the switching frequency and its multiples. These voltages may lead to undesirable current harmonics flowing into the grid. Such harmonics are not desirable because they can increase losses, and disturb other sensitive devices/loads connected to the point of common coupling (PCC) of the grid. Therefore, it is of paramount importance to connect the output of such inverters to an adequate low-pass filter to limit such harmonics to desirable limits specified in [12]. The size of the output filter can be effectively minimized if the conventional two-level inverter is replaced by a multilevel inverter. This is due to the fact that; multilevel inverters are able to produce a more refined staircase wave with reduced harmonic distortion. Over the last years, several different multilevel converter topologies have been reported in the technical literature [30-35]. The most

established topologies are, the neutral point clamped (NPC) or diode clamped [36], the flying capacitor (FC) or capacitor clamped [37], and the cascaded H-bridge (CHB) [38]. Among these, the diode-clamped and cascaded-H-bridge are widely used in renewable energy applications due to their structure [39-42]. Accordingly, in this thesis, a five-level diode-clamped inverter is chosen as a part of the proposed single-phase grid-connected PV system shown in Figure. 1.2. The main objective is to investigate the possibility of reducing the passive filter requirements by adopting such an inverter. As it will be demonstrated, adopting the five-level inverter can reduce the size of the output filter by approximately four times when compared to that of the two-level inverter. In the following section, an overview of the five-level inverter structure, operation, and modulation strategy used will be briefly introduced. Further details on the five-level inverter can be found in Appendix A.

1.3.1.1 *Five-level Diode-clamped Inverter*

The circuit diagram of the five-level diode-clamped inverter used in the proposed single-phase grid-connected PV system is shown in Figure. 1.3. The inverter consists of eight active switches with four series-connected dc capacitors. For simplicity, it is assumed throughout this thesis that, the DC-link capacitor voltage V_{dc} is fixed at a desired level and equally divided by the dc capacitors. This means that, the voltage across each dc capacitor is equal to $V_{dc}/4$, and the voltage stress of each switching device will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes (d_1-d_6). Practically, this can be achieved by connecting in series four independent ideal DC power supplies as described in Chapter 6.

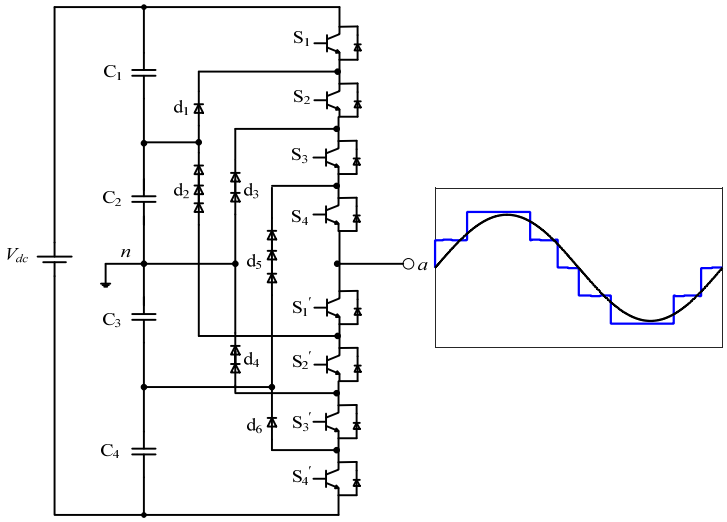


Figure 1.3. Single-phase five-level diode-clamped inverter used in the proposed grid-connected PV system

The relationship between switch operating status and the inverter terminal voltage Van is summarized in Table 1-1. Note that, the gate signal is of binary nature, where '0' indicates that an active switch is OFF, while '1' signifies that the switch is ON. There are five switch combinations where only four consecutive switches are always switched on simultaneously to synthesize five different voltage levels across the AC output of the inverter (i.e., *a* and *n*). For instance, when the top four switches are turned on (S_1-S_4), $V_{an} = V_{dc}/2$, whereas the conduction of the bottom four switches ($S_{1'}$-$S_{4'}$) results in $V_{an} = -V_{dc}/2$.

Table 1-1 Switching state and magnitude of output voltage of a five-level diode-clamped inverter

Switching State Number	Switching States								Output voltage V_{an} (V)
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	
1	1	1	1	1	0	0	0	0	$V_{dc}/2$
2	0	1	1	1	1	0	0	0	$V_{dc}/4$
3	0	0	1	1	1	1	0	0	0
4	0	0	0	1	1	1	1	0	$-V_{dc}/4$
5	0	0	0	0	1	1	1	1	$-V_{dc}/2$

In addition, it is important to notice that, although each active switch is required to block only a voltage equal to that of the capacitor voltage i.e., $V_{dc}/4$, the clamping diodes are required to have different voltage ratings for inverse blocking voltage. For example, when the bottom switches (S_1'-S_4') are turned on, d_2 needs to block three capacitor voltages, i.e., $3V_{dc}/4$. Similarly, d_3 and d_4 need to block $2V_{dc}/4$, and d_5 needs to block $3V_{dc}/4$. However, in practice the voltage rating for all the clamping diodes is typically selected to be exactly as the active device switches. As a consequence, the number of diodes required for each phase will be equal to $(m-1)(m-2)$, where m is the number of the required levels [31, 43]. In the case with five-level inverter, the number of diodes required will be 12 as shown if Figure. 1.3.

In order to demonstrate the advantages of adopting the single-phase five-level inverter over the conventional two-level inverter, the output voltage waveforms of both inverters are compared in Figure. 1.4. It is obvious that, the inverter output voltage enhances its quality as the number of levels increases. This leads to a large reduction in the total harmonic distortion (THD) of the

output waveform as shown in Figure. 1.5, consequently, allowing the possibility of use of a smaller size filter.

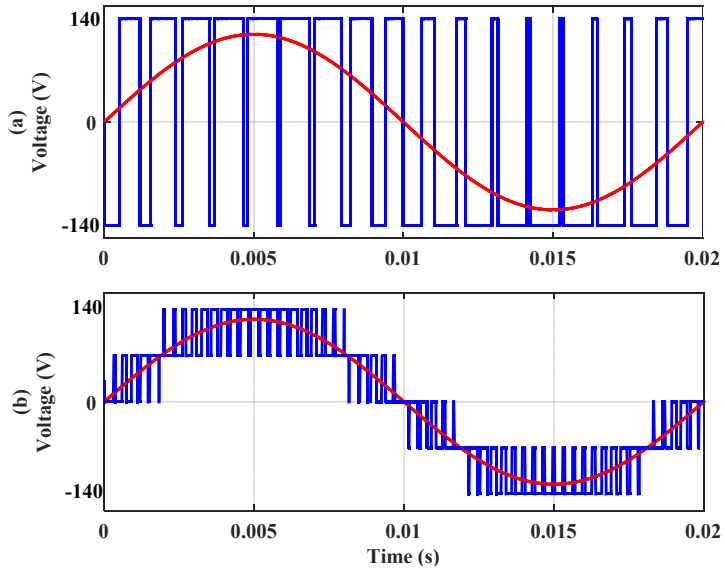


Figure 1.4. Single-phase inverter output voltage waveforms: (a) two-level, (b) five-level

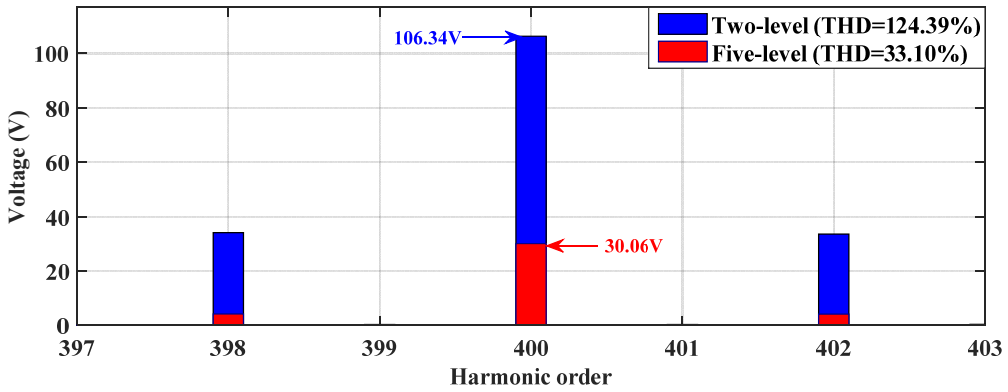


Figure 1.5. Unfiltered inverter output voltage harmonics at 20 kHz switching frequency for two and five-level inverters

Since the five-level inverter is able to switch its output voltage between five different dc voltage levels, there is an obvious reduction in its switching frequency harmonic magnitude when compared to the two-level inverter. In addition, it is clear that the ratio of the filter cut-off frequencies to attenuate the switching frequency harmonics to the same magnitude is around 3.5:1. This means, the cut-off frequency for the low-pass filter (LPF) used in conjunction with the five-level inverter, can be increased to be approximately three and a half times higher than that used with a two-level inverter. Increasing the cut-off frequency of the LPF can allow the closed loop control system to achieve a higher bandwidth response. Alternatively, the size of

the LPF connected to the five-level inverter can be made approximately 3.5 times smaller than that necessary for the two-level inverter.

In addition to the filter size reduction advantage, there are further merits in using the five-level inverter over the conventional two-level inverter. For example, the reverse blocking voltage of the switch devices is lowered from full to a quarter of the total DC link voltage. For instance, both two-level and five-level inverters require a voltage of around 760 V dc link to synthesize 230 Vac at the inverters output. This impacts on the semiconductor devices used in the inverter; 1200 V IGBTs would be needed in the case of two-level inverter, as opposed to 250 V MOSFET devices in the five-level [44]. This means, adopting five-level inverter would require each device to block only quarter of the DC link voltage compared with a conventional two-level where each device has to block the total DC voltage. This is not really an issue in low-power applications but it will become more important as system voltage levels increases in high voltage applications. In addition to the above merits, utilizing the five-level inverter allows the possibility of earthing the midpoint of the PV array. By earthing the mid-point, the capacitive earth currents and their negative influence on the electromagnetic compatibility (EMC) of the circuit will be eliminated. As a consequence, generation of common mode voltages can be avoided.

From the above discussed advantages, the five-level diode-clamped inverter is chosen over the conventional two-level inverter to perform as a power inverter in this thesis.

In the following section, the power switching strategies used for the five-level diode-clamped inverter will be briefly introduced.

1.3.1.2 *PWM Switching Strategies*

Various modulation techniques and control strategies have been developed and used for multilevel converters such as, multi-carrier based pulse width modulation (SPWM) [45, 46], selective harmonic elimination (SHE-PWM) [46, 47], and multilevel space vector modulation (SVM) [48, 49]. Among these switching techniques, the SPWM scheme which can be generally classified into two categories; phase-shifted and level-shifted modulations. These schemes are considered to be the most widely adopted, owing to their inherently simple implementation and lower computational requirements [43].

The multi-carrier level-shifted PWM (LS-PWM) strategy presented in [50], is considered to be the most widely adopted switching method for diode-clamped inverters. This is because each

carrier signal can be easily related to two power devices in the inverter [34, 35, 51]. For an *m*-level diode-clamped inverter using LS-PWM, (*m*–1) triangular carriers are required, all having the same frequency and amplitude. These triangular carriers are vertically arranged such that the bands they occupy are in contact [35, 51]. In order to determine the switched output voltages for the inverter, these carriers are continuously compared with a single sinusoidal reference. If the reference is greater than the carrier then the device corresponding to that carrier is turned on and vice versa [35, 50, 51]. Typically, there are three schemes for the LS-PWM: (a) in-phase disposition (IPD), where all carrier signals are in phase with each other; (b) phase opposition disposition (POD), where all carriers above the zero reference are in phase with each other but in opposite phase with those below the zero reference.; and (c) alternative phase opposition disposition (APOD), where carrier signals in adjacent bands are phase-shifted by 180° [35, 43, 50, 51]. An example of these arrangements for a five-level inverter (hence four carriers) is given in Appendix A.

It should be pointed out that, the IPD modulation scheme offers the best harmonic profile of all three modulation schemes, since all the carriers are in phase compared to the other two schemes [35, 50, 51]. Therefore, in what follows throughout the thesis, only the IPD modulation scheme will be used and implemented as the switching strategy for the five-level diode-clamped inverter. Different simulated waveforms of the five-level inverter when the IPD-PWM scheme is used are provided in Appendix A.

1.3.2 Low-pass Filter

As it has been underlined earlier, a low-pass filter is required to be connected at the output of the grid-connected inverter, to filter out unwanted switching frequency harmonics to a level that complies with the grid interconnection standards. In the technical literature, the L-filter, LC-filter and LCL-filter, are the most commonly used topologies for grid-connected inverters. Among these topologies, the third-order LCL filters have received much attention owing to their ability to provide higher harmonic attenuation capability around the switching frequency at smaller size and cost when compared to other topologies. Another advantage of the LCL filter is that the presence of the supply-side inductor inhibits the filter capacitor acting as a low impedance to supply generated harmonics. Considering the significant of these two advantages, an LCL filter is adopted for the experimental inverter set-up described in this thesis. A step-by-step design procedure of the LCL filter used in this thesis is provided in Appendix B. The

resultant LCL-filter parameters demonstrate that the size of the filter is approximately four times smaller than that of two-level inverter for the same system.

1.4 Grid Requirements for PV

The objective of grid-connected inverter systems is not only to convert power, but also to integrate distributed energy sources such as PV into the utility grid. Thus, these PV systems as an important source of distributed power generation are required to fulfil other necessary grid requirements. This includes safety, stability, smooth transfer of the electrical energy to the grid and most of all is to fully maximize the benefits of the integration such PV systems into the grid. Some of the most relevant grid requirements are briefly described below.

1.4.1 Response to Abnormal Grid Conditions

Abnormal conditions in terms of voltage amplitude and frequency can arise on the utility grid. In the event of such a case, the regulations require fast disconnection of the PV inverter system from the utility grid. This response is primarily required to guarantee the safety of utility maintenance personnel and the general public as well as to avoid damage to the photovoltaic system itself [11]. According to the standards IEEE 1547 [12], and IEC 61727 [13], the boundaries of operation with respect to grid voltage amplitude and frequency are given in Table 1-2, and Table 1-3 respectively, in which continuous normal operation areas are defined. It should be pointed out that, the voltages in (RMS) are measured at the point of common coupling (PCC), and the disconnection time specifies the time between the irregular condition happening and the inverter ceasing to energize the grid line [11].

Table 1-2: Disconnection time for voltage variations

IEEE 1547		IEC 61727	
Voltage range (%)	Disconnection time (sec)	Voltage range (%)	Disconnection time (sec)
$V < 50$	0.16	$V < 50$	0.1
$50 \leq V < 88$	2.00	$50 \leq V < 85$	2.00
$88 \leq V \leq 110$	Normal operation	$85 \leq V \leq 110$	Normal operation
$110 < V < 120$	1.00	$110 < V < 135$	2.00
$V \geq 120$	0.16	$V \geq 135$	0.05

Table 1-3: Disconnection time for frequency variations

IEEE 1547		IEC 61727	
Frequency range (%)	Disconnection time (sec)	Frequency range (%)	Disconnection time (sec)
$60.5 < f < 59.3$	0.16	$51 < f < 49$	0.2
$59.3 \leq f \leq 60.5$	Normal operation	$49 \leq f \leq 51$	Normal operation

These standards reveal that most demanding requirement is when the maximum disconnection time is 0.05s for a grid voltage amplitude deviation above 135% (Table 1-2). Consequently, a precise and fast grid voltage detection system is essential in order to fulfil these requirements. Note that, after a trip caused by irregular utility voltage or frequency conditions, the inverter can be reconnected only when the conditions given in Table 1-4 are met.

Table 1-4: Conditions for reconnection after trip

IEEE 1547	IEC 61727
$88 \leq V \leq 110$ (%) AND $59.3 \leq f \leq 60.5$ (Hz)	$85 \leq V \leq 110$ (%) AND $49 \leq f \leq 51$ (Hz)

1.4.2 Power Quality Issues

One of the most significant issues facing the widespread integration of distributed power generation systems (DPGSs) is that of power quality. Since the PV systems are considered to be an important source of distributed power generation, the quality of the power provided by them is ruled by series of strict standards on voltage, frequency and harmonics. Variation from these predefined regulations represents out-of-bounds situations and may require disconnection of the PV system from the utility grid [11].

1.4.2.1 *DC Current Injection*

DC current injection into the utility grid has been considered a particularly serious power quality issue in the new generation of transformer-less PV inverters. The injection of such a current into the utility grid can cause various problems, including malfunction of protection devices and saturation of the distribution transformers, leading to overheating and trips [51]. Thus, more attention is required in this matter by providing adequate means to suppress, or fully

eliminate the DC current components before connection to the utility grid is made. For the conventional PV systems on the other hand, the DC current component is typically removed by coupling the inverter output to the mains supply via a 50Hz isolation transformer [11, 51]. The relevant international standards on DC current injection are outlined in Table 1-5. Note that, the measured DC component should be below the limit for different loading conditions.

Table 1-5: DC current injection limitation

IEEE 1547	IEC 61727
$I_{dc} < 0.5$ (%) of the rated RMS current	$I_{dc} < 1$ (%) of the rated RMS current

1.4.2.2 *Current Harmonics*

Another major power quality issue associated with the integration of PV systems into the utility grid is the harmonics in the injected grid current. The generated harmonics can be separated according to their frequencies into lower and higher-order. Low-order harmonics can occur as a result of both intrinsic and extrinsic effects. Distortion generated intrinsically arises primarily from deficiencies in the inverter control loop, dead time effects, measurement inaccuracies, and lack of stiffness in the dc link. Moreover, extrinsic sources of low-order harmonics consist of the effect of connecting to a weak and polluted utility grid. The attenuation of such low-order harmonics (in the sub 1 kHz), is commonly performed using the inverter current control-loop [52, 53]. High-order harmonics on the other hand, which are mainly associated with the inverter switching frequency (in the kHz range), occur as multiples of the PWM switching frequency. These high-order harmonics can generally be suppressed by the addition of a cost-effective low-pass filter at the inverter output as it has been highlighted earlier [14, 54].

To ensure that the PV system output current contains low current distortion levels, stringent regulations have been put into place. These regulations require the overall total harmonic distortion (THD) of injected currents to be maintained less than 5%, whilst the amplitude of any single harmonic varies as presented in Table 1-6.

Table 1-6: Maximum current harmonics

IEEE 1547 and IEC 61727						
Individual harmonic order (odd harmonics)	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	Total harmonic distortion THD%
(%)	4.0	2.0	1.5	0.6	0.3	5.0
Even harmonics are limited to 25% of the odd harmonic limits listed above						

1.4.2.3 *Electromagnetic Interface (EMI)*

Modern power converters operating at high switching frequency with very short rise and fall times of voltages and currents can lead to significant EMI problems. This issue which propagates by conduction and/or radiation is severe mainly when the dc link midpoint cannot be earthed, resulting in the dc-link voltage switching at high frequency relative to earth [54, 55]. A promising candidate for low EMI is multilevel inverter technology, in which the mid-point can be grounded as demonstrated earlier with the five-level inverter [40].

1.4.3 Anti-Islanding Protection

Islanding for grid-connected PV systems occurs when a PV inverter does not disconnect from the grid when irregularity in the electrical supply network is detected. This means that the PV inverter continues to feed power to a grid that has lost power [11]. Typically, this can occur in the case of loss of mains due to electrical fault on the network or when the supply network is deliberately switched off for maintenance. In both cases, if the PV inverter does not disconnect, the following consequences may take place. A safety hazard for persons working on the utility line is likely, and also sensitive equipment being connected to the network may be subject to damage due to an out-of-phase closure. Therefore, in order to avoid these serious consequences, islanding must be detected and the PV inverter involved must be disconnected from the grid. This is referred to as anti-islanding (AI) [11, 14, 54]. Several Islanding detection schemes have been proposed, which can be classified into passive methods, and active methods. Details of these methods are out of the scope of this these and can be found in [56-59]

1.5 Grid Connected Photovoltaic System Review

The review presented in this chapter shows there is a clear need for continued research into improving the power quality of grid connected PV inverter systems. Mainly two areas have been highlighted in which it is believed significant improvements can be made. These are:

- The rejection of the DC offset associated with the grid voltage measurement circuits by modifying the structure of conventional Second-order Generalized Integrator (SOGI) PLL. As a result, the total harmonic content is reduced, and thus, the power quality of the current injected into the grid is improved.
- The use of a *dq* current controller for the purpose of eliminating the steady-state error associated with the conventional PI-current controller.

This thesis is devoted to addressing these two specific issues.

1.6 Thesis Overview

The thesis consists of nine chapters. The first chapter comprises of a general discussion on grid-connected photovoltaic systems. In this chapter, a five-level diode-clamped inverter is chosen for the purpose of reducing the output passive filter size requirements. A brief description of the other chapter's content is given below.

Chapter 2 introduces the basis of the synchronization issue and some of the most relevant state of the art structures for synchronization methods used in single-phase PV systems. A deep analysis of the conventional power-based phase-locked loop (pPLL) as the preferred tool for synchronization in single-phase systems is given. Practical limitations of the use of the pPLL are identified, and different previously reported solutions are discussed.

Chapter 3 considers the use of second-order generalized integrator based PLL (SOGI-PLL) as the most promising candidate for grid synchronisation in single-phase grid-connected power converters. An overview of the SOGI-PLL along with its structure and principle of operation are presented. Furthermore, the small signal linearized model for SOGI-PLL structure is derived. This is followed by step-by-step design guidelines to fine-tune its parameters ensuring a robust performance of the PLL. The performance of the proposed design method is then evaluated through extensive simulation tests, considering several utility grid disturbances. The major disadvantages associated with this method are highlighted and solved.

Chapter 4 aims to provide a comprehensive analysis of the effect of the dc offset based on the PLL in the synchronous reference frame (SRF). Two different existing offset rejection approaches based on the orthogonal signal generator (OSG) SOGI algorithm are discussed in detail. A novel method to tackle this issue is proposed, and its effectiveness is verified through simulation results.

Chapter 5 proposes a new alternative approach for the current regulation of single-phase voltage-source converters (VSCs) in the synchronous reference frame (*dq* frame). The proposed *dq*-current controller is able to eliminate the steady-state error associated with conventional PI-controllers in the stationary reference frame (S_tRF). Two different approaches for the *dq* current regulation are introduced and mathematically analysed. A performance evaluation of these approaches is provided at the end of this thesis.

Chapter 6 describes the implementation of a grid-connected PV inverter system for the experimental phase of the research work. An overview of the experimental hardware is presented, followed by a detailed description of the individual components and the microcontroller platform.

Chapter 7 presents the real-time experimental results for the PLL algorithm proposed in Chapter 4, when compared with those of the conventional SOGI-PLL and two other alternative dc rejection methods. Both steady-state and dynamic performance of the proposed PLL are examined.

Chapter 8 experimentally evaluates the performance of the simplified and the delay-based *dq* current control algorithms proposed in Chapter 5. In addition, a further experimental investigation is carried out to verify the impact of the proposed PLL on the power quality of the grid connected PV system. To highlight the effectiveness of the proposed PLL, the same investigation is conducted when the conventional SOGI PLL is used.

Finally**, Chapter 9** summarises the research work performed in this thesis, including a discussion on the degree to which the project aims have been met and possible areas of further research.

CHAPTER 2

Grid Synchronisation in Single-Phase PV Systems

2.1 Introduction

This chapter introduces the basis of the synchronization issue in single-phase PV systems and some of the most relevant state of the art structures of synchronization methods used in single-phase networks. Among several synchronization techniques, phase locked loop (PLL)-based algorithms have found a lot of interest, mainly due to their simplicity, robustness and effectiveness. Thus, thorough analysis of the conventional power-based PLL (pPLL) as the preferred tool for synchronization in single-phase systems is given. In this PLL, a sinusoidal multiplier is used as a phase detector (PD) by multiplying the grid voltage by the sine of the estimated phase angle. A result of this multiplication is a double-frequency term, which produces a high amplitude second-order harmonic in the estimated quantities by the pPLL. Among the various previously reported solutions, the orthogonal signal generation (OSG)-based PDs is set to be the best candidate in avoiding such a double-frequency ripple in the PLL estimated quantities. Therefore, a review of different orthogonal signal generator methods widely available in the literature is then carried out. This is followed by a full discussion on the appropriateness of each technique, in which the major benefits and drawbacks associated with each method are highlighted. Among the large number of reported OSG-PLLs, second order generalized integrator (SOGI-PLL) has become the most commonly used single-phase PLL, owing to its simple digital implementation, low computational burden, insensitivity to frequency variations and relatively high filtering capability. For these reasons, the possibility of using the SOGI-based PLL as a grid synchronisation unit in this project will be investigated in the forthcoming chapters.

2.2 Background

Due to the restriction of large and centralized power generation facilities, distributed power generation systems (DPGSs), mostly based on eco- friendly renewable energy sources, has gained a lot of attention during recent years worldwide [2, 60-62]. Small-scale DPG units, such as micro-turbines, roof-mounted photovoltaic, wind turbine systems, and fuel cells, are being employed at the distribution level [9]. In a DPGS, voltage source inverters (VSIs) are typically adopted to provide a controlled and high-quality power exchange with the single-phase grid or local loads [9, 60, 63].

The number of DPGSs connected to the utility network has now reached significant penetration levels. On one hand, these grid-connected DPGS can actively contribute in supporting the grid services (voltage /frequency), and maintaining generation even if the voltage at the point of common coupling (PCC) is distorted. This is primarily when high levels of power are considered for their power converters. On the other hand, this implies that the power quality, safety conditions and stability of the power system can be extremely affected [11, 64]. For this reason, the integration of such sources into the power grid must satisfy modern strict grid codes [11, 12, 65]. According to these regulations, a high quality current is to be injected by the DPGSs under normal and distorted grid voltage. That is, the current injected into the utility grid has to be properly synchronized to the utility voltage with high power quality. Therefore, the control strategies of the distributed power generation systems should be designed to meet the modern requirements for grid interconnection. Typically this control is based on a synchronization unit to ensure fast and accurate grid synchronization, and a current control strategy to enable an appropriate and high-quality current injection [63, 64]. It is essential to point out that, the successful performance of any current controller of grid-connected DPGS directly depends on the accurate response of the synchronization method used. Therefore, the performance of the synchronization method is crucial for a proper operation of the entire grid-connected DPGSs [2, 21].

In grid-connected applications, phase-locked loops (PLLs) are the most widely used technique for synchronization. This is because they are simple to implement digitally and if correctly tuned offer a robust performance. In recent years, several single-phase PLL techniques have been proposed [2, 7, 11, 66-68]. In the following, an overview of the most widely used synchronization methods, including Zero-crossing detection (ZCD) and phase-locked loop

(PLL), will be presented and discussed. The application of a conventional PLL scheme for synchronizing with the utility grid will provide evidence of the need to improve its structure by using an orthogonal signal generator (OSG).

It is worth mentioning that there are also PLL methods in the frequency-domain. These approaches usually obtain the grid voltage parameters via a discrete Fourier transform (DFT) [69]. Despite the high precision that can be achieved, the intensive computational effort prevents them from reaching high transient performance [70, 71]. Therefore, they are not considered in this thesis.

2.3 Zero-crossing detection (ZCD) technique

One of the simplest methods of obtaining the phase and frequency information is to detect the zero-crossing point of the grid voltage so that the generated signal can be synchronised with the grid voltage [2, 7]. This method, as presented in Figure 2.1, is based on using a comparator for detecting the changes in the polarity of the grid voltage waveform. A digital counter is used to measure the period of the square waveforms produced by the comparator. If it is assumed that the period of the current cycle is equal to that of the last cycle, then the interval between the two zero-crossings is added with the previous stored interval to obtain the period T of the signal. The frequency of the fundamental $\hat{\omega}$ can then be calculated. The phase-angle of the grid voltage $\hat{\theta}$ can now be obtained by integrating the estimated frequency [14].

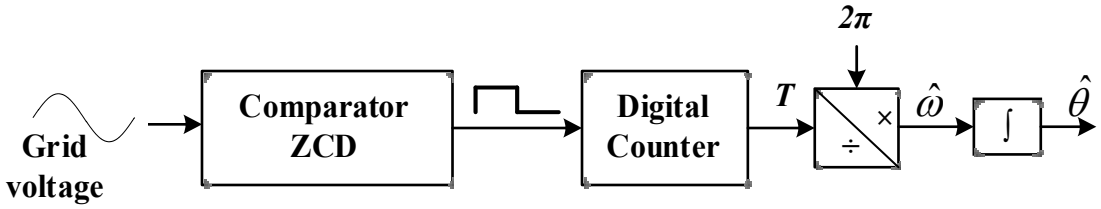


Figure 2.1. Block diagram of zero crossing detection

Despite the simplicity of implementation, the ZCD technique suffers from two major drawbacks. Firstly, due to the fact that system frequency information is only updated twice per power cycle, and is assumed to be constant in at least one half cycles, which is not always the case. Thus this method is very vulnerable to phase jumps and variations in the grid frequency, resulting in a poor phase tracking performance [67, 70, 72]. In order to mitigate this issue, a modified method based on multiple level crossing detection has been proposed in [73]. However, the complexity of the ZCD technique is increased. Additionally, the accuracy of this detection technique is not guaranteed under noisy and harmonically distorted conditions which

are common in the modern power electronic environment [7, 71]. Furthermore, these weaknesses are even more troublesome in the event of weak grid, where the voltage waveform becomes notably distorted by the harmonics [74]. To overcome this drawback, a simple low pass filter can be used. However, a major drawback of this method is the inherent phase lag of the filtered signal. Methods based on adaptive/predictive digital filtering algorithms have been proposed in the technical literature for cancelling delays in zero-crossing detection and attenuating the adverse effects resulting from the noise and switching notches of the grid voltage [74-77]. Some of these techniques are relatively complex and their performance is not completely acceptable when the grid voltage is affected by low-frequency harmonics or remarkable frequency variations [11].

2.4 Phase-Locked Loop (PLL) technique

In grid-connected applications, the PLLs are the most widely accepted synchronization techniques, mainly due to their ease of digital implementation, robustness, and effectiveness [11, 16, 66, 78]. A PLL is a nonlinear closed-loop system that measures the instantaneous values of its input signal i.e., grid voltage, in order to detect the phase of its fundamental frequency components and then synchronizes its output signal with respect to its input, so that the phase error between both input and output phases is minimum [17, 18, 78]

2.4.1 Basic structure of a Phase-Locked Loop (PLL)

Despite their differences, normally all PLL techniques are composed of three fundamental units [79], as illustrated in the block diagram of Figure. 2.2:

- The p*hase detector* (PD): This unit compares the phase angle of the reference input signal v, against the phase angle of the internally created signal $\hat{v}$; the output signal of the PD (i.e., ε_{PD}) is a measure of the phase error between its inputs. High-frequency AC components may appear together with the DC phase-angle error signal depending on the PD type.
- The *loop filter* (LF): This unit can be as simple as a first-order low-pass filter or a PI controller, thus it presents a low-pass filtering behaviour. This block is used to suppress the noise and high-frequency signal components from the PD output and to provide a DC-controlled signal component for the VCO.

- The *voltage-controlled oscillator* (VCO): This unit uses the LF output signal to synthesise a sinusoid with the phase and frequency to that of the input signal.

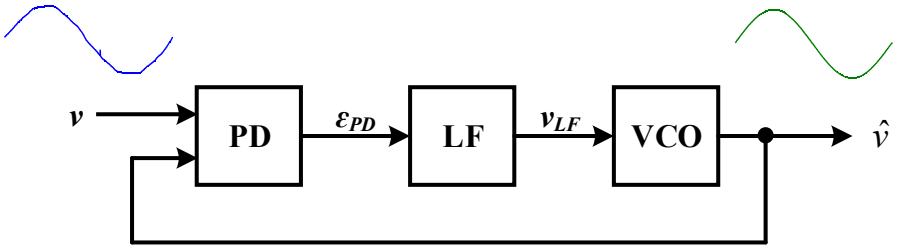


Figure 2.2. Basic structure of a PLL

In most cases, PLL algorithms differ from each other just in the way that the PD block is implemented. Since the PD is required to output the phase error quickly and precisely, its performance is the most critical piece in the PLL system design [70].

In the following, a brief review of the conventional PLL topology, which is referred to as a power-based PLL (pPLL) will be provided. The main drawbacks related to its implementation, and some previously reported solutions will be also discussed in this section.

2.4.2 Conventional power-based pPLL

Typically, the conventional single-phase pPLL uses a sinusoidal multiplier PD system which simply relies on the product of two signals at two different frequencies (i.e., the reference and estimated frequencies), to produce a signal at the difference and sum of the two input frequencies [16, 68, 80]. These PLLs are based on the instantaneous active power theory for single-phase systems. Thus, they are generally referred to as the power-based PLL (pPLL) [16, 17, 81].

Figure 2.3 displays the block diagram of the single-phase pPLL, in which the LF is based on a simple PI-controller and the VCO consists of a sinusoidal function supplied by a linear integrator. Note that, the feedforward term ω_{ff} defines the central frequency around which the PLL will lock to, and it is added to improve the initial dynamic performance of the PLL system [16, 82].

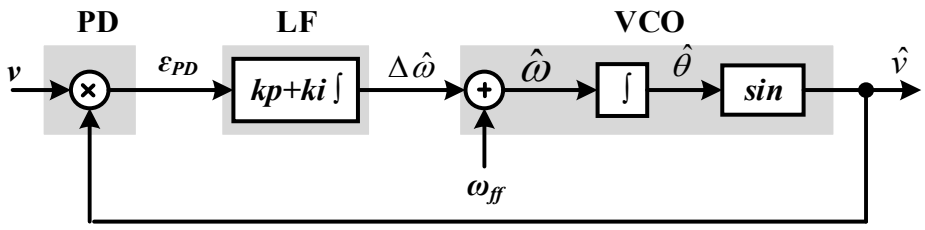


Figure 2.3. Block diagram of the single-phase pPLL

In the following, equations describing the behaviour of the single-phase pPLL will be developed. For the sake of simplicity, the input voltage signal applied to this system is assumed to be a pure sinusoid and is given by

$$\boldsymbol{v = V_m \cos \theta} \tag{2.1}$$

where: V_m, and θ are the input voltage amplitude, and phase-angle, respectively.

Note that, the analogy with active electric power can be used in order to understand the behaviour of the pPLL more easily [82]. If the PD block output signal (i.e., ε_{PD}) is zero, then the signal generated by the VCO, $\hat{v}$ and the fundamental input voltage signal, v will be in quadrature relative to each other [16]. Consequently, the estimated phase angle $\hat{\theta}$ is equal to the real phase angle θ. The signal generated by the VCO can be expressed as

$$\boldsymbol{\hat{v} = \sin \hat{\theta}} \tag{2.2}$$

Based on Figure.2.3, the phase error signal at the output of the multiplier PD can be expressed as

$$\boldsymbol{\varepsilon_{PD} = V_m \cos\theta \,.\, \sin\hat{\theta} = \frac{V_m}{2}\left[\underbrace{\sin(\theta - \hat{\theta})}_{dc\ term} + \underbrace{\sin(\theta + \hat{\theta})}_{double-frequency\ term}\right]} \tag{2.3}$$

When the frequency of the VCO is well tuned to the input signal frequency, i.e. $\hat{\omega} \approx \omega$, and for a small phase error $(\theta - \hat{\theta})$, (2.3) can be divided into two parts: a dc term that has the information on the phase angle error, and a high-amplitude double-frequency disturbance term that must be removed prior to the signal being fed into the LF to keep the perturbation on the utility grid phase angle within a satisfactory range [17, 83]. Although in theory the double-frequency component of the PD error signal is assumed to be filtered out by the LF, complete cancellation of this component by the LF is not possible in practice. Often a ripple at twice the fundamental frequency is present in the estimated quantities (i.e., $\hat{\omega}$ and $\hat{\theta}$) which contributes

to the degradation of the pPLL performance [54]. Figure 2.4 shows some representative simulation results describing the performance of the pPLL depicted in Figure 2.3 where the input grid signal v is affected by a frequency step changes (from 50 to 45 Hz) at time = 0.15s. The PLL parameters k_p, k_i were calculated according to [11] to achieve two different settling times t_s with a damping factor ξ = 0.707. It can be observed from Figure. 2.4 that, a high-amplitude steady-state oscillation error is made in the estimation of the frequency and phase angle of the input voltage v. This error is a consequence of the double-frequency term existing at the output of the multiplier PD (i.e., ε_{PD}) as underlined earlier in (2.3). Also, it is clear that the amplitude of this undesired error can be reduced by setting a longer settling time for the PLL (i.e., t_s=200ms) , which is equivalent to decreasing the bandwidth of the system to the half. Although reducing the bandwidth of the pPLL system could alleviate this problem; however, the transient response of the pPLL system will be significantly degraded.

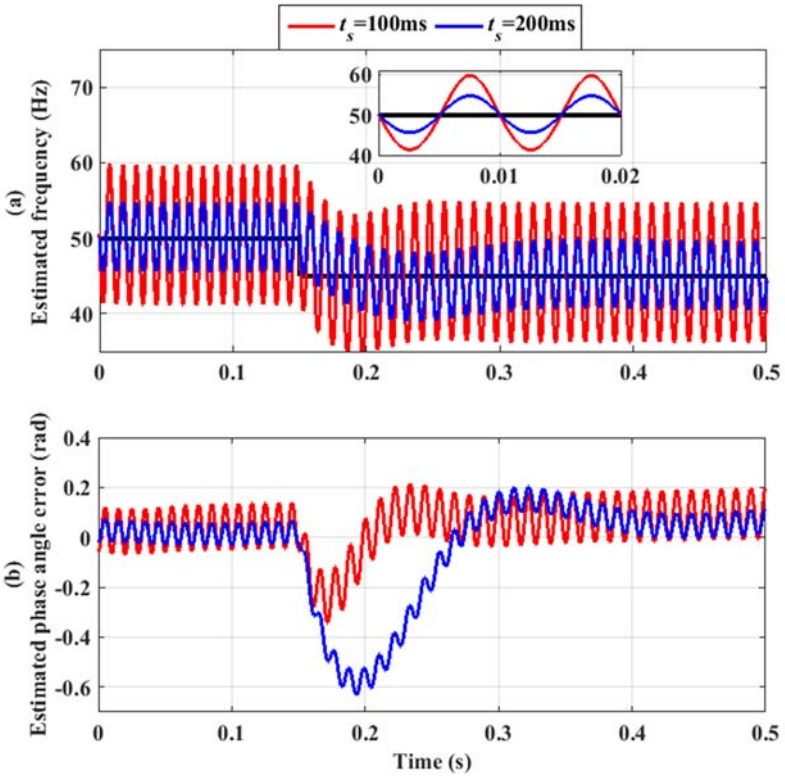


Figure 2.4.Response of the pPLL when the input voltage undergoes a frequency step change at two different settling times: (a) estimated frequency, and (b) estimated phase-angle error

As pointed out earlier in (2.3) and Figure. 2.4, there is a strong drawback associated with the pPLL technique: the product of the input voltage signal v and its orthogonal component $\hat{v}$ yields a second-order harmonic component in the PD output signal which significantly affects the estimated quantities of phase/frequency, and limits the bandwidth of the PLL [70]. In order to overcome this drawback, a low-pass filter with a low cut-off frequency can be added [17].

However, using a LPF with a low cut-off frequency significantly degrades the transient response of the PLL system. Nevertheless, this drawback can be minimized if the filter order is increased concurrently to its cut-off frequency; however, in addition to stability issues, using a high-order LPF imposes a high computational effort on the control system [16, 17]. A band-reject (notch) filter tuned at twice the input voltage fundamental frequency can be used to attenuate twice the grid frequency components as proposed in [84]. However, due to the variations of the grid frequency, the notch filter should be adaptive, which increases the system cost and complexity [78].

Recently, an effective method based on peak voltage detection (PVD) has been proposed in [72] to deal with the aforementioned problem of the pPLL without adding LPFs. This approach is referred to as the modified mixer PD (MMPD). Under steady-state phase/frequency-locked conditions, the low-frequency oscillations in the estimated quantities by the PLL are considerably suppressed by placing a PVD scheme at the input of the PLL so that a unity value of the input voltage amplitude is assumed, and adding a simple difference of product term generated by the estimated phase angle to the standard mixer PD, as presented in Figure. 2.5 [17, 68]. Despite exhibiting some improvements over the conventional pPLL technique, MMPD suffers from a major drawback; the accurate and fast estimation of the input voltage amplitude may not always be guaranteed [17, 85]. In this case, the PLL performance can be significantly degraded as demonstrated in Figure. 2.6.

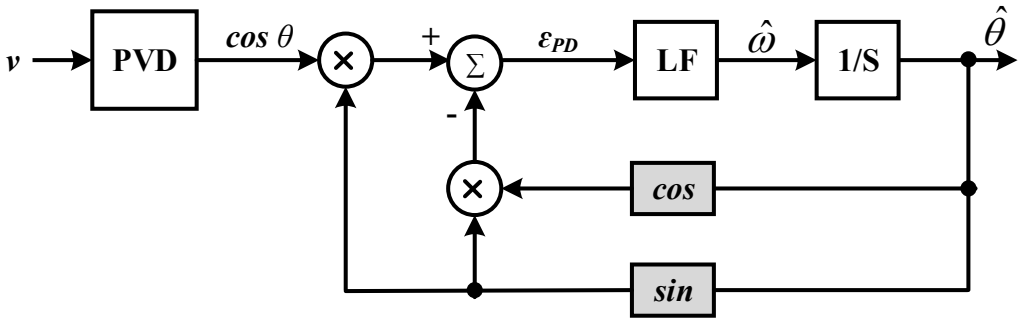


Figure 2.5. Modified mixer PD (MMPD)-based PLL [72]

From Figure.2.6, it is obvious that, although the proposed MMPD has successfully eliminated the ripple noise appearing in the estimated phase/ frequency quantities without the use of LPFs, however, regardless the cost and complexity forced by the PVD, its sensitivity to the grid voltage variations is high, since the voltage amplitude detected by the PVD technique may not always be rapid and precise.

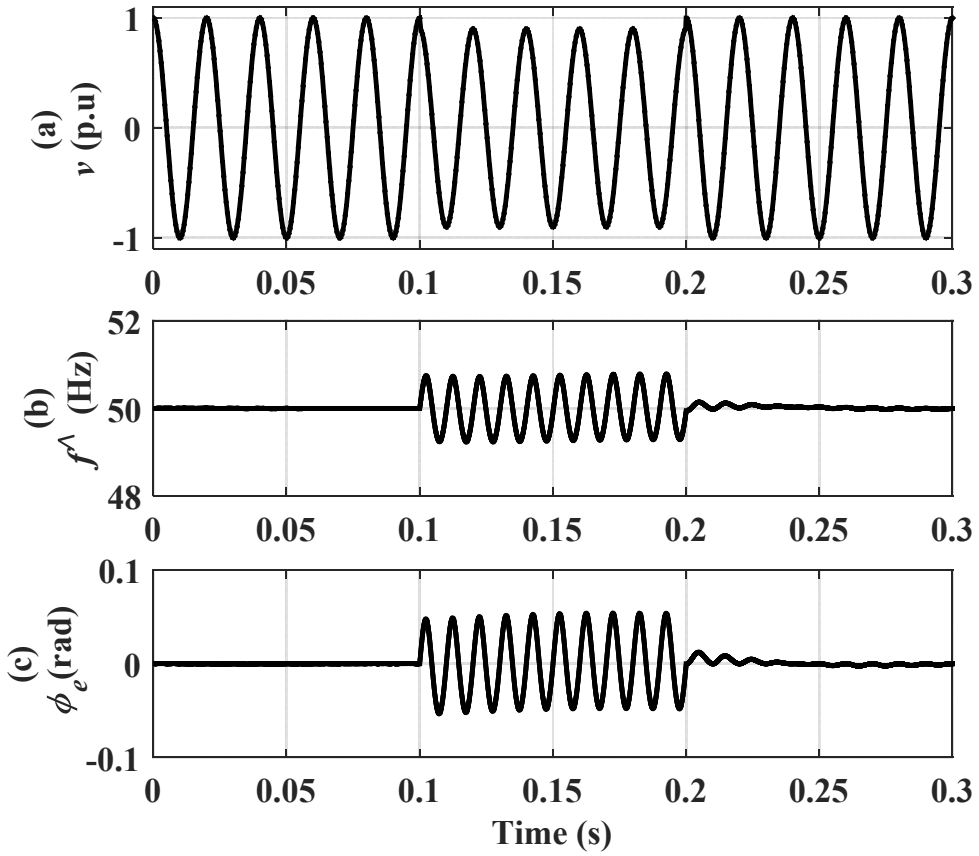


Figure 2.6. Response of the MMPD-based PLL when the amplitude of input voltage undergoes voltage sag of 0.1p.u: (a) grid voltage, (b) estimated frequency, and (c) estimated phase-angle error

Another approach using a double-frequency and amplitude compensation (DFAC) method is proposed in [17, 71]. Actually, the DFAC approach is equivalent to an adaptive notch filter/low-pass filter in the rotating reference frame, which entirely eliminates the unwanted double-frequency component caused by the PD [86].

Another effective approach to avoid the double-frequency ripple in the PLL estimated quantities is to use the transformation-based PDs (T-PDs) instead of simple multiplier PD. The T-PDs are commonly used in three-phase systems, with the synchronous reference frame (SRF), being most widely used due to its simplicity and effectiveness [78, 87]. For a single-phase application, however, the implementation of the rotational coordinate transformation is more complicated due to the reduced number of input signals available [15, 17, 66, 88, 89]. The common approach in single-phase systems is to develop techniques that are able to create a fast and accurate fictitious signal orthogonal to the original single-phase signal. This makes it possible to represent the single-phase system as a pseudo two-phase ($\alpha\beta$) system [78]. Performing the Park transformation on the two-phase ($\alpha\beta$) system, yields phase error information with high precision and zero steady-state error. These PLLs which are often called the orthogonal signal generation-

based PLLs (OSG-PLLs), are the most popular synchronisation technique in single-phase systems [66]. It should be pointed out that the main differences among various ways of realizing an OSG-based technique typically are based on how the fictitious orthogonal signal is created [90].

In the following, more comprehensive discussions on the implementation of the OSG-PLLs in single-phase systems using the OSG techniques will be provided.

2.4.3 PLL based on OSG (OSG-PLL)

In order to completely solve the second-order harmonic problem which is prevalent in the conventional pPLL technique without affecting the stability and the transient performance of the PLL; an OSG-based PD technique as shown in Figure.2.7 can be adopted. Again, for the sake of simplicity, the input voltage signal is assumed to be a clean sin wave, i.e., $v = V_m \cos\theta$ and the SOG, to be able to generate a set of in-quadrature signals without introducing any delay at any frequency from a given input signal.

The operating principle of the PLL based OSG structure consists in cancelling the undesired double-frequency components of the PD block output signal (i.e., ε_{PD}) when fictitious currents i_α and i_β are in quadrature with respective voltages v_α and v_β [11, 81].

The two orthogonal voltage signals (v_α ,v_β), the fictitious currents (i_α ,i_β), and the phase-angle error ε_{PD} resulting from the PLL based-OSG are defined by

$$\begin{cases} \boldsymbol{v_\alpha = v = V_m \cos\theta} \quad \boldsymbol{and} \quad \boldsymbol{v_\beta = V_m \sin\theta} \\ \boldsymbol{i_\alpha = \sin\hat{\theta}} \quad \boldsymbol{and} \quad \boldsymbol{i_\beta = -\cos\hat{\theta}} \\ \boldsymbol{\varepsilon_{PD} = V_m \sin(\hat{\theta} - \theta)} \end{cases} \tag{2.4}$$

According to (2.4), assuming that the PLL is well tuned, i.e. $\hat{\omega} \approx \omega$, as expected the T-PD does not generate any steady-state oscillatory term.

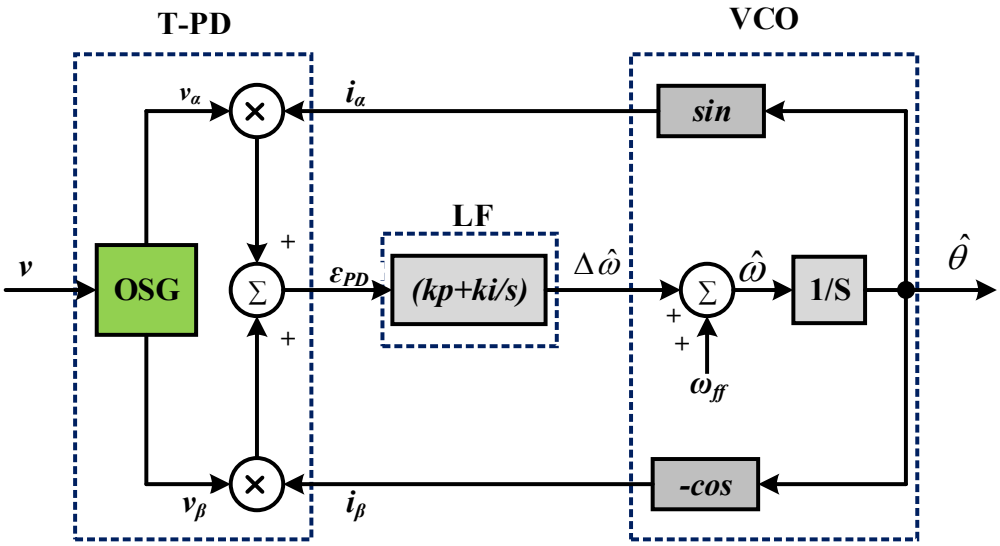


Figure 2.7. Block diagram of single-phase PLL based-OSG-PD

A review of the trigonometric expression of (2.4) reveals that this is a part of the Park transformation, which is defined by the equation (2.5). Therefore, the diagram of Figure 2.7 can be redrawn as shown in Figure 2.8 which represents the SRF-PLL system.

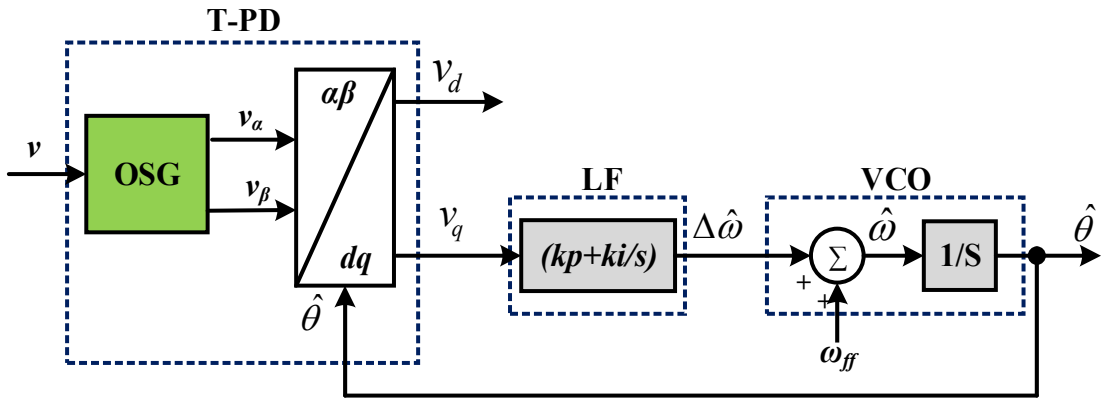


Figure 2.8. Block diagram of single-phase PLL in the rotating reference frame (SRF-PLL)

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}) & sin(\hat{\theta}) \\ -sin(\hat{\theta}) & cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2.5}$$

By substituting v_α and v_β from (2.4) into (2.5) the output of the PD of Figure.2.8 is given by the voltage vector of the following equation of (2.6). This equation will be free of oscillations if the PLL is well tuned to the input frequency, i.e. when $\omega \approx \hat{\omega}$.

$$\boldsymbol{v}_{(dq)} = \begin{bmatrix} \boldsymbol{v_d} \\ \boldsymbol{v_q} \end{bmatrix} = \boldsymbol{V_m} \begin{bmatrix} \boldsymbol{cos}(\widehat{\boldsymbol{\theta}} - \boldsymbol{\theta}) \\ \boldsymbol{sin}(\widehat{\boldsymbol{\theta}} - \boldsymbol{\theta}) \end{bmatrix} \tag{2.6}$$

When the PLL is perfectly locked, and according to Figure 2.8, the PI-controller of the LF will set the angular position of the dq reference frame to make v_q = 0 in the steady state, which means that the input voltage vector v will rotate orthogonally to the q axis of the rotating reference frame. In such a case, the v_d signal will provide the amplitude of the input voltage vector and the phase-angle detected by the PLL will be in-phase with the sinusoidal input voltage [11].

2.4.4 Overview of different PLLs based on OSG

Taking into account the importance of the OSG in the design of OSG-PLLs applied to synchronize with single-phase grids; several relevant techniques for generating the orthogonal voltage signal from a single-phase system have been described in the technical literature. The transfer delay [86, 91, 92], all-pass filter [9, 93], Hilbert transform [94, 95], Kalman filter [96], second-order generalized integrator [63, 68, 97], the derivative [98, 99], and inverse Park technique [16, 100] are the most common methods to create the orthogonal signal. Some of these OSG techniques will be briefly presented in the following.

2.4.4.1 *Transfer Delay-based OSG*

The delay method is regarded as the earliest method and its performance analysis can be found in [91, 92]. Due to its simple structure as presented in Figure. 2.9, this method can be easily implemented to generate the orthogonal signal by storing the past one-quarter of the number of samples contained in one fundamental frequency period in the memory of the DSP [11].

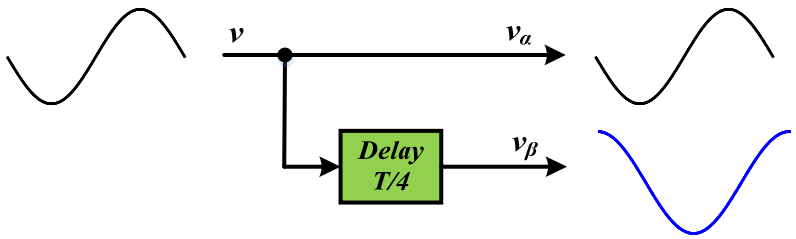


Figure 2.9. Transport delay-based OSG

This technique offers a reasonable performance if the grid voltage is a purely sinusoidal waveform at its rated grid frequency value. However, under off-nominal grid frequencies, the phase shift caused by the transfer delay unit, will not be perfectly 90°. This lack of orthogonality, as it will be shown in Figure.2.10, results in double-frequency steady-state errors in the estimated quantities by the OSG-PLL [86, 90]. To deal with this issue, various approaches have been proposed in the technical literature in recent years [86, 90, 101].

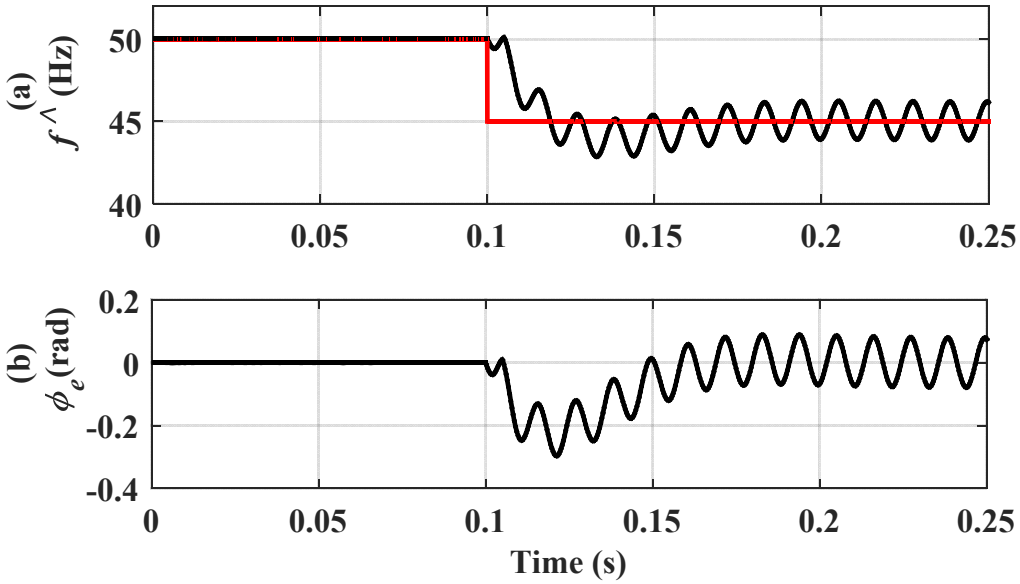


Figure 2.10. Response of the OSG-PLL transport delay-based under sudden frequency step of 5Hz

Another drawback associated with this technique is its lack of filtering capability, consequently if the single-phase input voltage is corrupted by harmonic components, which is nearly always the case, the generated orthogonal signals will not be orthogonal, since each of the frequency components of the input voltage signal had to be postponed by a quarter cycle of its fundamental period, resulting in oscillation ripple in the detected quantities by the PLL as it will be shown in Figure. 2.11. Consequently, this technique is definitely not a proper choice under distorted grid conditions [11, 89].

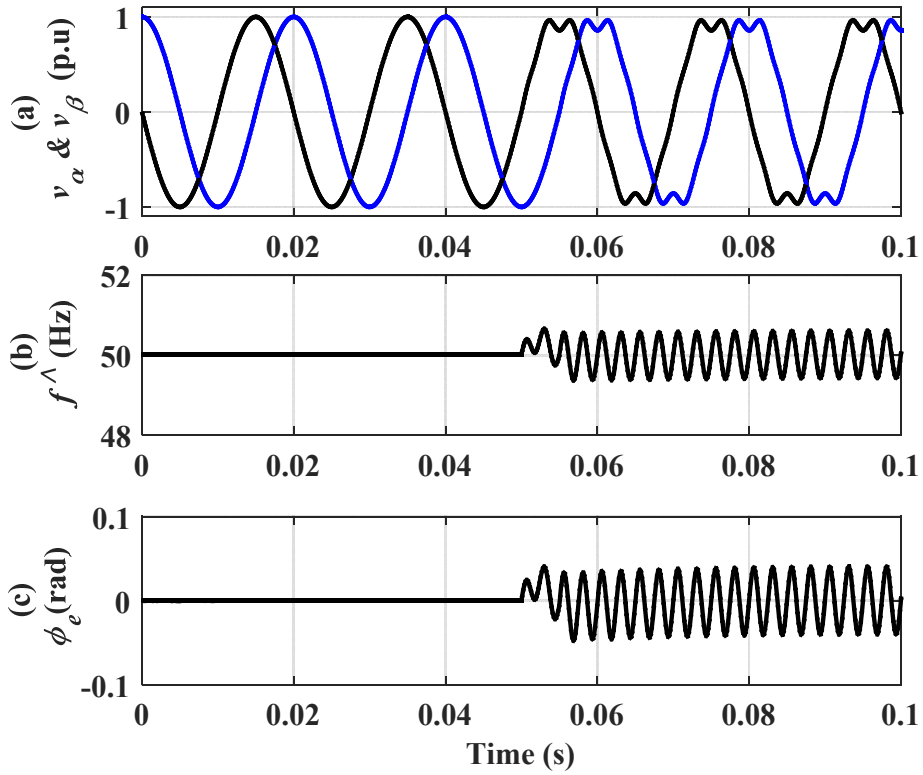


Figure 2.11. Response of the OSG-PLL transport delay-based when the input voltage undergoes an 8% THD

2.4.4.2 *Derivative-based OSG*

In order to overcome the long delay associated with the quarter-cycle delay method, references [98] and [99] uses the differential operation to create the orthogonal signal as shown in Figure.2.12. Although the dynamic response of the system can be improved, however, with high sampling frequency; the differential operation will introduce high frequency random noise and numerical errors [88]. Moreover, in the conditions where the grid frequency deviates from its nominal or when the grid voltage contains harmonics, the noise amplification caused by derivative function can significantly deteriorate the system performance as will be illustrated in Figures. 2.13 and 2.14 respectively. Therefore, this approach is rarely used in practical applications where the utility grid is highly distorted [66, 78].

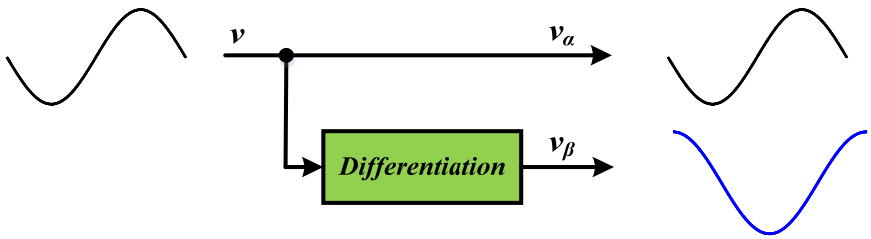


Figure 2.12. Derivative-based OSG

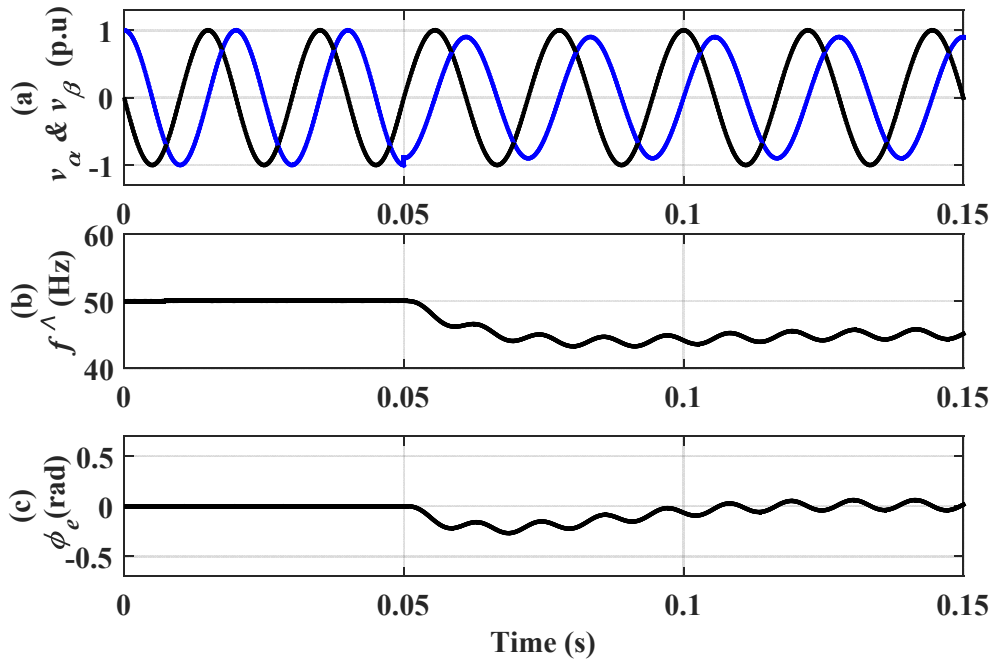


Figure 2.13. Response of the OSG-PLL derivative-based under sudden frequency step of 5Hz

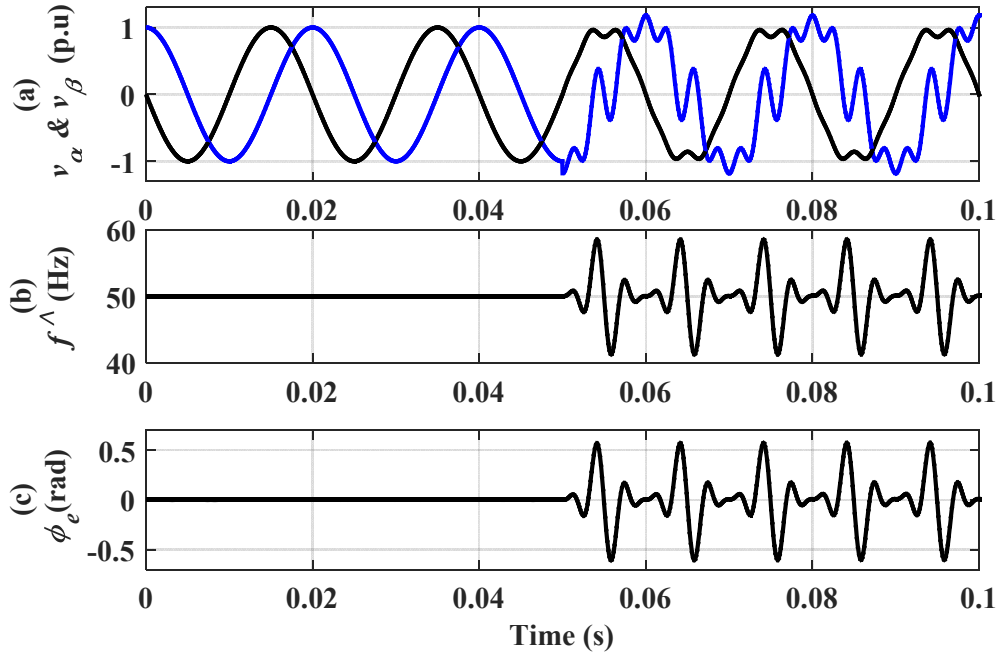


Figure 2.14.Response of the OSG-PLL derivative -based when the input voltage undergoes an 8% THD

2.4.4.3 *Inverse Park Transform-based OSG*

Figure.2.15 displays a schematic diagram of the inverse Park-based OSG introduced in [16, 66, 68, 100, 102]. As it can be seen, the required orthogonal signal (i.e., v_β) is internally generated by applying the inverse Park transformation to the filtered synchronous components, i.e., $v_{\bar{d}}$

and v_q^-. It should be noted that, the PLL transient behaviour generally depends on the characteristics of the two LPFs used to attenuate the possible harmonics/noises from the Park transformation output signals i.e., v_d and v_q. Thus, these LPFs must be adequately tuned in order to guarantee the performance of the single-phase PLL [16, 102]. Further details on the analysis and design of this method can be found in [11, 16, 68]. This method has some distinct merits over the previous mentioned methods, such as relatively high filtering capability and a frequency adaptive performance. However, due to the presence of the two interdependent nonlinear loops, the fine-tuning of the PLL's PI-controllers and the choice of the LPFs cut-off frequencies is a challenging task when compared with the other OSG algorithms [16, 100]. Additionally, the OSG output signals will never be in-quadrature unless the PLL is synchronized, which delays the transient process [70].

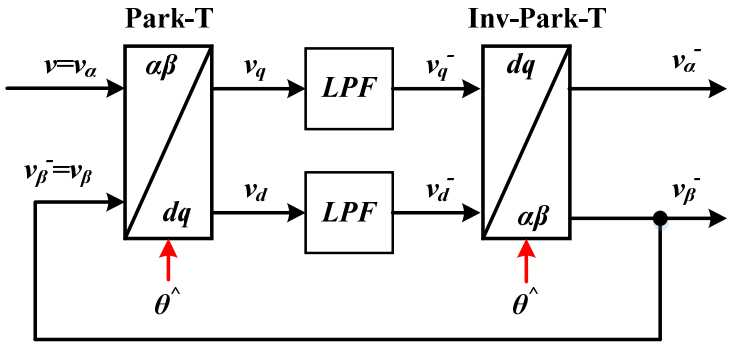


Figure 2.15. Inverse Park Transform-based OSG

2.4.4.4 *Other OSG techniques*

2.4.4.4.1 *Hilbert-transform*

Also called a 'quadrature filter', while this approach works well under ideal operation conditions, it has some shortcomings; high sensitivity to the grid frequency variations [103] and high real-time computation on the control system [100].

2.4.4.4.2 *All-pass filter*

Despite this approach not being affected by the grid frequency variations, it does not provide any filtering capability, thus the performance can be degraded with line-frequency harmonics [68].

2.4.4.4.3 *Kalman filter*

Despite the advantage it offers under frequency variation conditions, this technique however, suffers from high complexity and computational load [68, 104].

2.4.4.5 *Second-Order Generalized Integrator-based OSG*

The current state-of-the-art in OSGs is based on the second-order generalised integrator (SOGI) topology, which proves to have a very good performance, easy to design and digitally implement, low computational burden, insensitivity to frequency variations, and high filtering capability without delay [11, 68, 105]. Therefore, the OSG-PLL structure based on the SOGI has been chosen as the most promising candidate for the single-phase grid voltage synchronisation in this thesis. A more comprehensive study of the theory, the design, the implementation and the operation of the OSG-SOGI are presented and verified in the next chapters by both simulations and experiments. In addition, more improvements will be added to tackle issues such as dc offset.

2.5 Summary

Synchronisation is very important for grid-connected power converters and for controlling the power flow. In this chapter, several common synchronisation methods suitable for single-phase applications have been discussed. The issue of the high-amplitude double-frequency oscillations that appear at the estimated quantities by the conventional pPLL in steady-state conditions has been discussed in detail, and some of the previously reported solutions have been examined. One of most promising candidates for successfully solving the aforementioned problem associated with the pPLL without affecting the stability and the transient performance is to make use of the OSG-based PLL. Therefore, several techniques for orthogonal signal generation (OSG) have been presented and compared in terms of dynamic performance. Among various OSG techniques, the second-order generalized integrator SOGI proves to be the best, since it is easy to be digitally implemented, has perfect filtering capability and it is adaptive to frequency changes. Thus, SOGI-based PLL has been chosen to be used to perform the synchronisation unit required for this project. The theory, design, implementation and operation of the OSG-SOGI will be presented and verified in the forthcoming chapters by both simulations and experiments.

CHAPTER 3

Second Order Generalized Integrator-PLL (SOGI-PLL)

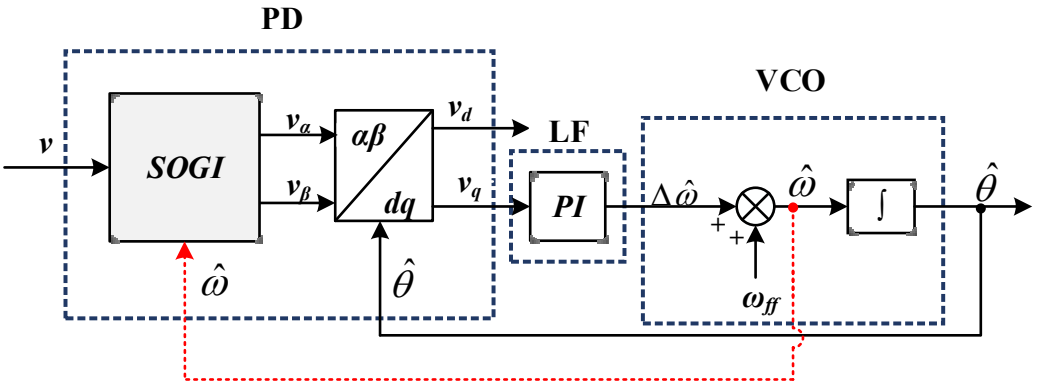
3.1 Introduction

This chapter considers the use of the SOGI-PLL as one of the advanced phase-locked loop (PLL) techniques that have been recently proposed for grid synchronisation in single-phase grid-connected PV systems. Despite the wide acceptance and use of this PLL, no complete design guidelines to fine-tune its parameters has been reported yet. Thus, in this chapter, an overview of the SOGI-PLL along with its structure and principle of operation are firstly presented. A small signal linearized model for SOGI-PLL structure is then derived, where the model significantly simplifies the stability analysis and the parameter design. This is followed by comprehensive design guidelines to fine-tune the PLL parameters ensuring a fast transient response, a high disturbance rejection capability, and a robust performance. Finally, the effectiveness of the proposed design method is evaluated through extensive simulation tests, considering several utility grid disturbances. This leads to a full discussion on the suitability of this technique, in which the major advantages and disadvantages associated with this method are highlighted. This will serve as a background to the research carried out in later chapters.

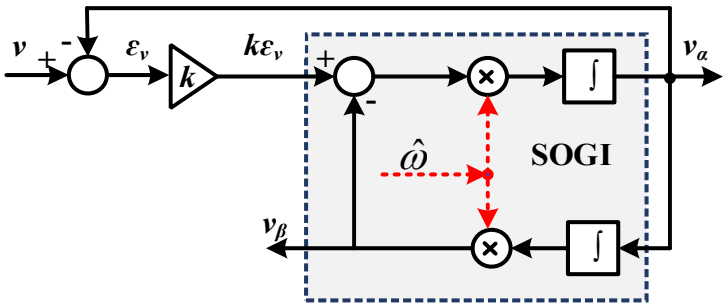
3.2 Overview of the SOGI-PLL structure

The basic configuration of the SOGI-PLL proposed in [97], is depicted in Figure. 3.1 (a), in which v is the input voltage, $\hat{\omega}$ and $\hat{\theta}$ are the estimated frequency and angle, respectively, and ω_{ff} is the feed-forward nominal frequency. The implementation of the SOGI block is shown in Figure. 3.1(b), and the Park ($\alpha\beta \rightarrow dq$) transformation is defined as follows

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}) & sin(\hat{\theta}) \\ -sin(\hat{\theta}) & cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.1}$$



(a)



(b)

Figure 3.1. SOGI-PLL: (a) Basic structure and (b) SOGI block.

From the adaptive filtering structure shown in Figure.3.1 (b), the characteristic transfer functions of the SOGI block can be defined as

$$G_{SOGI}(s) = \frac{v_\alpha}{k\varepsilon_v}(s) = \frac{\hat{\omega}s}{s^2 + \hat{\omega}^2} \tag{3.2}$$

$$G_\alpha(s) = \frac{v_\alpha}{v}(s) = \frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{3.3}$$

$$G_\beta(s) = \frac{v_\beta}{v}(s) = \left(\frac{\hat{\omega}}{s}\right)\frac{v_\alpha}{v}(s) = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} \tag{3.4}$$

where:

$k = 2\xi$: is a real positive constant gain, and commonly referred to as the SOGI damping factor, and, $\hat{\omega}$: is the centre frequency of the SOGI provided by the PLL.

Figure. 3.2 (a) and (b) shows the frequency response of transfer functions (3.3) and (3.4), respectively, for three different values of the damping factor k and for $\hat{\omega} = 2\pi.50$ rad/s.

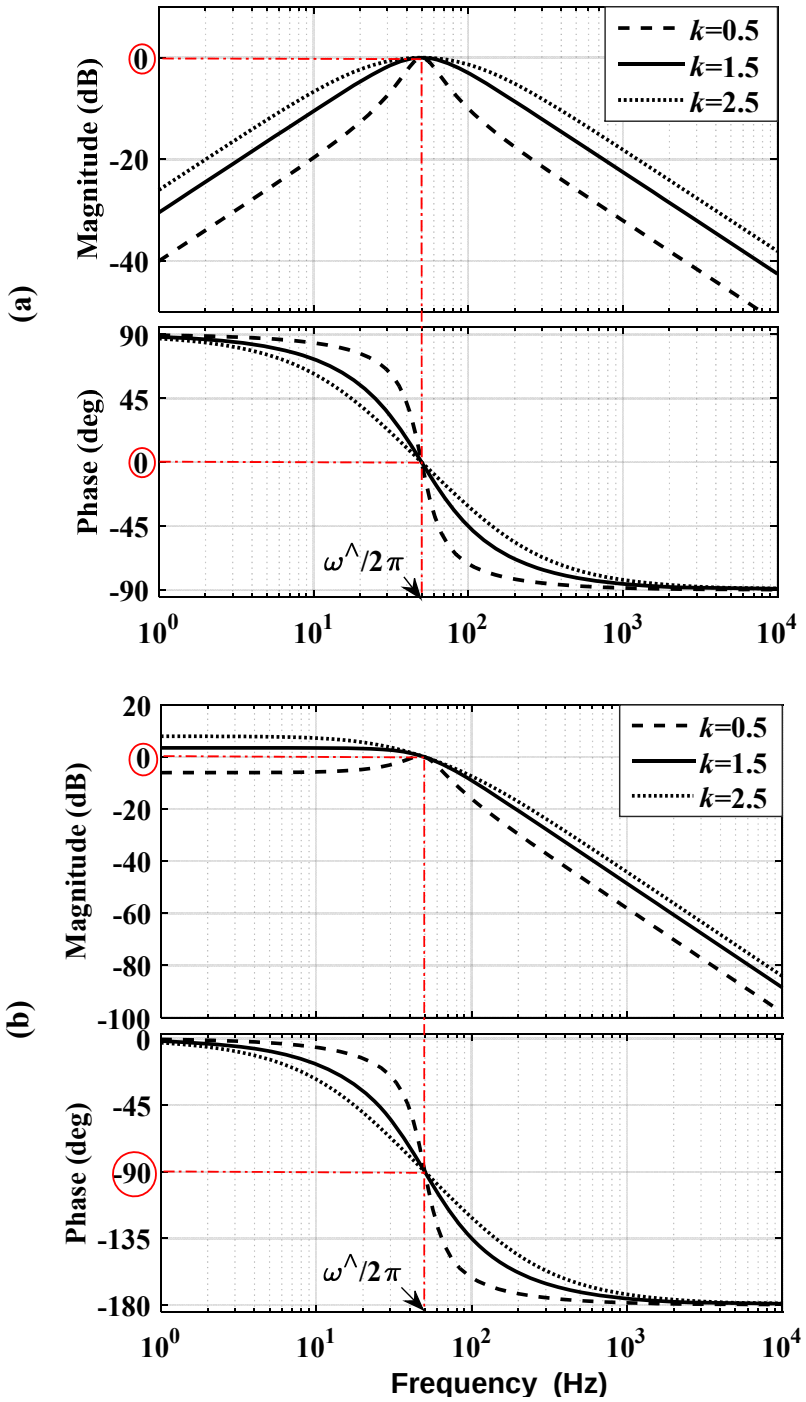


Figure 3.2. Frequency response of the characteristic transfer functions of the SOGI block for different values of gain k: (a) $G_\alpha(s)$ and (b) $G_\beta(s)$.

Based on these plots, the following can be concluded.

1) The transfer function $G_\alpha(s)$ exhibits a band-pass filtering characteristic with a centre frequency of $\hat{\omega}$. The sharpness (or bandwidth) of the passband is not a function of the centre frequency $\hat{\omega}$ but it is only determined by the gain k. In addition, it can be observed that, a lower k leads to a narrower bandwidth, and hence, better filtering capability [11, 97]. However, with a very low value of k, the dynamic performance of the PLL will be significantly degraded. Furthermore, If the estimated frequency $\hat{\omega}$ somehow arranged to matches the input frequency ω, then the in-phase signal v_α will have the same amplitude as the fundamental component of the input voltage v, with no phase shift.

2) The transfer function $G_\beta(s)$ exhibits a low-pass filtering characteristic. It offers better filtering characteristics for the high-frequency harmonics when compared with $G_\alpha(s)$, (i.e., $G_\beta(s)$ decays at rate of -50 dB/dec while $G_\alpha(s)$ decays with a rate of -20 dB/dec at high frequencies). However, the filtering characteristic of $G_\beta(s)$ at low-frequencies, (i.e., sub-harmonics from zero to 50Hz) is extremely degraded. On the contrary to $G_\alpha(s)$, the transfer function $G_\beta(s)$ suffers from a nonzero dc offset when the input signal contains a dc component. The amplitude of this offset is equal to the gain k times that of the input dc component. Again, if $\hat{\omega} = \omega$, then v_β will match the input voltage fundamental component amplitude but with a 90° phase shift.

To evaluate the time response of the SOGI of Figure.3.1 (b), let us assume that $v = V_m \cos\theta$. Hence, under a frequency-locked condition (i.e., $\hat{\omega} = \omega$) and for $0 \leq k < 2$, the mathematical expressions for the output signals of the SOGI defined by the transfer functions (3.3) and (3.4) when the input voltage v is suddenly applied are given by

$$v_\alpha(t) = V_m \cos\theta + A_\alpha e^{-\frac{k\omega}{2}t} \tag{3.5}$$

$$v_\beta(t) = V_m \sin\theta + A_\beta e^{-\frac{k\omega}{2}t} \tag{3.6}$$

where:

V_m , ω, and θ are the input voltage amplitude, angular frequency, and phase-angle, respectively. A_α, A_β , ϕ_α and ϕ_β are functions of V_m and k, which can be expressed as

$$\begin{cases} A_\alpha = \dfrac{V_m}{\sqrt{1-\left(\frac{k}{2}\right)^2}} cos\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\, t + \phi_\alpha\right) \\ A_\beta = \dfrac{V_m}{\sqrt{1-\left(\frac{k}{2}\right)^2}} sin\left(\omega\sqrt{1-\left(\frac{k}{2}\right)^2}\, t + \phi_\beta\right) \\ \phi_\alpha = \phi_\beta = arctan\dfrac{k/2}{\sqrt{1-(k/2)^2}} \end{cases} \tag{3.7}$$

As expected, in steady-state, v_α and v_β are in-phase and quadrature-phase with the input voltage v, respectively.

The estimated settling time t_s for a step response of $G_\alpha(s)$ and $G_\beta(s)$ to stabilise within a tolerance band of (2%) can be determined for different values of gain k from the derived step response expressions shown in Appendix C. Figure.3.3 illustrates the settling time versus k when and $\hat{\omega} = \omega$ =2π.50 rad/s.

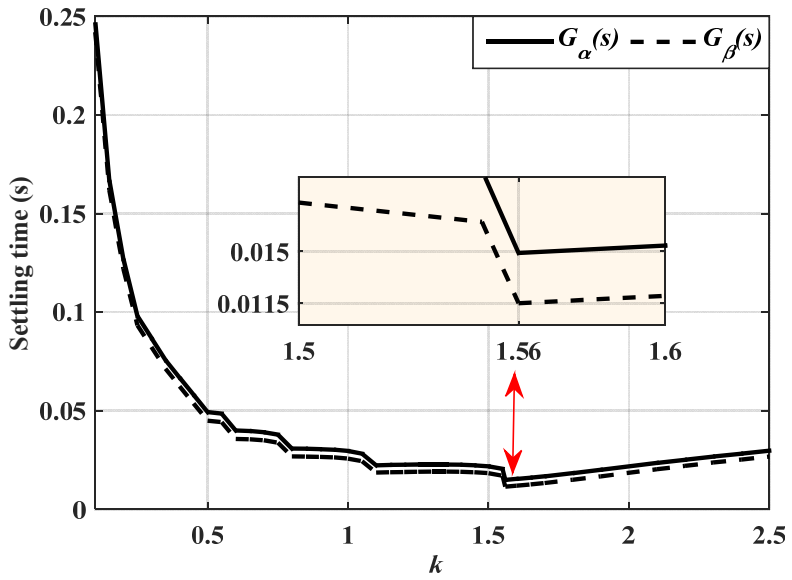


Figure 3.3 Settling time t_s versus gain k

It can be observed from Figure. 3.3 that the variation of the settling time versus k is not smooth and has jumps, and a small change in k will not always result in a proportional change in the settling time. In addition, it can be deduced that minimum settling time for both $G_\alpha(s)$ and $G_\beta(s)$ occurs when $k \approx 1.56$. Thus, by setting the gain k at its optimal value of 1.56, the transients due to the SOGI block can die out faster than other values.

Figure.3.4. shows the waveforms of (3.5) and (3.6) for three different values of k, (i.e., k =1, k =1.56 and k =2) and when $\hat{\omega} = \omega$ =2π.50 rad/s. As it can be observed that the minimum settling time occurs for k =1.56. These results roughly match the value obtained from Figure.3.3. It is worth noting that the lower the factor k is, the higher is the disturbance rejection capability, and hence, the better is the filtering property, but at the expense of the system dynamic response.

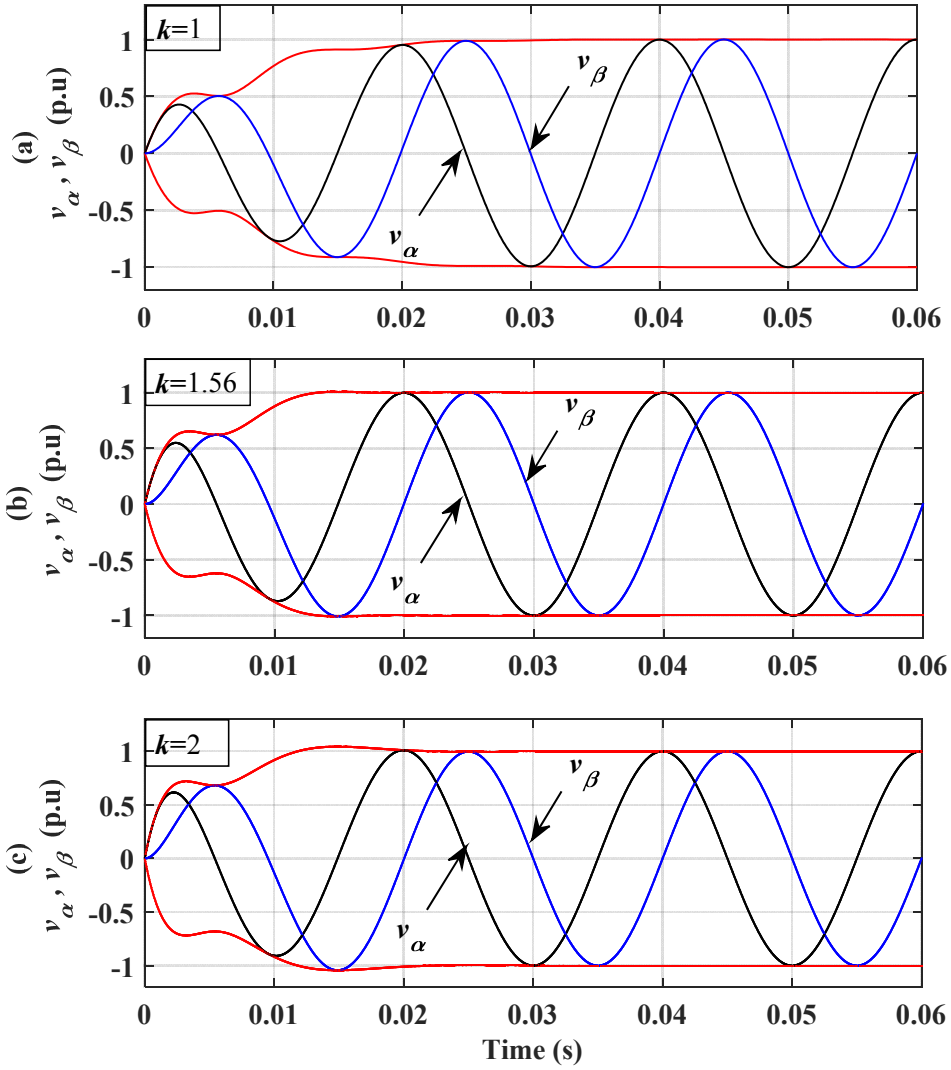


Figure 3.4. Response of the SOGI-OSG for different values of gain k: (a) (k=1), (b) (k=1.56) and (c) (k=2).

A unitary step response of the transfer function of (3.3) and (3.4) for three different values of k, (i.e., k =1, k =1.56 and k =2) and in the case where $\hat{\omega}$ = 2π.50 rad/s, is shown in Figure. 3.5. It can be observed that the settling time almost agrees with the values obtained from Figure.3.3 and Figure.3.4.

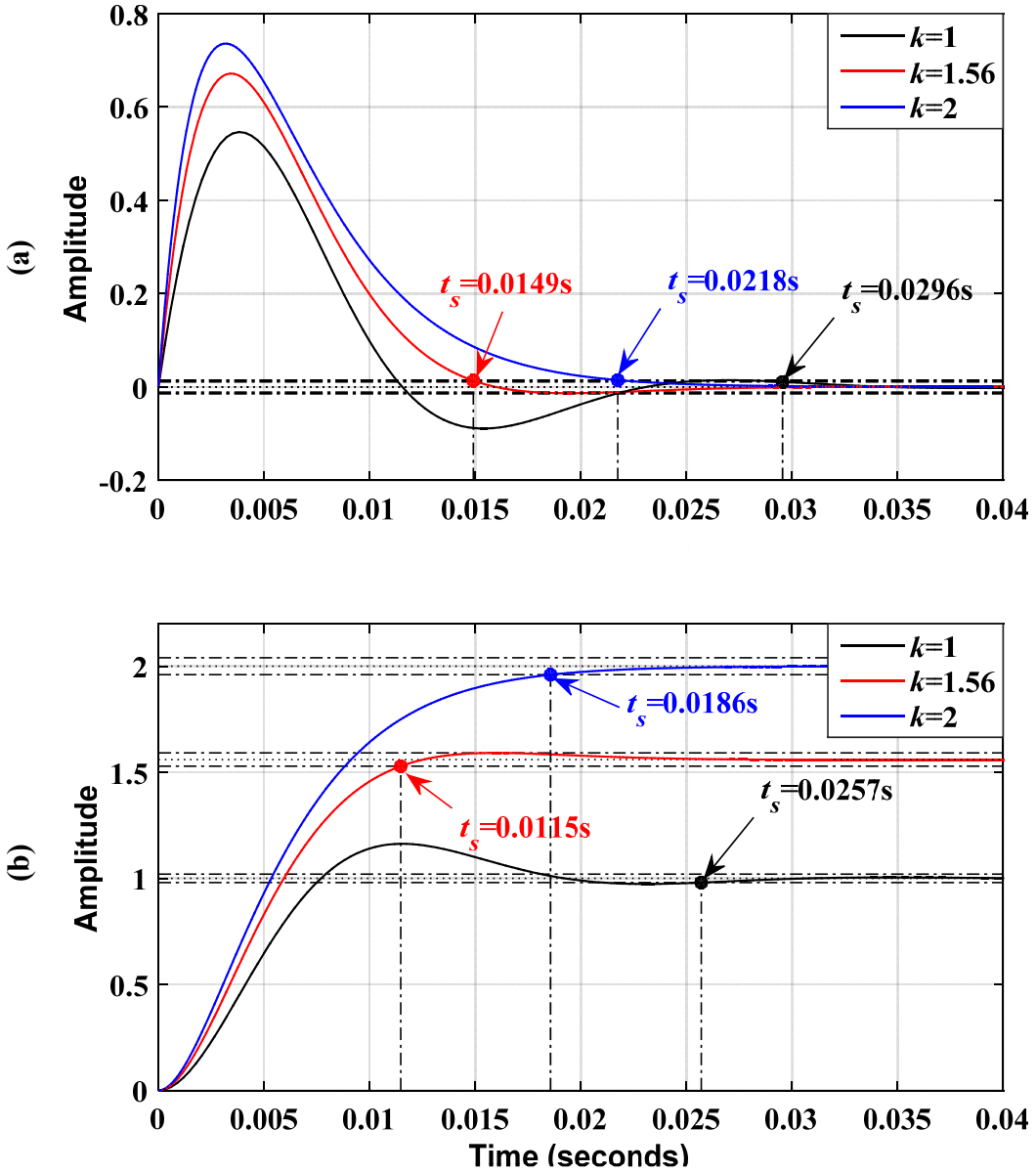


Figure 3.5. Step response of the characteristic transfer functions of the SOGI block for different values of gain k: (a) $G_\alpha(s)$ and (b) $G_\beta(s)$.

Now, by applying Park's transformation matrix (3.1) to (3.5) and (3.6) yields v_d and v_q signals as expressed in

$$v_d(t) = V_m\, cos(\theta_e) + \left[A_\alpha \cos\hat{\theta} + A_\beta \sin\hat{\theta}\right] \times e^{-\frac{k\omega}{2}t} \tag{3.8}$$

$$v_q(t) = V_m\, sin(\theta_e) - \left[A_\alpha \sin\hat{\theta} - A_\beta \cos\hat{\theta}\right] \times e^{-\frac{k\omega}{2}t} \tag{3.9}$$

where $\theta_e = \theta - \hat{\theta}$

From (3.8) and (3.9), it can be seen that in steady-state conditions, the fluctuating terms on the right-hand side, decay to zero with a time constant of $\tau_p = 2/k\omega$. Besides, $v_d(t)$ converges to $V_m\, cos(\theta_e)$ which yields an estimation of the input voltage amplitude, and $v_q(t)$ converges to $V_m\, sin(\theta_e)$ which represents the steady-state phase error information.

Now, to further attenuate the high-frequency noise which may exist in the input voltage v, the PD output signal, i.e., v_q, is passed through the LF (here, a proportional–integral controller). To reduce the control effort and accelerate the initial lock-in process, the feedforward fundamental frequency ω_{ff} is then added to the PI-controller output signal. The resulting estimated frequency $\hat{\omega}$ is then integrated afterward, to generate the estimated phase angle $\hat{\theta}$. The PI-controller's gains are designed so that in steady-state conditions v_q is regulated to zero and the estimated frequency is locked on the system frequency (i.e., $\omega = \hat{\omega}$). As a result and for a small difference between the real and estimated phase angles θ_e, the term $sin(\theta_e)$ can be approximated by $sin(\theta_e) \cong \theta_e$. Thus, the PLL can be treated as a liner control system with the input voltage amplitude V_m appearing as a gain in the forward path. A linearized model will be developed in the next section.

3.3 Linearized Small Signal Model

In this section, a generic linearized model for SOGI-PLL is presented. It is worth noting that, since the bandwidth of the PLL is much lower than its sampling frequency, the *s*-domain analysis/tuning can provide accuracy as good as that achievable in the *z*-domain. Besides, from the analysis/tuning point of you, using the Laplace domain is more convenient and straight forward than that in the *z*-domain [66]. For these reasons, the analysis/tuning of the linearized model of the PLL will be performed in the *s*-domain.

To derive the linearized model, the following assumptions are considered.

1) The estimated frequency is almost equal to the input frequency (i.e., $\omega = \hat{\omega}$).

2) There is a small difference between the real and estimated phase angles; thus, $\sin(\theta_e) \cong \theta_e$, and $\cos(\theta_e) \approx 1$.

3) The input voltage v is considered to be harmonic polluted (i.e., as a result of the propagation of non-linear loads in power systems), and is represented by

$$v = \underbrace{V_m \cos\theta}_{\text{Fundamental component}} + \underbrace{\sum_{h=3,5,7,\ldots..} V_h \cos\theta_h}_{\text{Harmonic components}} \tag{3.10}$$

where V_h, and θ_h represent the amplitude, and phase angle of the h^{th} harmonic component, respectively.

Initially, the harmonic components are neglected and only the fundamental component of (3.10) is considered as the input voltage. In this case, the PD output signal (i.e., v_q) is as stated in (3.11). Note that, in (3.11), the oscillating terms decay to zero with a time constant of $\tau_p = 2/k\omega$ and v_q converges to $V_m\theta_e$. Thus, for a sudden phase change, the PD output signal, i.e., v_q, can be approximated in the s domain as

$$v_q(s) \cong \frac{V_m}{\tau_p s + 1}\theta_e(s) \tag{3.11}$$

Now, once the PD response to the fundamental component is determined, the next step is to take into consideration the steady-state effect of the harmonics on the variables estimated by the PLL. It is important to notice that, in the steady-state condition, each input harmonic component of order h and amplitude of V_h produces two different components of orders h±1 in the PD output signal, i.e., v_q, with amplitudes of V_{h1} and V_{h2} [17, 68]. This can be mathematically expressed as

$$v_q(t) = V_{\text{h1}}\cos\left[\theta_h - \hat{\theta} + \theta_{h\beta}\right] - V_{\text{h2}}\cos\left[\theta_h + \hat{\theta} + \theta_{h\beta}\right] \tag{3.12}$$

where

V_{h1} and V_{h2} are the amplitudes of the two produced harmonic components, which can be expressed as

$$\begin{cases} V_{\text{h1}} = \dfrac{V_{h\beta}V_h}{2}(h+1) \\ V_{\text{h2}} = \dfrac{V_{h\beta}V_h}{2}(h-1) \end{cases} \tag{3.13}$$

and $V_{h\beta}$ and $\theta_{h\beta}$ denote the magnitude and the phase angle of the transfer function $G_\beta(s)$ in (3.4), respectively, for $s = jh\omega$. Consequently, the PD output signal, i.e., v_q, for a small angle difference θ_e, when the input voltage consists of fundamental component and harmonic components, can be approximated as follows:

$$v_q(s) \cong \left\{ \frac{V_m}{\tau_p s + 1} \theta_e(s) \right\} + D(s) \tag{3.14}$$

where, $D(s)$ is the Laplace transform of the harmonic function $g(2\omega, 4\omega, 6\omega, \ldots\ldots)$, which appears as a disturbance input to the SOGI-PLL linearized model.

Based on the above analysis, a generic block diagram of the linearized model of the SOGI-PLL can be obtained as shown in Figure. 3.6, where k_p and k_i are the gains associated with the PI regulator. It is worth mentioning here that the derived linearized model is strongly accurate for a k within the range of $0 \leq k < 2$. It is reported that, outside this range, the precision of the model starts to decline [68].

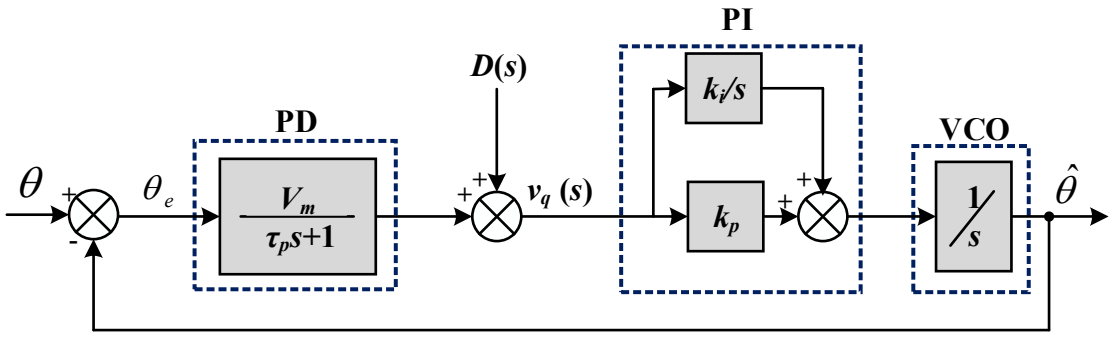


Figure 3.6. Linearized model of the SOGI-PLL

3.4 Design Guidelines

In this section, an efficient design method to fine-tune the PLL parameters (i.e., k_p, k_i, and τ_p) is introduced, such that the system stability is guaranteed, and in addition to an appropriate transient performance, and high disturbance rejection capability.

Notice that, in the linearized model shown in Figure.3.6, the amplitude of the input voltage V_m, contributes as a gain term in the forward path. Thus, under voltage sag conditions, there will be a gain loss significantly affecting the PLL stability and dynamic performance. This undesirable effect can be alleviated by compensating the PD output signal, i.e., v_q, before it is fed into the LF with an amplitude estimation method, as reported in [17]. A block diagram of the suggested amplitude compensation scheme is depicted in Figure.3.7. As shown, by dividing v_q by the estimated amplitude V_m, the input voltage amplitude can be guaranteed to be always unity during the steady-state condition. In addition, to avoid instability issues, the estimated

amplitude V_m is limited by a saturation block with upper and lower limits tuned according to the allowable range of input voltage amplitude variations [17].

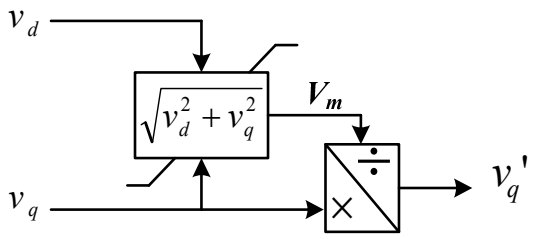


Figure 3.7. An amplitude compensation block

Based on the above discussion, a modified linearized model with unity input voltage amplitude V_m and with $D'(s)$ as a disturbance input to the linearized model, is illustrated in Figure.3.8, where $D'(s) = D(s)/V_m$. In this case, (3.14) becomes (3.15).

$$v_q'(s) \cong \left\{\frac{1}{\tau_p s + 1}\theta_e(s)\right\} + D'(s) \tag{3.15}$$

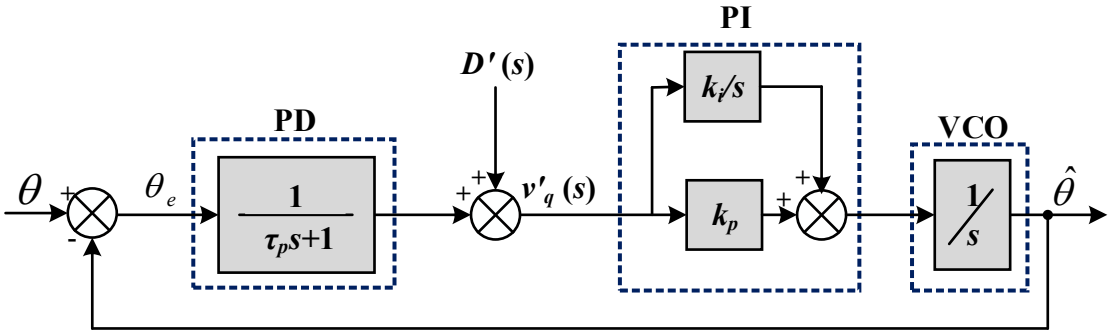


Figure 3.8. Modified linearized model

3.4.1 Stability

In the recent literature, several methods for designing the PI-controller parameters have been presented [106]. In this section, a systematic approach based on the symmetrical optimum method (SO) is proposed to fine-tune the PLL parameters. The idea behind this method is to optimize the phase margin (PM) to obtain its maximum at a given crossover frequency [107, 108].

From Figure.3.8, bearing in mind $\tau_i = (k_p/k_i)$, the open-loop transfer function of the PLL can be expressed as

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta_e(s)}\bigg|_{D'(s)=0} = \left(\frac{1}{\tau_p s + 1}\right)\left(\frac{k_p s + k_i}{s}\right)\left(\frac{1}{s}\right) = \frac{k_p s + k_i}{s^2(\tau_p s + 1)} = \frac{k_i(1 + \tau_i s)}{s^2(\tau_p s + 1)} \tag{3.16}$$

From (3.16), the amplitude and phase, frequency characteristics can be simply obtained as

$$|G_{ol}(j\omega)| = \frac{k_i}{\omega^2}\sqrt{\frac{(\tau_i\omega)^2 + 1}{(\tau_p\omega)^2 + 1}} \tag{3.17}$$

$$\measuredangle G_{ol}(j\omega) = tan^{-1}(\tau_i\omega) - 180^{\circ} - tan^{-1}(\tau_p\omega) \tag{3.18}$$

Therefore, the maximum PM can be expressed as

$$PM_{max} = \measuredangle G_{ol}(j\omega_c) + 180^{\circ} = \underbrace{tan^{-1}(\tau_i\omega_c)}_{\phi_i} + \underbrace{tan^{-1}(\tau_p\omega_c)}_{\phi_p} \tag{3.19}$$

where ω_c is the crossover frequency which is determined by differentiating (3.19) with respect to ω_c, i.e., $\partial(PM)/\partial(\omega_c)$ and equating the result to zero, yields

$$\omega_c = \frac{1}{\sqrt{\tau_i\tau_p}} \tag{3.20}$$

From (3.20), and supposing that, $\tau_i = \left(\frac{1}{\omega_c^2\tau_p}\right) = \lambda^2\tau_p$ where λ is a constant term, the following can be obtained

$$\begin{cases} \tau_i/\tau_p = \lambda^2 \\ \tau_i\omega_c = \lambda \\ \tau_p\omega_c = \dfrac{1}{\lambda} \end{cases} \tag{3.21}$$

Substituting (3.21) into (3.19), PM_{max} can be rewritten as

$$PM_{max} = tan^{-1}(\lambda) - tan^{-1}\left(\frac{1}{\lambda}\right) = tan^{-1}\left(\frac{\lambda^2 - 1}{2\lambda}\right) \quad (3.22)$$

Based on (3.22), the relationship between the factor λ and the phase margin PM is displayed in Figure.3.9. It can be seen that the higher the factor λ is, the higher is the phase margin, and hence, a more stable operation.

Figure 3.9. Phase margin versus factor λ

Typically, for a good stability a PM within the range of 30°< PM <60° is recommended [109]. To meet this, λ is required to be within the range of 1.732 < λ < 3.732 as highlighted in Figure.3.9.

Now, the PI-regulator parameters (i.e., k_p, k_i) are determined as a function of the factor λ and the time constant τ_p, by considering (3.20) and (3.21). By equating (3.17) to 1 when $\omega = \omega_c$, then the following equations are obtained

$$\begin{cases} k_i = \dfrac{1}{\lambda^3 \tau_p^2} \\ k_p = \tau_i k_i = \dfrac{1}{\lambda \tau_p} = \omega_c \end{cases} \quad (3.23)$$

From (3.23), it can be observed that, both k_p and k_i are functions of λ and τ_p. Furthermore, it can be concluded that, for given values of τ_i and τ_p, the PM of the PLL is maximized when the proportional gain k_p is equal to the crossover frequency ω_c. This can be observed graphically from the Bode-plot of the PLL open-loop transfer function as shown in Figure.3.10.

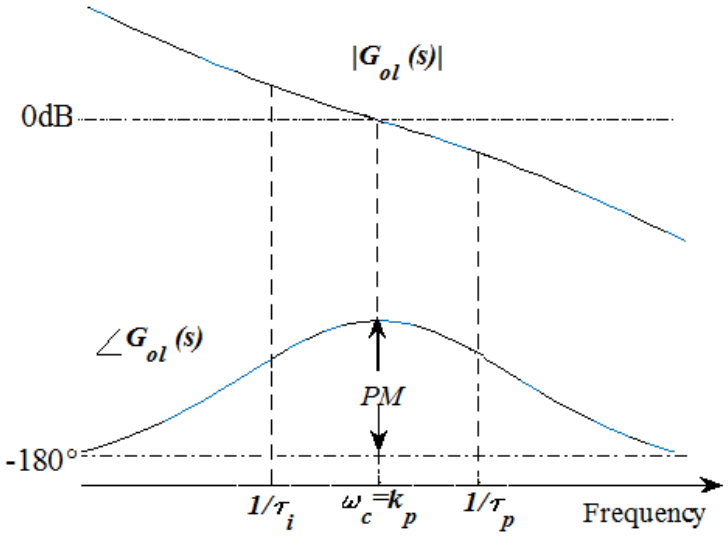


Figure 3.10. Logarithmic plot of the open-loop transfer function

Figure.3.11 illustrates the Bode-plot of the open-loop transfer function (3.16) for two different values of λ and for a given crossover frequency ω_c =100rad/s, confirming the same PM values obtained from Figure.3.9.

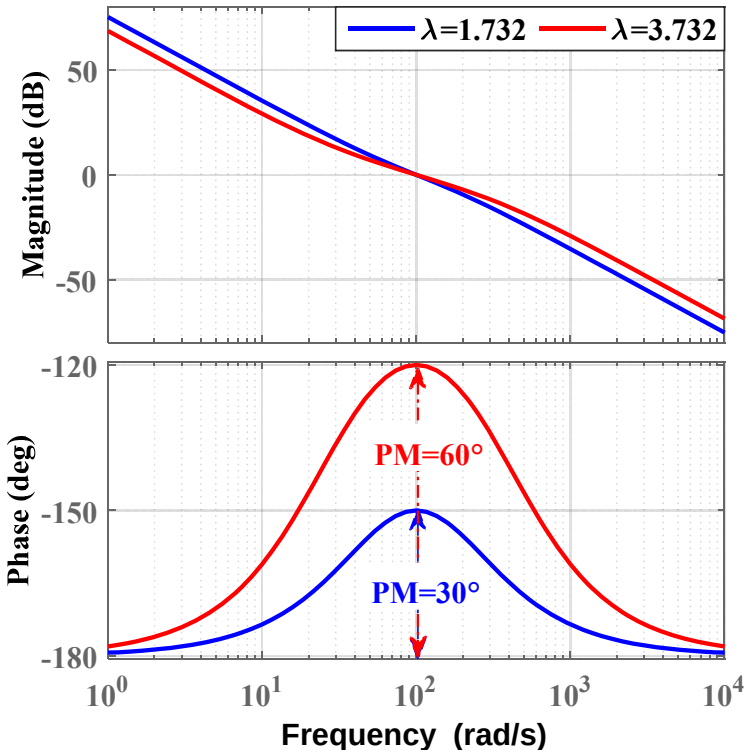


Figure 3.11. Bode-plot of the open-loop transfer for two different values of λ

Now, once the PI parameters k_p and k_i are obtained as a function of λ and τ_p, the next step is to determine the value of λ and τ_p. The selection of these parameters will be discussed in the next two sub-sections.

3.4.2 Transient Performance

The main emphasis of this sub-section is to optimize the PLL transient performance so that the settling time in response to both phase and frequency step changes is minimized.

Substituting (3.23) into (3.16), the open-loop transfer function $G_{ol}(s)$ can be rewritten as

$$G_{ol}(s) = \frac{\hat{\theta}(s)}{\theta_e(s)}\bigg|_{D'(s)=0} = \frac{\lambda\omega_c^2 s + \omega_c^3}{s^2(s+\lambda\omega_c)} \tag{3.24}$$

It can be seen that (3.24) is a typical open-loop transfer function of a type-II system (i.e., there are two poles at the origin). Thus, the PLL tracks both phase jump (step input) and frequency jump (ramp input) with guaranteed zero steady-state error [110].
From Figure. 3.8, the phase error transfer function relating the phase error ϕ_e to the phase input ϕ can be derived as

$$G_e(s) = \frac{\theta_e(s)}{\theta(s)}\bigg|_{D'(s)=0} = 1 - \frac{\hat{\theta}(s)}{\theta(s)}\bigg|_{D'(s)=0} = \left(\frac{1}{1+G_{ol}(s)}\right) \tag{3.25}$$

Substituting (3.24) into (3.25), and after some mathematical simplifications, yields

$$\begin{aligned} G_e(s) &= \frac{s^2(s+\lambda\omega_c)}{s^2(s+\lambda\omega_c) + \lambda\omega_c^2 s + \omega_c^3} \\ &= \frac{s^2(s+\lambda\omega_c)}{(s+\omega_c)(s^2 + (\lambda-1)\omega_c s + \omega_c^2)} \end{aligned} \tag{3.26}$$

and (3.26) can be rewritten in a normalised way as

$$G_e(s) = \frac{s^2(s+(2\xi+1)\omega_n)}{(s+\omega_n)(s^2+2\xi\omega_n s+\omega_n^2)} \tag{3.27}$$

where: $\omega_n = \omega_c$ is the natural frequency and $\xi = (\lambda-1)/2$, is the PLL damping factor.

Using (3.27), the Laplace transforms of the phase error $\theta_e(s) = G_e(s)\theta(s)$, resulting from phase $\Delta\phi$ and frequency $\Delta\omega$ jump changes, can be simply obtained as expressed in (3.28) and (3.29), respectively

$$\theta_e^{\Delta\phi}(s) = \frac{\Delta\phi}{s} G_e(s) = \frac{s(s + (2\xi + 1)\omega_n)\Delta\phi}{(s + \omega_n)(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{3.28}$$

$$\theta_e^{\Delta\omega}(s) = \frac{\Delta\omega}{s^2} G_e(s) = \frac{(s + (2\xi + 1)\omega_n)\Delta\omega}{(s + \omega_n)(s^2 + 2\xi\omega_n s + \omega_n^2)} \tag{3.29}$$

Taking the inverse Laplace transform of (3.28) and (3.29), yields (3.30) and (3.31) which are the time-domain tracking errors for phase $\theta_e^{\Delta\phi}(t)$ and frequency $\theta_e^{\Delta\omega}(t)$ jumps, respectively.

$$\theta_e^{\Delta\phi}(t) = \begin{cases} \dfrac{\Delta\phi}{\xi - 1}\left[\xi e^{-\omega_n t} - e^{-\xi\omega_n t}\cos\left(\omega_n t\sqrt{1 - \xi^2}\right)\right], & \xi < 1 \\ \Delta\phi\, e^{-\omega_n t}\,(1 + \omega_n t - \omega_n^2 t^2), & \xi = 1 \\ \dfrac{\Delta\phi}{\xi - 1}\left[\xi e^{-\omega_n t} - \dfrac{1}{2} e^{-\left(\xi - \sqrt{\xi^2 - 1}\right)\omega_n t} - \dfrac{1}{2} e^{-(\xi + \sqrt{\xi^2 - 1})\omega_n t}\right], & \xi > 1 \end{cases} \tag{3.30}$$

$$\theta_e^{\Delta\omega}(t) = \begin{cases} \dfrac{\Delta\omega}{(\xi - 1)\omega_n}\left[\xi e^{-\omega_n t} + e^{-\xi\omega_n t}\begin{Bmatrix} -\xi\cos\left(\omega_n t\sqrt{1 - \xi^2}\right) + \\ \sqrt{1 - \xi^2}\sin\left(\omega_n t\sqrt{1 - \xi^2}\right) \end{Bmatrix}\right], & \xi < 1 \\ \dfrac{\Delta\omega}{\omega_n} e^{-\omega_n t}\,(\omega_n t + \omega_n^2 t^2), & \xi = 1 \\ \dfrac{\Delta\omega}{(\xi - 1)\omega_n}\left[\xi e^{-\omega_n t} - \dfrac{\xi + \sqrt{\xi^2 - 1}}{2} e^{-\left(\xi - \sqrt{\xi^2 - 1}\right)\omega_n t} - \dfrac{\xi - \sqrt{\xi^2 - 1}}{2} e^{-\left(\xi + \sqrt{\xi^2 - 1}\right)\omega_n t}\right], & \xi > 1 \end{cases} \tag{3.31}$$

From (3.30) and (3.31), it is evident that, for both phase and frequency jumps and for all values of ζ, the PLL transient behaviour can be improved by increasing the natural frequency ω_n (i.e., t_s is proportional to ω_n). Thus, to achieve a faster transient response, ω_n should be chosen as high as possible. However, a high value of ω_n reduces the disturbance rejection capability of the PLL. Hence, a well-balanced trade-off between system dynamics and rejection of harmonic components must be met.

Since the appropriate operation of the PLL in terms of stability requires $1.732 < \lambda < 3.732$ and, hence, $0.366 < \xi < 1.366$, and for a given value of ω_n=135.86rad/s, the relationship between

the damping factor ξ, and the disturbance rejection capability at twice the fundamental frequency can be shown in Figure.3.12. It is clear that, for this range of variation, ξ has a rather small effect on the disturbance rejection capability of the PLL. Therefore, ω_n should be chosen to meet the required disturbance rejection of the PLL, and ξ should be selected according to the transient response and the stability margin requirements of the PLL.

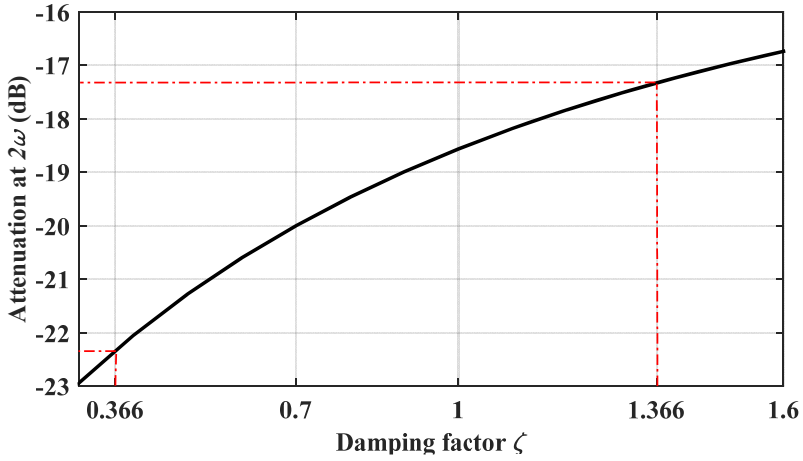


Figure 3.12. Attenuation versus damping factor ξ

Now, the next step is to select the damping factor ξ which provides a fast transient response as well as a stable operation for both phase and frequency step changes. Figure.3.13 illustrates the simulated settling time (which has been normalized by a factor of ω_n) as a function of ξ, for both phase and frequency jumps. Obviously, for underdamped conditions (i.e., $\zeta < 1$), both phase and frequency jumps have almost identical settling times. However, for overdamped conditions (i.e., $\zeta > 1$), a longer settling time is observed for the frequency jump. As highlighted in Figure. 3.13, the minimum settling time for both phase and frequency jumps occurs almost at $\zeta = 0.7$. Thus, in terms of settling time, $\zeta = 0.7$ is recommended as the optimum value of damping factor.

From (3.22), it is clear that the phase margin is only reliant on the factor λ and hence ζ. Therefore, it is important to confirm that the selected value of the damping factor $\zeta = 0.7$, is also a good choice in terms of stability. Substituting $\zeta = 0.7$, which corresponds to $\lambda = 2.4$ into (3.22), yields

$$PM|_{\xi=0.7} = 44.76° \tag{3.32}$$

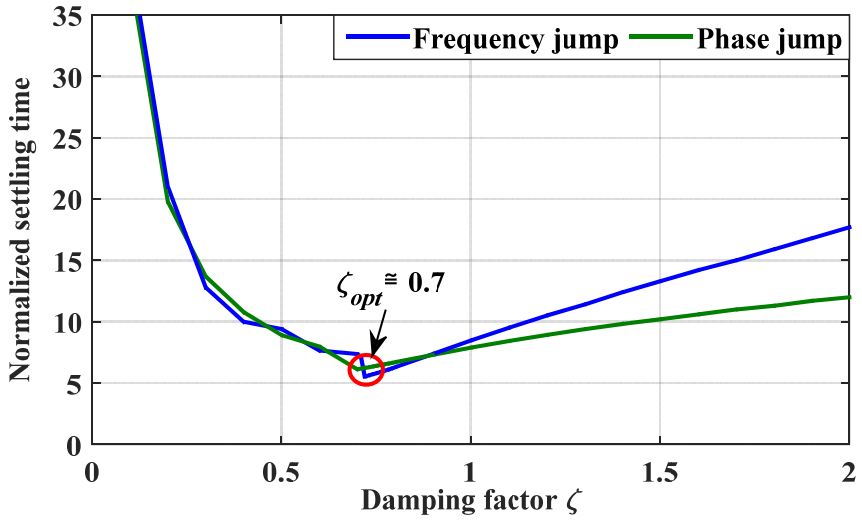


Figure 3.13. Normalized settling time versus damping factor ζ for both phase and frequency jumps.

Since the PM is within the recommended range (30°< PM <60°), the PLL stability is guaranteed. In addition, the Bode-plot of the open-loop transfer function (3.24) for three different values of natural frequency ω_n and when ζ=0.7 is depicted in Figure.3.14, and clearly confirms that the PM is within the desired range.

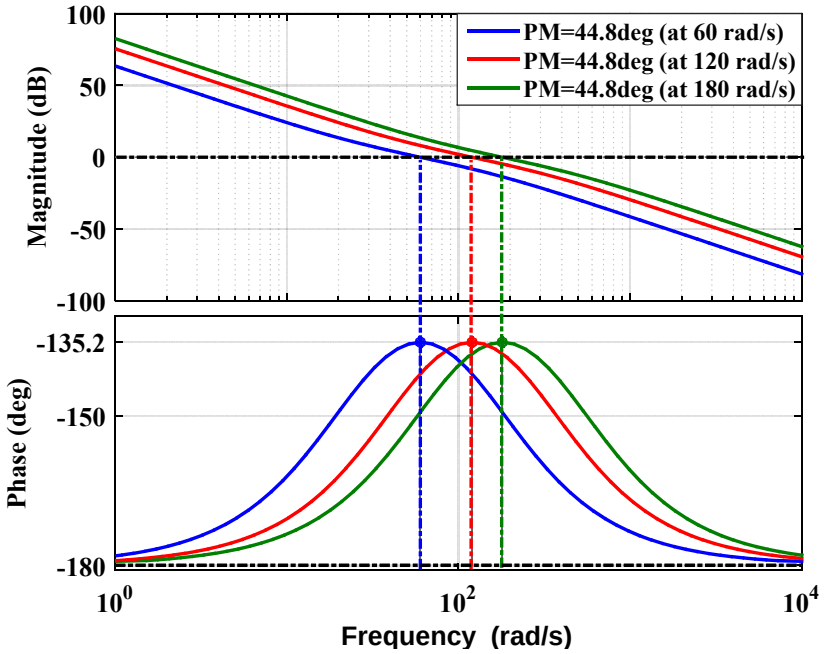


Figure 3.14. Bode-plot of the open-loop transfer function as a function of natural frequency ω_n

3.4.3 Disturbance Rejection

As underlined earlier, the odd harmonics (i.e., 3rd, 5th, 7th, etc.) which are present in the input voltage, will appear to the PLL linearized model as disturbance inputs in the form of even harmonics (i.e., 2nd, 4th, 6th, etc.) as shown in Figure. 3.8. Accordingly, it is essential to select the natural frequency ω_n in such a way that a sufficient attenuation at all concerned disturbance frequencies is provided.

From Figure. 3.8, and remembering that $D'(s) = D(s)/V_m$, the disturbance transfer function relating the estimated phase $\hat{\theta}$ to the disturbance input $D'(s)$ can be simply expressed as

$$G_{D'}(s) = \left.\frac{\hat{\theta}(s)}{D'(s)}\right|_{\theta(s)=0} = \left(\frac{G_{ol}(s)}{1+G_{ol}(s)}\right) = \frac{(2\xi+1)\omega_n^2 s + \omega_n^3}{(s+\omega_n)(s^2+2\xi\omega_n s+\omega_n^2)} \tag{3.33}$$

Figure.3.15 illustrates the Bode-plot of the transfer function (3.33) for three different values of the natural frequency ω_n, and when $\zeta = 0.7$. As shown, the transfer function (3.33) reveals a low-pass filtering features. The lower the natural frequency, the higher the attenuation at the disturbance frequencies is; and hence, the better the filtering capability, but at the expense of the system dynamic response.

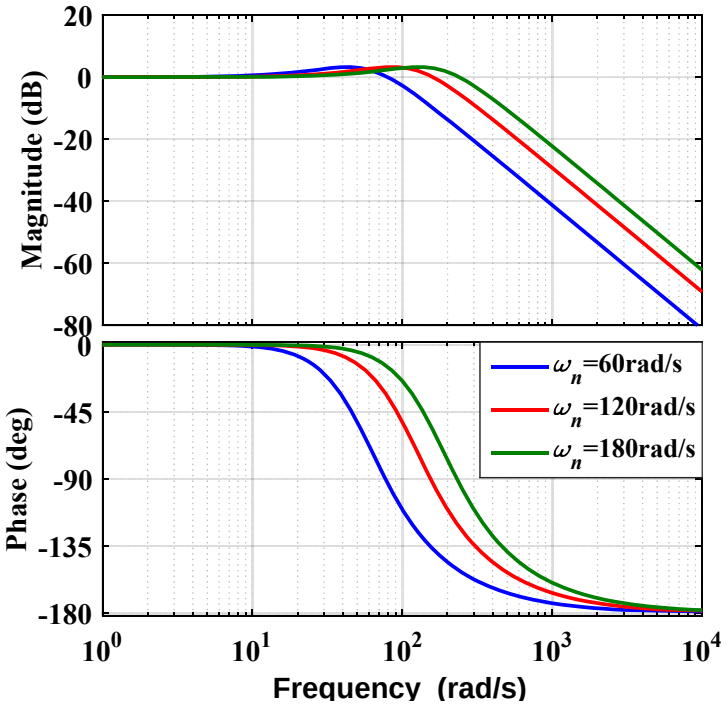


Figure 3.15. Bode-plot of the disturbance transfer function as a function of the natural frequency ω_n.

Owing to the low-pass filtering features of the PLL, provision an adequate attenuation at the lowest disturbance frequency (here, twice the input voltage fundamental frequency i.e., 2ω), ensures a high disturbance rejection capability at other frequencies. Based on (3.17), Figure.3.16 displays the attenuation provided by the PLL at twice the fundamental frequency, as a function of the natural frequency ω_n, for $\zeta = 0.7$. In this work, the desired attenuation to be achieved is chosen to be -20dB, which generally depends on the input voltage distortion level and also on the application where the PLL is used. The selected attenuation requires the natural frequency ω_n (and thus the crossover frequency ω_c) to be equals to 135.86 rad/s (i.e., 21.62Hz) as depicted in Figure.3.16.

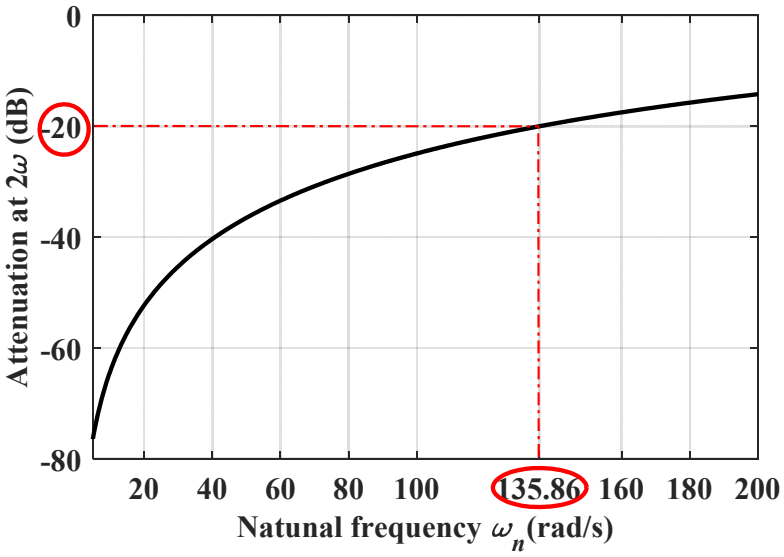


Figure 3.16. PLL attenuation at 2ω versus the natural frequency ω_n

Considering $\omega_c = 135.86$ rad/s, and $\lambda = 2.4$, the PLL parameters k_p , ki , and τ_p can be obtained as

$$\begin{cases} k_p = \omega_c = 135.86 \\ k_i = \dfrac{\omega_c^2}{\lambda} = 7690 \\ \tau_p = \dfrac{1}{\lambda \omega_c} = 3.066e-3s \end{cases} \tag{3.34}$$

From the designed time constant τ_p, the gain k of the SOGI can be simply determined as

$$k = \frac{2}{\tau_p \omega_{ff}} = 2 \tag{3.35}$$

With the designated PLL parameters given in (3.34), the Bode-plots for the open-loop transfer function (OLTF) corresponding to (3.24) and the closed-loop transfer function (CLTF) corresponding to (3.33) are depicted in Figure. 3.17. This confirms that the desired attenuation of -20dB at 100Hz is achieved when the crossover frequency is selected to be 21.62Hz. Also, for the same parameters given in (3.34), a step response of (3.33) is depicted in Figure.3.18 with a settling time of (t_s=45ms).

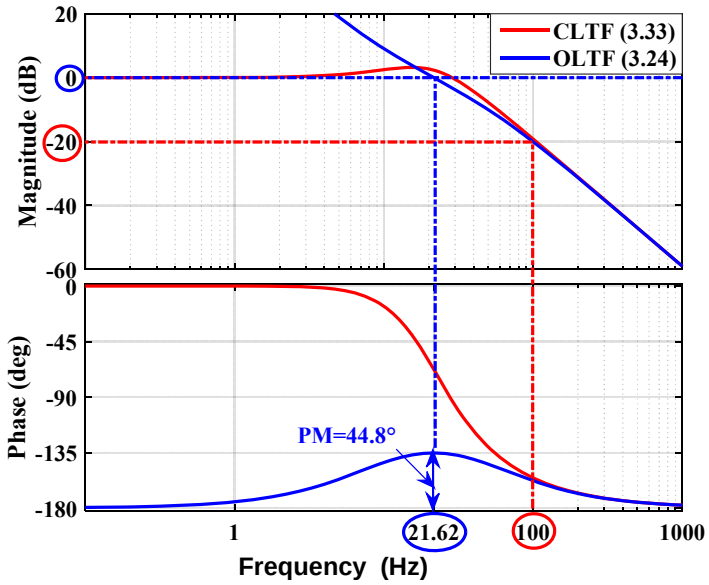


Figure 3.17. Bode-plots of the open-loop (OLTF) and closed loop (CLTF) transfer functions based on the PLL parameters of (3.34)

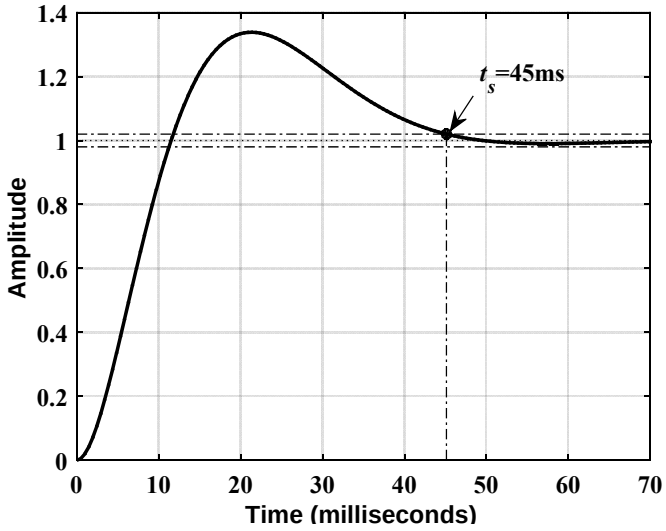


Figure 3.18. PLL response to input step disturbance

In addition, since the design guidelines performed in section 3.4 is based on the derived linearized small-signal model of Figure. 3.8. Thus, it is essential to ensure that this model is

accurate enough. Thus, the SOGI-PLL shown in Figure.3.1 and its linearized model are simulated using Matlab/Simulink with the PLL parameters of (3.34). The obtained results under a phase jump and a frequency step change are compared to each other. The corresponding simulation results are illustrated in Figure. 3.19. It can be observed that the derived model can well predict the transient behaviour of the SOGI-PLL system.

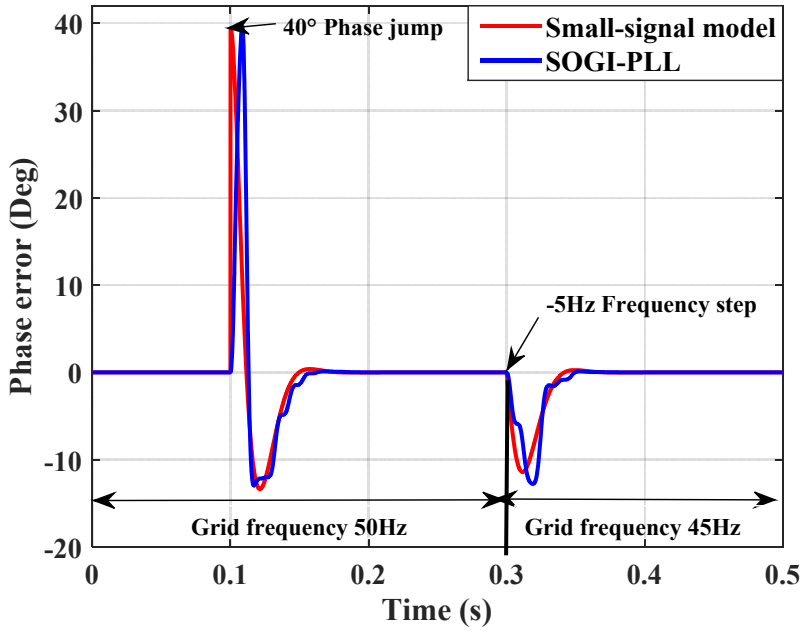


Figure 3.19. Accuracy assessment of the small-signal model of the SOGI-PLL

3.5 Performance Evaluation

In this section, the performance of the proposed design procedure of the SOGI-PLL under different grid scenarios is evaluated through extensive simulations tests carried out in a Matlab / Simulink environment. The simulation model in Simulink environment used for the evaluation is illustrated in Appendix C, and the SOGI-PLL parameters used are found in Table 3-1.

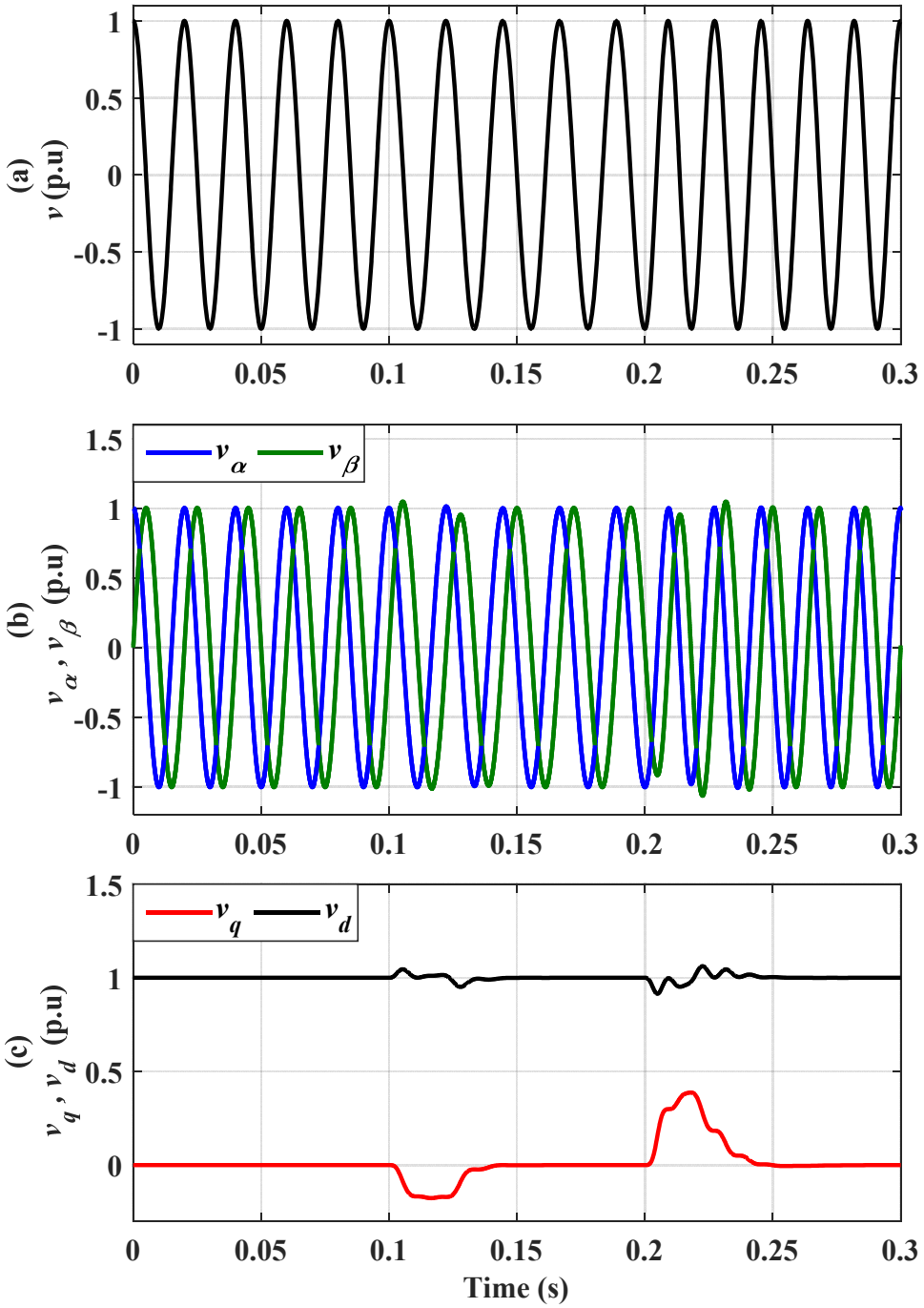
Table 3-1 SOGI-PLL parameters

Parameter	Symbol	Value (unit)
SOGI-OSG gain	k	2
Crossover frequency	ω_c	135.86 rad/s
PLL damping factor	ξ	0.7
Phase margin	PM	44.8°
PLL Proportional gain	k_p	135.86
PLL Integral gain	k_i	7690
Settling time	t_s	0.045s
Nominal frequency	ω	2.π.50 rad/s
Input voltage amplitude	V_m	1 p.u

3.5.1 Frequency Variation

Figure.3.20 shows the response of the SOGI-PLL depicted in Figure.3.1 where the input signal v undergoes frequency step changes (alternating between 45 and 55 Hz) at time =0.1s. In this simulation, the SOGI-OSG gain was set according to (3.35) at k =2, which in theory implies a settling time of roughly 20ms for the SOGI as highlithed earlier in Figures.3.4 and 3.5. The PLL parameters k_p and k_i were calculated according to (3.34) to achieve a settling time of 45ms in the PLL as depicted in Figure.3.18. As shown in Figure.3.20, the SOGI-OSG and the PLL interact with each other and the resulting response is a combination of the action of both systems. This is due to the fact that, in the SOGI-PLL there are two variables $\hat{\omega}$, $\hat{\theta}$ involved in the synchronization procedure, i.e. the SOGI-OSG tuned by using the detected frequency, $\hat{\omega}$, while the PLL is locked to the input phase-angle $\hat{\theta}$. Figure.3.20 (b), shows the two orthogonal signals generated by the SOGI-OSG. As expected, the transient response is extended until the grid frequency is newly tuned. Figure. 3.20 (c) shows the output variables of the Park transform. The v_d signal is equal to the amplitude of the input voltage v and the v_q signal is equaled to zero in the steady state by the action of the PLL. In Figure.3.20 (d), the estimated frequency locked to the rated frequecy with zero steady-state error in about 45 ms, i.e., less than 2.5 cycles of the fundamental frequency. In addition, and as shown in Figures.3.20 (e), and (f), a deviation

in the supply frequency will cause the phase angle error θ_e to increase. The PI-controller naturally works to bring this error back to zero. The phase-error peak is about 10º when the frequency step is 5Hz and 22 º when the step increases to 10Hz.



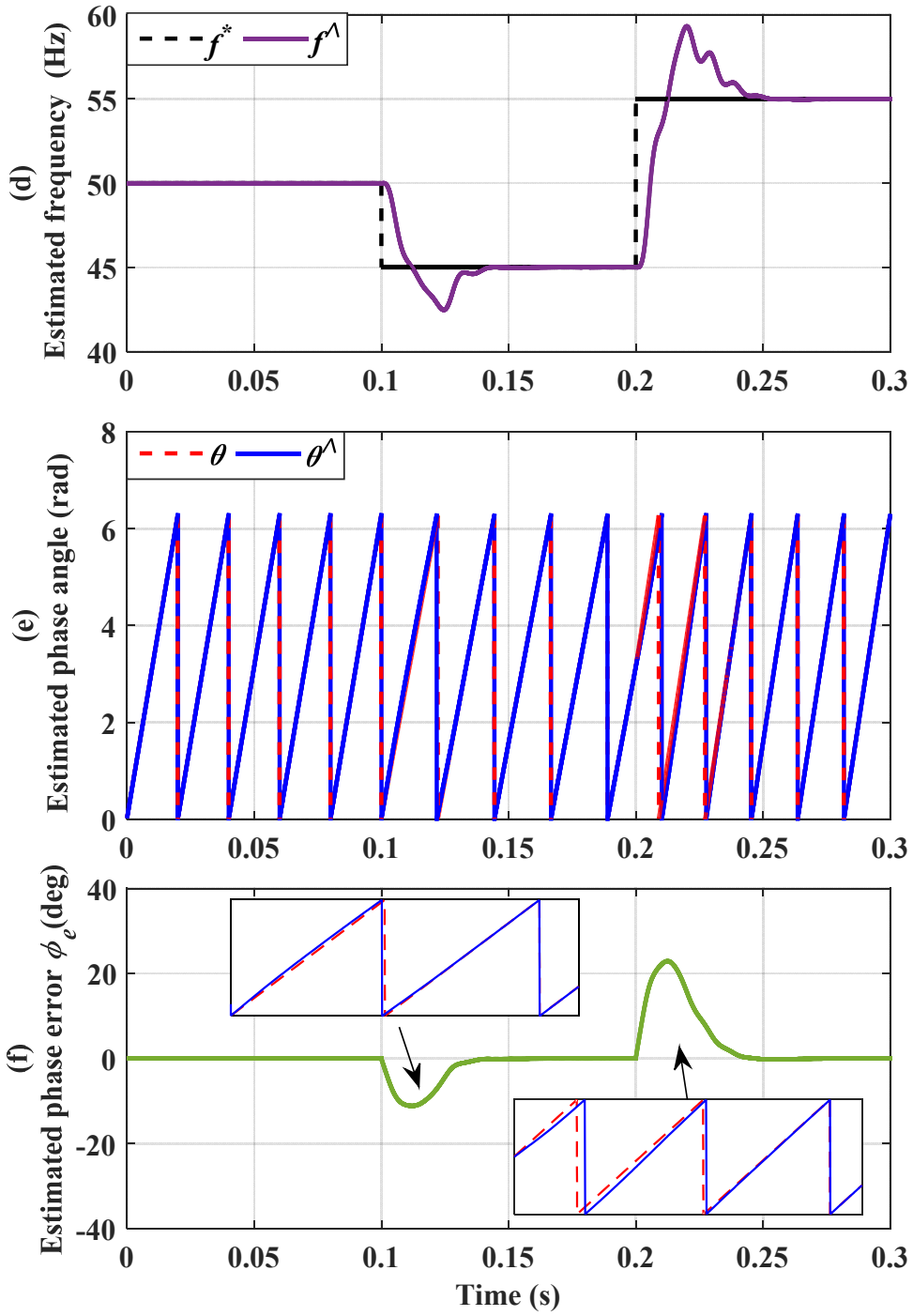
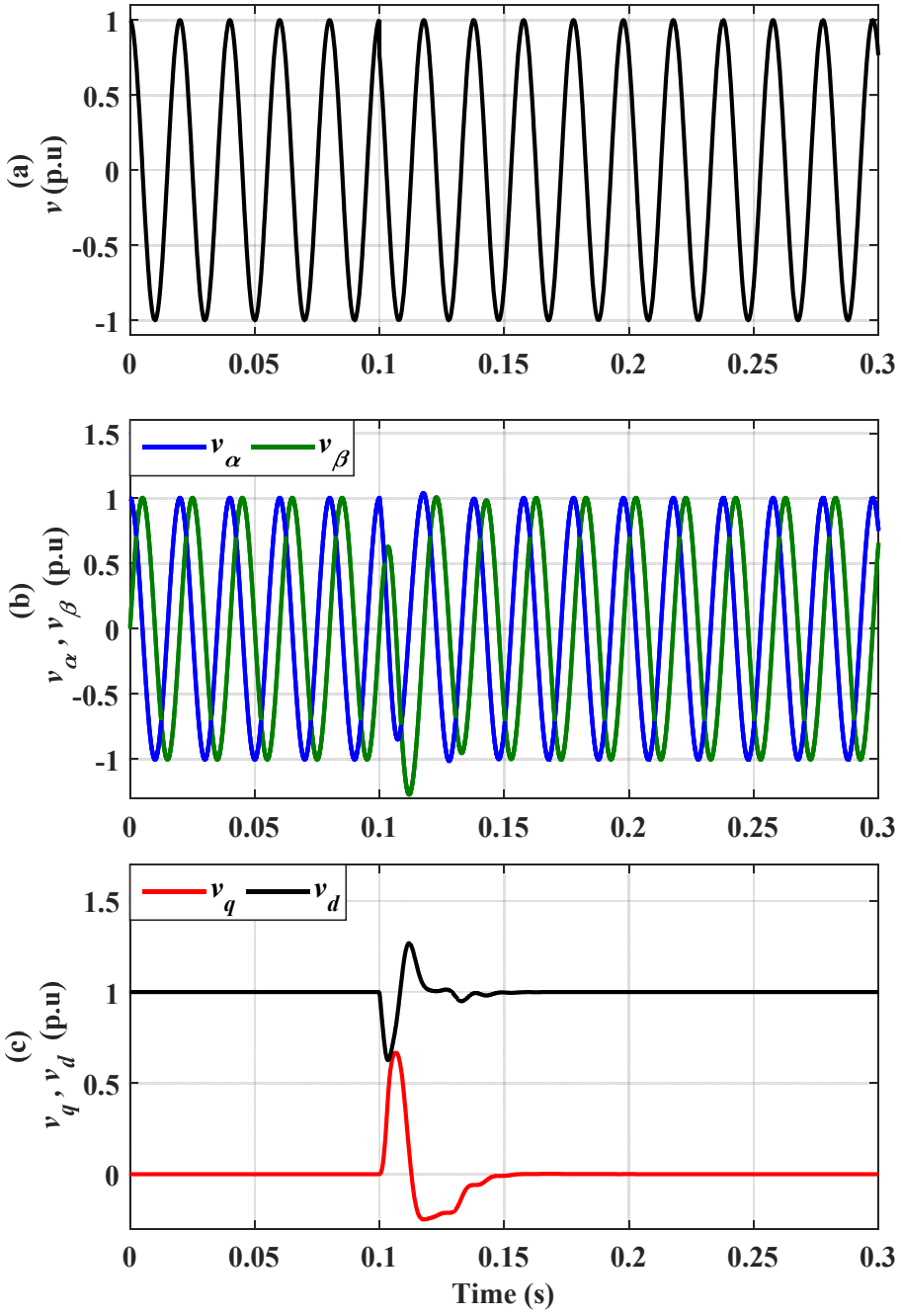


Figure 3.20. Response of the SOGI-PLL when the input voltage undergoes frequency step changes: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error.

3.5.2 Phase Jump

Figure. 3.21 depicts the simulation results, when a phase jump of 40° occurs in the input voltage v, at time =0.1s. It can be observed that the phase angle error decays to zero in about 45 ms (i.e., less than 2.5 cycles), and the overshoot is limited to 15°. It is worth mentioning here that, due to the PLL being an underdamped system (i.e. $\xi = 0.7$), and as expected, the frequency-step and phase-jump tranisent times are almost equivalent.



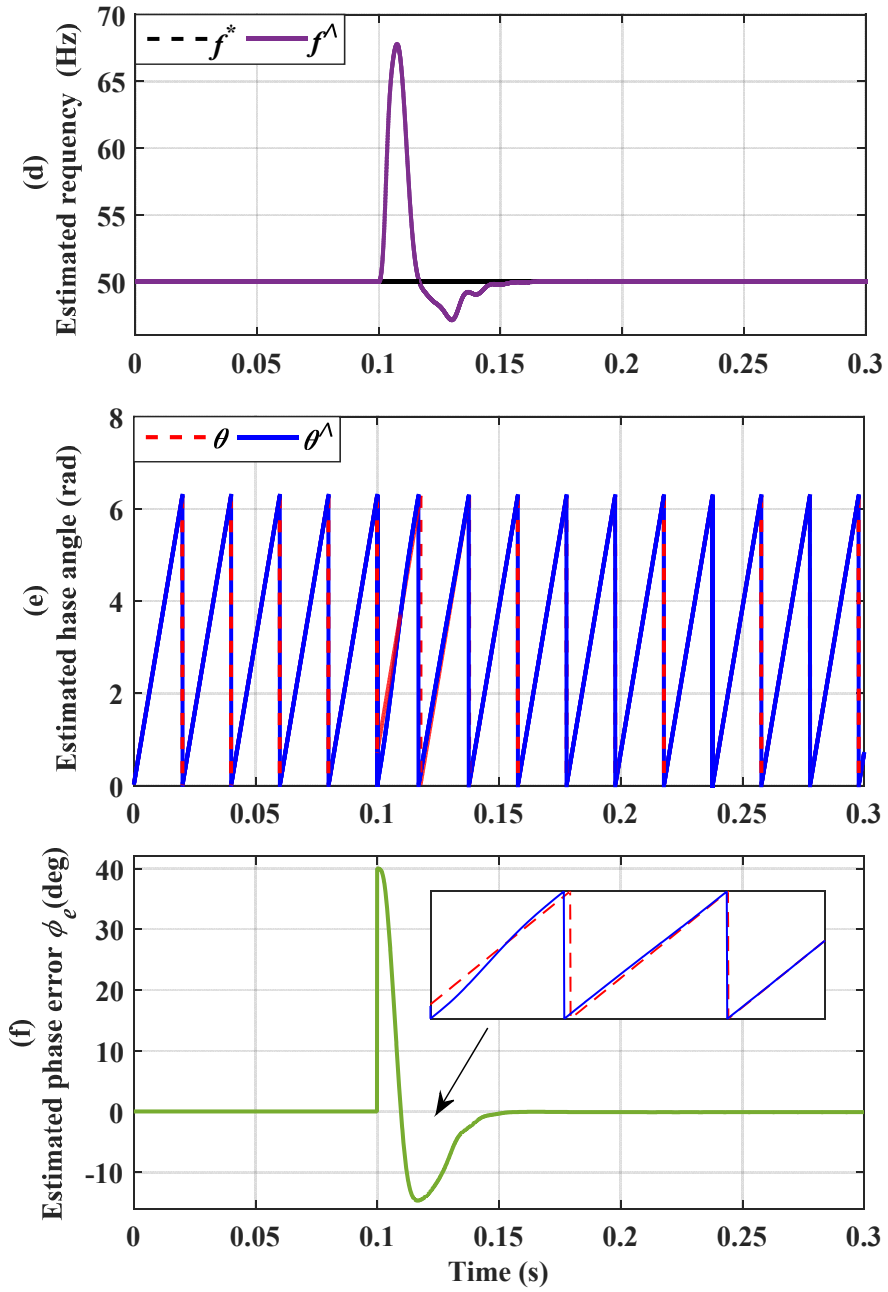


Figure 3.21. Response of the SOGI-PLL when the input voltage undergoes a phase jump of 40°: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error.

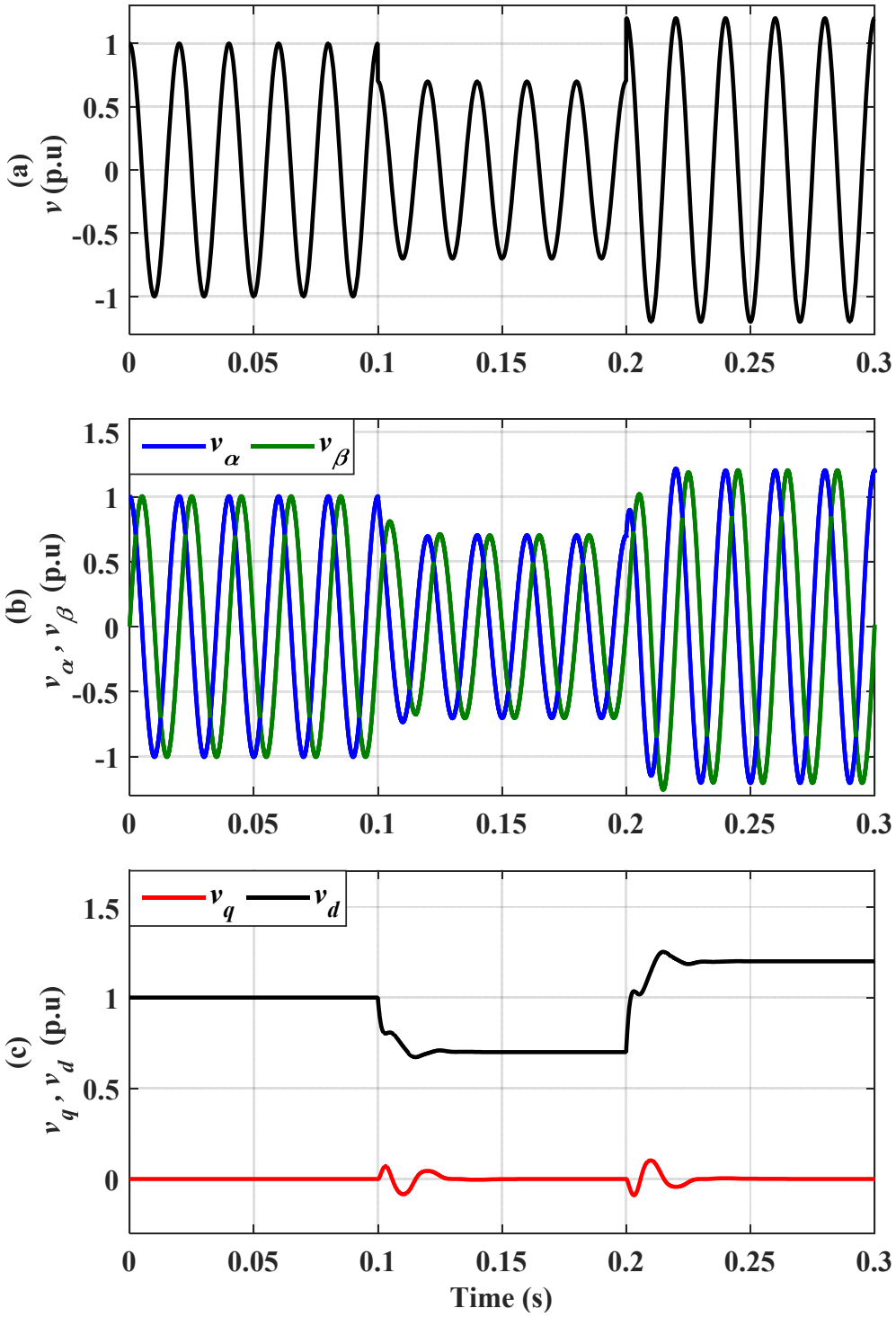
Because the frequency and phase angle are estimated within a single loop as shown in both Figure.3.1 and Figure.3.8, a large frequency transient is experienced during phase jumps. The propagation of the large frequency transient makes the produced signals v_α and v_β oscillatory, which is reflected back on the SRF-PLL stage. To avoid this issue, the PI controller with smaller *kp* and *ki* is often designed at the expense of slower dynamic response in SOGI-PLL [63].

3.5.3 Voltage Sag and Swell

Voltage sags and swells are the most severe condtions that may cause deterioration to the power quality in the utility grid [111]. Voltage sags are momentary in nature, and are produced mainly by the starting of large induction motors, line-to-ground faults, and sudden load changes or heavy loads. Whereas, the voltage swell is the opposite of the voltage sag, which is also transitory and occurs when an excessive load turns off in the power systems [111, 112]. During these disturbances, the amplitude compensation block of Figure 3.7, takes a fast action by quickly estimating the input voltage amplitude V_m, making the proposed design of the SOGI-PLL insensitive to the grid voltage amplitude variations during the steady-state condition.
To find the tranisent response of the proposed design, Figure. 3.22 shows the SOGI-PLL response, when the amplitude of the input voltage v, undergoes a voltage sag of 30%, at time = 0.1s, and a voltage swell of 20% at time = 0.2s. It is evident that with almost no overshoot, the amplitude attains the new steady-state value of 0.7 p.u within approximately one fundamental period. In the estimation of frequency, there is a deviation of 4 Hz for a period of 35 ms. The phase error settling time is lees than two cycles. During the transient, the peak-to-peak value of the phase error is limited to 4°. It is worth noting that, since the input frequency is kept constant in this test, the settling time for the detection of the input voltage amplitude is mainly determined by the SOGI-OSG dynamics as shown in Figure.3.22.(c).

3.5.4 Harmonic Distortion

Figure. 3.23 illustrates the response of the PLL system when a 15% third harmonic component is injected into the input voltage v, after 0.1s. It is evident in Figure.3.23(c), that the third harmonic distortion creates two different frequency components of 2ω and 4ω in the PD output signal, v_q. Besides, and because of the presence of harmonic distortion in the input voltage v, a noticable ripple of 3Hz in the estimated frequency and an oscillation of about 2° peak-to-peak phase estimation error in steady-state are obseved in Figures. 3.23 (d-f), respectively. It is worth mentioning that, this ripple and error can be further reduced by selecting a lower crossover frequency ω_c. This results in a higher attenuation at the disturbance frequencies, but at the cost of degrading the transient response of the PLL.


(a)
v (p.u)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
(b)
v_α , v_β (p.u)
v_α
v_β
1.5
1
0.5
0
-0.5
-1
(c)
v_q , v_d (p.u)
v_q
v_d
Time (s)

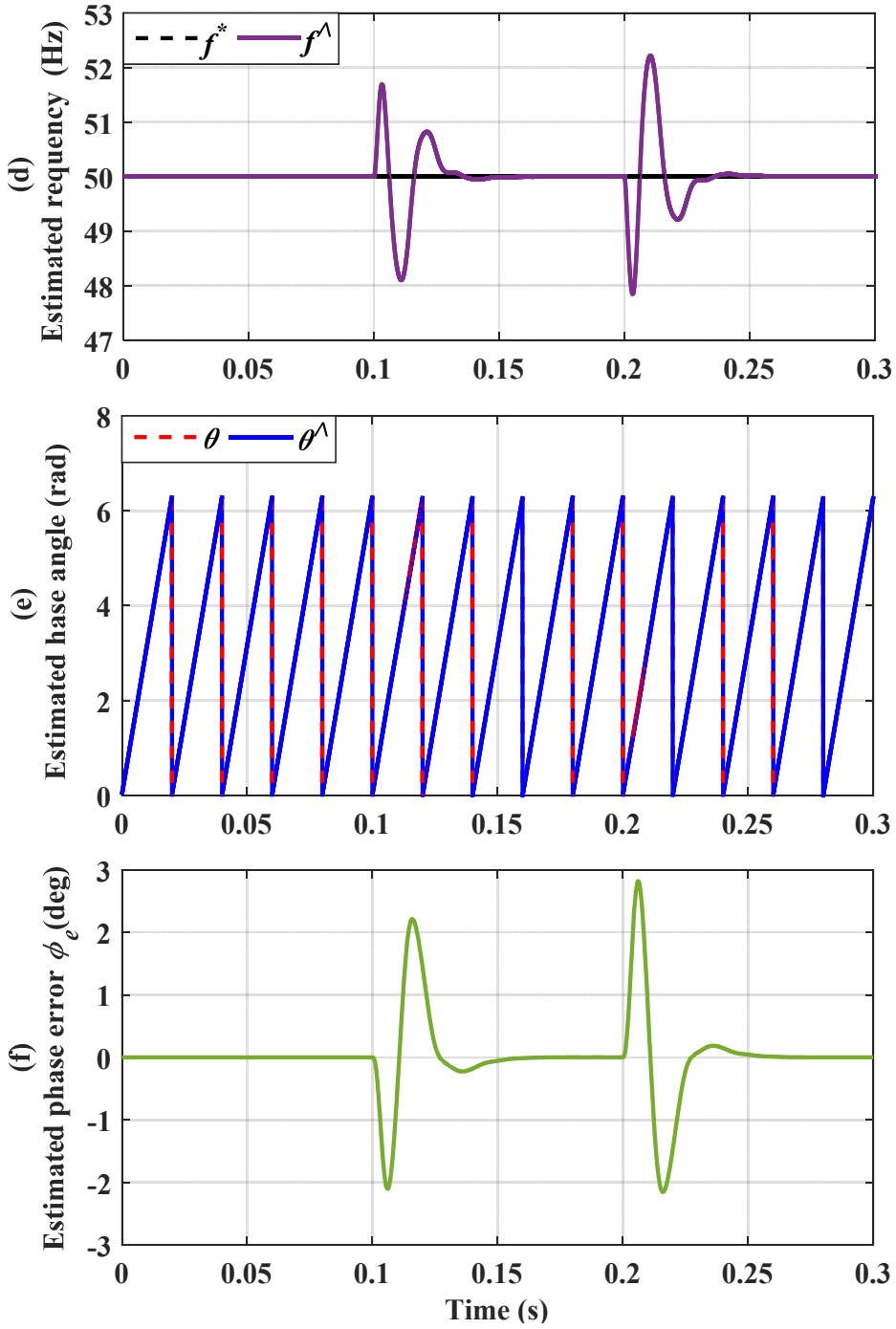
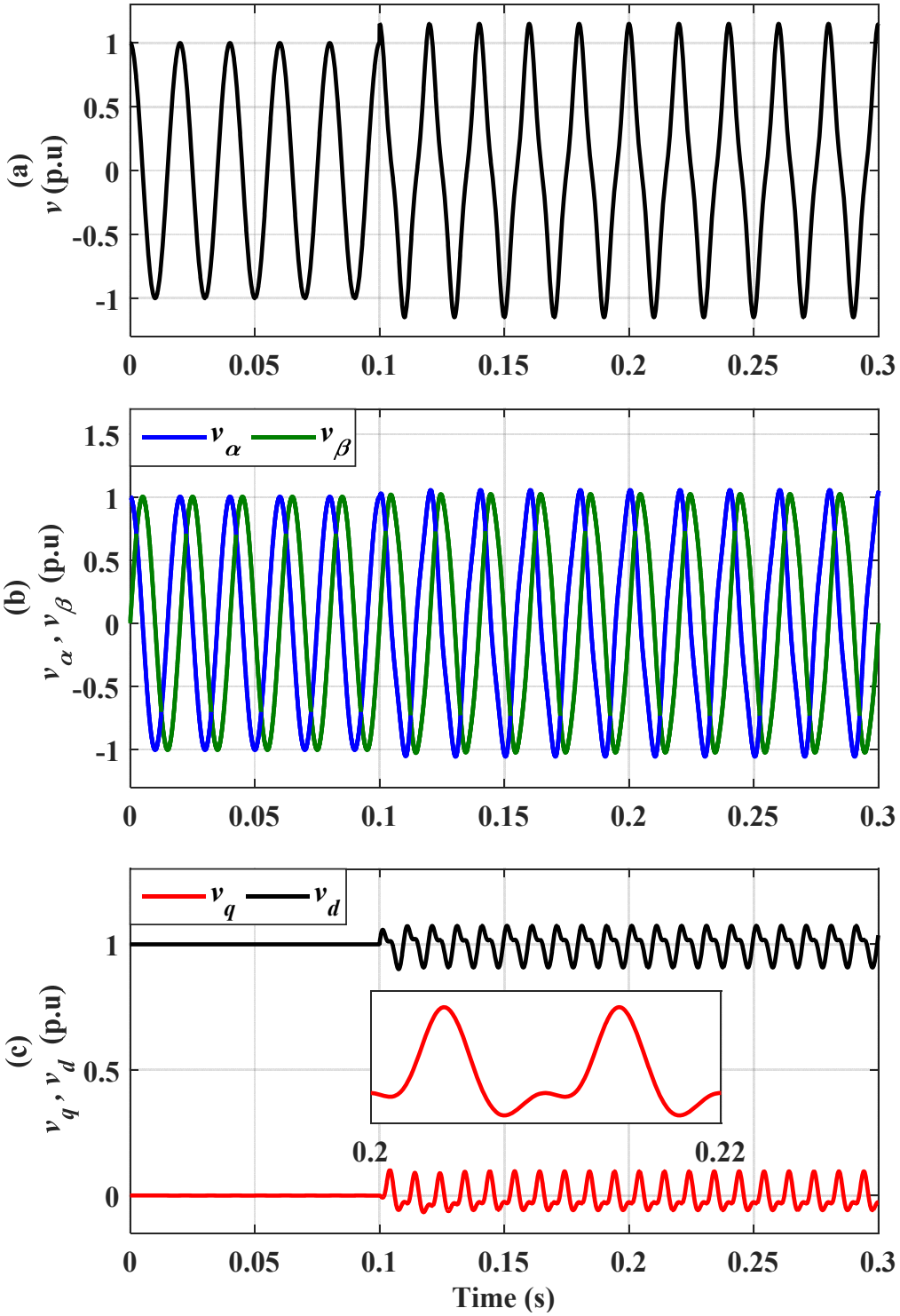


Figure 3.22. Response of the SOGI-PLL when the input voltage undergoes voltage sag of 30% and voltage swell of 50%: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error.


(a)
v (p.u)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
(b)
v_α , v_β (p.u)
v_α
v_β
1.5
1
0.5
0
-0.5
-1
(c)
v_q , v_d (p.u)
v_q
v_d
0.2
0.22
Time (s)

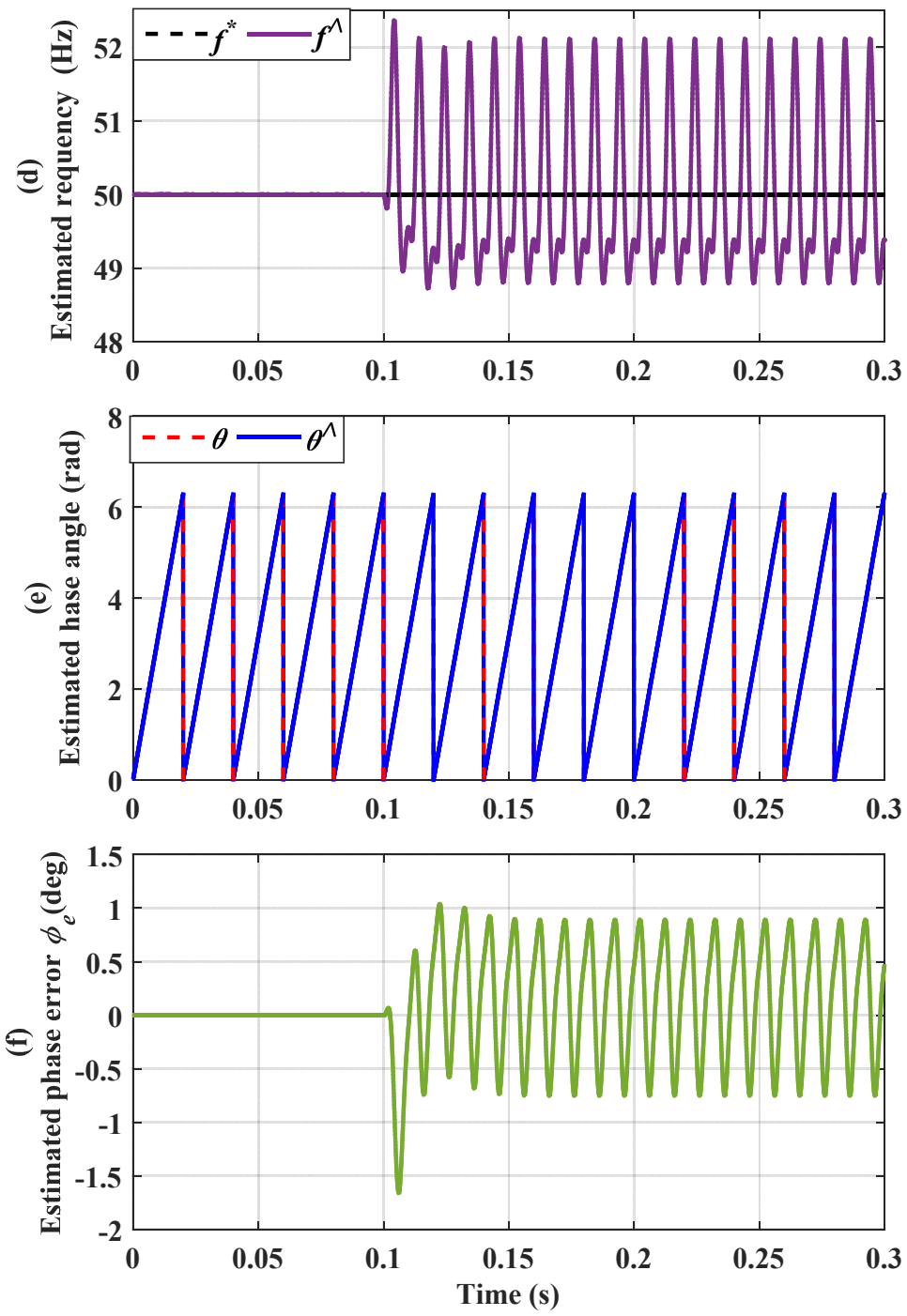


Figure 3.23. Response of the SOGI-PLL when the input voltage undergoes a 15% third-harmonic injection: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error.

3.5.5 DC offset

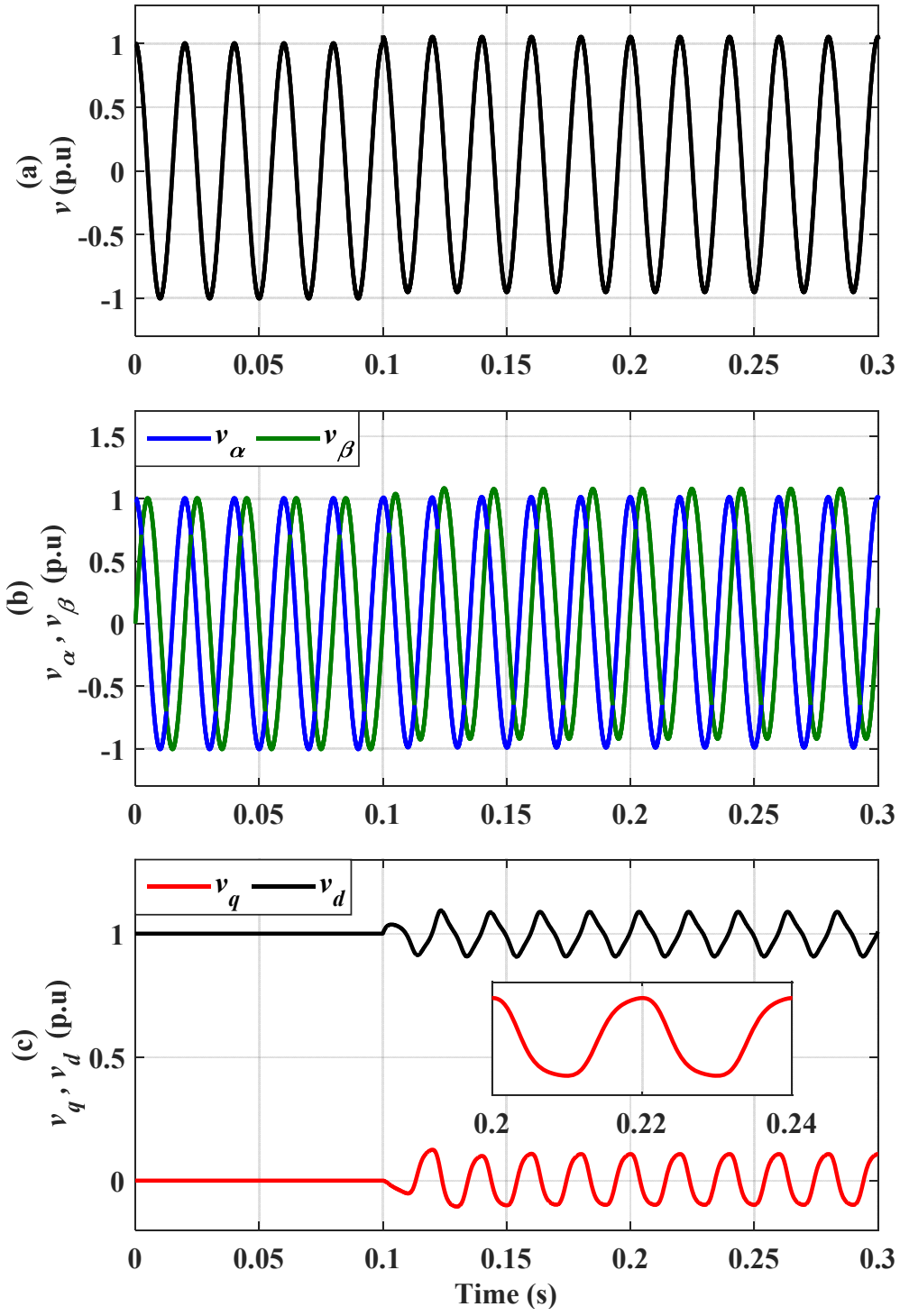
One critical concern that needs to be addressed here is the existence of a dc component in the measured input voltage *v*, which may be intrinsically present or may be generated due to grid faults, A/D conversion process, or saturation in current transformers [113, 114]. The presence of such a component in the PLL input causes undesirable periodic oscillatory errors in the estimated frequency, phase and amplitude [115-117].

Figure.3.24 shows the responses of the PLL when a sudden dc offset of 0.05 p.u occurs in the input voltage *v* after 0.1s. It is obvious from Figure.3.24 (b) that the orthogonal component v_β is directly affected by the presence of any voltage offset. This leads to fundamental frequency oscillations in the PLL estimated quantities that are difficult to filter, as shown in Figures.3.24 (c-f).

3.5.6 Sub-harmonics

One more important issue that needs to be considered is the presence of sub-harmonic voltage fluctuations. Sub-harmonics can be produced by nonlinear loads such as variable speed drives, rectifiers supplying repeated loads and wind generators that supply low frequency power due to wind speed deviations [118]. Typically the frequency of these subharmonics can be very low and create visual flicker in the range between 0.5Hz and 30Hz [119].

To evaluate this problem, Figure. 3.25 illustrates the performance of the SOGI-PLL in the presence of 10% subharmonic oscillations at a very low frequency (1 Hz). As seen in Figure.3.25 (b), oscillations caused by the presence of subharmonics in the input voltage *v* have a direct impact on the orthogonal component v_β due to the flat response of G_β for frequencies below the fundamental frequency as shown earlier in Figure.3.2 (b). As a consequence, the sub-harmonic distortion in the PD output produces ripple in the estimated quantities as shown Figures.3.25 (c-f).


(a)
v (p.u)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
(b)
v_α , v_β (p.u)
v_α
v_β
1.5
1
0.5
0
-0.5
-1
(c)
v_q , v_d (p.u)
v_q
v_d
0.2
0.22
0.24
Time (s)

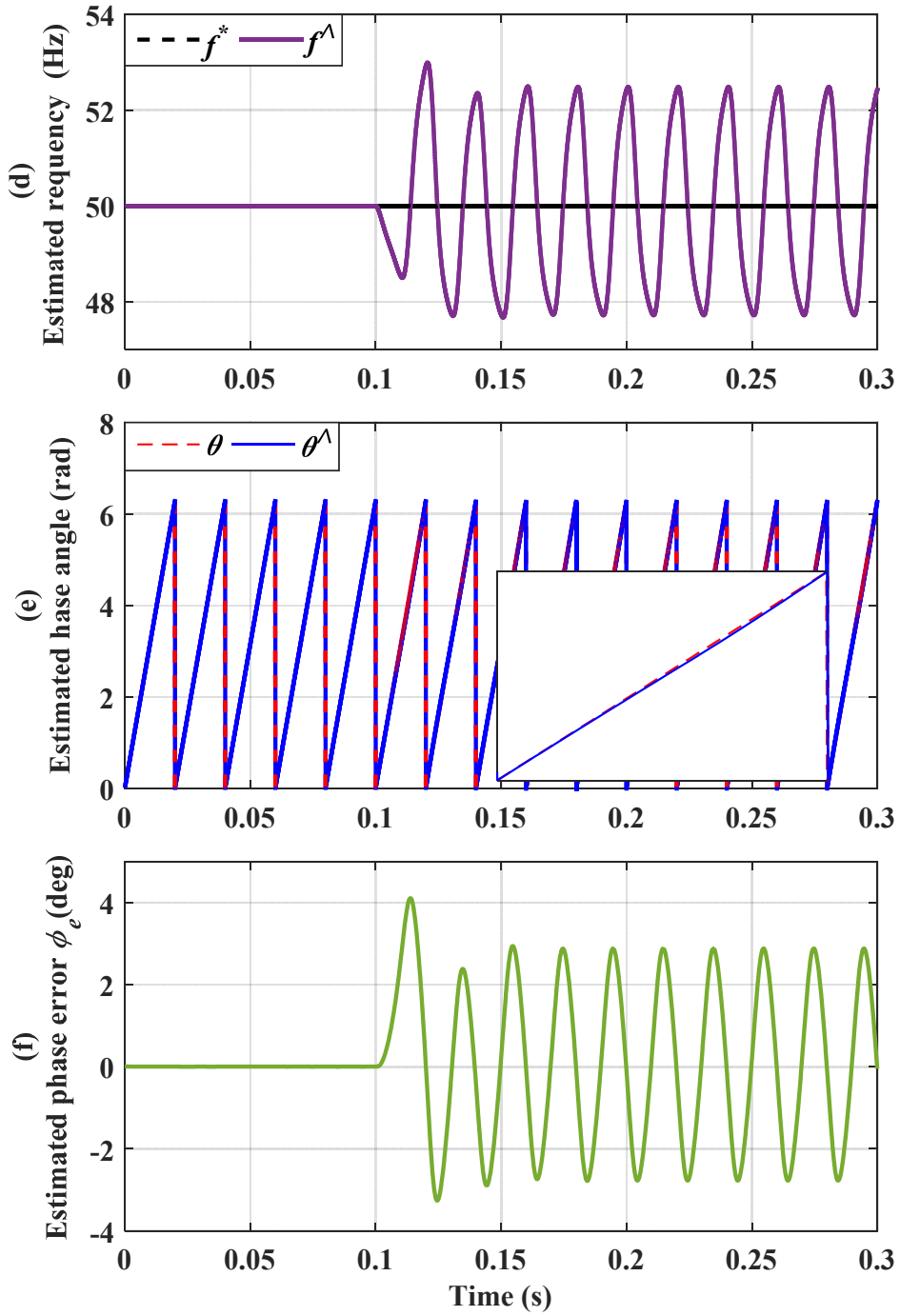
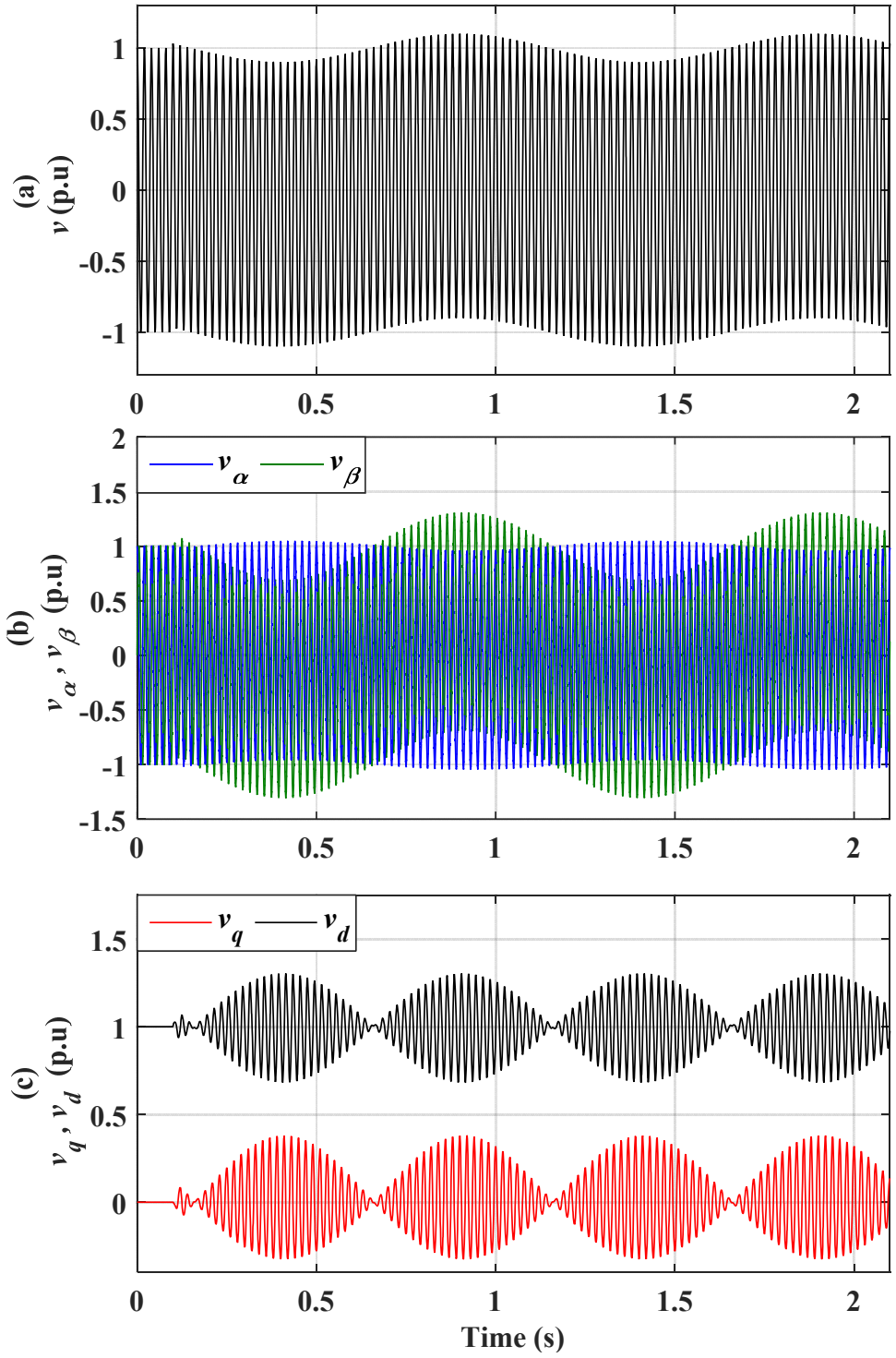


Figure 3.24. Response of the SOGI-PLL when the input voltage undergoes a 5% dc offset: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error


(a)
v (p.u)
1
0.5
0
-0.5
-1
0
0.5
1
1.5
2
(b)
v_α , v_β (p.u)
v_α
v_β
2
1.5
1
0.5
0
-0.5
-1
-1.5
(c)
v_q , v_d (p.u)
v_q
v_d
Time (s)

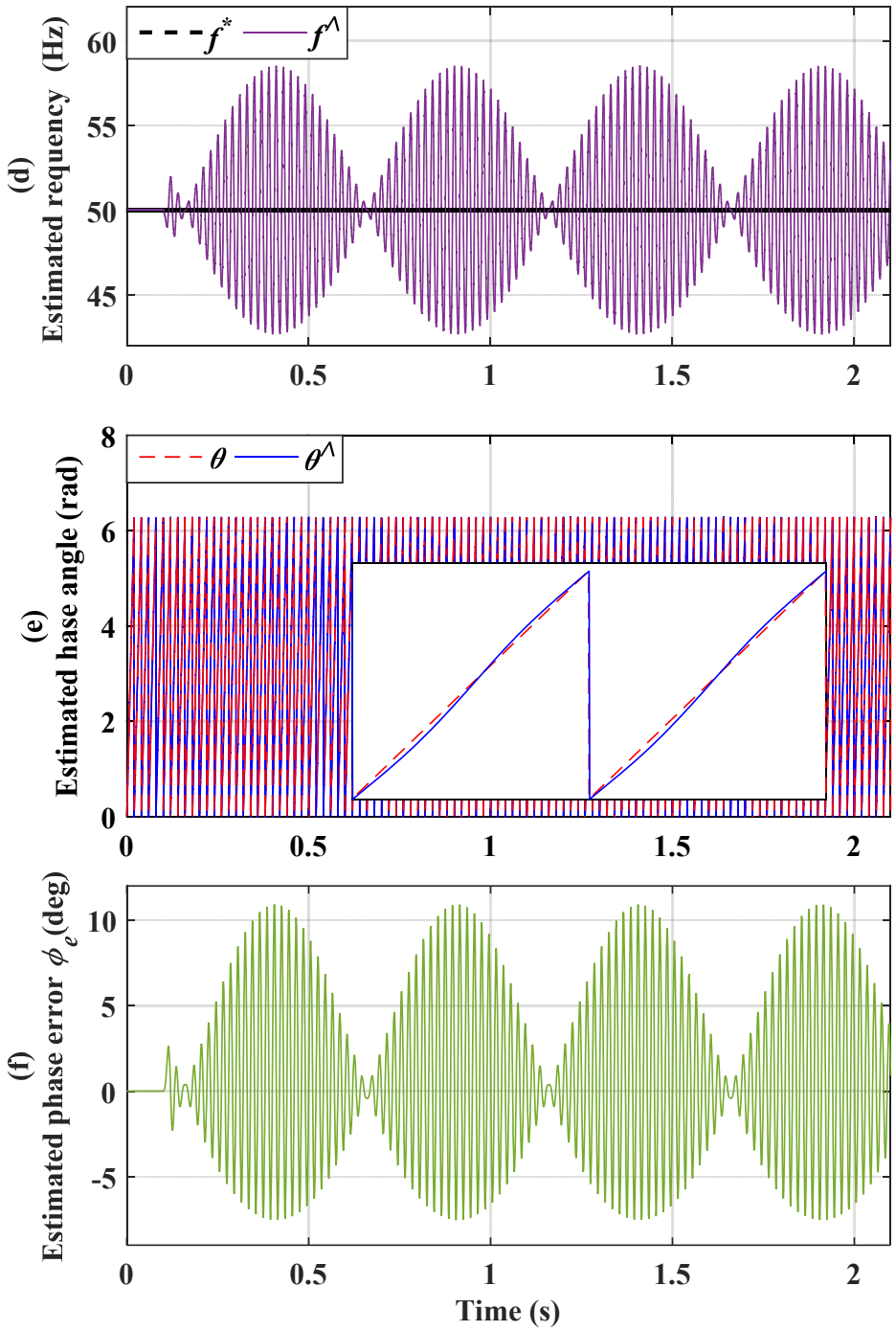


Figure 3.25. Response of the SOGI-PLL when the input voltage undergoes a 10% of 1Hz subharmonic: (a) Input voltage, (b) orthogonal signals generated by the SOGI-OSG, (c) signals in the synchronous reference frame, (d) estimated frequency, (e) estimated phase-angle and (f) estimated phase-angle error

3.6 Summary

An advanced and effective single-phase PLL structure, known as SOGI-PLL has been thoroughly analysed in this chapter. Through a comprehensive mathematical analysis, a linearized model for the SOGI-PLL has been developed. Then, a systematic design procedure to fine-tune the PLL parameters has been proposed. The proposed design selects the PLL parameters such that a desired attenuation of -20dB at the lowest disturbance frequency (here, 100Hz), and a fast dynamic response are achieved. To verify the effectiveness of proposed design method, extensive simulation studies have been provided considering various utility grid disturbances. The simulation results confirm that, the desired settling time and attenuation were both achieved when the PLL damping factor and crossover frequency were selected to be 0.7 and 21.62Hz respectively. In addition, these results show that, a higher attenuation at the disturbance frequencies can be attained by selecting a lower crossover frequency, but at the cost of degrading the transient response of the PLL. However, the results reveal the high sensitivity of the SOGI quadrature-phase output to input dc offset voltage and subharmonics. Such components produce errors in the estimated quantities by the PLL, which can result in dc current injection to the grid which is highly undesirable. To overcome this drawback associated with the SOGI-PLL, the next chapter addresses in details these issues with effective solutions.

CHAPTER 4

DC Component Rejection in SOGI-PLL Algorithm

4.1 Introduction

It has been pointed out in the previous chapter, that one important issue must be addressed is the presence of dc offset in the input signal of PLLs. The presence of such a component causes undesirable fundamental-frequency oscillations in their estimated quantities (i.e., utility voltage amplitude, phase and frequency). Consequently, the performance of the power conversion system may be degraded. The elimination of such oscillatory errors is a challenging problem because of their low frequency. Thus, this chapter aims to provide a comprehensive analysis of the effect of the dc offset based on the PLL in the synchronous reference frame (SRF). Two different existing offset rejection approaches based on the SOGI-OSG algorithm are discussed in detail. Design aspects of these methods are presented, and their advantages and disadvantages are evaluated. A novel method to tackle this issue is proposed in this chapter. This completely rejects the error caused by the dc component and demonstrates superior harmonic disturbance attenuation performance when compared with the other two alternative methods. The effectiveness of this approach is verified through digital computer simulation and will be validated by experimental results presented in the forthcoming chapters.

4.2 Overview of DC Component in PLL

The single-phase grid-connected converter (SPGC) is a key-enabling technology for renewable energy systems such as photovoltaic, fuel cells, and batteries, especially in residential applications [6, 120]. A precise and fast detection of phase angle, frequency and amplitude of the grid voltage is an essential requirement for effective operation and control of the grid-connected converters [21].

In three-phase systems, due to its simplicity and effectiveness, the synchronous reference frame phase-locked loop (SRF-PLL) is the most widely used technique for extracting these grid parameters [121]. In single-phase systems, however, designing SRF-PLLs is more complicated than in three-phase PLLs, due to the lack of multiple independent input signals [122]. To deal with the aforementioned problem, it is of paramount importance to develop proper techniques that are able to create a second signal in-quadrature with the fundamental single-phase signal, such that the original and the synthesized components together form the stationary reference frame. These PLLs are often called the orthogonal signal generation-based PLLs (OSG-PLLs) [78, 123].

Typically, these (OSG-PLLs) topologies differ from each other just in the technique they use for creating the fictitious orthogonal voltage signal. In the technical literature, there are a number of techniques for generating the orthogonal voltage system for a single-phase system. Some of the available methods make use of the transport delay block, Hilbert transformation and first-order differentiating method as presented in [86, 88, 100]. Nevertheless, these methods have one or more of the following shortcomings: frequency dependency, high complexity, nonlinearity, poor or no harmonic filtering capability [89]. In recent years, the second-order generalized integrator (SOGI) has been extensively used as a building block for orthogonal signal generation (OSG), owing to its simple structure, relatively fast transient response, high filtering capability without delays and desired frequency adaptive performance [89, 105].

Despite the wide use of the SOGI-OSG in several applications, such as frequency estimation (i.e., SOGI-FLL) [124], harmonic extraction (i.e., MSOGI-OSG) [20], and grid synchronization (i.e., SOGI-PLL) [89, 105], the SOGI-OSG is highly sensitive to the presence of dc and/or subharmonic components in its input signal. Such components produces errors on the quadrature signal [113, 114], which can cause failures of the systems implemented with the SOGI-OSG [117, 125].

This dc component can be generated by grid faults, measurement devices (i.e., due to saturation in a current transformer), A/D conversion process in fixed and floating-point digital signal processors, or dc injection by grid-connected power converters [117, 125-127]. The occurrence of this component in the input of the PLL produces fundamental frequency ripple in the estimated quantities by the PLL (i.e., phase-angle, frequency, and amplitude). In addition to these low frequency oscillatory errors, the PLL unit vector (sine and cosine of the phase-angle estimated by the PLL) which is usually used for creating reference current in the grid-connected converters, will inevitably contain some offset error, resulting in dc current injection to the grid which is highly undesirable [113, 114, 117, 126, 128]. The international standards, however, have defined stringent limits on the maximum allowable dc current injection of the grid-connected converters. For example, the standard IEC61727 [13] limits the dc current injection by the grid-connected photovoltaic inverters to less than 1% of their rated output current, while the standard IEEE 1547-2003 [12] states that the dc injection by the distributed resources should not exceed 0.5% of their rated output current. These strict limits confirm the importance of the dc offset rejection capability for PLLs in the grid-connected applications. Therefore, special attention should be paid when designing PLLs with the presence of the dc offset in their input.

To remedy this drawback of PLL algorithms, several methods have been proposed in the literature. In [127, 129], employing a band-pass filter (BPF) before the PLL input is suggested. The BPF successfully blocks the dc offset, but at the cost of degrading the PLL transient response and also causing phase and magnitude errors in the PLL input when the grid frequency deviates from its nominal value. The influence of these errors can be avoided by utilizing a frequency adaptive BPF as proposed in [125], which indeed adds some complexity and computation requirements for the digital controller used. In [115], a method of dc offset compensation in the single-phase SRF-PLLs is proposed. In this technique, the dc offset error can be readily estimated by separately integrating the input signal of the PLL loop-filter over two half-cycles according to the estimated phase-angle. Then, the integrated results are subtracted from each other and passed across a simple proportional-integral (PI) controller. By subtracting the output of the PI controller, which is an estimation of the input dc component from the PLL input signal, the resultant signal will be free of any dc component. A detailed study of five other techniques to deal with the problem of a dc component in the input signal can be found in [117]. Concentrating on the SOGI-OSG, an approach based on adding SOGI-OSGs as pre-filters is proposed in [125]. Although this method exhibits satisfactory

performance at both low-and high- frequency, it may be suboptimal since its parameters are assumed equal for simplicity. An alternative dc offset rejection method based on using a low-pass filter is proposed in [113]. Another modified SOGI-OSG method is reported in [114], in which an integrator is added to the SOGI-OSG structure to deal with the problem of dc offset.

A simple yet effective approach to overcome the drawback of the dc offset in single-phase PLLs based SOGI is proposed in this chapter. The key feature of this method is that, the orthogonal signal will be generated using a two-stage cascaded low-pass filter (CLPF). The input of the CLPF is taken directly from the in-phase signal v_α generated by the conventional SOGI-OSG taking advantage of it being free of any dc offset. This will ensure that the generated orthogonal signal v_β is not affected by any dc offset appearing in the input signal v. The resultant PLL structure is called (CLPF-SOGI-PLL). The PLL with the proposed algorithm which is characteristically suitable for digital implementation of single-phase grid-connected converters controller, has resulted in good steady-state and dynamic performance when compared with other methods reported in [113] and [114].

4.3 Effects of a DC Component in Grid Voltage Measurements

A. System Description

Figure.4.1 describes the general structure of the SPGC including power circuit and control algorithm, which is later, used to test the proposed method.

Figure.4.2 shows the block diagram of a conventional single-phase OSG-PLL, in which v, is the input voltage, $\hat{\omega}$, $\hat{\theta}$ are the estimated frequency and angle respectively, and ω_{ff} is the feed-forward nominal frequency. As illustrated in Figure. 4.1 and 4.2, the PLL is employed to synchronize the output current of the SPGC (i.e.,i) with the grid voltage (i.e., v), so that effective control and operation can be attained. In this thesis so far, the orthogonal signal generator required by the single-phase PLL is built using a second-order generalized integrator (SOGI) as discussed in Chapter 3.

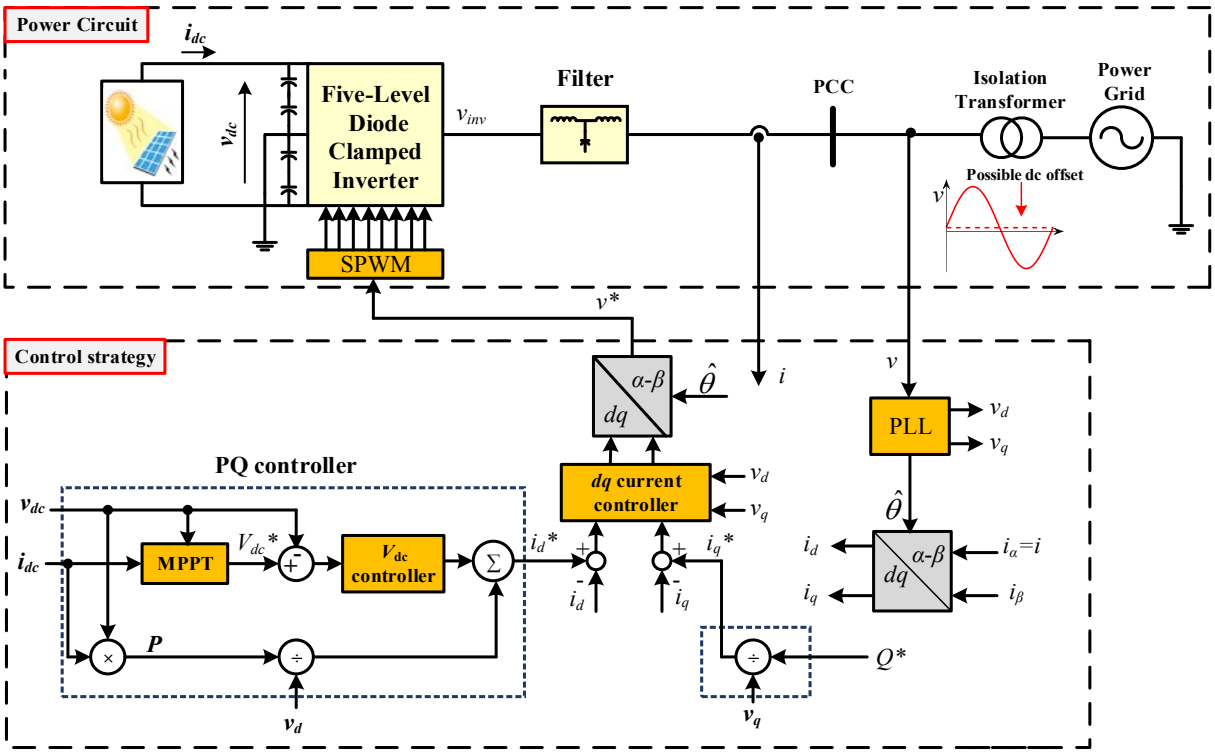


Figure 4.1. System configuration of SPGCs

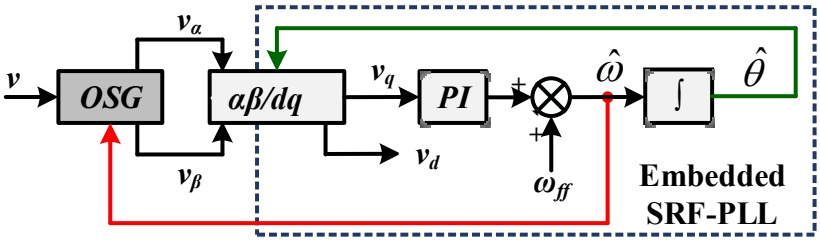


Figure 4.2. Block diagram of single-phase OSG-PLL

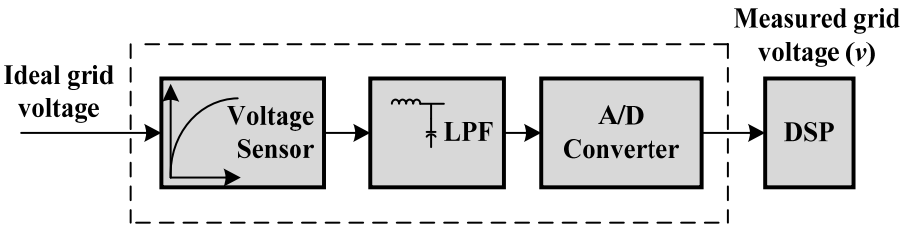


Figure 4.3. Grid voltage measurement circuit

B. Effect of DC Offset Error

In this section, the effect of the dc offset is mathematically analysed based on the SOGI-OSG-PLL shown in Figure. 4.2.

Ideally, the grid voltage without any dc offset can be defined as

$$\boldsymbol{v = V_m \cos \theta} \tag{4.1}$$

where: V_m and θ are the input voltage amplitude and phase-angle, respectively.

The measured grid voltage typically digitalized through an interface circuit which performs voltage sensing, filtering using low-pass filter, and A/D conversion as represented in Figure. 4.3. The non-linear characteristics of voltage sensors, A/D conversion process, and the thermal drift of analogue components (i.e., LPF), may cause a dc offset in the measured grid voltage, even if the grid interface circuit is well designed [115]. Consequently, the measured grid voltage including the dc offset error can be expressed as

$$\boldsymbol{v = V_m \cos(\theta) + \Delta_{dc}} \tag{4.2}$$

where: Δ_{dc} is the amplitude of the dc offset error.

Taking into account Δ_{dc}, the orthogonal signals which will be generated by the SOGI-OSG can then be written as

$$\begin{cases} \boldsymbol{v_\alpha = V_m \cos(\theta)} \\ \boldsymbol{v_\beta = V_m \sin(\theta) + \Delta_{dc}} \end{cases} \tag{4.3}$$

Notice that v_α will possess no dc offset as the v_β does and that is due to SOGI characteristics as it will be emphasised in the next section.

Now, applying Park's transformation matrix to (4.3) yields v_d and v_q signals as expressed in (4.4)

$$\begin{aligned} \begin{bmatrix} \boldsymbol{v_d} \\ \boldsymbol{v_q} \end{bmatrix} &= \begin{bmatrix} \boldsymbol{\cos(\hat{\theta})} & \boldsymbol{\sin(\hat{\theta})} \\ \boldsymbol{-\sin(\hat{\theta})} & \boldsymbol{\cos(\hat{\theta})} \end{bmatrix} \begin{bmatrix} \boldsymbol{v_\alpha} \\ \boldsymbol{v_\beta} \end{bmatrix} \\ &= \begin{bmatrix} \boldsymbol{\cos(\hat{\theta})} & \boldsymbol{\sin(\hat{\theta})} \\ \boldsymbol{-\sin(\hat{\theta})} & \boldsymbol{\cos(\hat{\theta})} \end{bmatrix} \begin{bmatrix} \boldsymbol{V_m \cos(\theta)} \\ \boldsymbol{V_m \sin(\theta) + \Delta_{dc}} \end{bmatrix} \end{aligned} \tag{4.4}$$

where $\hat{\theta}$ is the estimated grid angle and θ is the real grid angle.

After some mathematical manipulations, the synchronous *dq*-axis voltages including the dc offset error can be rewritten as

$$\begin{cases} \boldsymbol{v_d = V_m\, cos\left(\theta - \widehat{\theta}\right) + \Delta_{dc}\, \sin \widehat{\theta}} \\ \boldsymbol{v_q = V_m\, sin\left(\theta - \widehat{\theta}\right) + \Delta_{dc}\, \cos \widehat{\theta}} \end{cases} \tag{4.5}$$

Under frequency-locked condition (i.e.,$\omega \approx \widehat{\omega}$), and when the phase error is very small, (i.e.,$\theta = \hat{\theta} \rightarrow \theta_e \approx 0,$), (4.5) can be approximated as

$$\begin{cases} \boldsymbol{v_d = V_m + \Delta_{dc} sin\left(\widehat{\theta}\right)} \\ \boldsymbol{v_q = \Delta_{dc}\, cos\left(\widehat{\theta}\right)} \end{cases} \tag{4.6}$$

It is evident from (4.6) that due to the dc offset error, the synchronous *dq*-axis voltages have the same frequency components compared with the grid frequency. Furthermore, the oscillatory errors in the *dq*-axis voltages are mainly determined by sine and cosine terms with the estimated grid frequency and the dc offset error. Especially, the oscillatory error in the input signal of the PLL loop-filter (i.e., v_q) causes distortion in the frequency and phase-angle estimated by the PLL. Moreover, the ripple components in the v_d voltage cause the estimated grid voltage amplitude to be distorted. It is worth mentioning here that, the estimated grid voltage amplitude only relates to the feed-forward term at the output of the current controller and has no effect on the PLL performance [130]. Therefore, the dc offset error must be rejected so that the ripple components of the synchronous *dq*-axis voltages are suppressed and the distortion of the estimated grid angle, frequency and voltage amplitude is cleared.

4.4 Proposed DC Offset Rejection Technique

Based on the mathematical analysis conducted in section 4.3, it has been proved that, in the presence of such a component in the input signal, the loop filter suffers from a disturbance in its input at the fundamental frequency. Mitigating such a low-frequency error by further reducing the bandwidth of the embedded SRF-PLL is undesirable since it degrades the system dynamic response [67]. Consequently, this dc offset and other subharmonic components must be removed in a stage prior to the loop filter by modifying the SOGI structure in a way that the orthogonal signal does not contain any dc offset.

4.4.1 Review of Conventional SOGI- OSG

Figure.4.4 depicts the basic structure of the conventional SOGI-OSG which has been comprehensively discussed in Chapter 3. Its characteristics transfer functions are given in (4.7), while its frequency response is illustrated in Figure.4.5

$$\begin{cases} G_\alpha(s) = \dfrac{v_\alpha}{v}(s) = \dfrac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + (\hat{\omega})^2} \\ G_\beta(s) = \dfrac{v_\beta}{v}(s) = \dfrac{k(\hat{\omega})^2}{s^2 + k\hat{\omega}s + (\hat{\omega})^2} \end{cases} \tag{4.7}$$

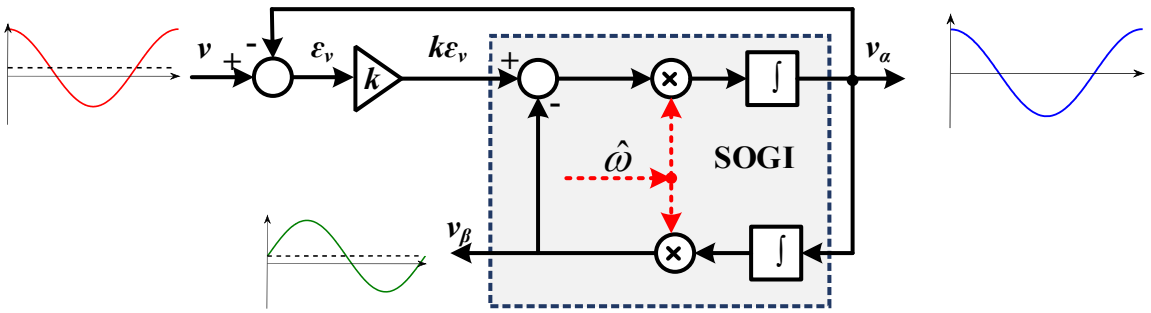


Figure 4.4. Basic structure of Conventional SOGI-OSG

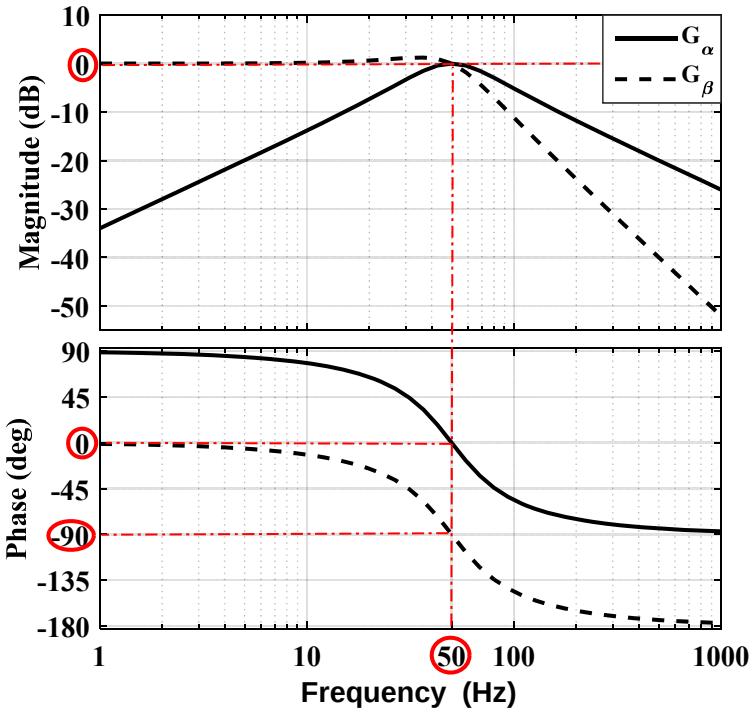


Figure 4.5. Bode-plots of $G_\alpha(s)$ and $G_\beta(s)$for k=1 and when $\hat{\omega}$ = 2π.50 rad/s.

From Figure.4.5, it is clear that the output v_α is a band-pass filtered version of the input v with a unity gain and no phase shift at a frequency of $\widehat{\omega}$. In contrast, the output v_β is a low-pass-filtered version of the input v with a unity gain and 90° phase shift at a frequency of $\widehat{\omega}$. It is very important to notice that, although the output v_β exhibits better filtering features for high frequencies as compared with v_α, it is directly affected by the presence of dc and other subharmonic components in the input signal, since it behaves as LPF. The magnitude of the offset in the orthogonal signal is *k* times that of the input dc component.

To evaluate this problem, Figure. 4.6(a) shows the SOGI-OSG responses when the input signal v undergoes a dc offset of 0.2 p.u at *t*= 0.05s, while Figure. 4.6(b) represents the SOGI-OSG response to subharmonic of 1Hz and 20% of v amplitude at *t*=0.05s.

As expected, the generated orthogonal signal v_β becomes biased when the input signal has a dc component as shown in Figure.4.6 (a). The magnitude of the dc offset in v_β is equal to 0.2p.u, since *k*=1. Likewise, the orthogonal signal v_β is directly affected by the presence of subharmonic components in the input signal as displayed in Figure.4.6 (b). Accordingly, and as it has been stressed earlier in (4.3) and (4.6), this undesired ripple generated in the orthogonal signal will be transferred to the loop-filter of the embedded SRF-PLL in the form of a low-frequency error affecting the accuracy of the estimated quantities by the PLL. In contrast to G_β, the transfer function G_α apparently offers better filtering features at low-frequencies, (i.e., subharmonics from zero to 50Hz) as apparent from Figure 4.5. As a result, the in-phase signal v_α will carry neither dc offset nor subharmonics as clearly shown in Figures.4.6 (a) and (b).

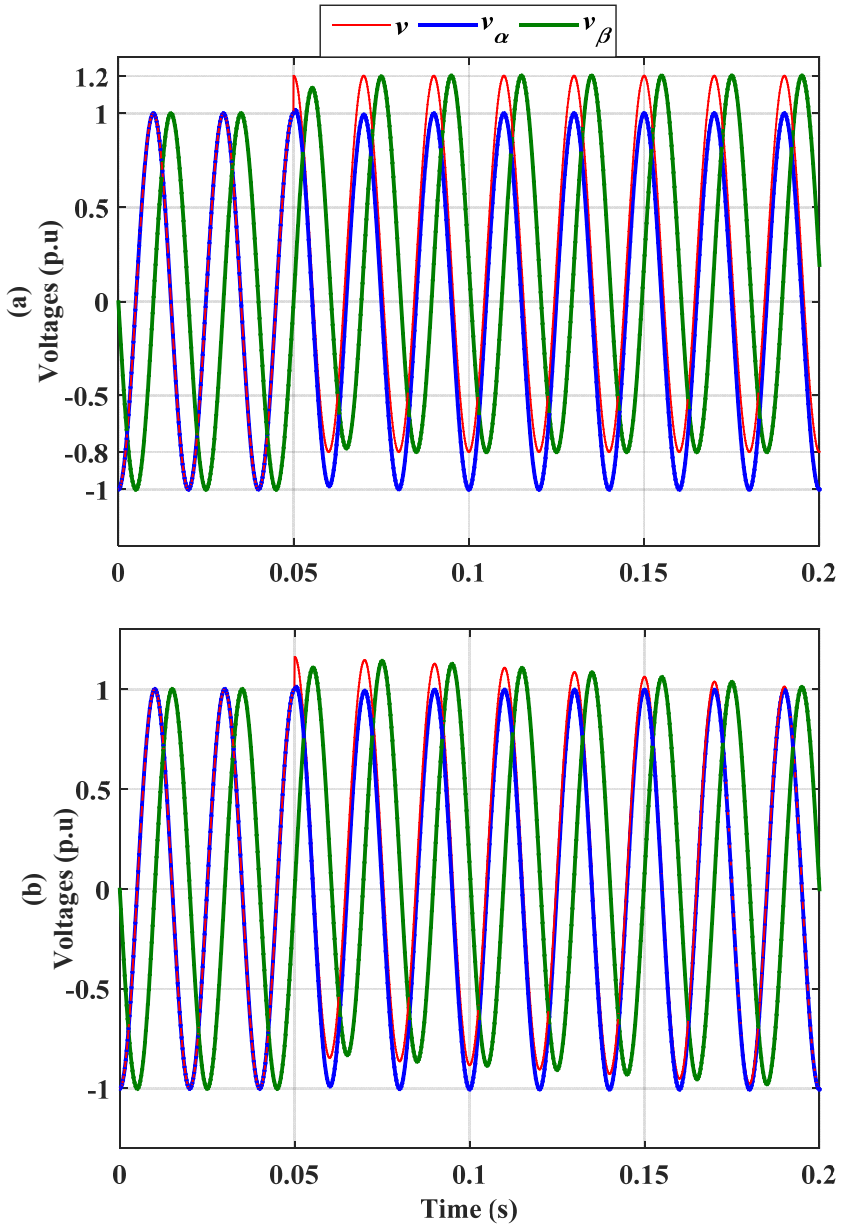


Figure 4.6. SOGI-OSG responses when the input signal *v* at time = 0.05s undergoes (a) a dc offset of 0.2 p.u. (b) a 1Hz subharmonic and 20% of V_m. (V_m=1p.u, *k*=1 and ω = 2π.50 rad/s)

Based on the fact that v_α is insensitive to input dc offset and other sub-harmonic components as it has been revealed in Figures 4.5 and 4.6, a proposed method for rejecting these components from the orthogonal signal will be introduced next.

4.4.2 Proposed CLPF-SOGI-OSG

The proposed solution to tackle the problem of dc offset and subharmonic components associated with the conventional SOGI-OSG is shown in Figure.4.7. The key point of this method is based on connecting a conventional SOGI-OSG in series with a simple two-stage cascaded low-pass filter (CLPF). The input signal v is fed into the conventional SOGI-OSG block, and its in-phase output signal v_α is used as an input signal of the CLPF. Since v_α is insensitive to any dc offset in the input signal v, the CLPF which behaves as an OSG will be able to generate an orthogonal signal $v_{\beta CLPF}$ free of any dc offset. Since both orthogonal signals (i.e., v_α and $v_{\beta CLPF}$) behave like a band -pass-filtered version of the input signal v. Consequently, neither v_α nor $v_{\beta CLPF}$ will possess any dc offset or sub-harmonic components, and since they are fed into the embedded SRF-PLL structure, thus the PLL operation no longer suffers from the presence of such component. For the sake of brevity, this technique is referred to as the CLPF-SOG-OSG.

It is worthwhile mentioning here, that since both SOGI-OSG and CLPF are adaptively tuned using the fundamental frequency provided by the embedded SRF-PLL (i.e., $\hat{\omega}$), the proposed structure will not be affected by the frequency changes. Furthermore, the generated orthogonal signal will be filtered without any delays due to resonance at the fundamental frequency as will be explained in the design procedure next.

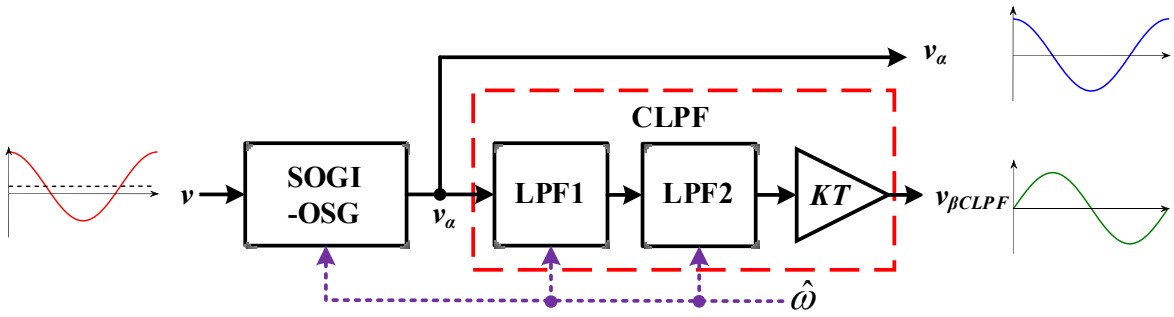


Figure 4.7. General structure of the proposed CLPF-SOGI-OSG

Consider a low-pass filter with transfer characteristic as

$$G(s) = \frac{1}{\tau s + 1} \tag{4.8}$$

where: τ is the time constant of the filter.

From (4.8), the gain (i.e., attenuation), and the phase lag frequency characteristics can be written, respectively, as

$$|G(j\omega)| = \frac{1}{\sqrt{1+(\tau\omega)^2}} \tag{4.9}$$

$$\phi = \measuredangle G(j\omega) = tan^{-1}(\tau\omega) \tag{4.10}$$

where: $\omega = \hat{\omega}$ is the frequency of the input signal (i.e., 2.π.50 rad/s).

Traditional single-stage low-pass filters can be used to generate the orthogonal signal; however, they have to be designed with a very large time constant (i.e., τ) in order to obtain the desired 90° shifted signal, inevitably making the dynamic response of the system very poor. This issue however can be effectively solved if a single-stage LPF is reconstructed using a number of cascaded LPFs with smaller time constants, thus the decay time can be reduced significantly, and correspondingly the dynamic performance can be improved as can be seen from Figures 4.8 and 4.9, respectively.

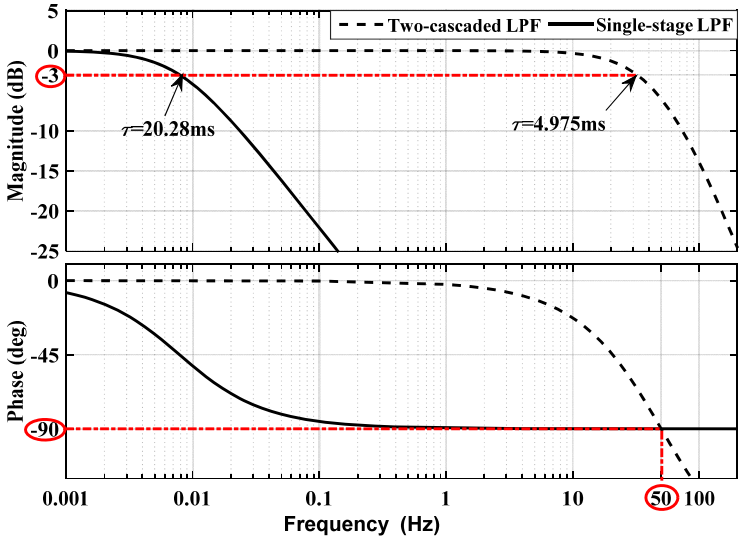


Figure 4.8. Bode-plots of (4.8) for creating v_β using single-stage LPF, and two-cascaded LPF

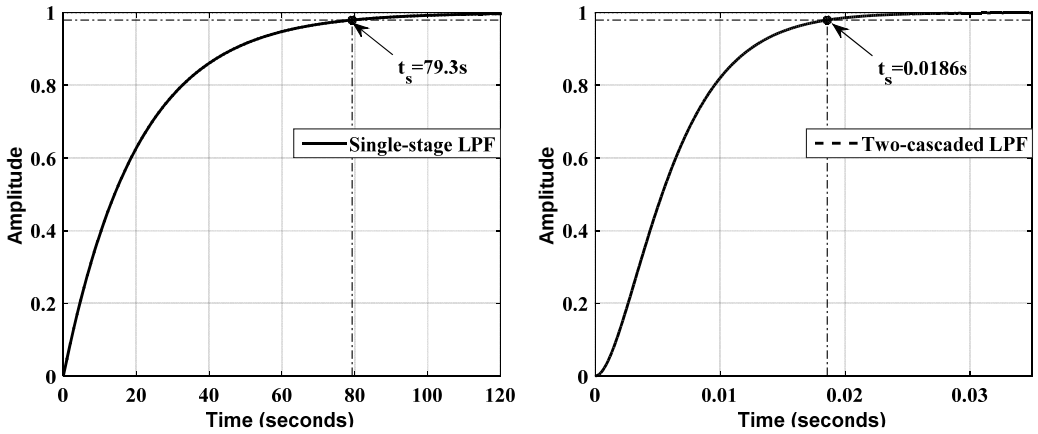


Figure 4.9. Step response of (4.8) for creating v_β using a single-stage LPF, and Two-cascaded LPF

For simplicity, cascading only two identical LPFs (i.e.,$\tau_1 = \tau_2 = \tau$) is considered in this investigation. When two LPFs are cascaded as shown in Figure.4.7, the total gain G_T and the total phase angle lag ϕ_T, can be expressed as in (4.11) and (4.12), respectively

$$\phi_T = \phi_1 + \phi_2 = tan^{-1}(\tau_1\hat{\omega}) + tan^{-1}(\tau_2\hat{\omega}) = 2tan^{-1}(\tau\hat{\omega}) \tag{4.11}$$

$$|G(j\hat{\omega})|_T = |G(j\hat{\omega})|_1|G(j\hat{\omega})|_2 = \frac{1}{\sqrt{1+(\tau_1\hat{\omega})^2}}.\frac{1}{\sqrt{1+(\tau_2\hat{\omega})^2}} = \frac{1}{\sqrt{[1+(\tau\hat{\omega})^2]^2}} \tag{4.12}$$

The generated signal v_β is required to have a unity gain (i.e., 0dB), and 90° phase-lag at a the fundamental frequency $\hat{\omega}$. Therefore, in order to achieve this, it is very important to determine the time constant τ so that the generated phase-lag ϕ_T = 90°, also to introduce a compensation gain K_T so that a unity gain (i.e., the output signal has the same magnitude as that of the input signal), is guaranteed.

Based on (4.11), with $\phi_T = 90°$ the time constant τ can be given, as

$$\tau_1 = \tau_2 = \tau = {}^1/_{\hat{\omega}} \tag{4.13}$$

Thus, the compensation gain $K_T = K_1.K_2$ can be expressed as

$$K_T = {}^1/_{G_T} = \sqrt{[1+(\tau\hat{\omega})^2]^2} = 2 \tag{4.14}$$

For a cascaded filter of (n) stages, (4.11) and (4.12) can be rewritten as

$$\tau = \frac{\tan\left(\frac{90}{n}\right)}{\hat{\omega}} \tag{4.15}$$

$$K_T = \sqrt{[1+(\tau\hat{\omega})^2]^n} \tag{4.16}$$

So, the input-to-output characteristics transfer function describing the dynamics of the two-CLPF can be expressed as

$$G_{2CLPF}(s) = \frac{v_{\beta CLPF}}{v_\alpha}(s) = \left(\frac{1}{\tau_1 s+1}\right)\left(\frac{1}{\tau_2 s+1}\right)(K_T) = \left(\frac{2}{\frac{s^2}{\hat{\omega}^2}+\frac{2s}{\hat{\omega}}+1}\right) \tag{4.17}$$

From (4.7) and (4.17), and based on the general structure of the proposed CLPF-SOGI-OSG shown in Figure.4.7, the transfer function relating the input signal v to the orthogonal output signal $v_{\beta CLPF}$ can be derived as

$$G_{\beta CLPF}(s) = \frac{v_{\beta CLPF}}{v}(s) = G_{\alpha}(s).G_{2CLPF}(s)$$
$$= \left(\frac{k\hat{\omega}s}{s^2 + k\hat{\omega}s + \omega^{\wedge 2}}\right)\left(\frac{2}{\frac{s^2}{\hat{\omega}^2} + \frac{2s}{\hat{\omega}} + 1}\right) = \left(\frac{2k\hat{\omega}^3 s}{\Delta_{CLPF}(s)}\right) \quad (4.18)$$

where: $\Delta_{CLPF}(s) = s^4 + \hat{\omega}s^3(2+k) + \hat{\omega}^2 s^2\,(2+2k) + \hat{\omega}^3 s(2+k) + \hat{\omega}^4$

Since $\Delta_{CLPF}(j\hat{\omega}) = -2k\hat{\omega}^4$, it is concluded that $v_{\beta CLPF}$ is a bandpass-filtered version of the input with 90° phase shift.

The frequency response of the transfer function (4.18) when it is compared with that of the conventional SOGI-OSG (4.7) is shown in Figure 4.10. In comparison to the conventional SOGI-OSG, the dc gain of $G_{\beta CLPF}$ (i.e., at s=0) is zero. Hence, no dc offset transfers to the orthogonal signal $v_{\beta CLPF}$. Since the dc gain of both inputs to the embeded SRF-PLL (v_{α} and $v_{\beta CLPF}$) is zero, consequently, the CLPF-SOGI-PLL will perform without any errors even if the input signal v contains dc offset or/and subharmonic components.

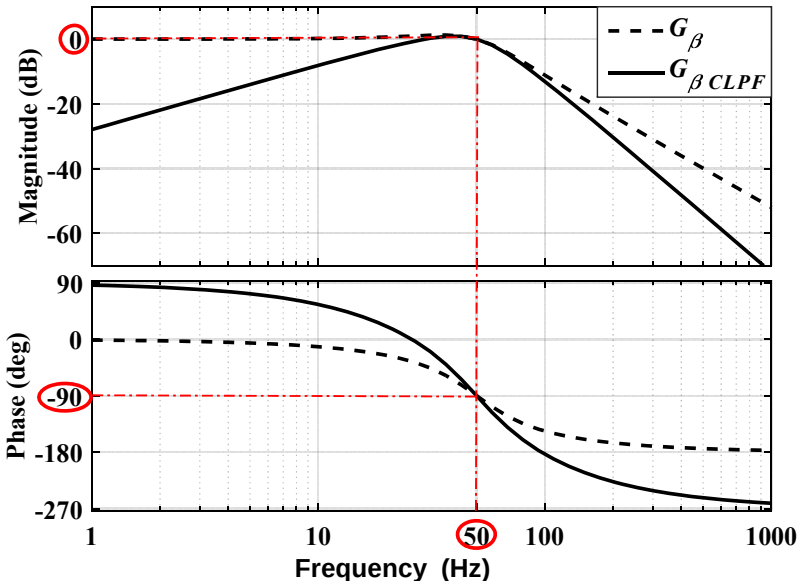


Figure 4.10. Bode plots of G_{β} and $G_{\beta CLPF}$ for k=1 and when $\hat{\omega}$ = 2π.50 rad/s.

A sample simulation result evaluating the response of the proposed CLPF-SOGI-OSG is shown in Figure. 4.11. As expected, the proposed technique continues to estimate an accurate orthogonal signal $v_{\beta CLPF}$ in spite of the deliberate disturbances in the input signal v such as dc offset and sub-harmonics.

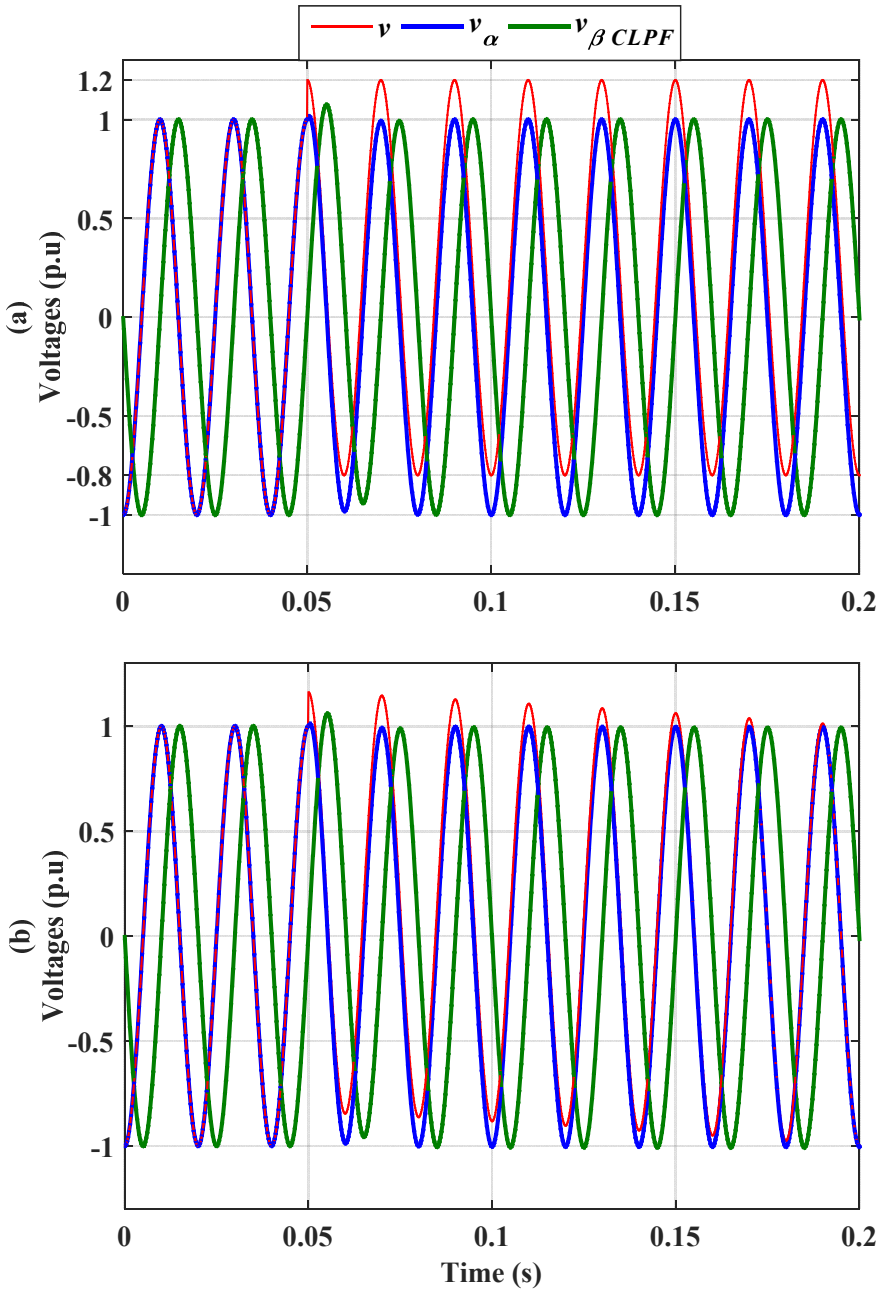


Figure 4.11. CLPF-SOGI-OSG responses when the input signal *v* at time = 0.05s undergoes (a) a dc offset of 0.2 p.u. (b) a 1Hz subharmonic and 20% of V_m. (V_m=1p.u, k=1 and $\widehat{\omega}$ = 2π.50 rad/s)

4.4.3 Other Alternative Methods

To highlight the effectiveness proposed CLPF-SOGI-PLL, two different existing approaches that have been recently used to address the problem of dc offset in the SOGI-PLL algorithm are discussed in details.

A. Ciobotaru's method [113]

A dc offset compensation method based on modifying the structure of the conventional SOGI-OSG is proposed in [113] . As shown in Figure. 4.12, if the input signal v contains any dc offset, the error signal ($\varepsilon_v = v - v_\alpha$) will carry that offset since v_α does not contain any dc component. The amplified error signal $k\varepsilon_v$ is passed through a first-order LPF to filter out any harmonics that the input signal v may contain. The output of the LPF (i.e., Δ_1), which is an estimation of the input dc component, is then subtracted from the conventional orthogonal signal v_β, that possess the same dc components. The resultant signal $v_{\beta 1}$ will be free of any dc component.

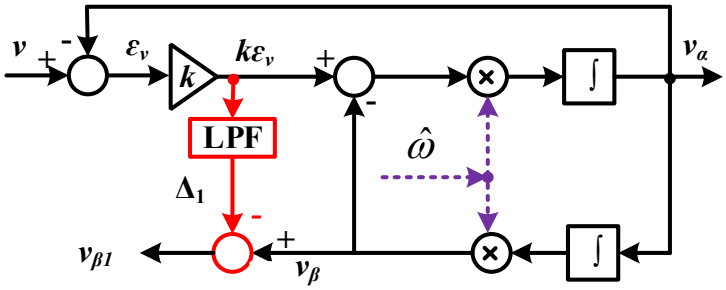


Figure 4.12. Structure of Ciobotaru's method [113]

Notice that, the alternative method of Figure. 4.12 has the same transfer function as that of the conventional SOGI method as far as v_α is concerned. On the other hand, the transfer function from the input v to the new orthogonal signal $v_{\beta 1}$ is given by

$$G_{\beta 1}(s) = \frac{v_{\beta 1}}{v}(s) = \frac{k\hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2} - k\frac{s^2 + \hat{\omega}^2}{s^2 + k\hat{\omega}s + \hat{\omega}^2}\left(\frac{\omega_{ct}}{s + \omega_{ct}}\right) \qquad (4.19)$$

where: $\omega_{ct} = 2.\pi.f_c$, is the cut-off frequency of the first-order LPF which must properly selected to attenuate higher order harmonics without degrading the dynamic response of the PLL. The Bode-plot representation and the step response of the transfer function (4.19) for three different values of f_c are illustrated in Figures. 4.13(a) and (b) respectively. Noticeably, this alternative method offers good filtering characteristics at low-frequencies, by effectively rejecting any dc or subharmonic components; however, it seriously degrades the high-

frequency harmonic filtering behaviour of the PLL system. One can select the lowest cut-off frequency, for example f_c=10Hz or less in order to improve the high-frequency filtering behaviour, but this is not acceptable since it seriously degrades the dynamic performance as shown in Figure. 4.13(b). Therefore, a trade-off between the high-frequency filtering capability and the PLL transient response must be properly made.

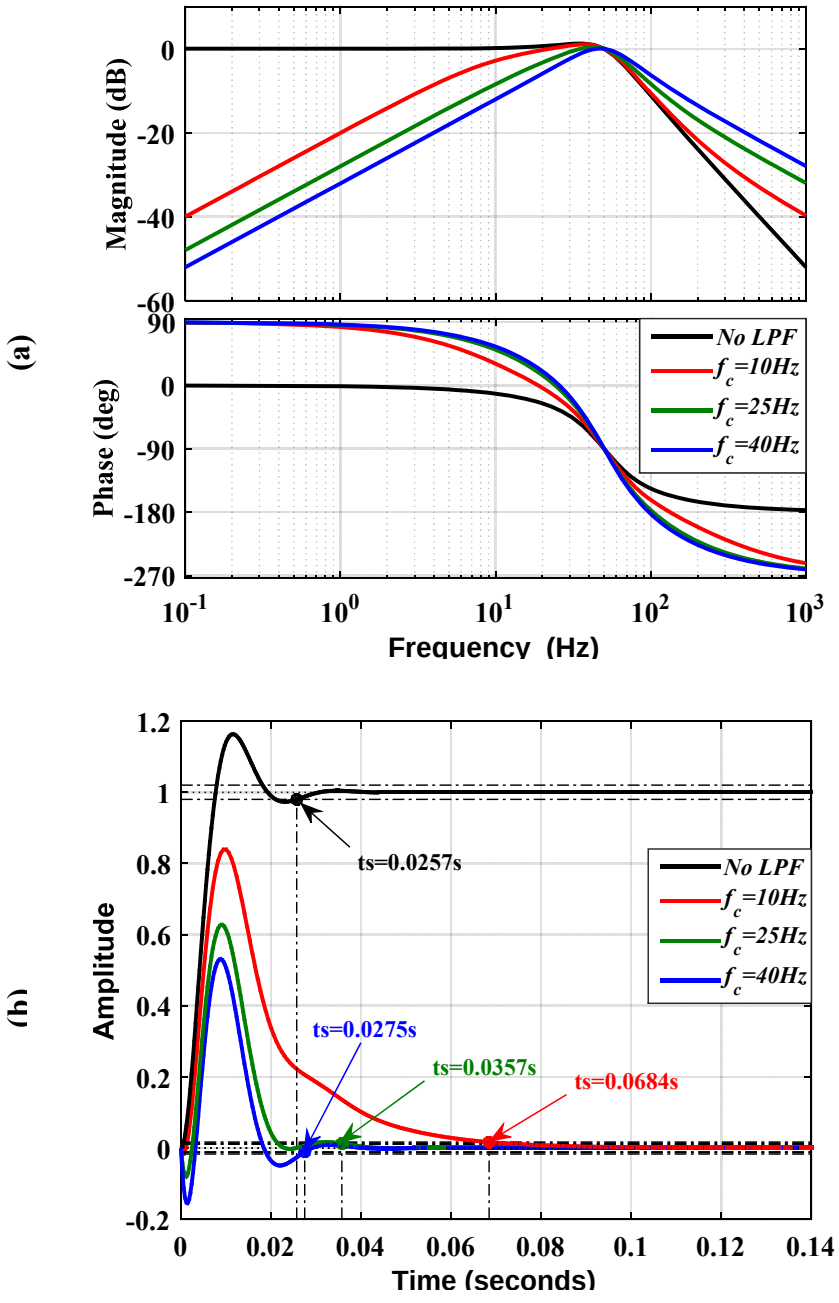


Figure 4.13. Bode-plot (a) and step response (b) of $G_{\beta 1}(s)$ at different values of f_c and when k=1

B. Karimi's method [114]

Another method based on adding a third integrator inside the conventional SOGI-OSG for removing the dc component from the orthogonal signal is reported in [114]. In this method, which is shown in Figure.4.14, the difference between the input signal v and the extracted fundamental component ($v_{\alpha 2} + \Delta_2$) is passed through an integrator. The output of the integrator (i.e., Δ_2), which is an estimation of the dc component of the input signal, is then subtracted from the PLL input signal v to remove this unwanted component. Thus, the PLL operation no longer suffers from the presence of such component.

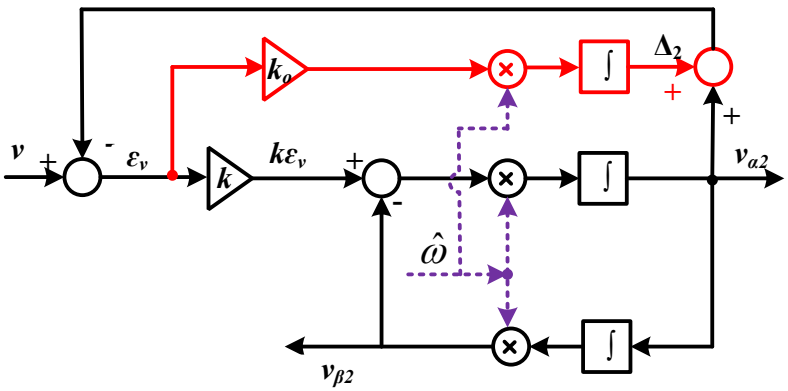


Figure 4.14. Structure of Karimi's method [114]

The characteristic transfer functions that describe this algorithm are defined as follows

$$\begin{cases} G_{\alpha 2}(s) = \dfrac{v_{\alpha 2}}{v}(s) = \dfrac{k\hat{\omega}s^2}{\Delta_2(s)} \\ G_{\beta 2}(s) = \dfrac{v_{\beta 2}}{v}(s) = \dfrac{k\hat{\omega}^2 s}{\Delta_2(s)} \end{cases} \tag{4.20}$$

where: $\Delta_2(s) = s^3 + (k + k_o)\,\hat{\omega}s^2 + \hat{\omega}^2 s + k_o\hat{\omega}^3$

The parameter k_o which is referred as the dc loop gain, can be selected based on the roots of $\Delta(s)$. For simplicity, assume that all three roots have equal real parts [114, 127] , i.e.

$$\begin{aligned} &s^3 + (k + k_o)\,\hat{\omega}s^2 + \hat{\omega}^2 s + k_o(k + k_o)\,\hat{\omega}^3 \\ &= (s + a)(s + a + j\beta)(s + a - j\beta) \end{aligned} \tag{4.21}$$

Then, this yields that k_o must satisfy

$$k_o^3 + 3kk_o^3 + (3k^2 + 9)k_o + k^3 - 4.5k = 0 \tag{4.22}$$

The equation (4.22) has two complex conjugate roots and one real root [127]. Figure.4.15 shows the real root of this equation (i.e., k_o) versus different values of k. For example, when k=1, the corresponding value of k_o based on Figure.4.15 is found to be equal to 0.2716.

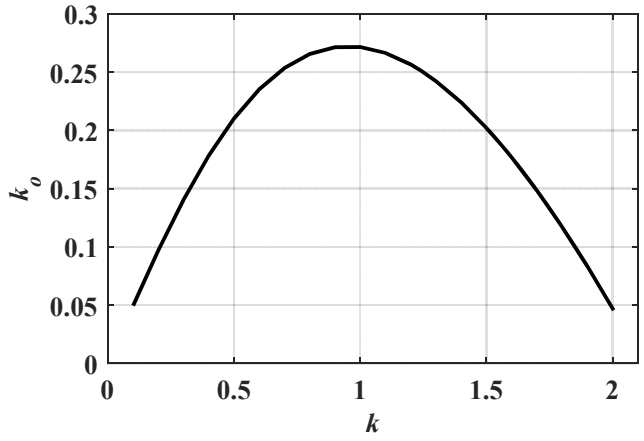


Figure 4.15. Design of dc loop's gain

The frequency response of the transfer functions (4.20) is depicted in Figure 4.16.

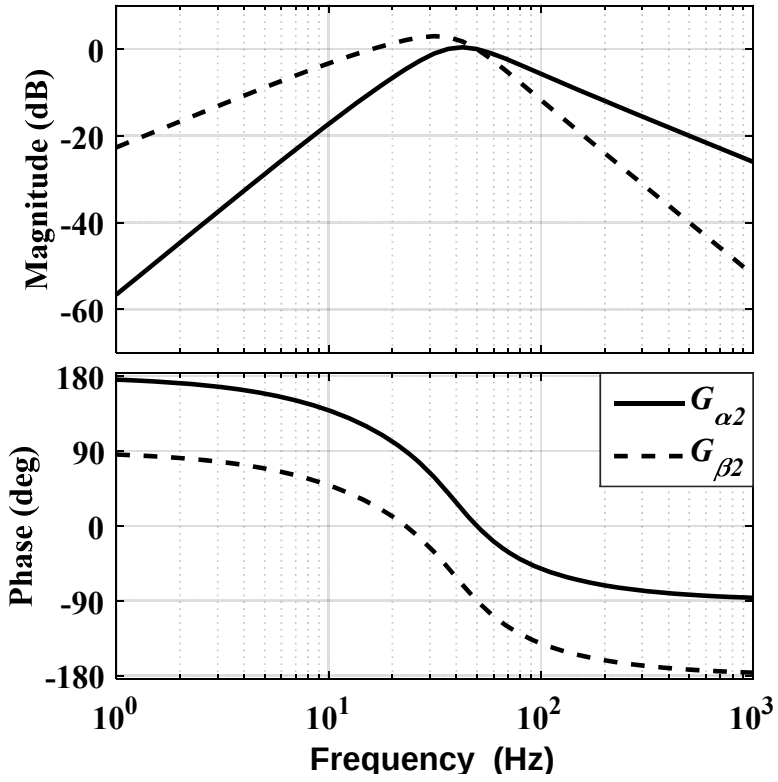


Figure 4.16. Frequency response of Karimi's method when k=1 and k_o= 0.2716

4.4.4 Comparison among CLPF-SOGI, and other existing dc offset rejection methods

For sensible comparison, the parameters tabulated in Table 4-1 are tuned, so that approximately an equal settling time is obtained for the all presented techniques.

Table 4-1 Parameters of different SOGI-OSG techniques

Conventional SOGI		Ciobotaru's method			Karimi's method			CLPF-SOGI	
t_s (s)	k	t_s (s)	k	f_c (Hz)	t_s (s)	k	k_o	t_s (s)	k
0.0257	1	0.0263	1	30	0.026	1	0.2716	0.0269	1

A step response of the above mentioned SOGI-OSG techniques with the selected parameters from table 4-1 is illustrated in Figure. 4 17. It can be observed that the settling times of all four topologies are almost equal.

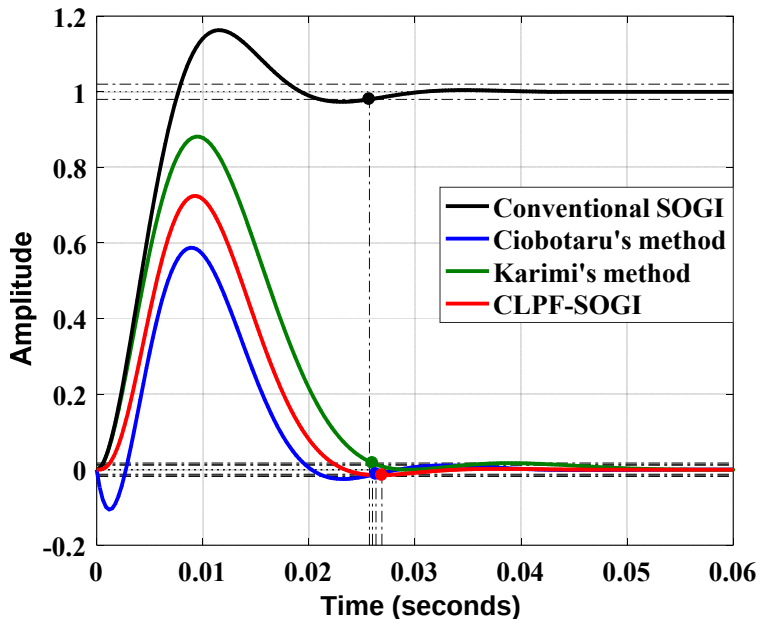


Figure 4.17. Step response of $G_{\beta}s$, $G_{\beta 1}s$, $G_{\beta 2}s$ and $G_{\beta CLPF}s$ based on table 4-1.

To evaluate the performance of the proposed method from the filtering point of view, and to compare it with that of the conventional SOGI-OSG and the two other alternative existing methods, a set of Bode-plots based on the selected parameters of Table 4.1, are provided as shown if Figures. 4.18 and 4.19.

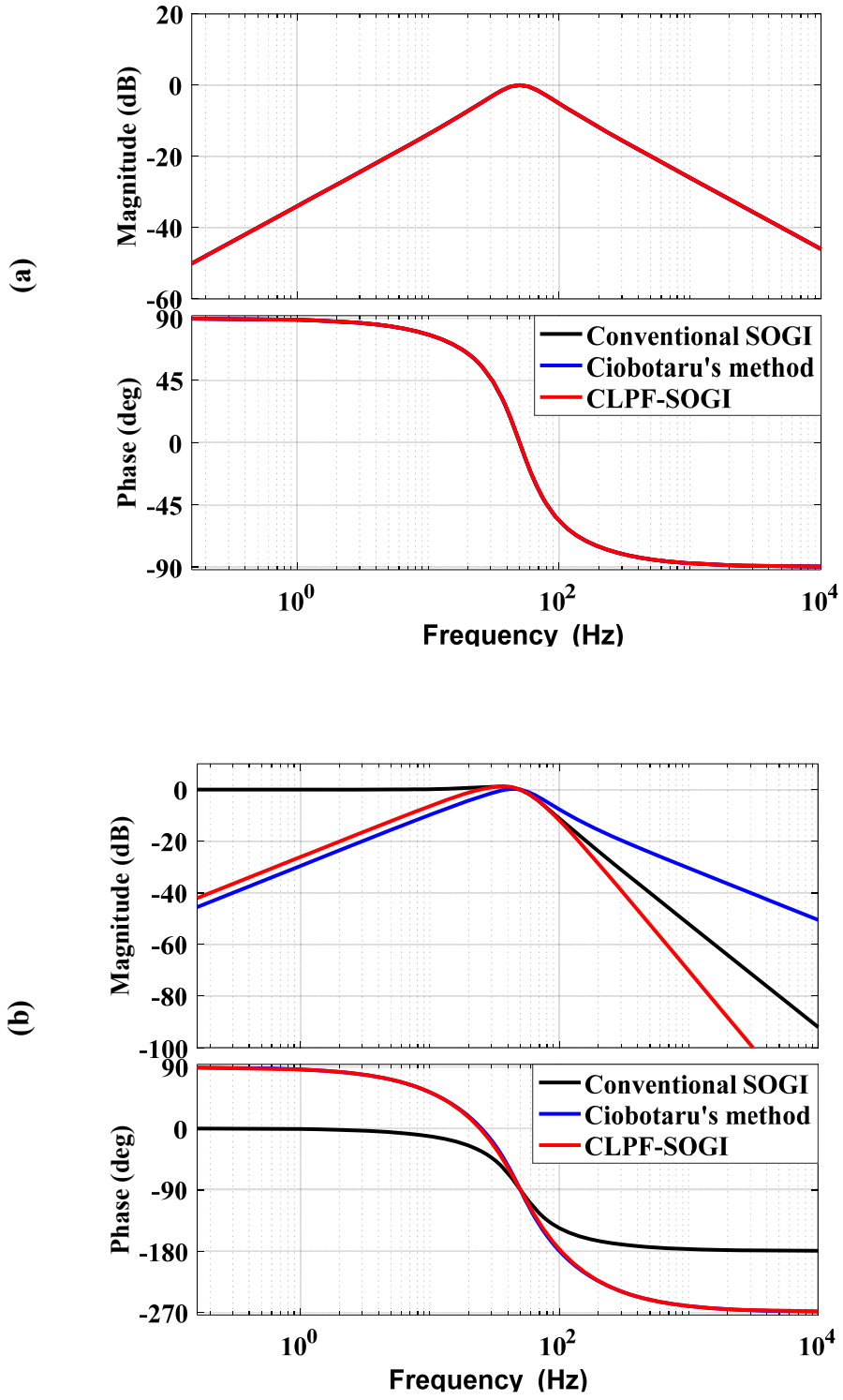


Figure 4.18. Frequency response plotted with Ciobotaru's method, proposed CLPF-SOGI, and conventional SOGI for relating (a) in-phase output to input *v* and (b) orthogonal output to input *v*.

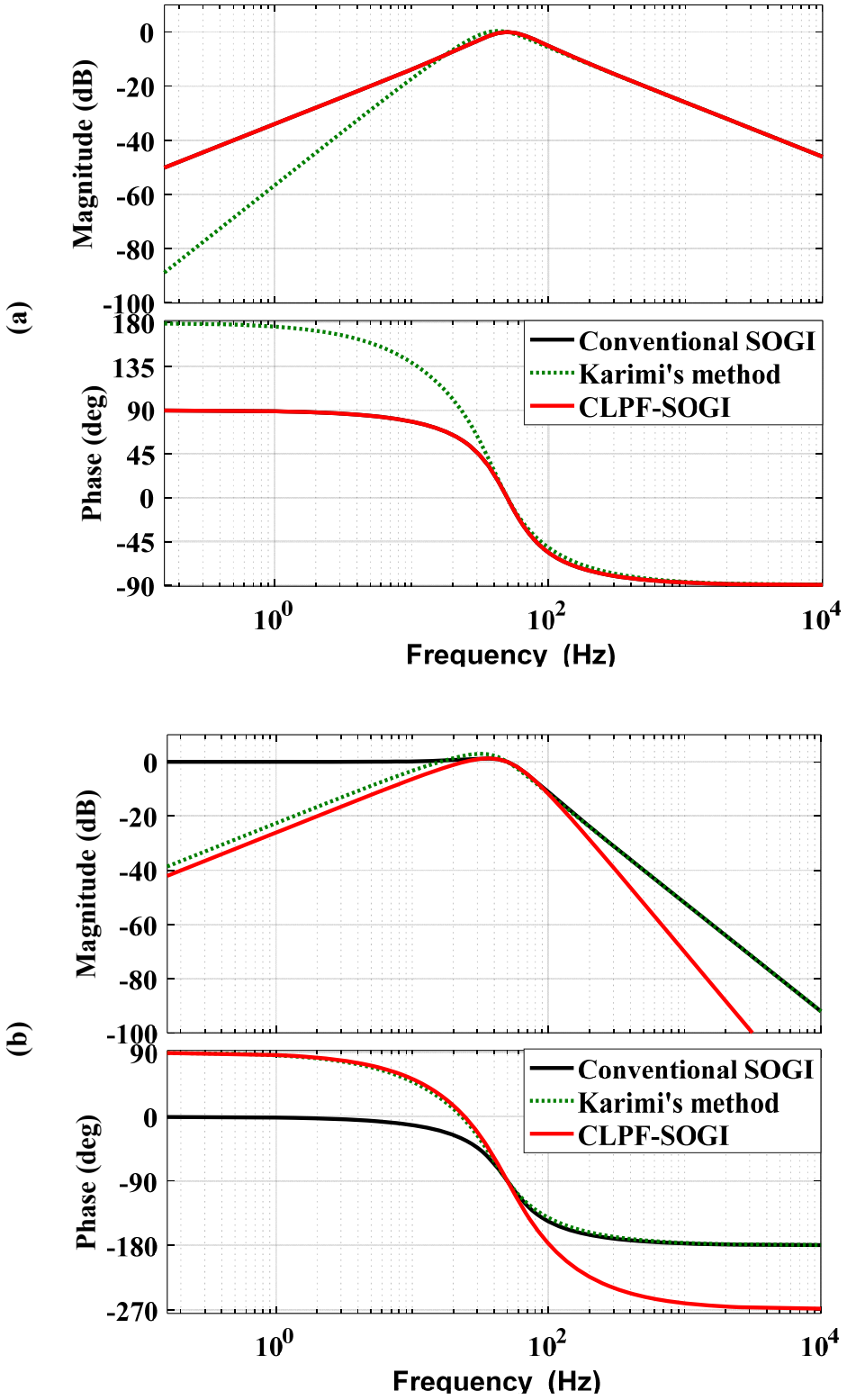


Figure 4.19. Frequency response plotted with Karimi's method, proposed CLPF-SOGI, and conventional SOGI-OSG for relating (a) in-phase output to input *v* and (b) orthogonal output to input *v*.

These Bode-diagrams lead to the following observations:

1) From Figure 4.18 (a) and Figure 4.19 (a), the proposed method and the alternative methods of [113] and [114] do not change the filtering behaviour of the in-phase output to input. Only minor improvement at lower frequency (i.e., less than 20Hz) is offered by the second method while a tiny degradation is caused by the same method at frequencies between (20Hz -50Hz).
2) As far as the in-quadrature output to the input is concerned, both alternative methods of [113] and [114] deteriorate the magnitude and phase-angle characteristics around the centre frequency of 50Hz of the generated orthogonal signal as shown in Figure 4.20. In contrast, the proposed CLPF-SOGI accurately estimates the amplitude and phase of the orthogonal signal without any errors.

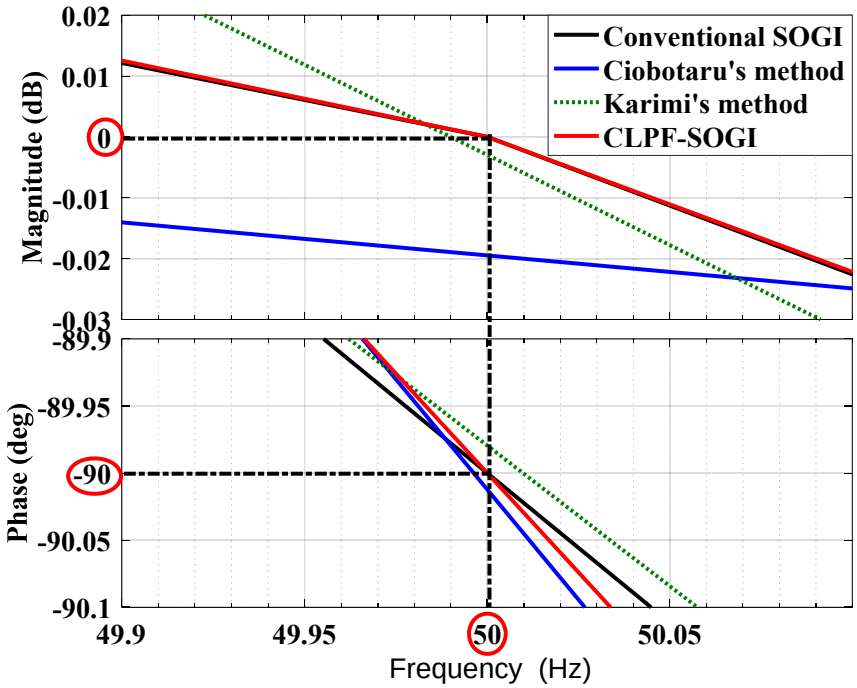


Figure 4.20. Zoomed frequency response of $G_\beta(s)$ for different SOGI-OSG techniques

3) Considering the orthogonal signal generation, the alternative method of [113] can significantly improve the filtering behaviour at low-frequencies, but at the cost of seriously degrading the high-frequency filtering characteristics of the system, as shown in Figure 4.18(b). For example, the level of degradation when compared to the conventional SOGI is about 10dB for the fifth harmonic. On the other hand, the alternative method of [114] as shown in Figure. 4.19(b) offers good filtering characteristics around subharmonics from zero to 10Hz; however, it causes some degradation at frequencies from 10Hz-50Hz. In addition,

this method has similar filtering characteristics to the conventional SOGI-OSG at frequencies higher than the centre frequency.

4) For the sake of clarity, the Bode-plot magnitude of Figures. 4.18(b) and 4.19(b) is combined together in Figure 4.21 observing that the proposed method of CLPF-SOGI offers the best degree of attenuation of high-frequency noise and harmonics when compared to the other alternative SOGI techniques. Based on Figure 4.21, a summary of the level of attenuation at different harmonic orders for different SOGI techniques is presented in Table 4-2.

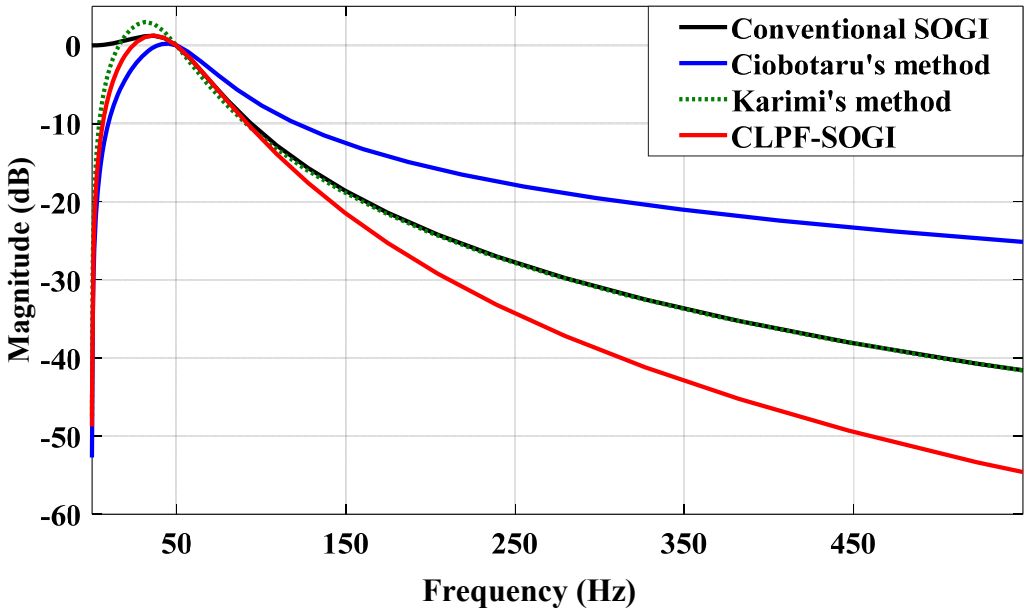


Figure 4.21. Amplitude Bode-plot of the orthogonal output to the input for different SOGI-OSG techniques

Table 4-2 Attenuation (dB) at different harmonics orders using different SOGI techniques

Harmonic order	Conventional SOGI	Ciobotaru's method	Karimi's method	CLPF-SOGI
3rd	-18.6	-12.5	-18.9	-23.1
5th	-27.7	-17.8	-27.8	-36
7th	-33.7	-21	-33.7	-44.7
9th	-38.1	-23.3	-38.1	-51.3
Rate of decay (dB)	-40.4	-22.7	-40.4	-59

4.5 Steady-state Performance Evaluation

To verify the effectivenes of the proposed method when compared to the other existing methods, a unity amplitude sinusoidal voltage signal v at a frequency of 50 Hz is considered for time domain simulations. In this simulation, the input voltage fundamantal component v is highly distotrted by 15% of the third, and 10% of the fifth harmonic, together with a 20% dc offset, leading to a total harmonic distortion (THD) of approximately 18% as shown in Figure. 4.22. It is important to notice that, in order to exhibit similar transient response for all methods, the tuning parameters presented in Table 4-1 are retained. In addition, since all four methods have similar filtering performance for the in-phase output to the input, thus, only the orthogonal output signal will be considered for this investigation. Simulations are performed in MATLAB/Simulink environment as shown in Appendix C, while the PLL parameters used for this evaluation are found in Table 4-3.

Table 4-3 PLL parameters

Parameter	Symbol	Value (unit)
PLL damping factor	ξ	0.7
PLL Proportional gain	k_p	65.45
PLL Integral gain	k_i	1784.86

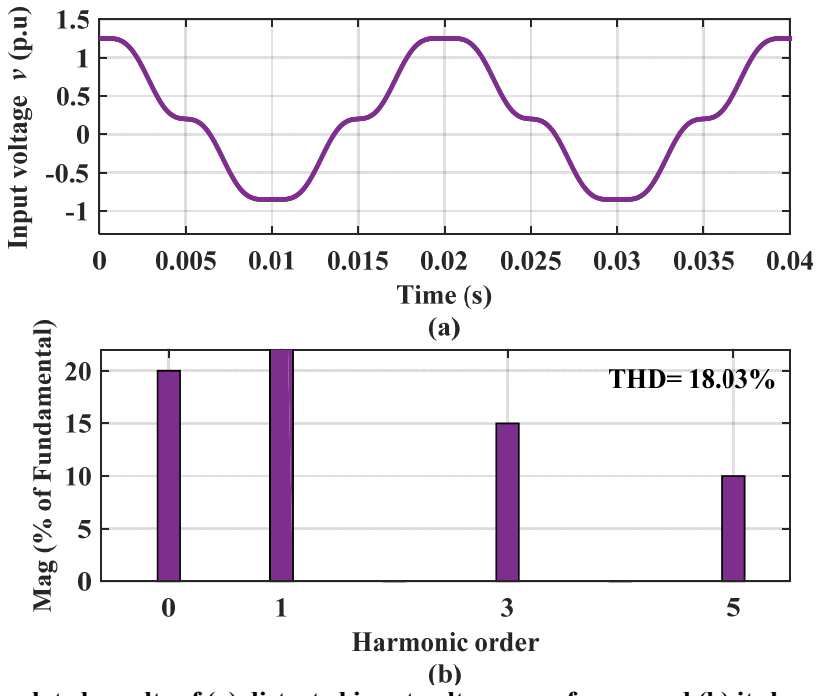


Figure 4.22. Simulated results of (a) distorted input voltage waveform *v* and (b) its harmonic spectrum

Figure. 4.23 (a) and (b) shows the orthogonal output waveform v_β and its harmonic spectrum when the input signal v described earlier is fed into the conventional SOGI-OSG. Clearly, the conventional SOGI-OSG does not reject the dc offset due to the low-pass characteristic of $G_\beta(s)$ derived in (4.7).

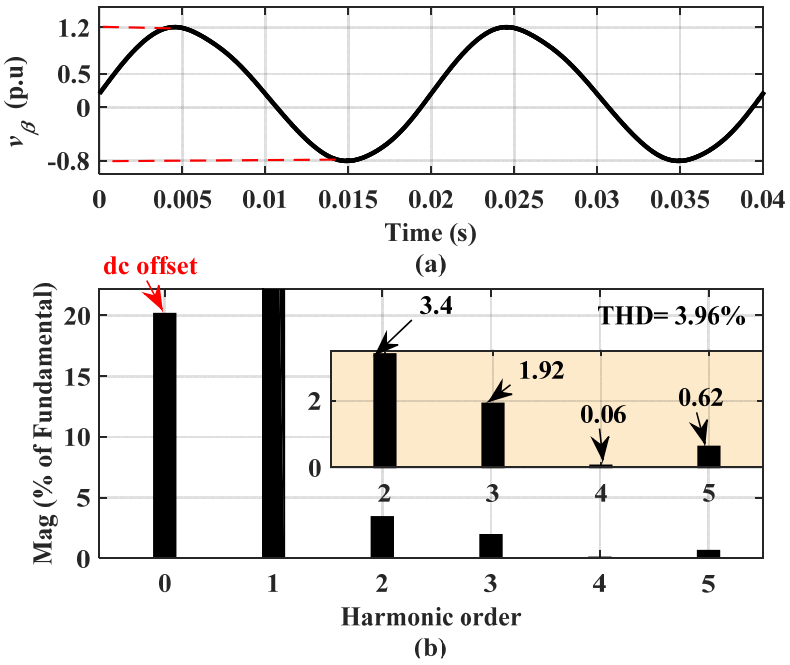


Figure 4.23. Results obtained with the conventional SOGI (a) orthogonal signal (b) its harmonic spectrum

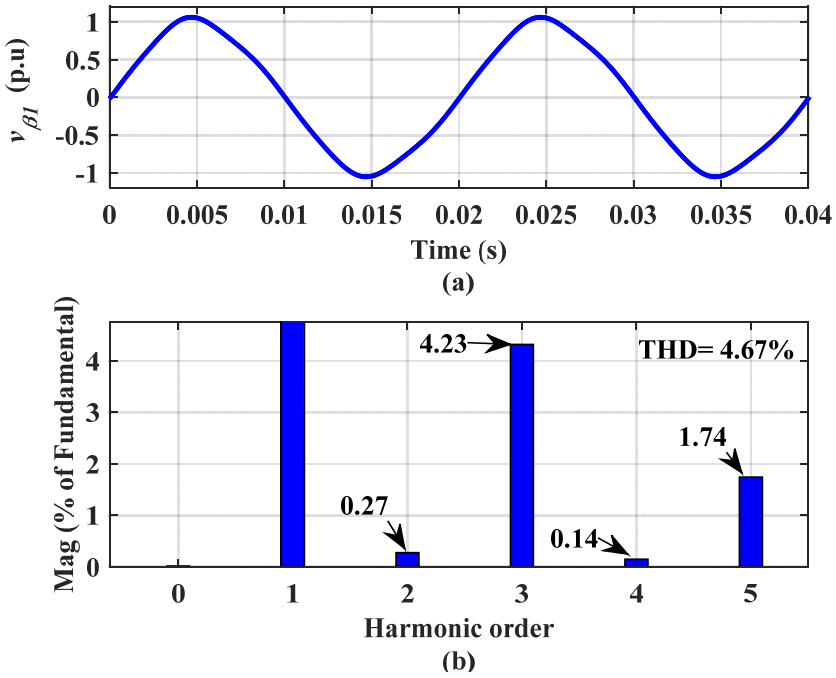


Figure 4.24. Results obtained with Ciobotaru's method [113] (a) orthogonal signal (b) its harmonic spectrum

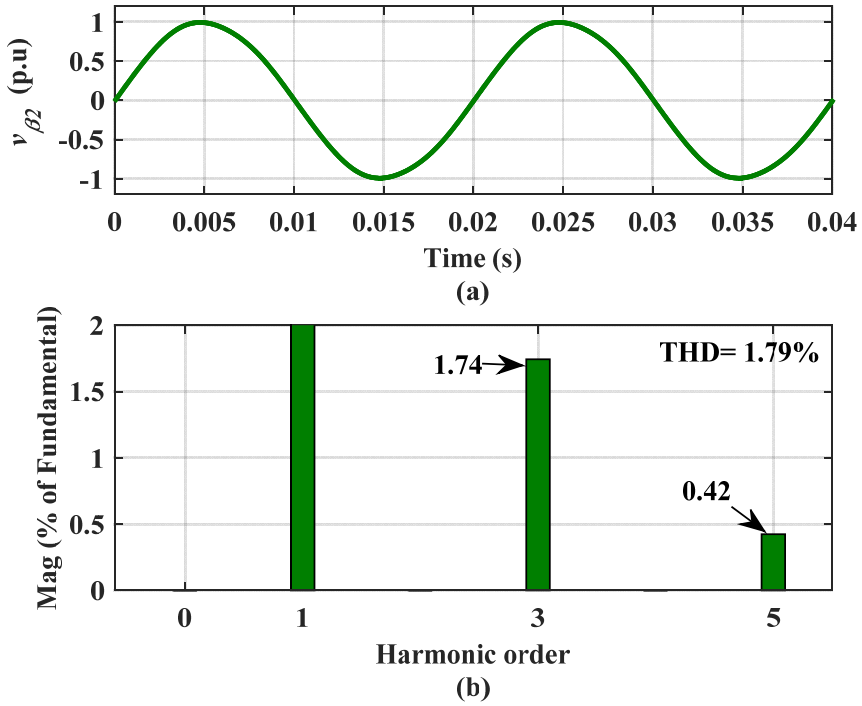


Figure 4.25. Results obtained with Karimi's method of [114] (a) orthogonal signal (b) its harmonic spectrum

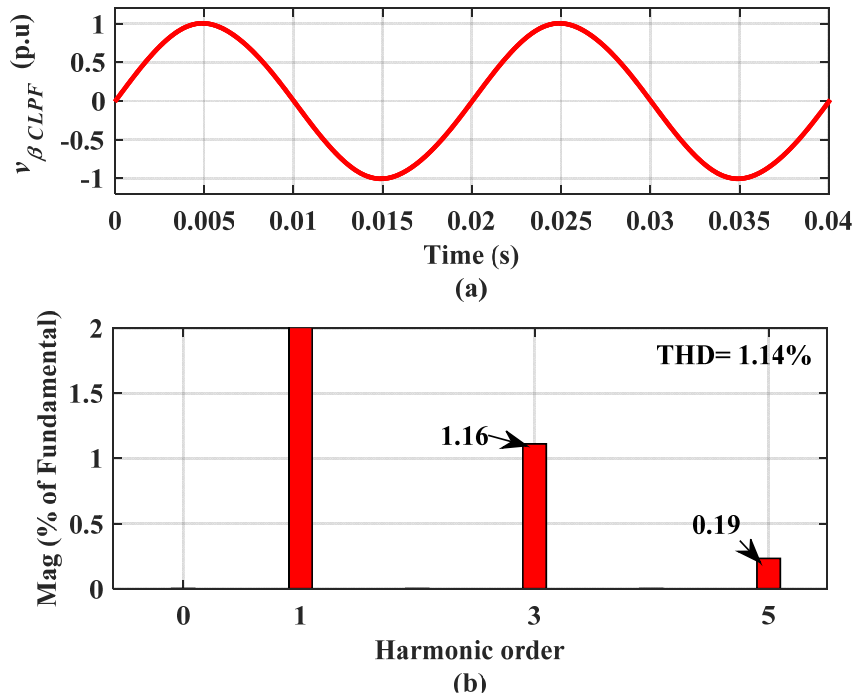


Figure 4.26. Results obtained with the proposed CLPF-SOGI (a) orthogonal signal (b) its harmonic spectrum

In comparison, Figure.4.24 shows results produced by Ciobotaru's method of [113], where the dc offset is successfully eliminated in the generated orthogonal signal $v_{\beta 1}$. However, as emphasised earlier in Figure. 4.21, this method does not produce satisfactory harmonic attenuation at its orthogonal signal $v_{\beta 1}$ due to its poor filtering capabilities at frequencies above the centre frequency $\hat{\omega}$. Figure.4.25 then shows the orthogonal signal $v_{\beta 2}$ obtained using Karimi's method of [114] and its associated harmonic spectrum. The dc offset is effectively rejected due to the band-pass filtering characteristics of $G_{\beta 2}(s)$ derived in (4.20). Again, the performance of this method at frequencies higher than the centre frequency is comparable with the conventional SOGI performance. Finally, Figure.4.26 depicts results from the proposed CLPF-SOGI-OSG; where the smoothest orthogonal waveform among the four methods can be clearly seen. Moreover, the dc-offset in $v_{\beta CLPF}$ is completely attenuated.

For the sake of clarity, the harmonic spectrum of the four methods investigated in this chapter is combined together as illustrated in Fig4.27. It is clear that Ciobotaru's method is more prone to errors caused by high-frequency harmonics than the other three methods. The reason is that for example, the conventional SOGI and Karimi's method offers transfer functions whose magnitude- frequency response as presented in Table 4-2 decays at a similar rate of -40.4dB/dec at high-frequencies, while the transfer function of (4.19) decays with a slope of -22.7dB/dec at high-frequencies. In contrast, the proposed CLPF-SOGI offers a transfer function with a slope of -59dB/dec and therefore, produces superior results as compared to the other three methods studied in this chapter.

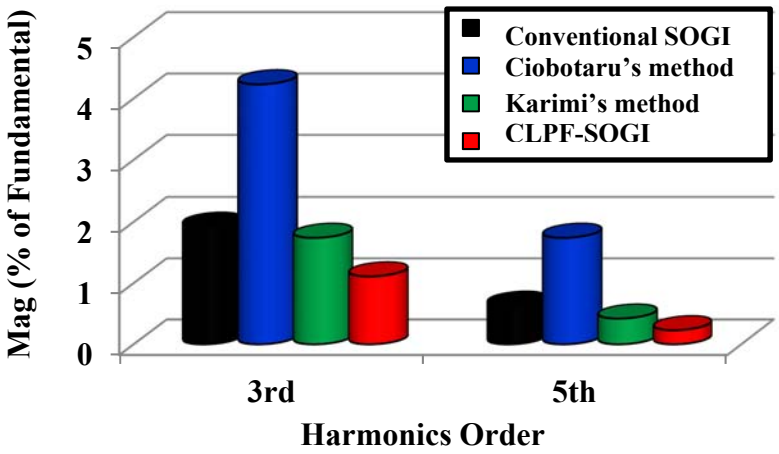


Figure 4.27. Harmonic spectrum of the four methods

4.6 The Effect of the PLL Method on the Grid-connected PV inverter Performance

According to Figure.4.1, the grid-connected PV system control strategy is based on; the PLL algorithm to ensure an accurate and fast grid synchronization, the active and reactive power (PQ) controller to generate the demand currents (i.e., i_d^* and i_q^* or i^*), and the current controller to enable an appropriate and high-quality current injection. It is also obvious that, the response of the PLL (i.e., $\hat{\theta}$, v_d, and v_q) directly affects the performance of both PQ and current controllers and, subsequently, the operation of the complete grid-connected PV system.

Thus, an investigation on how the proposed CLPF-SOGI PLL affects the performance of the grid-connected PV system in terms of the power quality is carried out using Matlab/Simulink as shown in Appendix C. In this case study, the conventional PI-current controller in the stationary reference frame is used, and the measured grid voltage signal is considered to contain dc components. This investigation shows the important influence of accurate synchronization on the response of the grid-connected PV system and reveals the considerable enhancement of the power quality of the PV system due to the proposed PLL.

In the simulation results presented in Figure.4.28, the capability of the CLPF-SOGI PLL to achieve a robust and accurate operation under the presence of dc offset in the grid voltage signal is tested. In this test, a dc offset of 0.05 p.u is deliberately added to the grid voltage signal at t=0.1s. To underline the effectiveness of the proposed PLL, a comparison between the responses of the proposed and conventional SOGI PLLs is presented. In order to have a sensible comparison, both PLLs use the parameters specified in Table 3-1. It can be noted that, the proposed PLL is able to completely reject the dc offset and perform a precise estimation of the amplitude, frequency and phase-angle of the grid voltage in less than 30ms. On the other hand, the accuracy of conventional SOGI PLL in estimating these quantities is highly affected by the occurrence of dc components in the grid voltage.

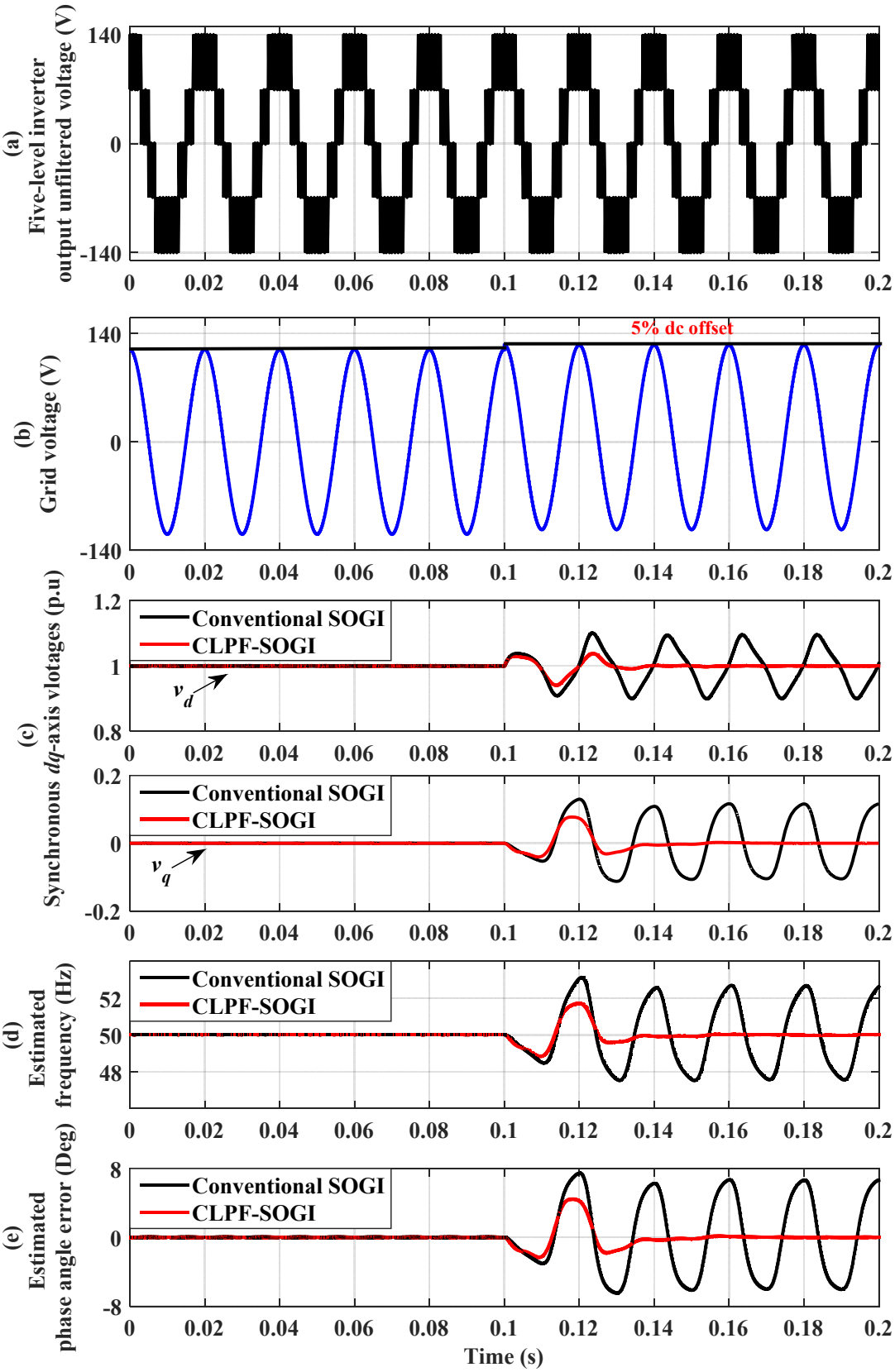


Figure 4.28 Simulation results comparing the responses of the CLPF-SOGI and the conventional SOGI PLL when the input voltage undergoes a 0.05p.u dc offset: (a) the inverter output voltage, (b) the grid voltage, (c) the synchronous *dq*-axis voltages, (d) the estimated frequency, and (e) the estimated phase-angle error

The results presented in Figure.4.28 demonstrate that, in comparison with the conventional SOGI PLL, the proposed CLPF-SOGI PLL estimates precisely the synchronisation signals (i.e., $\hat{\theta}$, v_d, and v_q) with a steady-state oscillation-free. These signals are used in the PQ controller to generate the reference currents, and in the current controller to guarantee a proper operation. Therefore, it is expected that the accurate synchronization will enhance the grid connected control and, as a consequence, the performance of the entire grid-connected PV system. In order to highlight the robustness of the proposed PLL and its effect on the performance of the grid-connected PV system, a power quality performance comparison is carried out. From the simulation results presented in Figure.4.29 (a), it is clear that, since the CLPF-SOGI PLL estimates accurately the synchronization signals, as a result, the grid-connected PV system injects a high-quality current with a total harmonic distortion (THD) of 1.79%. On the other hand, the degraded performance of the conventional SOGI PLL caused by the dc offset, increases oscillation on the estimated synchronization signals. This oscillation appears as a second-order harmonic in the generated reference current. Consequently, the operation of grid-connected PV system is greatly affected. As shown in Figure. 4.29(b), the grid-connected PV system with a non-robust synchronization method against dc offset, presents a low-quality current injection with a THD of 3.23%. This simulation study proves that, the accurate synchronization is a key aspect for the power quality of the grid-connected PV systems.

Notice that, in this simulation, owing to its simple structure, a conventional PI-current controller in the stationary reference-frame is implemented. Also, for simplicity the PQ controller which is responsible of generating the demand current is not considered in this simulation, however, instead the amplitude of demand current is generated manually with the help of the phase-angle generated by the PLL as shown in Appendix C.

A well-known drawback of the implementation of the conventional PI-controllers in the stationary reference frame is its inability to track a sinusoidal reference without steady-state error. This is due to the time-varying nature of the quantity being controlled. A sample simulation result demonstrating the behavior of such a controller is shown in Figure 4.30.

In order to overcome the limit of such a PI-controller in dealing with a sinusoidal reference, instead the PI-controller can be implemented in the synchronous reference-frame. This alternative approach to current regulation of single-phase grid-connected inverter in the synchronous reference frame will proposed in the next chapter.

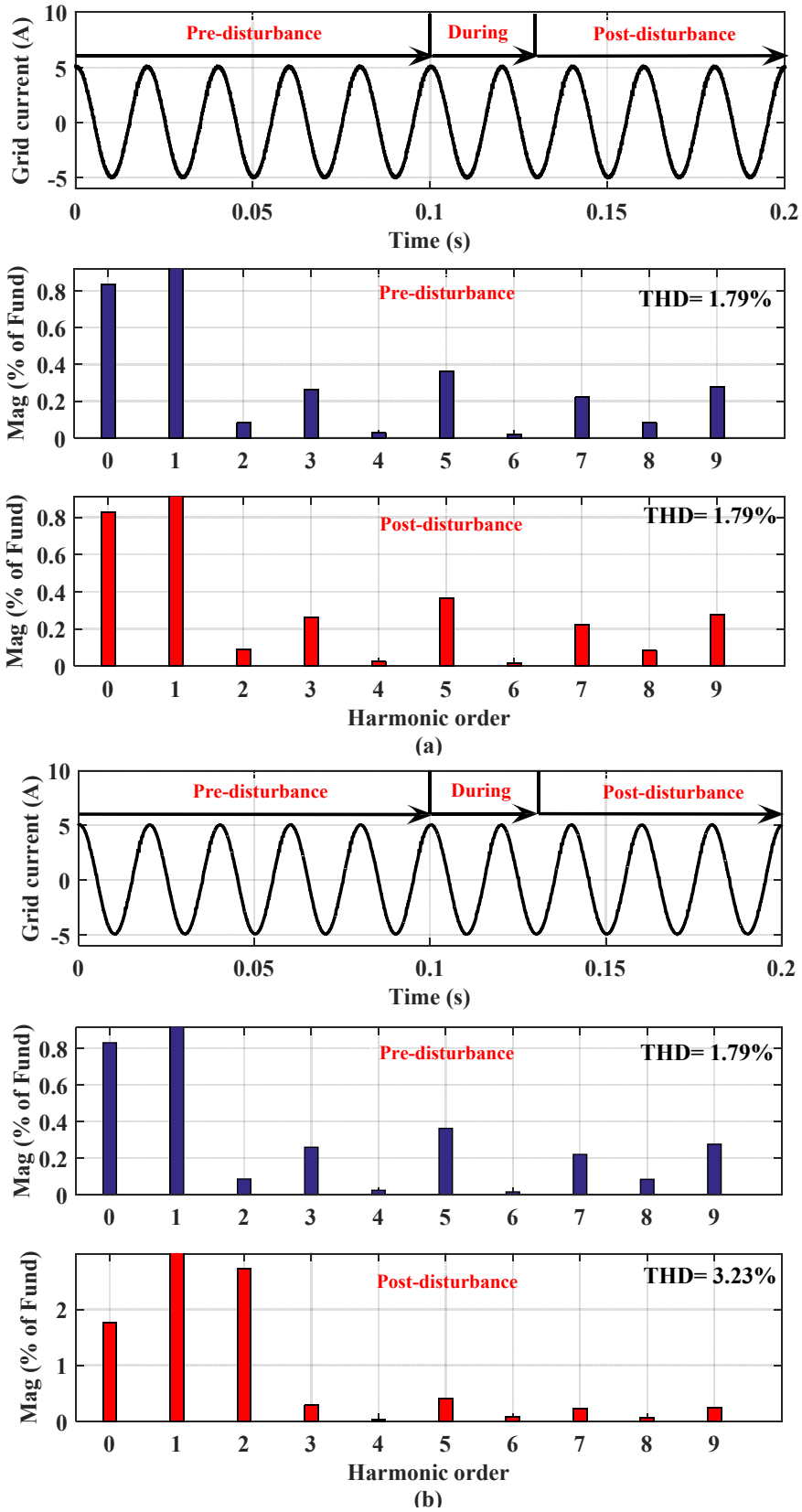


Figure 4.29. Simulation results for the performance of the grid-connected PV system when the input voltage undergoes a 0.05p.u dc offset at t=0.1s, when using (a) the proposed CLPF-SOGI PLL, and (b) the conventional SOGI PLL.

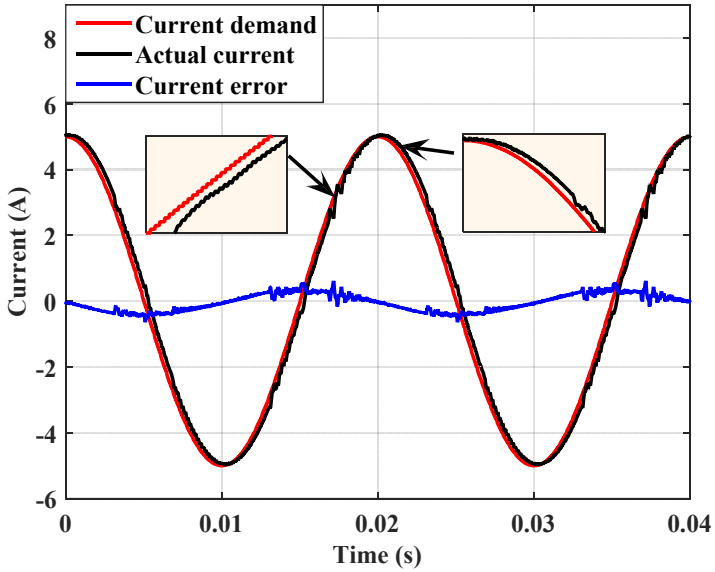


Figure 4.30. Typical behaviour of a stationary reference frame PI controller

4.7 Summary

A strategy to modify the conventional SOGI to alleviate the associated issues with the presence of dc component in the input signal has been proposed in this chapter. The proposed CLPF-SOGI method has been compared with two well-known approaches used to address the problem of dc offset in the SOGI-PLL algorithm in order to underline the effectiveness of it. It has been observed that, in addition to its ability to reject the dc offset, the proposed CLPF-SOGI offers the best degree of attenuation of high-frequency noise and harmonics when compared to the other alternative based SOGI techniques. For instant, both conventional SOGI and Karimi's method offer transfer functions whose magnitude- frequency response decays at a rate of -40.4dB/dec at high-frequencies. While, the transfer function of Ciobotaru's method decays with a slope of -22.7dB/dec at high-frequencies, which seriously degrades the high-frequency characteristics of the system. In contrast, the proposed CLPF-SOGI offers a transfer function with a slope of -59dB/dec and therefore, produces superior harmonic attenuation capability when compared to the other three methods studied in this chapter. The effectiveness of the proposed algorithm has been investigated in the frequency domain, before validation with time domain simulations.

In addition, the beneficial effect of the use of an accurate synchronization method on power quality of the grid-connected PV system has been also investigated. Results show that, in comparison to the conventional SOGI PLL, the proposed CLPF-SOGI PLL enhances the

performance of the grid-connected PV system by enabling a high-quality current injection regardless of the presence of dc offset in the grid voltage signal. For example, when deliberately introducing a dc offset of 0.05 p.u to the grid voltage signal, the proposed CLPF-SOGI PLL estimates precisely the synchronization signals required by the current controller with a steady-state oscillation-free. Consequently, the grid-connected PV system injects a high-quality current with no dc current component injection caused by such dc offset, and with a total harmonic distortion (THD) of 1.79%, which remains within the limits provided in Table 1-6. On the other hand, the inaccuracy of the conventional SOGI PLL in estimating the synchronization signals results in both dc current components and second-order harmonic in the injected grid current. This leads to a low-quality current injection with dc current component of 1.8% exceeding the limits provided in Table 1-5, and a THD of 3.23%. In general, the simulation study proves that; the accurate synchronization is a key aspect for the power quality of the grid-connected PV systems.

The next chapter introduces an alternative way of regulating the current of the proposed single-phase PV system using a PI-current controller implemented in the rotating reference frame (*dq* frame). This will be followed by a chapter that considers the implementation of grid-connected PV inverter system, which will be then followed by the experimental results of the proposed CLPF-SOGI-PLL as well as the proposed *dq* current controller validating the obtained simulation results.

CHAPTER 5

Grid Current Control

5.1 Introduction

Control of three-phase power converters in the rotating reference frame (RRF) is now a mature and well developed approach. However, for single-phase converters, it is not as well established as three-phase applications. This chapter proposes an alternative way for the current regulation of single-phase voltage-source converters (VSCs) in the RRF. A review of the methods presently employed to control single-phase systems in the RRF is introduced. The implemented test system is described, and the mathematical model for the adopted single-phase system is provided. This is followed by a design procedure of the current control loop to fine-tune its parameters and evaluate the stability of the whole closed-loop system. A brief review of the adopted conventional single-phase *dq* current control strategy is then given. Finally, the proposed simplified *dq* current control scheme is introduced with its mathematical analysis. Note that, the experimental based performance evaluation of the proposed and conventional control approaches will be presented in the forthcoming chapters.

5.2 Background

Distributed power generation systems (DPGSs) with mainly renewable energy resources such as small-scale photovoltaic and wind generation systems, has increased during recent years. In such applications, a voltage-source inverter (VSI) is interfaced to the utility grid through a low-pass filter, and a current control strategy. The control strategy is adopted by the VSI to regulate its output current and to provide a high-quality power exchange with the single-phase utility grid [2, 131]. Significant research has been conducted in the recent years on the current control of single-phase VSIs, and several advanced control strategies have been proposed. These control strategies include, hysteresis, predictive, deadbeat, proportional–integral (PI) and proportional–resonant (PR)-based control approaches [132-137].

Generally speaking, these control strategies can be classified into two major categories: 1) stationary reference frame (S_tRF) based controllers and 2) rotating reference frame (RRF) based

controllers. Among the S_tRF controllers, the use of a classical proportional-integral (PI) controller is considered as the most conventional approach, owing to its simple structure and digital implementation. However, it exhibits a well-known drawback of the inability to track a sinusoidal reference without steady-state error. This is due to the time-varying nature of quantity being controlled [22, 23]. Thus, other approaches such as S_tRF-based proportional-resonant (PR) control have been proposed [132, 133, 137]. The PR control has shown superiority in tracking ac reference signals in the stationary frame with zero steady-state error. This control approach is based on providing an infinite gain at the target frequency to eliminate steady-state error at that frequency, which is equivalent to having infinite gain in a PI-controller at dc [24, 25]. Although it is relatively simple to implement while providing satisfactory performance, PR control has several drawbacks, including an exponentially decaying response during step changes, its sensitivity to small variations in the interfaced-grid frequency, and the possibility of instability due to a small phase shift introduced by the used current sensors [24, 132].

In order to overcome the limit of a conventional S_tRF-PI controller in dealing with sinusoidal reference, the PI controller is implemented in the RRF. In an RRF, usually referred to as a *dq* frame, ac (time varying) quantities appear as dc (time invariant) quantities. This allows the controller to be designed as would be for a dc–dc converters, presenting infinite control gain at the steady-state operating point, and leading to zero steady-state error [24, 25]. The RRF-PI controller has been efficiently used for the current control of three-phase systems to obtain zero steady-state [25-28]. However, they encounter shortcomings when utilized in single-phase systems. In such systems, the use of RRF-PI controllers is not possible unless a fictitious quadrature signal is produced to form a two-axis environment (i.e.,$\alpha\beta$) [24, 29]. In the technical literature, many attempts have been reported to obtain the required orthogonal signal [9, 91, 94, 96, 98, 138]. The transfer delay technique is the earliest proposed method of obtaining the desired orthogonal signal by delaying the circuit variables by one quarter cycle of the fundamental period [91]. This method is simple and easy to implement, but phase shifting the real components to create the orthogonal signals may deteriorate the transient response of the system, as the real and fictitious axes do not run concurrently. Another approach proposes the use of differentiation to create the second set of phase variables [98]. However, the noise amplification caused by derivative function can significantly deteriorate the system performance under distorted grid voltage conditions. In [94] a Hilbert- transform, also called a

'quadrature filter', is presented. The main drawback of this approach is the high complexity and computational requirements for the control system. Estimation techniques such as Kalman filter method is proposed in [96]. Despite the advantages they offer, these techniques suffer from high complexity, and computational load. An all-pass-filter is proposed in [9] , but, the performance can be degraded with line-frequency harmonics. In [138] , the authors developed a fictitious-axis emulation technique to create the imaginary circuit with a fictitious axis running alongside with the real circuit, which helps to improve the poor dynamics of the conventional approach.

Shortcomings exist in all the orthogonal signal generation methods presented earlier due to phase delay, noise amplification; and complicated design and implementation effort. To overcome these limitations, a novel quasi-RRF-PI controller for single-phase systems is proposed. This is based on the so-called unbalanced *d-q* transformation which was originally presented in [104] for single-phase PLL systems. In this technique, the β-axis component of the controller is forced to zero, eliminating the need for the generation of such an orthogonal component. This is achieved while retaining all the advantages of operating in the rotating *dq* frame, i.e., zero steady-state error and ease of implementation. Besides, a superior dynamic performance compared to that of the conventional delay-based approach is achieved.

5.3 Current Regulation with PI Controller in the RRF

Figure.5.1 shows the schematic diagram of the study system, which consists of a single-phase VSI connected to the utility grid via an LCL filter. The filter is composed of an inverter-side inductor L_1, a parallel capacitor C_f, and a grid-side inductor L_2. The internal resistance of L_1 and L_2 are represented by R_1 and R_2, respectively.

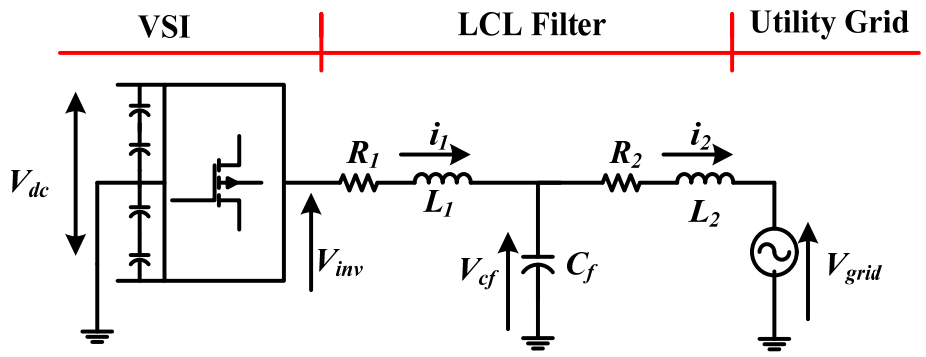


Figure 5.1. The schematic of a single-phase five-level diode-clamped grid-connected inverter test system

Since the proposed control scheme for single-phase VSIs is mainly based on the technique of vector control of three-phase systems, this method is briefly explained first. The vector control strategy based on simple PI-controllers is well-known and widely studied in the literature [28, 139, 140]. In the following, this control scheme is briefly reviewed.

5.3.1 Mathematical Model

In the following, a mathematical model of the single-phase system shown in Figure.5.1 is described. A structural diagram is derived, which is adopted for the design of both conventional and simplified controllers in the rotating reference frame (RRF). It is worthwhile mentioning here that, the DC-side dynamics of Figure. 5.1 are neglected, and it is assumed that the DC-link capacitor voltages are balanced and fixed at a desired level by connecting in series four independent ideal DC power supplies. Hence, a controller is not needed to regulate the DC-link voltage. Otherwise, an outer controller can be introduced to regulate the DC-link voltages and to generate the reference current $i_{ref,d}$ accordingly.

Based on the system shown in Figure.5.1, the dynamics of the ac side of the test system can be described as:

$$\begin{cases} v_{inv} = R_1 i_1 + SL_1 i_1 + v_{cf} \\ v_{cf} = R_2 i_2 + SL_2 i_2 + v_{grid} \\ i_1 = i_2 + C_f \dfrac{v_{cf}}{S} \end{cases} \tag{5.4}$$

where, V_{inv}, V_{cf}, V_{grid}, i_1, and i_2 represent the inverter terminal voltage, the capacitor voltage, the utility grid voltage, the converter-side current and the grid current, respectively.

In the following, the influence of the C_f capacitor of the LCL filter in the current control design will be neglected since it only deals with the high frequency switching ripple components. In fact, at frequencies lower than half of the resonance frequency, the LCL-filter inverter and the L-filter inverter models are practically the same as shown in Figure 5.2. Hence, the frequency characteristic is equivalent to that of a filter made by the sum of the inverter and grid-side inductors (L_1+L_2). Therefore, the vector control for the proposed system is similar to that used for a VSC with an L filter [11].

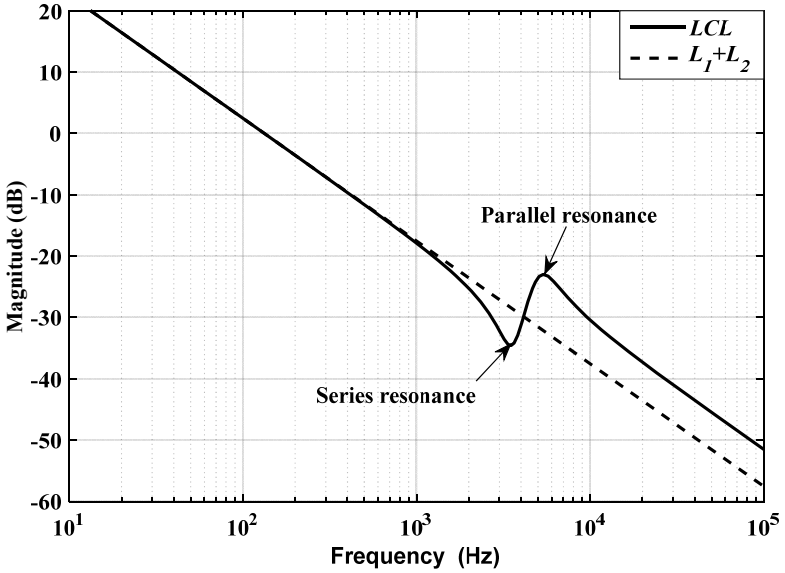


Figure 5.2. Frequency characteristics of (*i*/*v*) of the LCL filter

Thus, in the *α*-*β* frame, the single-phase grid connected inverter equation (5.1) is simplified into (5.2).

$$\begin{cases} v_{inv}^{\alpha} = (R_1 + R_2)i_{\alpha} + S(L_1 + L_2)i_{\alpha} + v_{grid}^{\alpha} \\ v_{inv}^{\beta} = (R_1 + R_2)i_{\beta} + S(L_1 + L_2)i_{\beta} + v_{grid}^{\beta} \end{cases} \tag{5.2}$$

Based on (5.2), a structural diagram of the system in the SRF (*α*-*β* frame) is drawn as in Figure. 5.3.

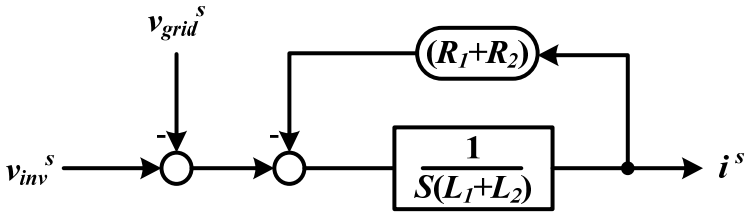


Figure 5.3. Structural diagram of the test system in the SRF (*αβ*-frame)

Note that, the superscript *s* denotes the quantities in the *αβ* frame.

Further, after applying a stationary-to-synchronous transformation to (5.2) according to $x_{dq} = x_{\alpha\beta}e^{-j\omega t}$, the dynamic of the ac-side variables expressed in the *dq* frame, are

$$\begin{cases} v_{inv}^{d} = (R_1 + R_2)i_d + S(L_1 + L_2)i_d - \omega(L_1 + L_2)i_q + v_{grid}^{d} \\ v_{inv}^{q} = (R_1 + R_2)i_q + S(L_1 + L_2)i_q + \omega(L_1 + L_2)i_d + v_{grid}^{q} \end{cases} \quad (5.3)$$

The system in the RRF based on (5.3) is diagrammatically illustrated in Figure.5.4, containing the typical coupling terms.

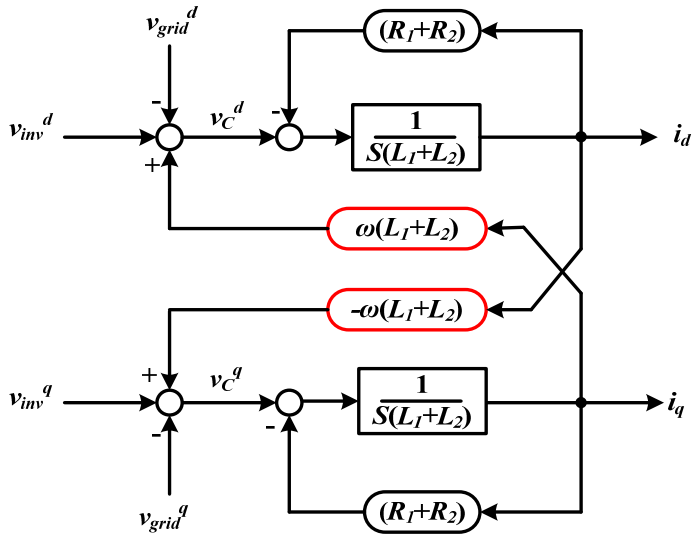


Figure 5.4. Structural diagram of the test system in the RRF

Adopting (5.3), in order to achieve a decoupled control of i_d and i_q, the terminal voltage produced by the inverter should be controlled as follows:

$$\begin{cases} v_{inv}^{d} = v_C^{d} - \omega(L_1 + L_2)i_q + v_{grid}^{d} \\ V_{inv}^{q} = v_C^{q} + \omega(L_1 + L_2)i_d + v_{grid}^{q} \end{cases} \quad (5.4)$$

where, v_C^d and v_C^q denote the control signals of the d and q axes in the RRF respectively, while ω is the nominal grid frequency (rad/s).

Substituting v_{inv}^d and v_{inv}^q from (5.4), into (5.3), yields the following decoupled system:

$$\begin{cases} v_C^{d} = (R_1 + R_2)i_d + s(L_1 + L_2)i_d \\ v_C^{q} = (R_1 + R_2)i_q + s(L_1 + L_2)i_q \end{cases} \quad (5.5)$$

As a result, the transfer function of the decoupled plant can be derived as

$$G_P(s) = (i_d/v_C^d) = (i_q/v_C^q) = \frac{1}{(R_T + sL_T)} = \frac{K_{plant}}{(1 + \tau_P s)} \quad (5.6)$$

where the time constant of plant $\tau_P = L_T/R_T$, and the gain of plant $K_{Plant} = 1/R_T$.

From (5.6), it should be noted that, since i_d and i_q respond to v_C^d and v_C^q through a simple first-order transfer function, the control rule of (5.4) is completed by defining feedback loops with simple first order PI-controllers. Based on (5.4), the structural diagram of a conventional current regulator based on PI-controllers is illustrated in Figure. 5.5, in which the voltage feed-forward (v_{grid}^d and v_{grid}^q) and the coupling terms ($\omega(L_1 + L_2)$) are shown.

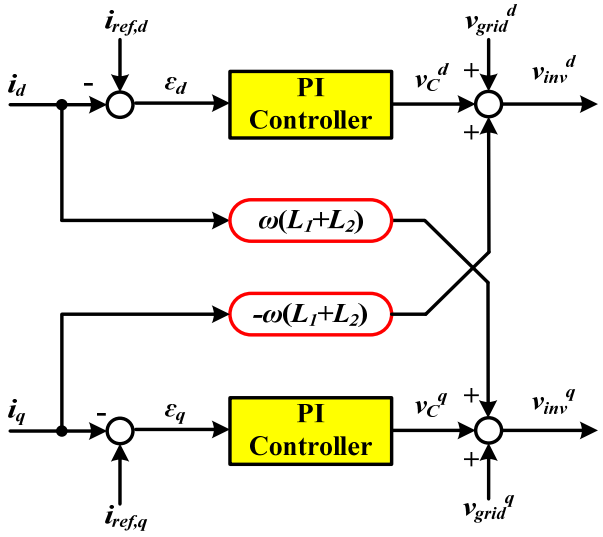


Figure 5.5. Structural diagram of the decoupled *dq* current controller

In the next section, the design procedure of the PI controllers in the RRF (i.e., *dq* frame), alongside with their associated control loops are detailed.

5.3.2 Current Control Loop

A block diagram of the corresponding current control loop in the *dq* frame is depicted in Figure. 5.6. Note that, since the *d* and the *q* current loop controllers are identical, the subscripts *d,q* were dropped.

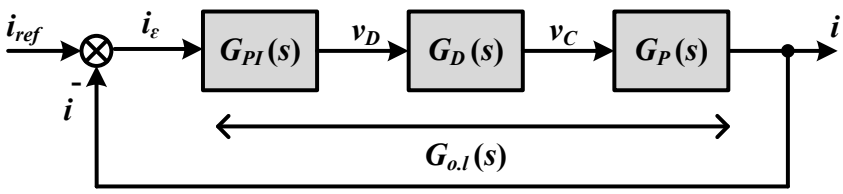


Figure 5.6. Block diagram of current control loop.

In order to achieve the pre-specified dynamics, a conventional PI current controller is adopted which is represented by $G_{PI}(s)$ and defined as

$$G_{PI}(s) = (v_D/i_\varepsilon) = \left(\frac{k_p s + k_i}{s}\right) = \frac{k_p(1+\tau_i s)}{\tau_i s} \tag{5.7}$$

where $\tau_i = k_p/k_i$, is the time constant of controller, k_p and k_i are the PI-controller gains. The transfer function $G_D(s)$ represents the delays present in the current control loop due to operation of the PWM ($0.5T_s$), together with the computational device (T_s), where T_s is the sampling time [11]. The two delays can be grouped together to form a first order element, as described in (5.8).

$$G_D(s) = (v_C/v_D) = \frac{1}{1+1.5T_s s} \tag{5.8}$$

Then, the controller is designed based on the open-loop transfer function $G_{ol}(s)$, as shown in Figure. 5.6, which can be presented as

$$\begin{aligned} G_{ol}(s) &= (i/i_\varepsilon) = G_{PI}(s).G_D(s).G_P(s) \\ &= \left(\frac{k_p(1+\tau_i s)}{\tau_i s}\right)\left(\frac{1}{1+1.5T_s s}\right)\left(\frac{K_{Plant}}{(1+\tau_P s)}\right) \end{aligned} \tag{5.9}$$

By choosing the PI-controller time constant τ_i equal to that of the dominant time constant of the plant τ_P, allows the simplification of (5.9), leading to

$$G_{ol}(s) = \left(\frac{k_p.K_{plant}}{\tau_i s(1+1.5T_s s)}\right) \tag{5.10}$$

As a consequence, the dominant pole of the system is cancelled; making the closed-loop transfer function of the system in Figure. 5.6 becomes second order as

$$G_{cl}(s) = \left(\frac{G_{ol}(s)}{1+G_{ol}(s)}\right) = \left(\frac{\frac{2k_p}{3T_s L_T}}{s^2 + \frac{2}{3T_s}s + \frac{2k_p}{3T_s L_T}}\right) \tag{5.11}$$

This means that

$$\begin{cases} \omega_n^2 = \dfrac{2k_p}{3T_s L_T} \\ \zeta\omega_n = \dfrac{1}{3T_s} \end{cases} \tag{5.12}$$

For a selected damping factor ζ, the proportional k_p and integral k_i gains of the PI-controller can be expressed as

$$\begin{cases} k_p = \dfrac{L_T}{6\zeta^2 T_s} \\ k_i = \dfrac{R_T}{6\zeta^2 T_s} \end{cases} \tag{5.13}$$

The adjustment of the current regulators according to (5.11) and (5.13) provides a good control of the overshot to the step change in the reference. Choosing to have the system to be optimally damped by setting the damping factor ζ in (5.13) to be (0.707), this results in an overshoot of about 4% as shown in Figure. 5.7.

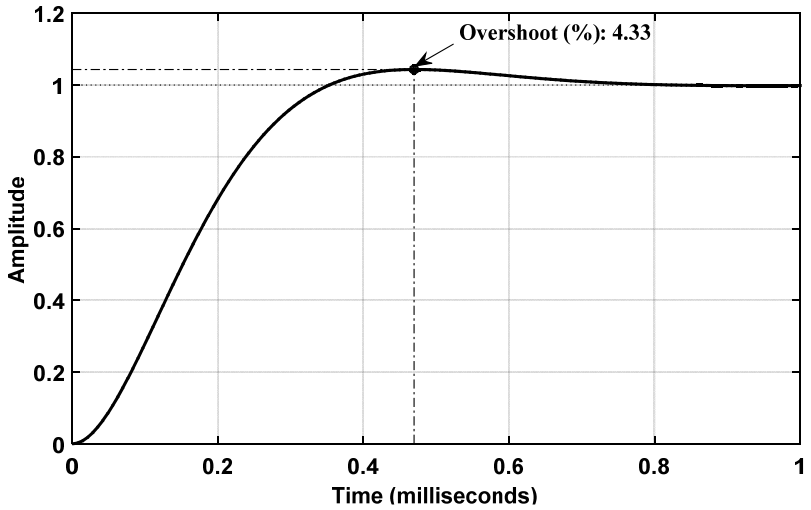


Figure 5.7. A step response of (5.11) for ζ =0.707

5.4 Conventional Single-phase *dq* Current Controller

The structural diagram of the conventional single-phase *dq* controller is shown in Figure.5.8, in which the fictitious orthogonal current component i_β is obtained by delaying the real components i_α by a quarter of the fundamental period. The measured and the shifted current components are first fed into a *αβ–dq* transformation, and a conventional *dq* current controller shown in Figure. 5.5, with decoupling strategy implemented. Then, the resulting control signals v_{inv}^d and v_{inv}^q are transformed back to the *α-β* frame to obtain the corresponding ac control signals. Typically, the *α* component (v_{inv}^α) of the control signal is employed and fed into the pulse-width modulation (PWM) stage, while the v_{inv}^β component is neglected.

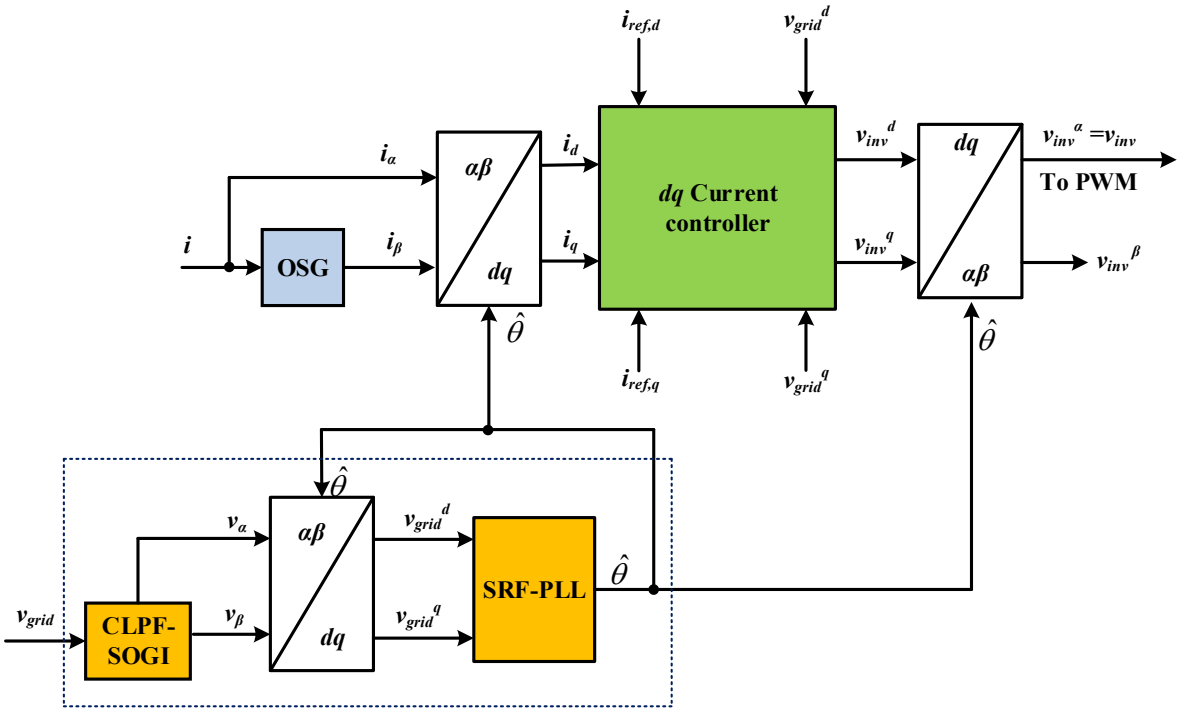


Figure 5.8. Structural diagram of the conventional single-phase *dq* controller

It is worth remarking that, a single-phase phase-locked loop based on (CLPF-SOGI-PLL) which was introduced in the previous chapter is adopted to generate the reference phase angle $\hat{\theta}$, which is required for the *αβ–dq* and the *dq-αβ* transformations as depicted in Figure. 5.8. Also, an OSG such as the CLPF presented earlier in Chapter 4, can be utilised as a means of generating the orthogonal current i_β required for this controller.

This approach is rather simple and straightforward; however, phase shifting the current to create the required orthogonal signal tends to deteriorate the transient response of the system, as the real and fictive components do not run simultaneously. Consequently, any transient in the real physical component is also experienced in the fictitious orthogonal component a quarter of fundamental period later. Since the reference current is subject to frequent step changes, delaying the current deteriorates the dynamics of the system and makes it slower and oscillatory [24] . To avoid this shortcoming, a simplified *dq* current control strategy based on the so-called unbalanced *d-q* transformation is proposed.

5.5 Simplified Single-phase *dq* Current Controller

The control strategy of the previous section necessitates a *αβ–dq* transformation, which, in single-phase systems, is not applicable because there is only one phase variable available, while this transformation needs at least two orthogonal variables. Therefore, to make the aforementioned current control strategy applicable to single-phase systems, a fictitious component orthogonal to the existing physical component should be created. Typically, this is achieved by phase shifting the measured real signal such that the physical and fictitious signals together form the *αβ*-frame. As emphasised earlier, the introduction of such delay in the system deteriorates the transient response of the system, which becomes slower and oscillatory.

To tackle the aforementioned drawbacks, a simplified *dq* current control scheme as shown in Figure. 5.9, is proposed. This approach is simply based on forcing the fictive *β*-axis component to remains zero all the time when transforming both reference and actual ac current signals (i.e.,$i_{ref,\alpha}$ and i_{α}).

The transformations from the stationary frame *αβ* to the rotating frame *dq* and vice versa are given by (5.14)

$$\begin{cases} \begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \\ \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} cos(\theta) & -sin(\theta) \\ sin(\theta) & cos(\theta) \end{bmatrix} \cdot \begin{bmatrix} d \\ q \end{bmatrix} \end{cases} \tag{5.14}$$

Since the *β*-axis is forced to be zero all the time, a simplification will result in the current control loop system as follows

Using the estimated phase angle provided by the PLL $\hat{\theta}$, a reference current $i_{ref,\alpha}$ can be defined as

$$i_{ref,\alpha} = I\, cos(\hat{\theta}) \tag{5.15}$$

Applying the *dq* transformation in (5.14) with (θ=$\hat{\theta}$), two reference currents in the *dq* frame can be determined as

$$\begin{bmatrix} i_{ref,d} \\ i_{ref,q} \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}) & sin(\hat{\theta}) \\ -sin(\hat{\theta}) & cos(\hat{\theta}) \end{bmatrix} \cdot \begin{bmatrix} i_{ref,\alpha} \\ 0 \end{bmatrix} \tag{5.16}$$

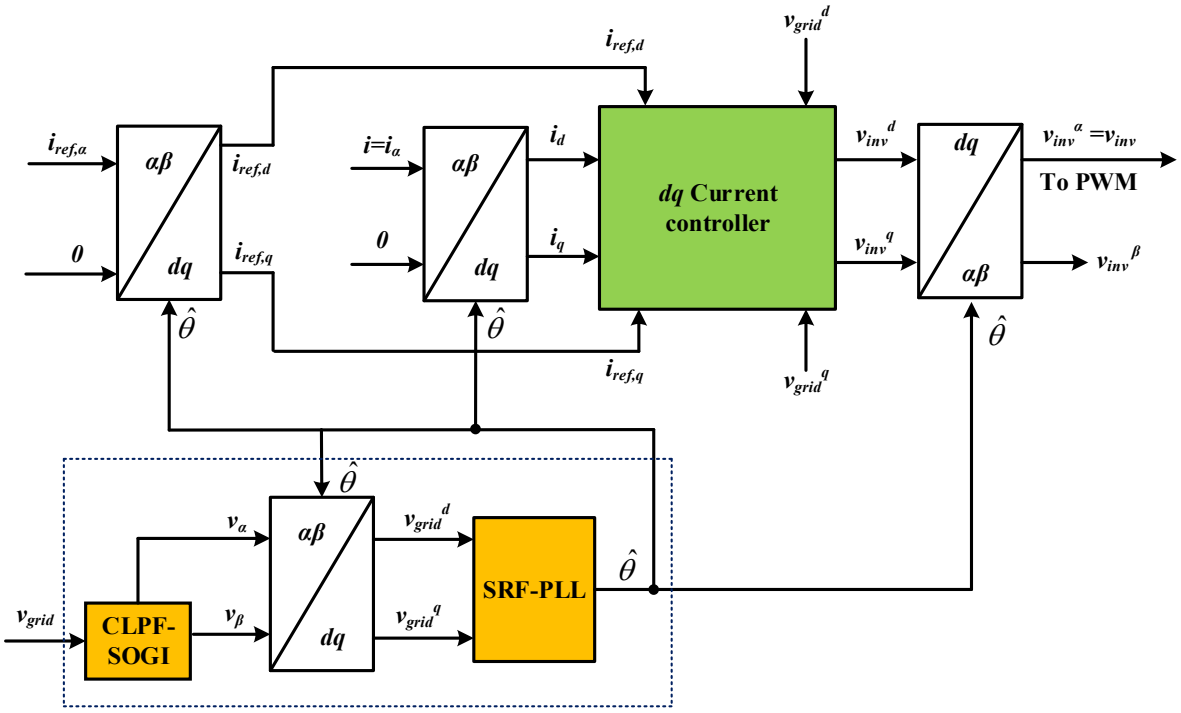


Figure 5.9. Structural diagram of the simplified single-phase *dq* controller

The actual measured current i_α is defined as in (5.17)

$$i_\alpha = i = I_m \cos(\hat{\theta}) \tag{5.17}$$

which results in two currents in the *dq* frame as

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} cos(\hat{\theta}) & sin(\hat{\theta}) \\ -sin(\hat{\theta}) & cos(\hat{\theta}) \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ 0 \end{bmatrix} \tag{5.18}$$

As a consequence, the steady state errors in the *dq* frame (i.e.,ε_d and ε_q) are given by (5.19)

$$\begin{cases} \varepsilon_d = i_{ref,d} - i_d = [i_{ref,\alpha}\cos(\hat{\theta})] - [i_\alpha \cos(\hat{\theta})] \\ \qquad\qquad = (i_{ref,\alpha} - i_\alpha)\cos(\hat{\theta}) \\ \varepsilon_q = i_{ref,q} - i_q = [-i_{ref,\alpha}\sin(\hat{\theta})] - [-i_\alpha \sin(\hat{\theta})] \\ \qquad\qquad = (i_\alpha - i_{ref,\alpha})\sin(\hat{\theta}) \end{cases} \tag{5.19}$$

Note that, for both current regulation schemes, and to prevent integral windup and unnecessary PWM over modulation, the integral term and overall output control signal are clamped by the saturation blocks of Anti-Windup and PWM Limit respectively.

5.6 Summary

Linear direct-quadrature (*dq*) PI-controllers are generally accepted due to their high performance compared to that of stationary *αβ*-frame controllers. This is because of they operate on dc quantities, achieving zero steady-state error. In single-phase systems, however, PI-based *dq* controllers cannot be directly applied due to the reduced number of input signals available compared to three-phase systems. The common approach in single-phase systems is to create a synthesized phase signal orthogonal to the fundamental of the real single-phase system. This is to obtain dc quantities by means of a stationary-frame to rotating-frame transformation. The orthogonal imaginary quantities in common approaches are obtained by phase shifting the real components by a quarter of the fundamental period. The introduction of such a delay in the system deteriorates the dynamic response, which becomes slower and oscillatory. In this thesis, an alternative controller scheme which is referred to as the simplified *dq* controller is proposed. The proposed scheme does not require orthogonal quantities to be generated, making it easier to be implemented. In this chapter, it was decided to omit a simulation study because the area was not part of the central research theme and therefore experimental results alone are considered sufficient. In this regard, the simplified *dq* control method will be experimentally evaluated and compared to the conventional delay-based *dq* control method in Chapter 8.

The following chapter will describe in detail the implementation of a grid-connected PV inverter system.

CHAPTER 6

Implementation of Grid-Connected PV Inverter System

6.1 Introduction

This chapter considers the implementation of a grid-connected PV inverter system for the experimental phase of the research work. An overview of the grid-connected experimental hardware is presented, followed by a detailed description of the system individual components and the microcontroller platform.

6.2 Overview of Experimental Grid-Connected PV Inverter System

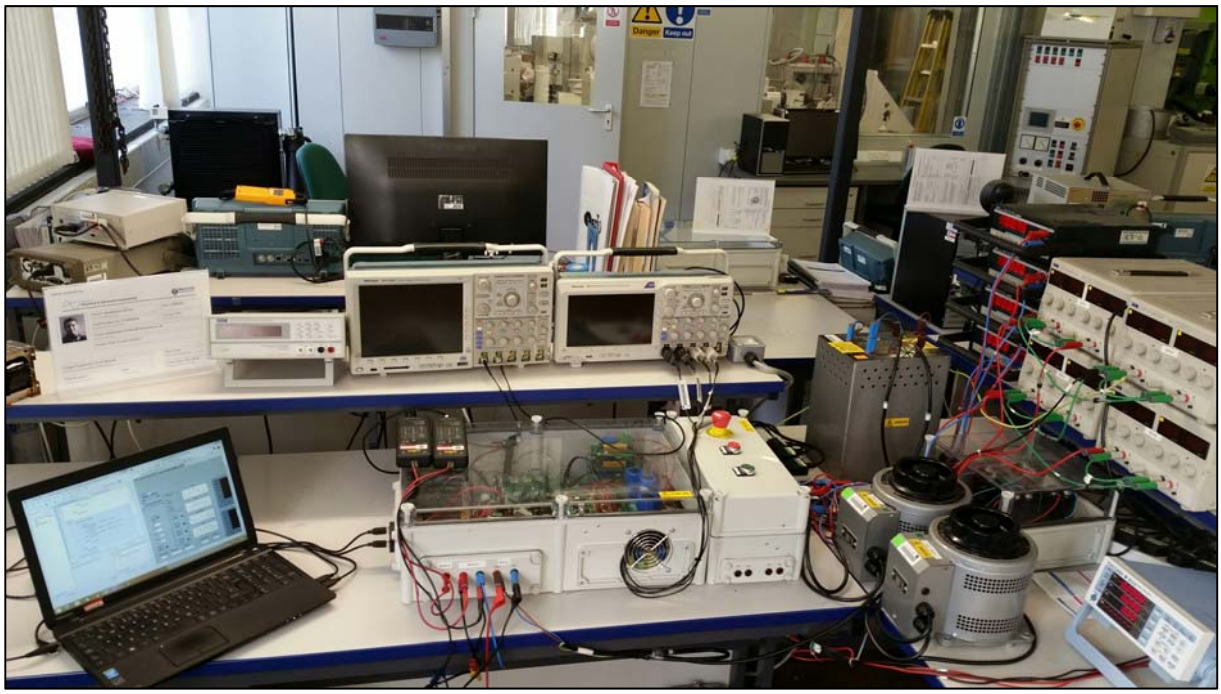


Figure 6.1. Test rig for experimental grid-connected PV inverter system.

The test bench shown in Figure.6.1 is set up in the Electrical Power (EP) laboratory at Newcastle University in order to experimentally evaluate the proposed CLPF-SOGI-PLL algorithm along with both *dq* current control methods developed in previous chapters.

Figure.6.2 shows in some details the circuit layout of the experimental test rig for the grid connection of a five-level diode-clamped inverter. The circuit consists of four series connected DC power supplies, which provide the DC link voltage required for the inverter. The inverter feeds an LCL filter, the output of which is coupled to the distribution grid via a variac and an isolation transformer. During the experimental work, a microcontroller system was employed to control the output current of the inverter system. This involved synchronization to the utility grid using an improved phase-locked loop (PLL). In the following sections, the individual experimental hardware components are briefly introduced.

6.3 DC Power Supply

For the five-level diode clamped inverter described earlier in Chapter 1, to be interfaced to the 230V mains supply, it is appropriate to have a DC bus voltage in the region of 800V. However, due to the absence of an actual solar array in the (EP) laboratory that can provide such a DC voltage level, DC supply sources are to be used instead. The DC supply sources are able to provide a relatively stiff DC voltage, and therefore acts equally to the controlled voltage output of the boost converter stage of a conventional, commercial grid connected inverter system. For the correct operation of this topology, it is required to maintain equal DC-link voltage levels; thus, four independent DC power supplies are to be connected series and utilized for this purpose as shown in Figures. 6.1 and 6.2. Although the experimental test rig was first designed to operate at the nominal grid voltage, due to economic factors associated with the project, a reduced DC voltage of 280V was used throughout the experimental test which results in about 85V on the grid side instead of 230V. It is worth remarking that, four blocking diodes (6A, 200V) as shown in Figure. 6.2 are placed between these DC power supplies and the inverter DC link to protect the power supplies by preventing reverse current flowing into the DC power supplies as they are not designed for sinking power. Also, an emergency stop button shown in Figure. 6.1 can be pressed to safely isolate the experimental inverter system in the case of emergency.

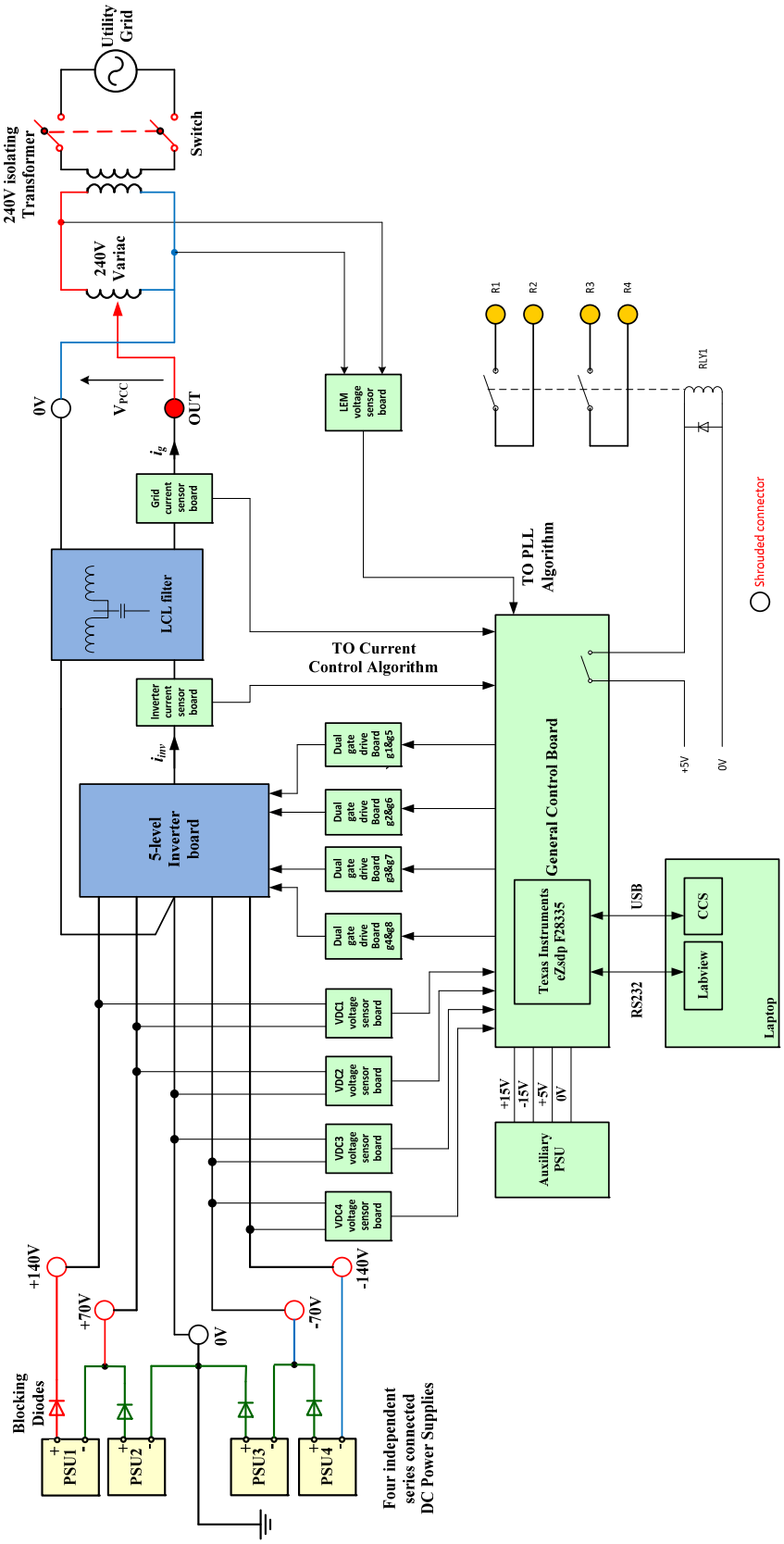


Figure 6.2. Circuit layout of the experimental grid-connected PV inverter system

6.4 Experimental Five-level Diode-clamped Inverter Module

An experimental five-level diode-clamped inverter board was built as a grid-connect power inverter to investigate the interaction between a PV inverter system and the utility grid when the proposed CLPF-SOGI-PLL and the *dq* current control schemes are adopted. A photograph of the inverter module is shown in Figure. 6.3.

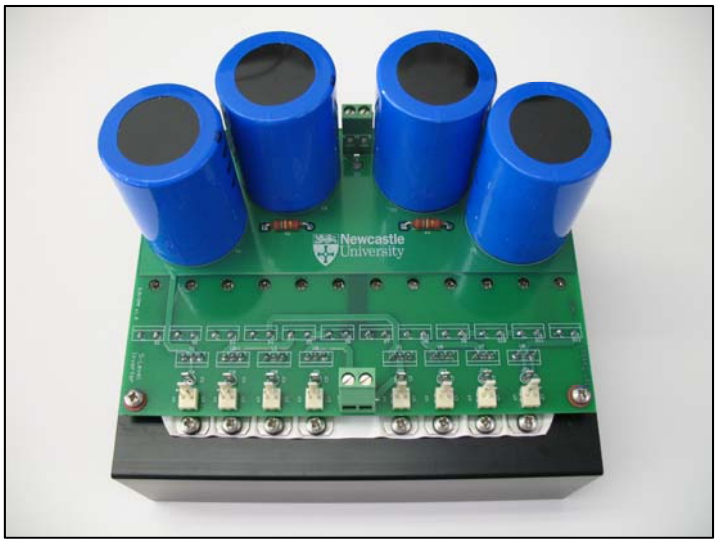


Figure 6.3. Five-level Diode-clamped Inverter

The inverter unit is rated for any DC link voltage up to 800V; compatible with a mains AC output voltage of 230V. Four polarized aluminium electrolytic capacitors (C1-C4) rated for 250V DC (1000μF each) are connected in parallel across the DC link to smooth out the low frequency voltage ripple on the DC link. Additionally, four multi-layer ceramic snubber capacitors (C5-C8) (100nF each) are connected in parallel across the DC link for the purpose of filtering high frequency components. Furthermore, four 150 kΩ voltage sharing resistors (R1-R4) are also connected in parallel with these capacitors to ensure equal voltage sharing between the capacitors. The five-level inverter itself is made up eight STP17NF25 power MOSFET devices, with the following specifications: V_{DS}=250V, V_{GS}=±20V, I_D=17A, and $T_{J(MAX)}$=150ºC, and twelve 15ETH03PBF ultrafast recovery diodes were used as the clamping diodes. In order to provide adequate passive cooling at the desired power level, all MOSFETs and diodes are to be directly mounted on heat sink as shown in Figure. 6.3. It should be pointed out that, the voltage sharing resistors are not actually required in the case when independent series connected DC power supplies are used to balance the DC-link voltage. Voltage sharing

resistors tend to be used in two-level converters with a single DC-link supply. They would also be necessary in multilevel converters such as flying capacitors type which has one supply.

6.5 Controller Details

A Texas Instruments eZdsp^{TM} F28335 floating point microcontroller board is employed for controlling the experimental grid-connected PV inverter system. This DSP has the advantage of fast processing, with hardware features such as high speed clock, off-chip SRAM memory, a built-in PWM generating circuit, RS-232 serial interface, etc. Together with the software development environment; it can meet the application requirements.
A standard general purpose power interface board designed at Newcastle University is used to provide an interface between the microcontroller board and the power circuit hardware. The main functions used in this project are:

- *Gate drive interface*: The gate drive interface includes connections of 6 pairs of eZdsp PWM signals to be interfaced to 6 external gate drive boards provided. Each interface includes two PWM signals. Also, two fault reset signals (Reset-A and Reset-B) are included on the gate driver connectors for fault indication function.
- *Sensor Interface*: Ten identical sensor interface circuits are included on the board, allowing different connection of current and voltage sensor signals to the processor ADC inputs via an op-amp. Six of these circuits are connected to sensor out-of-range trip circuits; in order to provide both overcurrent and overvoltage protection capability as will now be explained next.
- *Sensor out-of-range trip circuit*: This circuit employs six voltage window detector circuits to detect if the sensor reading goes out of normal range. In this work, four of these circuits (WD1-WD4) are connected to four voltage sensor interface circuits to facilitate fast hardware over-voltage protection across the DC link capacitors by monitoring the DC-link voltages, and ensuring that the voltage of each capacitor does not exceed the desired level. In addition, and in order to protect the inverter circuit against overcurrent, the remaining two window detector circuits (WD5-WD6) are used as over-current trip by connecting them to the inverter and the grid current sensor interface circuits. The upper and lower limits of the voltage window detector are set using a pair of trim pot variable resistors. The

dual signal voltage comparator is connected to a trip zone input signal on the DSP which can be used to disable the PWM outputs.

- *Digital to Analogue (DAC) Converter*: A 12-bit DAC is provided to allow access to internal software signals in real-time when the controller is still operating. A TLV 5604 SPI DAC is used to provide 4 DAC output channels.

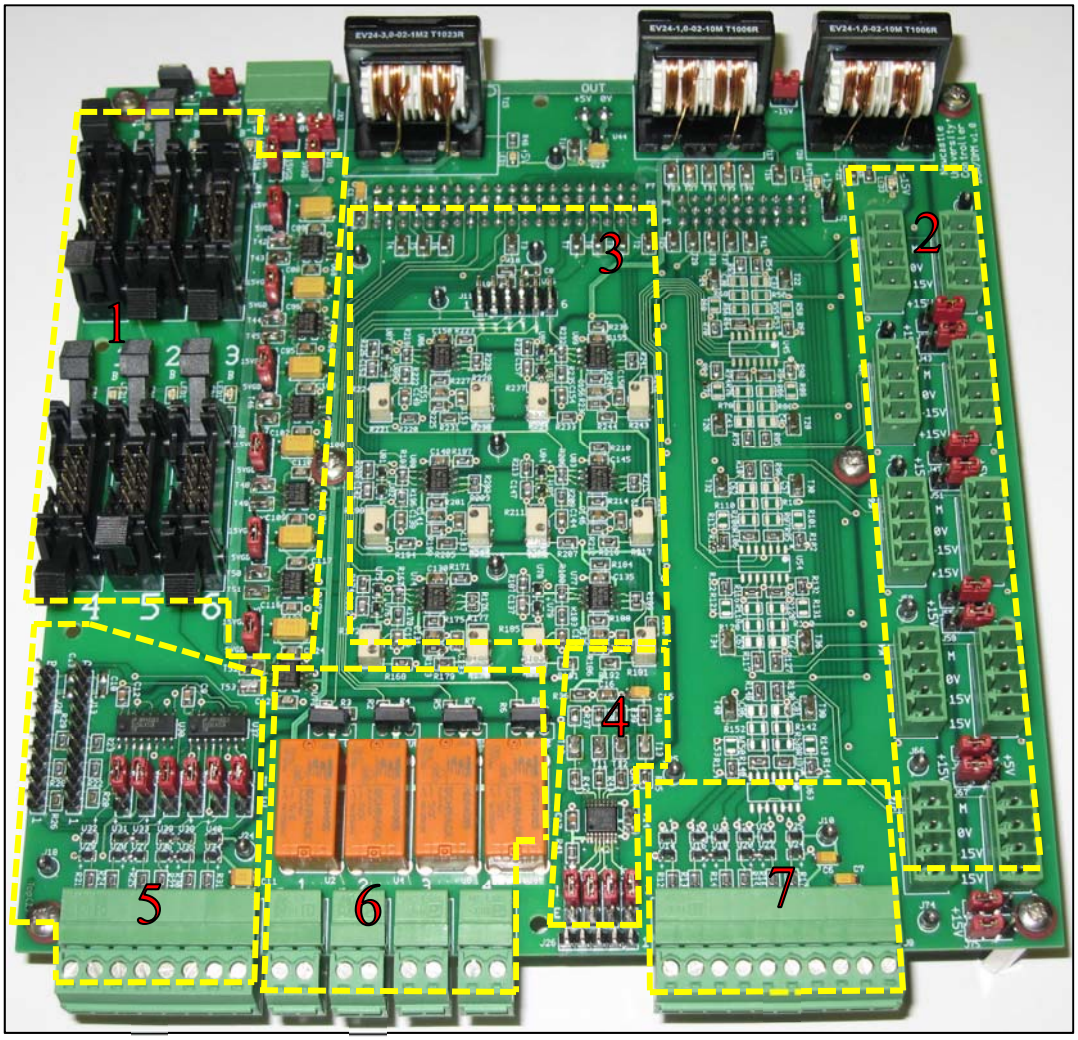


Figure 6.4. General Purpose Power Interface Board; (1) Gate drive interface, (2) Sensor Interface, (3) Sensor out-of-range trip circuit, (4) Digital to Analogue (DAC) Converter, (5) Shaft Encoder Interface, (6) Relay Circuits, and (7) General Analogue Interface

In addition to the above mentioned functions, there are also other features such as a shaft encoder interface, on-board relays, and a general analogue interface, (not used for this research). The general purpose power interface board including the above mentioned features is shown in Figure. 6.4.

6.6 Gate Drives

The gate drive signals of the five-level inverter are provided by four identical dual gate drive circuit boards as shown in Figure 6.5. Each dual gate drive board contains two identical gate drive circuits input control interface circuit (A and B). The gate drive circuits operate as a complimentary pair in order to control the two complimentary switches (i.e., S_1 and S_1') of the five-level inverter. The gate drivers take the PWM switching signals provided by the microcontroller module and switch the MOSFETs by applying the gate voltage across MOSFET drain and source (V_{DS}). A gate drive module based on ACPL-332J opto-coupled driver device is used on this board. The dead-time for the gate driver module is set to be 1*us* to prevent shoot-through of the MOSFETs.

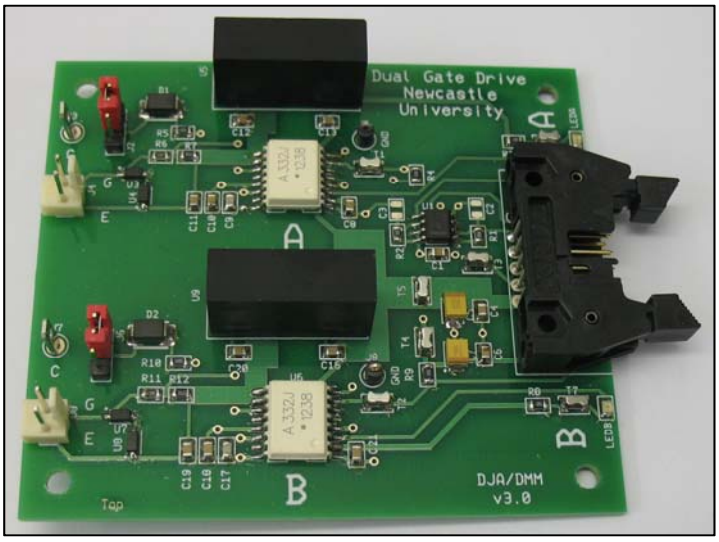


Figure 6.5. Dual gate drive board

6.7 Voltage and Current Sensors

For the purpose of output current control, two current sensors are included to measure the inverter output and the grid-side currents. One of these values, through the sensor interface, will feed into the DSP to serve as feedback signals to the control loop. Also, a voltage sensor is used to measure the grid voltage and feed it back to the controller for both the PLL as well as for terminal voltage feedforward compensation. These sensors implement hall-effect transducers (current: LEM CAS15-NP, voltage: LEM LV25-P) due to their good overall performance, high immunity to external interference, and ease of use.

6.8 AC-Side Filter

Higher order LCL filters can provide higher harmonic attenuation capability around the switching frequency, leading to a decrease in the size of filter when compared to the traditional L filters. Therefore, an LCL filter is connected to the output of the inverter as shown in the circuit layout of Figure. 6.2. Further details on the design of this filter can be found in Appendix B. The specifications of the LCL filter used in the experimental phase are summarized in Table 6-1.

Table 6-1: LCL filter parameters

Symbol	Description	Value	Unit
V_{grid}	Nominal grid voltage (rms)	85	V
V_{dc}	DC-link voltage	280	V
f	Nominal grid frequency	50	Hz
f_{sw}	Switching frequency	20	kHz
i_g	Nominal grid current at 50Hz	5	Arms
Δig	Grid ripple current at 20kHz	0.5	Arms
P_{loss}	Total loss of both inductors at full load current	≤ 6	W
L_1	Inverter-side inductor	0.81	mH
R_1	Inverter -side resistor	0.113	Ω
C_f	Parallel capacitor	3.3	μF
L_2	Grid-side inductor	0.14	mH
R_2	Grid-side resistor	0.103	Ω

All the above hardware components have been mounted together in an enclosure as shown in Figure. 6.6.

6.9 Variac and Isolation Transformer

The five-level diode clamped inverter is coupled to the supply network through a variac and an isolation transformer. An isolation transformer is included to protect the mains supply from any excessive DC current components that might arise at the inverter output due to the experimental nature of the work, while, the variac is included to allow variable control over the voltage at the inverter output circuit. This allows initial experimental work to be carried out at low voltage levels. Once deemed to be working, the variac is turned up for further testing at a desired voltage level.

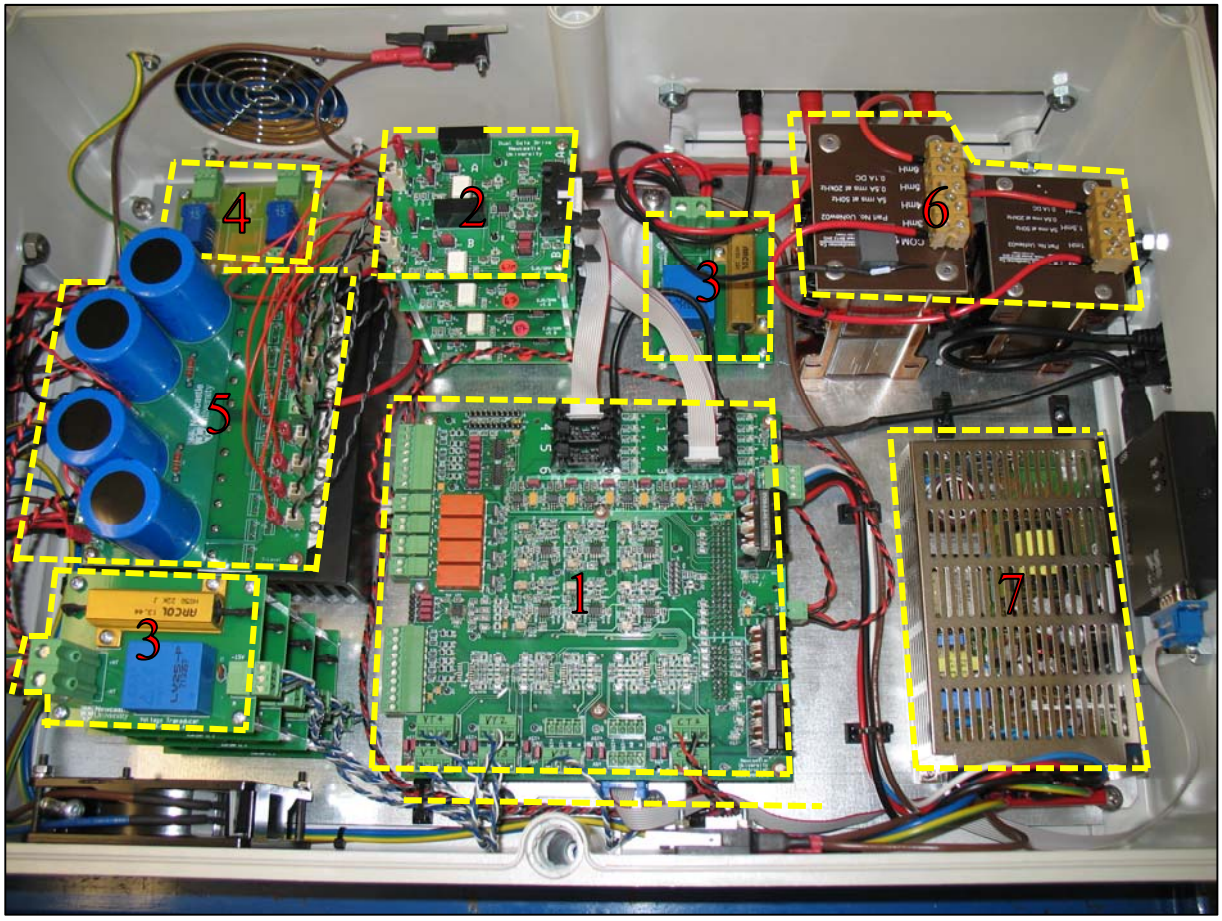


Figure 6.6. Five-level diode-clamped inverter system including: 1) Power interface board. 2) Dual gate drive boards. 3) Voltage sensor boards. 4) Current sensor boards. 5) Five-level diode-clamped inverter 6) LCL filter 7) Control board PSU

6.10 Software Development Environment

The Code Composer Studio, a development environment supplied with the eZdsp board is used to programme and debug the real-time control code. To control the microcontroller in real-time operation, a user control panel LabVIEW-TM is used to communicate in a safe way with the DSP via an RS232 serial interface. The test and control information are uploaded to the DSP and the system parameter measurements are downloaded from the DSP during the operation.

6.11 The implementation of the PLL based CLPF-SOGI

The grid-connected PV inverter system must operate in a unity power factor with respect to the network voltage. In this thesis, this is achieved by implementing a Phase-Locked Loop (PLL). In the previous chapters, the whole PLL system as shown in Figure.6.7 was represented in the *s*-domain. However, since the experimental implementation of the grid-connected PV system

is to be realized and executed in digital signal processor environment; hence a discrete-time model of the whole PLL system is to be developed to facilitate such an implementation.

In order for the digital implementation response to correspond to the theoretical studies, it is very important to make a correct discretization to optimize their behaviour. Thus, in the following, a digital implementation of the PLL system will be carried out.

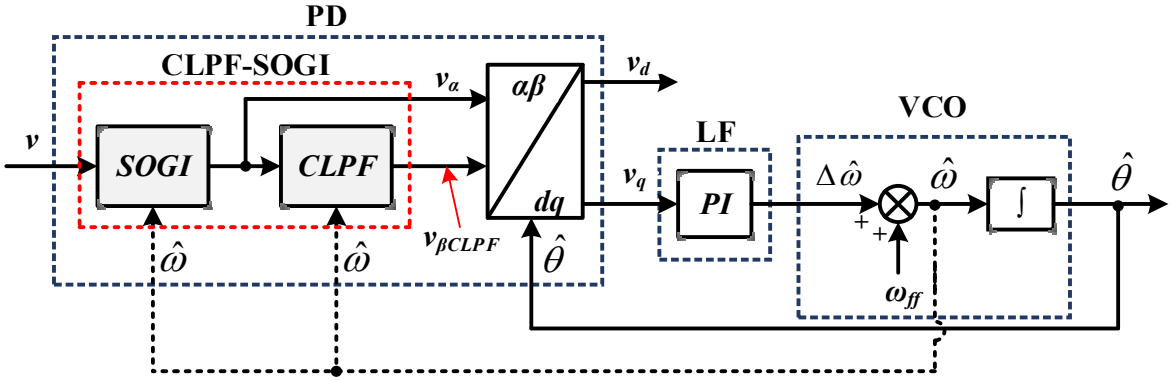


Figure 6.7. Block diagram of the proposed CLPF-SOGI based PLL in the *s* domain

6.11.1 Discretization of the conventional SOGI

As presented earlier in Chapters 3 and 4, the SOGI proved to be a very promising candidate for providing the orthogonal voltage system to an embedded SRF-PLL. However, its discrete implementation needs special attention. Various methods can be used to discretize the continuous time system, such as backward Euler, forward Euler and Trapezoidal (Tustin) [141]. Due to its simplicity and reduced computational requirements when implemented digitally, Euler's method is considered to be the most preferred method to obtain a discrete-time integrator [97, 141]. For the Euler Forward method, *s* is approximated by $= \frac{1-z^{-1}}{T_s z^{-1}}$, while for the Backward Euler method, *s* is approximated by $s = \frac{1-z^{-1}}{T_s}$, where T_s is the sample period. Consequently, the conventional OSG-SOGI structure presented earlier in Figure.4.4, can be easily implemented in a discrete form using the Euler Forward method for the first integrator (whose output is v_α), and the Backward Euler method for the second integrator (whose output is v_β). This is to avoid an algebraic loop as presented in Figure 6.8. However, the discrete time integrator using the Euler method does not have an ideal phase of -90° over all the spectrum of frequencies as shown in Figure 6.9. For example, it can be clearly noticed that at a fundamental

frequency of 50 Hz, the Forward and Backward Euler methods are not able to provide an exact phase of -90°. As a result, the orthogonal signal v_β will not be exactly 90° phase shifted with respect to v_α. The solution for this concern, it is to make use of more advanced digital methods for the discrete-time integrator. Thus, Tustin's method is suggested as an alternative method since it provides more accurate results when it compared to the Euler method [97, 141].

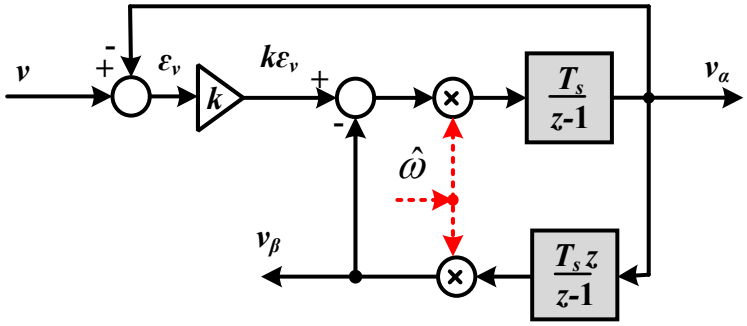


Figure 6.8. The Euler method implementation of the SOGI-OSG

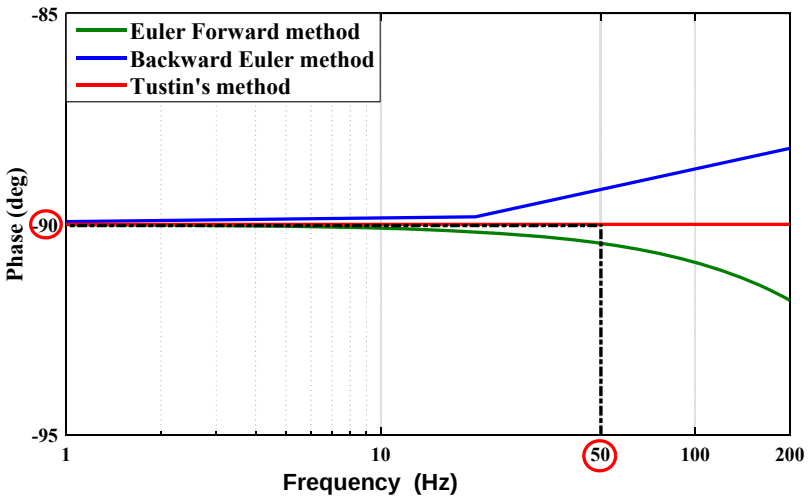


Figure 6.9. Phase Bode-plot of a discrete-time integrator using Euler-forward, Backward-Euler and Tustin's methods when T_s=50µs

The Tustin's method is basically based on the trapezoidal integration formula in which *s* can be approximated by $\frac{2}{T_s}\frac{z-1}{z+1}$ [97, 141]. As it can be noted from Figure 6.9, in comparison to the Euler methods, a phase of -90° can be guaranteed using the Tustin's method for the whole range of frequencies. However, this method cannot be applied as directly as the Euler method by just exchanging both integrators from Figure 4.4 by $\frac{2}{T_s}\frac{z-1}{z+1}$. The reason is due to algebraic loops that may be created which may pose some implementation problems. To overcome this issue, the

close-loop transfer function of (4.7) is to be discretized instead. Therefore, by substituting *s* by $\frac{2}{T_s}\frac{z-1}{z+1}$, into (4.7) the discrete transfer function can be obtained as follows

$$\begin{cases} G_\alpha(z) = \dfrac{v_\alpha}{v}(z) = \dfrac{k\hat{\omega}\dfrac{2}{T_s}\dfrac{z-1}{z+1}}{\left[\dfrac{2}{T_s}\dfrac{z-1}{z+1}\right]^2 + k\hat{\omega}\dfrac{2}{T_s}\dfrac{z-1}{z+1} + (\hat{\omega})^2} \\ G_\beta(z) = \dfrac{v_\beta}{v}(z) = \dfrac{k\omega^{\wedge 2}}{\left[\dfrac{2}{T_s}\dfrac{z-1}{z+1}\right]^2 + k\hat{\omega}\dfrac{2}{T_s}\dfrac{z-1}{z+1} + (\hat{\omega})^2} \end{cases} \quad (6.1)$$

After some rearrangements

$$\begin{cases} G_\alpha(z) = \dfrac{(2k\hat{\omega}T_s)(z^2-1)}{4(z-1)^2 + (2k\hat{\omega}T_s)(z^2-1) + (\hat{\omega}T_s)^2(z+1)^2} \\ G_\beta(z) = \dfrac{k\,(\hat{\omega}T_s)^2(z+1)^2}{4(z-1)^2 + (2k\hat{\omega}T_s)(z^2-1) + (\hat{\omega}T_s)^2(z+1)^2} \end{cases} \quad (6.2)$$

Now, by using $A = 2k\hat{\omega}T_s$ and $B = (\hat{\omega}T_s)^2$, and after some mathematical manipulation

$$\boldsymbol{G_\alpha(z) = \dfrac{\left(\dfrac{A}{A+B+4}\right) + \left(\dfrac{-A}{A+B+4}\right)z^{-2}}{1 - \left(\dfrac{2(4-B)}{A+B+4}\right)z^{-1} - \left(\dfrac{(A-B-4)}{A+B+4}\right)z^{-2}}} \quad (6.3)$$

A simple discrete form of (6.3) is obtained

$$\boldsymbol{G_\alpha(z) = b_0 . \dfrac{1 - z^{-2}}{1 - a_0 z^{-1} - a_1 z^{-2}}} \quad (6.4)$$

where:

$$b_0 = \left(\frac{A}{A+B+4}\right) \quad \& \quad a_0 = \left(\frac{2(4-B)}{A+B+4}\right) \quad \& \; a_1 = \left(\frac{(A-B-4)}{A+B+4}\right)$$

Similarly,

$$\boldsymbol{G_\beta(z) = \dfrac{\left(\dfrac{k.B}{A+B+4}\right) + 2\left(\dfrac{k.B}{A+B+4}\right)z^{-1} + \left(\dfrac{k.B}{A+B+4}\right)z^{-2}}{1 - \left(\dfrac{2(4-B)}{A+B+4}\right)z^{-1} - \left(\dfrac{(A-B-4)}{A+B+4}\right)z^{-2}}} \quad (6.5)$$

This can be simplified as

$$\boldsymbol{G_\beta(z) = b_1 . \dfrac{1 + 2.z^{-1} + z^{-2}}{1 - a_0 z^{-1} - a_1 z^{-2}}} \quad (6.6)$$

where:

$$b_1 = \left(\frac{k.B}{A+B+4}\right) = b_0\left(\frac{k.B}{A}\right) = b_0\left(\frac{\widehat{\omega}T_s}{2}\right)$$

The implementation of the Tustin's method using (6.4) and (6.6) is depicted in Figure. 6.10, in which $C = (2T_s\widehat{\omega})$.

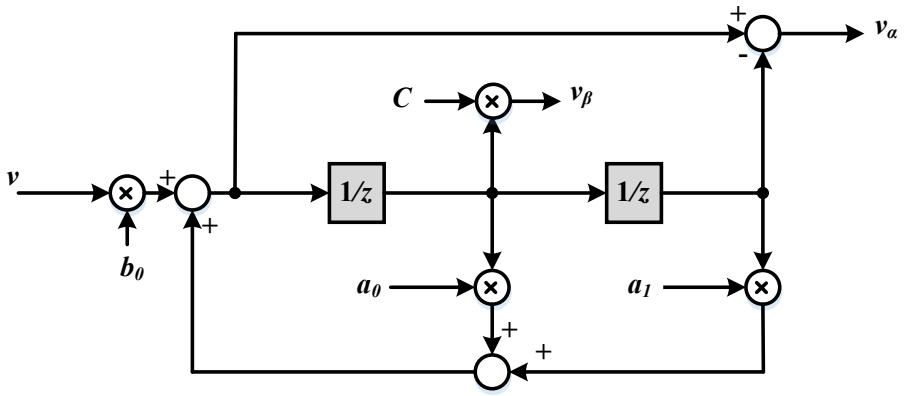


Figure 6.10. The Tustin's method implementation of the conventional OSG-SOGI

Figure.6.11 depicts the frequency response of the conventional-SOGI in both *s* and *z* domain confirming the correct choice of discretization method.

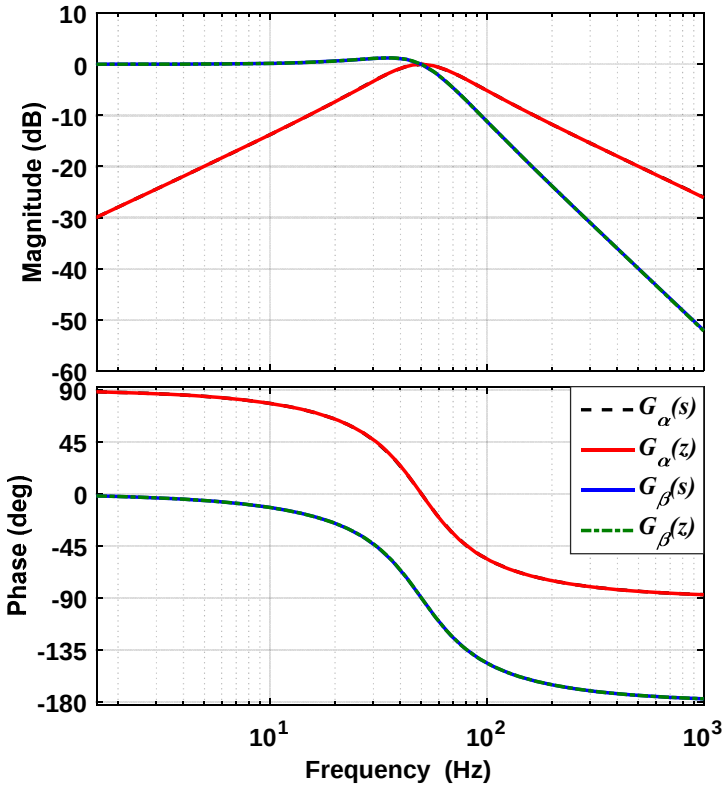


Figure 6.11. Bod-plots of (5.4) and (5.6) along with (4.7)

In order to evaluate the performance of the discrete SOGI when the two above mentioned discretization methods of Figure.6.8 and 6.10 are used, a Matlab/Simulink model as shown in Appendix C is used. The input voltage signal v is an ideal sinusoid with 50 Hz fundamental frequency and amplitude of 100V. As it can be noticed from Figure.6.12, in the case where the Euler's method of Figure.6.8 is implemented as an OSG, and due to the fact that v_β is not exactly 90° phase shifted with respect to v_α, a ripple of twice the fundamental frequency appears in the estimated quantities of the PLL (i.e., amplitude and frequency of the input signal). On the contrary to the Euler's method, the implementation the Tustin's method can provide significantly superior performance.

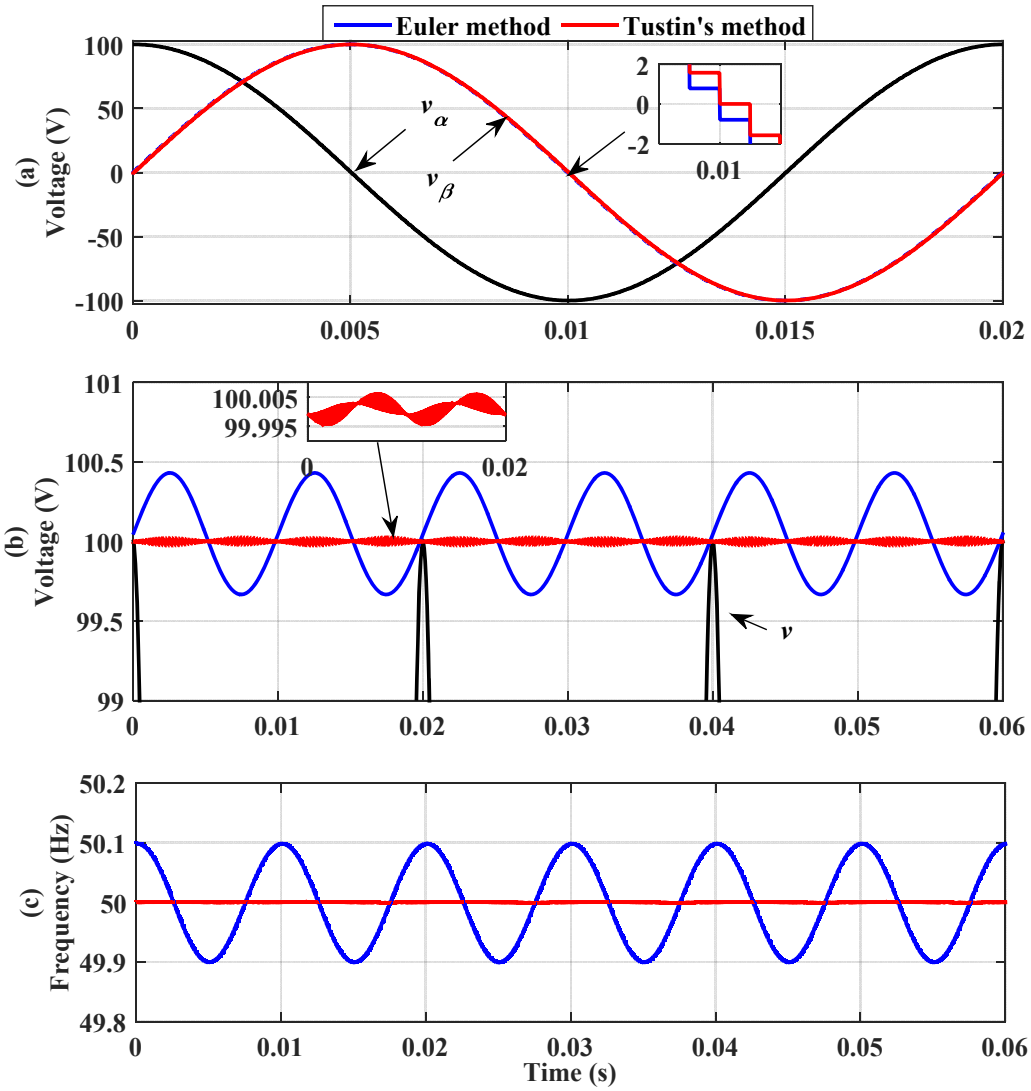


Figure 6.12. Performance comparison when the Euler and the Tustin's methods are used (a) orthogonal signals (v_α and v_β), (b) estimated amplitude and (c) estimated frequency of the input signal v.

6.11.2 Discretization of the proposed CLPF

Since the proposed CLPF-SOGI method described earlier in section 4.4.2, consists of two main blocks, a conventional SOGI which has already been discretized in 6.11.1, and a CLPF block which is responsible of generating the desired orthogonal signal $v_{\beta CLPF}$. In the following, the CLPF block which is basically composed of two cascaded LPFs will be discretized using Tustin's method owing to its increased accuracy.

Now, for simplicity let us first consider discretizing only one of the two-cascaded LPFs. In this case and based on (4.14), the desired phase lag and compensation gain of each filter will be equal to 45° and $\sqrt{2}$, respectively. Thus, the transfer function of such an LPF in the *s* domain relating the output signal y to the input signal x can be rewritten as

$$G(s) = \frac{y}{x} = \frac{\sqrt{2}}{\tau s + 1} \tag{6.7}$$

Substituting *s* by $\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$, into (6.7), the discrete transfer function can be approximated as

$$\sqrt{2}x = \tau\left(\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}\right)y + y \tag{6.8}$$

After some arrangements

$$\sqrt{2}x(1+z^{-1}) = \tau\left(\frac{2}{T_s}(1-z^{-1})\right)y + y(1+z^{-1}) \tag{6.9}$$

$$\begin{aligned}\sqrt{2}\big(x(k)+x(k-1)\big) &= \frac{2.\tau}{T_s}\big(y(k)-y(k-1)\big) + y(k) + y(k-1)\\ &= y(k)\left(\frac{T_s+2.\tau}{T_s}\right) + y(k-1)\left(\frac{T_s-2.\tau}{T_s}\right)\end{aligned} \tag{6.10}$$

Then by re-arranging (6.10) to generate an expression for the output signal $y(k)$

$$y(k) = a\big(x(k)+x(k-1)\big) - by(k-1) \tag{6.11}$$

where:

$$a = \left(\frac{\sqrt{2}.T_s}{T_s+2.\tau}\right) \quad \& \quad b = \left(\frac{T_s-2.\tau}{T_s+2.\tau}\right) \quad \& \quad \tau = 1/\widehat{\omega}$$

The implementation of the Tustin's method for the CLPF using (6.11) is depicted in Figure. 6.13.

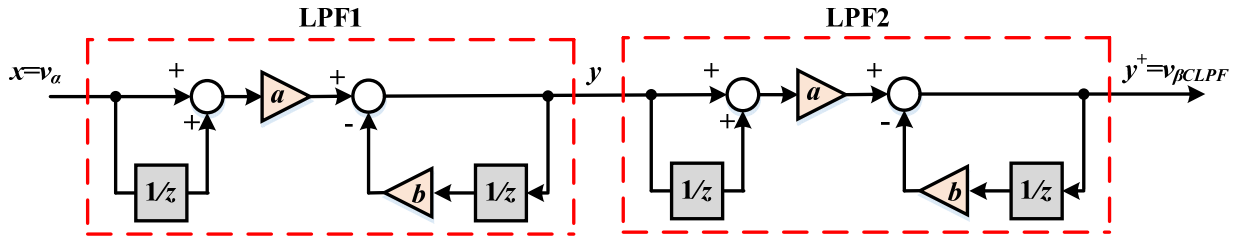


Figure 6.13. The Tustin's method implementation of the CLPF

While the complete diagram of the proposed discretized CLPF-SOGI can be illustrated in Figure.6.14

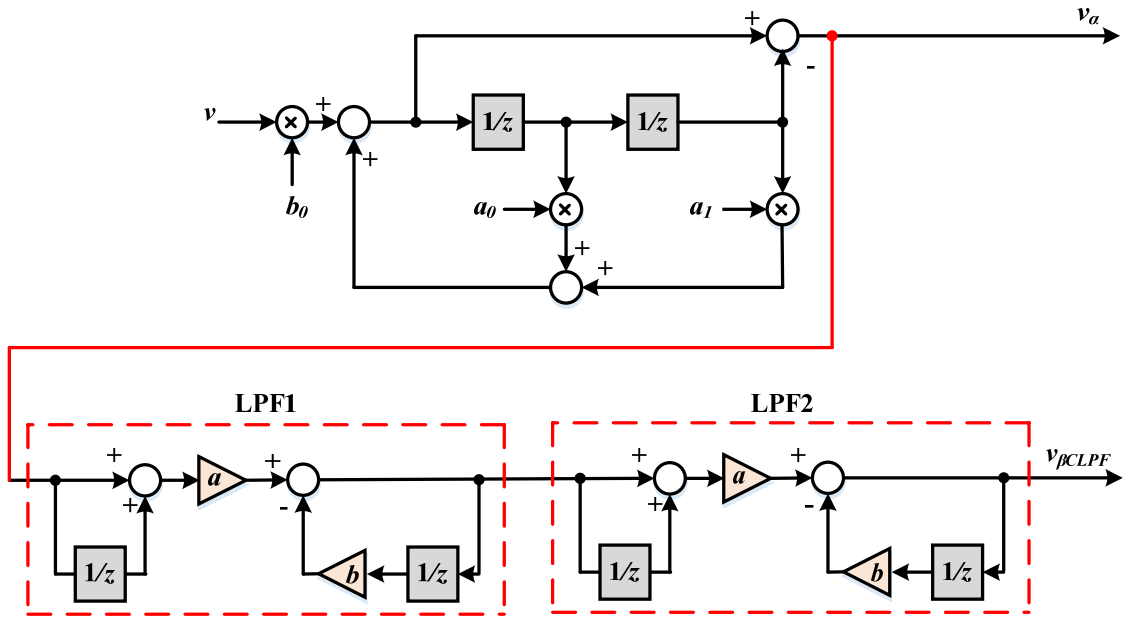


Figure 6.14. The Tustin's method implementation of the proposed CLPF-SOGI

6.11.3 Discretization of the loop filter (LF)

It has been pointed out earlier that, the loop filter (LF) is equivalent to a PI-controller. Typically this PI-controller is used to attenuate the noise and high-frequency components from the PD output (v_q) and to provide a DC-controlled signal component ($\Delta\hat{\omega}$) for the VCO. A block diagram of a typical PI-controller in the continuous domain is shown in Figure. 6.15, where v_q is the PD output signal that needs to be filtered out, and $\Delta\hat{\omega}$ is the output control signal which is to be added to the fundamental frequency ω_{ff} before being fed into the voltage-controlled

oscillator (VCO). The relationship between the input signal v_q and output signal $\Delta\hat{\omega}$ of the PI-controller presented in Figure.6.15, can be derived as following

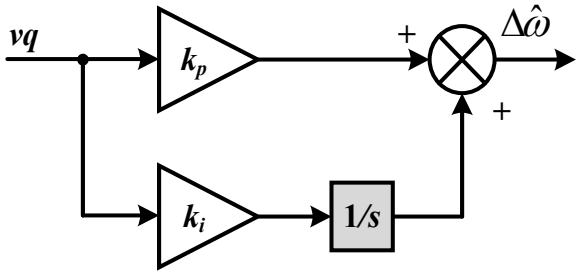


Figure 6.15. Block diagram of a PI controller in the *s* domain

$$G_{PI}(s) = \frac{\Delta\hat{\omega}}{v_q} = k_p + \frac{k_i}{s} \tag{6.12}$$

For simplicity, the Euler backward method is used to discretize the PI-controller. By substituting the term *s* in 6.12 by the term $\frac{z-1}{zT_s}$, the PI-controller discrete transfer function can be approximated as

$$G_{PI}(z) = \frac{\Delta\hat{\omega}}{v_q} = k_p + k_i T_s \frac{z}{z-1} \tag{6.13}$$

$$\Delta\hat{\omega}(k) = \underbrace{k_p . v_q(k)}_{\Delta_p(k)} + \underbrace{k_i T_s \frac{z}{z-1} v_q(k)}_{\Delta_i(k)} \tag{6.14}$$

The integral term $\Delta_i(k)$ can be simplified as

$$\begin{aligned} \Delta_i(k) &= k_i T_s \frac{1}{1-z^{-1}} v_q(k) \\ (1-z^{-1})\Delta_i(k) &= k_i T_s v_q(k) \\ \Delta_i(k) - z^{-1}\Delta_i(k) &= k_i T_s v_q(k) \\ \Delta_i(k) &= k_i T_s v_q(k) + z^{-1}\Delta_i(k) \end{aligned} \tag{6.15}$$

Based on (6.14) and (6.15), the difference equations of the PI-controller suitable for implementation in the microcontroller can be rewritten as

$$\begin{cases} \Delta_p(k) = k_p.v_q(k) \\ \Delta_i(k) = k_i T_s v_q(k) + z^{-1}\Delta_i(k) \\ \Delta\hat{\omega}(k) = \Delta_p(k) + \Delta_i(k) \end{cases} \quad (6.16)$$

The block diagram of the digital PI-controller is depicted in Figure. 6.16.

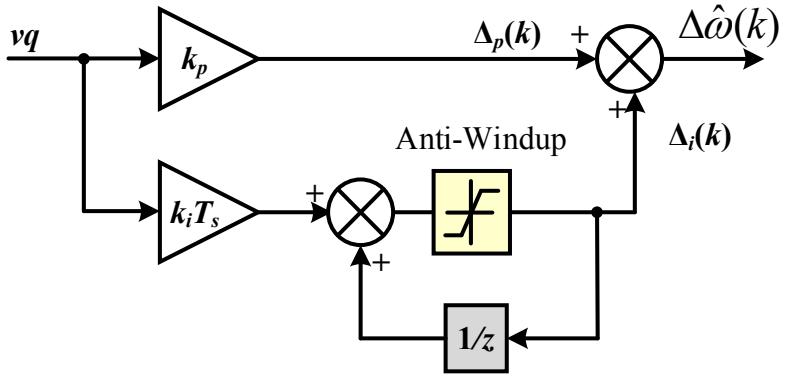


Figure 6.16. Digital implementation of the PI controller used for the PLL

It is worth it remarking that, in order to prevent integral windup, the integral term is clamped by a saturation block (Anti-Windup).

6.11.4 Discretization of the voltage-controlled oscillator (VCO)

The voltage-controlled oscillator (VCO) uses the sum of the PI-controller output signal ($\Delta\hat{\omega}$) and the feedforward fundamental frequency ω_{ff}, to synthesise a sinusoid with the phase and frequency to that of the input signal. A simple block diagram of the VCO in the *s* domain is shown in Figure. 6.17.

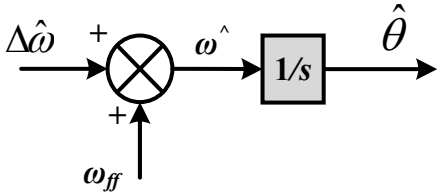


Figure 6.17. Block diagram of the VCO in the s domain

By applying Z-transformation using Tustin's method, the following difference equation is derived:

$$G_{VCO}(s) = \frac{\hat{\theta}}{\hat{\omega}} = \frac{1}{s} \rightarrow G_{VCO}(z) = \frac{T_s}{2}\frac{1+z^{-1}}{1-z^{-1}} \tag{6.17}$$

$$\begin{aligned} \hat{\theta}(k)(1-z^{-1}) &= \frac{T_s}{2}\hat{\omega}(k)(1+z^{-1}) \\ \hat{\theta}(k) &= \frac{T_s}{2}\left(\hat{\omega}(k) + z^{-1}\hat{\omega}(k)\right) + \hat{\theta}(k)z^{-1} \end{aligned} \tag{6.18}$$

The block diagram of the digital implementation of the VCO is depicted in Figure. 6.18.

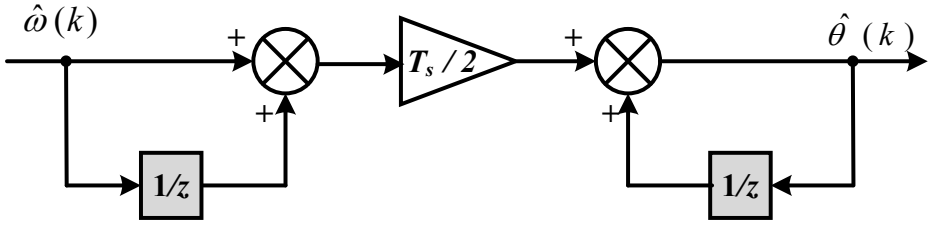


Figure 6.18. Digital implementation of the VCO

6.12 The implementation of *dq* Current Controller

As proposed in Chapter 5, in this thesis a *dq* current control algorithm is chosen for implementation on the DSP system to control the current of the grid-connected PV inverter system. This choice is made primarily because the implementation of a *dq* current controller can lead to zero steady-state error when compared with the stationary reference frame PI-controller. As it can be seen from Figure.6.19, two simple PI-controllers along with the voltage feed-forward and coupling terms are involved in the controlling process. The resulting control signals (v_{inv}^{d} and v_{inv}^{q}), are then transformed back to the stationary reference-frame to obtain the corresponding AC control signal (v_{inv}^{α}). The modulation index is then calculated by dividing the required converter terminal voltage (v_{inv}^{α}) by the half of dc link voltage, $V_{dc}/2$. To prevent integral windup and unnecessary PWM over-modulation, the integral term and overall output control signals are limited by the saturation blocks Anti-Windup and PWM Limit, respectively. The *dq* current controller is fine-tuned via the proportional and integral gain parameters as proposed in Section 5.4.2, to achieve the best output current fidelity as possible. Both identical PI-controllers are discretized and implemented in software on the Texas Instrument TMF28335 processor. The discretization of the PI-control algorithm is the same as that of the PI-controller used in conjunction with the PLL which is discretised using the Euler Backward as in Sub-section 6.11.3. A block diagram of the digital implementation of PI-controllers is illustrated in Figure. 6.20.

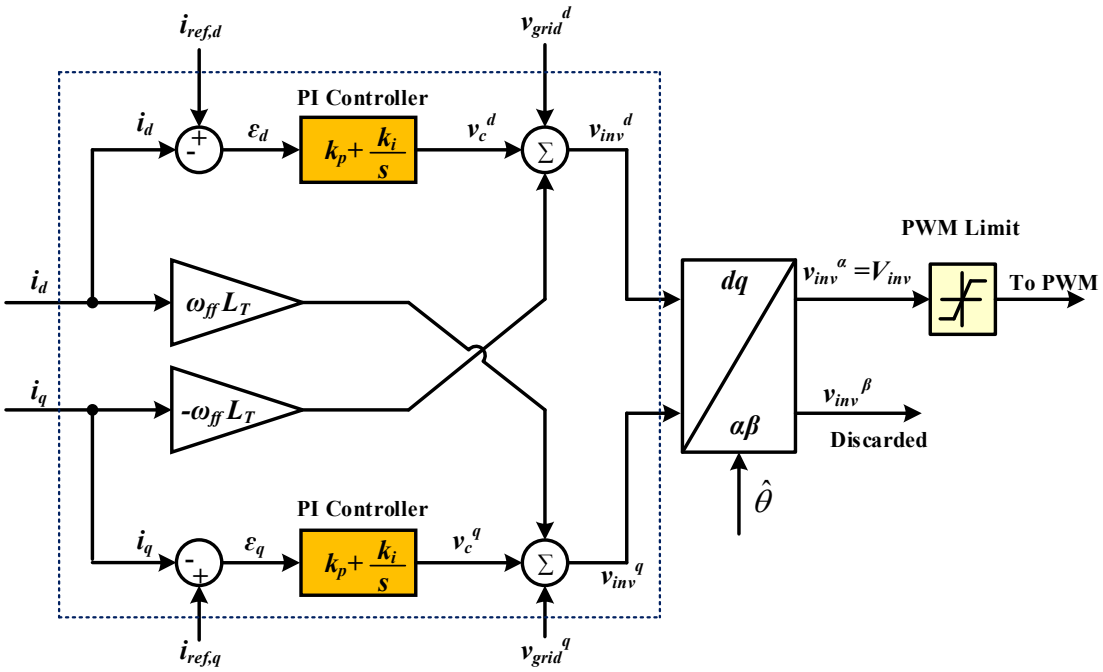


Figure 6.19. Block diagram of *dq* current controller in the *s* domain.

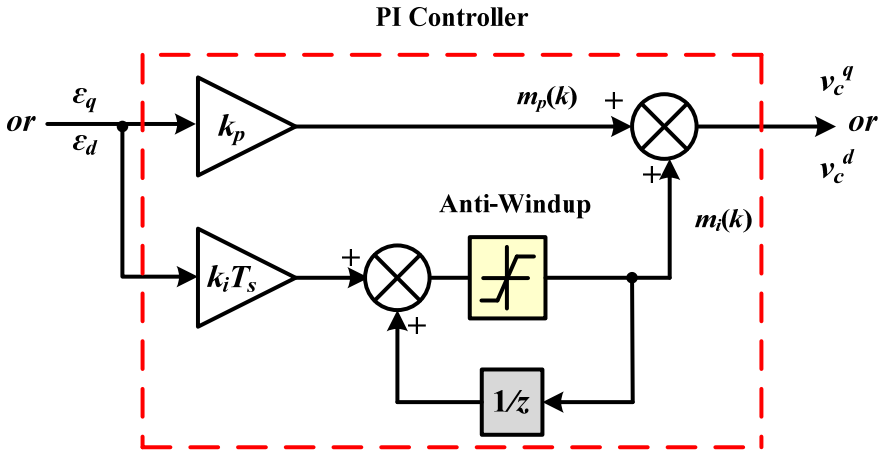


Figure 6.20. Digital implementation of the PI controller used for the *dq* current control algorithm

6.13 Pulse width modulation (PWM) set-up

The in-phase disposition (IDP) PWM scheme described in Chapter 1 is implemented in the practical experiments. In these experiments, the PWM has been set-up to produce a carrier frequency of 20 kHz. The timing of the PWM hardware is derived from the 150MHz processor clock (SYSCLKOUT). This setting results in a modulation index range of 0-3750.

Figure. 6.21 shows the basic logic for the switching of the five-level inverter. Further details on how the PWM set-up for the five-level inverter can be found in Appendix A.

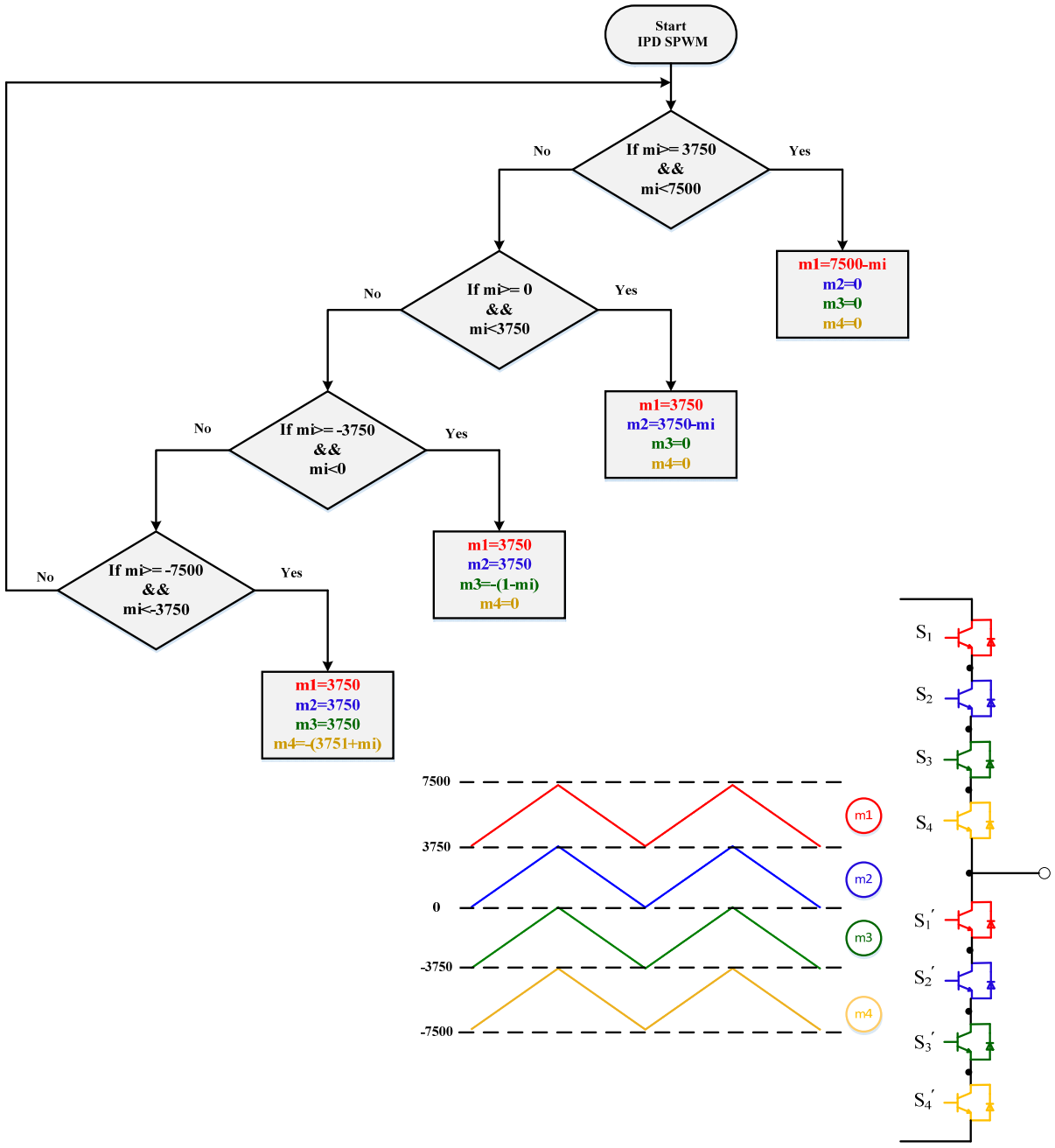


Figure 6.21. The switching logic for the five-level inverter

6.14 Grid Connection Sequence

Connection to the utility grid is made through the following procedure in conjunction with Figures. 6.1 and 6.2.

1) Initially set the DC power supplies and the variac to zero volts. In this way, no voltage is applied to the DC link of the inverter, and zero network voltage appears at the LCL filter system output.
2) The microcontroller operation is started, which creates PWM signals to control the switches and to synchronise the inverter output current to the grid voltage.
3) The grid-side switch is switched ON so that PLL is connected to the mains supply which always has a strong signal regardless of the variac setting. At this point, the variac output voltage is kept at zero volts.
4) Switch ON the DC power supplies, so that a DC link voltage is established at the LCL filter input. The current demand of the inverter is set to the desired level.
5) The current controller is set up to provide a sinusoidal current into the short circuit.
6) The variac output is now gradually increased whilst monitoring the measured current which should stay constant and track its demand. As a result, the effective PCC voltage at the inverter output increases. The modulation index should increase as the inverter current controller attempts to counteract the applied PCC voltage.
7) The PCC voltage seen at the LCL filter output is steadily increased by the variac until it reaches the rated output voltage for the DC link voltage of the inverter. With 280V DC link voltage, a distribution grid voltage of 100 V may be applied to the LCL filter system output.
8) The current demand of the inverter current controller can now be set to the full current demand of the inverter system. The controller will now be working in order to inject controllable current into the distribution grid. At this point, the inverter is now performing fully as a grid connected inverter system, under full rated conditions.

6.15 Summary

In this chapter, a description of the experimental test rig used to examine the performance of the proposed CLPF-SOGI-PLL technique and the *dq* current control scheme has been provided. Also, an overview of the control unit which is based on an eZdsp F28335 board has been presented, detailing the key features of the purpose power interface power.
In the forthcoming chapters, the performance of the proposed control methods implemented on this test rig will be presented.

CHAPTER 7

Performance Evaluation of The CLPF-SOGI based PLL

7.1 Introduction

This chapter presents the experimental results for the CLPF-SOGI-PLL system described in Chapter 4 and implemented in Chapter 6. The chapter is split into two main sections. Initially, the steady-state performance of the CLPF-SOGI is investigated with particular interest in the dc offset rejection and harmonic attenuation capability. To highlight the effectiveness of the proposed method, its harmonic profile results are compared with those of the conventional SOGI and two other alternative dc rejection methods described in Chapter 4. The second section, considers the dynamic performance of the proposed scheme in comparison with the conventional SOGI PLL under several grid disturbance tests.

In the following set of experimental verifications, the desired input grid voltage signal v is generated internally within the code in the DSP. It is then sent to the 12-bit external digital-to-analogue converter (DAC) of the power interface board through the serial peripheral interface (SPI) to generate the analogue test signal. Subsequently, this input signal is then acquired by the DSP to accomplish the required PLL algorithm. With these arrangements, disturbances consisting different grid abnormalities can be easily simulated. Furthermore, the real instantaneous phase angle (θ) of the generated grid signal can be created internally to compare with the estimated phase angle ($\hat{\theta}$) so that phase error can be determined. With this provision, relative performance examination of algorithm is possible. The selected estimated quantities such as amplitude, frequency, and phase-angle are also sent to DAC to be observed by an oscilloscope in real-time. In addition, to control the DSP in real-time operation, LabVIEW™ software package is used to communicate with the DSP, as well as to implement a Graphical User Interface (GUI). This is achieved via an RS232 serial interface between the DSP and the host computer. This GUI is programmed to update the required reference disturbance (i.e., grid amplitude, frequency, dc offset and so on) and to generate and transfer such a disturbance at a

certain time to the DSP. Simultaneously, it also reads and presents important quantities within the DSP on the screen for the user in order to save it as a real date to be plotted later. The results obtained were for a sampling frequency of 20 kHz.

Although the operation of the CLPF-SOGI-PLL system will be tested for artificially grid events generated within the DSP, the intended mode of operation is to a real grid. To demonstrate this, a 240V single phase 50Hz real grid signal with 0.6% dc offset and a THD of 2.93% will be also fed into the PLL algorithms implemented on the DSP board to test their performance under the real grid signal.

7.2 Steady-state Performance Evaluation

In this section, the performance of the proposed CLPF-SOGI scheme in comparison with the other techniques that have been discussed in Chapter 4 is evaluated throught a real-time experimantal setup described in Chapter 6. This is to verify the effectievenes of the proposed techique with a particular interest in the dc offset rejection and harmonic attenuation capability. Therefore, a previous simulation test described in section 4.5, with the same specified parameters of Table 4-1 and 4-3, is experimentally carried out here to verify the validity of the proposed technique. As can be seen from Figure 7.1, the input voltage signal v is highly polluted by 15% of the third, and 10% of the fifth harmonic, together with a 20% dc offset, leading to a total harmonic distortion (THD) of approximately 18.13%

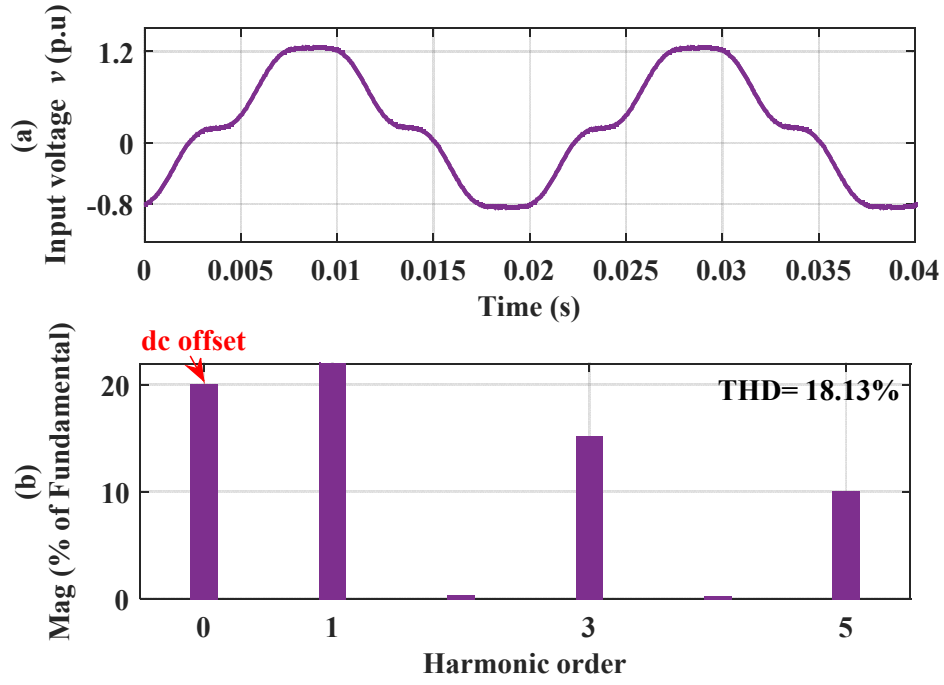


Figure 7.1. Experimental results of; (a) distorted input voltage waveform v and (b) its harmonic spectrum

The orthogonal output waveform v_β and its harmonic content when the input signal v is fed into the conventional SOGI-OSG are illustrated in Figure. 7.2. Visibly, the orthogonal signal v_β is highly affected by the presence of the dc offset in the input signal. The amplitude of this offset is equal to the gain k times that of the input dc component in the input signal v (i.e., 1×0.2=0.2p.u). This is due to the low-pass behaviour of $G_\beta(s)$ derived in (4.7) for the conventional SOGI-OSG. Note that $k = 2\xi$, is the SOGI damping factor.

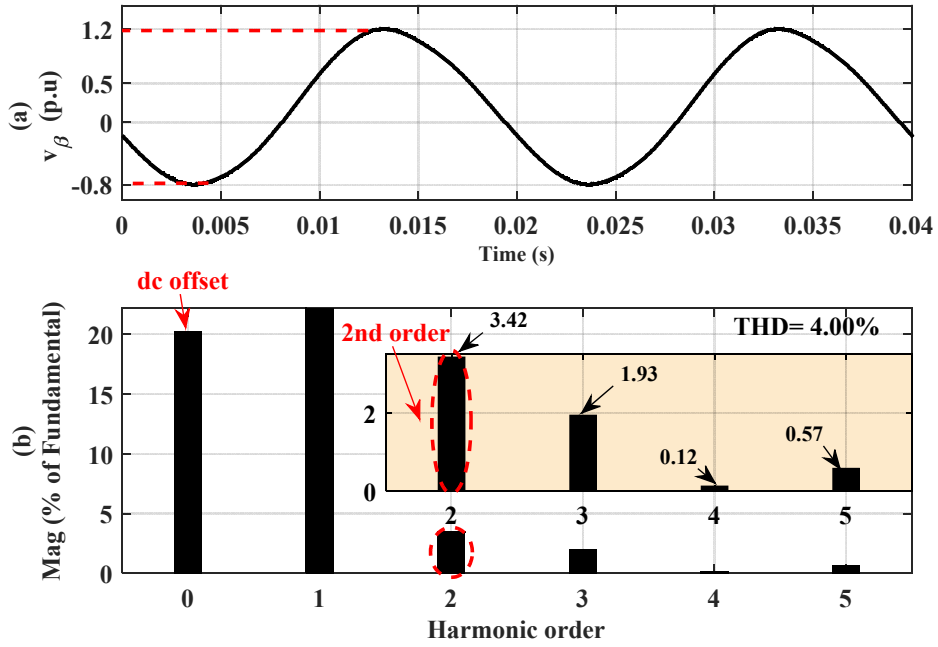


Figure 7.2. Results obtained with the conventional SOGI (a) orthogonal signal (b) its harmonic spectrum

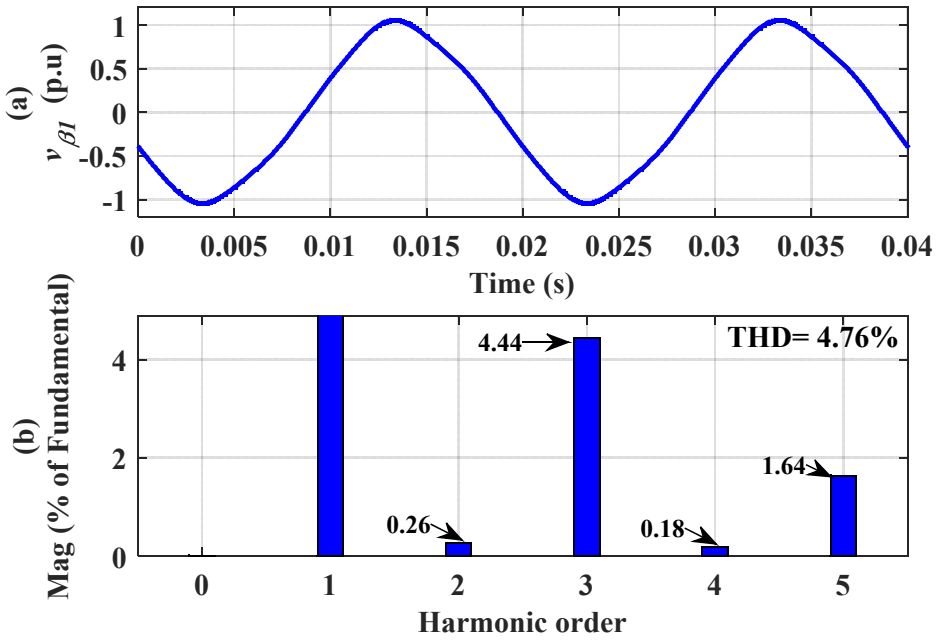


Figure 7.3. Results obtained with the first method of [113] (a) orthogonal signal (b) its harmonic spectrum

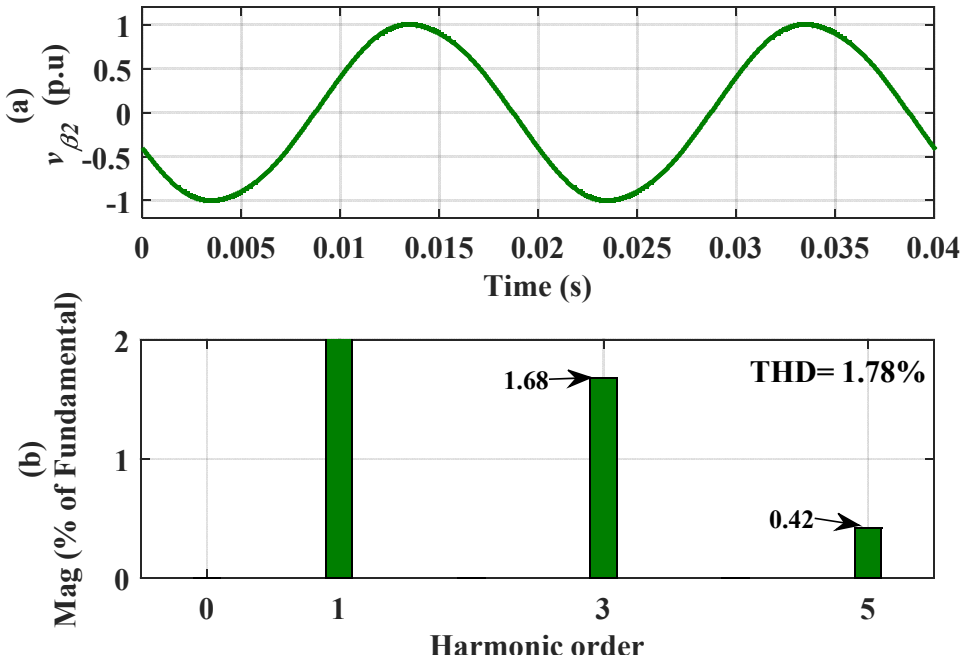


Figure 7.4. Results obtained with the second method of [114] (a) orthogonal signal (b) its harmonic spectrum

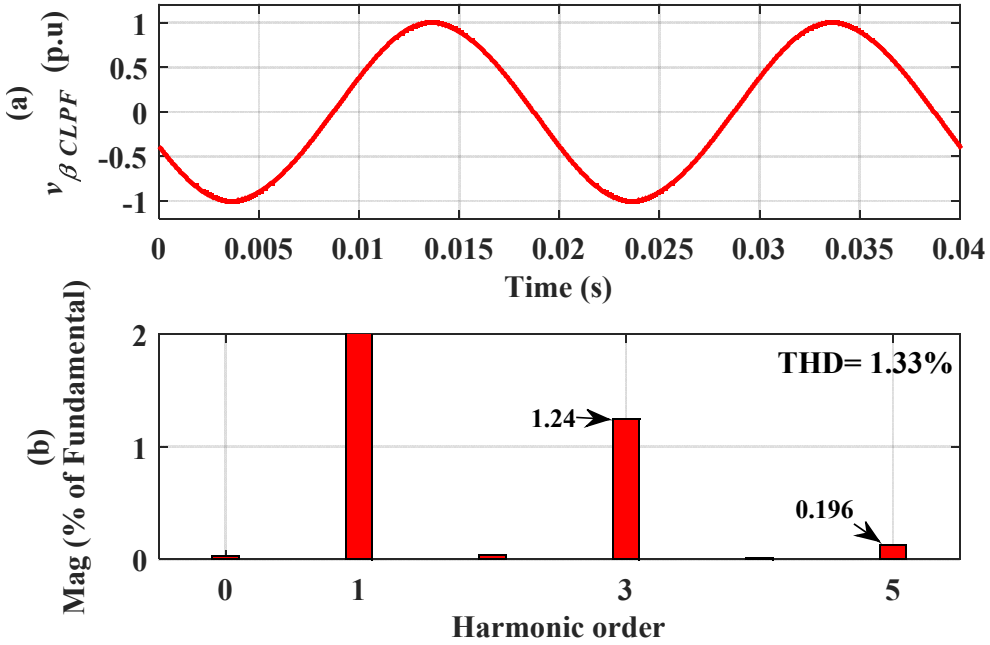


Figure 7.5. Results obtained with the proposed CLPF-SOGI (a) orthogonal signal (b) its harmonic spectrum

In comparison, Figure.7.3 shows results obtained from using the first method of [113] , where it is clear that the dc offset has been fully removed in the orthogonal signal $v_{\beta 1}$, however, as

pointed out earlier in Figure. 4.21, the output waveform of $v_{\beta 1}$ becomes clearly distorted due to the poor attenuation characteristics of this method at frequencies higher than the centre frequency $\hat{\omega}$. Figure.7.4 then shows the orthogonal signal $v_{\beta 2}$ and its harmonic profile when the second alternative method of [114] is used as an OSG. The dc offset is effectively rejected due to the band-pass filtering characteristics of $G_{\beta 2}(s)$ derived in (4.20). Again, the performance of this method at frequencies higher than the centre frequency is comparable with the conventional SOGI performance. Finally, Figure. 7.5 shows results gained from adopting the proposed CLPF-SOGI-OSG; where the smoothest orthogonal waveform among the four methods can be clearly observed. Additionally, the dc-offset in $v_{\beta CLPF}$ is completely suppressed.

The harmonic profile for the four methods experimentally examined in this section is gathered together in Figure. 7.6. It is obvious that the first alternative method of [113] is more susceptible to errors caused by high-frequency harmonics than the other three methods. In addition, since the conventional SOGI and the second alternative method of [114] offer a transfer functions with similar decay rate at high-frequencies, they present almost similar performance. On the other hand, the proposed CLPF-SOGI shows a superior harmonic attenuation characteristic when compared with the other methods.

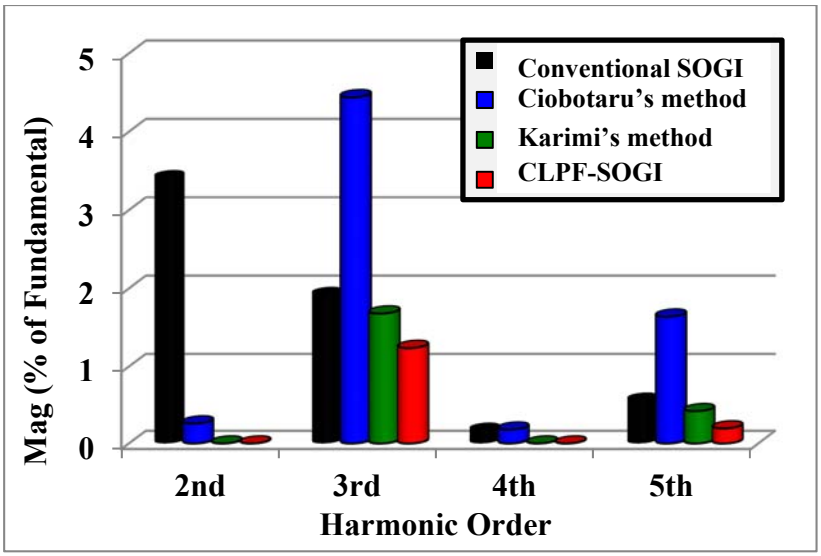


Figure 7.6. Experimental harmonic spectrum of the orthogonal signal generated using four different methods

Finally, the analytical, numerical and experimental results of the orthogonal signal's harmonic spectrum that have been obtained using Bode-plots of Table 4-2, simulation as shown in

Figure.4.27, and DSP as depicted in Figure. 7.6 respectively are shown in Figure. 7.7 for comparison.

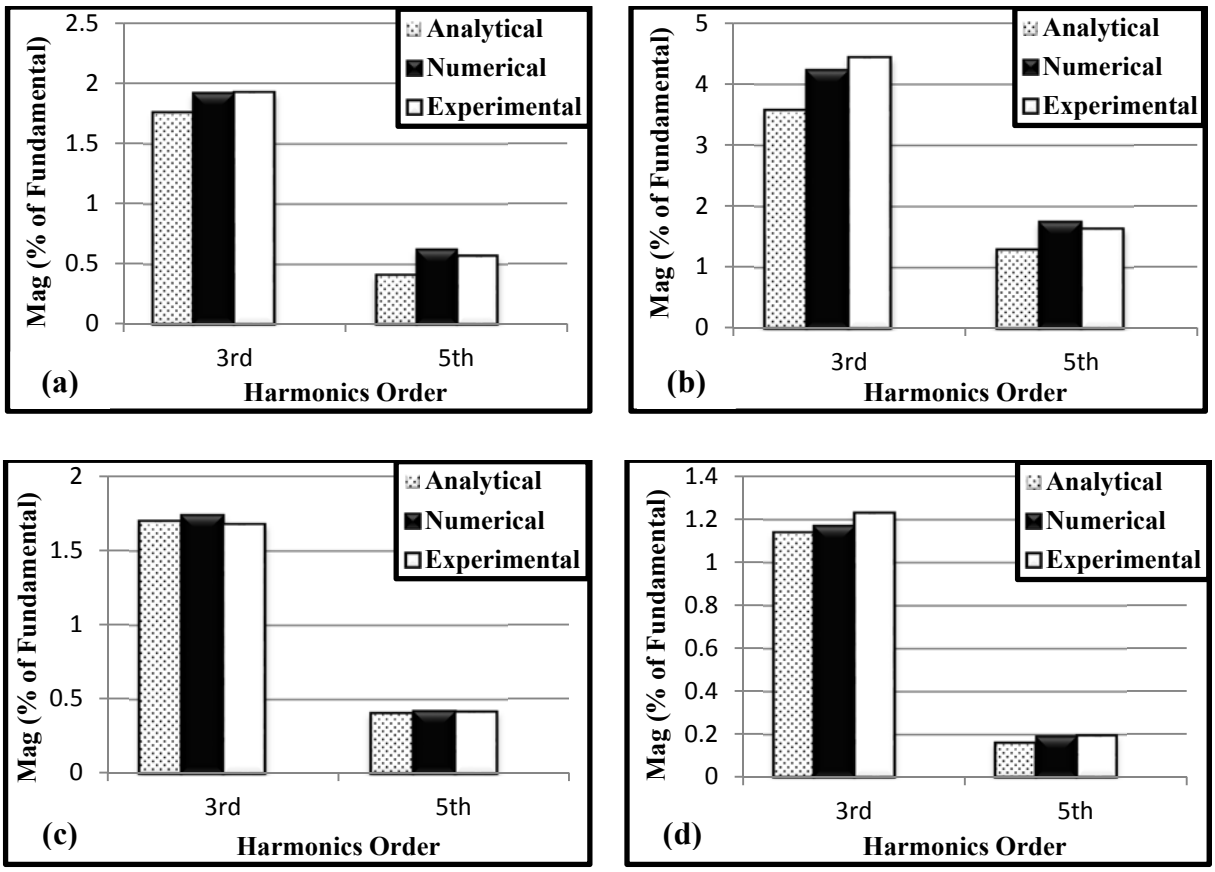


Figure 7.7. Analytical, numerical and experimental harmonics of (a) the conventional SOGI, (b) the first method, (c) the second method, and (d) the proposed CLPF-SOGI

Note that, there is a good agreement between the analytical, numerical and experimental results for all methods, which verifies the validity of the proposed PLL scheme.

To further support the effectiveness of the proposed CLPF-SOGI-PLL, an additional set of experimental results is included. Figure.7.8 shows the input signal v and the estimated synchronizing signal ($S = cos\,\hat{\theta}$), when the conventional SOGI-PLL is used. The presence of the dc component in the input signal v, causes distortion in the estimated synchronizing signal component S, which appears as a second-order harmonic as shown in Figure. 7.8. Since this signal will be essential for the current control algorithm, therefore, it will definitely have a major effect on the quality of the injected current into the grid as will be investigated later. On the other hand, the proposed CLPF-SOGI incorporates the dc component in its modelling and, thus, fully eliminates the distortion from the estimated synchronisation signal as shown in Figure. 7.9. This of course will add a great advantage to the current control algorithm since its

reference current will be free of any dc components. Also, the total harmonic distortion of the synchronization signal will be perfectly improved when compared to the conventional SOGI.

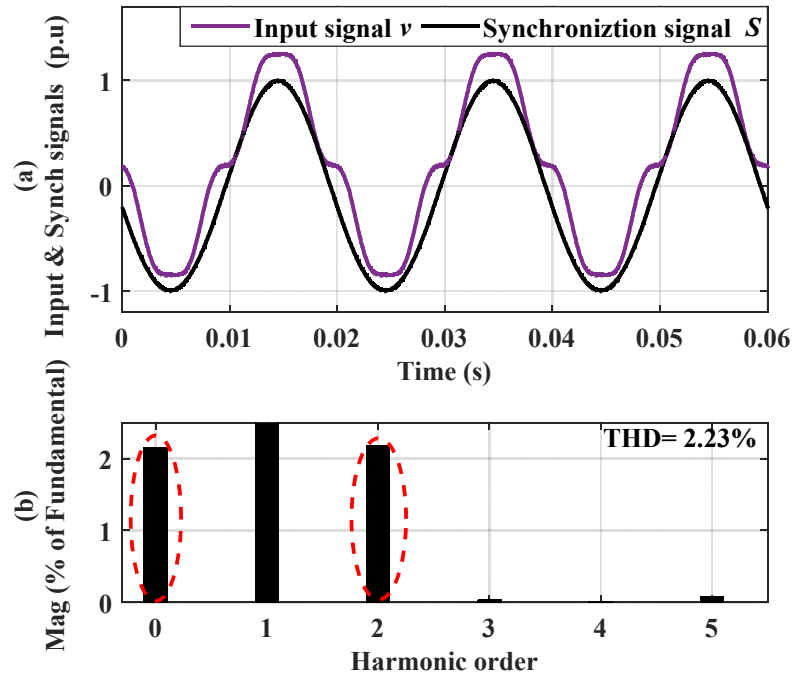


Figure 7.8. Performance of the conventional SOGI in estimating the synchronisation signal: (a) input signal and estimated signal, (b) harmonic content of the estimated synchronization signal

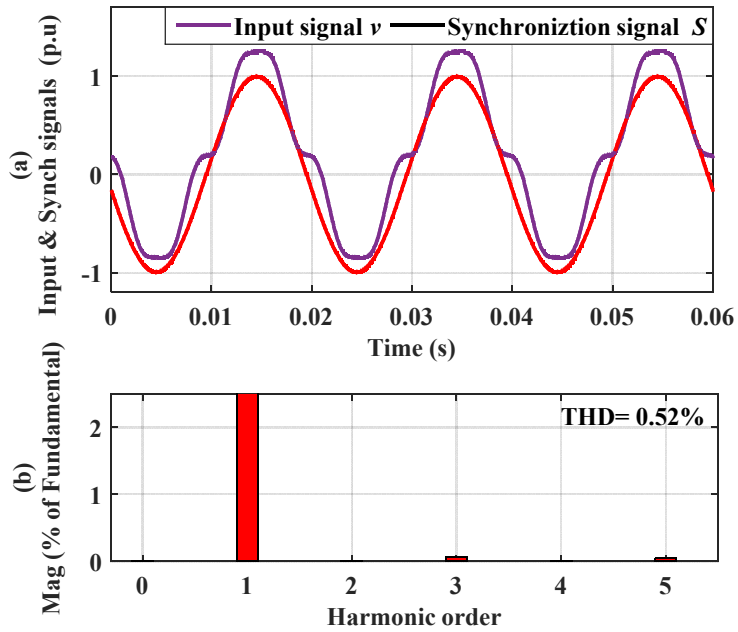
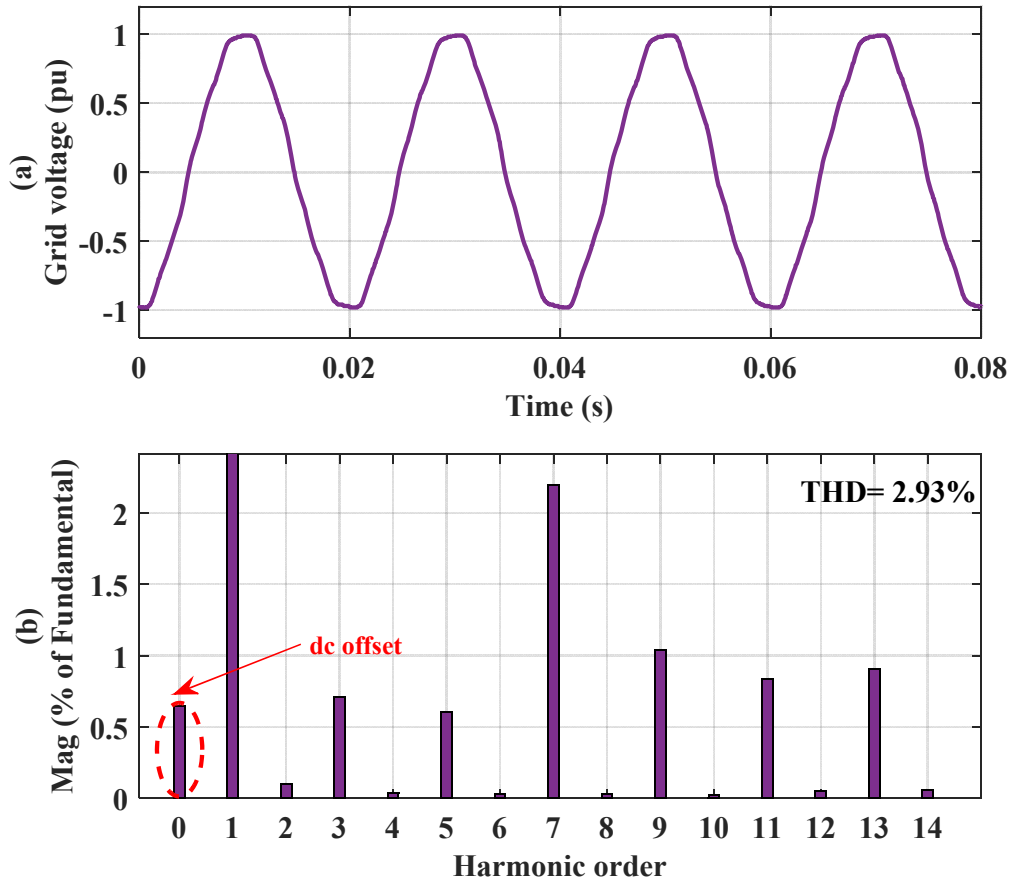


Figure 7.9. Performance of the proposed CLPF-SOGI in estimating the synchronisation signal: (a) input signal and estimated signal, (b) harmonic content of the estimated synchronization signal

Furthermore, instead of v is being generated internally, the real grid voltage signal with THD of 2.93% is acquired by means of voltage sensor and analogue-to-digital converter (DAC) of

the power interface board. This signal is then fed into the PLL algorithms implemented on the DSP board to test the performance of both PLLs with the real grid signal.

It can be observed from the obtained results of Figure. 7.10 that, the estimated quantities by the CLPF-SOGI PLL have much lower ripple that those obtained by the conventional SOGI PLL. For example, oscillations with ripple of 0.03 p.u in the estimated grid amplitude, and 0.87 Hz in the frequency are recorded with the conventional SOGI PLL, while the obtained ripples when the CLPF-SOGI PLL is employed are 0.016 p.u and 0.54Hz for the estimated voltage amplitude and frequency respectively. The main cause of the relatevily high ripple is due to the presence of dc offset in the measured grid voltage signal for which the conventional SOGI is unable to reject.



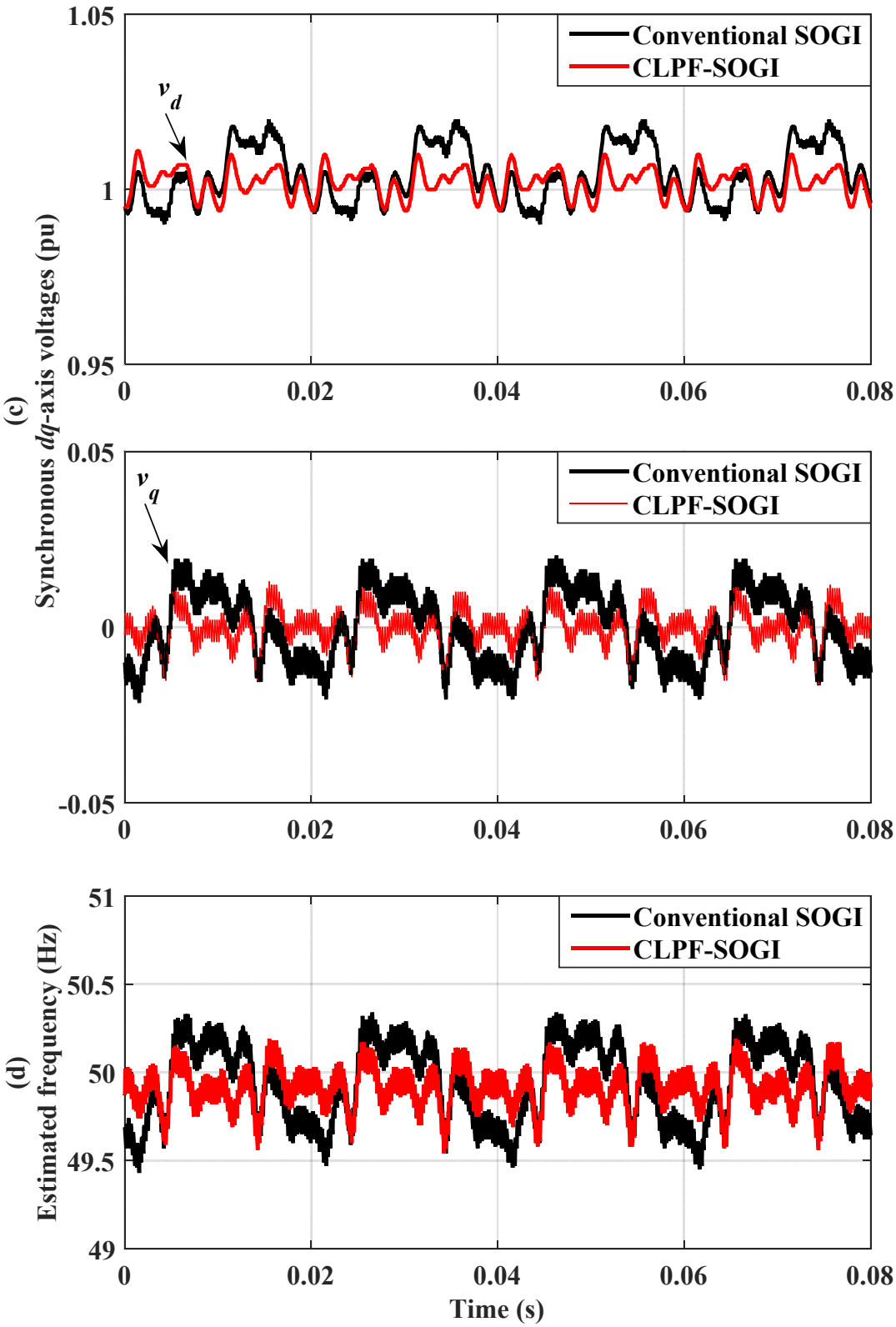


Figure 7.10. Performance of conventional SOGI-PLL and CLPF-SOGI with the real grid voltage signal: (a) Input grid voltage, (b) harmonic spectrum of the grid voltage, (c) signals in the synchronous reference frame, and (d) estimated frequency.

7.3 Dynamic Performance Evaluation under Individual Disturbance Test Cases

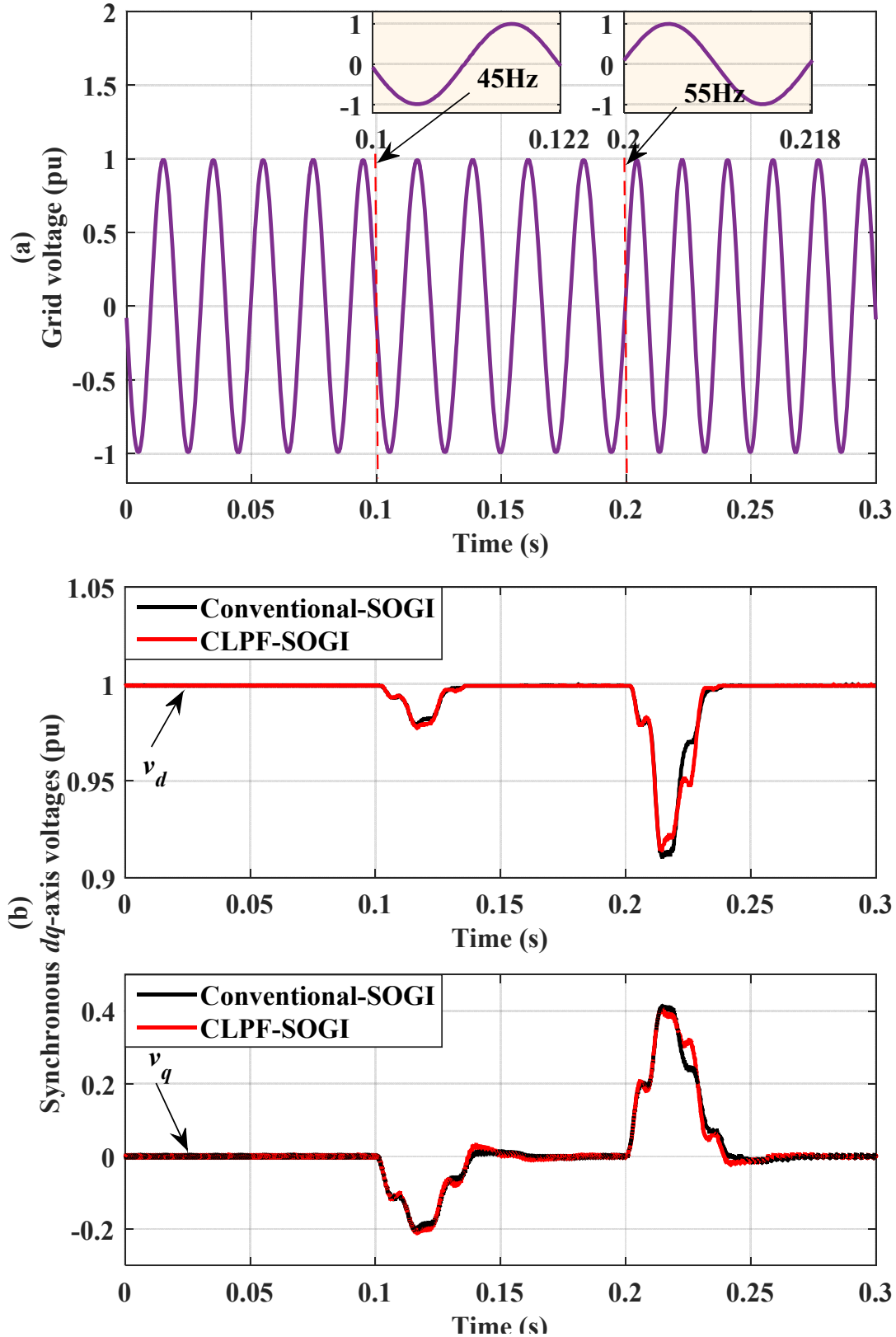
In this group of test cases, the performance of the proposed CLPF-SOGI-PLL algorithm is experimentally implemented and assessed under different individual grid disturbances. To highlight the effectiveness of the proposed CLPF-SOGI-PLL, the conventional SOGI-PLL is also implemented, and its results are compared with those of the proposed technique. The considered parameters for both PLLs used in these test cases are shown in Table 7-1. Six different test cases are considered, with grid disturbances occurring at t=0.1s.

Table 7-1 SOGI-PLL and CLPF-SOGI PLL parameters

Parameter	Symbol	Value (unit)
SOGI-OSG gain	k	2
Crossover frequency	ω_c	135.86 rad/s
PLL damping factor	ξ	0.7
Phase margin	PM	44.8°
PLL Proportional gain	k_p	135.86
PLL Integral gain	k_i	7690
Settling time	t_s	0.045s
Nominal frequency	ω	2.π.50 rad/s
Input voltage amplitude	V_m	1 p.u
CLPF time constant	τ	(1/ ω^)s
Sampling frequency	f_s	20kHz

7.3.1 Performance Comparison under Frequency Variation

To mainly test the frequency adaptive nature of the proposed algorithm, Figure.7.11 shows the experimental results when the input signal's frequency varies between 45 and 55 Hz. It can be observed from Figure. 7.11 that, with the same PLL control gains, the CLPF-SOGI-PLL has nearly the same dynamic performance, but with rather faster transient response in comparison to the conventional SOGI-PLL (i.e., the 2% settelling time is around 37.5 and 39.1ms for CLPF-SOGI and conventional SOGI-PLL respectively). It should be highlighted that, in the case where small changes in the grid frequency are expected, the steady-state performance of both PLLs can be improved by narrwoing the bandwidth of the PLL. This will have another advantage of avoiding the issue of large frequency transient that is usually experienced during phase jumps, but at the expense of slower dynamic response in PLL system.


(a)
Grid voltage (pu)
45Hz
55Hz
0.1
0.122
0.2
0.218
Time (s)
(b)
Synchronous dq-axis voltages (pu)
Conventional-SOGI
CLPF-SOGI
v_d
v_q
Time (s)

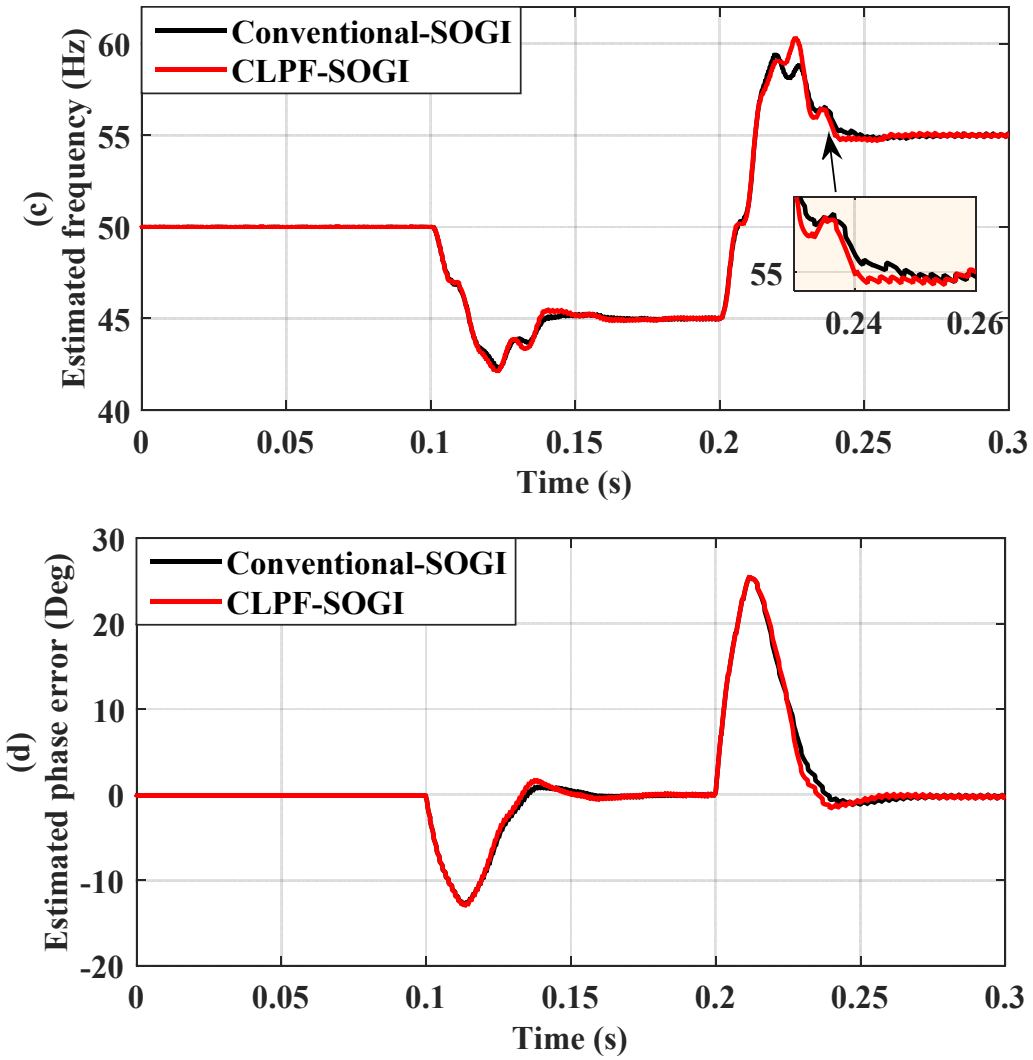
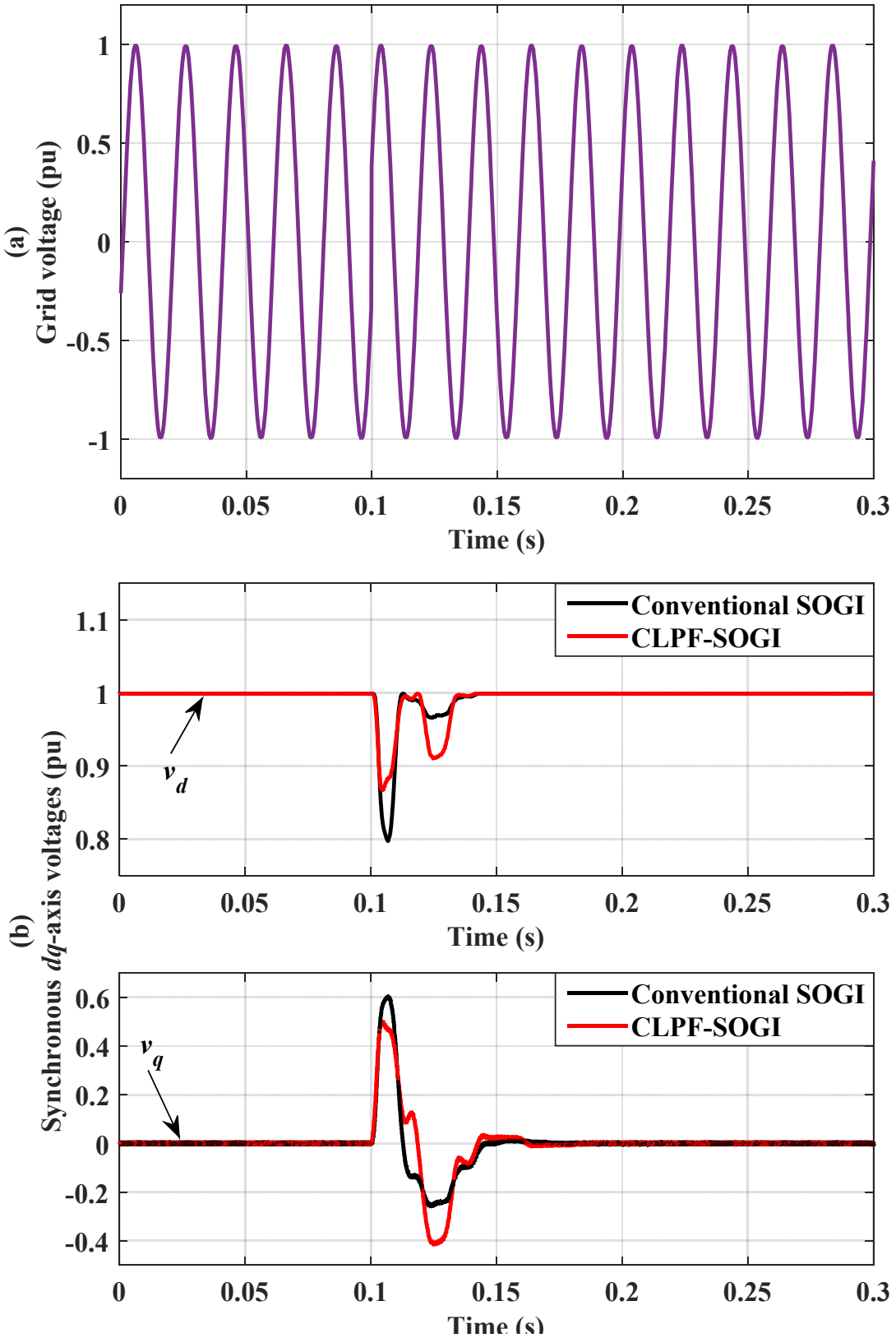


Figure 7.11. Performance of conventional SOGI-PLL and CLPF-SOGI PLL when the input voltage undergoes frequency step changes: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.3.2 Performance Comparison under Phase-angle Jump

Figure. 7.12 depicts the experimental results, when the grid voltage experiences a phase-angle jump of +40°. Due to this disturbance, there is a 0.13 and 0.2 p.u peak voltage amplitude error when CLPF-SOGI and conventional SOGI-PLL are used respectively. The correct value of the voltage amplitude is estimated after around 31ms for both techniques. As expected, a large frequency transient is experienced during this phase jump disturbance. This is due to the frequency and phase angle being estimated within a single loop. The overshoot is limited to 13.4Hz and 16.5Hz for CLPF-SOGI and conventional SOGI PLLs respectively. The 2% settling time, i.e., the time after which the PLL phase error reachs and remains within 0.8° of the

neighbrhood of zero for CLPF-SOGI and conventional SOGI is approximately 38ms and 41ms respectievely.



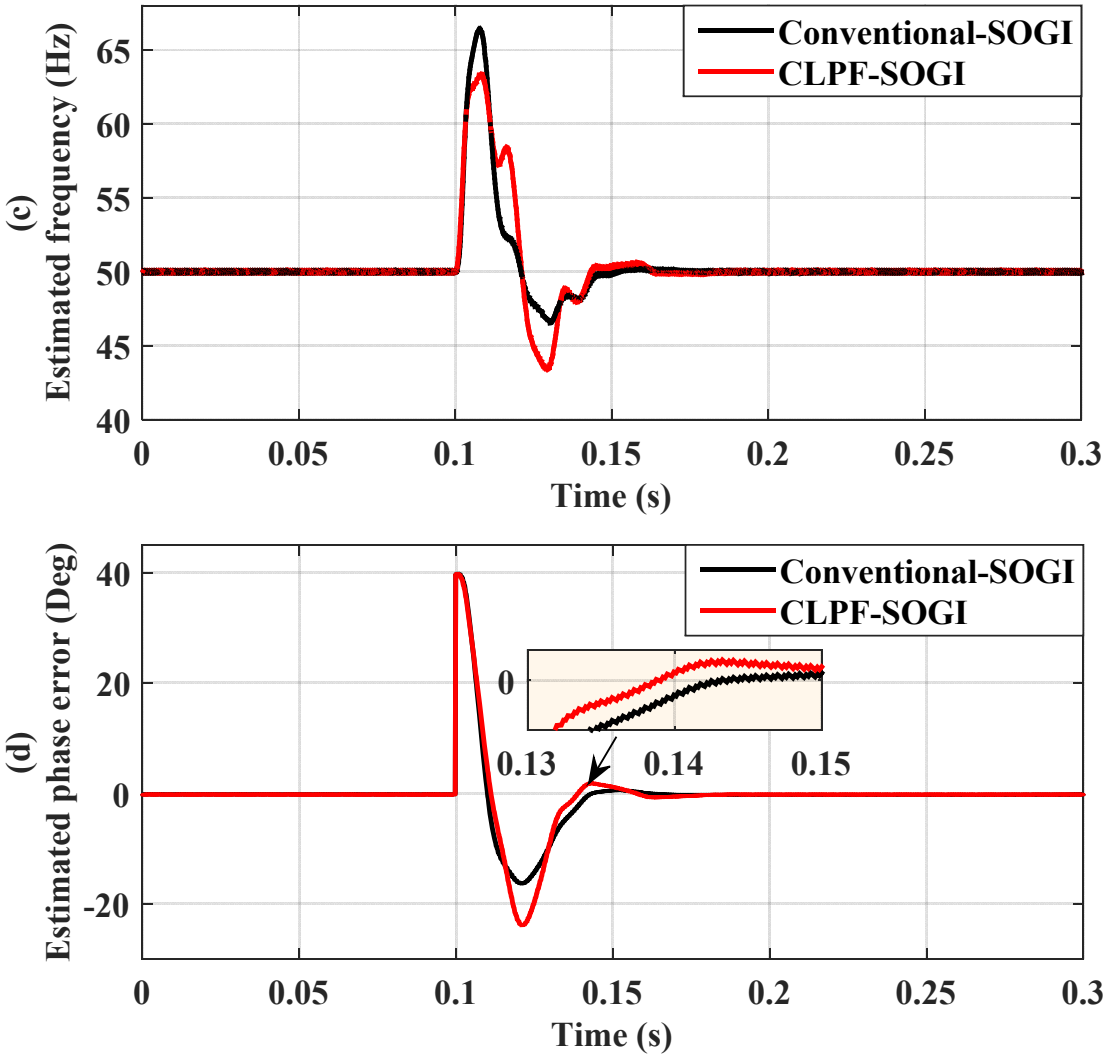
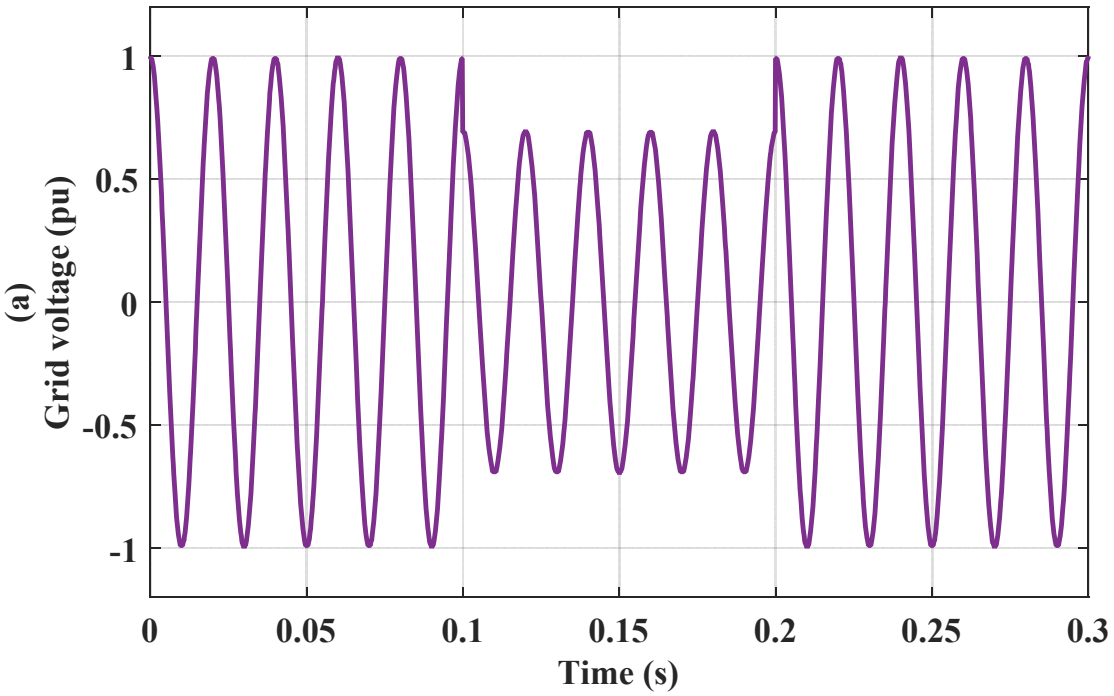
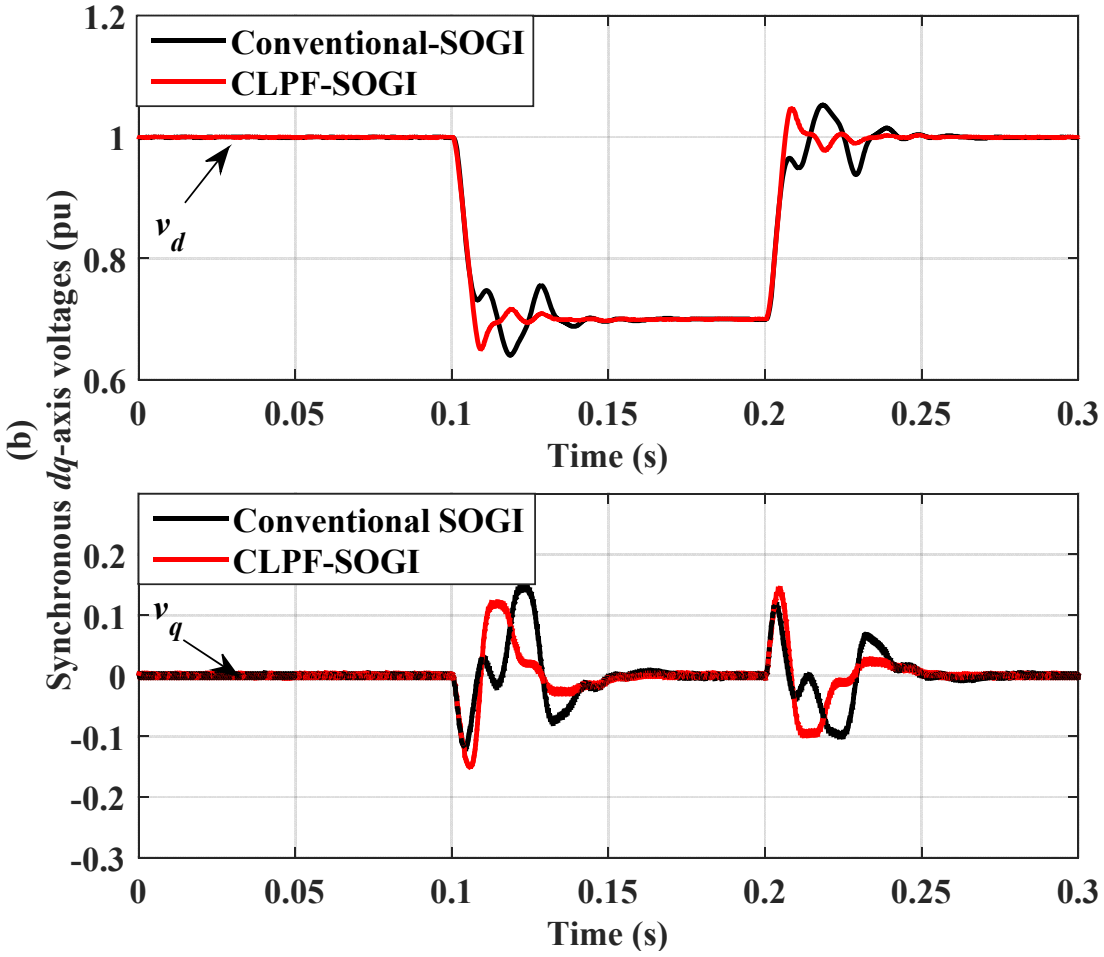


Figure 7.12. Performance of conventional SOGI-PLL and CLPF-SOGI PLL when the input voltage undergoes a phase jump of 40°: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.3.3 Performance Comparison under Voltage Sag

The tranisent response of the proposed CLPF-SOGI and the conventional SOGI-PLLs when the grid is subjected to 0.3 p.u voltage sag is shown in Figure. 7.13. It is clear that in both schemes, the voltage amplitude attains the new steady-state value of 0.7 p.u within approximately less than one fundamental period. However, the conventional SOGI-PLL shows some fluctuation around the steady-state value. In the estimation of frequency, both schemes exhibit a relatively high frequency overshoot (3.5Hz) with similar dynamic response with a settling time of less than two cycles. Furthermore, the correct value of phase-angle is estimated after two cycles.


(a)
Grid voltage (pu)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)


(b)
Synchronous dq-axis voltages (pu)
Conventional-SOGI
CLPF-SOGI
v_d
1.2
1
0.8
0.6
Time (s)
Conventional SOGI
CLPF-SOGI
v_q
0.2
0.1
0
-0.1
-0.2
-0.3
Time (s)

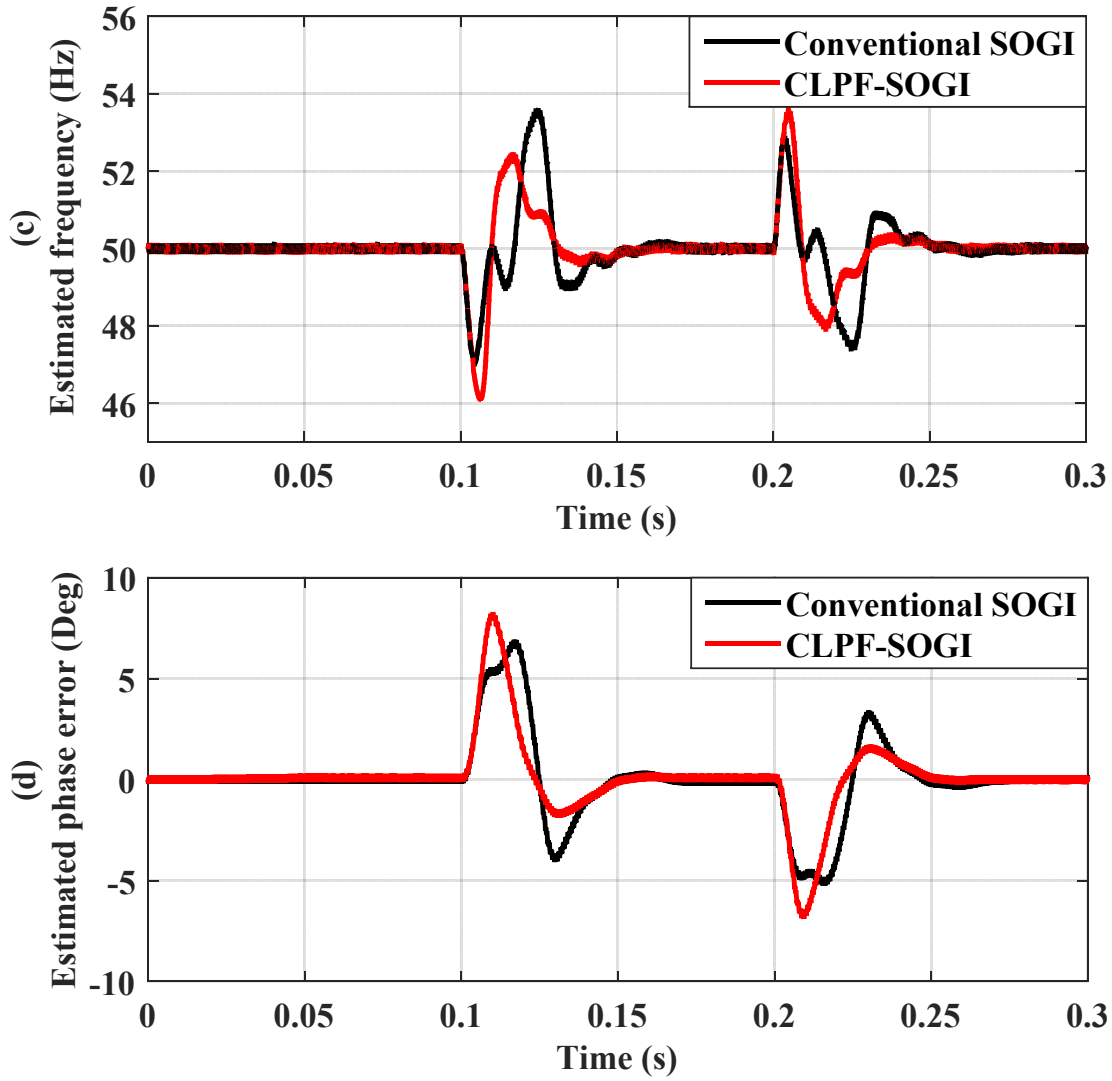
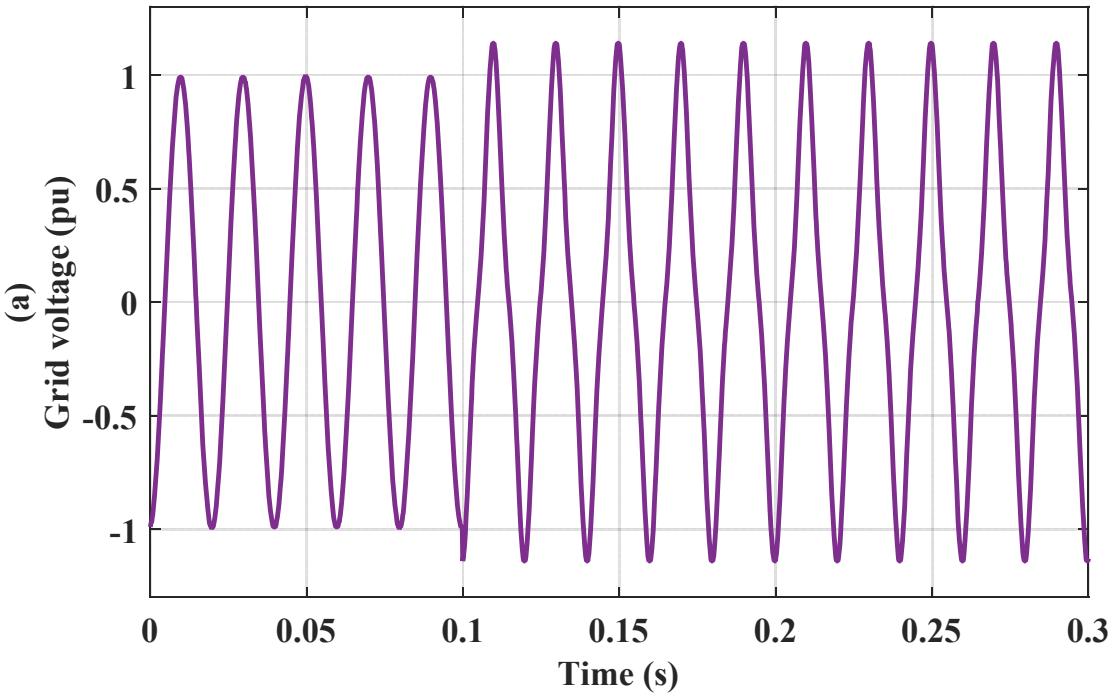
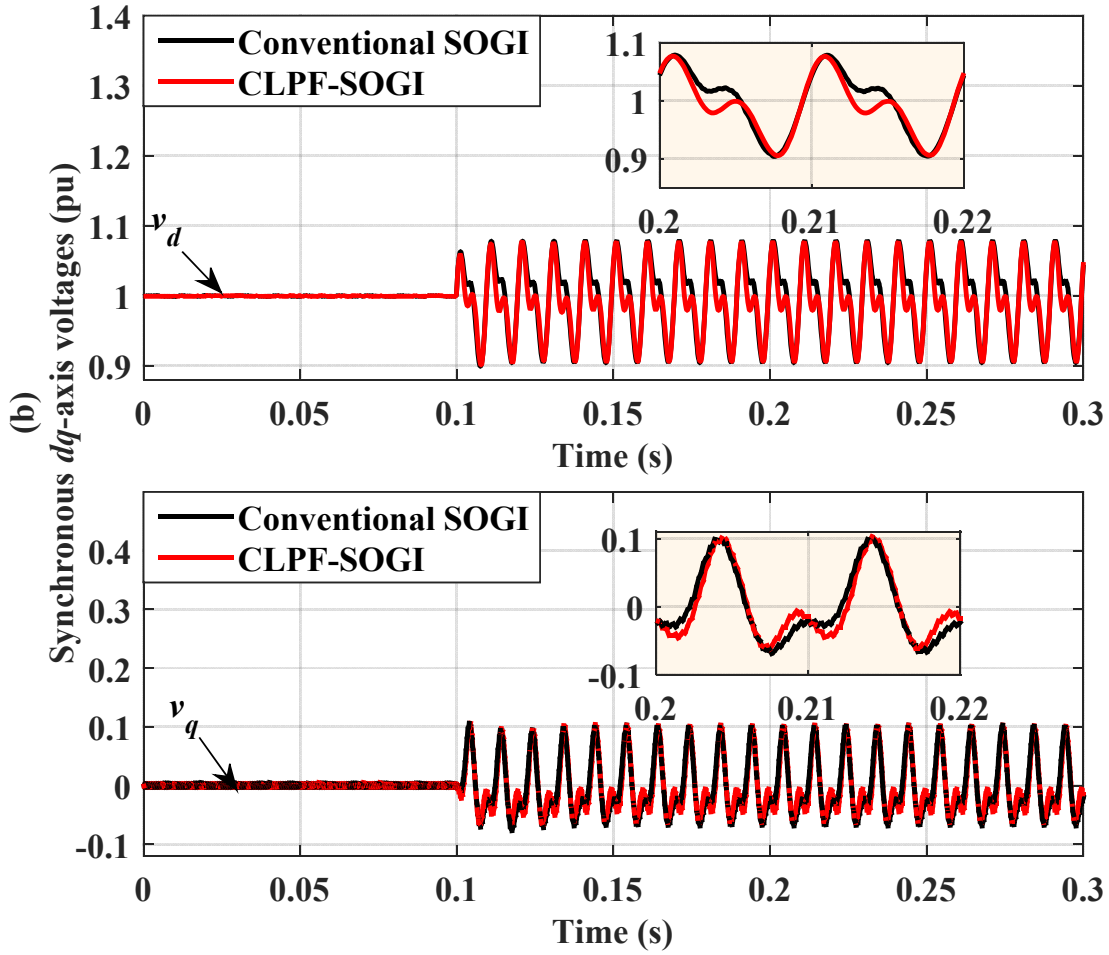


Figure 7.13. Performance of conventional SOGI-PLL and CLPF-SOGI PLL when the input voltage undergoes a voltage-sag of 0.3p.u: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.3.4 Performance Comparison under Grid Voltage Harmonics

The performance of the two PLLs in distorted grid conditions is investigated in this test case. A 15% third-harmonic component is injected into the input the grid voltage signal. As illustrated in Figure. 7.14, the harmonic distortion causes noticable oscillations in the estimated quantities of the PLLs in the steady-state. By comparison, the oscillation in the proposed CLPF-SOGI-PLL is slightly smaller, with a frequency error of about 3.5Hz. The conventional SOGI shows a frequency error of about 3.7Hz. It is worth mentioning that, these oscillations can be further attenuated by narrowing the PLL band-width, but at the cost of slower dynamic response of the PLL system.


(a)
Grid voltage (pu)
1
0.5
0
-0.5
-1
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)


(b)
Synchronous dq-axis voltages (pu)
Conventional SOGI
CLPF-SOGI
v_d
1.4
1.3
1.2
1.1
1
0.9
1.1
1
0.9
0.2
0.21
0.22
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)
Conventional SOGI
CLPF-SOGI
v_q
0.4
0.3
0.2
0.1
0
-0.1
0.1
0
-0.1
0.2
0.21
0.22
0
0.05
0.1
0.15
0.2
0.25
0.3
Time (s)

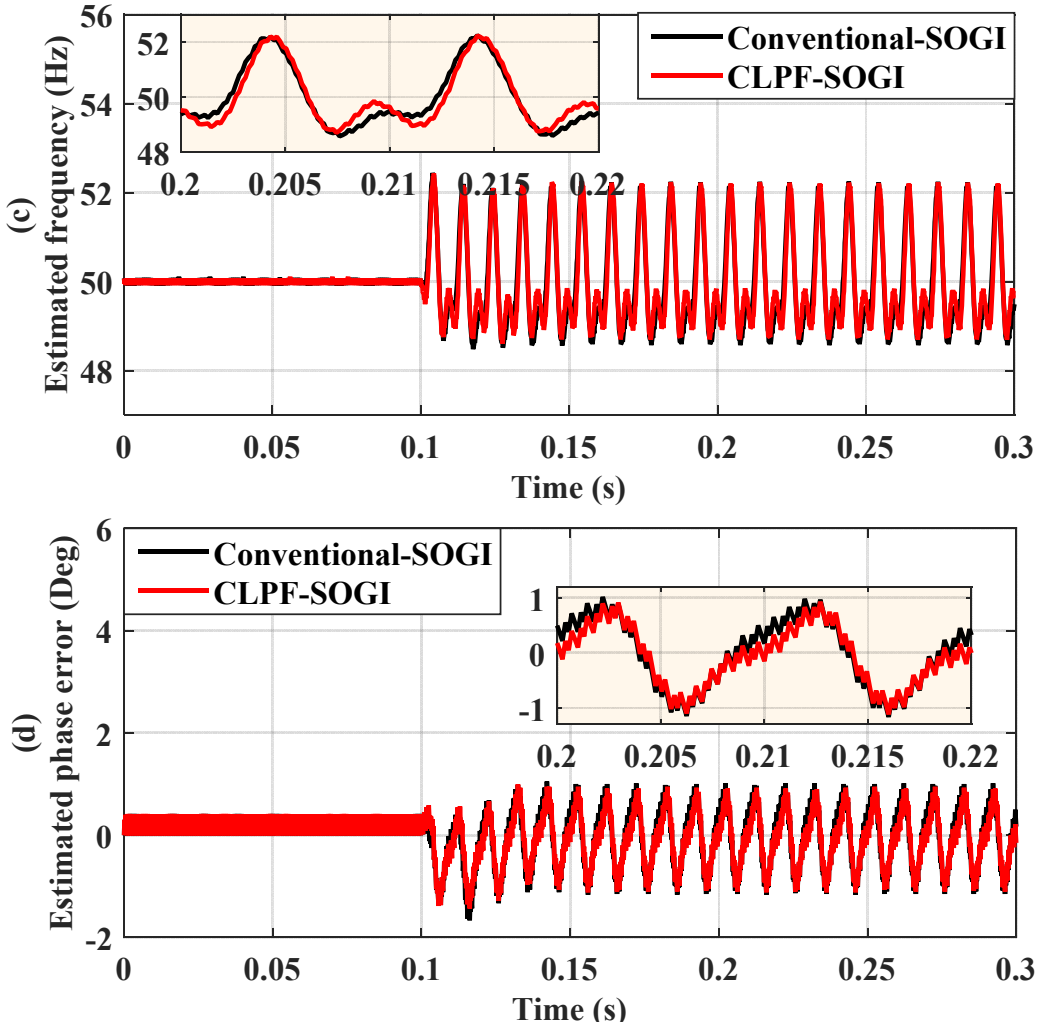
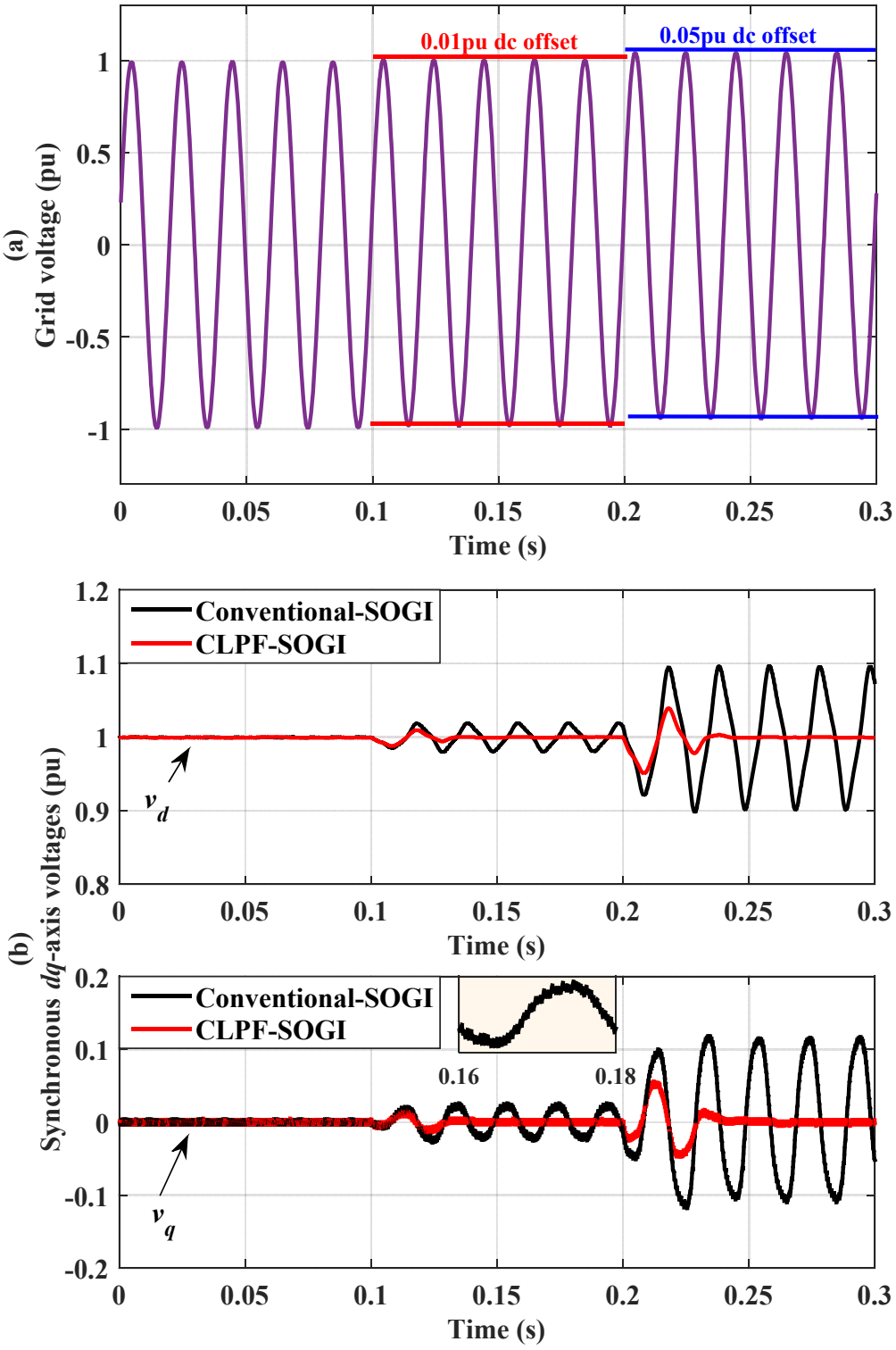


Figure 7.14. Performance of conventional SOGI-PLL and CLPF-SOGI PLL when the input voltage undergoes a voltage-sag of 0.3p.u: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.3.5 Performance Comparison under DC Offset

In order to test the robustness of the proposed CLPF-SOGI method for offset rejection, two different dc components (0.01 and 0.05 p.u) at two different times (0.1 and 0.2s) are suddenly added. The waveforms corresponding to this test case are depicted in Figure. 7.15. It can be observed that, the presence of dc offset in the measured grid voltage signal, siginficantly affects the quantities estimated by the conventional SOGI PLL. Steady-state oscillations with 0.04 p.u to 0.2 p.u ripple in the estimated grid amplitude, 1.2Hz to 5Hz ripple in the estimated frequency, and 1.4° to 6° peak-peak error in the estimated phase-angle error, are opserved. Notice that, these errors have the same frequency to that of the grid voltage, which is very hard to suppress using an extremely low-bandwidth since this can degrade the dynamic response of the PLL

system [115, 142]. However, using the proposed CLPF-SOGI PLL scheme, the steady-state ripple of the estimated quantities are effectively suppressed. As can be seen, the proposed PLL quickly rejects the dc offset and as a result, the transient exists only for about one cycle.



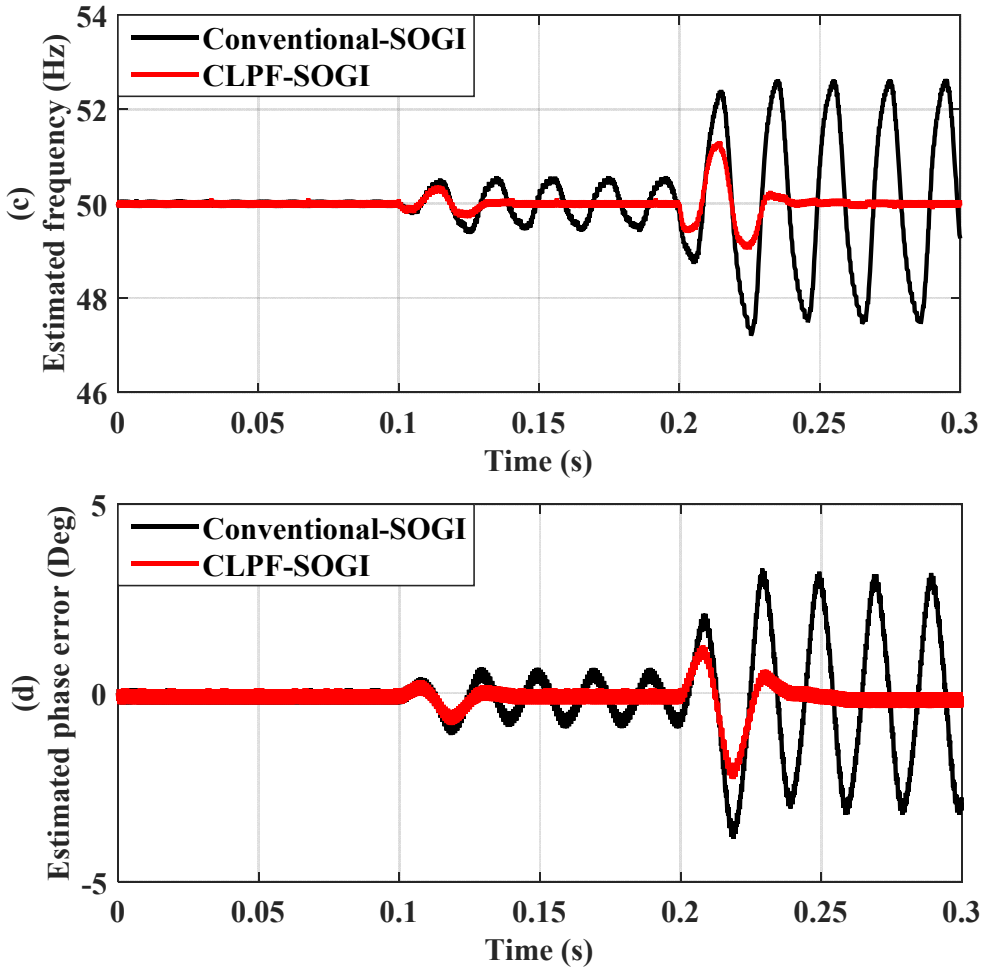
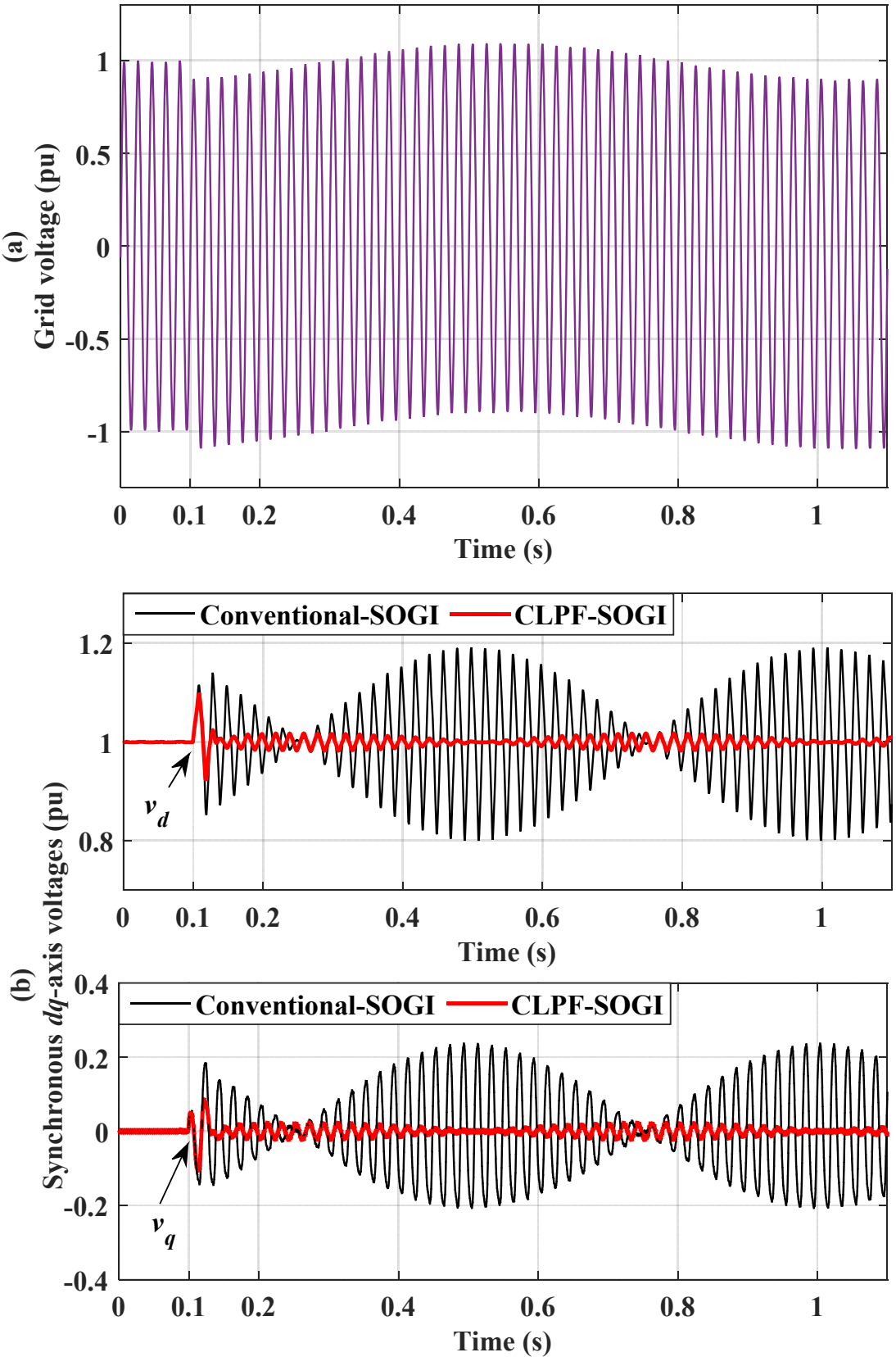


Figure 7.15. Performance of conventional SOGI-PLL and CLPF-SOGI PLL when the input voltage undergoes a 0.01 and 0.05 dc offset: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.3.6 Performance Comparison with subharmonics added

Figure.7.16 shows the response of the two implemented PLLs in the presence of 0.1p.u subharmonic oscillations at a very low frequency of 1 Hz. As expected, the presence of such a subharmonic in the input voltage signal, notebly deteriorates the estimated quantities by the conventional SOGI PLL. This is due to the LPF charasteristics that G_β has for frequencies below the fundamental frequency. As a result, a steady-state ripple of 10 Hz occurs in the estimated frequency, a peak-to-peak error in the estimated amplitude of 0.4p.u, and an oscillation of about 12° in the estemated phase-angle error. These distortions are very important and can deteriorate the response of the PLL system. On the other hand, by adopting the CLPF-SOGI PLL, the negative effect of grid subharmonics can be effectively alleviated. For this case, it is important to highlight that a maximum frequency ripple is only 1 Hz, which is ten times lower than the

previous case. Besides, the maximum amplitude and phase angle distortion have been greatly reduced to less than 0.04p.u and 1.4° respectively.



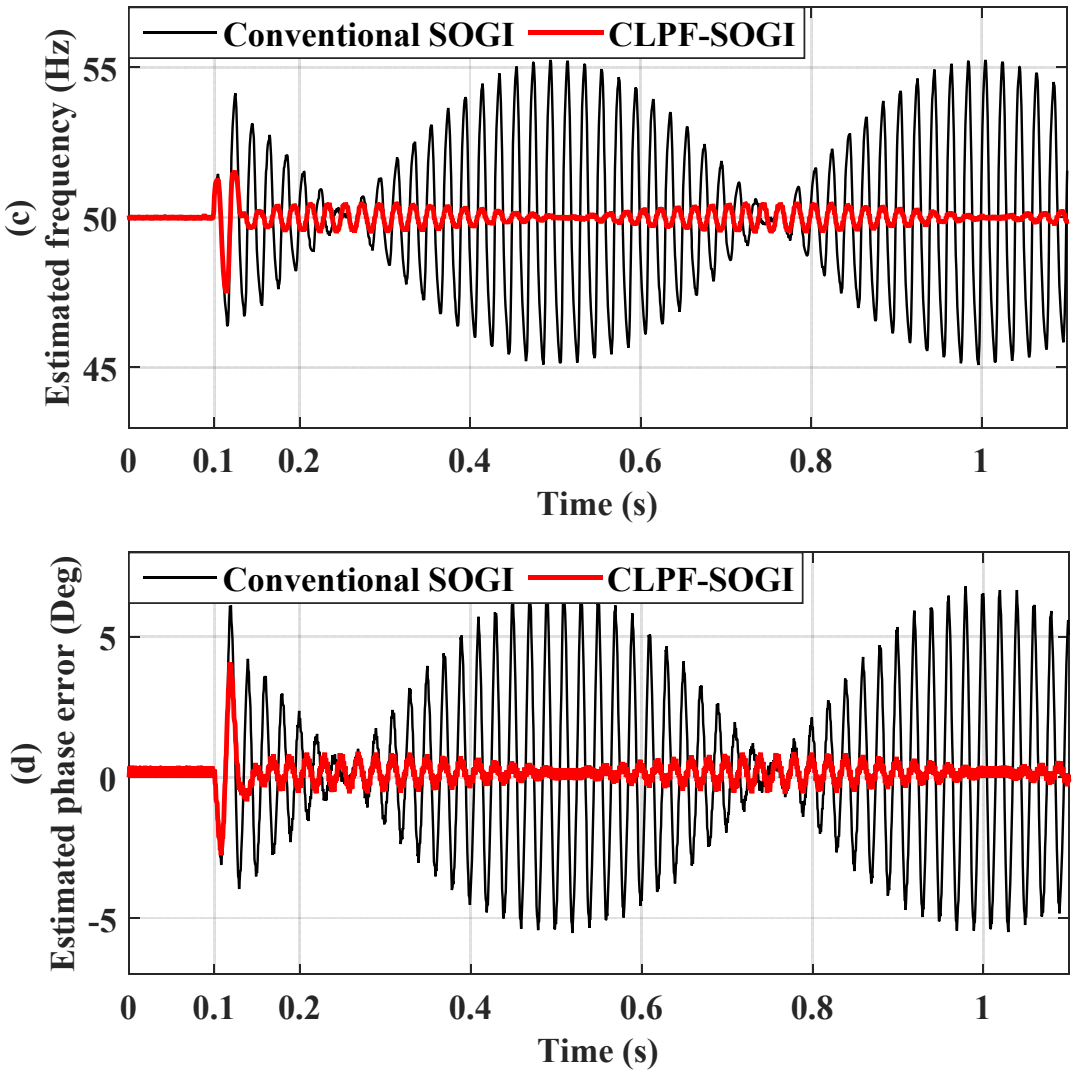


Figure 7.16. Performance of conventional SOGI PLL and CLPF-SOGI PLL when the input voltage undergoes a 10% of 1Hz subharmonic: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.4 Dynamic Performance Evaluation under Combined Disturbances Test Cases

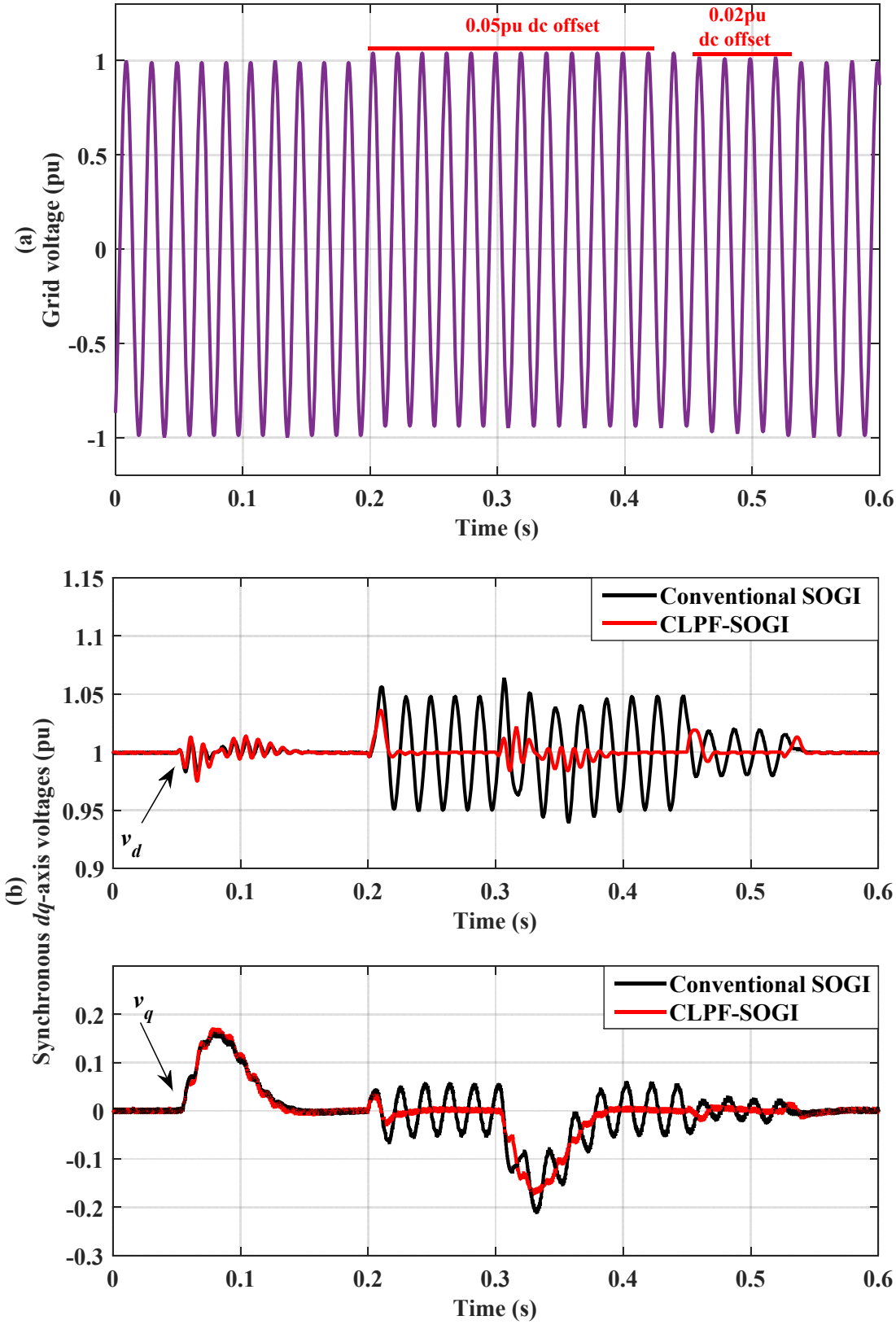
To further improve the evaluation of the proposed CLPF-SOGI-PLL scheme performance in comparison with the conventional SOGI-PLL, two more different test cases are conducted where collective disturbances are involved. In both cases, the tuning parameters for both PLLs have been set according to Table 7-2, in which the wide-bandwidth of the PLL algorithms used in Table 7-1 for section 7.3 evaluations has been replaced by a narrow-bandwidth as it has been suggested earlier in 6.3.1.

Table 7-2 SOGI-PLL and CLPF-SOGI PLL parameters

Parameter	Symbol	Value (unit)
SOGI-OSG gain	k	1
Crossover frequency	ω_c	65.45 rad/s
PLL damping factor	ξ	0.7
Phase margin	PM	44.8°
PLL Proportional gain	k_p	65.45
PLL Integral gain	k_i	1784
Settling time	t_s	0.0937s
Nominal frequency	ω	2.π.50 rad/s
Input voltage amplitude	V_m	1 p.u
CLPF time constant	τ	(1/ ω^)s
Sampling frequency	f_s	20kHz

7.4.1 Performance Comparison under Frequency Variations with DC Offset

To take into consideration the effect of the grid frequency deviations on the PLL dc offset elimination capability, this test is conducted under the nominal frequency (i.e., 50Hz) and off-nominal frequency 52Hz. Figure. 7.17 shows performance of both CLPF-SOGI and conventional SOGI when the grid voltage undergoes a frequency step change of +2Hz at t=0.05s that is followed with a 0.05 p.u jump in the dc component. Again at t=0.3s, the grid voltage frequency is returned back to its nominal value. At time t=0.45s the dc component is reduced to 0.02p.u before it is minimized to zero. It is observed that, the proposed techniques performs successfully to reject the error caused by the dc offset regardless the value of grid frequency. On the other hand, and as expected the conventional technique is unable to supress the errors caused by such dc components.


0.05pu dc offset
0.02pu
dc offset
(a)
Grid voltage (pu)
Time (s)
(b)
Synchronous dq-axis voltages (pu)
Conventional SOGI
CLPF-SOGI
v_d
v_q
Time (s)

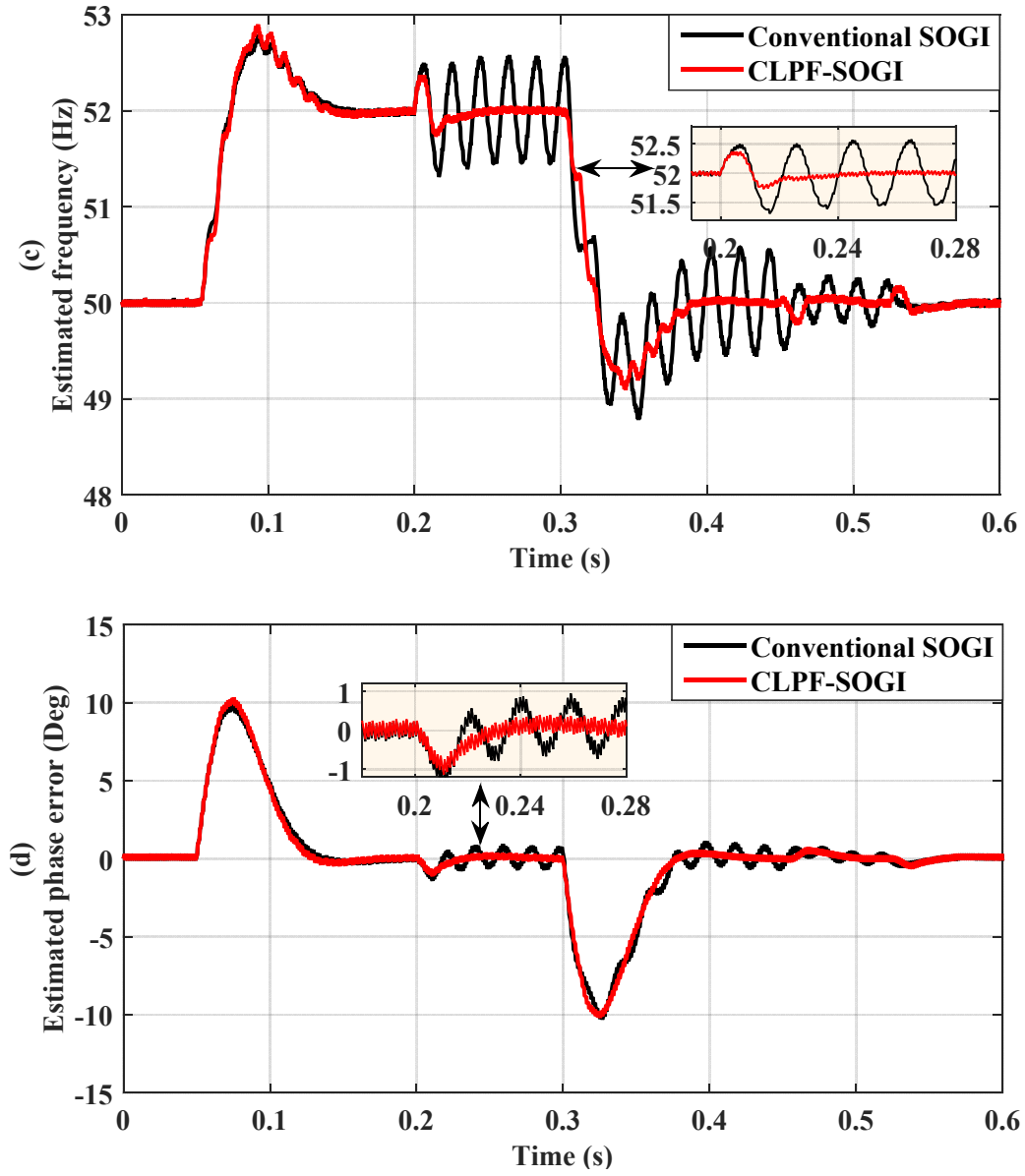
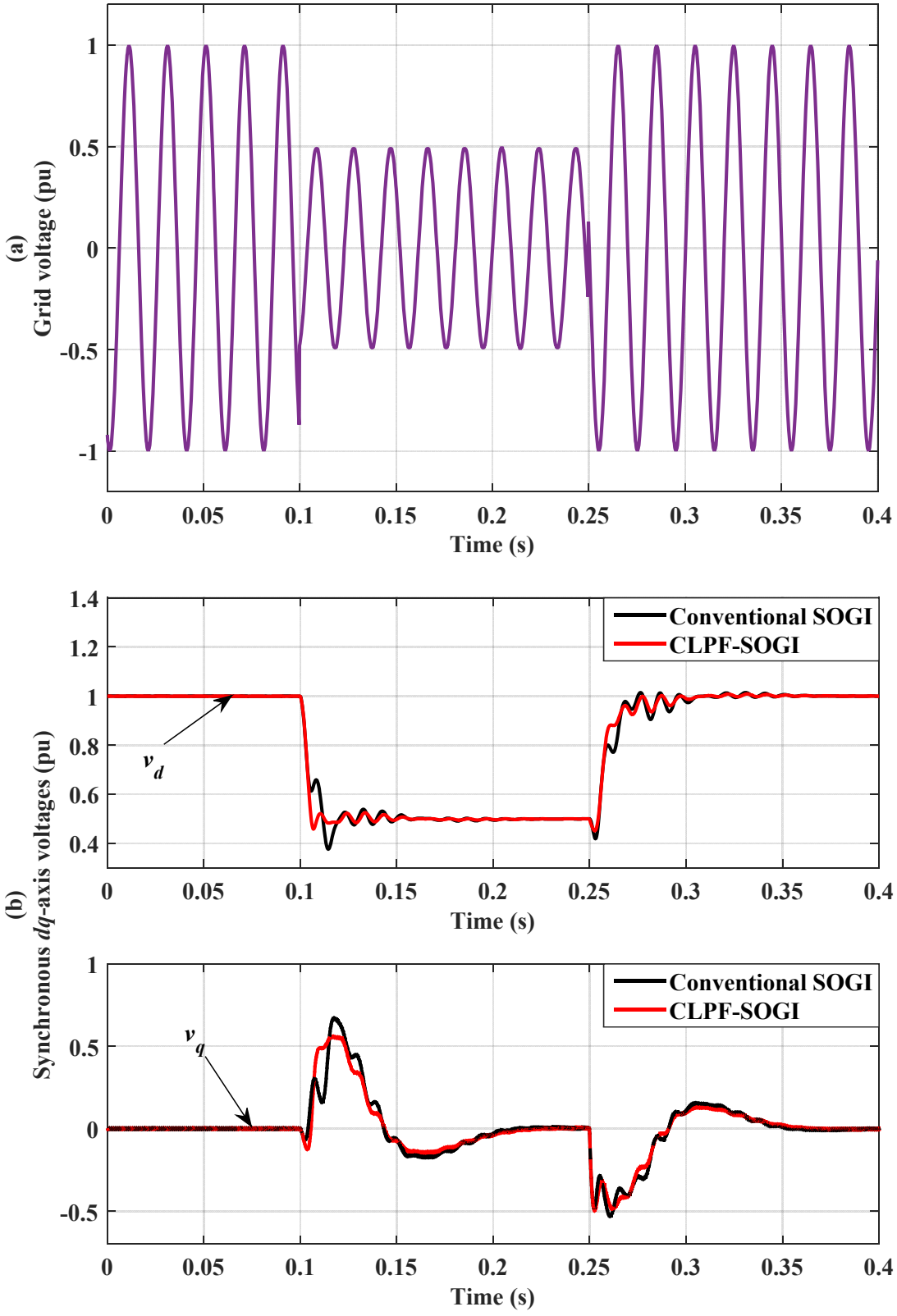


Figure 7.17. Performance of conventional SOGI PLL and CLPF-SOGI PLL under frequency variations with dc offset: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.4.2 Performance Comparison under Voltage Sag, Phase Jump and Frequency Changes

As suggested in [123], a more severe and realistic grid disturbance condition that may occur in the utility grid due to short-circuit fault is considered in this test case as shown in Figure. 7.18. This case involves of a voltage sag of 0.5 p.u, a phase jump of 40°, and a frequency step of 2 Hz (from 50 to 52 Hz and then from 52 back to nominal grid frequency). From the obtained results, it can be clearly noted that, both PLL schemes present almost identical transient response. Also, it can be seen that the detected phase-angle and frequency reach their desired

values in about 93.7ms, matching the theoretical value specified in Table 7-2 that can be calculated through (3.33).



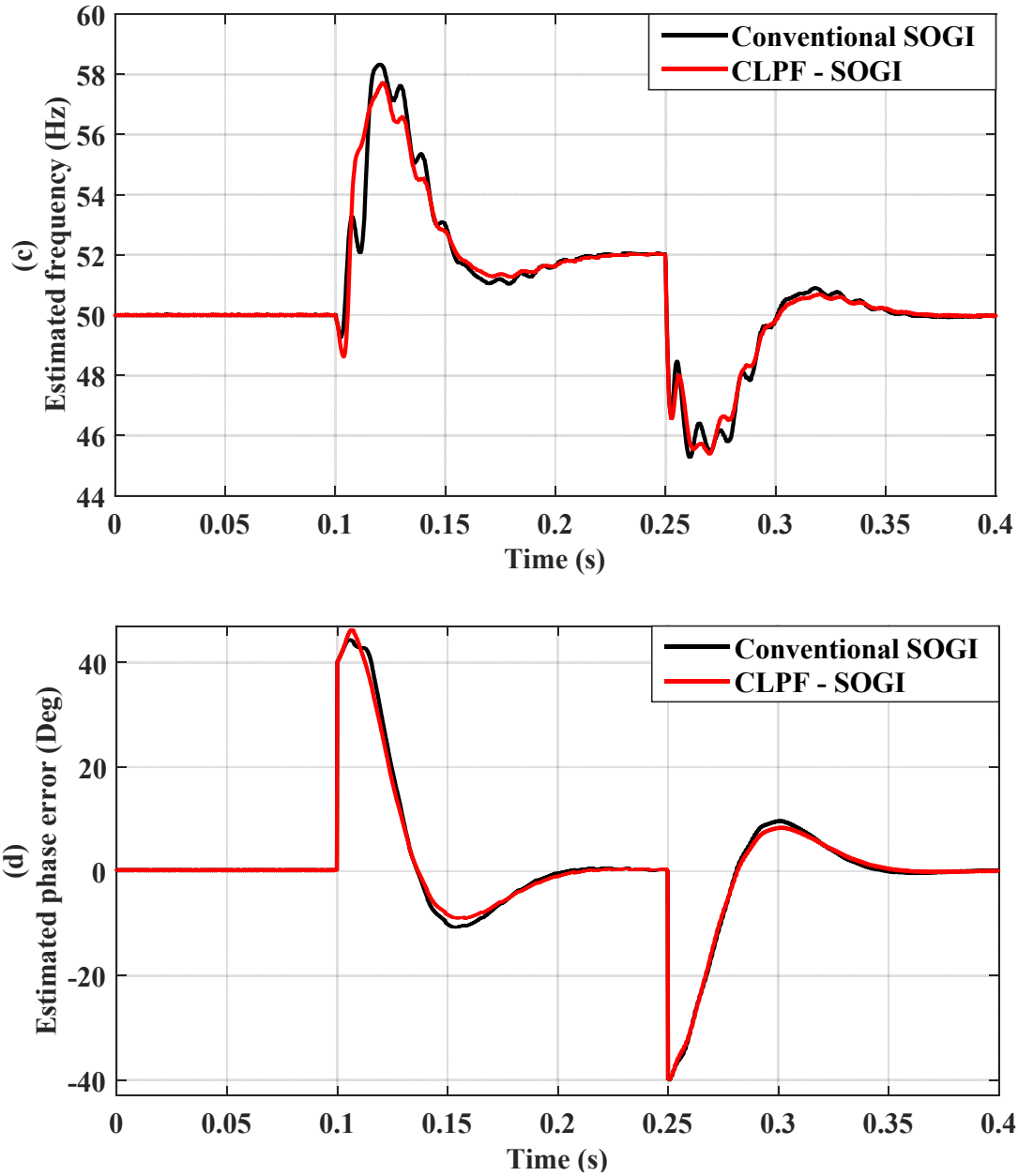


Figure 7.18. Performance of conventional SOGI PLL and CLPF-SOGI PLL under voltage sag with phase jump and frequency variations: (a) Input voltage, (b) signals in the synchronous reference frame, (c) estimated frequency, and (d) estimated phase-angle error.

7.5 Summary

This chapter has presented experimental results of a single-phase PLL system; implementing four different orthogonal signal generator techniques (OSG) based SOGI-PLL. Steady-state results have shown the capability of the proposed CLPF-SOGI PLL to completely remove the dc component. In addition, they have illustrated the ability of the proposed PLL to provide a superior harmonic attenuation performance when compared with the other methods. To verify

this, the obtained experimental results have been compared with those of analytical and numerical results obtained in Figures 4.21 and 4.27 respectively. A good agreement has been found between these results validating the proposed approach.

It has also been shown that, the presence of such dc component in the input signal results in deteriorating the estimated synchronisation signal produced by the conventional SOGI PLL. In this case, the synchronization signal will possess dc components and second-order harmonics. The presence of such components in the synchronization signal is undesirable as it can result in dc current injection into the grid. However, this undesired component is completely suppressed when the proposed CLPF-SOGI PLL scheme is used. This issue will be investigated in the next chapter.

To further support the effectiveness of the proposed PLL, a real grid signal is used as an input signal for both PLLs in order to estimate the required attributes. The corresponding results obtained by the proposed PLL are shown to be better when compared to classic SOGI PLL in terms of steady-state ripple. Furthermore, to examine the dynamic response of the proposed CLPF-SOGI PLL, various test cases have been conducted. To point out the effectiveness of the proposed method, the conventional SOGI-PLL is also implemented, and its results are compared with those of the proposed technique. The reported experimental results have shown that, the proposed PLL presents a similar dynamic response with the conventional PLL under several grid abnormalities. However, the proposed CLPF-SOGI has more advantages in terms of grid dc offset voltage rejection, subharmonics alleviation and enhanced harmonic attenuation. Hence, the proposed CLPF-SOGI PLL can be preferred over the conventional SOGI PLL to achieve a perfect steady-state and transient performance under the presence of dc component in or /and harmonic distorted environments.

Finally, since the operation of the current controller is based on the accurate estimation of the synchronization signals, it is expected that the accurate synchronization will directly affect the performance of the grid-connected PV system. Therefore, in addition to the performance evaluation of the proposed *dq* current controller, a further experimental investigation to verify the beneficial impact of the accurate synchronization on the power quality of the grid-connected PV system is conducted in the next chapter.

CHAPTER 8

Performance Evaluation of the DQ Current Controller

8.1 Introduction

This chapter presents the results for the simplified *dq* current control algorithm described in Chapter 5. The chapter is split into two sections. In the first section, the performance of the proposed *dq* current controller for single-phase grid-connected VSI with LCL filter is evaluated by means of experimental results. To demonstrate the effectiveness of the proposed approach in improving the poor dynamic response related to the conventional *dq* controller, the performance of both approaches is experimentally evaluated.

In the second section, a further experimental investigation to verify the beneficial impact of the proposed CLPF-SOGI PLL on the power quality of the grid-connected PV system is conducted. To highlight the effectiveness of the proposed PLL, a power quality performance comparison between both PLL schemes are carried out. In this comparison, a dc offset is deliberately added to the measured grid voltage signal, to evaluate the immunity of the proposed CLPF-SOGI PLL as well as to investigate the influence of such a disturbance on the quality of the injected current. From the obtained results, it can be observed that the accurate operation of the proposed CLPF-SOGI PLL enhances the performance of the grid-connected PV system and enables a high-quality current injection in the presence of high level of dc component in the grid voltage signal. The experimental results show the significance of the contribution of the proposed CLPF-SOGI PLL in the power quality of grid-connected PV systems.

8.2 Transient Performance Evaluation

This section aims to experimentally evaluate the performance of the proposed simplified-*dq* current control scheme and also to compare it with that of the conventional delay-based control strategy. The test system described in Chapter 6 along with the corresponding parameters presented in Table 6-1 is adopted. Note that, in the following test case, both controllers are designed based on the same design criteria described in Chapter 5 to have the same bandwidth by fine tuning the PI-controller gains as follows: k_p= 1860, and k_i=18671 with a damping factor ζ = 0.7. Also, it is worth remarking that, the proposed CLPF-SOGI PLL that was discretized in Chapter 6 is employed to generate the synchronisation signals (i.e., $\hat{\theta}$, v_{grid}^{d}, and v_{grid}^{q}) which are required for performing both control algorithms as depicted in Figures. 8.1 and 8.3.

To demonstrate the transient performance of both current regulation schemes, a reference tracking test in *d*-axis is carried out. The response of each control strategy is experimentally assessed subsequent to two step changes in the *d*-axis reference value, while the reference value of the q-axis is maintained constant at zero during the whole process.

In order to digitally implement the control strategies, the PI-controllers of Figures. 8.1 and 8.3 are first discretized as presented in Chapter 6, in Figure 6.20 and then developed in C code.

8.2.1 Conventional dq Current Controller

The control strategy shown in Figure.8.1 includes the CLPF that was discretized in Chapter 6 as a means of generating the orthogonal current i_β required for this controller. Initially, the five-level inverter of Figure.6.2 injects a zero value of the *d* component of the grid current. At time instant *t* =0.03s, the reference value of the *d*-axis steps up to 0.5 p.u. Moreover, at time instant *t* = 0.11s, the reference value of *d*-axis steps up to its full value of 1 p.u. Figure. 8.2(a) depicts the grid voltage and its generated orthogonal voltage v_β. Due to the grid being stiff enough, these voltages remain unchanged during step changes. However, as shown in Figure. 8.2(b), upon each step-change in the *d*-axis reference, the controller tries hard to regulate the α current at the desired value; however, due to excessive transients, there is an overshoot in the regulated current. Moreover, as shown in Figure.8.2(c), the corresponding *d*- axis of the current changes to track the reference value changes but, experiences non-negligible transients for approximately one cycle due to the delay used in the controller. Therefore, it takes almost 20ms for the controller to regulate the *d* component of the current to track the reference value with a

zero steady-state error. Also, it is observed from Figure. 8.2(c) that, although the reference value of the *q*-axis is kept constant at zero throughout the process of this test, subsequent to each step change in the *d*-axis, the *q*-axis also experiences a non-negligible transient that lasts for nearly 20ms. Thus, the conducted study reveals that, the conventional current control approach suffers from two major drawbacks; excessive transients subsequent to any step change in its *d*-axis, and also from coupled axes.

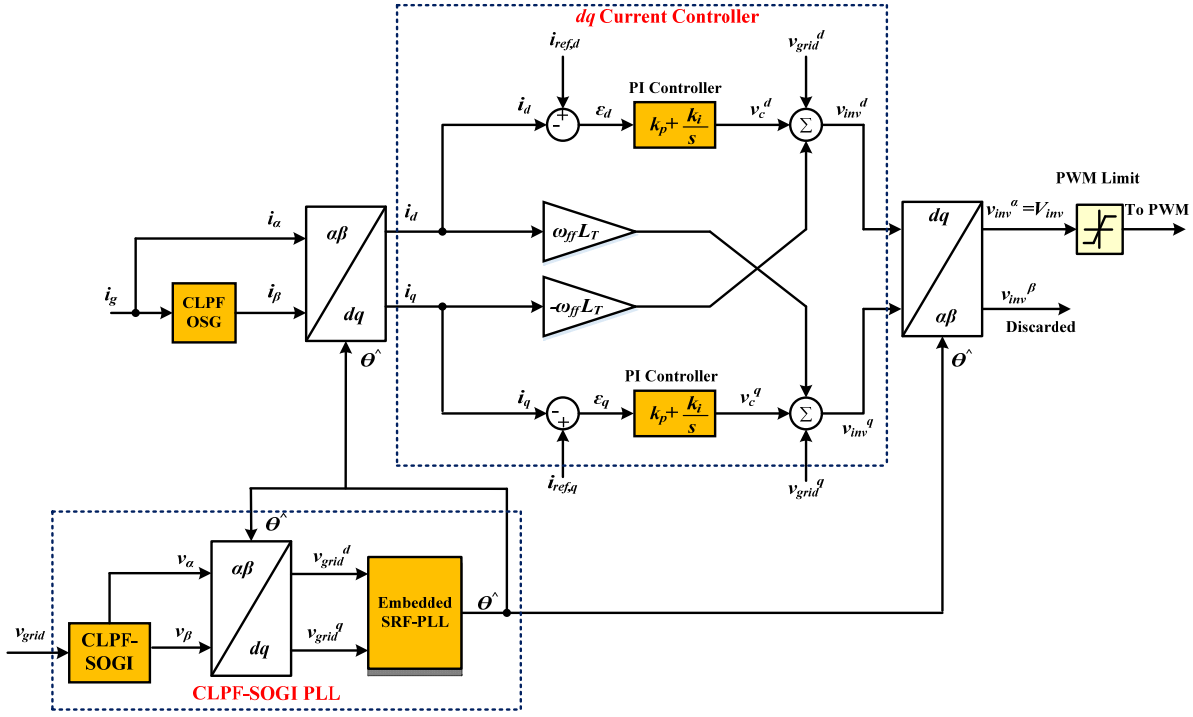


Figure 8.1. Structure of the conventional single-phase current-regulation scheme

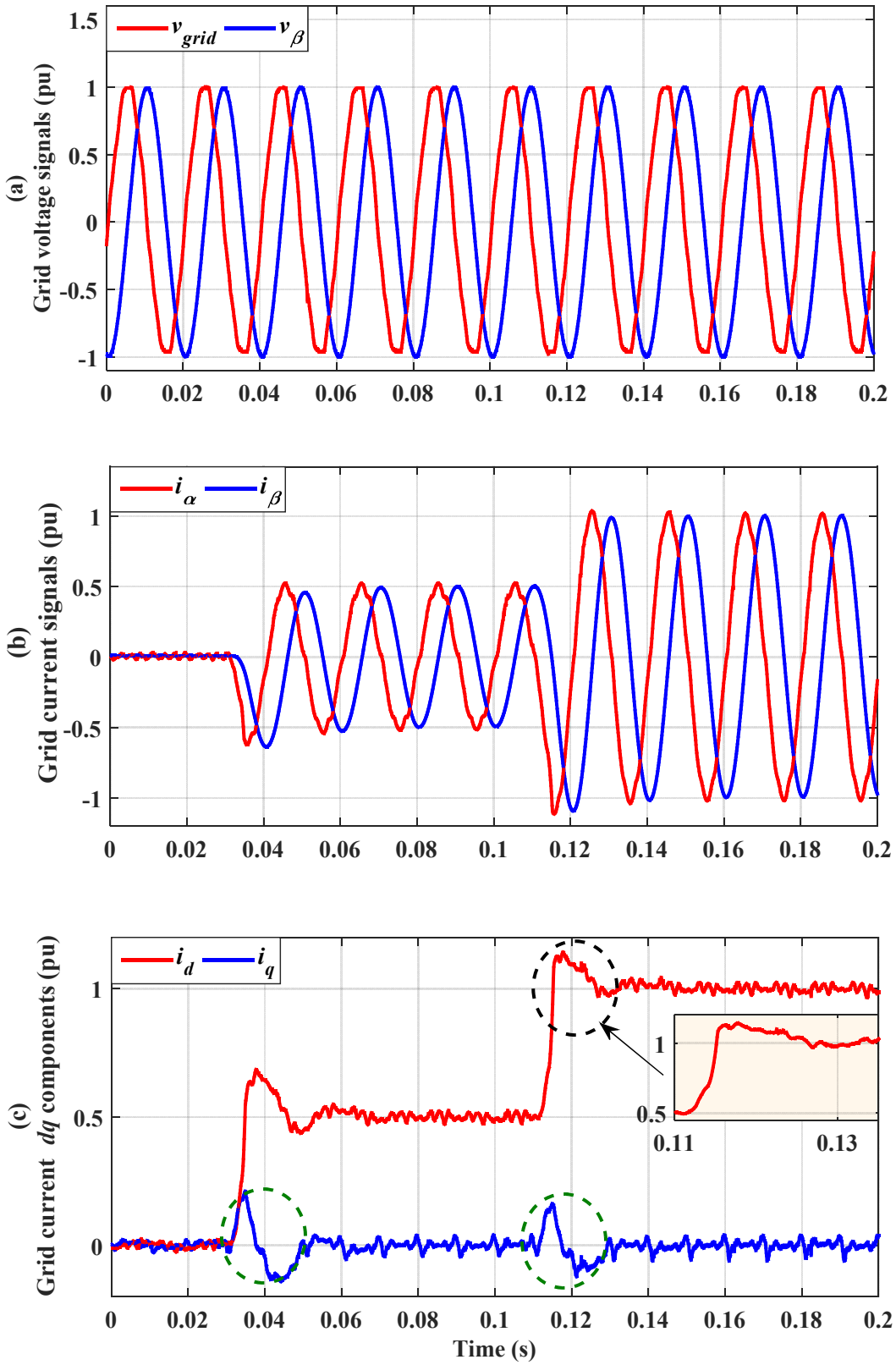


Figure 8.2 Experimental results of the transient response of the conventional delay-based controller during step changes in *d*-axis: (a) The grid voltage and its associated orthogonal component. (b) The grid current and its emulated orthogonal component. (c) The *d*-*q*-axes corresponding to the grid current and its emulated orthogonal component.

8.2.2 Simplified dq Current Controller

In order to properly compare the response of both control approaches, the same previous test described in section 8.2.1 is carried out for the simplified-based approach of Figure. 8.3. This is performed with exactly the same PI-controllers 'gains. The inverter of Figure.6.2 initially sets the *d* component of the grid current to zero. While the reference value of the *q*-axis is maintained constant at zero, the reference value of the *d*-axis steps up to 0.5 p.u at t = 0.02s, and then is changed to 1p.u at t = 0.06s, implying changes in the active power flow as well. Figure.8.4 (a) illustrates the grid voltage orthogonal components (i.e., v_α and v_β), which remain unchanged during the reference tracking changes. However, subsequent to each change in the *d*-axis reference value, the controller drives the grid current at the demanded level in almost 2ms. This is achieved with very little variations during the transient and zero steady-state error as shown in Figure. 8.4(b). Moreover, Figure. 8.4(c) shows the d-q components of the grid current which are controlled to their demanded values by the simplified *dq* control scheme. The later confirms that, contrary to the conventional controller, subject to each *d*-axis step change, the system experiences very short and negligible transients, and the reference value of is tracked in about 2ms with zero steady-state error. Also, subsequent to each step change in the *d*-axis reference value, the *q*-component of the current continues almost unchanged demonstrating the decoupling ability of the proposed controller.

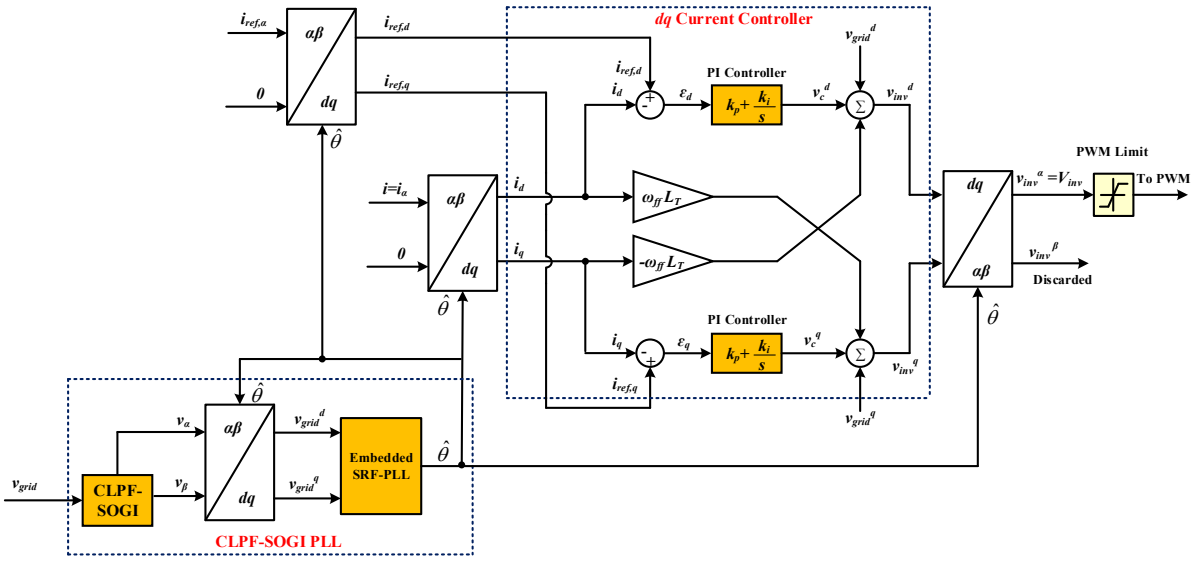


Figure 8.3. Structure of the simplified single-phase current-regulation scheme

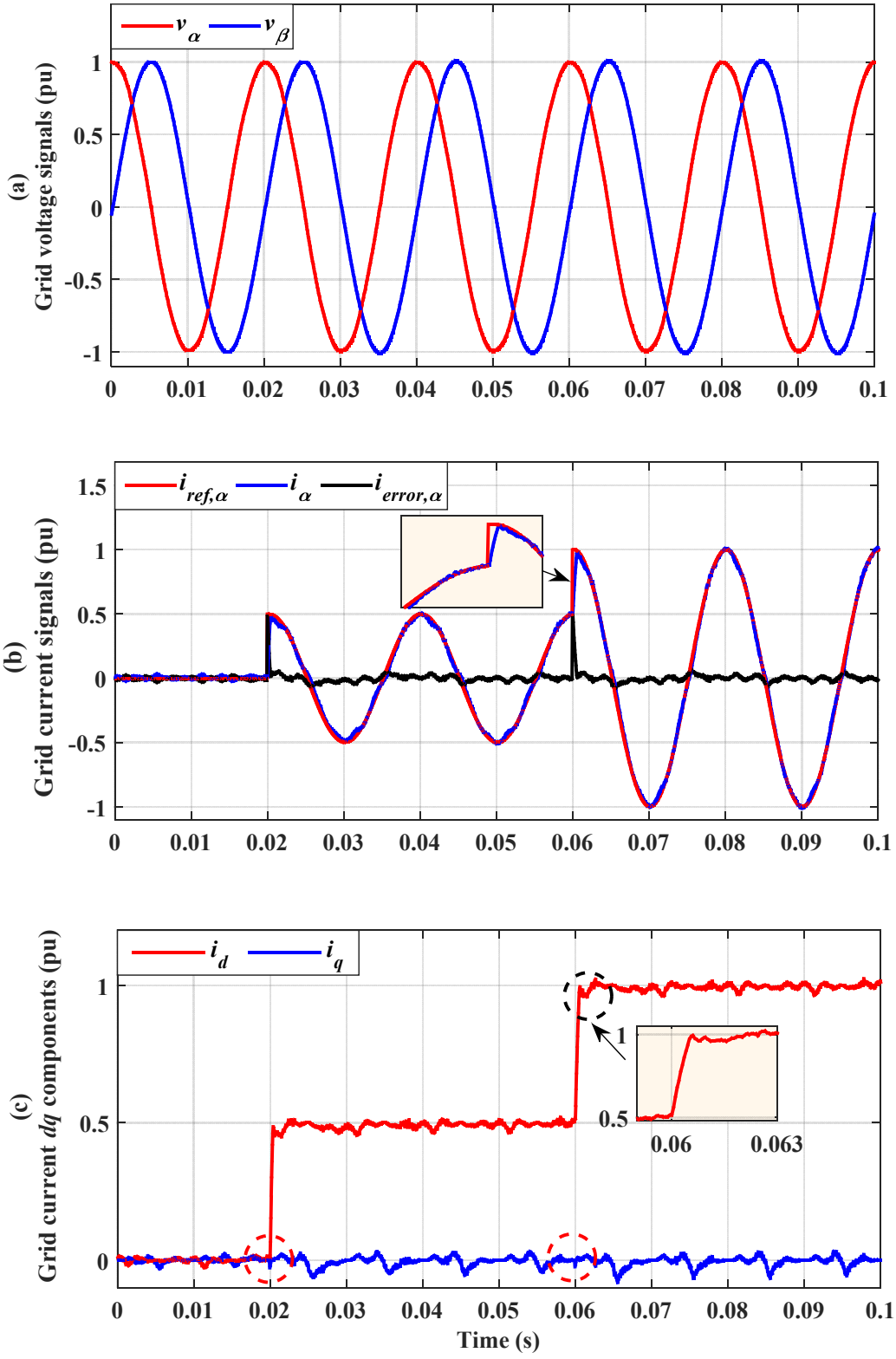


Figure 8.4 Experimental results of the transient response of the simplified controller during step changes in *d*-axis: (a) The grid voltage orthogonal signals. (b) The reference and actual grid currents with their associated tracking error. (c) The *d*- and *q*-axes corresponding to the grid current

The presented test results of Figures. 8.2 and 8.4 verify that the proposed simplified *dq* controller has the following features over the conventional *dq* controller: 1) It is capable of tracking the reference signals with a zero steady-state error within a few milliseconds; 2) It has fast dynamics (approximately 10 times faster); and 3) Compared to the conventional approach, it has superior axis decoupling capability.

8.3 The Effect of the PLL Method on the Grid-connected PV Inverter Performance

According to Figures. 8.1 and 8.3, it is obvious that the response of the PLL (i.e., $\hat{\theta}$, v_{grid}^{d}, and v_{grid}^{q}) directly affects the performance of both current controllers and, subsequently, the operation of the complete grid-connected PV system. Thus, in this section an experimental investigation is described on how the proposed CLPF-SOGI PLL affects the performance of the grid-connected PV system in terms of the power quality. In this study, the simplified *dq* current controller is used, and the measured grid voltage signal is considered to contain dc components. This investigation verifies the significant influence of the accurate synchronization on the response of the grid-connected PV system and reveals a considerable improvement of the power quality of the PV system due to the proposed PLL.

To emphasize the robustness of the proposed PLL and its effect on the performance of the grid-connected PV system, a power quality performance comparison is carried out. This comparison is conducted under the presence of a dc offset in the grid voltage when the proposed CLPF-SOGI PLL and conventional SOGI PLL structures are used for synchronisation. Note that, in order to have a sensible comparison, both PLLs use the parameters specified in Table 3-1.

In this experimental investigation, a grid voltage signal of 85Vrms with a THD of 3.15% is synchronized with the grid-connected PV system's output current of 3.83Arms. The effect of the proposed PLL on the performance of the grid-connected PV system is experimentally evaluated, and compared to that of the conventional SOGI PLL scheme. To examine the immunity of the grid-connected PV system to a dc offset, an excessively large dc component of 17V (20%) is added to the grid voltage signal. Figure.8.5 demonstrates the PV system performance when the proposed CLPF-SOGI PLL is employed for synchronisation.

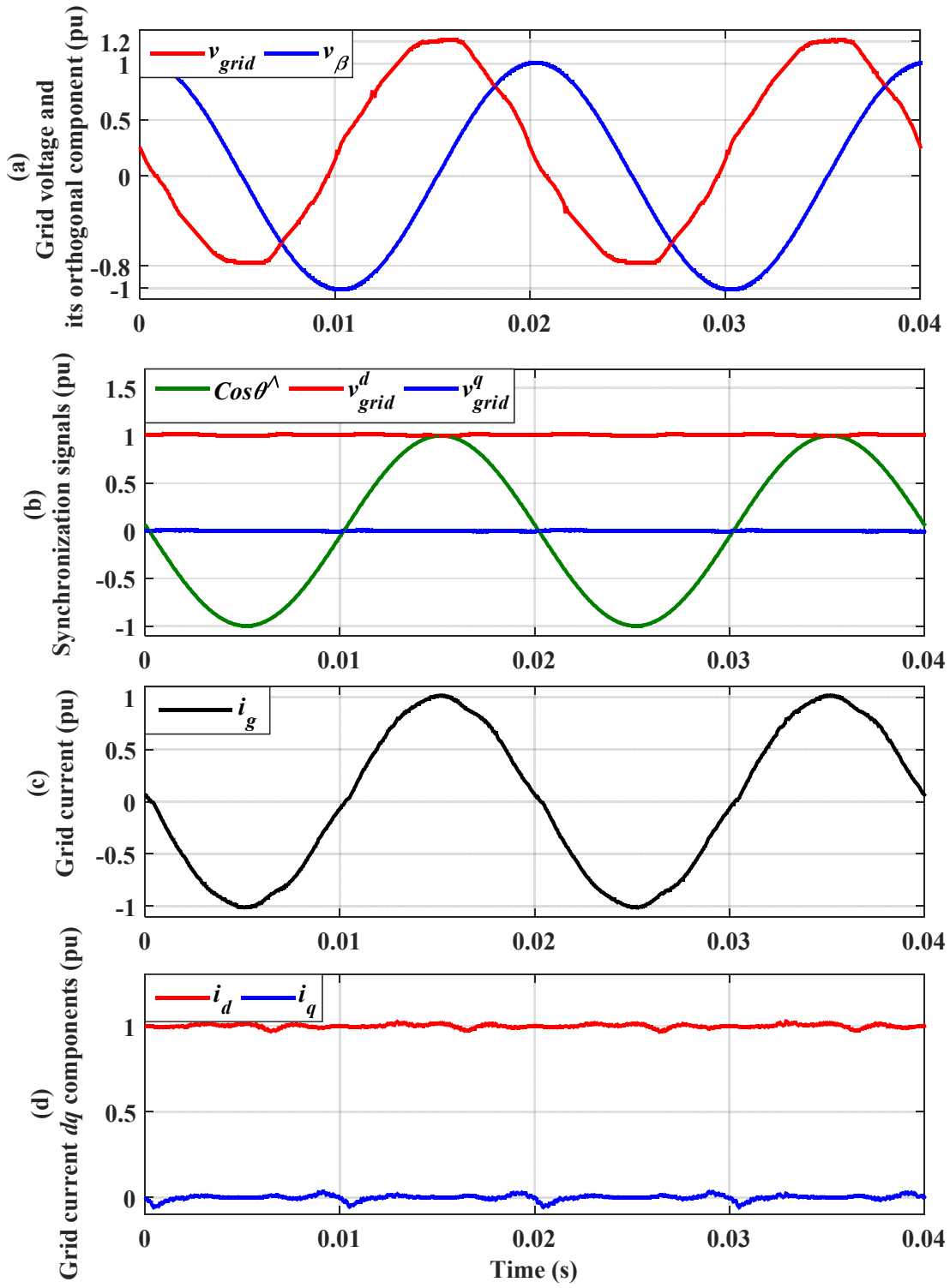


Figure 8.5. Steady-state performance of the grid-connected PV system when the proposed CLPF-SOGI PLL is used with a large dc component of 0.2p.u in the measured grid voltage: (a) The grid voltage and its associated orthogonal component. (b) The synchronization signals associated with the CLPF-SOGI PLL. (c) The grid current. (d) The *d*- and *q*-axes corresponding to the grid current

It can be observed from Figure. 8.5 that, despite the presence of a large dc component in the grid voltage signal, the proposed CLPF-SOGI PLL is still able to achieve a precise estimation of the synchronization signals (i.e., $\theta^{\wedge}$, v_{grid}^{d}, and v_{grid}^{q}). As a result, these accurate synchronization signals directly affect the performance of the simplified *dq* current control strategy of Figure 8.3. Consequently, the grid-connected PV system injects a high-quality current with THD of 2.67% as demonstrated in Figre 8.6.

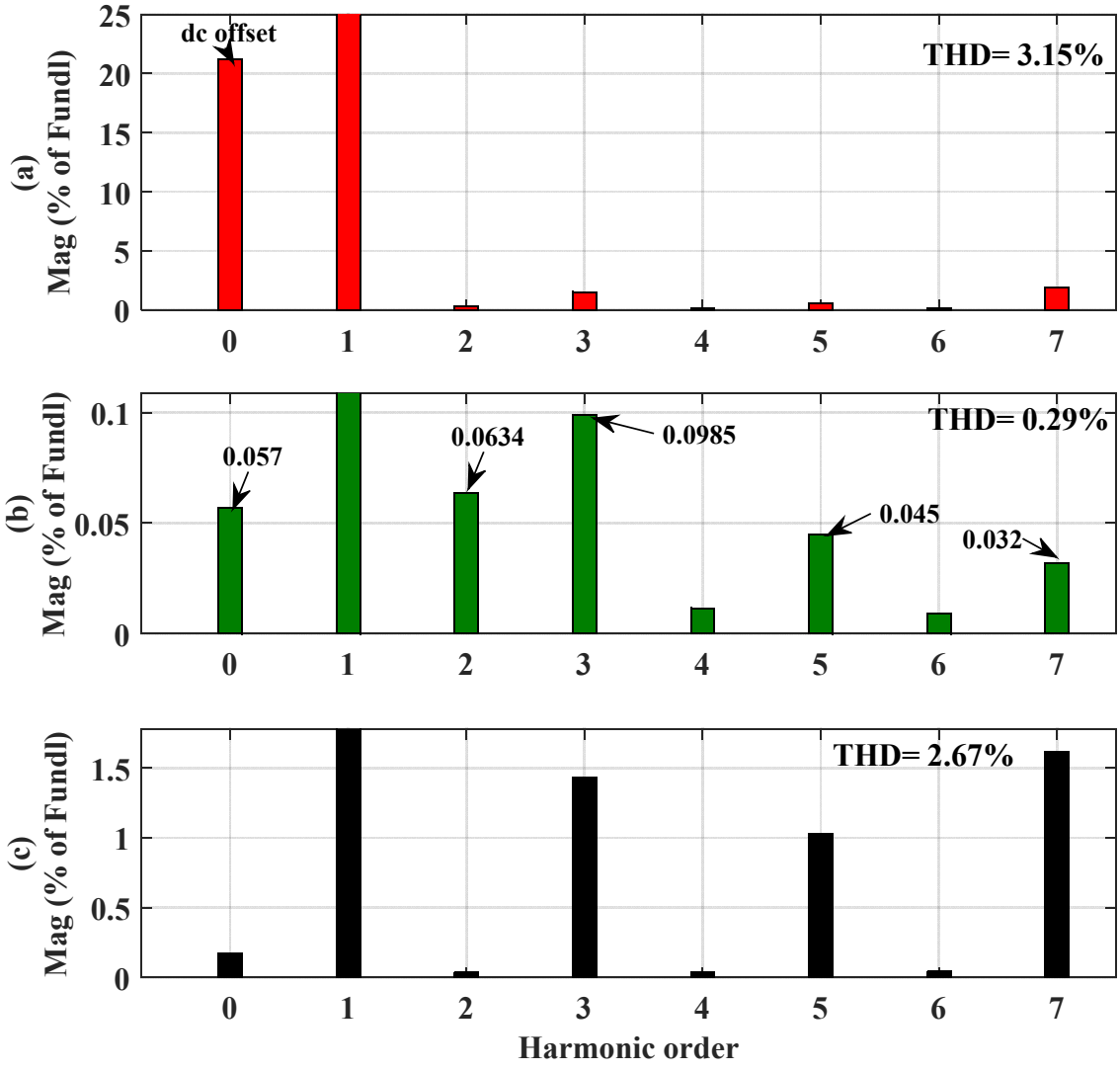


Figure 8.6. Harmonic content of: (a) The utility grid, (b) The reference current. (c) The grid current, under the presence of large dc component in the grid voltage signal and when the proposed CLPF-SOGI PLL is used for synchronization.

On the other hand, the accuracy of the conventional SOGI PLL in estimating these signals is significantly affected by the occurrence of such dc components in the grid voltage signal as presented in Figure 8.7.

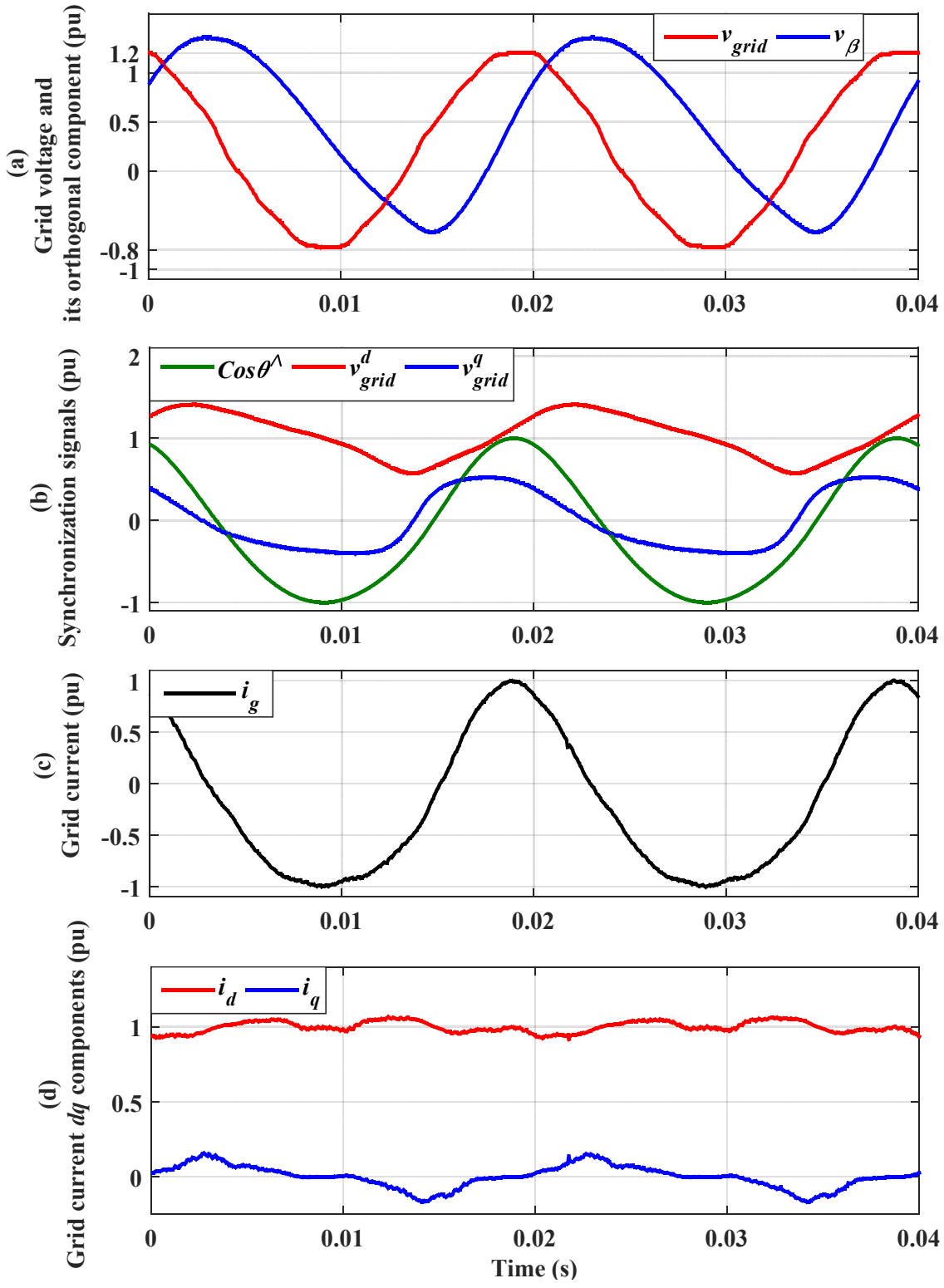


Figure 8.7. Steady-state performance of the grid-connected PV system when the conventional SOGI PLL is used with a large dc component of 0.2p.u in the measured grid voltage: (a) The grid voltage and its associated orthogonal component. (b) The synchronization signals associated with the conventional SOGI PLL. (c) The grid current. (d) The *d*- and *q*-axes corresponding to the grid current

The degraded performance of the conventional SOGI PLL, caused by the dc offset increases distortion on the estimated synchronisation signals. This distortion appears as a second-order harmonic in the generated reference current and consequently, the operation of the *dq* current controller is greatly affected. Thus, as shown in Figure. 8.8, the grid-connected system with a non-robust synchronization method against dc offset, exhibits an extremely low-quality current injection with a THD of 18.43%

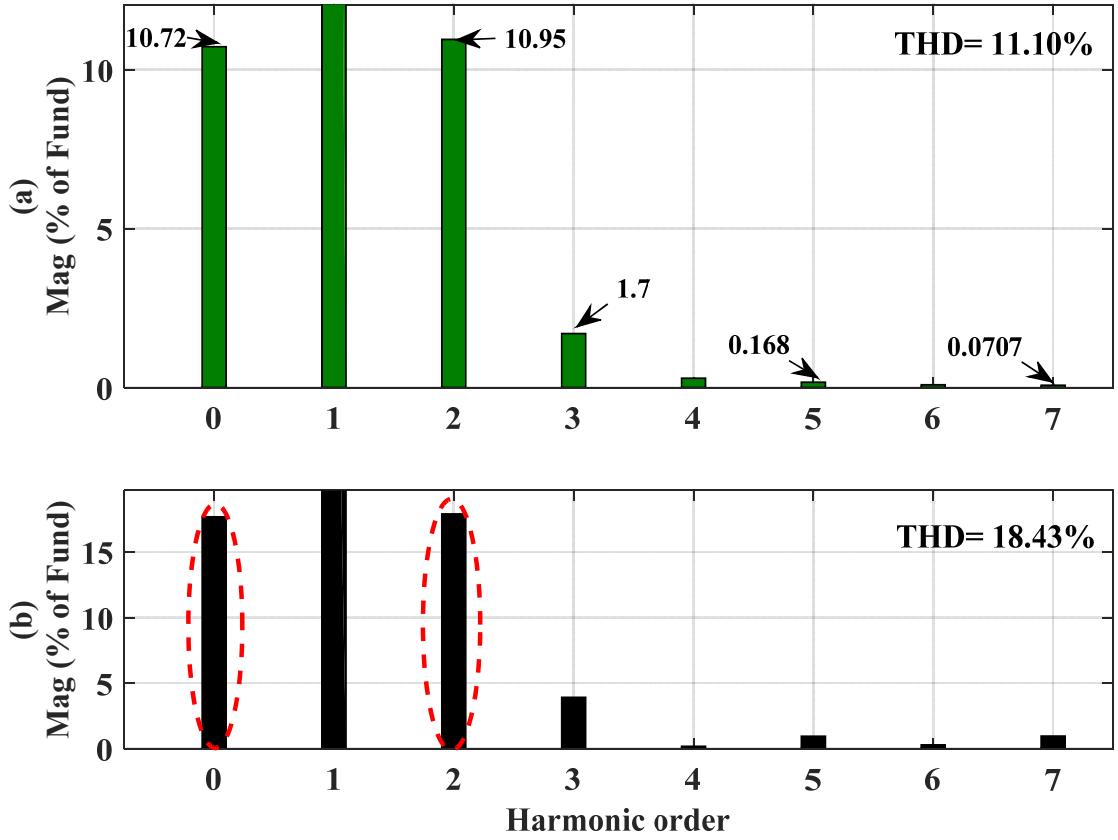


Figure 8.8. Harmonic content of: (a) The reference current. (b) The grid current, under the presence of large dc component in the grid voltage signal and when the conventional SOGI PLL is used for synchronization.

It is important to evaluate the performance of the grid-connected PV inverter system in the case where no deliberate dc component is added to the grid voltage signal. In this case, and due to the A/D conversion process in microcontroller and DSPs, the grid signal still possess some dc offset of 1.6% as shown in Figure. 8.9(a). A comparison of the harmonic content of the grid-connected PV system output current when both conventional and proposed PLL schemes are used is presented in Figure.8.9 (b). The comparison proves the effectiveness of using the robust CLPF-SOGI PLL over the conventional SOGI PLL in improving the quality of the injected current. As can be seen, the inaccuracy of the conventional SOGI PLL in estimating the

synchronization signals results in second-order harmonic appearing in the grid current leading to a low-quality current injection with a THD of 3.03%. On the other hand, the correct estimation of the synchronization signals using the proposed CLPF-SOGI PLL scheme achieves a higher-quality injected current with a THD of 2.63%

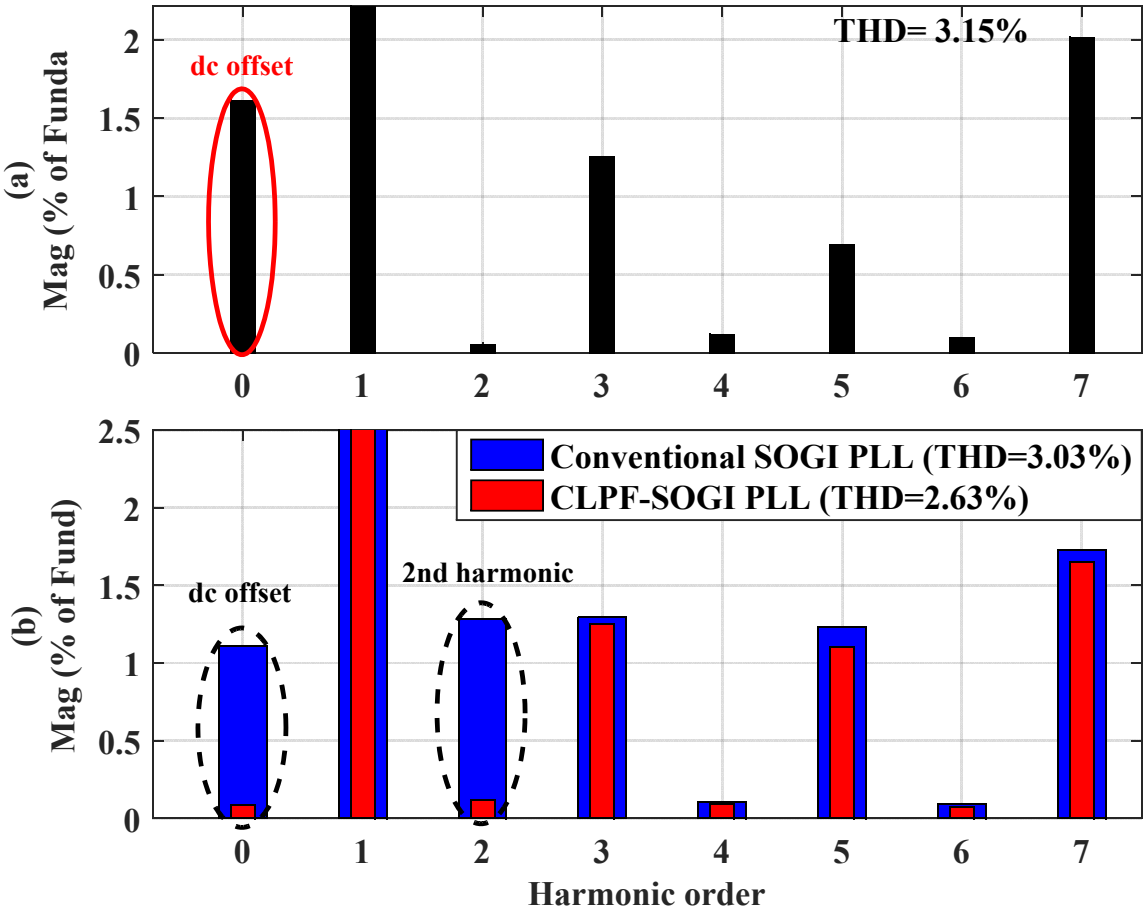


Figure 8.9. Harmonic content of: (a) The actual grid voltage with no added dc offset. (b) The grid current when both conventional SOGI PLL and CLPF-SOGI PLL schemes are used for synchronization

The experimental results in Figures. 8.5-8.9 show the important influence of the proposed CLPF-SOGI PLL in enhancing the power quality of grid-connected PV systems when compared to the conventional SOGI PLL scheme.

8.4 Summary

A simplified *dq* control strategy for the current regulation of grid-connected single-phase VSCs based on the so-called unbalanced *d-q* transformation has been validated experimentally. In order to demonstrate the effectiveness of this strategy in terms of improving the poor dynamic response associated with the conventional *dq* control strategy, the transient performance of both schemes has been experimentally evaluated. Compared to the existing conventional approaches that use phase shifting techniques as a means of creating the required orthogonal current, the proposed *dq* control approach has the advantage that it is not necessary to use such a technique. This results in simplifying the digital implementation of the controller leading to fast and non-oscillatory dynamics. Moreover, despite both schemes being capable of regulating the current and achieving zero steady-state error, in terms of axis-decoupling capability, the proposed scheme shows superior performance compared to the conventional approach.

Additionally, the beneficial effect of the proposed PLL on the power quality of the grid-connected PV system has been also investigated. Experimental results reveal that, when compared with the conventional SOGI PLL, the proposed PLL significantly improves the performance of the grid-connected PV system by enabling a high-quality current injection regardless the level of dc offset being in the input voltage signal.

CHAPTER 9

Thesis Conclusions

9.1 Conclusion from CLPF-SOGI PLL Algorithm

The well-known SOGI-PLL approach has been chosen to perform as a synchronization unit in the control strategy of the single-phase grid-connected PV system described earlier in Chapters 1 and 6. This is because of it is easy to be digitally implemented, has perfect filtering capability and it is adaptive to frequency changes. Despite the wide acceptance and use of this PLL, no comprehensive design strategies to fine-tune its parameters has been described yet. Thus, in chapter 3, a small signal linearized model of the SOGI-PLL structure that significantly simplifies the stability analysis and the parameter design has been developed. The proposed design has chosen the PLL parameters in a way that a high attenuation of -20dB at the lowest disturbance frequency as well as a fast transient response are achieved. To assess the effectiveness of proposed design procedure, extensive simulation and experimental tests under different grid scenarios have been carried out. Simulations were conducted in MATLAB/Simulink environment, while experiments were based on a TMS320F28335 floating-point 150MHz digital signal controller from Texas Instruments. The obtained results have shown that, both fast dynamic response and high attenuation capability were successfully met at different utility grid disturbances when the PLL damping factor and the crossover frequency were selected to be 0.7 and 21.62Hz respectively. Also, they have demonstrated that, a higher attenuation at the disturbance frequencies can be accomplished by selecting a lower crossover frequency, but at the cost of degrading the transient response of the PLL. However, the results reveal the high sensitivity of the conventional SOGI to the presence of dc offset in the input voltage signal. Such components produce undesirable fundamental-frequency ripple in the estimated quantities by the PLL (i.e., utility voltage amplitude, phase angle, and frequency). As a result, more dc current components can be injected to the grid, degrading the quality of the injected current to the grid.

To overcome this problem, a simple yet effective novel strategy referred as to CLPF-SOGI PLL has been proposed and implemented in Chapters 4, 6 and 7. This strategy is based on using an

adaptive two-stage cascaded low-pass filter (CLPF) as an orthogonal signal generator (OSG) to produce an orthogonal signal free of any dc offset. The effectiveness of the proposed CLPF-SOGI PLL scheme has been verified through analytical, simulation and experimental tests. In addition, the proposed PLL method has been compared with two well-known approaches used to address the problem of dc offset in the SOGI-PLL algorithm. The results obtained have observed that, in addition to its ability to reject the dc offset, the proposed CLPF-SOGI offers the best degree of attenuation of high-frequency harmonics when compared to the other alternative based SOGI techniques. For instant, both conventional SOGI and Karimi's method offer transfer functions whose magnitude- frequency response decays at a rate of -40.4dB/dec at high-frequencies. While, the transfer function of Ciobotaru's method decays with a slope of -22.7dB/dec at high-frequencies, which seriously degrades the high-frequency characteristics of the system. In contrast, the proposed CLPF-SOGI offers a transfer function with a slope of -59dB/dec and therefore, produces superior harmonic attenuation capability when compared to the other three methods studied in Chapter 4.

Additionally, the beneficial effect of the use of an accurate synchronization method on power quality of the grid-connected PV system has been also investigated. Simulation and experimental results have shown that, when compared with the conventional SOGI PLL, the proposed CLPF-SOGI PLL significantly improves the performance of the grid-connected PV system by enabling a high-quality current injection regardless the level of dc offset in the grid voltage signal. For example, in Chapter 8 the immunity of the grid-connected PV system to a dc offset has been experimentally examined. A case study where an excessively large dc component of 0.2 p.u was added to the grid voltage signal has been conducted. Results have shown that, despite the presence of a large dc component in the grid voltage signal, the proposed CLPF-SOGI PLL is still able to achieve a precise estimation of the synchronization signals, and as a result, the grid-connected PV system injects a high-quality current with a THD of 2.67%, which remains within the limits provided in Table 1-6. In this test, it has been found that there was no dc current component injected to the grid caused by such dc offset. On the other hand, the inaccuracy of the conventional SOGI PLL in estimating the synchronization signals results in both dc current components and second-order harmonic in the injected grid current. This leads to an extremely low-quality current injection with dc current component of 17%, and a THD of 18.43%, exceeding the limits provided in Table 1-5 and 1-6 respectively. Another case study where no dc offset component was added to the utility grid signal has been carried out.

In this case, and due to the A/D conversion process in microcontroller and DSPs, the grid signal still possess some dc offset of 1.6%. A comparison of the harmonic content of the grid-connected PV system output current when both conventional and proposed CLPF-SOGI PLL schemes are used proves the effectiveness of using the robust CLPF-SOGI PLL over the conventional SOGI PLL in improving the quality of the injected current. The inaccuracy of the conventional SOGI PLL in estimating the synchronization signals results in a dc current injection of 1.15% and a second-order harmonic of 1.3% appearing in the grid current leading to a low-quality current injection with a THD of 3.03%. On the other hand, the correct estimation of the synchronization signals using the proposed CLPF-SOGI PLL scheme achieves a higher-quality injected current with a THD of 2.63%, with no dc current injection caused by such dc offset. In general, both simulation and experimental studies proves that; the accurate synchronization is a key aspect for the power quality of the grid-connected PV systems.

9.2 Conclusion from Grid Current Control

Generally, grid-connected PV inverter systems need a current control scheme to regulate their output current as well as to provide a high-quality power exchange with the utility grid. Because of their simple digital implementation, PI controllers in the stationary reference frame are well-known as the most traditional approaches used for current controlled single-phase inverters. However, due to the the time-varying nature of quantity being controlled, PI-controllers have a major drawback of failure to track a sinusoidal reference without steady-state error. This disadvantage however, can be effectively overcome by instead implementing the PI-controller in the synchronous reference frame (i.e., *dq* frame). In such a way, the ac (time varying) quantities appear as dc (time invariant) quantities in the steady-state. This allows the controller to be designed as for dc–dc converters, presenting infinite control gain at the steady-state operating point, and leading to zero steady-state error. Generally speaking, designing a PI-controller using the concept of *dq* reference frame for single-phase systems is more complicated than for three-phase cases. This is because the use of the *dq* controllers in single-phase systems is not possible unless a fictitious orthogonal component is produced to form a two-axis environment (i.e.,$\alpha\beta$). A simple and direct way of generating this orthogonal component (β) can be achieved using the above mentioned CLPF approach. Therefore, and in order to perform the *dq* current controller, a mathematical model for the adopted single-phase system has been provided in Chapter 5. This is then followed by a design procedure of the current control loop to fine-tune its parameters and evaluate the stability of the whole closed-loop system. The

performance of the *dq* current controller based on CLPF has been experimentally evaluated in Chapter 8. Despite the CLPF-*dq* controller being able to track the demand current with zero steady-state error, the conducted study has revealed a major shortcoming represented in its inability to have a fast response. It has been found that, the corresponding *d*- axis of the current changes to track the reference value changes but, experiences non-negligible transients for approximately one cycle (20ms) due to the phase shifting techniques used in generating the orthogonal signal.

To overcome this drawback associated with the conventional *dq* controller based CLPF, a novel quasi-*dq* current controller approach referred as to the simplified *dq* current controller has been proposed in Chapter 5. This is based on the so-called unbalanced *d-q* transformation which was originally performed for single-phase PLL systems. In this approach, the generation of such an orthogonal component is not required since the β-axis component of the controller is forced to zero. In order to demonstrate the effectiveness of this strategy to improve the poor dynamic response of the CLPF-*dq* controller, the transient performance of both schemes has been experimentally compared. It has been observed that, contrary to the conventional *dq* controller, subject to each *d*-axis step change, the system experiences very short and negligible transients, and the reference value of it is tracked in about 2ms with zero steady-state error.

9.3 Future Work

The performance of the current controller for grid-connected PV systems can be significantly enhanced if the grid synchronization is more robust to highly distorted grid voltages. Taking the SOGI-PLL as an example, this can be simply achieved by significantly reducing the system band-width (i.e., having a low-gain PLL). However, this degrades the system dynamics and is not acceptable.

By developing an adaptive PLL algorithm, the fixed-gains of the PLL system (k_p and k_i) which have been used in this thesis can be replaced by adaptation mechanism. This adaptive algorithm has to take advantage of the positive attributes of the implementation of both low and high-gains PLL by switching smoothly between low and high gains as the operational conditions dictate. For example, in the steady-state conditions, the low-gains (reduced band-width) will be used to guarantee that the best steady-state performance is achieved when compared to the steady-state performance with the fixed low-gains. Similarly, when a disturbance occurs, the

adaptive PLL algorithm will use the high-gains to have a fast transient when compared to the transient performance of the fixed-high gains PLL.

By implementing such a PLL, an improved dynamic response, high accuracy and noise immunity can be achieved.

9.4 Research Outcomes

The research work carried out in this thesis has resulted in two publications in IEEE

- A. M. Mnider, D. J. Atkinson, M. Dahidah, and M. Armstrong, "A simplified DQ controller for single-phase grid-connected PV inverters." *In the 7th International Renewable Energy Congress (IREC)* 2016, pp. 1-6.
- M. Mnider, D. J. Atkinson, M. Dahidah, Y. B. Zbede, and M. Armstrong, "A programmable cascaded LPF based PLL scheme for single-phase grid-connected inverters." *In the 7th International Renewable Energy Congress (IREC)* 2016, pp. 1-6.

In addition, at the time of submission, a paper presenting the outcomes from the practical research has been submitted for review to IEEE Transaction on Power Electronics.

Appendix A : Five-level Diode-clamped Inverter

A.1 Introduction

The basic concept to perform power inversion in multilevel inverters is based on a series connection of low rating power electronic devices with several low capacitive voltage sources. This is to synthesize a desired AC stepped output voltage waveform. Furthermore, by adding more levels on the DC link side, the synthesized AC output waveform adds more steps. This can produce a more refined staircase wave with reduced harmonic distortion, as a result, reducing the filter requirements [31, 35, 40, 45].

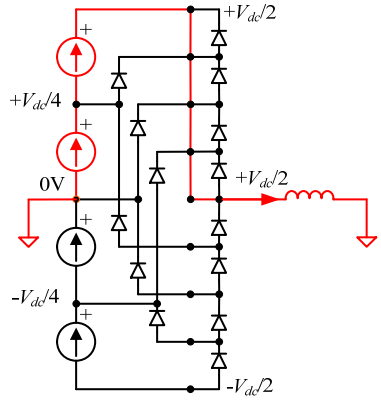
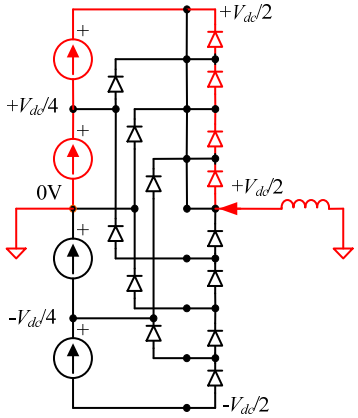
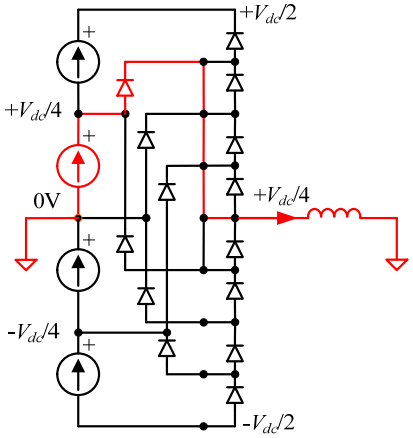
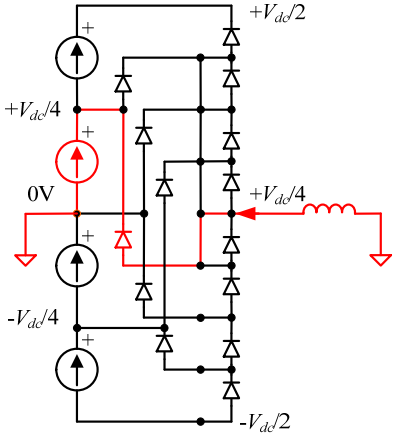
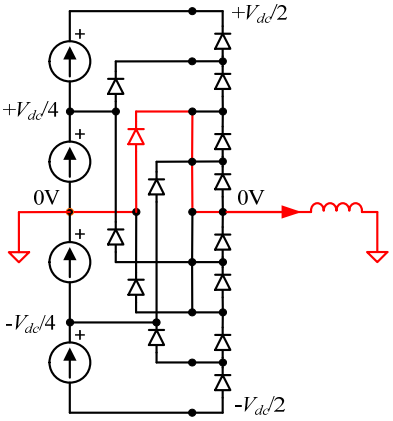
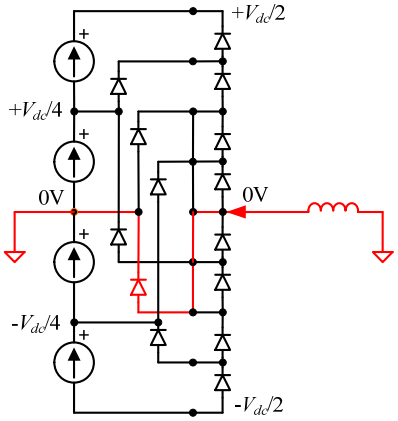
In this thesis, a five-level diode-clamped inverter has been chosen as a part of the proposed single-phase grid-connected PV system. The main reason is to study the opportunity of reducing the output passive filter size by adopting such an inverter when compared to the conventional tow-level inverter.

A.2 Switching States of the Five-level Inverter

The relationship between switch operating statuses, current flowing through the dc-link capacitors and the clamping diodes, and the inverter terminal voltage Van is tabulated in Table A-1. Based on Table A-1; Figure. A.1 shows the five different switching states for the output phase voltage of the inverter. The obtained equivalent circuit is highlighted to show how the output node (a) is linked to the positive, neutral, and negative nodes of the DC side circuit.

Table A-1: Switching states, and Magnitude of output voltage of a five-level diode-clamped inverter

S NO	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4	C_1	C_2	C_3	C_4	d_1	d_2	d_3	d_4	d_5	d_6	V_{an}
1	1	1	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	$V_{dc}/2$
2	0	1	1	1	1	0	0	0	0	1	0	0	1	1	0	0	0	0	$V_{dc}/4$
3	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
4	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	0	1	1	$-V_{dc}/4$
5	0	0	0	0	1	1	1	1	0	0	1	1	0	0	0	0	0	0	$-V_{dc}/2$
Note: '1' indicates that switch is On, capacitor or diode are carrying current, while '0' means the opposite.																			

Switching state (1) ($V_{an}= V_{dc}/2$)	
$i_{c1}=i_{c2}=i_L$ & $i_{c3}=i_4=0$	$i_{c1}=i_{c2}=i_L$ & $i_{c3}=i_4=0$
	
Switching state (2) ($V_{an}= V_{dc}/4$)	
$i_{c1}= i_{c3}=i_4=0$ & $i_{c2}=i_L$	$i_{c1}= i_{c3}=i_4=0$ & $i_{c2}=i_L$
	
Inverter State (3) ($V_{an}= 0$)	
$i_{c1}=i_{c2}= i_{c3}=i_4=0$	$i_{c1}=i_{c2}= i_{c3}=i_4=0$
	

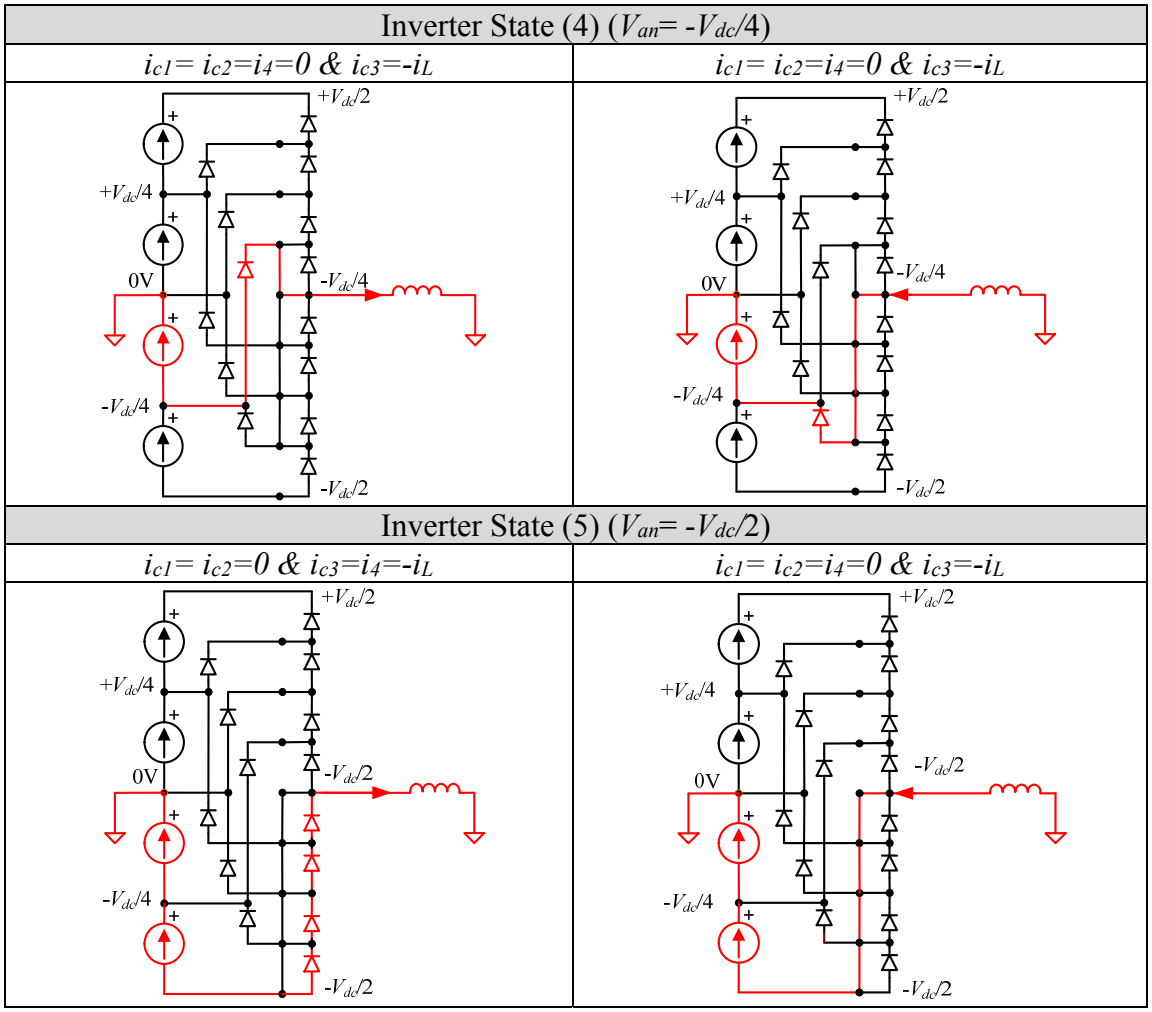


Figure. A.1 Detailed switching states of a five-level inverter

A.3 Level-shifted PWM Switching Strategies

The three different LS-PWM schemes described earlier in Chapter 1 are shown in Figure.A-2.

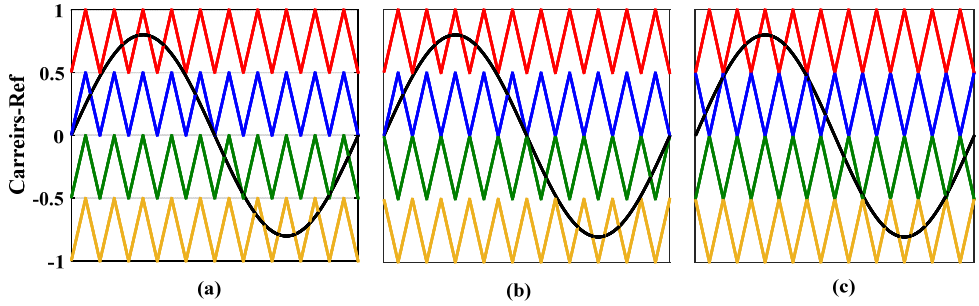


Figure. A.2 LS-PWM carrier arrangements: (a) IPD, (b) POD, and (c) APOD

To assess the performance of the five-level inverter when it is controlled using the IPD-PWM scheme, a simulation model is developed in Matlab/Simulink environment as shown in Figure. A.3.This is followed by a detailed control diagram of the IPD-PWM shown in Figure.A-4.

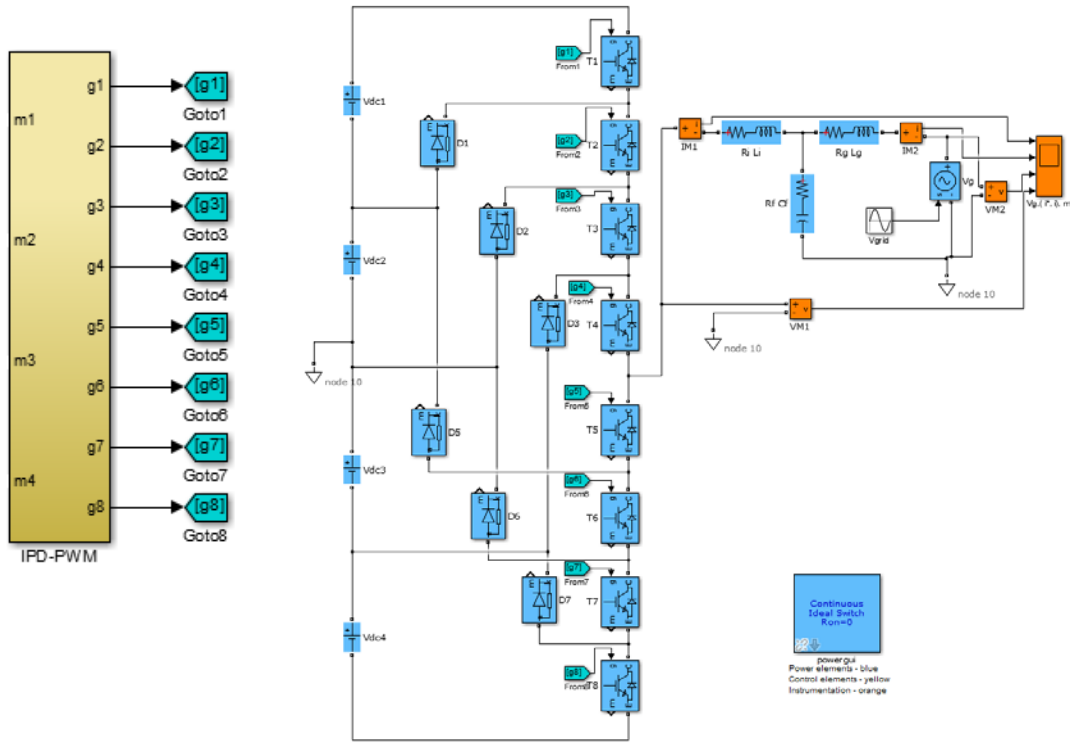


Figure. A.3 Simulink model of the five-level diode-clamped inverter with its associated IPD-PWM

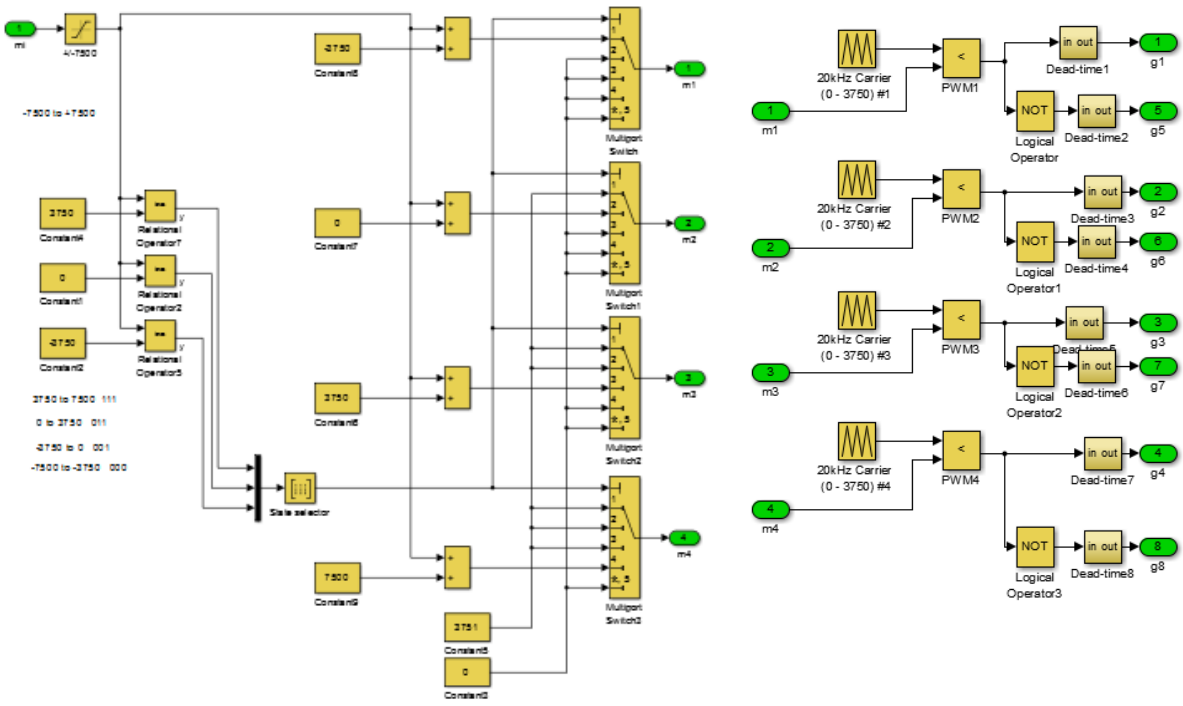


Figure. A.4 Detailed Simulink block of IPD-PWM

Figure.A-5 illustrates the principle of the IPD-PWM when it is applied for the five-level inverter. The gate signals g_1, g_2, g_3, and g_4 for the top four switches S_1, S_2, S_3 and S_4 of Figure. A-3, are generated at the intersections of the carrier waves and the sinusoidal reference m1-m4, respectively. The gatings for the bottom four devices S_1', S_2', S_3', and S_4', are complementary to g_1, g_2, g_3, and g_4.

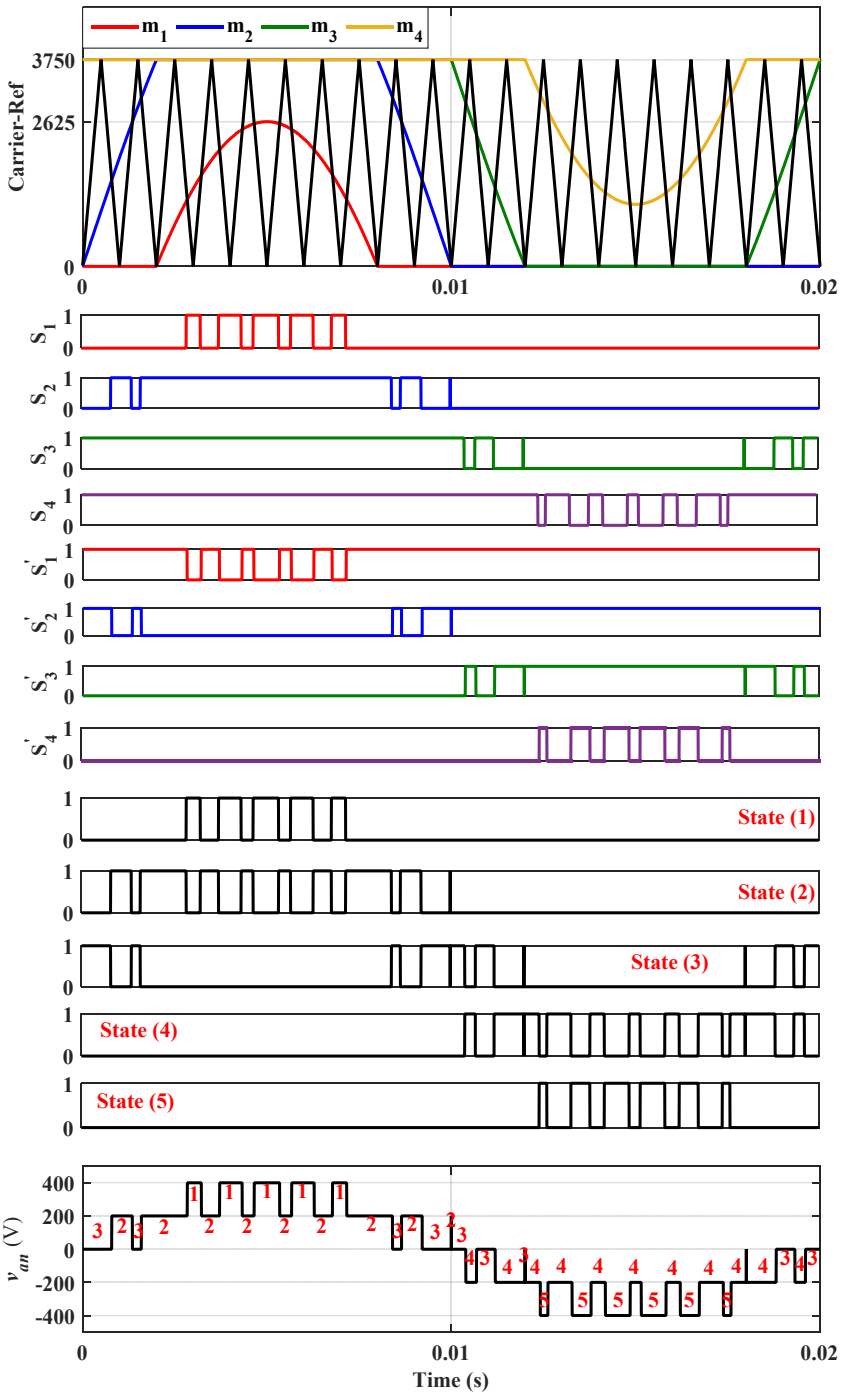
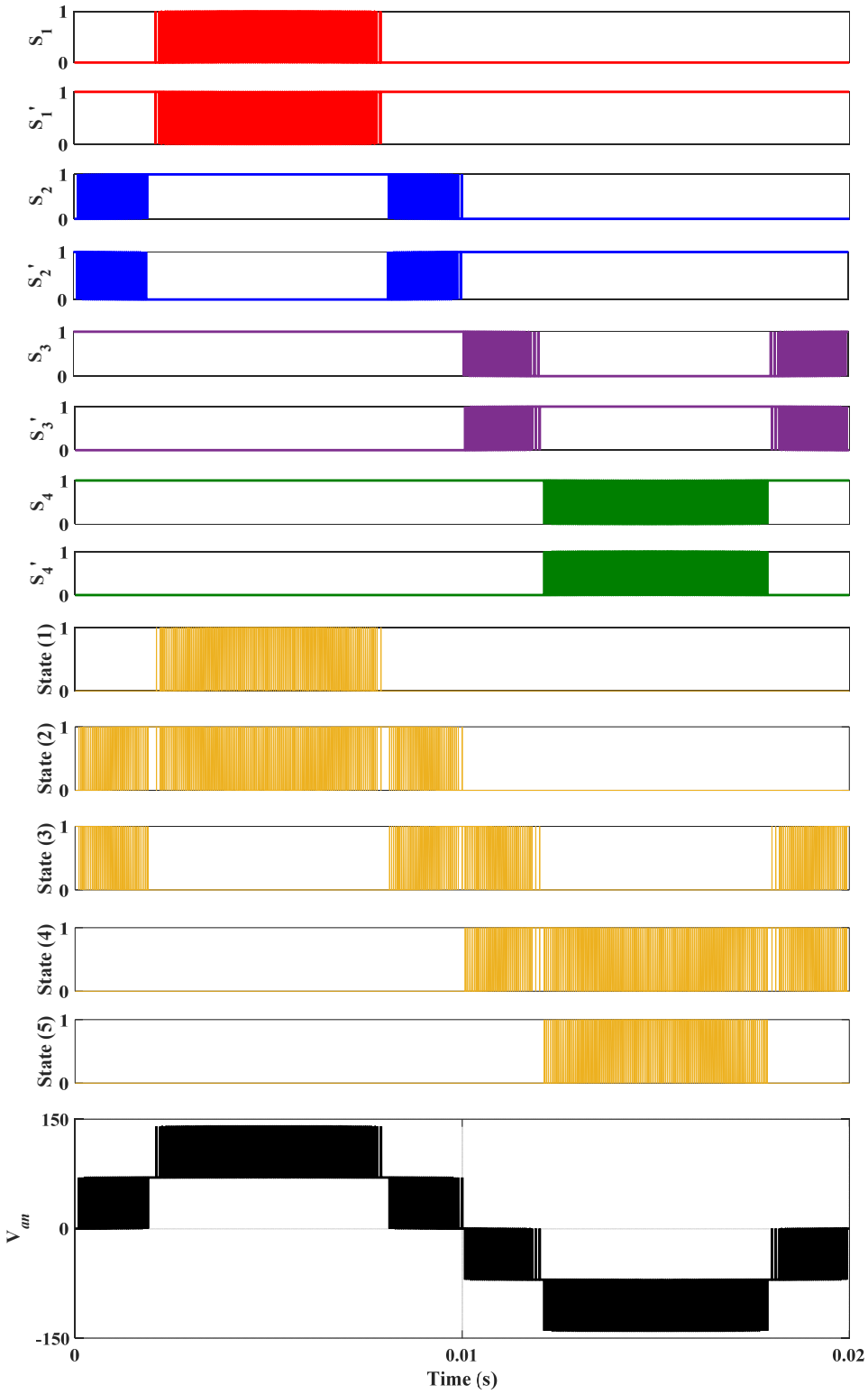
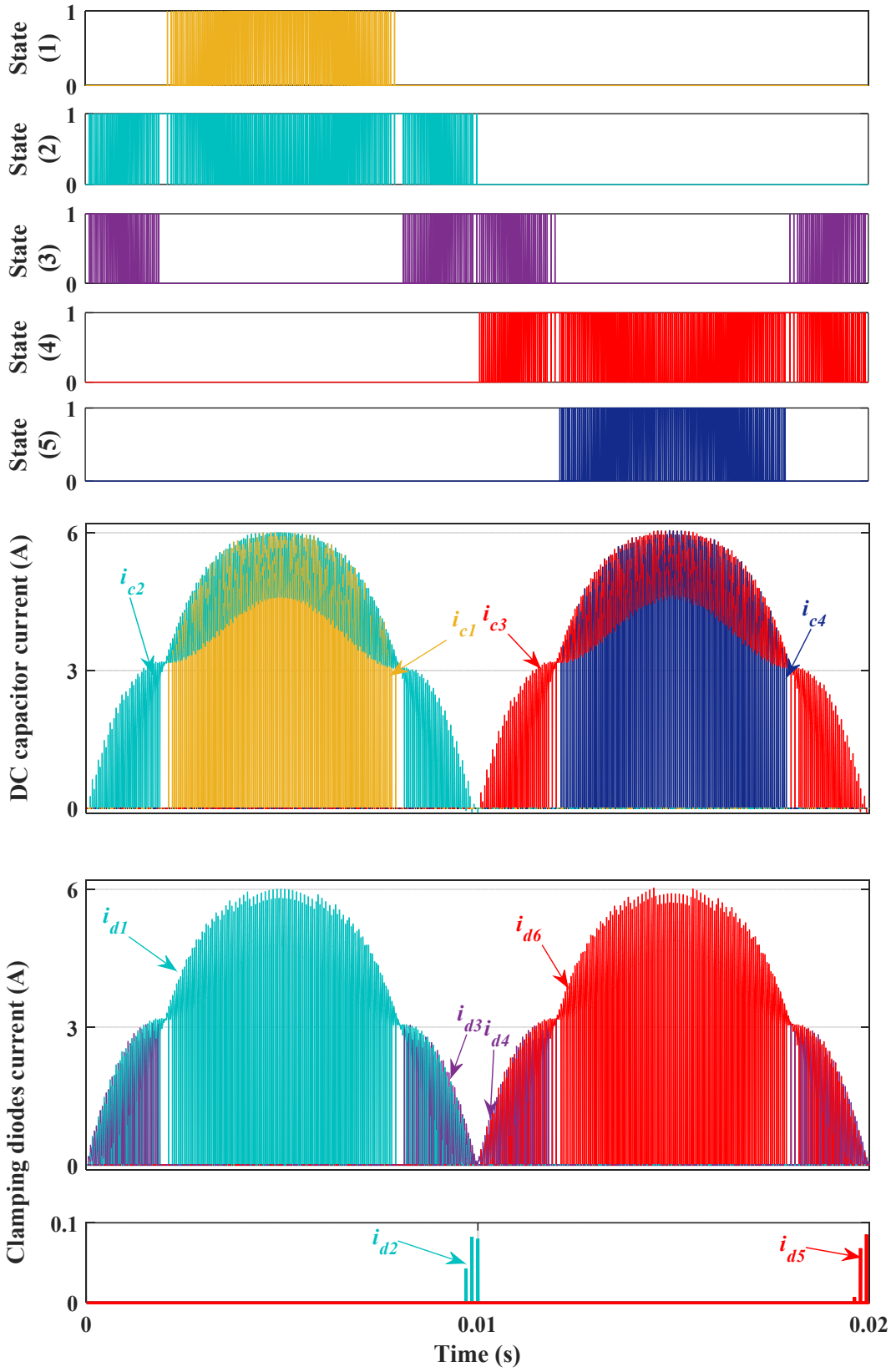


Figure. A.5. Simulated waveforms of the five-level diode-clamped inverter using IPD-PWM (f_m = 50 Hz, f_{cr} = 1000 Hz, m_a = 0.85)

More detailed waveforms of the principle of the IPD-PWM when applied to the five-level inverter with resistive load of 22 Ω are illustrated in Figure.A-6. In this example, the modulation index was set to 0.85, and the switching frequency to 20 kHz.




State (1)
State (2)
State (3)
State (4)
State (5)
1
0
DC capacitor current (A)
6
3
0
i_{c2}
i_{c1}
i_{c3}
i_{c4}
Clamping diodes current (A)
i_{d1}
i_{d6}
i_{d3}
i_{d4}
0.1
i_{d2}
i_{d5}
0
0.01
0.02
Time (s)

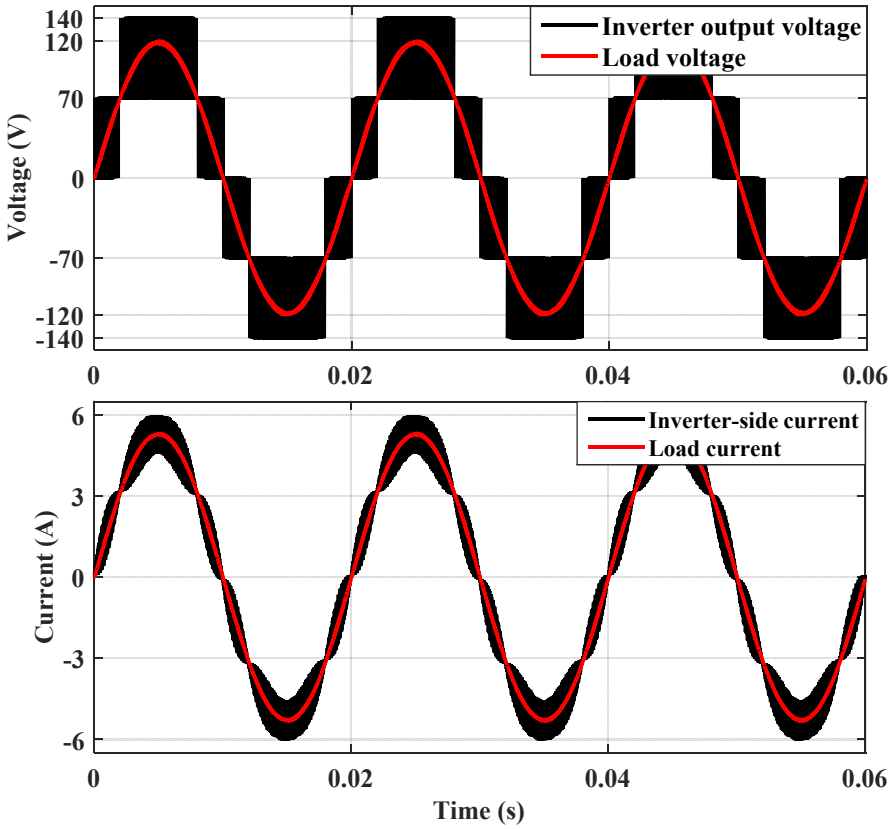


Figure. A.6 More detailed simulated waveforms of the five-level diode-clamped inverter with a resistive load of 22 Ω using IPD-PWM (fsw = 20 kHz, ma = 0.85)

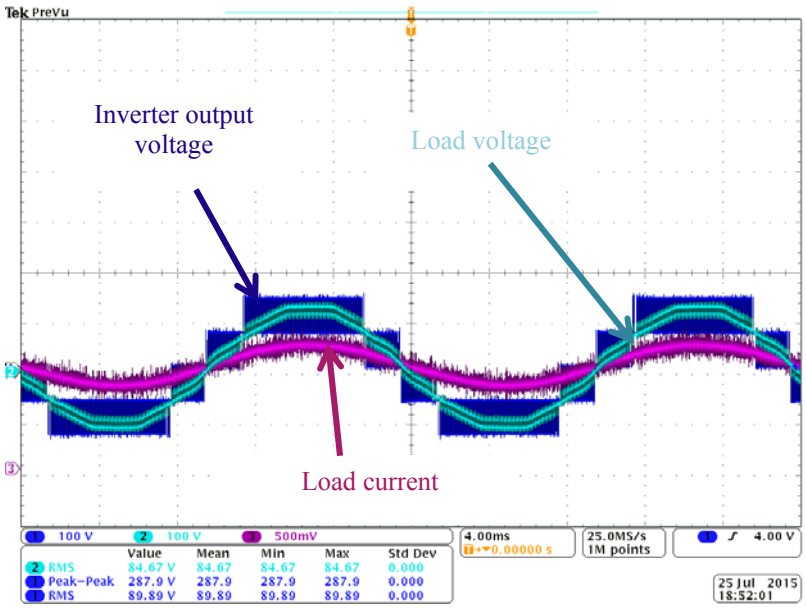


Figure. A.7 Sample of experimental waveforms of the five-level diode-clamped inverter using IPD modulation

Appendix B : LCL Filter Design

B.1 LCL Filter Analysis and Design Consideration

The LCL-filter equivalent circuit diagram is shown in Figure.B-1, where V_{inv} and V_{grid} are inverter and grid voltage, respectively. The filter is made up of an inverter-side inductor L_1, a parallel capacitor C_f, and a grid-side inductor L_2. The equivalent series resistance (ESR) of L_1 and L_2 are represented by R_1 and R_2 respectively. A damping resistor R_d, is required for damping the resonance ripple.

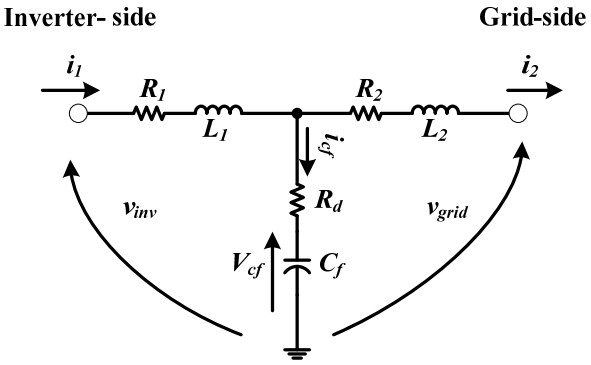


Figure. B-1 Equivalent single-phase LCL filter

The current ripple attenuation at the switching frequency is calculated by taking into consideration that; at high frequencies, the inverter acts as a harmonic generator, while the grid voltage can be assumed as an ideal sinusoidal voltage source capable of supplying a constant voltage/current only at fundamental frequency. Thus, at the switching frequency, the inverter voltage harmonic,$v_{inv}(h_{sw}) \neq 0$, while the grid voltage harmonic, $v_{grid}(h_{sw}) = 0$ (short-circuit). Based on this, (neglecting damping) and assuming that the value of R_1 and R_2 are small enough to be neglected, the ripple attenuation passing from the inverter-side to the grid-side can be computed with the following steps:

$$\begin{aligned} \boldsymbol{V_{inv}(s) = SL_1 i_1(s) + V_{cf}(s)} \\ \boldsymbol{V_{cf}(s) = SL_2 i_2(s)\,,\ \ (v_{grid}(s) = 0)} \end{aligned} \tag{B.1}$$

$$i_1(s) = I_{cf}(s) + i_2(s) = SC_f V_{cf}(s) + i_2(s) = S^2 C_f L_2 i_2(s) + i_2(s) \tag{B.2}$$

$$V_{inv}(s) = S^3 C_f L_1 L_2 i_2(s) + S(L_1 + L_2) i_2(s) \tag{B.3}$$

$$H(s)_{v_{inv}\to i_2} = \frac{i_2(s)}{v_{inv}(s)} = \frac{1}{C_f L_1 L_2 S^3 + (L_1 + L_2)S} \tag{B.4}$$

$$H(s)_{i_2\to i_1} = \frac{i_2(s)}{i_1(s)} = \frac{1}{C_f L_2 S^2 + 1} \tag{B.5}$$

However, system including LCL filter is of third-order, and there exists a higher ripple response at the resonant frequency of the filter. To maintain stability and take an advantage of the high attenuation provided by the LCL filter, this higher ripple produced by the resonance of the filter must be properly damped. The most common method is to insert a damping resistor R_d in series with the capacitor shunt branch of the filter C_f as shown in Figure.B-1. Then, with some simple algebraic manipulations, the transfer functions of (B.4) and (B.5) with damping resistance become

$$\boldsymbol{H_D(s)_{v_{inv}\to i_2}} = \frac{\boldsymbol{i_2(s)}}{\boldsymbol{v_{inv}(s)}} = \frac{\boldsymbol{R_d C_f S + 1}}{\boldsymbol{L_1 C_f L_2 S^3 + (L_1 + L_2) R_f C_f S^2 + (L_1 + L_2) S}} \tag{B.6}$$

$$H_D(s)_{i_2\to i_1} = \frac{i_2(s)}{i_1(s)} = \frac{R_d C_f S + 1}{C_f L_2 S^2 + R_d C_f S + 1} \tag{B.7}$$

When designing the LCL filter, there are some restrictions on the parameter values should be considered [143]:

a) The value of the inverter-side inductor L_1 is designed in order to limit the ripple of the converter-side current. Moreover, the inductor should be properly designed so as not to saturate and hence, the correct inductor choice is a trade-off between ripple reduction and inductor size. Accepting high values of the current ripple may lead to saturation problems in the core of inductors. The permissible ripple current is generally lower than 20% of the rated current.
b) The capacitor value C_f is limited to the decrease of the capacitive reactive power at rated load (generally less than 5%).
c) The upper limit to the total inductance (L_1+L_2) should not exceed 0.1pu in order to limit the voltage drop across the inductances [144].
d) To avoid resonance problems in the lower and upper parts of the harmonic spectrum, the resonance frequency f_{res} should be in a range of ten times the fundamental frequency and one-half of the switching.

e) The possible instability of the current control loop is caused by the zero impedance that the LCL filters offers at its resonance frequency. The proper damping of these dynamics can be achieved by modifying the filter structure with the addition of passive elements (passive damping) or by acting on the parameters or on the structure of the controller that manage the power converter (active damping) [143]. In this LCL filter design, and to avoid the resonance phenomenon 'oscillation', passive damping is used bearing in mind that losses cannot be as high as to reduce efficiency [145, 146].

f) IEEE 519-2014 recommends that harmonics higher than the 35th should be limited. For a grid-tied inverter system, if the short-circuit current of power system is lower than 20 times the nominal grid-side fundamental current, then each harmonic current of higher than the 35th should be less than 0.3% of the rated fundamental current. Also, THD should be less than 5% [147].

B.2 LCL Filter Design Procedure

Based on the aforementioned desired limits, the filter can be designed with the following six-step-by-step procedure.

1) Choose the desired current ripple (Δ) on the inverter side in order to design the inverter-side inductor L_1. In the case where the five-level single phase diode-clamped inverter is adopted as shown in Figure.B-2, the inverter side inductor can be determined as follows

$$\boldsymbol{L_1 = \frac{V_{inv} - V_{grid}}{2\Delta I_{1_{max}}} m T_{sw} = \frac{\frac{V_{dc}}{4}(1-m)}{2\Delta I_{1_{max}}} \frac{m}{f_{sw}}} \quad \text{(B.8)}$$

where: f_{sw} is the inverter switching frequency, m is the inverter modulation index. From (B.8), it is clear that the maximum peak-to-peak current ripple ($2\Delta I_{1_{max}}$) occurs at m= 0.5, thus

$$\boldsymbol{L_1 \approx \frac{V_{dc}}{32\Delta I_{1_{max}} f_{sw}}} \quad \text{(B.9)}$$

In the case where a two-level inverter is used as shown in Figure.B-3, the inverter side inductor can be calculated using the following equation

$$\boldsymbol{L_1 = \frac{V_{dc}(1-m)}{2\Delta I_{1_{max}}} \frac{m}{f_{sw}} \approx \frac{V_{dc}}{8\Delta I_{1_{max}} f_{sw}}} \quad \text{(B.10)}$$

It is clear that, as a result of adopting the five-level inverter, the requirements of the output AC filter can be effectively reduced by four times when compared to the two-level topology for the same system.

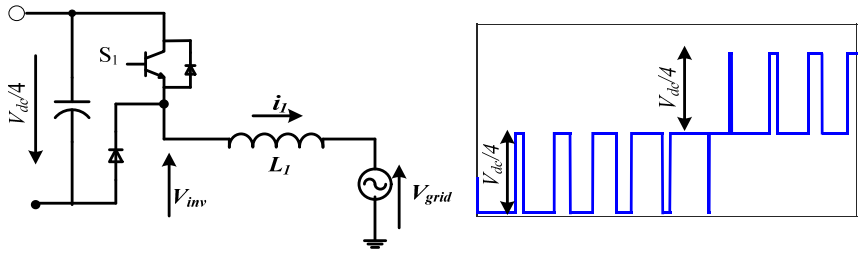


Figure. B-2 Simplified circuit of the five-level diode-clamped inverter with part of its output voltage

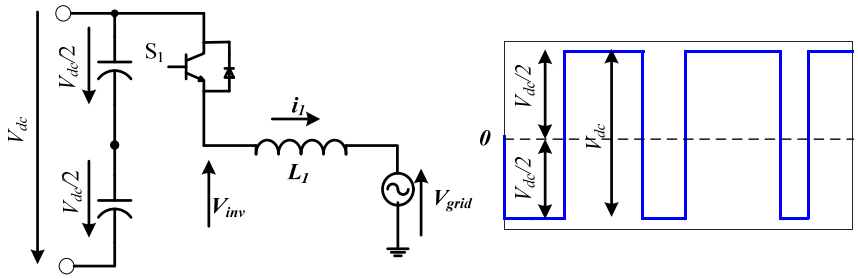


Figure. B-3 Simplified circuit of the two-level inverter with part of its output voltage

2) Select the reactive power absorbed by the filter capacitance in the rated conditions to determine the capacitor value. The highest capacitor value is limited by the condition where its consumption reactive power should be no more than ($x \leq 5\%$) of the rated power.

$$\boldsymbol{C_f = \frac{Q_{re}}{\pi f_g V_{grid}^2} = \frac{xP_n}{2\pi f_g V_{grid}^2} = xC_b} \tag{B.11}$$

where: Q_{re} is the reactive power absorbed by filter capacitor; P_n is the rated power; f_g is the fundamental frequency, and $\boldsymbol{C_b}$ is the base capacitance.

3) The grid side inductor L_2 mainly depends on the objective to attenuate each harmonic around the switching frequency down to 0.3%. The ripple attenuation of the current at the switching frequency is given by

$$\boldsymbol{k_a = \frac{i_2(h_{sw})}{i_1(h_{sw})} = \frac{1}{|r[1 - L_1 C_b \omega_{sw}{}^2 x] + 1|}} \tag{B.12}$$

And hence:

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f {\omega_{sw}}^2} \tag{B.13}$$

where: $i_2(h_{sw})$ is the grid-side current ripple at the switching frequency; $i_1(h_{sw})$ is the inverter-side current ripple at the switching frequency and ω_{sw} is the switching frequency. If the sum of the two inductances does not respect condition (c), another attenuation level should be chosen, or another value for the absorbed reactive power should be selected as per step 2.

4) Verify the resonance frequency f_{res} obtained. This can be calculated using the following

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{B.14}$$

The resonant frequency is limited by condition (d). If it is not in the specified range, the reactive power absorbed returned in step 2 or the attention factor returned in step 3 should be changed.

5) To avoid resonance oscillation, set the damping according to condition (e). The damping resistance R_d should be one third of the filter capacitor at resonant frequency [143, 148].

$$R_d = \frac{1}{3\ \omega_{res} C_f} \tag{B.15}$$

6. Verify harmonics current profile to satisfy condition (f). If the condition is not satisfied, the design procedure returns to step 1. The ripple attenuation of the current at the switching frequency when considering the damping is given by

$$k_{a(d)} = \frac{i_2(h_{sw})}{i_1(h_{sw})} = \frac{R_d C_f \omega_{sw} + 1}{C_f L_2 {\omega_{sw}}^2 + R_d C_f \omega_{sw} + 1} \tag{B.16}$$

The step-by-step procedure has been applied to a single-phase grid-connected five-level diode clamped inverter based on the parameters shown in Table B-1 to obtain the LCL filter parameters as following:

Table B-1: Inverter System Parameters

Parameter	Symbol	Value (unit)
Grid fundamental frequency	f_g	50Hz
Inverter switching frequency	f_{sw}	20kHz
System rated power	P_n	350W
System rated voltage	V_{grid}	90V
DC link voltage	V_{dc}	280V

1) Adopting a 10% ripple of the rated current for the design parameters is given by, $I_{1_{max}} = \left(\sqrt{2}\frac{P_n}{V_{grid}}\right) = 5.4A$, (B.9) gives an inductance L_1=0.81mH. By adding the LC part, the aim is selected to reduce the current ripple from 10% to 2% (ripple attenuation k_a= 0.2) as will be demonstrated in step 6.
2) Using the power rating of the inverter P_n and the grid voltage V_{grid}, the base impedance Z_b= $\frac{v_{grid}^2}{P_n}$ =23Ω, the base capacitance C_b is 137μF and the base inductance L_b is 73mH. Using (B.11) and considering a value of $x = 2.5\%$, the resultant capacitor value C_f=3.425 μF.
3) Setting the desired current ripple attenuation factor k_a =20%, with respect to the ripple on the converter side, using (B.13) a value of L_2 = 0.11mH is calculated. It is worth mentioning that, since (B.13) does not take into account the losses and damping. Thus, the desired attenuation *k*a should be multiplied by a factor that takes into account the losses and damping [143]. In this case, by taking in to account the damping, k_a =15%, which results in L_2 = 0.14mH. Also, L_T is 0.013pu < 0.1pu.
4) Using (B-14), the resonant frequency is calculated to be 7.87 kHz, which meets condition (d). $10f_g < f_{res} < 0.5f_{sw}$
5) Adopting (B.15) gives the damping resistance R_d = 2Ω.
6) Based on (B.16), the ripple attenuation $k_{a(d)}$ of the current at the switching frequency when considering the damping is calculated to be 0.2. This means that the LCL filter should reduce the expected current ripple to 20%, resulting in a ripple value of (2%) in the grid-side current ($20\% = \frac{i_2(ripple)\%}{10\%}$).

Table B-2: LCL Filter Parameters

Parameter	Symbol	Value (unit)
Inverter-side inductance	L_1	0.81mH
Grid-side inductance	L_2	0.14mH
Parallel capacitor	C_f	3.425uF
Resonant frequency	f_{res}	7.87kHz
Damping resistor	R_d	1.97 Ω

Figure.B-4 shows the bode-plot of the transfer function (B.5) and (B.7) of the filter with a passive damping and without damping. The filter parameters are set as in Table: B-2. Note that using these specified parameters, the desired ripple attenuation of the current at the switching frequency (20%) is achieved.

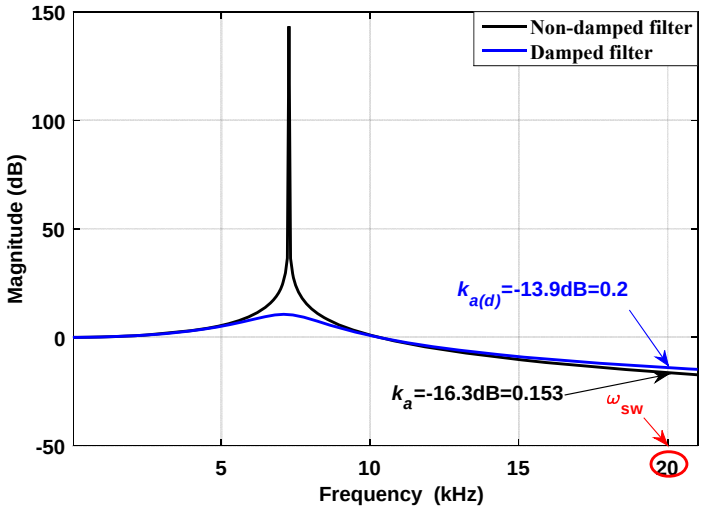


Figure. B-4 Bode-plot of (B.5) and (B.7)

Figure.B-5 shows the simulated inverter and grid currents and their associated high-frequency spectra obtained with the LCL filter, operating under rated conditions. The largest near switching frequency current harmonic component is 5.68% on the converter side and 1.13% on the grid side. Thus, it has been reduced to 20%, confirming the effectiveness of the design.

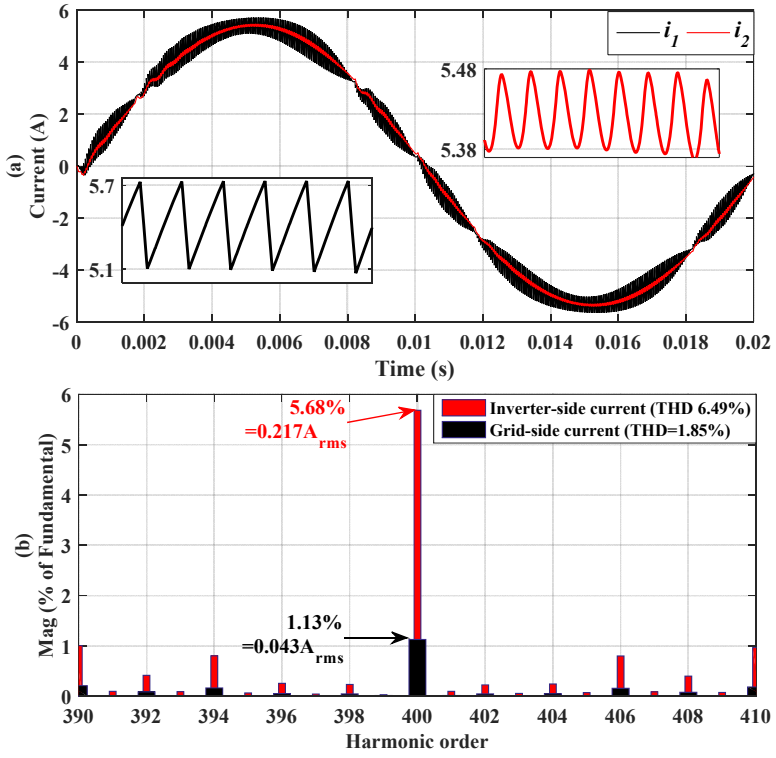


Figure. B-5 (a) Simulated steady-state inverter-side current (i_1) and grid-side current (i_2), and (b) their spectra at high frequency with LCL filter (rated conditions)

Appendix C : Phase-locked Loop

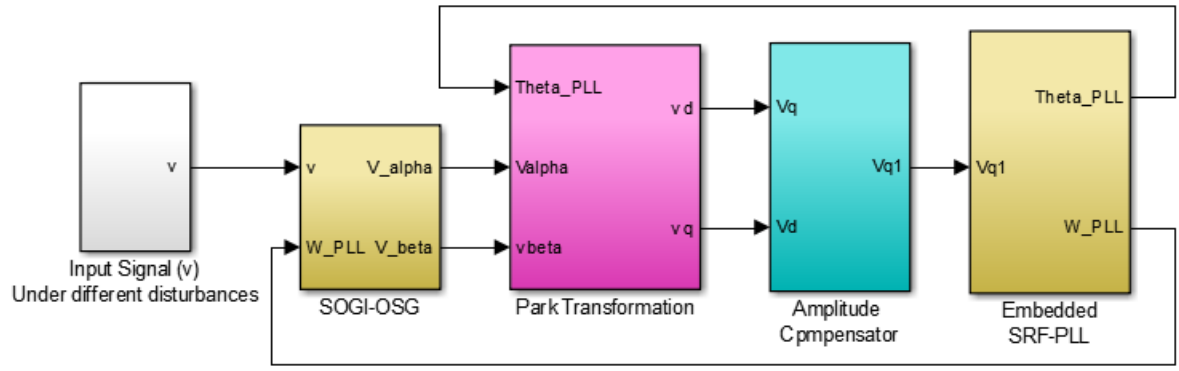
C.1 Selection of *k* in SOGI transfer functions

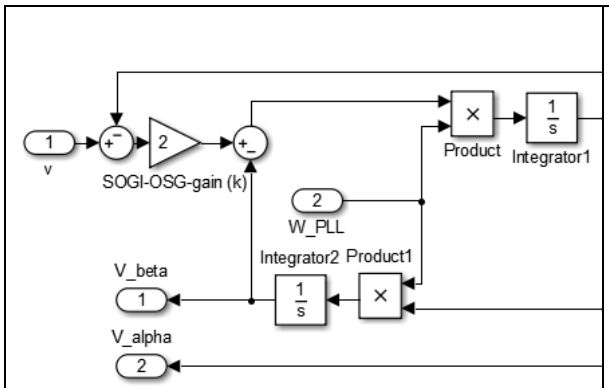
The settling time of the SOGI characteristics transfer functions described in (3.3) and (3.4) for step input is a function of the SOGI gain *k*. The selection of the optimum value of *k* that results in the smallest settling time for a step response can be determined using Table C-1 [149].

Table C-1: Step response of $G_\alpha(s)$ and $G_\beta(s)$ for different values of k

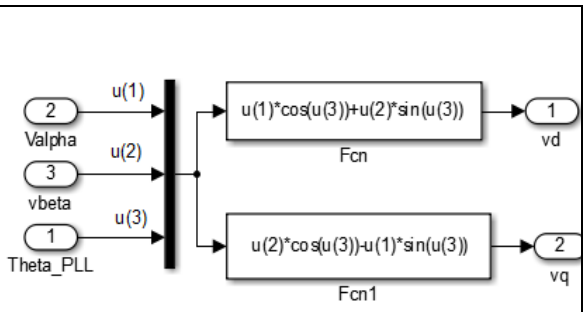
Transfer function	Case	Step response expression
$G_\alpha(s)$	*k*<2	$\frac{2k}{\sqrt{4-k^2}} e^{-k\hat{\omega} t/2} \sin\left(\hat{\omega}\sqrt{4-k^2}\, t/2\right)$
	k=2	$2\hat{\omega} t e^{-\hat{\omega} t}$
	k>2	$\frac{k}{\sqrt{k^2-4}}\left\{e^{-(k-\sqrt{k^2-4})\hat{\omega} t/2} - e^{-(k+\sqrt{k^2-4})\hat{\omega} t/2}\right\}$
$G_\beta(s)$	*k*<2	$\frac{-2k}{\sqrt{4-k^2}} e^{-k\hat{\omega} t/2} \sin\left(\hat{\omega}\sqrt{4-k^2}\, t/2 + \tan^{-1}\left(\frac{\sqrt{k^2-4}}{k}\right)\right) + k$
	k=2	$2 - 2e^{-\hat{\omega} t}(1+\hat{\omega} t)$
	k>2	$\left\{C_1 e^{-(k-\sqrt{k^2-4})\hat{\omega} t/2} - C_2 e^{-(k+\sqrt{k^2-4})\hat{\omega} t/2}\right\} + k$ $C_1 = \frac{-k(k+\sqrt{k^2-4})}{2\sqrt{k^2-4}}, C_2 = \frac{k(-k+\sqrt{k^2-4})}{2\sqrt{k^2-4}}$

C.2 Simulation model for the performance evaluation of conventional SOGI-PLL

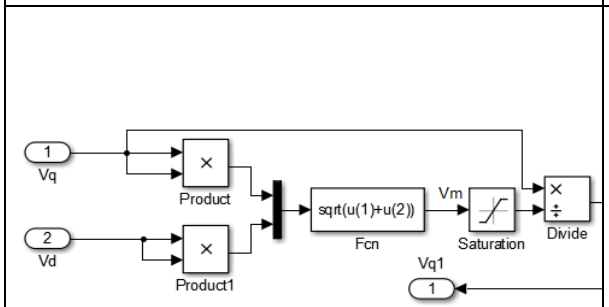




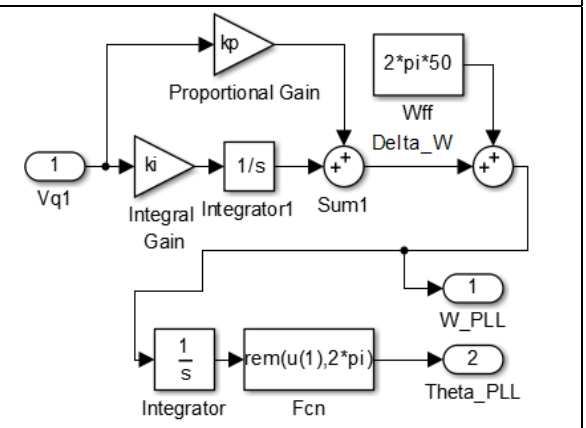
SOGI-OSG



Park Transformation



Amplitude Compensator



Embedded SRF-PLL

Figure. C.1 Simulation model used for performance evaluation of the conventional SOGI-PLL

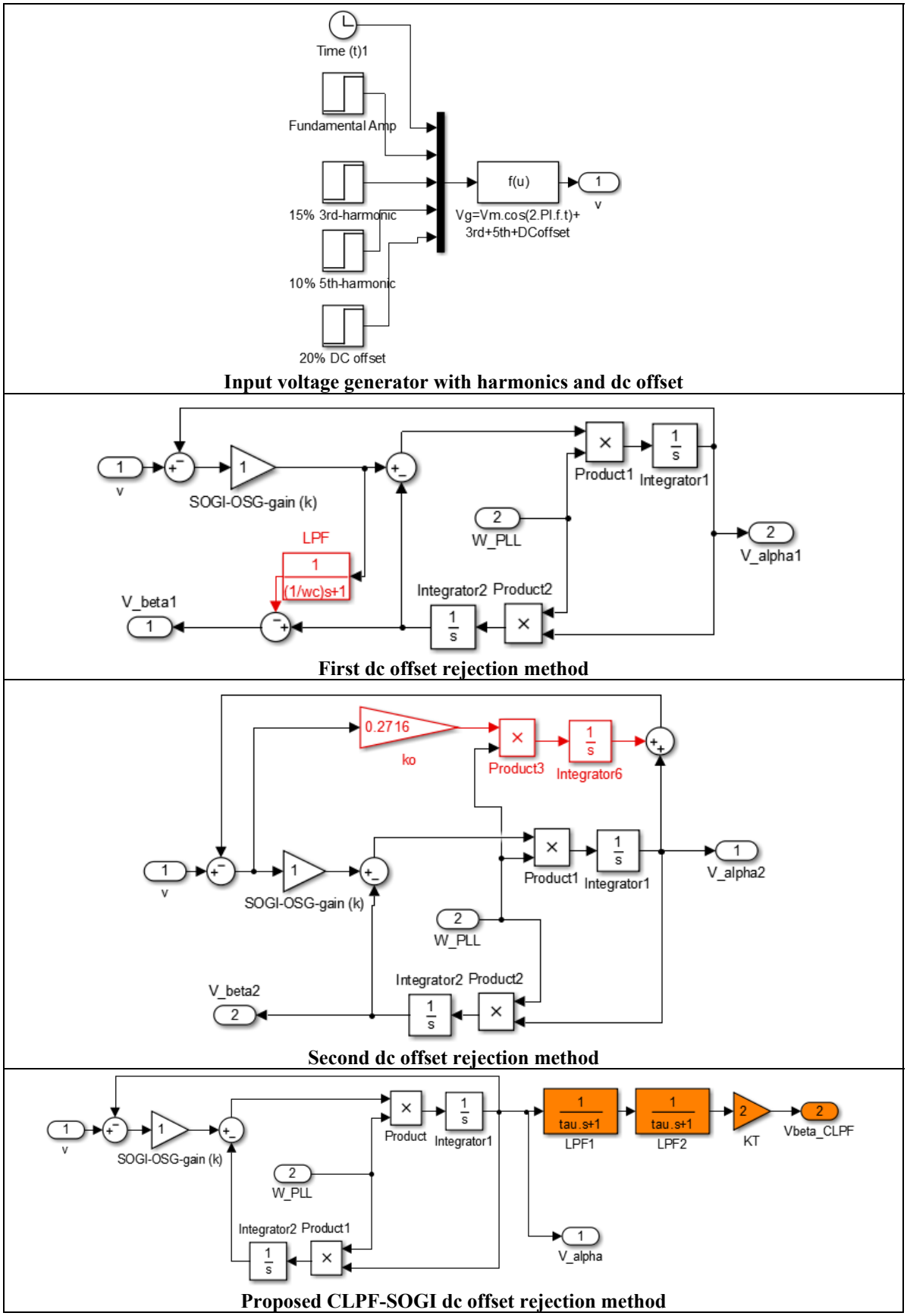


Figure. C.2 Simulation models for performance evaluation of different DC offset rejection approaches

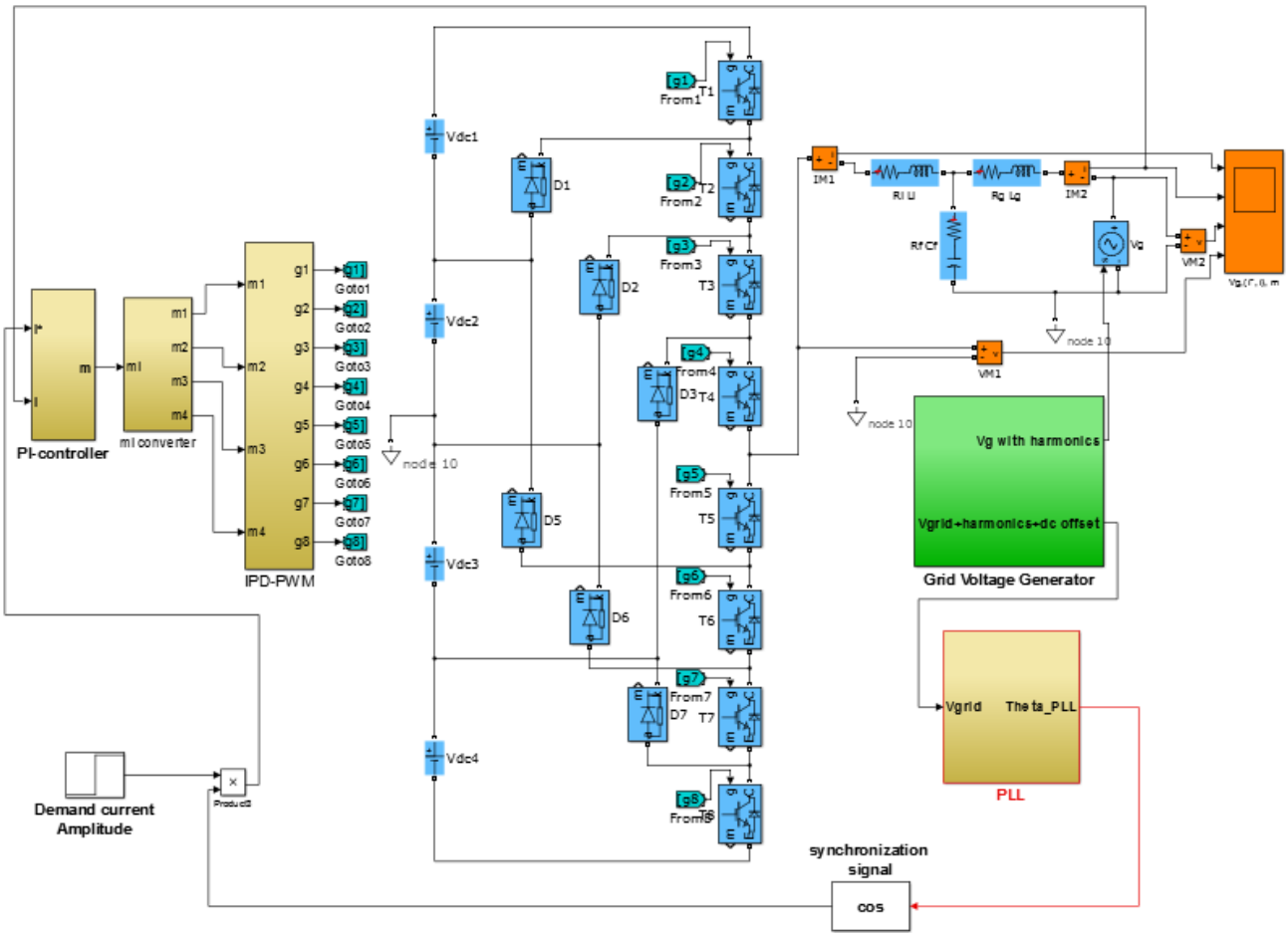


Figure. C.3 Simulation model for the evaluation of effect of the PLL method on the grid-connected PV system performance

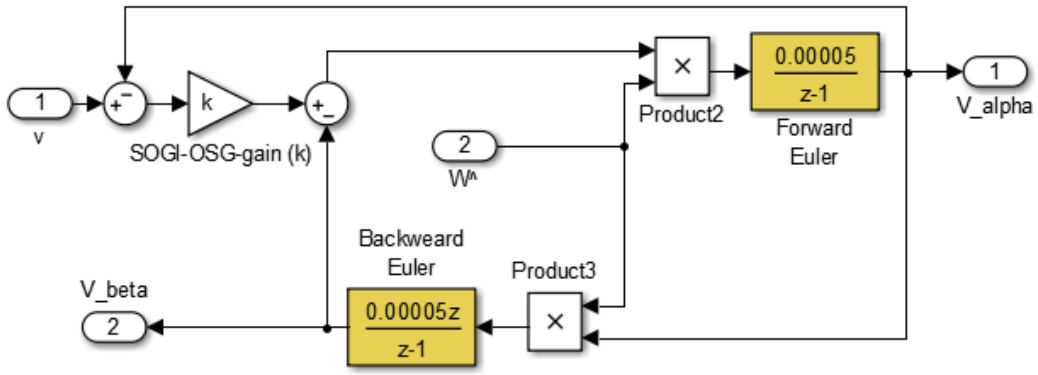


Figure. C.4 Simulation model for the Euler's method implementation of the conventional OSG-SOGI

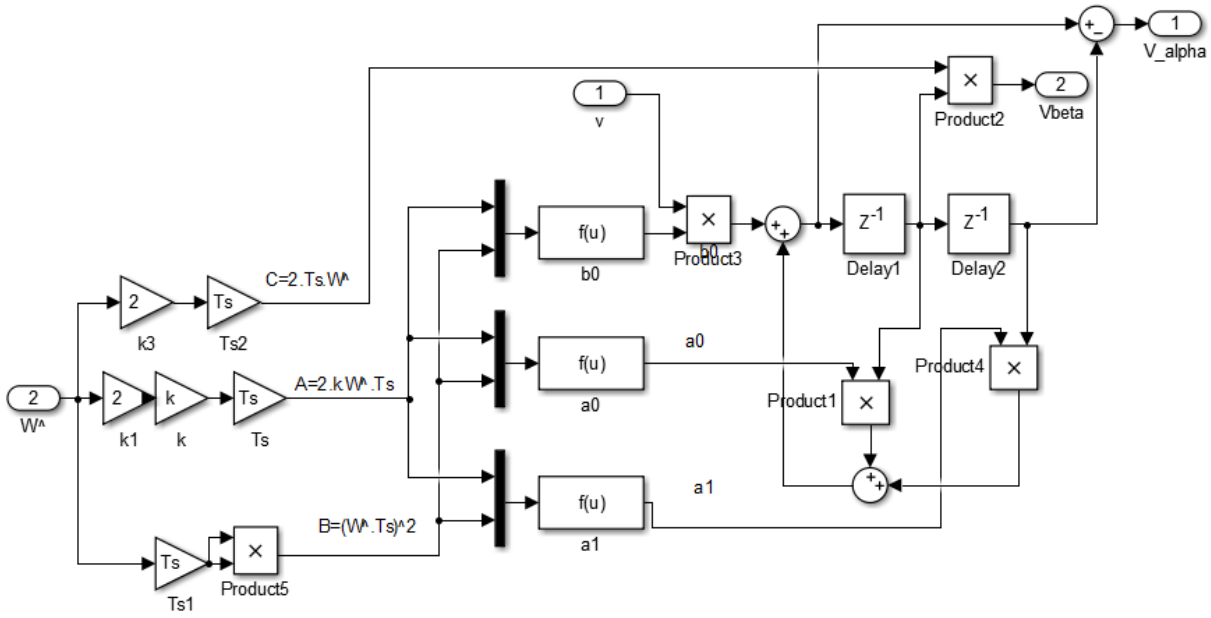


Figure. C.5 Simulation model for the Tustin's method implementation of the conventional OSG-SOGI

Appendix D : Programming Code

D1. Programming code for the conventional SOGI-PLL

In the following, for demonstrating purpose, programming code for the conventional SOGI-PLL based on Tustin's method described in Section 6.11 is presented.

```
#if 1 //********(Conventional SOGI-PLL)*********//
K=2;
Ts=0.00005; // 1/20khz
Valfa_PLL=(Vgrid);//measured from the grid voltage sensor
X=2*K*W_PLL_1*Ts;
Y=W_PLL_1*Ts*W_PLL_1*Ts;
Z=2*W_PLL_1*Ts;
b2=X+Y+4;
b0=X/b2;
a1=2*(4-Y)/b2;
a2=(X-Y-4)/b2;
cd=(b0*Valfa_PLL)+(a1*cd_1)+(a2*cd_2);
Valfa_PLL_plus = cd-cd_2;
Vbeta_PLL=cd_1*Z;
cd_2=cd_1;
cd_1=cd;
Valfa_PLL_plus_1=Valfa_PLL_plus;
#endif

//*****Working out the Amplitude of the grid voltage Vm *******//
#if 1
u1=Valfa_PLL_plus*Valfa_PLL_plus;
u2=Vbeta_PLL*Vbeta_PLL;
Vg_max=sqrt(u1+u2);
Valfa_pu=Valfa_PLL_plus/Vg_max;
Vbeta_pu=Vbeta_PLL/Vg_max;
#endif

//*****************Embeded SRF-PLL*********************//
vide =  Valfa_pu*cos_t[(int)Theta_PLL] + Vbeta_pu*sin_t[(int)Theta_PLL];
viqe = -Valfa_pu*sin_t[(int)Theta_PLL] + Vbeta_pu*cos_t[(int)Theta_PLL];
kp_PLL=135.84;
ki_PLL=0.3844;
Delta_W=kp_PLL*PLL_error+zd_PLL;
if(release)
      zd_PLL = zd_PLL + ki_PLL*PLL_error;
if(!release)
      {
            zd_PLL=0;
      }

       //Anti-windup code
      if(zd_PLL > 400)
            zd_PLL = 400;
      if(zd_PLL < -400)
```

```
            zd_PLL = -400;
W_PLL=Wff+Delta_W;
W_PLL_1=W_PLL;

Theta_PLL=Theta_PLL_1+((Ts/2)*(W_PLL+W_PLL_1)); //using Tustin's
//Theta_PLL=Theta_PLL_1+W_PLL*Ts; //using backward Euler
//Theta_PLL=Theta_PLL_1+W_PLL_1*Ts; //using forward Euler

Freq=W_PLL/(2*PI); //Frequency from PLL
if (Theta_PLL>=(2*PI))
      Theta_PLL-=(2*PI);
if(Theta_PLL > 6.283)
      Theta_PLL = 6.283;
      if(Theta_PLL < -6.283)
            Theta_PLL = -6.283;
Theta_PLL_1=Theta_PLL;
Theta_PLL=114.591559*Theta_PLL;  //(720/2*PI) = Theta_PLL=Theta_PLL*(2pi/720) rad
V_ref=cos_t[(int)Theta_PLL];
//*****************End of Conventional SOGI***********************//
#endif
```

D2. Programming code for the proposed CLPF-SOGI PLL

Programming code for the proposed CLPF-SOGI PLL based on Tustin's method described in Section 6.11 is presented.

```
#if 1  //******* Proposed CLPF-SOGI PLL ************
K1=2;
Valfa_PLL=(Vgrid);//measured from the grid voltage sensor
#if 1
XCLPF=2*K1*W_PLL_CLPF_1*Ts;
YCLPF=W_PLL_CLPF_1*Ts*W_PLL_CLPF_1*Ts;
ZCLPF=2*W_PLL_CLPF_1*Ts;
b2CLPF=XCLPF+YCLPF+4;
b0CLPF=XCLPF/b2CLPF;
a1CLPF=2*(4-YCLPF)/b2CLPF;
a2CLPF=(XCLPF-YCLPF-4)/b2CLPF;
cdCLPF=(b0CLPF*Valfa_PLL)+(a1CLPF*cdCLPF_1)+(a2CLPF*cdCLPF_2);
Valfa_CLPF = cdCLPF-cdCLPF_2;
cdCLPF_2=cdCLPF_1;
cdCLPF_1=cdCLPF;
#endif
#if 1 // using the Valfa_CLPF generated by SOGI as an input to CLPF to generate
Vbeta
Valfa=Valfa_CLPF;
Tau=(1/(W_PLL_CLPF_1));//(Tau=1/W) Low pass filter parameters to get 90 phase-shift
      Ts=0.00005; // 1/20khz
 // Discretization using Trapezoidal method
      a=1.414213562*Ts/(2*Tau+Ts); //(1.4142316=sqrt2) (gain 'a')
      b=(Ts-2*Tau)/(2*Tau+Ts);   (gain 'b')
Valfa_plus=(a*Valfa+a*Valfa_1);
Valfa_plus1=Valfa_plus-(b*Valfa_plus1_1); //45 deg
Valfa_plus2=(a*Valfa_plus1+a*Valfa_plus1_1);
```

```
Vbeta=Valfa_plus2-(b*Vbeta_1); //90deg
Valfa_1=Valfa;
Valfa_plus1_1=Valfa_plus1;
Vbeta_1=Vbeta;
#endif

//********Working out the Amplitude of the grid voltage Vm ***************//
#if 1
u1CLPF=Valfa_CLPF*Valfa_CLPF;
u2CLPF=Vbeta*Vbeta;
Vg_maxCLPF=sqrt(u1CLPF+u2CLPF);

Valfa_pu_CLPF=Valfa_CLPF/Vg_maxCLPF;
Vbeta_pu_CLPF=Vbeta/Vg_maxCLPF;
#endif

#if           1//*****************Embedded           SRF-PLL-using           CLPF
method************************//
vide_CLPF= Valfa_pu_CLPF*cos_t[(int)Theta_PLL_CLPF]+
                                    Vbeta_pu_CLPF*sin_t[(int)Theta_PLL_CLPF];

viqe_CLPF = -Valfa_pu_CLPF*sin_t[(int)Theta_PLL_CLPF]+
                             Vbeta_pu_CLPF*cos_t[(int)Theta_PLL_CLPF]; //PLL error

kp_PLL=135.84;
ki_PLL=0.3844;
Delta_W_CLPF=kp_PLL*PLL_error_CLPF+zd_PLL_CLPF;
if(release)
       zd_PLL_CLPF = zd_PLL_CLPF + ki_PLL*PLL_error_CLPF;
if(!release)
       {
              zd_PLL_CLPF=0;
       }
        //Anti-windup code
       if(zd_PLL_CLPF > 400)
              zd_PLL_CLPF = 400;
       if(zd_PLL_CLPF < -400)
              zd_PLL_CLPF = -400;
W_PLL_CLPF=Wff+Delta_W_CLPF; //rad/s (2PI'rad'*F'1/s')
W_PLL_CLPF_1=W_PLL_CLPF;

Theta_PLL_CLPF=Theta_PLL_CLPF_1+((Ts/2)*(W_PLL_CLPF+W_PLL_CLPF_1)); //using Trap

Freq_CLPF=W_PLL_CLPF/(2*PI); //Frequency from PLL
if (Theta_PLL_CLPF>=(2*PI))
       Theta_PLL_CLPF-=(2*PI);
if(Theta_PLL_CLPF > 6.283)
       Theta_PLL_CLPF = 6.283;
       if(Theta_PLL_CLPF < -6.283)
              Theta_PLL_CLPF = -6.283;
Theta_PLL_CLPF_1=Theta_PLL_CLPF;
Theta_PLL_CLPF=114.591559*Theta_PLL_CLPF;
V_ref_CLPF=cos_t[(int)Theta_PLL_CLPF];
//*****************End of 2CLPF method************************//
#endif
#endif
```

D3. Programming code for the proposed simplified *dq* current controller

Programming code for the proposed simplified *dq* current controller described in Section 6.12 is presented.

```
#if 1 //====Closed Loop Operation using Simplified dq current control===
       Ialfa_s=i_grid; // using the grid current as a feedback current
       Valfa_g=Vg;
       error_1=Valfa_g-Valfa_g_plus_1;
       error_2=error_1-Vbeta_g_1;
       W_1=error_2*Wff;
       Valfa_g_plus = Valfa_g_plus_1+W_1*Ts;
       Valfa_g_plus_1=Valfa_g_plus;
       W_2=Valfa_g_plus*Wff;
       Vbeta_g=Vbeta_g_1+W_2*Ts;
       Vbeta_g_1=Vbeta_g;

Vg_d=Valfa_g*cos_t[(int)Theta_PLL_CLPF] + Vbeta_g*sin_t[(int)Theta_PLL_CLPF];
Vg_q=Vbeta_g*cos_t[(int)Theta_PLL_CLPF] - Valfa_g*sin_t[(int)Theta_PLL_CLPF];

             // PIdq current controller//
#endif

#if 1 // Current step
             if(store_enable)
             {
                    baset++;
                    if(baset<400)
                           par3=0;
                    else if(baset<1200)
                           par3=27;
                    else
                           par3=54;
             }
             else
                    baset=0;

#endif
Id_ref = par3; //The peak value of the demand current
Id_ref=0.1*Id_ref;
Iq_ref = 0;
Ialfa_s_ref = Id_ref*cos_t[(int)Theta_PLL_CLPF];
error_alfa_s=Ialfa_s_ref-Ialfa_s;
#if 1
error_d=error_alfa_s*cos_t[(int)Theta_PLL_CLPF];
       error_q=-error_alfa_s*sin_t[(int)Theta_PLL_CLPF];
#endif

L=2e-3; //3.5e-3 Decoupling
kp=par5; //1600*1
ki=par6;
Vcd = kp*error_d+ zd;
Vcq = kp*error_q+ zq;
             if(release)
                    zd = zd + ki*error_d;
```

```
                zq = zq + ki*error_q;
            if(!release)
            {
                zd=0;
                zq=0;
            }
            // Anti-windup code
            if(zd > 7500)
                zd = 7500;
            if(zd < -7500)
            zd = -7500;
            if(zq > 7500)
                zq = 7500;
            if(zq < -7500)
                zq = -7500;

            if(Vcd > 7499)
                Vcd = 7499;
            if(Vcd <-7499)
                Vcd = -7499;

            if(Vcq > 7499)
                Vcq = 7499;
            if(Vcq <-7499)
                Vcq = -7499;
            Id=Id_ref-error_d; //error_d=Id_ref-Id //Id = the demand current
            Iq=Iq_ref-error_q; //error_q=Iq_ref-Iq & Iq_ref=0


#if 1
      Vind=Vcd + (120*Vg_maxCLPF)-(Iq_ref*Wff*L);
      Vinq=Vcq + (120*viqe_CLPF)+(Id_ref*Wff*L);
#endif

            if(Vind > 7499)
                Vind = 7499;
            if(Vind <-7499)
                Vind = -7499;

            if(Vinq > 7499)
                Vinq = 7499;
            if(Vinq <-7499)
                Vinq = -7499;
//Transforming the rotating output signals of the PIdq controller (Vind&Vinq) back
to the stationary reference frame to be sent to the PWM generator//
// The Alfa component of the control signal will be fed into the PWM modulator
Vin_alfa_v=Vind*cos_t[(int)Theta_PLL_CLPF] - Vinq*sin_t[(int)Theta_PLL_CLPF];

            if(Vin_alfa_v > 7499)
                Vin_alfa_v = 7499;
            if(Vin_alfa_v <-7499)
                Vin_alfa_v = -7499;
            modindex=Vin_alfa_v;

    // check that modulation index is in range (-7500 to +7499)

#endif//*************************************************************
```

D4. Pulse width modulation (PWM) set-up

Programming code for the pulse width modulation (PWM) described in Section 6.13 is presented.

```
#if 1

	if((modindex >= 3750) && (modindex < 7500))
	{
		ma = 7499 - modindex;
		mb = 0;
		mc = 0;
		md = 0;
	}

	if((modindex >= 0) && (modindex < 3750))
	{
		ma = 3750;
		mb = 3750 - modindex;
		mc = 0;
		md = 0;
	}

	if((modindex >= -3750) && (modindex < 0))
	{
		ma = 3750;
		mb = 3750;
		mc = -(1 + modindex);
		md = 0;
		}

	if((modindex >= -7500) && (modindex < -3750))
	{
		ma = 3750;
		mb = 3750;
		mc = 3750;
		md = -(3751 + modindex);
	}

#endif
```

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