High Power Density AC to DC Conversion with Reduced Input Current Harmonics

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Abstract

This thesis investigates the benefits and challenges arising from the use of minimal capacitance in AC to DC converters. The purpose of the research is to ultimately improve the power density and power factor of electrical systems connected to the grid. This is carried out in the context of a low cost brushless DC drive system operating from an offline power supply.

The work begins with a review of existing applications where it is practical to use a limited amount of DC link capacitance. The vast majority of these have a load which is insensitive to supply power variations at twice the line frequency. Low performance motor drives are found to be the most prevalent, with the inertia of the rotor mitigating the effect of torque ripple. Further research is carried out on active power factor correction techniques suitable for this application, leading to the conclusion that no appropriate systems exist.

A power supply is developed to enable a 24V, 200W brushless motor drive to operate from the mains. The system runs successfully using only 1µF of DC link capacitance, which causes the motor supply voltage to have 100% ripple. It is noted that whilst this drastically reduces the low frequency input current harmonics, those occurring at the load switching frequency are greatly increased.

To combat this, a novel active power factor correction system is proposed using a notch filter to detect the input current error. The common problem of voltage feedback ripple is avoided by eliminating the voltage control loop altogether. The main limitations are identified as a high sensitivity to load step changes and variations in line frequency. Despite this, a high power factor is maintained in all operating conditions, as well as compliance with the relevant harmonic standards.

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Contents

List of Symbols and Abbreviations

I_{load}	Load current
N_{phase}	Phase number
f_{supply}	Supply frequency
C_{DC}	DC link capacitance
V_{DC}	DC link voltage
V_{ripple}	DC link voltage ripple
V_{AC}	AC supply voltage
I_{AC}	AC supply current
P_{in}	Input power
I_{DC}	DC input current
$\hat{V}$	Supply voltage amplitude
$\hat{I}$	Supply current amplitude
L_{out}	Output filter inductor
V_{batt}	Battery voltage
V_{in}	DC input voltage
E_C	DC link capacitor energy
P_{in}	Input power
P_{out}	Output power
I_{ref}	Reference current
V_{ff}	Voltage feedforward
V_{ea}	Voltage error amplifier output
V_{ref}	Voltage reference
I_{in}	DC input current
V_{out}	Output voltage
i	Current
t	Time
I_{comp}	Compensation current
I_{load}	Load current

T	Torque
E	Voltage
R	Resistance
θ	Angle
L	Inductance
V_{phase}	Phase voltage
R_{src}	Source resistance
L_{src}	Source inductance
I_{phase}	Phase current
L_{wind}	Winding inductance
R_{wind}	Winding resistance
C_{drive}	Motor drive capacitance
I_{inv}	Inverter current
N	Number of turns
f	Frequency
B_{sat}	Saturation flux density
D	Duty cycle
$R_{DS(on)}$	Conducting drain-source channel resistance
B	Flux density
H	Magnetic Field Strength
f_{sw}	Switching frequency
$\hat{B}$	Peak flux density
B_r	Remanent flux density
C_{src}	Source capacitance
C_{out}	Output capacitance
L_{out}	Output inductance
L_{leak}	Leakage inductance
V_{GS}	Gate-Source voltage
V_{pri}	Primary winding voltage
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_{DS}	Drain-source capacitance
C_{ISS}	MOSFET input capacitance

C_{OSS}	MOSFET output capacitance
C_{pri}	primary winding capacitance
P_{sw}	Switching loss
P_{COSS}	Parasitic capacitance switching loss
I_{DS}	Drain-source current
V_{DS}	Drain-source voltage
t_{on}	Turn-on transition time
t_{off}	Turn-off transition time
P_{CPRI}	Primary winding capacitance loss
P_{cond}	Conduction loss
P_{RR}	Reverse recovery loss
E_{filter}	Filter energy storage
$P_{harmonic}$	Harmonic power
L_{boost}	Boost inductance
$\hat{V_{in}}$	Peak input voltage
I_{ripple}	Ripple current
PF_D	Displacement power factor
f_{notch}	Notch filter tuned frequency

AC	Alternating Current
DC	Direct Current
VSD	Variable Speed Drive
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
LED	Light Emitting Diode
RMS	Root Mean Square
EMI	Electro-Magnetic Interference
IEC	International Electrotechnical Commission
PFC	Power Factor Correction
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
HVAC	Heating Ventilation and Air Conditioning

PWM	Pulse Width Modulation
DTC	Direct Torque Control
SVM	Space Vector Modulation
FOC	Field Oriented Control
CCCV	Constant Current Constant Voltage
SRC	Sinusoidal Ripple Current
DAB	Dual Active Bridge
APFC	Active Power Factor Correction
ARES	Active Ripple Energy Storage
PV	Photo-Voltaic
MTBF	Mean Time Between Failures
EMC	Electro-Magnetic Compatibility
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
FET	Field Effect Transistor
THD	Total Harmonic Distortion
APF	Active Power Filter
BLDC	BrushLess Direct Current
RPM	Revolutions Per Minute
BEMF	Back ElectroMotive Force
PCB	Printed Circuit Board
ADC	Analogue to Digital Converter
FFT	Fast Fourier Transform
PI	Proportional-Integral
GBP	Gain Bandwidth Product

Chapter 1

Introduction

1.1 AC to DC Converters

Many electrical systems which are connected to the mains cannot derive their power directly from an AC source. It is first necessary to convert this to a DC source, most commonly with a diode bridge rectifier and DC link capacitor as shown in Figure 1.1. These components can be found on the front end of consumer electronic products, Variable Speed Drives (VSDs) and computer power supplies among numerous other applications. Over time, the constant demand for new technology has vastly increased the number of these systems connected to the grid.

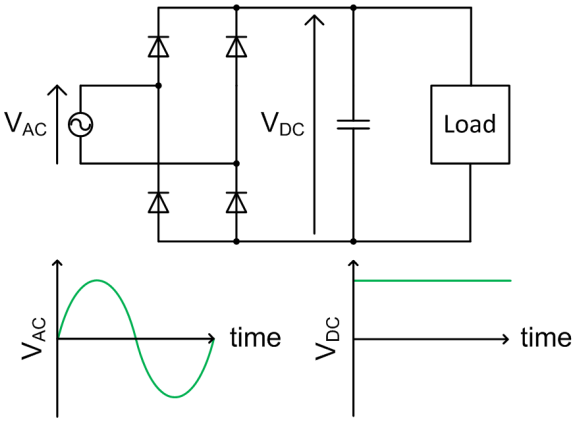

Figure 1.1: A single-phase AC to DC converter constructed from a diode bridge rectifier and smoothing capacitor

For a single-phase supply, AC to DC conversion entails the transformation of time-varying power to constant power. This process inherently requires energy storage to account for the short term imbalance between the input and output power of the system. When the magnitude of the AC voltage exceeds the DC voltage, the

rectifier diodes are forward biased, allowing charge to flow into the capacitor and hence energy is stored. When the DC voltage exceeds the AC voltage, the rectifier diodes are reverse biased and the capacitor discharges, providing the sole source of energy for the load. This process of charging and discharging causes a ripple in the DC link voltage which is determined by four factors; the load current I_{load}, number of phases N_{phase}, supply frequency f_{supply} and DC link capacitance C_{DC}.

$$V_{ripple} = \frac{I_{load}}{2N_{phase}.f_{supply}.C_{DC}} \tag{1.1}$$

As the number of phases, supply frequency and average load current will be fixed for a given application, it is therefore necessary to have a large DC link capacitance in order to achieve a small ripple voltage. Whilst this is beneficial to the performance of the load, it has a negative impact on the volume and cost of the system. The intrinsic link between operating frequency and size has lead to DC link capacitance being the key limiting factor in AC to DC converter power density [1]. DC to DC converters are far superior in this respect as the operating frequency is chosen as part of the system design, constrained only by the limits of the components and control system. For mains connected loads requiring a constant supply voltage, improvements in capacitor technology offer the only significant method of reducing the size and cost of the AC to DC stage.

Electrolytic capacitors are the favoured devices for this purpose as they have a far greater energy storage density than electrostatic variants [2]. It is for this reason alone that they remain the popular choice for line frequency filtering applications. However, in almost every other respect they are inferior, suffering from high Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) coupled with a poor tolerance to temperature. Additionally, the liquid electrolyte used in their construction degrades over time, leading to failure rates almost two orders of magnitude higher than 'dry' capacitor variants [3]. This poses significant issues for power converters in long-term installations such as solar generators or LED lighting systems.

The combination of a large capacitor and a bridge rectifier leads to a further problem in the form of highly distorted input current. Due to the non-linear behaviour

of the diodes, current can only be drawn from the supply when they are forward biased. As can be seen in Figure 1.2, a small DC link voltage ripple leads to a very short diode conduction period and subsequently a short spike of input current near the peak of the mains voltage. The non-sinusoidal current contains harmonics which do not contribute to the active power flow in the system, leading to a poor power factor, typically less than 0.7 [4].

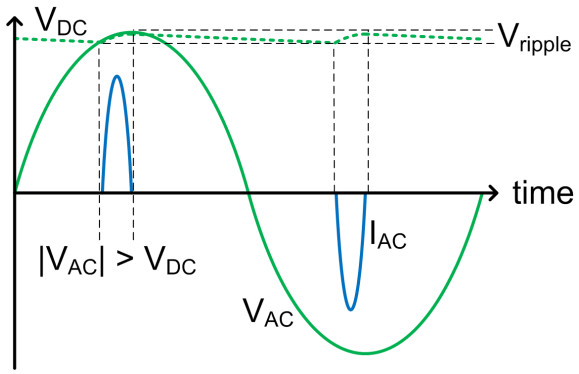

Figure 1.2: Input current distortion caused by high DC link capacitance

Poor power factor and high current distortion have a number of side effects detrimental to the performance of the power network and the systems connected to it:

1. Voltage distortion resulting from the harmonic currents flowing through the impedance of the supply system.
2. Higher RMS current for a given real power, requiring over-rating of transformers, switchgear and cables making them larger and more costly; this is becoming a significant issue as the price of copper rises [5].
3. High frequency current pulses causing additional transformer heating, false tripping of breakers and skin effect in conductors.
4. Interference with sensitive equipment due to increased $\frac{di}{dt}$ and therefore greater conducted/radiated Electro-Magnetic Interference (EMI).
5. Resonance and reactive power injection by harmonic filters [6].

In an effort to control these issues, IEC 1000-3-2, which sets limits on harmonic current emissions in equipment up to 16A per phase, was adopted as a European

Standard in 2001 (as EN 61000-3-2). This requires virtually all consumer and light industrial electrical equipment to be designed with consideration for its effect on supply current distortion [7]. The standard sets limits for individual harmonic magnitudes for the input current to a device, with the requirements varying depending on its classification.

The most significant of these requirements are the Class A limits as they cover the widest range of applications. These are shown in Table 1.1 along with the Class D limits applicable to devices "shown to have a pronounced effect on the public electricity system". The key difference between the Class A and Class D limits is that the former are given in absolute terms, whereas the latter are scaled by the active load power.

	Class A	Class D	
Harmonic order n	Current limit (A)	Current limit (mA/W)	Max current (A)
3	2.3	3.4	2.3
5	1.14	1.9	1.14
7	0.77	1.0	0.77
9	0.4	0.5	0.4
11	0.33	0.35	0.33
13	0.21	0.30	0.21
15 - 39 odd	0.15 x $\frac{15}{n}$	$\frac{3.85}{n}$	0.15 x $\frac{15}{n}$
2	1.08	-	-
4	0.43	-	-
6	0.3	-	-
8 - 40 even	0.23 x $\frac{8}{n}$	-	-

Table 1.1: BS EN 61000-3-2 harmonic current limits

In order to meet these requirements, the conventional approach is to add a Power Factor Correction (PFC) circuit, using either passive or active filtering techniques. This allows for a reduction in input current harmonics whilst maintaining a constant DC output voltage; the penalty for this is a further increase in size and cost.

1.2 Reduced DC Link Capacitance

In response to the problems discussed previously, there has been growing academic and industrial interest in the design of power converters with reduced DC link capacitance. For certain applications, an acceptable performance can still be achieved when the DC link voltage, and subsequently the output power, has a very large ripple at twice the line frequency. This is always the case in single-phase AC systems such as heaters, incandescent lighting or induction motors, where the load responds to the average, rather than instantaneous value of the supplied power. For example, the 100Hz (or 120Hz) variation in input power to a heating element is not seen in its output as the thermal time constant prevents a significant change in temperature at this frequency. Similarly, the inertia of a universal or induction motor means that its speed will be relatively constant over one half-cycle of the mains, despite the large variation in torque. In these applications there is still energy storage present, but instead of a dedicated component such as a capacitor, it is the load itself which provides this function.

As discussed extensively in the next chapter, this same principle can be applied to DC loads which do not require constant power. By limiting the imbalance between the input and output power of an AC to DC converter, the energy storage requirement is reduced, leading to a potentially more compact and lower cost system. The increased DC link voltage ripple results in a longer conduction period for the rectifier diodes and subsequently a smoother input current with less harmonic content.

Whilst this concept and its benefits are clear, the new challenges it creates are not inconsiderable. By removing the decoupling between the supply and load, the subsystems become far more interdependent, with a change in one reflected immediately in the other. A holistic approach is required for the system design in order for it to function properly, with a greater consideration for the dynamic behaviour of the load and varying supply conditions. It is the study of this problem and its potential solutions which ultimately forms the key focus of this work.

1.3 Thesis Overview

This thesis begins with research into existing applications where the DC link capacitance is purposefully small. Compared to a conventional design, the DC link

capacitance can be reduced by more than 99% in some cases, whereas in others it may be as little as 30%. However, in each case this is done for the purposes of improving size, cost, lifetime or harmonic performance. Particular attention is paid to the detrimental effects this has on load behaviour, along with the techniques used to mitigate them. A review of power factor correction techniques is included, which fundamentally concludes that no existing systems are suited for use with reduced DC link capacitance.

Low performance motor drives are found to be the main application for this concept, with considerable existing work by academics and the industrial sponsor for this research. A 200W 24V brushless DC motor drive is selected as the test load, requiring a DC to DC converter to provide the correct supply voltage. This provides another platform on which to analyse the effects of reduced DC link capacitance, particularly the loss of efficiency with an increasingly dynamic load.

Load harmonics in the input current are identified as the key challenge of this application, leading to the development of a novel control system designed to attenuate them using the minimum amount of energy storage. Fundamental analysis of harmonic filtering is followed by the simulation of two different control methods for a boost converter front-end. The more successful technique based on notch filtering is implemented in hardware, with Chapter 6 covering the design process in detail.

Finally, the system is tested over a range of operating conditions in order to thoroughly analyse its behaviour. The main performance limitations are shown to be an increased sensitivity to rapid load reductions and variations in supply frequency. Furthermore, an important compromise is noted between the level of harmonic attenuation achieved and the peak DC link voltage. Despite this, the controller is shown to maintain a power factor exceeding 0.9 even in worst case conditions, as well as meeting the more challenging scaled EN 61000-3-2 harmonic limits.

1.4 Novel Aspects

All of the research contained within this thesis stems from the idea that in certain power converter applications, an improvement in size, cost and power factor can be realised through a reduction in DC link capacitance. The challenge is in solving

the new problems that occur when there is virtually zero decoupling between the different subsystems. The most significant contributions to knowledge are:

1. An active power factor correction system which does not require a reference current or voltage control loop, thus allowing it to work with 100% DC link voltage ripple. The input current error is extracted by a notch filter tuned to the supply frequency rather than by the subtraction of an ideal reference. A patent application covering this concept is currently being compiled by Dyson Technology Ltd.

2. An active power factor correction system which only attenuates the high frequency harmonic content of the line current, removing the need for a large DC link capacitor. This works in conjunction with an existing motor drive control strategy designed to produce minimal low frequency harmonics.

3. New research into the practical limits of minimising energy storage in low cost power supplies such as those found in domestic appliances or other applications with reduced performance requirements.

4. A novel current sensing system which provides a measure of the line input current by multiplying the DC link input current with the polarity of the input voltage. This provides the essential AC current signal necessary for extraction of the harmonic content without the additional distortion caused by the rectification process. By placing the current sensor after the bridge rectifier, a simple non-isolated shunt arrangement can be used, providing a very compact, low cost solution which can measure from DC into the MHz range. A patent application covering this circuit design is currently being compiled by Dyson Technology Ltd.

Chapter 2

A Literature Review of Reduced Capacitance Power Systems

This chapter reviews prior art in two key areas relevant to the work in this thesis. The first analyses existing power converter applications which make use of reduced DC link capacitance. This provides valuable insight into the challenges faced when designing such systems, one of which is load frequency distortion of the supply current. Subsequently this leads on to the second research area; power factor correction.

2.1 Existing Applications for Reduced DC Link Capacitance

2.1.1 Three-Phase Motor Drives

Research in this field has shown that the problems discussed in the previous chapter can be mitigated somewhat through the use of reduced DC link capacitance. Its main application is in three-phase converter/inverter drives (see Figure 2.1), where the problems caused by limited decoupling can be overcome [8–13]. These systems work on the principle that if the instantaneous input and output currents can be forced to the same value, no DC link energy storage is required. The dynamics of the control system determine the extent to which this can be achieved; a fast and accurate scheme will require minimal capacitance to cater for the imbalance between input and output currents [10]. It has been proposed by Kim and Sul [11] that the power device junction capacitance alone could be adequate, allowing one-chip AC-DC-AC power conversion. However, this is likely to be impractical as a sufficiently high speed voltage control loop would rapidly modulate the input current amplitude, causing distortion and subsequently a poor power factor. A clear parallel can

be drawn between this system and a matrix converter, and would likely suffer from many of the same drawbacks.

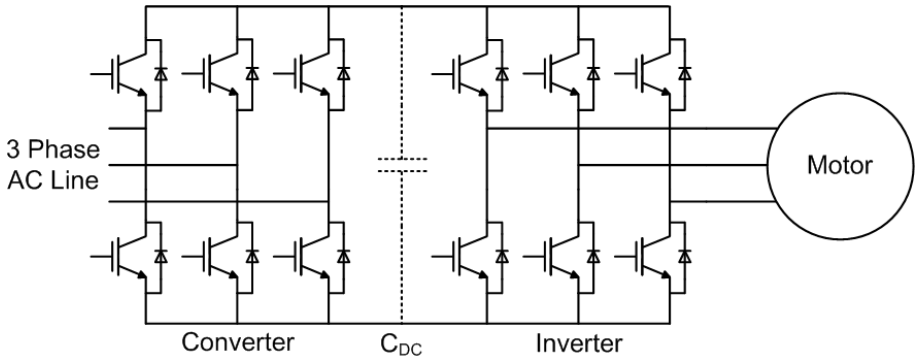

Figure 2.1: three-phase converter/inverter with minimal DC link capacitance

Due to the nature of three-phase systems, it is possible to obtain an approximately constant power transfer if the load appears linear, unlike in single-phase systems where the power is inherently time varying. This is ideal in the case of a motor drive system where the load typically demands constant power.

A number of different converter control strategies have been developed with the aim of maintaining a constant DC link voltage whilst keeping the input power factor high. Kim and Sul [11] use a power estimator technique based on the load and system losses to predict the active power required from the input. A space-vector based current controller is used for rapid control of the source and load side currents. Malesani *et al.* [10] use actual DC link current measurements to generate a feed-forward compensation term to speed up the system response. There are however a number of problems associated with DC link current measurement, most significantly the additional stray inductance caused by the sensor itself [9] and the need for a low pass filter due to the switching noise on the link. A low pass filter will introduce delay into the system, limiting the speed of the current regulation. Due to the importance of current control bandwidth, other techniques have been employed such as deadbeat control [14], direct capacitor current control [8] and feedback linearisation [9].

Whilst exhibiting good performance in terms of both input and output current quality, such converter/inverter systems suffer from high cost and complexity. An alternative solution is to use an uncontrolled rectifier for AC/DC conversion, using

diodes rather than active devices such as IGBTs or MOSFETs. Andersen *et al.* [15] present a reduced capacitance AC drive intended for HVAC (Heating Ventilation and Air Conditioning) applications. The application is critical to the feasibility of the reduced capacitance drive system, as HVAC involves fan-type loads which can tolerate a certain degree of torque ripple. The performance requirements in terms of efficiency, acoustic noise and harmonic distortion however are high. For a full wave rectified three-phase voltage, the maximum theoretical DC link ripple is $1 - \frac{\sqrt{3}}{2} \approx 13\%$, which will be seen if no DC link capacitance is used. As discussed previously, there is essentially no voltage hold-up in a reduced capacitance converter and so the full ripple voltage will be seen by the inverter. The output current will subsequently contain a 300Hz component (6 times the line frequency) which will produce a corresponding torque ripple. In the work carried out by Andersen *et al.* [15] a 12% torque ripple is seen due to this effect. For a fan load, this is not a problem unless the 300Hz modulation is audible. If smoother torque is required, the voltage ripple can be compensated for by modulating the PWM in anti-phase with the voltage. Upon implementing this technique, a 50% reduction in torque ripple was seen.

Similar work has been carried out by Kretschmar and Nee [16], but without torque ripple compensation. The inverter produced an almost pure sinusoidal current waveform despite the use of an open loop control system; this is most likely due to the higher motor frequency and simulated line inductance used during the tests. It is worth noting that line impedance is an often overlooked factor when considering the harmonic performance of a device, yet its effects can be significant. A highly inductive supply line is equivalent to adding a dedicated AC choke, and will therefore attenuate harmonics considerably.

2.1.2 Single-Phase Motor Drives

For single-phase systems the performance limitations resulting from a low capacitance DC link are much more severe, and therefore the intended applications must be carefully considered. This is due to the 100% ripple voltage observed when there is no DC link energy storage present. As with three-phase systems, the main application is in motor drives, where the inertia of the load mitigates the effect of torque ripple [17–23].

As shown in Figure. 2.2, a single-phase linear load will draw power in a time varying fashion. Assuming the load is linear, the input power varies as a function of sin^2, as shown in Equation. 2.1.

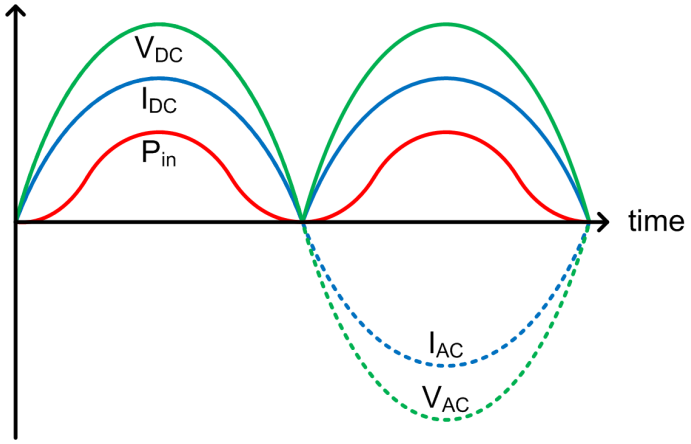

Figure 2.2: Ideal DC link voltage, current and input power waveforms for a single-phase load

$$P_{input} = \quad \hat{V}\hat{I}sin^2(\omega(t)) \tag{2.1}$$

Given that there is no decoupling available, the output power must therefore vary in the same manner, at the same time. Such oscillations in output power have long been accepted in domestic appliances through the use of universal motors, which can be found in products such as drills, vacuum cleaners and food processors. When combined with new brushless motor technology, this property can be capitalised on for improvements in power density, harmonics, efficiency and product lifetime.

Whilst it is possible to run a low capacitance drive using basic PWM control, its performance can be improved through the use of more advanced modulation techniques, as in a conventional drive system. As outlined in [22] and [17] Direct Torque Control (DTC) can be effective where a heavily fluctuating inverter supply exists. DTC allows the motor variables of flux and torque to be controlled directly by making calculations based on the measured motor voltage and current. The estimated flux and torque values are compared with a reference, and an error compensation is made by the inverter if they lie outside a set tolerance band. This works well with

a fluctuating DC link voltage, as the controller simply increases the power device conduction times as the voltage drops. For the majority of the mains cycle, full motor torque can be maintained by compensating for the voltage ripple, resulting in a trapezoidal torque profile as shown in Figure 2.3. Once the voltage falls below a certain point, the stator flux linkage cannot be maintained and the torque drops off. This is not a problem however, as excessive DC link voltage compensation will result in high distortion of the input current, causing the system to become self-defeating.

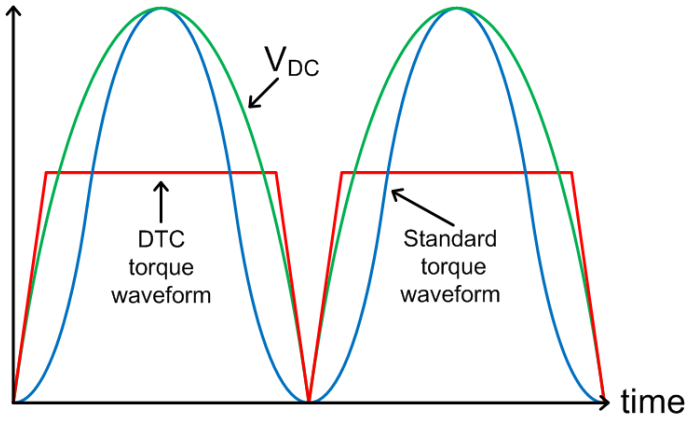

Figure 2.3: Trapezoidal torque profile resulting from DC link voltage compensation

DTC is a form of hysteresis control, and subsequently has a variable switching frequency. This complicates harmonic filtering and can induce resonances between the small DC link capacitor and line inductance. If this poses a particular problem, fixed-frequency techniques such as Space Vector Modulation (SVM) can be used instead, with the operating frequency set above the resonance [22]. The rapid integration and vector multiplication make DTC computationally intense, but given the speed of modern microcontrollers this is no longer an issue except in extremely cost sensitive applications.

Haga *et al.* [17] make use of the dither effect combined with DTC to simultaneously control the input current waveform and motor torque. Dither is a technique used to linearise non-linear systems by intentionally adding noise to a signal, in this case the converter input current. The inverter switching signals have a high frequency (dither) component superimposed on the motor control signals. The dither component is controlled such that it causes a sinusoidal input current to be drawn when passed through a low pass filter. Due to the frequency of the signal, the presence of

the small DC link capacitor is sufficient, removing the need for an AC input filter. The system behaves somewhat like a combined converter/inverter, but achieves input and output current control using a single power stage. Due to its linearisation properties, the dither effect can be applied to systems with a conventional DC link as demonstrated by Cacciato *et al.* [4].

As an alternative to DTC, Lamsahel and Mutschler [23] propose the use of Field Oriented Control (FOC) in low capacitance drives for domestic appliances. FOC is simpler to implement and has a fixed switching frequency, allowing the use of basic microcontrollers which results in lower cost products. A basic FOC system can successfully control a low capacitance drive, but the resulting motor torque has a high harmonic content. An improvement is seen when the D and Q axis current reference values are modulated by the DC link voltage. Although the input current is significantly more distorted than in [17], full compliance with BS EN 61000-3-2 is still achieved. This example reiterates the key challenge with reduced capacitance drive systems, in that torque ripple and input current distortion are in constant contention; a reduction in one results in an increase in the other.

2.1.3 Battery Charging

Another potential application for low DC link capacitance is battery charging, inviting the possibility of a combined power supply/fast charger sharing the same hardware. The key to making this work is sinusoidal modulation of the load (charging) power, in much the same way as it is with a motor drive. A similar challenge is presented, as conventional charging techniques often use a Constant Current Constant Voltage (CCCV) approach, producing a constant power load [24].

Due to their high energy density, lithium-ion cells form the basis for batteries in a vast range of products, from electric vehicles to mobile phones. This has naturally lead to research into understanding and improving the charging process [24–26], with a particularly relevant conclusion for this application; Sinusoidal Ripple Current (SRC) charging above 10Hz does not degrade the performance or lifetime of the cells. Furthermore, Chen *et al.* [24] demonstrated that by charging at the minimum AC impedance frequency, the cell temperature, lifetime and charging efficiency were notably improved over CCCV methods.

An important difference between a battery charger and a motor load is that whilst they can both tolerate large ripple currents, lithium ion cells require a tightly controlled charging voltage. This is a difficult problem to overcome in a system with minimal DC link capacitance and a high input power factor requirement. The expected 100% DC link voltage ripple seen in Figure 2.2 would be damaging if it was passed through to the cells, so a more elaborate power control method is necessary.

Research by Rosekeit and DeDonker [27] and Xue *et al.* [28] proposes a constant voltage sinusoidal ripple current charging technique which results in a very high input power factor from a compact converter design. Low value film capacitors are used in place of large electrolytics, saving valuable space and increasing the system lifetime, particularly important issues in the electric vehicle application. The chargers use a two stage approach as shown in Figure 2.4, with the full bridge front end providing power factor correction and DC link voltage regulation, and the Dual Active Bridge (DAB) providing charging current control.

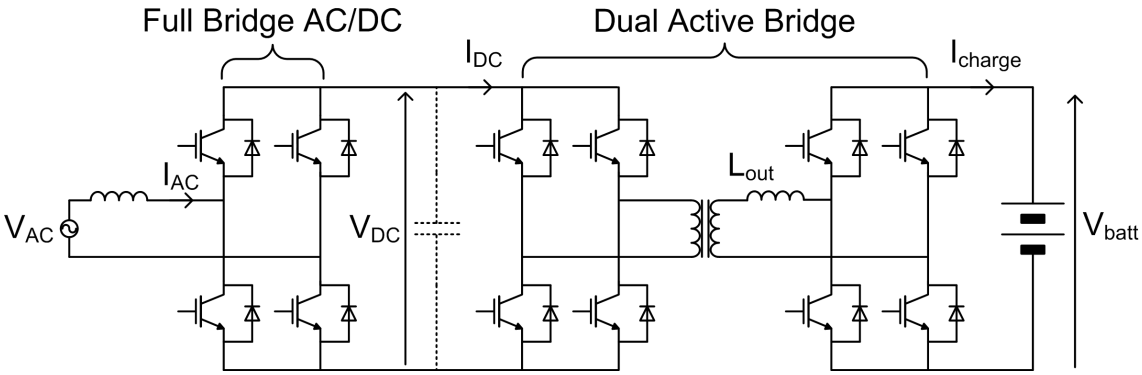

Figure 2.4: Battery charger with Full Bridge AC/DC stage and Dual Active Bridge DC/DC stage

Much like the low DC link capacitance motor drives discussed in Section 2.1.2 and 2.1.1, the charger uses the concept of instantaneously balanced input and output power to minimise the required energy storage. As the system is single-phase, this means the output power must vary sinusoidally, but without significant modulation of the charging voltage. The only option therefore is to force the charging current, I_{charge}, to have a sinusoidal component in phase with the converter input power as shown in Figure 2.5. Due to the transformer I_{charge} is equal to I_{DC} multiplied by the turns ratio.

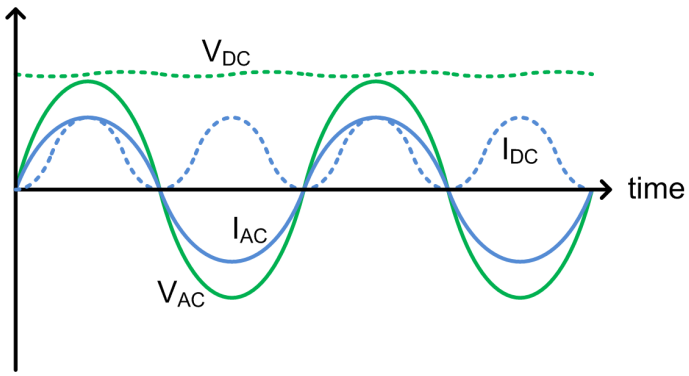

Figure 2.5: Key waveforms of the two stage low DC link capacitance charger

The input and output current control loops have a high bandwidth to ensure a significant imbalance does not occur, as this would produce a large fluctuation in the DC link voltage through the subsequent charging or discharging of the DC link capacitor. Theoretically, if the control system was fast enough the DC link capacitor would not be necessary other than to filter the power device switching noise, and would consequently be extremely small. In a realistic design such as [27] or [28], a certain amount of DC link voltage ripple will be produced however.

The dual active bridge is combined with L_{out} to produce current source behaviour, giving a predictable enough output to allow open loop control if desired. On the other hand it is noted in [28] that a larger current error is produced, requiring a larger DC link capacitor to account for the greater power imbalance. The error stems from the slightly nonlinear relationship between DAB phase shift (i.e. angle between inverter and rectifier bridge switching waveform) and output current.

A limitation of sinusoidal ripple current charging is that the mean charging power has to be reduced slightly to prevent over-voltage damage to lithium ion cells. The varying charge current will produce a corresponding voltage ripple due to the internal impedance of the cells, and the peak of this voltage cannot be allowed to go above a maximum value. So rather than charging constantly at the maximum allowable voltage, a reduced mean value must be used as shown in Figure 2.6.

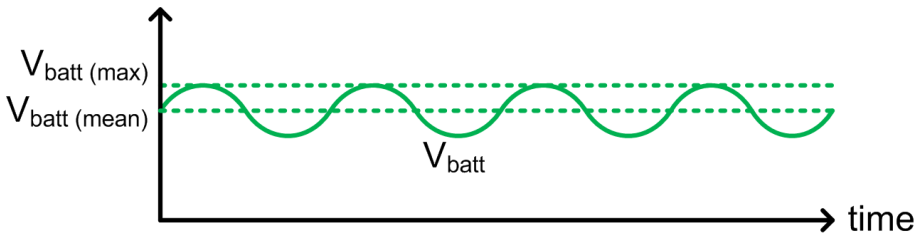

Figure 2.6: Reduction in mean charging voltage to prevent cell damage (exaggerated)

Despite the more stringent voltage regulation issue, battery charging lends itself well to the low DC link capacitance concept for two key reasons. Firstly, it presents a reasonably linear and constant load such that the converter input power always has a sink, and therefore does not require storage in reactive components. The second advantage is that the load time constant of a battery is very long, meaning that the reference value for the current control loop will subsequently change very slowly, helping to prevent second harmonic distortion of the line input current through changes in load behaviour [27]. This is the same reason that conventional Active Power Factor Correction (APFC) systems have a very slow voltage control loop (<20Hz), a point which is discussed further in section 2.3.2.

2.1.4 LED lighting

The use of LED lighting over conventional incandescent/fluorescent sources is becoming more popular as the technology is improved. There are a number of factors behind this, the most significant being high efficiency and increased lifetime. The most significant drawback is the low voltage DC operation and thus the need for a power supply which matches the performance of the LED modules themselves. Given the lifetime of LEDs is in the order of 50,000 to 100,000 hours this poses a problem for power supplies using electrolytic capacitors which will typically fail much sooner than this [29,30]. In response to the problem, research has been carried out [29–32] into the reduction of DC link capacitance such that longer lifetime 'dry' capacitor topologies can be used.

Unlike certain motor drive and battery charging applications, it is not desirable to have a sin^2 fluctuation in power with LED lighting due to the flicker effect this produces, and subsequently a large net reduction in energy storage is not possible. Despite the fact that conventional lighting systems produce flicker at twice the line

frequency (i.e. 100Hz in Europe), the effect is less severe due to the long load time constant. The brightness of an incandescent bulb does not vary significantly over one half cycle of the mains, and so the flicker it produces is equally small. This is analogous to the inertia of a motor preventing 100Hz modulation of its power from producing a noticeable variation in speed (discussed in section 2.1.2). LEDs on the other hand have virtually no load time constant and will produce a light output proportional to the instantaneous driving current, giving them a 'flicker depth' of 100% if driven from a sinusoidally varying power supply [33]. This means that over one half cycle of the mains, LEDs will transition from zero output to full output and back again. Although it is accepted that humans can only perceive light flicker up to approximately 70Hz, prolonged exposure to higher invisible frequencies can be detrimental to health, causing headaches, migraines and reduced visual performance [33].

The four power supply designs discussed in this section all get round the problem by using a large filter capacitor on the converter output, where the low voltage enables the use of long lifetime devices with a relatively high capacity. This removes the second harmonic ripple from the output, driving the LEDs with constant current and thus eliminating flicker. The high voltage DC link is still designed to have a large (but not 100%) ripple, requiring minimal capacitance which subsequently enables the use of film [30–32] or ceramic [29] devices instead of electrolytics. An advantage that LED power supplies have over other reduced capacitance converters is that their power rating is normally very low, meaning that less capacitance is required for a given DC link voltage ripple. For example, a 13.5W converter is designed in [32] with a 3uF DC link capacitance, small enough to allow a film device to be used. However, when the very low power (and therefore load current) of the system is considered, it can be seen that in a relative sense this is a significant amount of energy storage.

Due to the constant power output, all of the designs require an APFC stage to overcome the severe input current distortion that would otherwise result. The active shaping of the input current increases the short term imbalance between input and output power, causing a proportional increase in DC link voltage ripple. As identified by Gu *et al.* [30], the operational stability of the system is limited to the point at which the DC link voltage becomes smaller than the input voltage; an issue with any boost-derived topology. This is normally an unlikely scenario, as a conventional DC link design provides sufficient decoupling to safely limit the voltage ripple. In

this case however, the voltage on the DC link capacitor can change rapidly, potentially pushing the boost converter outside of its operating range, resulting in loss of input current control.

The reason for this is down to the fact that a boost converter can only provide uni-directional current control. By referring to Figure 2.7 it can be seen that the input current can always be increased by closing the switch (Figure 2.7 (a)) but it cannot necessarily be decreased by opening the switch (Figure 2.7 (b)) due to its parallel connection with the load. If the output voltage of the converter, V_{DC}, is less than the input voltage, V_{in}, then the load will draw current directly from the input rather than the capacitor. Under this condition the input current will be unregulated, resulting in distortion and therefore reduced power factor. If V_{DC} can be maintained above V_{in}, opening the boost switch will always cause the input current to fall, allowing total control of the input current shape. The boundary condition for stability is shown in Figure 2.8.

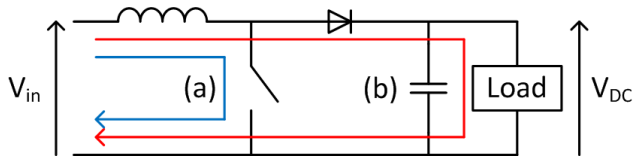

Figure 2.7: Uni-directional current control limitation of a boost converter PFC circuit

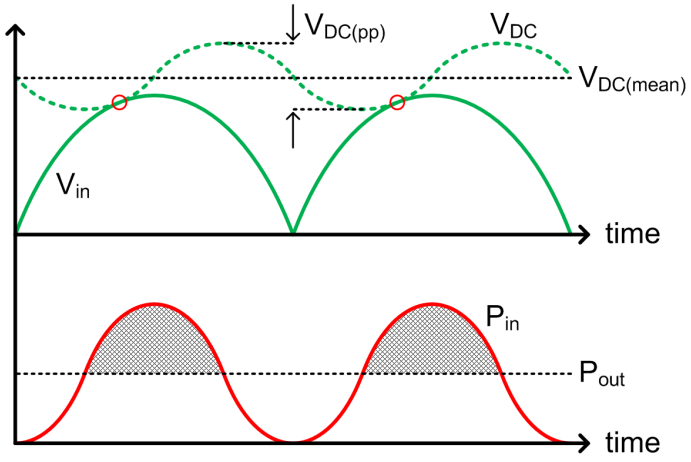

Figure 2.8: Stability limit for boost converter operation and DC link capacitor energy storage cycle

Three solutions to the boost converter instability issue are proposed. The first is to increase the mean capacitor voltage, $V_{DC(mean)}$, such that a given ripple magnitude, $V_{DC(pp)}$, cannot cause an intersection between V_{DC} and V_{in}. This can be achieved by increasing the mean duty cycle of the boost converter without altering the shape of the modulation waveform. The downside of this approach is increased stress on the components and a potential increase in cost if higher rated devices are necessary.

The second option is to reduce the ripple voltage by limiting the input-output power imbalance. As can be deduced from Figure 2.8 and 2.7, the integral of $P_{in} - P_{out}$ is equal to the change in DC link capacitor energy ΔE_c (the boost inductor stores a minimal amount of energy in comparison). The shaded area where $P_{in} > P_{out}$ is equal to the energy stored by the capacitor, and the area where $P_{in} < P_{out}$ is equal to the energy released. If the input power is allowed to move away from the ideal sin^2 shape towards the constant value of the load, ΔE_c will be reduced giving a corresponding reduction in the ripple voltage. The obvious downside of this approach is the input current will no longer be sinusoidal, decreasing the power factor.

$$E_c = \frac{1}{2}CV^2 \tag{2.2}$$

$$\Delta E_c = \int P_{in} - P_{out} \, \mathrm{d}t \tag{2.3}$$

The final and most complex option is put forward by Gu *et al.* [30], and involves injection of a 3rd harmonic component into the input current. Whilst this will clearly have an impact on power factor, it allows a greater level of voltage ripple before V_{in} intersects V_{DC}. By adding a 3rd harmonic signal to the APFC reference current, the input current and DC link voltage will be modulated in a corresponding fashion as shown in Figure 2.9.

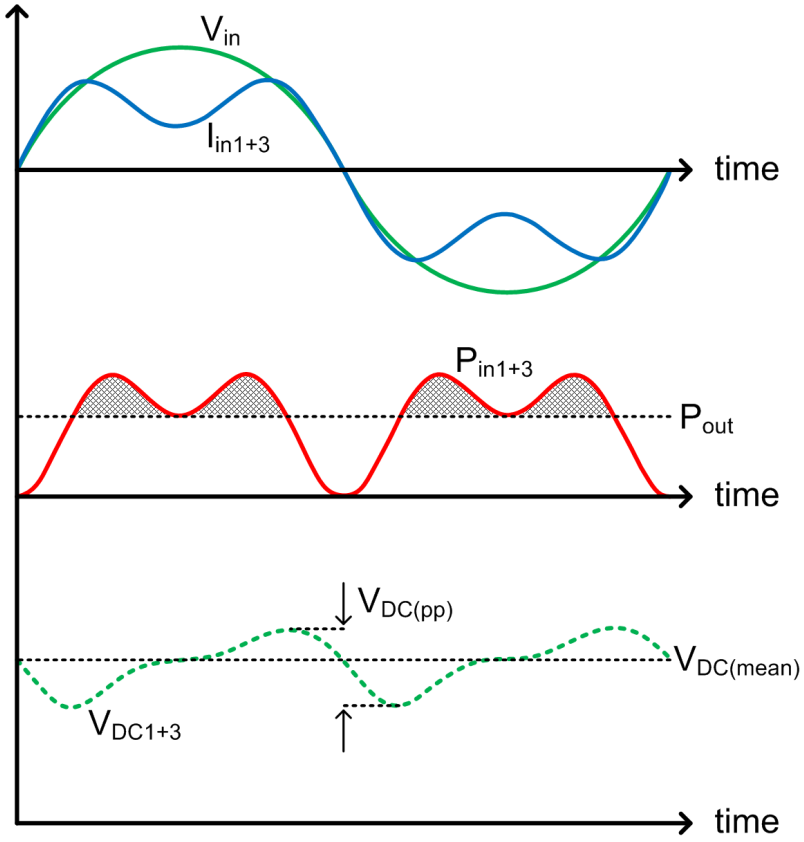

Figure 2.9: Modulation of I_{in}, P_{in} and V_{DC} with 3rd harmonic injection

Figure 2.10 shows that the 3rd harmonic component does not reduce the magnitude of the ripple voltage, but instead shifts the V_{DC} minimum point such that an intersection with V_{in} is avoided. The results in [30] show that for a given DC link voltage, the DC link capacitor can be reduced in size by 34% over a system without 3rd harmonic injection. This allowed the 60W converter to use a 2µF DC link capacitor where a 3µF device was previously required. The penalty for this improvement is a reduction in power factor from 1 to 0.9 due to the 3rd harmonic.

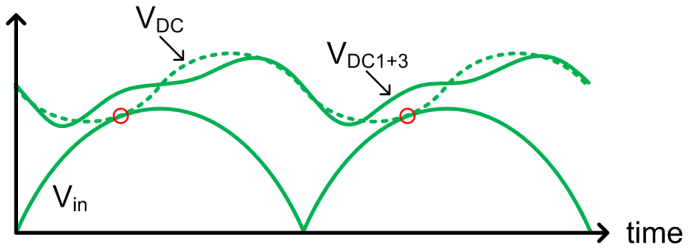

Figure 2.10: V_{DC} comparison showing the increased ripple voltage limit through 3rd harmonic injection

2.1.5 Auxiliary Ripple Energy Storage

The final application area for reduced DC link capacitance is in converters with an Auxiliary Ripple Energy Storage (ARES) system. Unlike the other applications discussed previously, converters with ARES can have small film based DC link capacitors without having to compromise on the DC side performance or introduce distortion to the AC side [3]. The advantage of such a system is best demonstrated by the poor energy utilisation of a conventional DC link capacitor. As described by Equation 2.3, the change in capacitor energy, ΔE_c, is equal to the difference between the input and output energy of the converter (i.e. integral of the power difference over time). In an ideal case the capacitor would be just big enough to store the peak input/output energy imbalance such that it is completely charged and discharged over every half cycle of the mains. This represents the theoretical minimum energy storage requirement, and thus the minimum capacitor size.

The difficulty with this is that a change in energy implies a change in voltage for a capacitor (see Equation 2.2), creating DC link voltage ripple which is unsuitable for many converter loads. If a small DC link voltage ripple is desired, then a small relative change in energy takes place as energy is proportional to voltage^2. For example, a DC link capacitor with a mean voltage of 400V and a ripple of 10V peak-peak has a relative energy change of 5% over half a mains cycle, meaning that 95% of the stored energy is unused. To overcome this issue an ARES converter is proposed in [3, 34–37] which involves storing the ripple energy in a capacitor which is not directly connected to the DC link, allowing its voltage to vary without affecting the DC link voltage. The auxiliary capacitor can therefore be much smaller than the equivalent conventional DC link capacitor. As shown in Figure 2.11, this system can be applied in situations where the mains is either the source (e.g. LED ballast) or the load (photovoltaic generator), and is particularly useful where long converter lifetimes require the use of film capacitors.

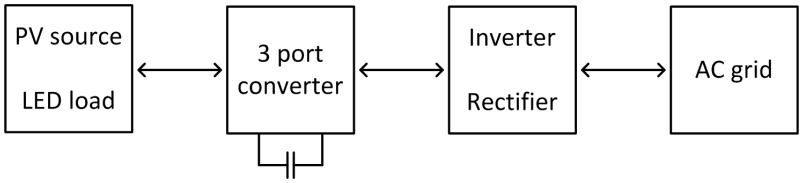

Figure 2.11: Auxiliary Ripple Energy Storage system block diagram

$$P_{aux} = \quad P_{DC} - P_{AC} \tag{2.4}$$

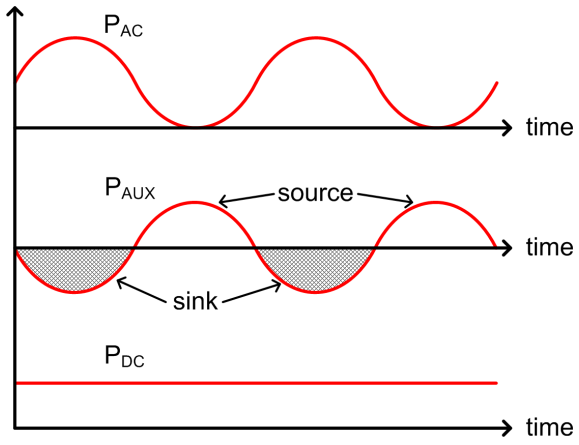

Figure 2.12: Waveforms showing the AC, DC and auxiliary power flow in the three port converter

The simplest implementation of the ARES converters proposed in [3,34,36,37] is put forward by Wang *et al.* [36], and can be seen in Figure 2.13. The auxiliary capacitor is connected to the DC link via a bidirectional buck/boost converter, allowing it to store energy when $P_{AC} > P_{DC}$ and release energy when $P_{AC} < P_{DC}$. Through appropriate modulation of switches Q_5 and Q_6, a stable DC link voltage can be produced from a heavily rippling auxiliary capacitor voltage. The DC link capacitor C_{DC} is small as it only serves to filter the power electronic switching noise from the buck/boost converter and provide a buffer for error in the ARES control.

In theory this arrangement allows the absolute minimum capacitor energy/size to be used as defined by Equation 2.3. For the design in [36] requiring 4% peak-peak ripple, this leads to a capacitor size reduction of 12.5 times over that of a conventional DC link set-up (1.6mF to 125µF). In practice this cannot quite be achieved due to limits on the auxiliary capacitor ripple current and the maximum converter duty cycle. It becomes impossible for the buck/boost converter to maintain a constant output voltage when the input (auxiliary capacitor) voltage becomes very small due to the extremely high duty cycle required. 200µF was found to be the practical minimum to maintain a 4% peak-peak ripple, a reduction of 8 times from the 1.6mF required with a conventional design. Use of the ARES converter in this case lead

to an overall power density increase of 100% for the PWM rectifier and enabled the use of long lifetime film capacitors where electrolytic devices would otherwise have been necessary.

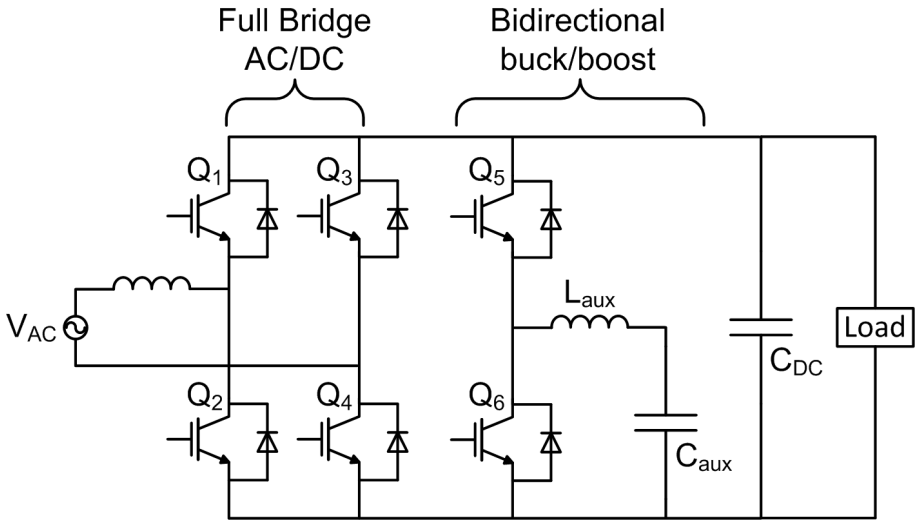

Figure 2.13: ARES converter topology used in [36] with full bridge APFC front end

2.2 Capacitor Technology

As discussed previously, reducing DC link capacitance can have a number of benefits when film based devices are employed. Recent improvements have made these capacitors suitable for high voltage, high ripple current applications such as the DC link of an offline power supply where electrolytic devices have traditionally been used.

As polypropylene capacitors have no electrolyte they do not suffer from 'dry-out' issues, and are also self healing, as faults are removed through vaporisation of the electrode in the region of the short. This provides a significant advantage for many power electronic systems as electrolytic capacitors will normally be the first components to fail, often in short-circuit which creates a high risk of explosion [19, 38]. It is for these reasons that film based capacitors exhibit failure rates almost two orders of magnitude lower than electrolyic devices [3]. In the consumer electronics market however, this feature can be of limited value as product lifetimes are often less than a few thousand operating hours. As a point of comparison, at 85^{o}C Epcos MKP polypropylene capacitors have an Mean Time Between Failures (MTBF)

of 200,000 hours, whereas their B43564 electrolytic devices have an MTBF of only 15,000 hours [39]. It should be noted however, that 85^oC is typically the maximum temperature polypropylene devices can handle without de-rating; for every 10^oC above this the life expectancy is approximately halved [40] [41].

Polypropylene devices possess an extremely high dielectric strength, allowing them to be rated for operation well above 1000V DC and thus removing the need to use series/parallel connected capacitors across a high voltage bus. This is advantageous in that capacitor balancing is not required, and a single component can replace a number of smaller components, potentially reducing manufacturing time and cost.

A further benefit is that of minimal equivalent series resistance, which gives rise to low power dissipation and therefore high ripple current handling capabilities. For example, a 2.2µF 450V Epcos MKP polypropylene capacitor has a ripple current rating of 7.5A [39]. An equivalent Panasonic NHG electrolytic capacitor has a rating of only 29mA [42]. To put this into perspective, building up a ripple current rating of 7.5A would require 259 electrolytic capacitors in parallel. This would clearly be impractical, outweighing the capacitance to volume advantage that electrolytics have. This represents a common problem when specifying DC link capacitor values, and is often rectified by over-rating the capacitance in order to achieve an appropriate ripple current rating.

The use of stacked polypropylene film layers give the devices a much reduced equivalent series inductance when compared with spiral-wound electrolytic designs. This aids in mitigating the DC link voltage spikes induced by power device switching, as demonstrated in [40] where voltage overshoot was reduced by 58%. This reduction was significant enough to allow all of the DC link snubber capacitors to be removed.

Polypropylene devices are stable over a wide range of operating conditions; within the specified operating range, the performance of polypropylene capacitors is not significantly affected by temperature, humidity or frequency. ESR and capacitance values are virtually constant under all rated conditions (+/-2%), making them far easier to specify for a particular application. For electrolytic devices, a 20% change in capacitance over the rated temperature range is not unreasonable [39].

Despite the many advantages of film capacitor technology, electrolytic devices remain the popular choice for two main reasons; capacitance to volume ratio (factor of 100x higher) and capacitance to cost ratio (factor of 10x cheaper). Having said this, the cost can be offset somewhat by the saving in reduced EMI filtering requirements. In applications such as line frequency filtering, where large amounts of capacitance are required, electrolytic devices remain the obvious choice [2]. However for this application, where a very high ripple current to capacitance rating is required, the advantages of electrolytic devices are negated. Not only this, but their use is virtually impossible as an excessive capacitance rating is required to achieve the ripple current handling, defeating the point of a low capacitance DC link system.

2.3 Power Factor Correction

As discussed in the introduction, the ever increasing number of electronic loads on the mains has made power factor an important issue. With the introduction of Electro-Magnetic Compatibility (EMC) standards such as EN 61000-3-2 it is a requirement for mains connected loads to have a minimum harmonic performance [7]. Almost any load with an AC/DC conversion stage will require some form of power factor correction circuitry in order to meet this standard, making it an area of considerable interest for the electronics industry. As always in the consumer market, the challenge lies in meeting this specification at a minimum cost and generally in the smallest package possible. At the higher end of the market, further voluntary standards can be met to provide an additional selling point to the customer. One such standard is Energy Star, a government-backed initiative which highlights particularly energy efficient products, and in many cases includes a minimum power factor rating (e.g. >0.9 at 100% load for a computer power supply) [43]. This section of the thesis provides an overview of the current techniques available for meeting these standards, with a particular emphasis placed on low complexity and cost.

2.3.1 Passive PFC

A simple, reliable and efficient approach to reducing load harmonics from an AC/DC converter is the addition of a passive filter. In many cases this will simply require an inductor to be placed between the supply and the bridge rectifier. A further

benefit of the passive approach is that no additional EMI is created as there is no high frequency switching involved. The basic nature of this modification allows it to be retrofitted to existing designs to make them compliant, generally increasing the power factor from under 0.7 to around 0.9 [4]. However, the level of improvement seen is greatly affected by variations in load and input voltage, and furthermore the low cutoff frequency of such a filter makes the input inductor very large. The fixed component values of a passive PFC approach also mean that it will not work with universal line voltage (85-250V) which is vitually a given feature of modern electronic equipment. Resonant LC filters can be used to target specific harmonics (generally the third, fifth and seventh) and achieve a greater power factor, but the additional size and cost of the reactive components makes this uneconomical for many applications. Despite these drawbacks, for very cost sensitive and low performance applications the simplicity of a passive PFC system often makes it the preferred approach.

2.3.2 Active PFC

Conventional APFC Hardware and Control System

In order to overcome the poor performance, size and adaptability of passive PFC techniques, a range of active solutions have been created [44]. For low cost single-phase applications, the most common approach is to place a boost converter after the diode bridge as shown in Figure 2.14. This arrangement benefits from a low side/grounded switching device and an input side inductor which allows for Continuous Conduction Mode (CCM) current, reducing the amount of EMI filtering required. The addition of this active element allows for precise shaping of the input current, achieving unity power factor over a wide range of input voltage and load conditions. Regulation of the DC link voltage also allows the design of the load or secondary DC/DC stage to be optimised around a specific operating point [45]. The main disadvantage of a boost derived solution is that the output voltage, V_{out}, must be greater than the input voltage, V_{in}, which places additional stresses on the switching components.

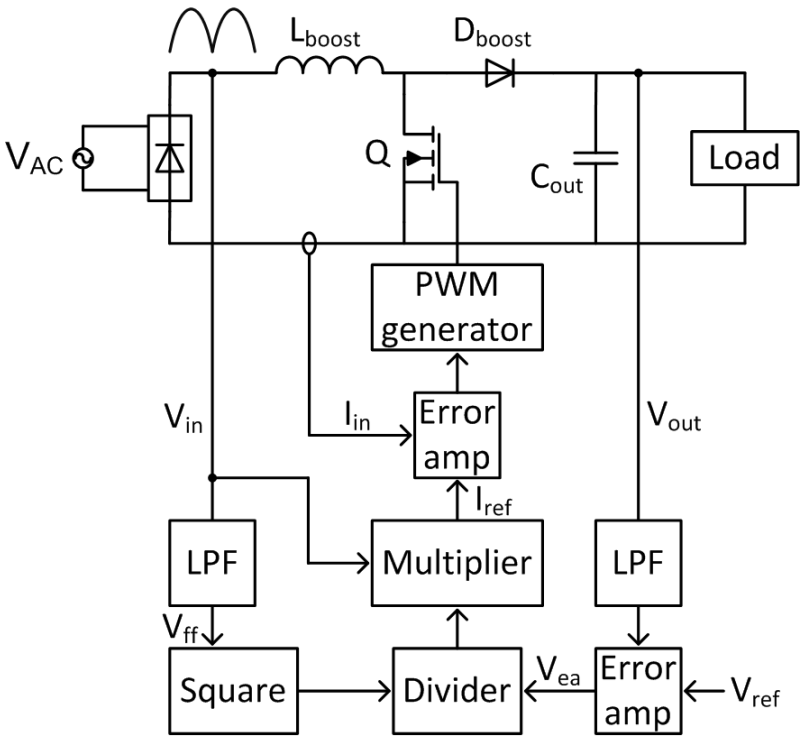

Figure 2.14: Hardware and control for a conventional boost APFC system

The primary function of the boost PFC system is to shape the input current, I_{in}, to be proportional to the input voltage, V_{in}, thus making the load appear resistive. This is carried out by actively controlling the boost switch such that the input current tracks a reference, I_{ref}, as closely as possible. To achieve the lowest input current distortion, CCM control is used whereby the input current does not fall to zero between switching events (see Figure 2.15). For situations where higher input current distortion can be tolerated, Discontinuous Conduction Mode (DCM) may be used with the benefits of reduced swiching frequency and/or inductor size, as well as reduced control complexity given that the input current is zero at the start of each switching event (see Figure 2.16).

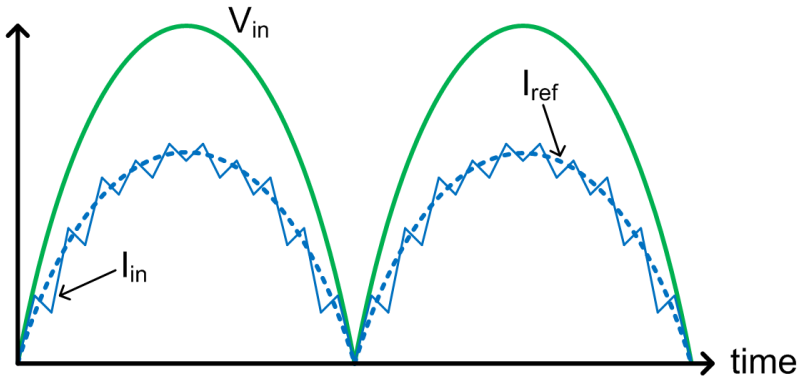

Figure 2.15: Boost APFC waveforms showing input current tracking reference in CCM

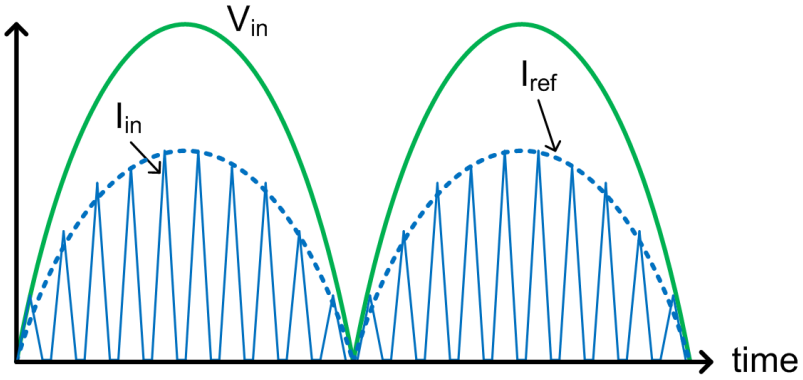

Figure 2.16: Boost APFC waveforms showing input current tracking reference in DCM

The secondary function of the boost PFC system is to regulate the output voltage. Conventionally this is a stable DC voltage with a small ripple component dependent on the size of the DC link capacitor. The output voltage is controlled by altering the mean amplitude of the reference current signal. As can be seen in Figure 2.14 this signal is generated by multiplying the rectified line voltage, V_{in}, with the output of the voltage error amplifier V_{ea}. The current reference therefore has a shape which is proportional to the input voltage and a mean amplitude dependent on the output voltage error.

Before the voltage error signal reaches the multiplier, it is first divided by the square of the mean input voltage (V_{ff}) in order to keep the gain of the voltage control loop constant. This is required because the mean input voltage will vary with changes in

the mains supply voltage, and would otherwise affect the power of the system. For example, if the mains voltage were to double, V_{in} would double causing the output of the multiplier block (I_{ref}) to double. For a constant power load, if the input voltage doubles the input current must halve, so clearly the previously described operation would not be appropriate. However, by dividing the voltage error signal by the square of the mean input voltage, the current reference will be reduced proportionally, maintaining constant input power [46].

The simultaneous regulation of input current and output voltage with a single switch poses somewhat of a problem for the control system. By forcing the input current to be proportional to the input voltage, the input power becomes a sin^2 function at twice the line frequency. This causes the DC link capacitor to be charged/discharged at the same frequency, creating a ripple voltage which lags 90 degrees behind the charging current. Eliminating this voltage ripple would require a high bandwidth voltage control loop to modulate the reference current amplitude, subsequently distorting the input current shape. The contention between the two aspects of the control system means that the only way to achieve the desired result is to have a fast current control loop and a slow voltage control loop (typically < 20Hz) which will not distort the input current shape. A very large DC link capacitor is required to account for the low bandwidth of the voltage regulation and smooth the second harmonic power flow.

A further challenge is presented in the form of second harmonic ripple in the V_{ff} and V_{ea} signals. Despite using a low pass filter to generate these signals from the input and output voltages, a certain amount of second harmonic will still be present. This distortion passes through the divider and multiplier, affecting the reference current and therefore the actual input current. When passed through the diode bridge, the second harmonic creates both a third harmonic and a fundamental component phase shifted 90 degrees from the input voltage, increasing the distortion and displacement of the input current which reduces the power factor.

Ripple in the feedforward voltage signal (V_{ff}) clearly needs to be low if a high power factor is to be achieved, implying the need for a lowpass filter with a very low cutoff frequency. The downside of this is that the system will have a very slow response to changes in input voltage. Conventionally a compromise is made by using a two pole filter which will have a faster transient response for a given attenuation, with

the added benefit of phase shifting the second harmonic by 180 degrees, removing the phase displacement issue mentioned previously. A similar issue exists with second harmonic ripple in the output voltage error signal, requiring the error amplifier to shift the ripple by 90 degrees to bring it back in phase with the input voltage [46].

Alternative APFC Control Systems

The use of a conventional APFC control system with reduced DC link capacitance poses a considerable problem. Not only is there little energy storage to buffer the already low bandwidth voltage regulation, but the very large DC link voltage ripple requires the input to the voltage error amplifier to be heavily filtered. As discussed in the previous section, it is necessary to remove the ripple from the DC link voltage measurement to prevent it from modulating the input current reference. Where a conventional APFC system will typically have less than 10% DC link voltage ripple, a reduced capacitance converter has up to 100% ripple. It is therefore necessary to have ten times the attenuation (-20dB) to produce the same amount of ripple in the DC link voltage sensor signal. For a first order lowpass filter (-20dB/decade rolloff) this requires the cutoff frequency to be reduced by a factor of 10, resulting in a proportional reduction in the control system bandwidth. Subsequently, such a system would only work if the input voltage and load conditions could be guaranteed to change at a very slow rate, greatly limiting the range of possible applications.

A number of options are available which avoid or improve the voltage control bandwidth issue by breaking the twice line frequency bandwidth limit [47]. One option is to place a notch filter between the divider and multiplier blocks to remove the second harmonic ripple. This allows the voltage control loop bandwidth to be increased, improving the dynamic response of the system and reducing the DC link voltage ripple. Research by Williams [48] demonstrated that the addition of a notch filter with a Q factor of 10 tuned to the second harmonic frequency allowed unity input power factor to be maintained whilst reducing the the output voltage ripple by 73%. Two limitations of this approach are noted; very tight component tolerances are required to obtain the high Q factor and the filter will only work at the precise tuned frequency, ruling out operation at 50Hz or 60Hz without modification. However, this research was carried out before the prevalence of low cost microcontrollers, and as such an adaptive and precise digital filter could potentially alleviate these issues.

An alternative approach is not to use a multiplier based controller and instead operate the boost converter in discontinuous conduction mode, allowing the system to behave as a natural voltage follower [45]. By allowing the input current to fall to zero after each switching event, it will have a mean value proportional to the input voltage as can be seen in Figure 2.16. When the boost switch is closed, the boost inductor is shorted across the mains supply and therefore the input current ramp rate is dependent solely on the input voltage and not the load. Given a fixed switching time period, mean current is proportional to $\frac{\delta i}{\delta t}$ and therefore voltage, allowing the current control loop and input current sensor to be removed. This type of control is best suited to applications where higher input current distortion can be offset against reduced cost, control complexity and boost inductor size [49]. Work by Caruso *et al.* [50] has shown that the use of this technique can lend itself well to drives used in domestic appliances as the operating conditions are generally predictable and known in advance. As DCM operation is necessary for the voltage follower behaviour to take place, it is common for other hardware topologies such as flyback, SEPIC or Ćuk to be used which do not require V_{out} to be higher than V_{in} and also provide galvanic isolation.

Rather than removing the current sensor as with the DCM voltage follower technique, other control system designs have been produced to eliminate input voltage sensing [51, 52]. Similarly, this approach is most effective where the operating conditions are known in advance, allowing predictive open loop control to compensate for the lack of feedback. The steady state transfer function of the power converter and load is used to derive a non-linear PWM sequence which results in a high input power factor. As input current sensing is still present, CCM operation is possible which improves the power factor over DCM approaches, with the design in [52] exceeding the performance of a conventional APFC system with complete voltage and current feedback information. An alternative design is put forward by Ohnishi and Hojo [53] which has no input current or DC link voltage sensors, and relies solely on an input voltage measurement with semi open-loop control. The control system is simple and low cost, producing a high quality input current waveform, but is dependent on a predictable known load and stable DC link voltage in order to function properly. Such 'sensorless' techniques are therefore challenging to implement with a reduced DC link capacitance system. The authors suggest it is well suited to an application such as a lighting dimmer where the load does not vary and the cost must be minimised.

For very cost sensitive applications, there are power factor control schemes which meet the requirements of EN 61000-3-2 but do not necessarily produce a high power factor [54–60]. Conventional AC/DC converters with a power rating of between 75W and 600W will normally fall into the Class D category of equipment due to having an input current waveform shape which falls within the envelope shown in Figure 2.17 for at least 95% of each half period of the mains.

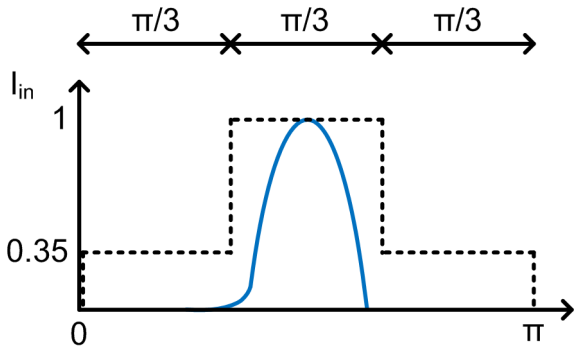

Figure 2.17: Class D input current envelope for EN 61000-3-2

At low power levels the Class D regulations are much harder to meet than Class A (see Table 1.1) as the harmonic limits are scaled by the amplitude of the fundamental. Considerable leeway can be gained by using a simple power converter which modifies the input current shape sufficiently to allow the device to be reclassified. One method of doing this is put forward by Rossetto *et al.* [59] which uses a boost converter switched at the second harmonic frequency (100Hz) to cause current flow outside of the Class D envelope. The boost switch turn-on is at a fixed time after the mains zero crossing, and the turn off time is controlled by the output voltage regulator. The benefits of this approach are low control complexity and a low switching frequency giving rise to minimal losses and EMI filtering requirements. The change from Class D to Class A allowed the filter inductor to be reduced from 19mH (passive PFC) to 6mH (active PFC) whilst gaining output voltage regulation a the same time. The EMC reclassification idea is also used by García *et al.* [54] but is implemented using flyback and forward-derived converters to allow power factor control and an isolated, low voltage output in a single stage [61].

For higher power low cost applications, single stage PFC and DC/DC converters exist based around the full bridge topology [55–58, 62, 63], combining the functions of a boost converter and H-bridge with little or no additional power devices. One

of the simpler implementations by Moschopoulos [57] is shown in Figure 2.18, with the key feature being the connection of L_{boost} to the drain of Q_2 rather than the drain of Q_1. This simple change allows Q_2 to control the input current in much the same way as with a conventional boost converter, with Q_1 or its body diode acting as the boost diode. The component layout of this approach has an advantage over the simpler forward-derived converters in that CCM operation can be achieved, in some cases allowing compliance with the Class D harmonic standards. The single stage approach still ultimately limits the power factor that can be achieved, in this case due largely to the fact that the boost and H-bridge functions are interleaved, meaning that input current control only takes place during the freewheeling phase of the load cycle [62]. Using the FET body diode to carry a significant proportion of the boost freewheeling current can also lead to excessive losses, as this component is typically much slower than the dedicated ultrafast discrete part that would normally be used.

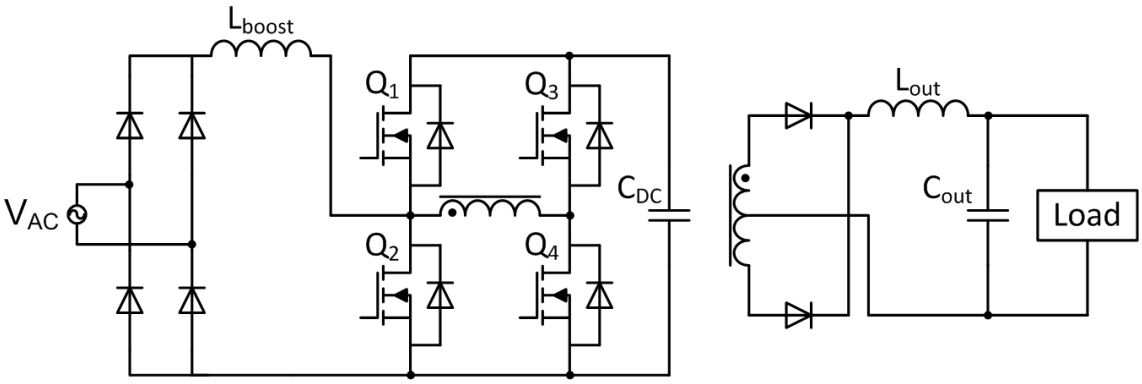

Figure 2.18: Integrated H bridge and boost converter with no additional power devices

As mentioned in Section 2.1.2, it is possible to use existing power converter hardware to improve the input current shape through use of the Dither effect [4]. Dither is often used to linearise non-linear systems that have a dead-band in their behaviour, in this case the gaps in input current conduction of a standard AC/DC converter (see Figure 1.2). A high frequency oscillation is injected into the motor drive inverter signals (but could equally be applied to a DC/DC converter) which does not create any net torque but generates short additional time periods where V_{in} is greater than V_{DC}, thus allowing input current flow over a larger proportion of the mains cycle and

subsequently improving power factor. Much like the designs mentioned previously, this approach meets the European harmonic standards at the minimum possible cost, passing the regulations whilst still having 45% THD of the input current.

As well as the need to meet low frequency current harmonic (EMC) regulations, mains connected equipment must also meet high frequency EMI regulations which poses a challenge when designing a compact power converter. The reduction of low frequency current harmonics with an APFC system will generally require the use of a high frequency switching action to control the input current, which itself produces considerable distortion to the mains voltage. An additional filter is required to remove this to achieve compliance with all the relevant standards, highlighting the need for a design compromise to be found. As mentioned previously, the use of DCM reduces the size of the boost inductor, but the increased switching frequency noise forces the use of a larger EMI filter, meaning that a net size reduction is not necessarily produced. The optimum combination of design parameters is therefore application specific, but the best results are achieved by aiming to meet only the precise requirements of the standards, much like the Class D to Class A waveform modification outlined previously. For example, a non-linear relationship exists between switching frequency and minimum filter size as the EMI regulations only begin at 150kHz, meaning that frequencies below this are exempt from testing. Increasing the APFC switching frequency from 140kHz to 160khz will in fact *increase* the required filter inductor size despite the fact that the harmonic distortion will have fallen [64, 65]. Careful consideration for these design trade-offs must therefore be made in order to produce the most compact solution overall.

Active Power Filters

An Active Power Filter (APF) is an alternative system for controlling harmonic and reactive power flow on the grid. It is typically used to improve the power factor of a large system with many connected loads, sensing and cancelling their net harmonic content and phase displacement [66]. These power converters normally feature four quadrant operation to allow both sourcing and sinking of reactive power flow, making them potentially more complex than an APFC system which typically only have control over current in one direction (sink). Another key difference is that APFs are generally connected in a parallel shunt arrangement with the non-linear load, only processing the reactive portion of the power flow (see Figure 2.19) [67, 68]. This

increases the efficiency over that of an APFC system which has to process the entire load power [69].

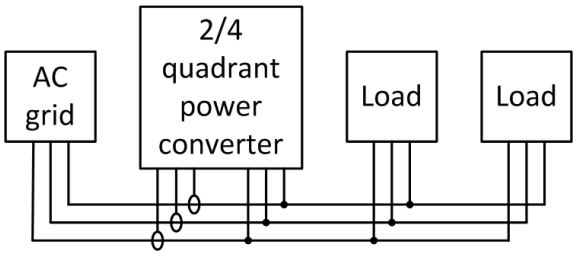

Figure 2.19: Use of an active power filter for controlling the net reactive power from a number of systems

Clearly a complex four quadrant converter is not suitable for power factor control in a low cost appliance, but the basic operating principle can be used in a two quadrant APF placed after the rectifier in an AC/DC converter. In terms of hardware, such a system is in fact very similar to the auxiliary ripple energy storage system discussed in Section 2.1.5, using a bi-directional buck/boost converter connected in parallel across the DC link (see Figure 2.20). Current harmonics on the DC link are sensed, and then an equal and opposite compensation current is injected by the APF to cancel them out, resulting in a pure sinusoidal input [69]. The compensation current is calculated by subtracting the non-linear load current from the active component of the fundamental load current [67]. This approach to power factor correction lends itself well to a reduced DC link capacitance system where the fundamental load current naturally follows the line voltage. The level of energy storage in C_{aux} only has to be sufficient to supply the lowest frequency harmonic power component, which will generally be less than the fundamental. If the load harmonics are all at a high frequency, the APF energy storage can therefore be made very small.

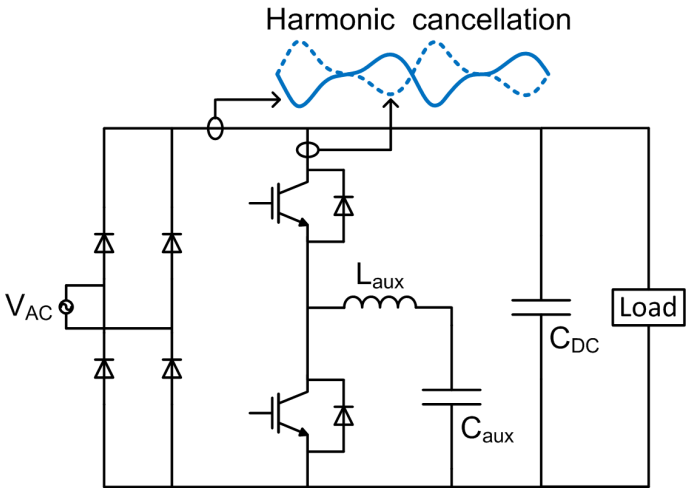

Figure 2.20: Two quadrant DC side active power filter

Antiwave APFC Control System

An APFC system of particular relevance to this thesis is the Antiwave control technique developed by Smith in collaboration with Dyson Technology Ltd [70]. It was designed to be an extremely low cost active power factor correction system for a 1600W BLDC motor drive which also made use of reduced DC link capacitance. The motor drive load current naturally follows the DC link voltage giving rise to the sinusoidal envelope seen in Figure 2.22. Even before power factor correction takes place, the load current shape resembles that of a discontinuous APFC system (see Figure 2.16), albeit with lower frequency switching harmonics. The input current therefore contains little low frequency distortion, leaving the APFC system to deal with only the switching frequency component. As discussed in Section 2.3.2 this limits the amount of energy storage required for power factor correction, making the overall system more compact.

The hardware for the Antiwave APFC and motor drive system can be seen in Figure 2.21. A boost converter has been added between the rectifier and H-bridge of the standard motor drive with its control coming from the existing microcontroller to reduce the cost. The most notable feature of this system is the lack of any voltage or current sensors for control of the boost converter making it completely open loop. Having accurately characterised the system, a predefined PWM sequence can be used to drive the boost switch generating a compensation current, I_{comp}, in anti-phase with the load harmonics, I_{load}, which results in a sinusoidal input current I_{in} as shown in Figure 2.22. The Antiwave PWM sequence is synchronised to the motor

drive switching signals, allowing it to operate without any sensors. The control difficulties arising from DC link voltage ripple and line voltage variation do not occur in this case as they are not measured. As the motor drive automatically adjusts to variations in supply voltage there is no need for the APFC system to compensate for this.

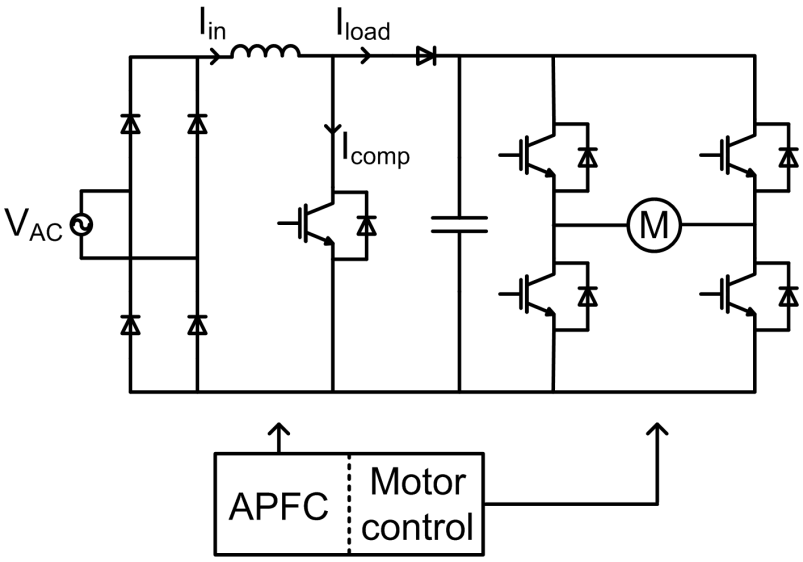

Figure 2.21: Hardware for the Antiwave APFC and motor drive system

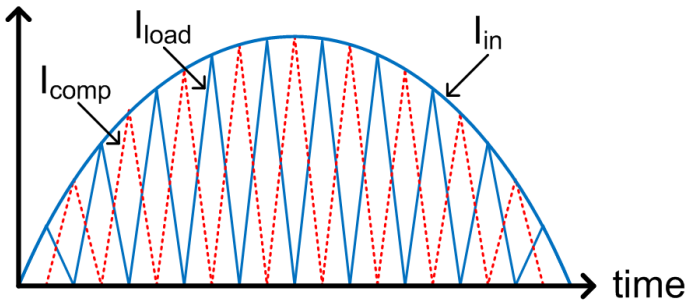

Figure 2.22: Antiwave load harmonic compensation producing a sinusoidal input current

The highly application specific nature of this system is its main drawback, requiring accurate characterisation of the load and limiting its adaptability. A further challenge in using it in a portable power supply is the need for a data connection between the load and APFC controller to allow estimation and cancellation of the

load harmonic current. This adds significant cost and complexity to a system ultimately designed with the opposite intention.

2.4 Conclusion

For loads which can tolerate a large ripple in the supply voltage and/or current, reducing the DC link capacitance can improve power density, power factor and reliability, as well as reducing cost. Fan based motor loads are particularly well suited as line frequency torque ripple does not generally affect their performance. The key to making this work in any system is the balancing of instantaneous input and output power flow, a considerable challenge in single-phase systems where the power must vary sinusoidally. This highlights a compromise between input and output power quality, particularly in single stage systems such as low cost motor drives where smoothing torque ripple will increase input current distortion.

All of the existing single-phase reduced capacitance systems are either too complex, expensive or under-performing for this application. An absolute minimum of active components, processing power and filtering is necessary in order to produce a viable solution. There is a need to exploit the ability of the motor drive to handle sinusoidal power flow and therefore reduce the harmonic filtering requirements.

Active power factor correction is necessary for the reduction of input current harmonics without using large additional filter components. The boost topology will give the best overall input current quality whilst maintaining a low cost. However, there are no existing control systems suitable for use with 100% DC link voltage ripple, highlighting a valuable area of research. The challenge lies in generating a reference input current signal which is proportional to both the input voltage and load power. A number of open-loop and waveform modification techniques have been considered which avoid this issue, but the resulting input current quality is not sufficiently high for this application, particularly if the power level were to be scaled up. Where a boost PFC front end is used with a heavily rippling DC link, a further challenge is presented in maintaining control stability such that the mains input voltage does not exceed the DC link voltage. At this point, control over the input current shape is lost.

DC-side active power filters demonstrate a method of direct harmonic cancellation which lends itself well to a reduced DC link capacitance system, given the minimum energy storage requirement is determined by the load harmonic frequency rather than the line input frequency. Implementation of the APF control approach in a more cost effective manner holds promise for the power factor correction needs of this application. The Antiwave APFC technique takes a similar approach of directly cancelling load harmonics and has been shown to work with limited DC link capacitance. Adapting such a scheme to function in a closed loop manner may allow it to work in a power supply application where load feedforward information is not practically available.

Chapter 3

The Reduced DC Link Capacitance Power Supply and Motor Drive

Having identified low performance motor drives as an ideal application for reduced DC link capacitance, this chapter describes the development of a power system suitable for building on the work found in the literature review. The starting point is a high speed BLDC compressor motor designed by the industrial sponsor for its portable products. This chapter begins by outlining the design and operation of the standard motor drive, in order to provide a clear understanding of its behaviour before being modified. The key parameters are used to build a simulation model of the motor drive, which is then verified against actual hardware measurements.

The first major hurdle to overcome was the fact that the motor drive was designed to operate from a 24V DC supply. Whilst it would have been simpler to start with a high voltage system, there were two reasons this motor drive was chosen. Firstly, the addition of a DC to DC converter provided another platform on which to analyse the effect of reduced DC link capacitance. No previous research was found relating to this application and it was therefore seen to have potential for novelty. Secondly, the industrial sponsor for this work had a significant interest in making further improvements to the motor drive system, giving access to a range of resources which would otherwise be unavailable.

The second half of this chapter includes the research and design of a compact and low cost power supply based on the reduced DC link capacitance concept. The key factors affecting the performance, size and cost of the system are discussed, leading to the development of a second simulation. This works in conjunction with the mo-

tor drive model to produce a complete system simulation which is later validated in Chapter 4. The final section of this chapter covers the practical implementation of the power supply, derived directly from the simulation model.

3.1 The 200W 100,000RPM BLDC Motor Drive

This section describes the salient features of the 200W BLDC motor drive used extensively in this research. It was originally developed by Dyson for its handheld vacuum cleaners, meaning that the motor had to be very compact, efficient and lightweight, whilst also being low cost. As can be seen in Figure 3.1, the motor is a two-pole 'C' core design integrated with the drive into a single package. This removes the need for wired connections and allows the power devices to sit within the high speed airflow from the compressor, cooling them sufficiently without heatsinks.

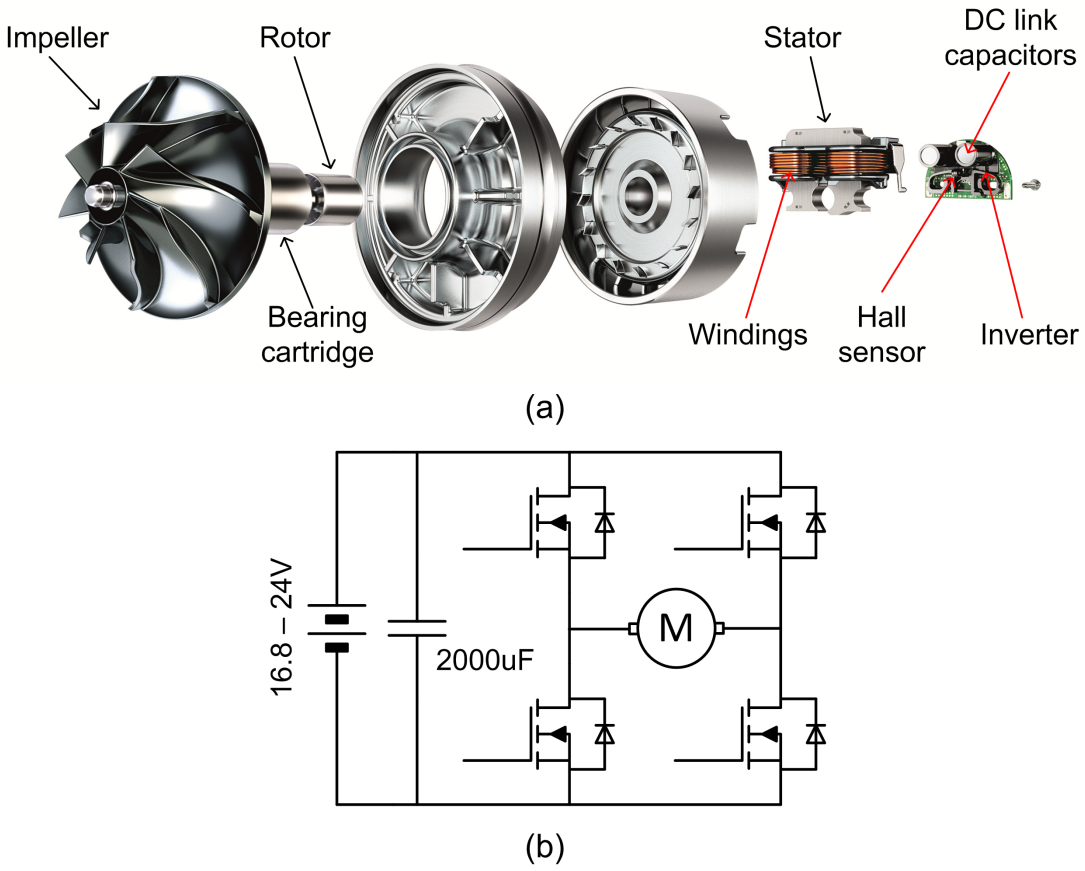

Figure 3.1: The 200W 100kRPM BLDC motor drive (a) exploded view (b) simplified circuit diagram

The power supply for the motor drive is a lithium-ion battery pack with 2000uF of DC link capacitance to limit the current ripple. A basic 8-bit microcontroller constantly adjusts the motor switching angles based on the supply voltage and RPM, allowing the drive to produce a continuous 200W output power across the whole battery voltage range (16.8-24V).

Given that the torque, T, a motor can produce is proportional to its size, Equation 3.1 explains why the motor has to operate at extremely high speed, ω, to produce the required output power, P_{output}, from a small package.

$$P_{output} = \quad T\omega \tag{3.1}$$

As discussed by Leaver *et al.* [71], above 100,000 RPM bearing loss, iron loss, critical speeds and manufacturing tolerances become very significant, meaning that further increases in speed can actually lead to an increase in size and cost.

The motor is controlled using a relatively simple system that avoids the use of pulse width modulation. The high operating speed, when combined with an appropriate winding inductance, Back ElectroMotive Force (BEMF) and phase voltage create a quasi-sinusoidal phase current from a square-wave driving voltage. As the current waveform does not have to be modulated, the switching frequency is very low, reducing losses and computational demand. The key motor drive waveforms can be seen in Figure 3.2(a).

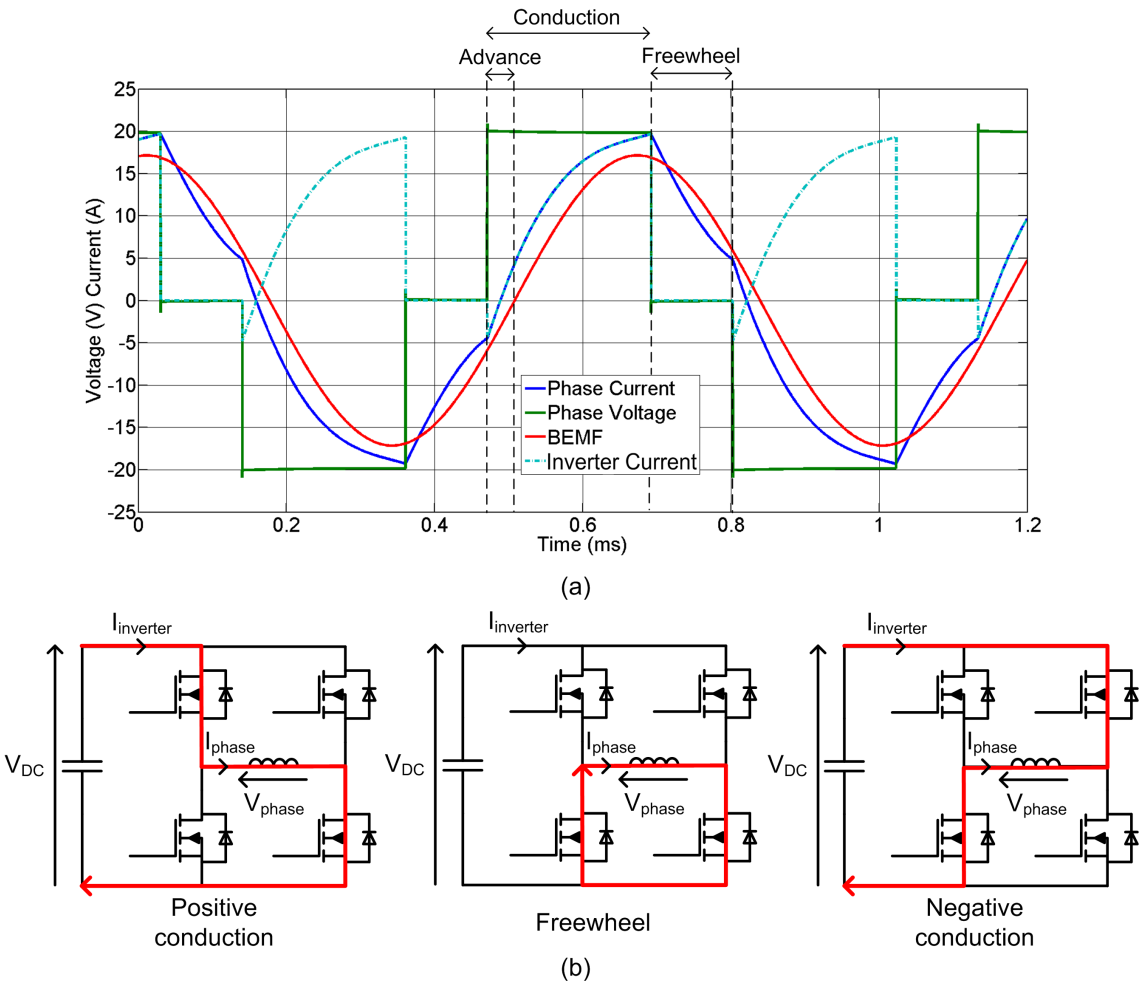

Figure 3.2: (a) Key motor waveforms and (b) the relevant H bridge switching states

The phase voltage waveform is generated by an inverter with two main switching states; conduction (positive/negative) and freewheel. The conduction period begins with voltage being applied ahead of the BEMF zero crossing point to allow the phase current to ramp up quickly. This 'advance' period is one of the methods used to control the motor power, and can be explained through use of the basic motor phase (3.2) and input power (3.3) equations.

$$V_{phase} = \quad L\frac{\delta i}{\delta t} + E + iR \tag{3.2}$$

$$P_{input} = \quad Ei\cos\theta \tag{3.3}$$

By rearranging equation 3.2 it can be seen that positive phase voltage, V_{phase} and negative BEMF, E, will result in a greater $\frac{\delta i}{\delta t}$ given a fixed inductance, L, and negligible iR losses. This initial rapid rise produces a larger RMS phase current, and therefore a greater input power, P_{input}. A compromise exists however, as advance can also increase the displacement, θ, between the BEMF and phase current which reduces the net power produced.

During the conduction period the applied phase voltage stays constant but the BEMF rises, causing $\frac{\delta i}{\delta t}$ to decrease over time as shown in Figure 3.2(a). After this, the motor enters the freewheeling period where the the two lowside MOSFETs conduct (Figure 3.2(b)), causing the phase current to ramp down rapidly. During this period the inverter input current, $\mathrm{I_{inverter}}$, remains at zero. By referring back to Equation 3.2, it can be seen that when $V_{phase} = 0$ and the BEMF is positive, $\frac{\delta i}{\delta t}$ becomes negative. The combination of the conduction and freewheeling states gives rise to a phase current which is reasonably sinusoidal and in phase with the BEMF, a critical factor in achieving high power and efficiency.

A complete electrical cycle of the motor consists of the following periods: positive conduction - freewheel - negative conduction - freewheel. Owing to its two-pole design, this is also one mechanical cycle, giving the lowest possible electrical frequency for a given operating speed. The benefit of this is reduced iron loss in the motor and reduced switching loss in the drive, as well as limiting the computational demand on the microcontroller.

3.2 200W BLDC Motor Drive Simulation

The first step in developing the system simulation was to design an equivalent-circuit model of the 200W BLDC motor drive which would later be used as the power supply load. This was a relatively straightforward process as all the parameters could be taken from the existing design work for the motor. The top level circuit model can be seen in Figure 3.3 with the relevant parameters shown in Table 3.1.

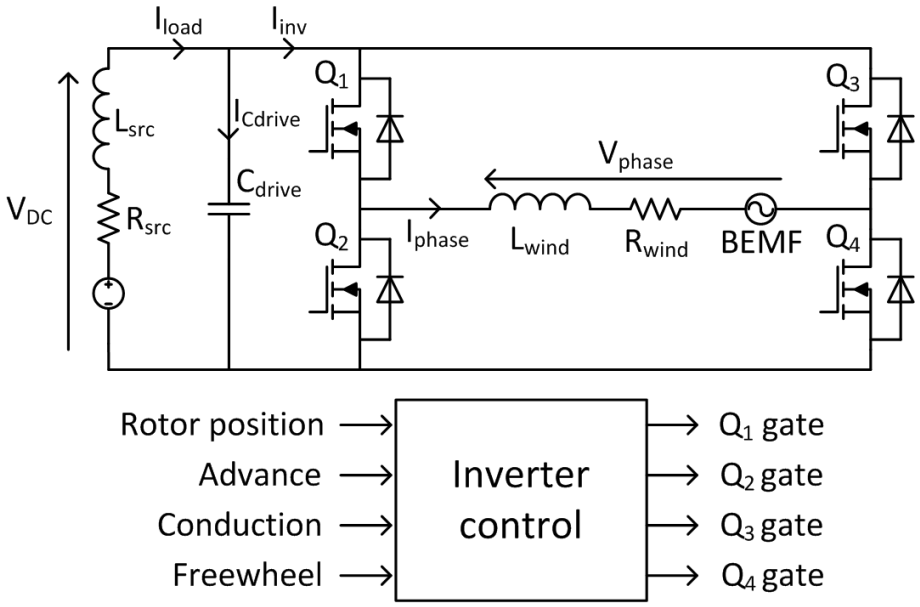

Figure 3.3: Simulation model of the 200W BLDC motor drive

Parameter	Value
V_{DC}	23V
C_{drive}	2000µF
L_{wind}	75µH
R_{wind}	24.6mΩ
R_{src}	40mΩ
L_{src}	1.5µH
BEMF	$17.15V_{pk-pk}$
Speed	90,600RPM
Advance	8.6°
Conduction	91°
Freewheel	89°
MOSFETs	IRFH7932

Table 3.1: Parameters for the 200W BLDC motor drive model

The SaberRD power electronics simulation package was chosen to carry out all of the simulation work in this thesis. One of the key reasons behind this choice was the fact that SaberRD includes powerful control system functions along with detailed component-level modelling. The combination of these two features gives an advantage over many other SPICE-based circuit simulators which tend to focus solely on the electrical domain.

The model simulates the motor drive running in a steady state condition with the supply voltage and motor speed set at the nominal operating point. The advance, conduction and freewheel angles required to support this operating condition are derived from real motor measurements. These angles are fed to a logic control block along with the rotor position, generating the appropriate MOSFET gating signals at the output. The equivalent-circuit model of the motor was based on the motor phase voltage equation (see Equation 3.4), allowing the phase current to be determined from the BEMF, phase voltage, winding resistance and winding inductance.

$$V_{phase} = \quad L\frac{\delta i}{\delta t} + E + iR \tag{3.4}$$

The simulation as a whole was designed to be as simple as possible whilst producing the correct electrical behaviour, most significantly the current draw (I_{load}) as this represents the power supply load. By taking a 'system level' approach to the simulation, it was possible to quickly produce accurate first-order behaviour which matched that of the real motor drive. However, it was necessary to go beyond this with regards to the inverter MOSFET models, as their non-ideal behaviour had an impact on the fundamental operation of the motor drive. Shown in Table 3.2 are the additional parameters used to form the IRFH7932 MOSFET models. Note that the device performance is based on a gate-source voltage of 4.5V and a gate resistance of 1.8Ω.

Parameter (MOSFET)	Value
$R_{DS(on)}$	3.3mΩ
Turn-on time	48ns
Turn-off time	20ns
Output capacitance	830pF
Parameter (Body diode)	**Value**
Forward voltage	1V
Reverse recovery time	32ns
Reverse recovery charge	50nC

Table 3.2: Parameters used in the IRFH7932 MOSFET model

In order to further improve the correlation between the simulated and real behaviour of the motor drive, it was also necessary to model the power source impedance. As mentioned previously, the standard motor drive is supplied by a lithium-ion battery pack. However, in order to provide a consistent, controllable supply with over-current protection, it was necessary to use a laboratory DC power supply for the practical motor drive tests. The resistance, R_{src}, and inductance, L_{src} of the power supply output and associated cabling were therefore included as part of the simulation model.

The key simulated motor drive waveforms are shown in Figure 3.4 along with their respective hardware measurements for validation. Whilst it is clear that the two sets of results are closely correlated, there are a few finer observations worthy of discussion. Firstly, it can be seen in Figure 3.4 (a) that the magnitude of the applied phase voltage decreases slightly over the conduction period. This happens because the DC power supply has a non-zero impedance, and therefore does not form a perfect voltage source for the inverter. As current is applied to the phase windings, the DC link capacitor discharges, causing the DC link voltage to fall. During the freewheeling period, the capacitor continues to recharge until its voltage is equal to that of the supply.

The second point to note is that a fixed value was used for the simulated phase inductance, whereas in reality it varies with current and rotor position. Modelling this effect would require a two-dimensional matrix of values with the position coordinates determined from the BEMF. Due to the complexity of implementing this in a circuit simulation package, a single mean value was taken from the flux-linkage vs. current characteristic for the motor. Figure 3.4 (b) shows the simulated peak phase current to be slightly higher than in reality, suggesting that the average phase inductance value used was too small. However, due to the very close correlation achieved overall, it was deemed unnecessary to use a more detailed inductance model.

It was not possible to measure the BEMF whilst the motor was operating, as the application of phase voltage by the inverter prevents it from being externally visible. The simplest option was to perform a 'run-down' test, which involves running the motor at the nominal speed, switching off the inverter, and then immediately measuring the BEMF. This means that the waveform in Figure 3.4 (c) had to be measured separately from the three other waveforms. However, as the measurement

was made in the first electrical cycle following the inverter shut-down, the change in frequency and amplitude of the BEMF was negligible.

The final and most important observation to make is the highly dynamic nature of the load current (Figure 3.4 (d)). Whilst the DC link capacitors provide a certain amount of decoupling between the power supply and inverter, a very large ripple current still exists. This waveform is particularly significant, as it defines the load which is presented to the AC to DC converter, DC to DC converter and APFC systems discussed over the next four chapters.

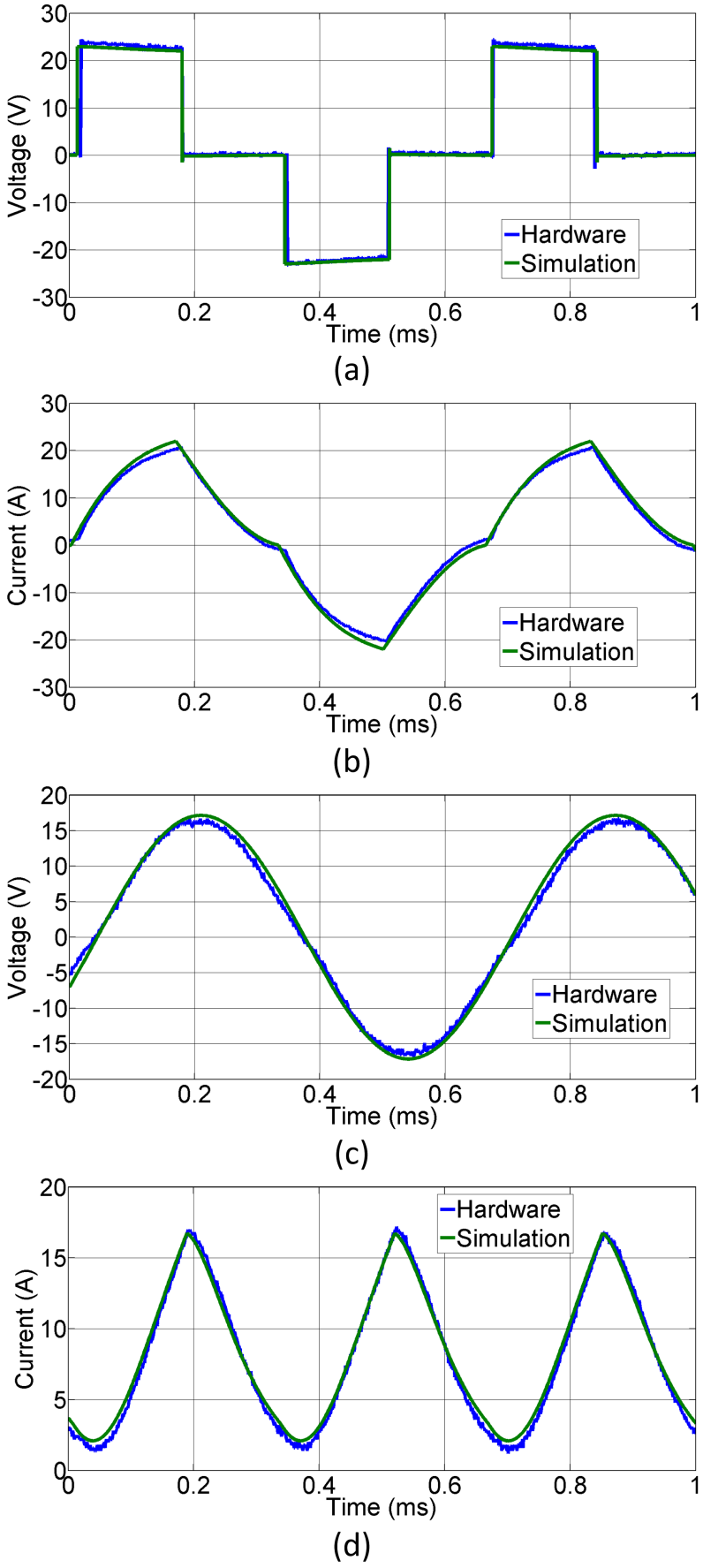

Figure 3.4: Key operating waveforms of the standard 200W BLDC motor (a) phase voltage (b) phase current (c) back EMF (d) load current

3.3 Power Converter Design

As outlined in the introduction, the aim of this research is to study the effect of using minimal DC link capacitance in an offline power system. The 24V BLDC motor drive characterised in the previous section could clearly not be powered directly from the mains. It was therefore necessary to research and then develop a power converter which would allow the low voltage DC system to operate from a 230V AC supply. This section provides a summary of the key considerations made when designing this system.

3.3.1 Transformer Isolation

One of the most basic design choices for an offline Switched Mode Power Supply (SMPS) is whether to use an isolated or non-isolated approach. For voltage step-down conversion, the most basic solution is to use a line frequency transformer, rectifier and DC link capacitor. Such a system is reliable, efficient and easy to design, but is very large and expensive due to the quantities of iron and copper required to make the transformer. The reason for its size and subsequent cost lies in the very low frequency at which the transformer operates (50/60Hz). Equation 3.5 [72], derived from Faraday's law of induction, demonstrates the relationship between transformer size and operating frequency.

$$A_C = \frac{\sqrt{2}E_{RMS}}{2\pi N f B_{sat}}^{1} \tag{3.5}$$

It can be seen that the cross sectional area of the core, A_C, is inversely proportional to the operating frequency, f, of the transformer. The parameters N (number of turns) and E_{RMS} (RMS voltage across windings) are largely fixed by the application, whilst B_{sat} (core saturation flux density) is an intrinsic property of the core material. Even the most advanced electrical steels will begin to saturate around two Tesla, making core saturation very much a limiting factor. Frequency, therefore, is the only variable which can be used to widely control the transformer size. It is for this reason that, since the availability of appropriate switching devices, power supplies have moved to ever higher operating frequencies to increase power density.

[1] valid only when E is sinusoidal

Non-isolated Converters

Given that a line frequency power converter is impractically large and expensive, the next most basic option is to use a non-isolated buck converter, which has no transformer at all. It should be noted that in order to do this, the AC supply must first be rectified as a buck converter is DC to DC only. This is in contrast to a transformer, which is AC to AC only, and must therefore be rectified after the voltage step-down has taken place. The key components of a buck converter are shown in Figure 3.5.

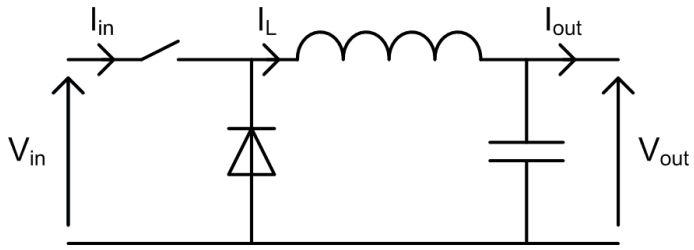

Figure 3.5: Basic buck converter

Through modulation of the switching device duty ratio, D, the converter's output voltage can be regulated such that:

$$V_{out} = \quad V_{in}D \tag{3.6}$$

Equation 3.6 makes it clear that the control system can be very basic, using the output voltage error to alter D appropriately. Furthermore, the converter hardware is made up of only four key components and so the system as a whole can be very simple. In applications such as the conversion of 12V to 5V on a computer motherboard, a buck converter is ideal; in others it can be completely impractical. A key limitation is the range of achievable output voltages due to problems encountered when a very low duty ratio is used. As can be seen from Figure 3.5 the switching device carries the full load current, which will be many times the average input current when a large voltage step-down is required. Furthermore, at low duty ratios the peak switching device current has to be very large in order to maintain the required RMS current, as shown in Figure 3.6. The peak to average ratio of any waveform can be referred to as the 'crest factor', and is an important consideration in the design of power supplies.

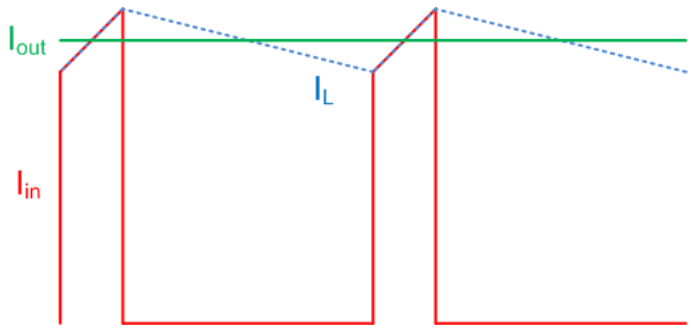

Figure 3.6: Buck converter current waveforms

A high crest factor places a large amount of stress on all the components, not least the power devices which risk being pushed outside of their Safe Operating Area (SOA). Given a fixed operating frequency and gate drive performance, the power device switching losses are mainly determined by the converter input voltage and output current [73], and so it is clear that large voltage conversion ratios are not desirable. As the ultimate aim is to produce a highly compact power supply, efficiency is critical as there is little value in producing a low parts-count converter that requires a very large heatsink. Control problems can also result from using a small duty ratio, as there is a minimal operating range available. If 10% duty cycle is required for nominal output at full load, it may not be possible to reduce it far enough to provide the correct output under light load conditions. Furthermore, short pulses also mean that measurements made for current regulation may be extremely noisy, resulting in unstable control of the switching device.

This problem can be largely avoided through the use of cascaded converters, as discussed in [74] and [75]. The concept is very straightforward; use two converter stages in series and subsequently the individual voltage conversion requirement is halved. As demonstrated by Huber and Jovanović [74], this can allow conversion ratios of 10:1 whilst maintaining high (+90%) efficiency. This is possible as the voltage across each power device also halved, allowing the use of Schottky diodes and low $R_{DS(on)}$ MOSFETs. A high overall efficiency can therefore be maintained even though the energy flowing through the converter is processed twice. The use of such a technique is particularly attractive as it too avoids the use of a transformer, helping to keep the size, cost and complexity of the converter down.

Even through the use of cascaded power stages, there are a number of significant drawbacks to non-isolated converters. The first stems from the ground connection shared by the input and output. Where large voltage conversion ratios exist, an equally large current conversion takes place, meaning that the ground rail sees a significant change in the current flowing along its length. Due to the non-zero impedance of the ground rail, a differential voltage will be produced between different points of the circuit, subsequently providing different reference voltages for the various stages of the converter [73]. A very careful Printed Circuit Board (PCB) layout is required to mitigate this problem.

Due to the position of the switching device in a buck converter, a floating gate drive circuit is required. Level shifting circuits tend to limit the maximum operating frequency due to high power dissipation and bootstrap capacitor charging [76], whereas gate drive transformers limit the duty cycle due to the required core reset time. Neither of these are ideal, but due to the low nominal duty of the intended application, a transformer isolated design is preferable. The switching device location also causes problems with current measurement, as a sense resistor placed in series with the power device will have a small differential signal voltage superimposed on top of a large common mode voltage, requiring the use of a high quality differential amplifier. The alternative is to use a current sense transformer, but this too suffers from duty cycle limits and is also costly [73].

A further issue caused by the switching device position is that of discontinuous input current, a problem which is exacerbated by low duty cycle operation. As can be seen in Figure 3.6, the input current is a sequence of trapezoidal waveforms and will therefore have a high harmonic content. In most situations this would not be a problem, but in the case of a mains connected converter a large amount of input filtering would be required to keep harmonics under control, and as such the design does not lend itself to applications requiring a high power factor.

The final, and possibly most serious issue is that of safety. If the power devices fail short circuit, or a control error generates 100% duty cycle, the converter output will be directly connected to the input. If the output terminal is user-accessible, such as on a laptop power supply, a serious risk of electric shock exists. Even where this is not the case, it is likely that there will be serious damage to the connected product. In a transformer isolated design power device failure will simply result in

saturation of the transformer, accompanied by a drop in output voltage. In the case of excessive duty cycle, the maximum output voltage is limited by the transformer turns ratio, and is unlikely to be dangerous. Finally, by galvanically isolating the output, a potential earth path is removed, further reducing the risk of shock.

3.3.2 Transformer Design and Topology Selection

Virtually all the shortcomings of non-isolated designs can be overcome through the use of a transformer, with the notable exception of size. For such a converter to be viable, every benefit of transformer isolation must be fully utilized, in order that savings can be made from other areas to offset the size and cost of the additional component. In a typical offline supply the isolation transformer occupies 25% of the volume and 30% of the weight, making it the largest individual component in many cases [77]. Shown in Figure 3.7 is a single switch forward converter, the most basic isolated variant of a buck converter.

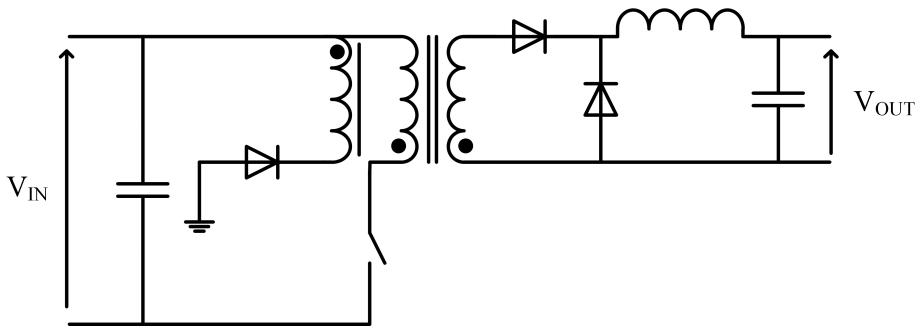

Figure 3.7: Single switch forward converter

$$V_{out} = \frac{N_2}{N_1} V_{in} D \tag{3.7}$$

Control of a forward converter is essentially the same as that of a buck converter, with the added benefit of a transformer to provide voltage conversion (see Equation 3.7). As the turns ratio can be freely chosen, the power device duty can be optimally selected. A larger duty cycle reduces input capacitor stress and improves the noise immunity of current/voltage sensing [73]. Furthermore, switching losses can be made comparatively small as the power device does not have to handle the input

voltage *and* output current. Losses in the rectifier are also reduced as the secondary side voltage is much smaller. This increased efficiency can allow for reduced cooling requirements and therefore a smaller heatsink. As the switching device is ground referenced, gate drive and current sensing circuits can also be simplified.

A complication arising from transformer-based designs is the need for control signals to cross the isolation barrier. For output voltage regulation, secondary side voltage sensing is required, but this information needs to be fed to the control system driving the power device on the primary side. There are two common methods by which this can be achieved; opto or transformer coupling. Opto-couplers are typically small, low cost devices but exhibit a non-linear signal transfer ratio with respect to frequency, temperature and age. Furthermore, they are highly susceptible to noise and variable manufacturing tolerances [78]. Despite these drawbacks, in applications with relaxed voltage regulation requirements, the low cost and simplicity of opto-coupling can make it an appropriate choice. As proposed by Balogh *et al.* [73], in particularly low performance applications it is possible to approximate the secondary voltage by sensing the primary voltage via an auxiliary transformer winding, thus avoiding crossing the isolation barrier altogether.

Core Excitation

Isolation transformers can be split into two categories depending on the method of core excitation:

- unidirectional - forward and flyback converters
- bidirectional - push-pull, half-bridge and full-bridge converters

As the name suggests, unidirectional excitation involves passing time varying DC current through the transformer windings, and thus producing only a positive flux density. This is also referred to as single quadrant operation, which can be seen in the example transformer B-H loop in Figure 3.8. For bidirectional excitation, square-wave AC current is fed into the transformer windings, inducing both positive and negative flux, and is therefore referred to as two quadrant operation.

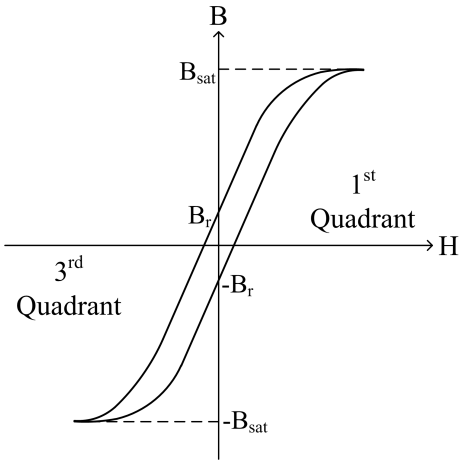

Figure 3.8: Hysteresis loop for a generic soft magnetic material

By referring back to Equation 3.5, it can be seen that the transformer core area, A_C, is dependent on the saturation flux density, B_{sat}. This assumes full sinusoidal excitation of the core, which is not valid in this case, and so a restatement of the formula is necessary [79] (see Equation 3.8).

$$A_C = \frac{V_{DC}}{4N_1 f_{sw}(\Delta\hat{B})_{max}}{}^{1} \tag{3.8}$$

In this case the converter DC input voltage, V_{DC}, is exerted on the primary winding, N_1, and the saturation flux density component has been substituted with the peak flux density variation term, $(\Delta\hat{B})_{max}$.

For unidirectional excitation:

$$(\Delta\hat{B})_{max} \leq 0.5(B_{sat} - B_r) \tag{3.9}$$

For bidirectional excitation:

$$(\Delta\hat{B})_{max} \leq B_{sat} \tag{3.10}$$

It is clear from Equations 3.9 and 3.10 that bidirectional excitation allows for a significantly reduced core size, and so effectively makes more efficient use of the

[1] valid for square-wave V_{DC}

available core material. This is one of the key advantages of a bidirectional converter topology in terms of increasing power density, but the increased component count and control complexity must be accounted for. A further consideration is that when operating in excess of 100kHz, $(\Delta\hat{B})_{max}$ is normally reduced below B_{sat} to prevent excessive core loss [79].

In single quadrant operation, some means of resetting the transformer core must be present, providing a freewheeling path for the magnetisation current. This is the purpose of the tertiary winding shown on the forward converter in Figure 3.7, which allows the current to flow into the input capacitor, thus recovering the energy. The tertiary winding is usually wound 1:1 with the primary, often in a bifilar fashion to provide good coupling (i.e. minimal leakage) [80]. In this case the duty cycle is limited to 50% to allow for complete resetting of the core.

The flyback transformer is a special case as it is in fact a coupled inductor, which differs from a transformer in that it intentionally stores energy. A significant air-gap is introduced into the core to allow for energy storage, with the added benefits of forcing the residual flux density, B_r, virtually to zero and linearising the B-H characteristic. To a much smaller extent this is also done with forward converter transformers to improve $(\Delta\hat{B})_{max}$ (see Equation 3.9). Power only flows from the primary to the secondary of the flyback transformer at the point of transition, i.e. when the power device turns off and current stops flowing in the primary winding. The inductively stored energy causes current to flow in the secondary, demagnetising the core in the process, thus removing the need for a reset winding (see Figure 3.10).

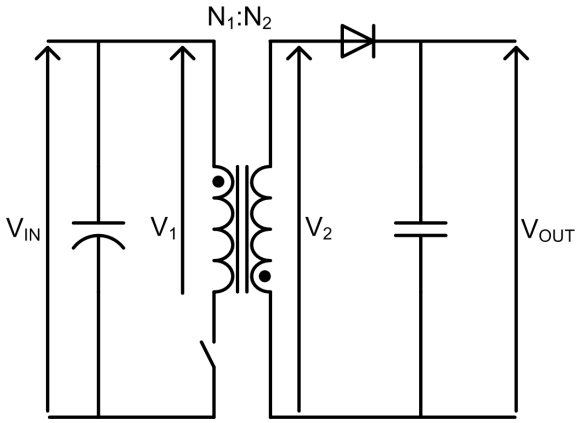

Figure 3.9: Basic flyback converter

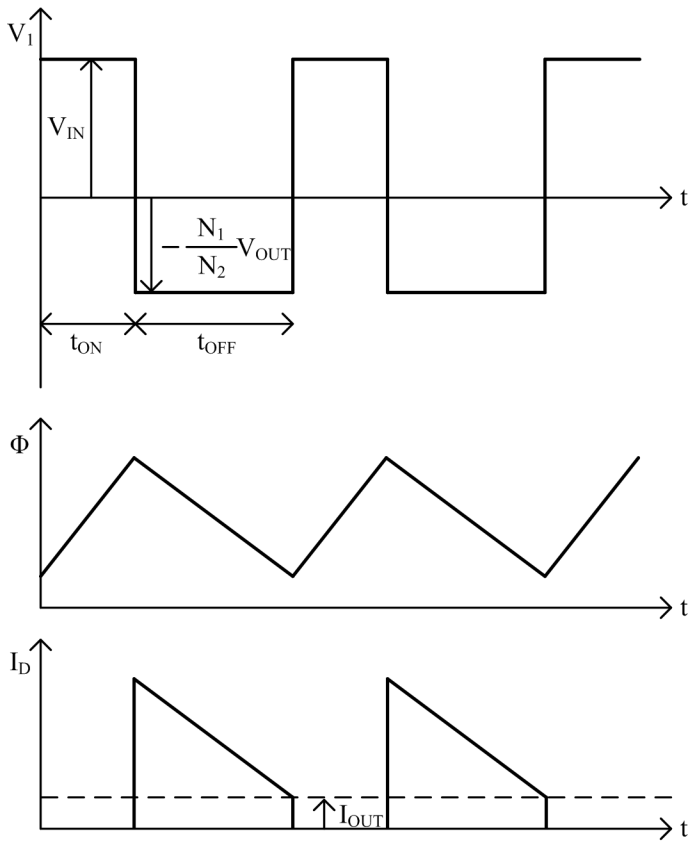

Figure 3.10: Basic flyback converter waveforms

As a core reset mechanism is not required in two quadrant operation, it is possible for the effective duty cycle to reach almost 100%, making the secondary voltage almost constant DC. As proposed by Balough *et al.* [73], this can allow the output filter to be minimised or even omitted in some cases, giving considerable size and cost savings. Furthermore, the very high duty cycle can allow the switching devices to operate in a quasi-resonant fashion through the use of parasitic components, subsequently reducing turn-on losses significantly.

Geometries

Transformer cores are available in a wide range of configurations to suit different applications. In the case of high power density converters, the three most significant designs will be briefly discussed here. The most commonly used core is known as an EE core as a consequence of its construction from two back-to-back 'E' shaped sections. The core shape allows the windings to be formed around a bobbin which makes manufacturing simpler, and also allows the winding ends to enter/leave the core easily due to the open sides. This is beneficial where multiple output voltages

are desired, but also increases EMI due to the limited shielding. An air gap can be accommodated by shortening the centre leg without incurring significant fringing effects.

Toroidal cores benefit from a high power density (in terms of both size and weight) and minimal EMI. The toroid shape constrains the flux to the core material very effectively, virtually eliminating stray fields. As is the case with all winding designs, if the cross section of the core is round rather than square, the windings will be 11% shorter for the same given core area, reducing the resistance and therefore losses. As toroidal cores must be wound directly, rather than using a bobbin, they tend to be more expensive to manufacture due to the slower and more complex winding machinery required [72]. The entire surface area of a toroidal transformer can be open to the air, making cooling more efficient than other approaches which are at least partly enclosed.

The third and potentially most interesting design is the planar transformer. The core is made from two thin pieces of soft magnetic material which sit either side of PCB containing tracks which act as windings. The minimum PCB track width limits the number of turns, making planar transformers suitable for modest turns ratios only (up to approximately 10:1). The large exposed surface area of the core provides excellent thermal characteristics [81]. The result is a very low profile, high power density, low cost transformer which is ideally suited to mass manufacture. For lower volume production the devices can be bought as individual components in a wide range of power ratings.

3.4 Power Supply Simulation

The second step in the simulation design was to develop a power supply model suitable for running the 200W BLDC motor from a mains source. The design was focused around the reduced DC link capacitance concept, thus requiring the motor drive to operate from a supply with 100% DC link voltage ripple. This meant that the power supply needed only to reduce the rectified mains voltage to a level compatible with the existing $24V_{DC}$ design. The target output voltage was therefore a rectified sine wave with a mean value of 24V in order to maintain the same load power. This can be seen in Figure 3.11.

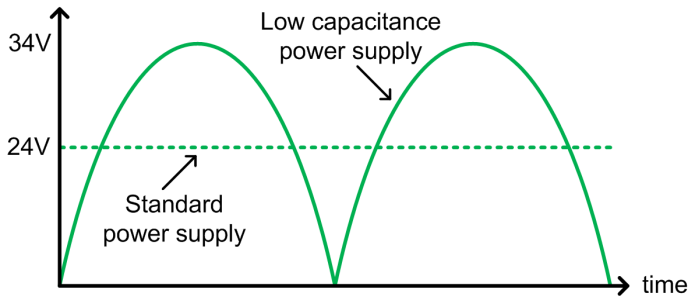

Figure 3.11: Target output voltage of the reduced DC link capacitance power supply

The simplest way to generate such a voltage would be through the use of a line frequency transformer and diode bridge. Whilst also being efficient and reliable, this approach would be impractical due to the very large and expensive transformer, negating any power density gains made through a reduction in DC link capacitance. Instead, a switch-mode based converter was required which could produce the same output from a much smaller package, at a much lower cost.

In terms of power supply design, an isolated approach was needed on the grounds of safety, control flexibility and input current quality. In order to minimise the transformer size, two quadrant excitation was needed, ruling out the use of topologies such as flyback or forward. A half bridge arrangement could have been used, but the increased DC link capacitance requirement coupled with greater switching device currents meant that a full bridge was more suitable. The higher power handling of a full bridge converter made it more robust for development purposes and easily scalable for larger loads. In terms of transformer topology, a planar design was ideal due to its high power density, low profile and low losses. A circuit diagram for the top level model is shown in Figure 3.12.

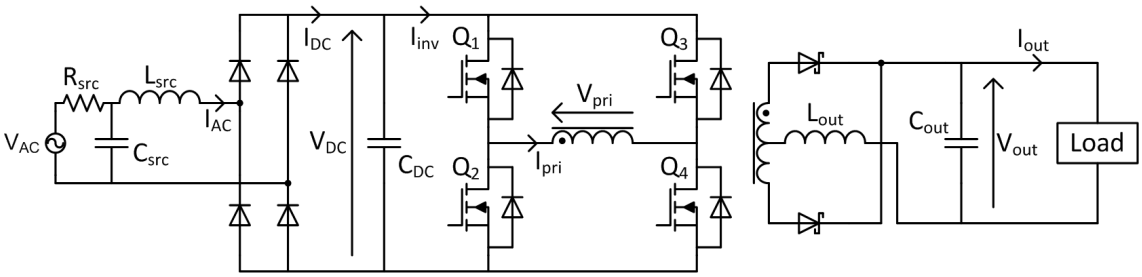

Figure 3.12: Simulation model of the reduced DC link capacitance power supply

Given that the output voltage could contain 100% ripple, tight regulation was unnecessary and so the power supply was designed to operate in an open loop manner. The only constraints were to limit the peak secondary voltage to 35V to prevent damage to the motor drive, and to keep the mean voltage between 16.8V and 24V. As discussed in Section 3.1 the motor drive control system has the ability to produce constant output power across this supply range. The benefit of such an approach is a reduction in components and control complexity, helping to reduce the size and cost of the converter.

From the outset, the simulation model was developed using the parameters of real components chosen to provide good performance whilst remaining low cost. This approach was taken throughout the project, as the use of specialist or exotic parts would not be suitable for mass manufacture of a consumer electronic product. Furthermore, it was critical for the simulation to account for parasitic effects such as transformer leakage inductance or diode reverse recovery, so the use of idealised component models would not have been suitable. Due to the very high frequencies involved, such effects have a significant impact on the power supply operation, particularly in a reduced capacitance system where there is minimal decoupling between components.

Shown in Table 3.3 are the key parameters for the power supply simulation model. The source impedance components (R_{src}, L_{src} and C_{src}) serve to model the output stage of the linear AC source used whilst testing the power supply hardware. Again, due to the reduced capacitance nature of the power supply, the source impedance has a considerable effect on the system performance, most significantly the input current harmonics. It was therefore necessary for the simulation to account for this in order to produce results consistent with hardware measurements.

Parameter	Value
V_{AC}	$230V_{RMS}$
C_{DC}	1µF
Transformer	SX55 planar
Turns ratio	12:1:1
C_{out}	5µF
L_{out}	30nH
L_{leak}	180nH
R_{src}	400mΩ
L_{src}	5µH
C_{src}	100nF
f_{switch}	500kHz
Duty cycle	75%
MOSFETs	IPP65R420
Schottkys	STPS20L60

Table 3.3: Parameters for the power supply model

As with the motor drive model discussed in Section 3.2, it was necessary to model the non-ideal behaviour of the inverter MOSFETs in order to produce accurate simulation results, in particular the system efficiency. The Schottky rectifier diodes also had a significant impact on this, however their lack of reverse recovery meant it was only necessary to account for the 0.56V forward voltage in the model. Shown in Table 3.4 are the additional parameters used in the IPP65R420 inverter MOSFET models. Note that the device performance is based on a gate-source voltage of 13V and a gate resistance of 3.4Ω.

Parameter (MOSFET)	Value
$R_{DS(on)}$	42mΩ
Turn-on time	7ns
Turn-off time	8ns
Output capacitance	45pF
Parameter (Body diode)	**Value**
Forward voltage	0.9V
Reverse recovery time	90ns
Reverse recovery charge	300nC

Table 3.4: Parameters used in the IPP65R420 MOSFET model

The transformer model is based on a Standex SX55 planar design rated for 350W at 500kHz when bipolar excitation is used. Both the primary and secondary leakage inductances are modelled, with the secondary forming part of the output filter to save on an additional component. The 5µF output capacitor is modelled as a low ESR polypropylene film device capable of handling the high ripple current resulting from such a small filter inductance. Together the two components form a 411kHz low pass filter suitable for smoothing the rectified 1MHz output voltage/current ripple. The 1µF DC link capacitor is similarly a low ESR polypropylene film device as it also has to handle a high ripple current across a range of frequencies (100Hz recitifed mains, 3.3kHz motor load frequency and 50-200kHz APFC). A further benefit of using a film capacitor is the high dielectric strength, allowing for a higher voltage rating than a typical electrolytic device. In this case a 630V part was used, which along with the 650V rated MOSFETs gave the potential for high DC link voltages without damage. If electrolytics were used it would be necessary to have two balanced series connected devices to produce a sufficient voltage rating, increasing the number of power supply components.

Schottky devices were chosen for the secondary rectifier as these would give the lowest possible loss from an uncontrolled device. The small forward voltage and zero reverse recovery make them suitable for high current, high frequency applications such as this. An efficiency improvement could have been made through use of a synchronous rectifier, but the additional control complexity would make it prohibitively expensive. Self-driven synchronous rectifiers are often used to mitigate this problem, using the transformer secondary voltage to directly drive a pair of FETs. However, it has been noted by Cobos *et al.* [82] that this arrangement suffers from a high sensitivity to input voltage variation as this directly impacts on the MOSFET gate signals. Use of such an arrangement would therefore be almost impossible in a reduced capacitance system.

The full bridge converter is driven in a push-pull fashion as shown in Figure 3.13, the standard method of control for a hard-switched system. Phase shift control could also have been used, but offers no advantage without the addition of resonant components. The use of a soft switching design was considered in order to reduce losses, but was ruled out for a number of reasons. Firstly, modern low cost power devices now have switching times in the order of nanoseconds, allowing hard-switched operation up to approximately 500kHz with reasonable efficiency [79]. Secondly, successfully

implementing a soft switching design is much more difficult in a reduced capacitance system. As noted by Xue *et al.* [28], the very large DC link voltage ripple means that the system cannot always be kept within the necessary operating range for zero voltage or zero current switching. As this is only possible for a portion of the mains cycle, the efficiency gains from soft switching are less significant. Finally there was a practical consideration given the limited time available for the project and the fact that its main focus was on the APFC system, not the DC/DC converter design. It was therefore decided that this would form part of the future work for the project.

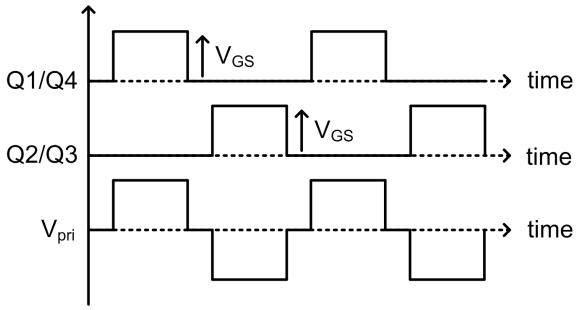

Figure 3.13: Push-pull control waveforms for the full bridge converter

It was deemed unnecessary to develop a full simulation model for the gate driver circuit as its effect on the MOSFET switching performance could be accounted for directly. This was done by combining the relevant parameters from the power device and gate driver IC datasheets, such that transition times, $R_{DS(on)}$, parasitic capacitance and body diode reverse recovery could all be accounted for. For the hardware implementation a high speed, high current gate driver IC was used for each leg of the converter, using a bootstrap supply to produce the necessary gate-source voltage for the high side MOSFET. Due to the high frequencies involved, particular care was taken during the PCB layout of the gate driver circuits in order to minimise stray inductance and maximise switching performance.

3.5 Prototype Hardware

In order to validate the simulation results a hardware implementation of the reduced capacitance power supply was required. This section builds on the basic schematic and component selection outlined in Section 3.4 and explains the salient features of the prototype power supply.

Shown in Figure 3.14 is the PCB based on the simulation schematic in Figure 3.12, with the key components highlighted for clarity. The first point to note is the presence of a boost converter front end. This was added for use in the APFC stage of the project and will be covered in detail in Chapters 5, 6 and 7. All of the results in this chapter were measured with the boost converter components removed. The DC link and output capacitors, MOSFETs, gate drives, Schottky rectifier and transformer are all as described in Section 3.4.

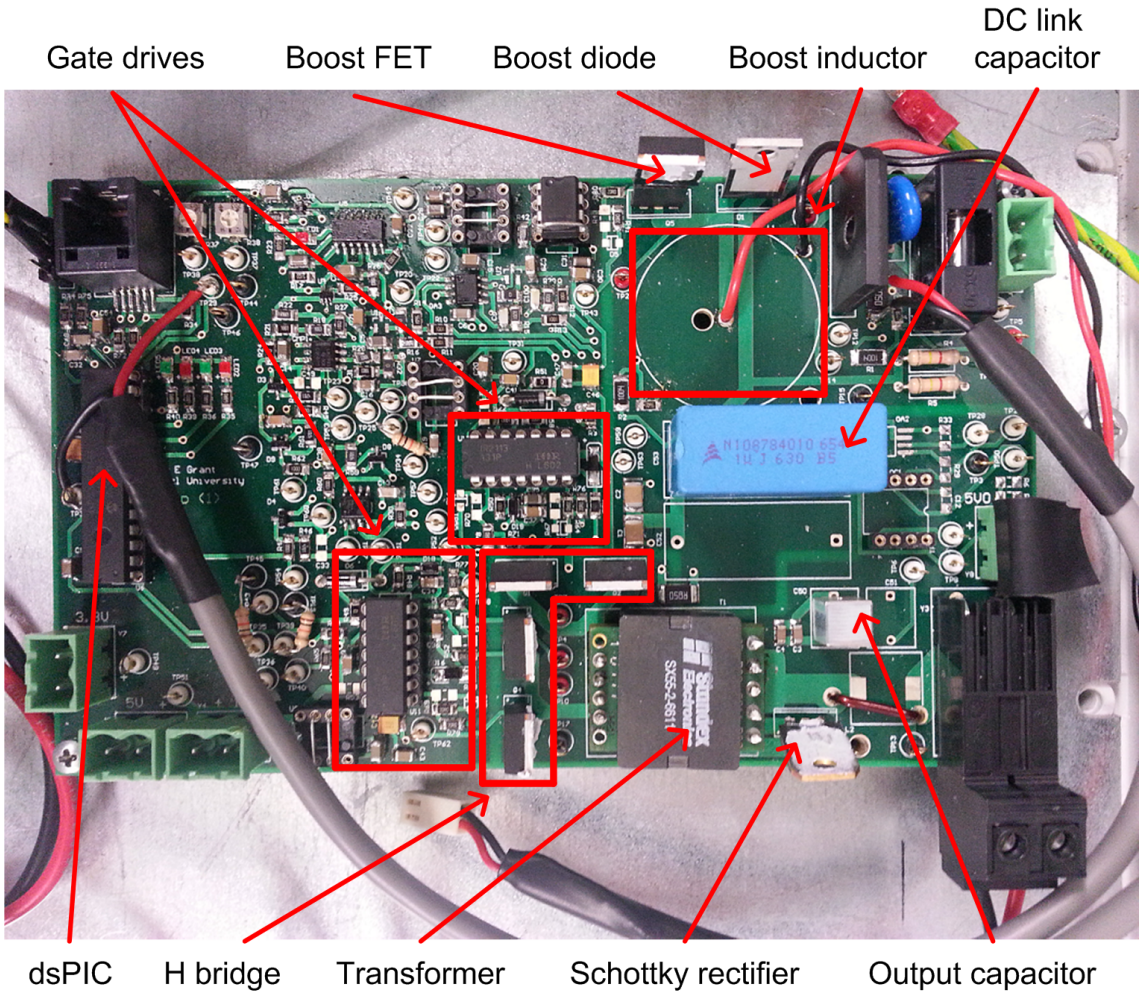

Figure 3.14: Prototype power supply with key subsystems labelled

A dsPIC 33F series microcontroller was used for control of the power supply as well as other diagnostics and protection features. Whilst this was not in keeping with the low cost nature of the design, simple control system changes in software saved a considerable amount of development time. It was always the intention that the final control system developed would be capable of implementation in a low cost manner,

using either an analogue design or a very low cost microcontroller. As the PCB was designed at an early stage in the project, it was necessary to keep the hardware as flexible and robust as possible for development purposes. This is also the reason a number of empty component spaces can be seen; some of the parts were found to be unnecessary at the practical stage.

In order to keep as many control options open as possible, a range of sensors provided feedback to the microcontroller. Shunt based sensors were used to detect the DC-side input current (I_{DC}) and inverter current (I_{inv}), giving wide bandwidth feedback from a compact and low cost circuit design. These sensors were also used as part of the hardware and software overcurrent protection systems which disabled the power device switching on detection of a fault. DC link (V_{DC}) and output voltage (V_{out}) measurements were made using a potential divider to drop the voltage to a level compatible with the microcontroller Analogue to Digital Converter (ADC). The output voltage feedback signal was isolated through the use of an optocoupler. This component was included at the early design stage to make the system as flexible as possible, but owing to the open-loop control system it was never actually used. The DC link voltage sensor signal was also fed into the hardware protection system to prevent damage through over voltage. Schottky diode clamps were fitted in case any sensor signal went outside the ADC input range.

A serial communication interface was added to allow real time data logging for debugging and diagnostics purposes. This was particularly useful for monitoring ADC data before and after processing, making it easier to fine tune the software parameters. The low voltage DC supplies for the control hardware and gate drive circuits were provided by isolated TRACO units for simplicity. Ultimately these would also be replaced with low cost on-board supplies, but this was seen as unnecessary for the purposes of this project.

A final point to note is that due to the boost converter not being used at this stage, the power supply output voltage is lower than the required $24V_{mean}$. The transformer turns ratio was chosen based on a peak DC link voltage of between 400-450V, and so the rectified mains voltage ($330V_{peak}$) results in a lower output voltage. As can be seen in the next chapter, this subsequently causes the motor drive load to operate at a reduced power.

Chapter 4

Test Results and Validation of the Power System Simulation

This chapter contains the results from simulation and practical testing of the reduced DC link capacitance power supply described previously. The behaviour of the system is analysed using three different loads, in order to demonstrate how its performance is affected under different operating conditions. Particularly close attention is paid to the impact the power supply load has on the input current harmonics and power supply efficiency. For the majority of the tests carried out, practical and simulation results are shown together with a close agreement between the two. Where this is not possible, simulation results are provided alone to give an indication of the expected system behaviour.

4.1 Power Supply Testing with a Resistive-Inductive Load

The initial testing phase of the power supply simulation and hardware used an RL load to check the basic functionality of the system. A 1.6Ω wire-wound power resistor was used which had a significant inductance of 10µH due to its construction method. The power supply setup remains unchanged for all the tests carried out in this chapter, using the parameters found in Table 3.3.

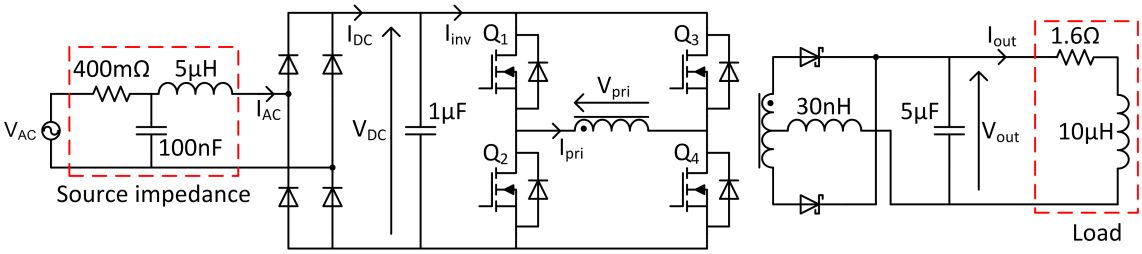

Figure 4.1: Simulation and hardware test setup for the reduced capacitance power supply with an RL load

By observing Figure 4.2, 4.3 and 4.4 it is immediately clear that the very small DC link capacitance causes the power supply output and DC link voltages to follow the rectified mains input. The linear RL load subsequently causes the output and input current to have the same shape, producing a high power factor as seen in Figure 4.5. The power supply does still present a slightly capacitive load to the mains giving rise to the 4% leading phase displacement. This is of little significance however as a power factor of 0.998 is still achieved.

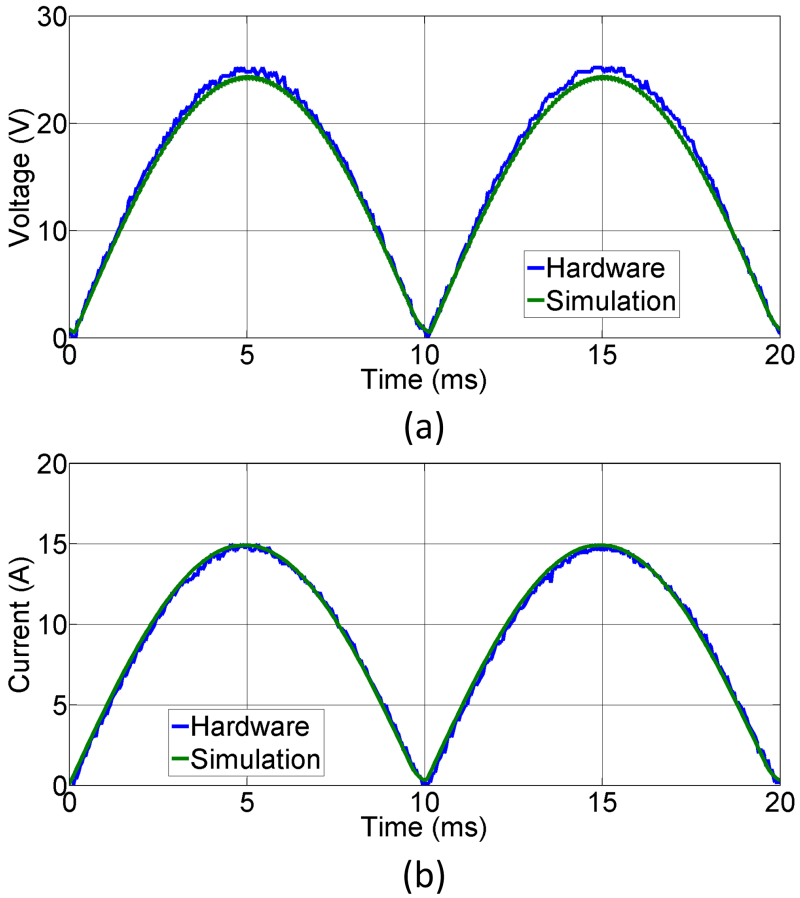

Figure 4.2: Power supply output (a) voltage and (b) current for an RL load

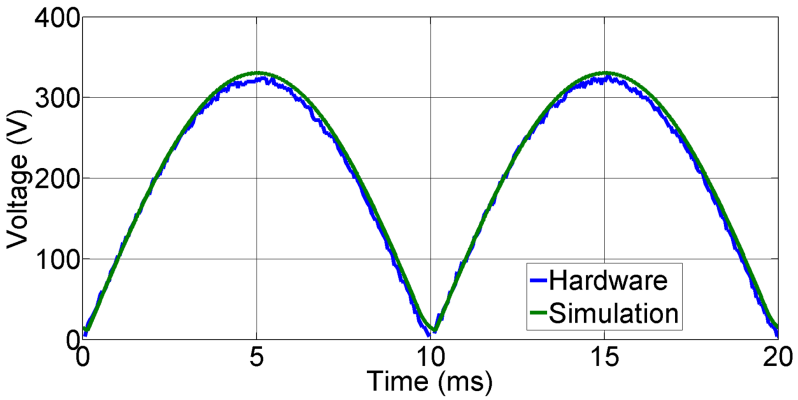

Figure 4.3: Power supply DC link voltage for an RL load

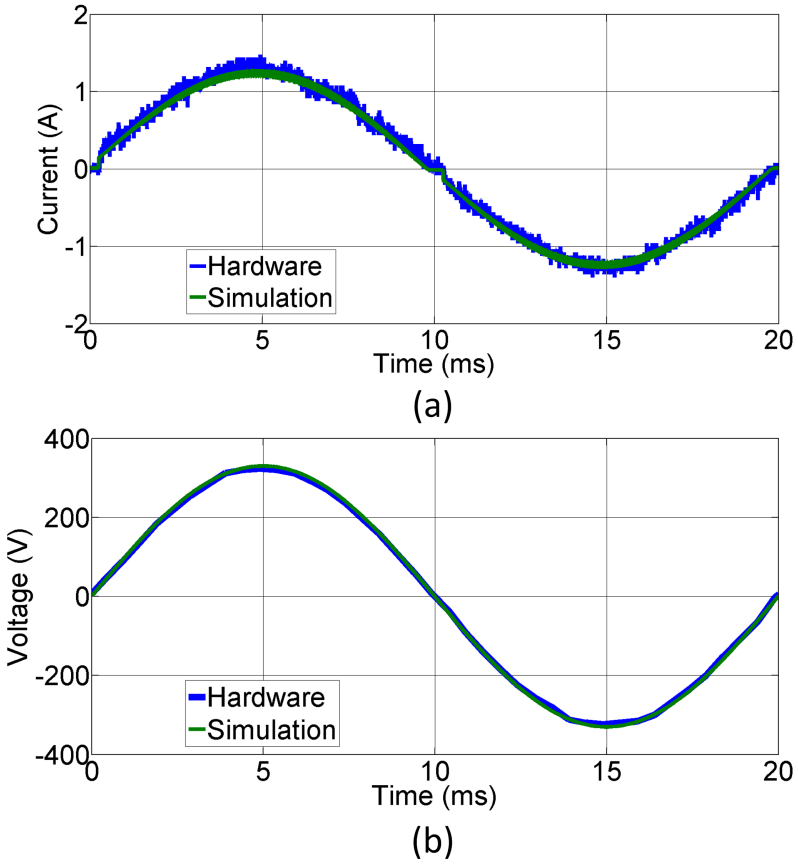

Figure 4.4: Power supply input (a) current and (b) voltage for an RL load

Further results can be seen in Table 4.1 along with the relative error between simulation and hardware measurements. A very close correlation is achieved between all of the waveforms, with a maximum error of 3.5% in the output voltage.

Parameter	Hardware	Simulation	Error
I_{AC}	$0.890A_{RMS}$	$0.880A_{RMS}$	1.1%
V_{AC}	$229V_{RMS}$	$233V_{RMS}$	1.7%
V_{DC}	$204.1V_{mean}$	$210.2V_{mean}$	2.9%
V_{out}	$15.85V_{mean}$	$15.30V_{mean}$	3.5%
I_{out}	$9.27A_{mean}$	$9.40A_{mean}$	1.4%
P_{in}	204W	205W	0.5%
P_{out}	183W	187W	2.1%
Efficiency	89.7%	91.2%	1.6%

Table 4.1: Key measurements for the power supply hardware and simulation with an RL load

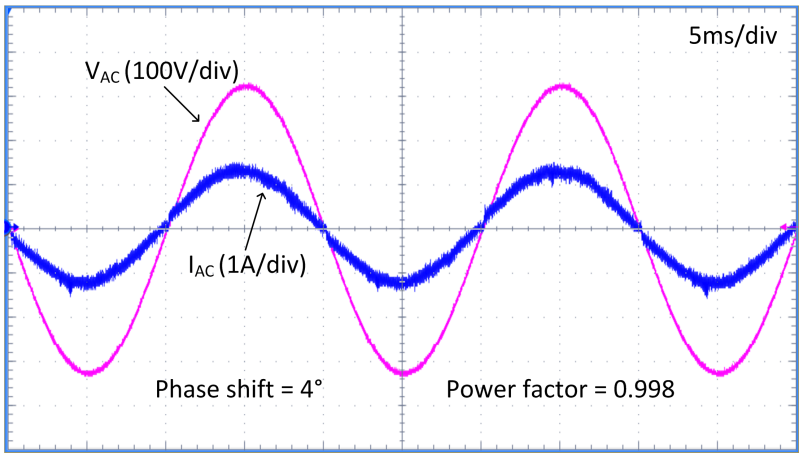

Figure 4.5: Oscilloscope screenshot showing power supply input voltage and current for an RL load

Shown in Figure 4.6 is the transformer primary voltage V_{pri} and current I_{pri}. Due to the construction of the planar transformer it was not possible to directly measure the primary current. As marked on Figure 4.6 (b), the current was instead measured at the source pin of Q4 using a Rogowski coil, meaning that only positive current could be detected.

The most significant observation is the discrepancy between the two primary voltage waveforms during the freewheeling period. During this time the hardware waveform does not match the idealised waveform shown in Figure 3.13. The reason for this is that during the freewheeling period all of the MOSFETs are off, which causes the transformer primary voltage to become undefined once the primary current stops flowing. This could be overcome by forcing zero volts across the primary during the

freewheeling period, but there is no particular advantage to doing this. Rather than switching all the power devices off during the freewheeling period, either the high side (Q1/Q3) or low side (Q2/Q4) MOSFETs would be kept on. The simulation results do not show this issue as the MOSFET models all have identical parameters. The devices therefore switch off in exactly the same amount of time and have the same impedance, creating a net voltage of zero across the transformer primary.

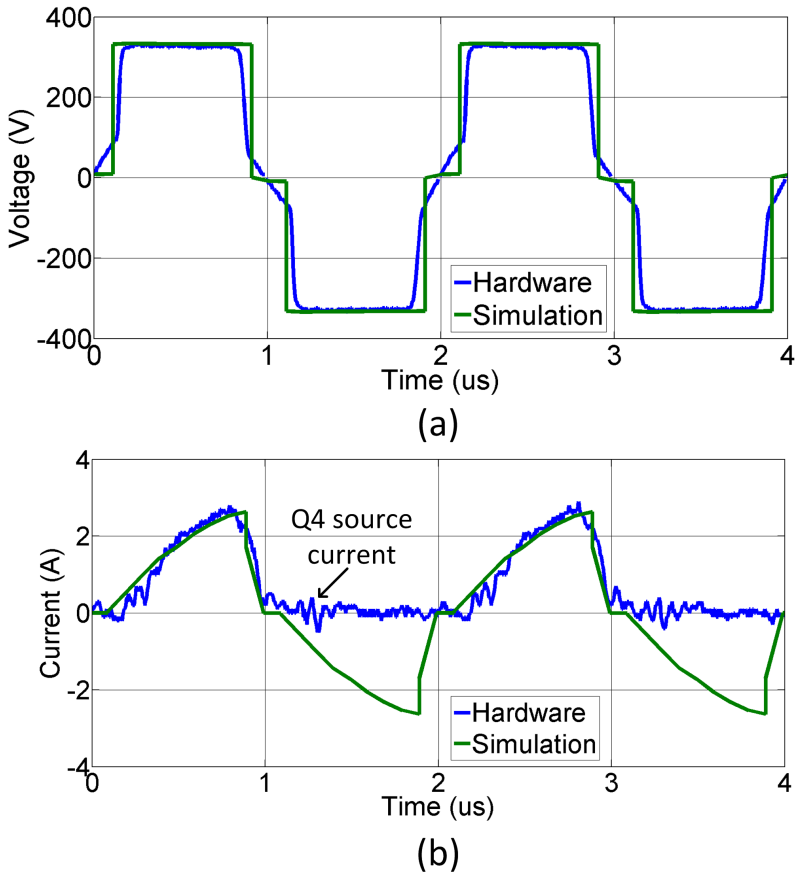

Figure 4.6: Power supply transformer primary (a) voltage and (b) current for an RL load

4.2 Power Supply Testing with a BLDC Motor Drive

The second round of tests on the power supply were carried out using the 200W BLDC motor described in Section 3.1. A diagram of the hardware and simulation setup for this test is shown in Figure 4.7, with the motor drive parameters as per Table 4.2. As previously, the power supply parameters can be found in Table 3.3.

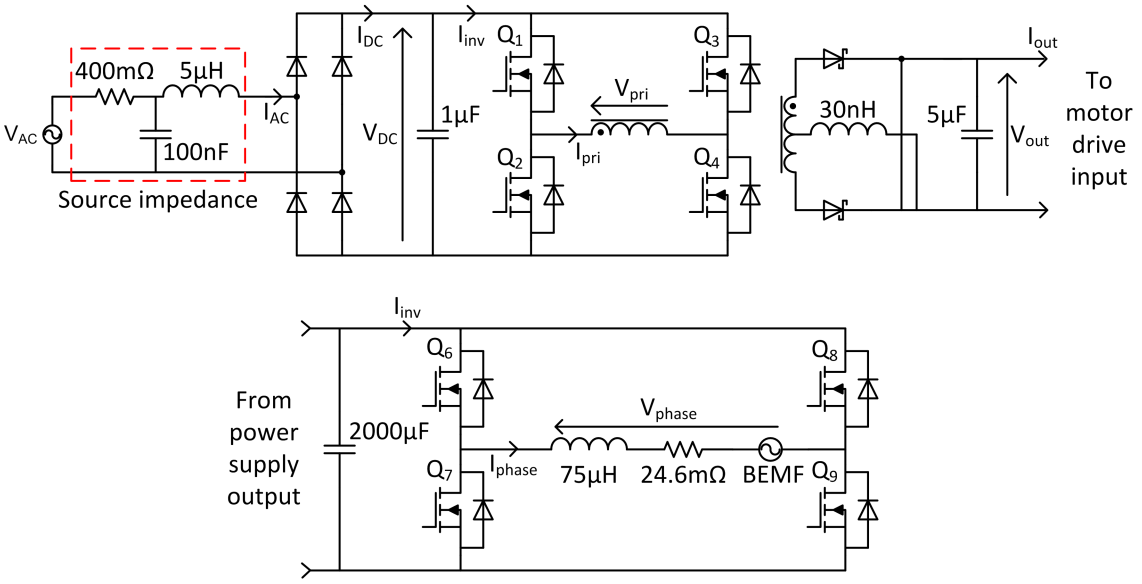

Figure 4.7: Simulation and hardware test setup for the reduced capacitance power supply and 200W BLDC motor drive load

Parameter	Value
V_{out}	$18V_{mean}$
C_{drive}	2000µF
L_{wind}	75µH
R_{wind}	24.6mΩ
BEMF	$17.15V_{pk-pk}$
Speed	94,500RPM
Advance	8.6°
Conduction	53°
Freewheel	127°
MOSFETs	IRFH7932

Table 4.2: Parameters for the 200W BLDC motor drive when running from the reduced capacitance power supply

As the motor drive was designed to operate from a stable $24V_{DC}$ supply two small modifications were required for it to run successfully from the reduced capacitance power supply. Firstly it was necessary to provide a constant 5V supply rail for the control electronics. This was achieved by adding a blocking diode and a capacitor before the existing 5V regulator to smooth the voltage ripple as shown in Figure 4.8. The second modification was a minor change to the drive software which involved

the removal of the under-voltage lockout. This prevented the drive from shutting down when the power supply output voltage fell below 16.8V; an event which would otherwise occur every 10ms.

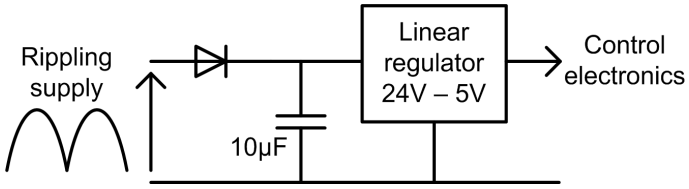

Figure 4.8: Additional smoothing capacitor and diode added to stabilise 5V rail on the motor drive PCB

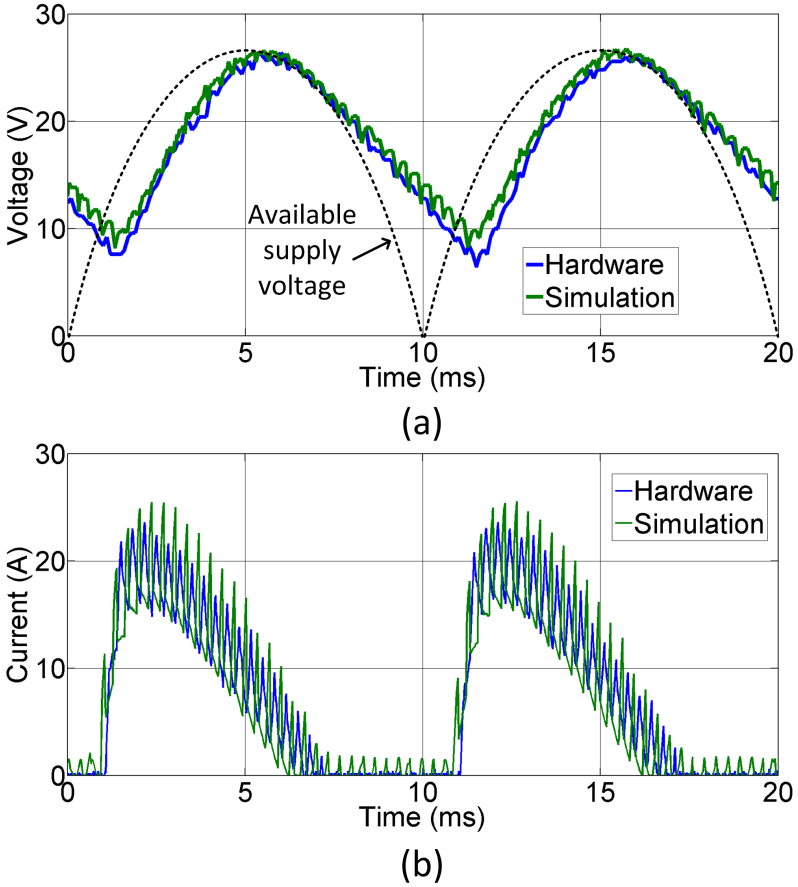

Figure 4.9: Power supply output (a) voltage and (b) current for a 200W BLDC motor load

It is clear from Figure 4.9 that the power supply output voltage does not directly resemble the rectified mains. This is due to the 2000µF capacitance in the motor drive (C_{drive}) acting as part of the output filter and providing a certain amount of

voltage holdup. For a considerable amount of time the power supply output voltage is larger than the available supply voltage, causing the output current to drop to zero during this period. Due to the minimal (high voltage) DC link capacitance, this non-sinusoidal load current shape is directly reflected in the input current shape as shown in Figure 4.11 (b).

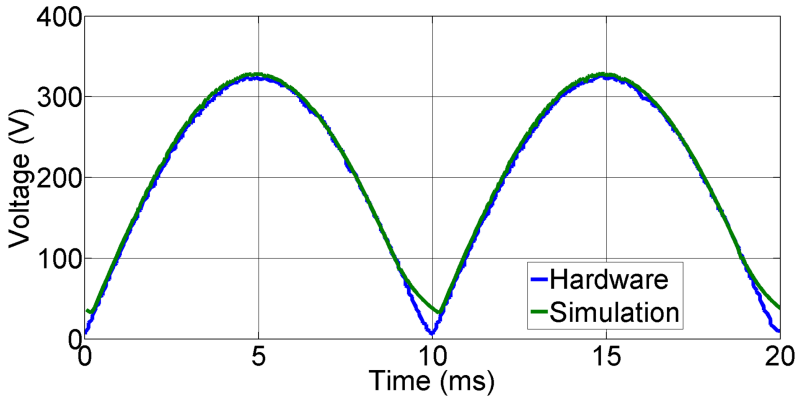

Figure 4.10: Power supply DC link voltage for a 200W BLDC motor load

The slight discrepancy between the two DC link voltage waveforms (Figure 4.10) is due to a limitation in the modelling of switching loss in the full system simulation. When the output current falls to zero (see Figure 4.9 (b)) there is no longer any load on the power supply. If the power supply was 100% efficient the DC link voltage would be constant during this period as there would be nothing to discharge it. However, as the DC link capacitance is so small the inverter losses still present a significant enough load to discharge it rapidly. When the DC link voltage becomes very small, the simulated inverter loss is negligible leading to the reduced discharge rate of the DC link capacitor. During this period the real (hardware) inverter loss is still significant, causing the DC link capacitor to discharge to virtually zero. This discrepancy can also be seen in the hardware input current (Figure 4.11) where a small current draw still exists near the mains zero crossing. As there is no load on the power supply this current draw is solely to supply the inverter losses. The simulation results show no current draw during this period as the DC link voltage is still higher than the mains voltage.

This relatively long period of time when the power supply is unloaded is the reason for the notable drop in efficiency (Table 4.3) compared to the RL load results (Table 4.1). This issue is analysed in more detail in Section 4.5.

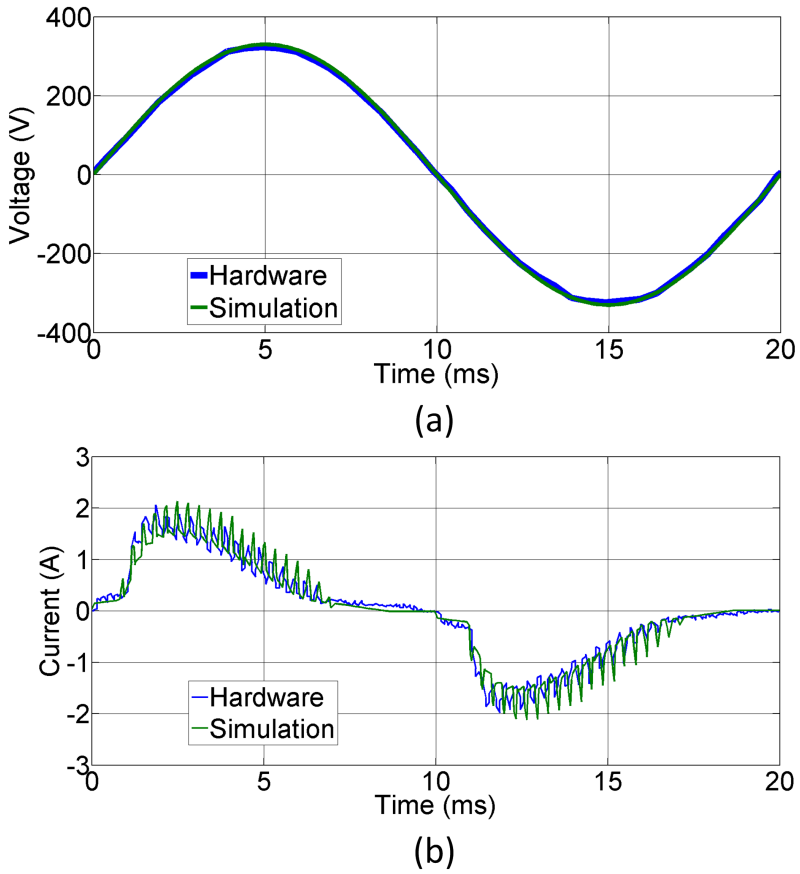

Figure 4.11: Power supply input(a) voltage and (b) current for a 200W BLDC motor load

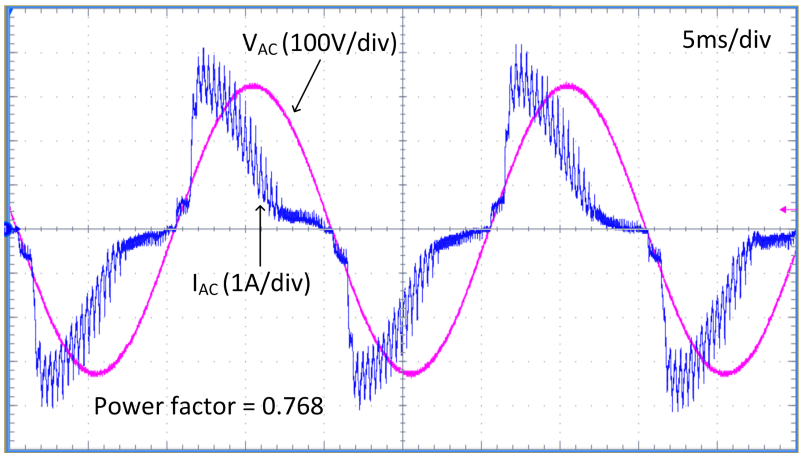

Figure 4.12: Oscilloscope screenshot showing power supply input voltage and current for a 200W BLDC motor load

Parameter	Hardware	Simulation	Error
I_{AC}	$0.91A_{RMS}$	$0.85A_{RMS}$	6.6%
V_{AC}	$230V_{RMS}$	$230V_{RMS}$	0%
V_{DC}	$202V_{mean}$	$218V_{mean}$	7.4%
V_{out}	$18V_{mean}$	$18.7V_{mean}$	3.7%
I_{out}	$6.88A_{mean}$	$6.53A_{mean}$	5.1%
P_{in}	160W	157W	1.9%
P_{out}	133W	130W	2.3%
Efficiency	83.1%	82.8%	0.4%

Table 4.3: Key measurements for the power supply hardware and simulation with a 200W BLDC motor load

Measurement Setup for Fourier Analysis

The simulation and hardware results in this thesis include a considerable amount of Fourier analysis in order to clearly demonstrate the harmonic performance of each test setup. An overview of the Fast Fourier Transform (FFT) acquisition method is given below and is consistent throughout the thesis.

Parameter	Hardware	Simulation
Window function	Rectangular	Rectangular
Sample time	40ms	40ms
Sampling frequency	1MHz	1MHz
Frequency span	500kHz	500kHz
Frequency resolution	50Hz	50Hz
Processor	Tektronix DPO7104 oscilloscope	SaberRD waveform calculator

Table 4.4: Fast Fourier Transform acquisition settings used for all tests

It should be noted that when testing a product for compliance with BS EN 61000-3-2 regulations, it is necessary to use a longer 1.5 second capture window followed by an arithmetic average of each harmonic amplitude. This is to ensure that variations in the cycle-by-cycle harmonic spectrum of the product are accounted for. There are two reasons this exact procedure was not adhered to during the results analysis in this thesis. Firstly, it was not practical to generate 1.5 seconds of simulation data due to the 10ns time step required to properly capture the power device switching

events. As well as taking many hours to complete, the simulation PC did not have enough memory to store the vast amount of data which would have been produced. Secondly, due to the idealised nature of the simulation, it produced completely consistent results from one mains cycle to the next, therefore making a long capture window redundant. Whilst neither of these issues applied to the hardware tests, it was deemed sensible to use the same test method for consistency.

Fourier analysis of the input current (Figure 4.13 and 4.14) shows the presence of significant low order harmonics as well as the motor drive switching frequency. Figure 4.14 includes the BS EN 61000-3-2 Class A harmonic limits which have been scaled down based on the active input power to the system. If the absolute harmonic limits were used (Table 1.1) there would be no risk of exceeding them in this case due to the relatively low power of the system. Therefore, in order to demonstrate the scalability of the approach used in this thesis, all harmonic analysis is carried out with respect to the relative, rather than absolute harmonic limits. This is identical to the approach taken for Class D devices (Table 1.1), whereby the limits are given as mA per Watt of active input power.

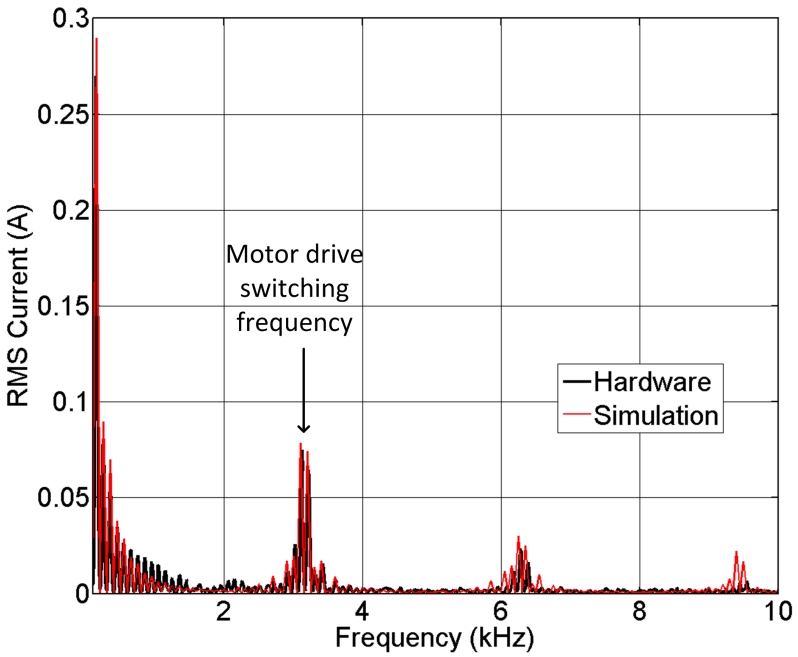

Figure 4.13: Power supply input current harmonics with a 200W BLDC motor load

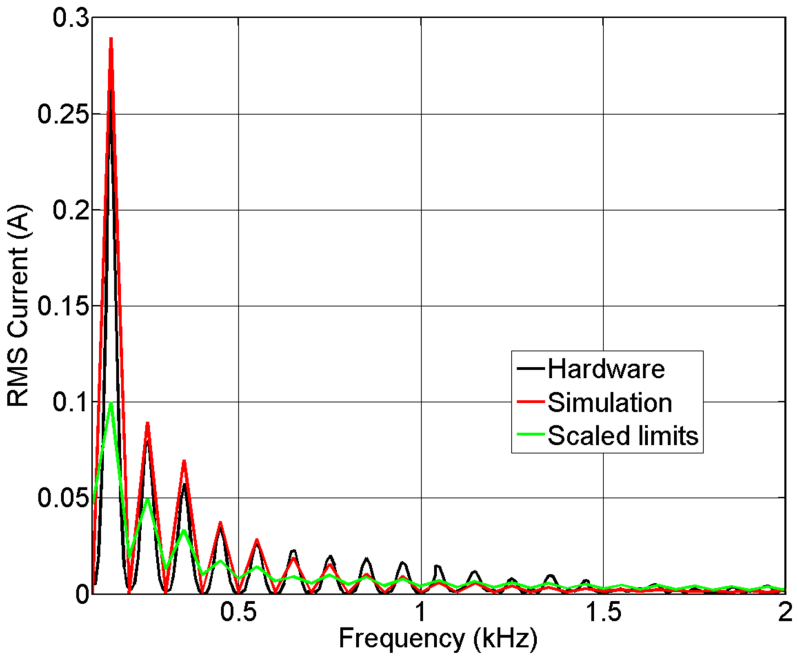

Figure 4.14: Input current harmonics with a 200W BLDC motor load shown against scaled BS EN 61000-3-2 Class A limits

It can be seen that a high load capacitance causes distortion to the input current shape in exactly the same manner as a large DC link capacitance would. By dividing the capacitance on the secondary side of the transformer by the square of the turns ratio, the equivalent primary side capacitance can be deduced. Given the turns ratio is 12 in this case, the equivalent DC link capacitance is 13.9µF. In order to improve the harmonic performance of the complete system it is therefore necessary to also minimise the load capacitance as demonstrated in Section 4.3.

4.3 Power Supply Testing with a Zero Capacitance BLDC Motor Drive

For the following tests the two parallel 1000µF motor drive capacitors were removed to assess the conclusions reached in the previous section. As discussed in Section 3.1, the motor drive was originally designed to operate from a lithium-ion battery pack. To prevent the cells from overheating, the capacitors were fitted in parallel to reduce the amplitude of the ripple current drawn from the battery pack. When operating from the reduced capacitance power supply, these components were not strictly necessary for the motor drive to run, and hence they were removed. A dia-

gram of the hardware and simulation setup for these tests is shown in Figure 4.15, with the motor drive parameters as per Table 4.5. As previously, the power supply parameters can be found in Table 3.3.

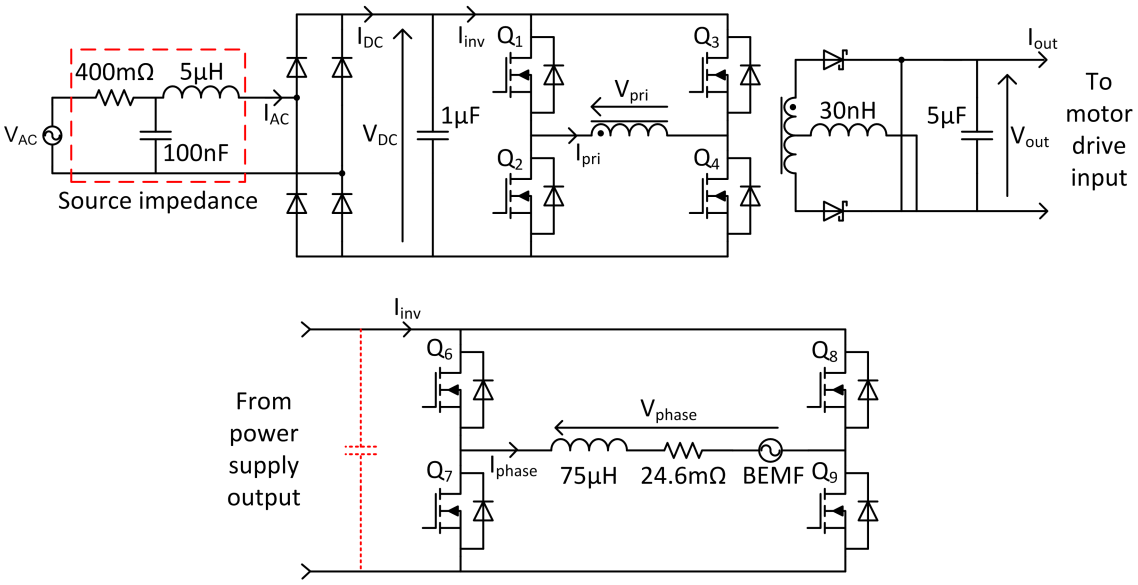

Figure 4.15: Simulation and hardware test setup for the reduced capacitance power supply and zero capacitance 200W BLDC motor drive load

Parameter	Value
V_{out}	16.5V_{mean}
C_{drive}	Removed
L_{wind}	75µH
R_{wind}	24.6mΩ
BEMF	17.15V_{pk-pk}
Speed	90,000RPM
Advance	10°
Conduction	91°
Freewheel	89°
MOSFETs	IRFH7932

Table 4.5: Parameters for the zero capacitance 200W BLDC motor drive when running from the reduced capacitance power supply

As seen in Figure 4.16 (a) and 4.18, the removal of the motor drive capacitance caused the output and DC link voltage waveforms to resemble a rectified sinusoid,

much like those seen in the earlier resistive load tests. On the other hand, it is clear from Figure 4.16 (b) that the power supply output current envelope does not match that of the output voltage, indicating a non-resistive load behaviour. Due to the minimal decoupling available, this directly affects the input current shape and therefore power factor. The non-linear load current draw occurs as the standard motor drive control system is designed to produce a constant output power over a range of supply voltages (as outlined in Section 3.1). This means that as the power supply output voltage falls, the control system attempts to increase the current to compensate. Under these conditions the motor drive therefore exhibits a negative impedance characteristic which is not conducive to producing a high input power factor.

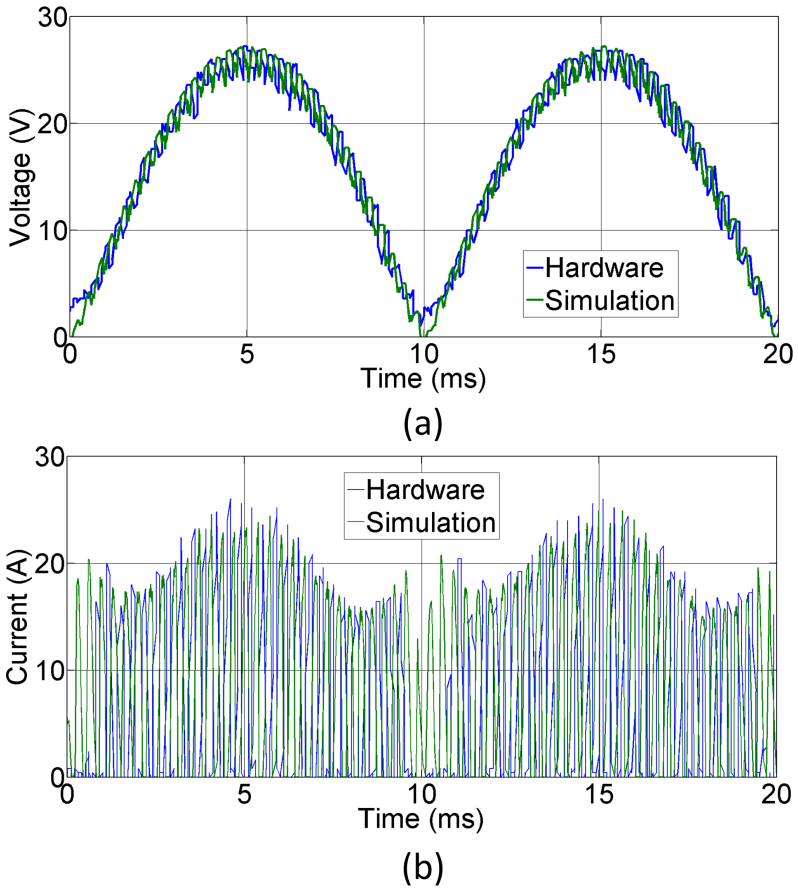

Figure 4.16: Power supply output voltage (a) and current (b) for a zero capacitance 200W BLDC motor load

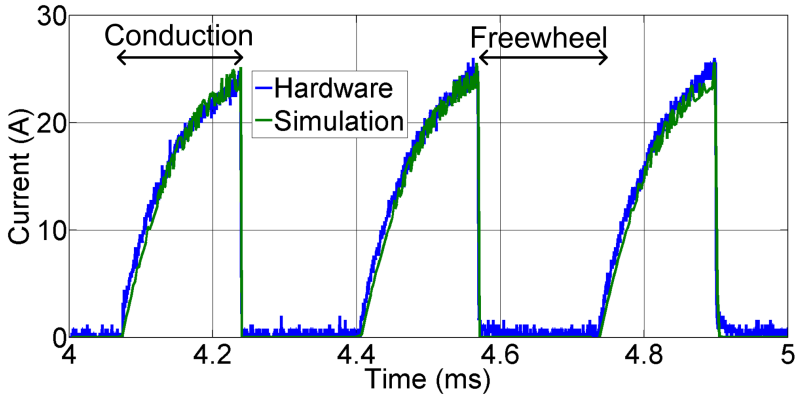

Figure 4.17: Zoomed view of output current measurement in Figure 4.16

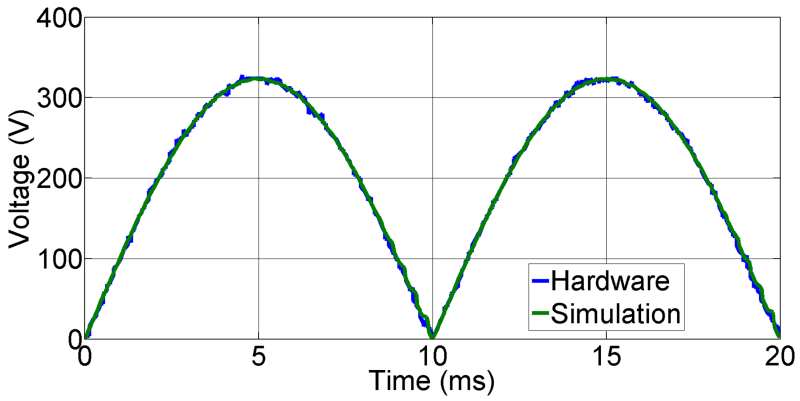

Figure 4.18: Power supply DC link voltage for a zero capacitance 200W BLDC motor load

As with the resistive-inductive and standard motor drive loads tested, the power supply input current profile (Figure 4.19) matches that of the output current (Figure 4.16) due to the minimal decoupling. An even greater drop in efficiency (Table 4.6) is seen with the zero capacitance motor load because the power supply spends more time in an unloaded state. Given that the motor drive has a fixed conduction angle of 91° out of every 180° half-cycle, it only presents a load to the power supply for approximately 51% of the time. By contrast the 2000µF capacitance of the standard motor drive causes it to present a load 65% of the time as can be seen in Figure 4.9, and hence the efficiency is greater. It can also be seen that with the standard motor drive the power supply is only unloaded when the DC link voltage is small, making the loss less severe. For the tests using a power resistor there is a constant load on the power supply, resulting in the highest overall efficiency. This issue is discussed in more detail in Section 4.5.

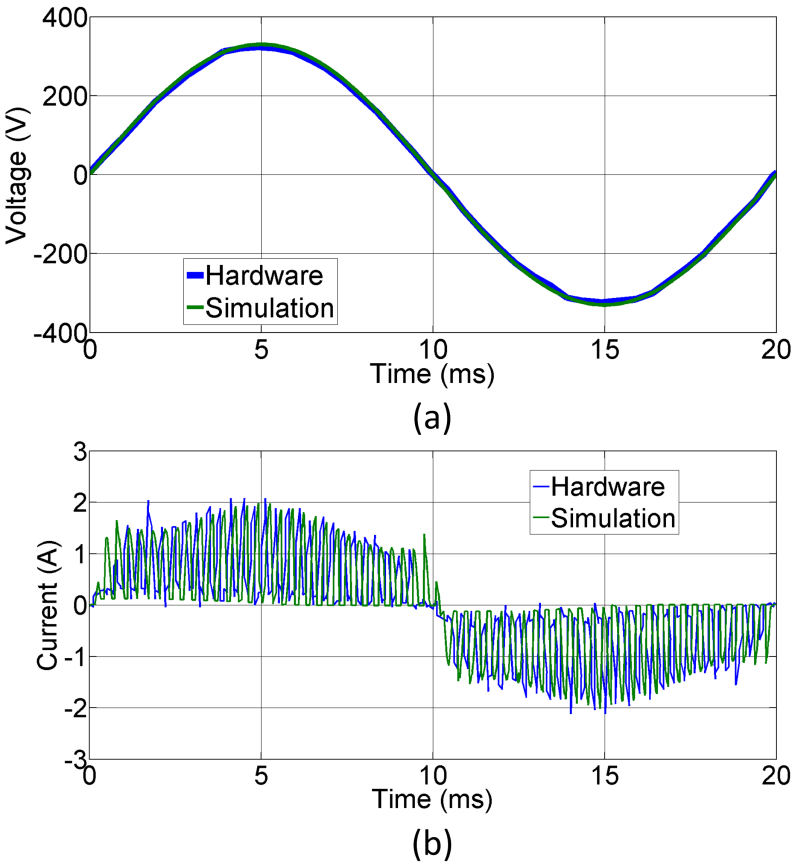

Figure 4.19: Power supply input (a) voltage and (b) current for a zero capacitance 200W BLDC motor load

Parameter	Hardware	Simulation	Error
I_{AC}	$0.92A_{RMS}$	$0.97A_{RMS}$	5.2%
V_{AC}	$230V_{RMS}$	$230V_{RMS}$	0%
V_{DC}	$205V_{mean}$	$206V_{mean}$	0.5%
V_{out}	$16.5V_{mean}$	$16.3V_{mean}$	1.2%
I_{out}	$7.93A_{mean}$	$7.86A_{mean}$	0.9%
P_{in}	156W	159W	1.9%
P_{out}	120W	123W	2.4%
Efficiency	76.9%	77.4%	0.6%

Table 4.6: Key measurements for the power supply hardware and simulation with a zero capacitance 200W BLDC motor load

As with the standard motor drive load, the input current draw caused by the no-load losses can be seen in the oscilloscope screenshot in Figure 4.20. In between the pulses caused by the motor drive conduction it can be seen that the input current

does not fall to zero, instead oscillating at a frequency of 1MHz due to the power supply switching (2x 500kHz PWM frequency). As there is no power supply output current during these periods, the input current supplies only the inverter switching losses. As the bridge rectifier and DC link capacitor ESR losses were under 0.5W each they were relatively insignificant. Additionally, the gate drivers and control electronics were powered from external sources so they did not contribute to the input current draw at all.

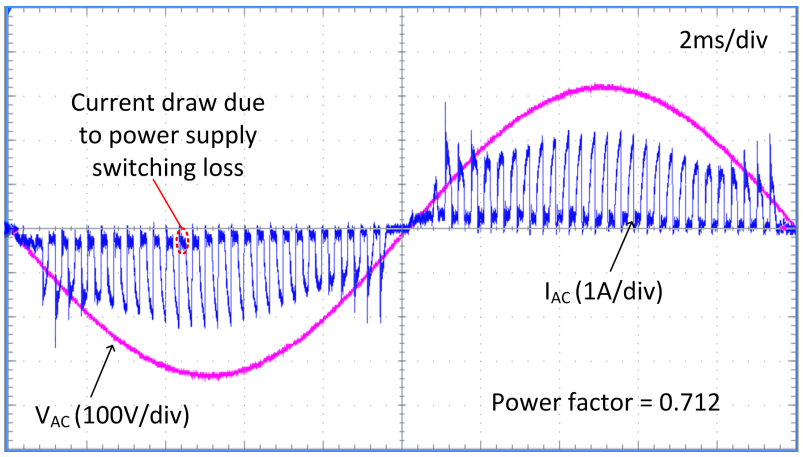

Figure 4.20: Oscilloscope screenshot showing power supply input voltage and current for a zero capacitance 200W BLDC motor load

Shown in Figure 4.21 and 4.22 are the FFT results for the power supply input current whilst running the zero capacitance motor drive. Compared with the standard motor drive results (Figure 4.14), a significant reduction in low order harmonics can be seen. However, It is clear that further work is still required for the system to meet the scaled EN61000-3-2 harmonic limits. It is also evident that by removing the large capacitors from the motor drive, the 3kHz load frequency harmonics have become far more prominent. Despite almost meeting the harmonic limits, the net result is a power factor of only 0.712. This would prevent the system from meeting the requirements of other desirable standards such as Energy Star.

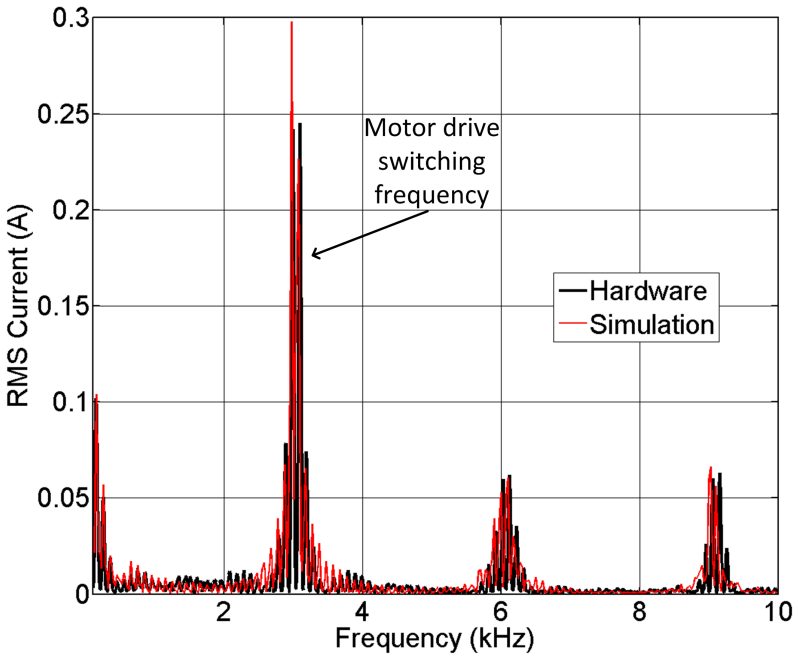

Figure 4.21: Input current harmonics for a reduced capacitance power supply and motor drive

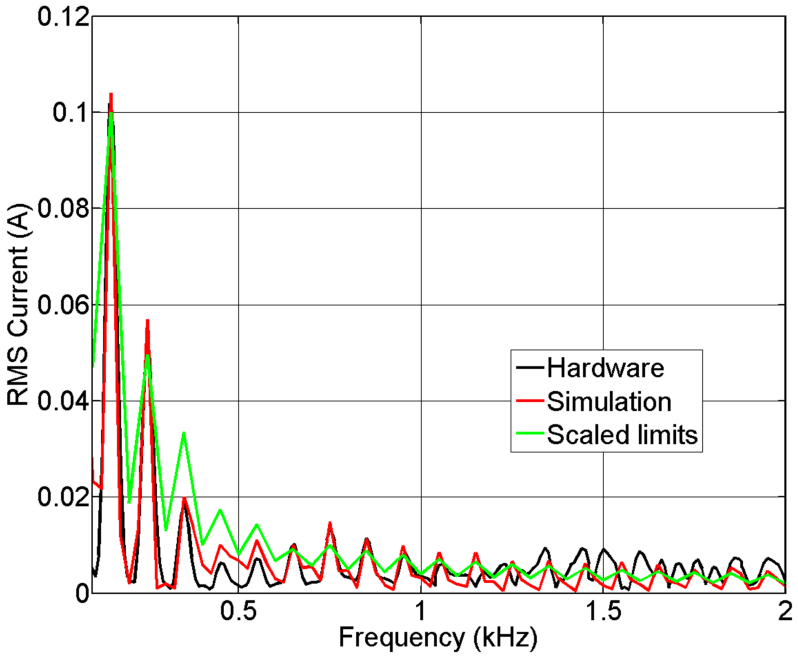

Figure 4.22: Input current harmonics for a reduced capacitance power supply and motor drive shown against scaled BS EN 61000-3-2 Class A limits

4.3.1 Motor Drive Conduction Angle Modulation

To reduce the magnitude of the low order (0-2kHz) input current harmonics, it was necessary to alter the motor drive control system so that the inverter current demand was always proportional to the supply voltage. This would then make the load appear linear and reduce the level of harmonics in the input current. As a result of this change, the low order harmonics (particularly the 3^{rd}, 5^{th} and 7^{th}) can be eliminated at their source rather than through passive or active filtering, helping to reduce the size and cost of the overall system. This technique does not affect the size of the motor drive switching harmonic (3.1kHz), but due to its higher frequency it can be suitably attenuated using a relatively small filter.

Existing Implementation

This same issue was faced by the industrial sponsor during the development of a single-phase, mains-powered, 1600W BLDC motor drive system for high power compressor applications. The motor drive also used a reduced capacitance approach with 100% DC link voltage ripple, in an effort to improve the net power density and power factor of the system. This similarly suffered from a non-linear load behaviour, whereby the current drawn by the motor drive was not proportional to the DC link voltage. The remainder of this section describes the technique used to solve this problem, which was subsequently adapted and simulated for the 200W motor drive used in this research.

Shown in Figure 4.23 is the simplified circuit for the 1600W BLDC motor drive system, along with the DC link voltage and speed over one mains cycle. Given that there is 100% ripple in the DC link voltage, it is not possible to maintain constant power over a complete mains cycle. For the purposes of improving input current harmonics, it is of course desirable to make the motor power vary sinusoidally, such that it looks like a linear load and achieves a high power factor. This sinusoidal variation in power subsequently causes the speed to vary at the same frequency, but due to the inertia of the system it is not significant enough to be noticed by the user, nor does it cause any significant issues with the performance of the compressor. It should be noted that the optimisation of the motor drive for harmonic performance does have a negative impact on power density, requiring a slightly larger motor for a given power output. However, extensive research has shown this to be a worthwhile

compromise; a point made particularly clear through the decision to implement it in a mass-manufactured product.

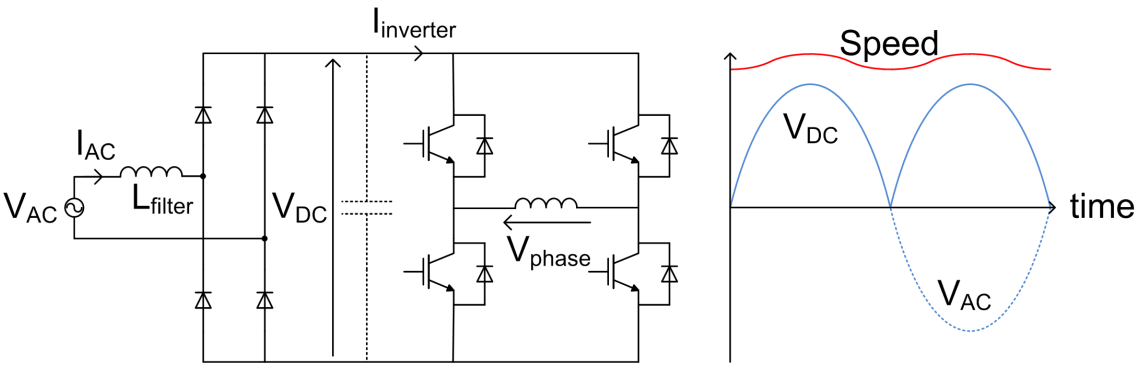

Figure 4.23: Schematic and supply voltage waveforms for the 1600W motor drive

To further improve the input current quality, the drive control system modulates the size of the conduction angle in a predefined pattern synchronised to the line voltage. As was shown in Figure 3.2 the conduction angle is the portion of the motor electrical half-cycle during which the DC link voltage is applied across the motor winding terminals. For a single-phase motor this can be up to 180 degrees (as there is a positive and negative half-cycle), and is the period where the motor receives power from the drive.

To ensure the modulation sequence remains synchronised with the mains, the system includes a zero crossing detector. This provides a digital signal to the microcontroller which changes state each time the mains voltage crosses zero. When this occurs, a 'change notification' interrupt is triggered which resets the lookup table pointer to the beginning of the conduction angle map. To ensure that supply voltage noise does not cause false triggering of the zero crossing detector, an RC lowpass filter is used with the cutoff frequency chosen to provide maximum noise rejection without introducing significant phase shift.

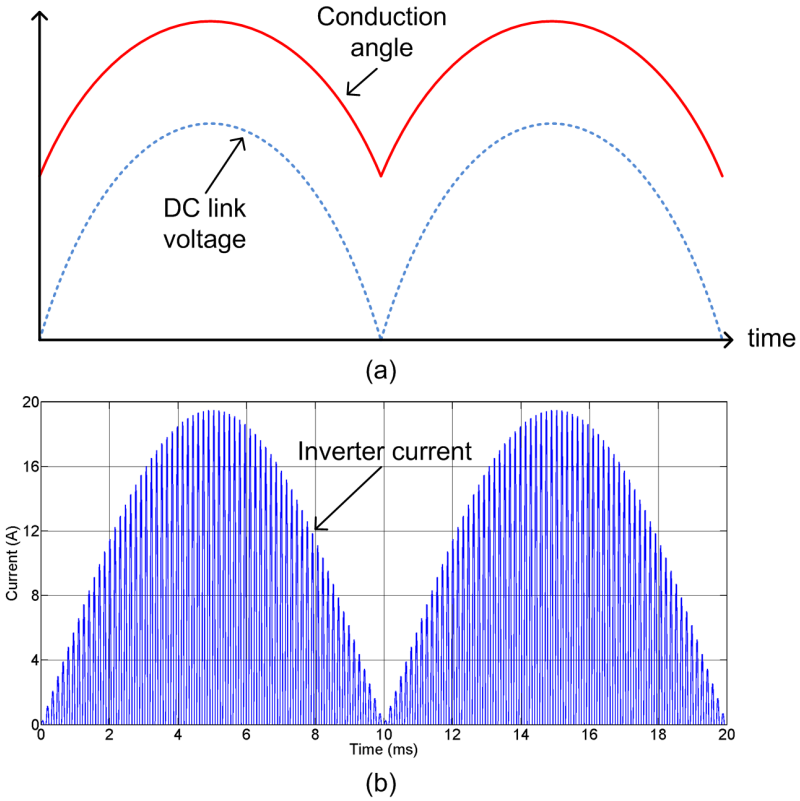

Figure 4.24: (a) Mains-synchronised conduction angle modulation sequence and (b) resulting inverter current

The modulation pattern (Figure 4.24(a)) causes the envelope of the inverter current draw (Figure 4.24(b)) to follow the shape of the DC link voltage. The 2.5mH filter inductor and 4.4µF DC link capacitor form a 1.5kHz low pass filter, resulting in a 25dB reduction in the inverter switching frequency component, and subsequently an input current as shown in Figure 4.25. If this control modification had not been implemented, the motor drive would have produced more low-frequency current harmonics; ultimately requiring a lower frequency, and therefore larger input filter. This being said, even with the conduction angle modulation system, the necessary LC filter makes up a significant proportion of the overall motor drive volume and cost.

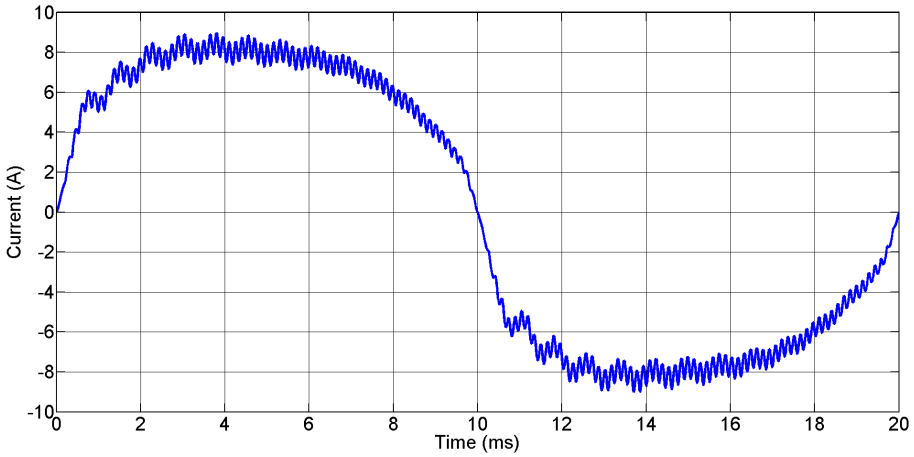

Figure 4.25: Line current of the 1600W BLDC motor

Adaptation for the 200W BLDC Motor Drive

A look up table was produced relating the supply voltage to the motor conduction angle, which then allowed control of the phase current. As the shape of the supply voltage was known in advance (a rectified sinusoid), it was simpler to modulate the conduction angle based on time rather than voltage. By synchronising the look up table to the zero crossing of the mains supply, a pre-programmed sequence could be used without continuous monitoring of the DC link voltage. The contents of this lookup table are shown graphically in Figure 4.26.

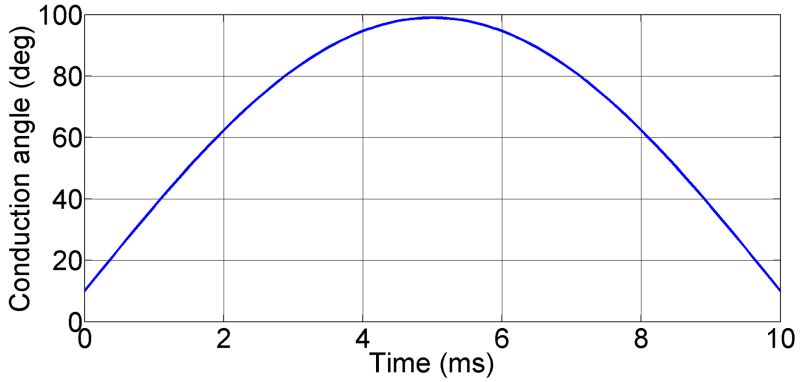

Figure 4.26: Conduction angle modulation map to improve motor drive low order harmonic performance

Due to the time constraints on the project, the conduction angle modulation controller could only be tested in simulation. A hardware implementation would have

required the addition of a mains zero crossing detector along with considerable changes to the drive control software. However, the simulated input current waveform (Figure 4.27) and its respective FFTs (Figure 4.28 and 4.29) show a marked reduction in low order harmonics due to this change, particularly below 500Hz. On the other hand, the system is much less effective above 1kHz, with a number of harmonic components hitting the scaled limits.

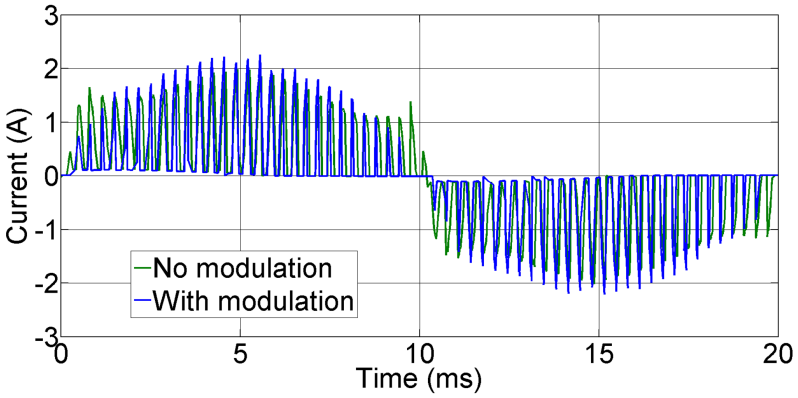

Figure 4.27: Input current comparison with and without conduction angle modulation

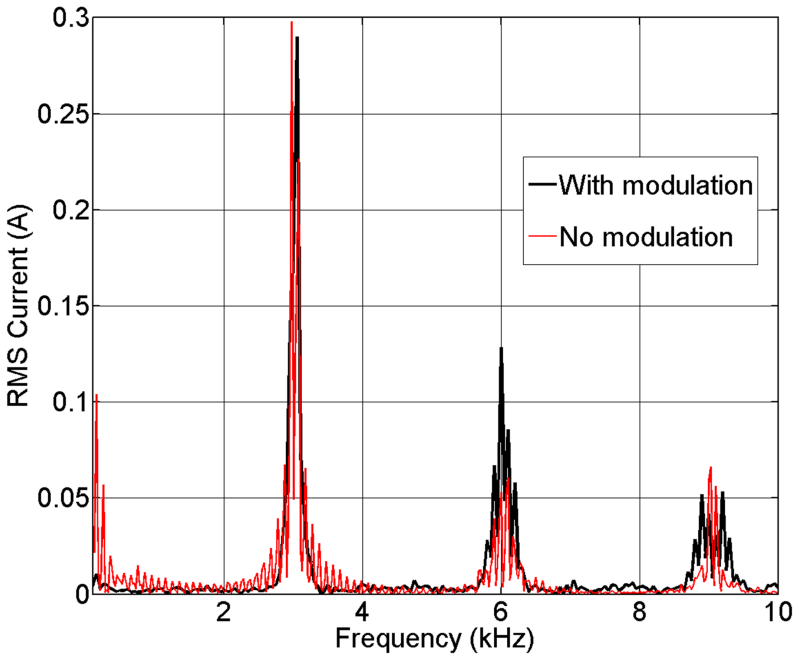

Figure 4.28: Input current harmonics with and without conduction angle modulation

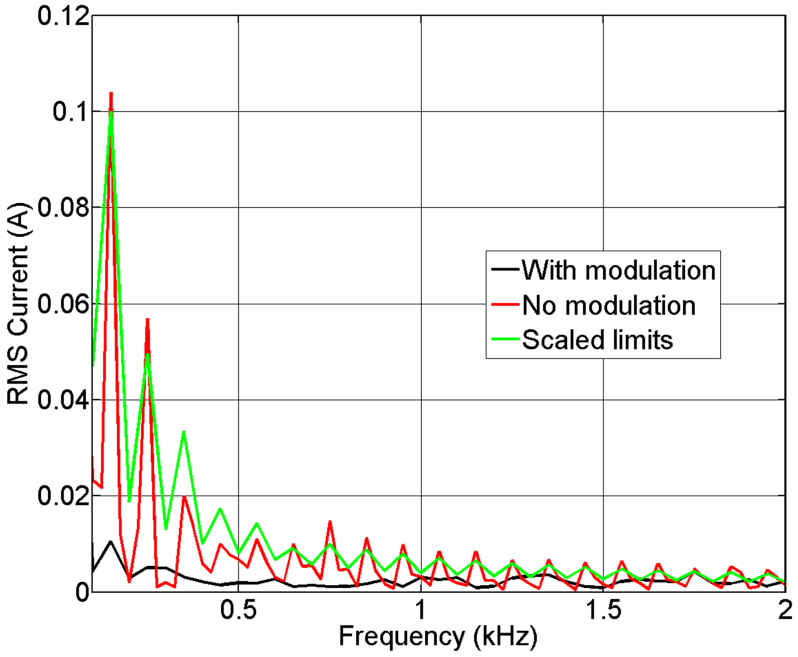

Figure 4.29: Input current harmonics shown against scaled BS EN 61000-3-2 Class A limits

A downside of improving the low order harmonic performance of the system is an increased motor torque ripple at 100Hz, which produces a corresponding ripple in the motor speed. This is seen in the performance of the 1600W BLDC motor, but is not significant enough to be noticed by the user, and therefore not considered a major problem. The net positive impact of this modification means that a practical implementation would be a desirable future extension to this work.

4.4 Power Supply Simulation with a Conventional Smooth DC Link Voltage

To provide a point of comparison, the simulation model was altered to have a conventional smooth DC link voltage, keeping the zero capacitance BLDC motor drive as the load. A diagram of the simulation setup for these tests is shown in Figure 4.30, with the relevant motor drive parameters in Table 4.7. As previously, the power supply parameters are unchanged and can be found in Table 3.3. Unfortunately, it was not practical to add a large electrolytic capacitor to the power supply PCB, so no hardware results could be obtained for the tests in this section.

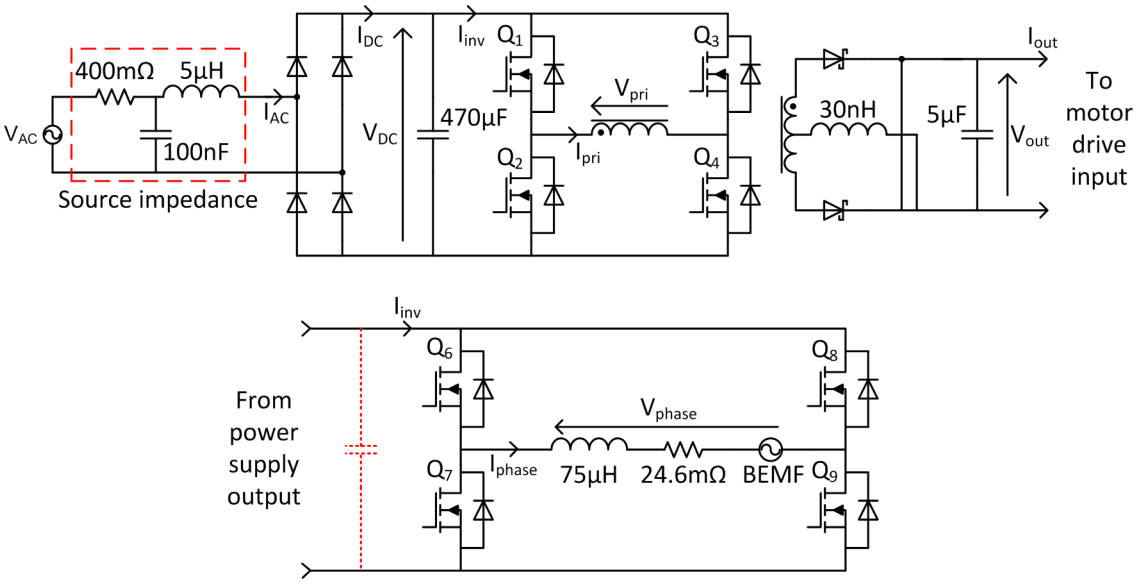

Figure 4.30: Simulation and hardware test setup for the high capacitance power supply and zero capacitance 200W BLDC motor drive load

Parameter	Value
V_{out}	25.7V_{mean}
C_{drive}	Removed
L_{wind}	75µH
R_{wind}	24.6mΩ
BEMF	17.15V_{pk-pk}
Speed	90,600RPM
Advance	10°
Conduction	79°
Freewheel	101°
MOSFETs	IRFH7932

Table 4.7: Parameters for the zero capacitance 200W BLDC motor drive when running from a high capacitance power supply

By replacing the 1µF film DC link capacitor model with a 470µF electrolytic device, a ripple voltage of 20V_{pk-pk} was achieved as shown in Figure 4.31. Consequently there was only a very short period where the supply voltage exceeded the DC link voltage, restricting the input current flow to short pulses (see Figure 4.32). As a result of this the input current has a very rich harmonic spectrum, leading to a high RMS input current and subsequently a very poor power factor of 0.45.

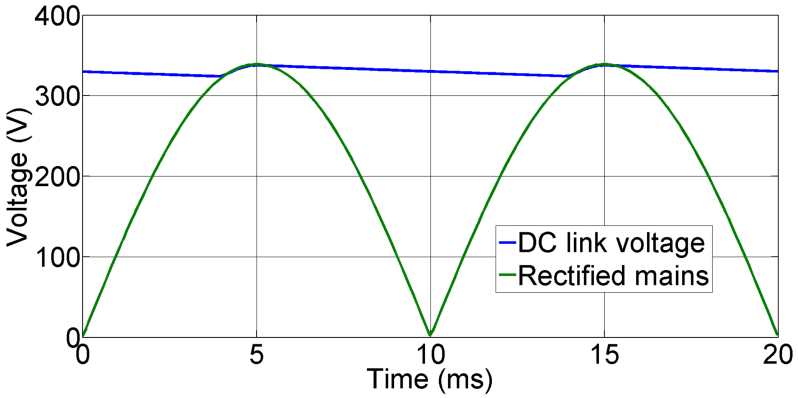

Figure 4.31: Simulated DC link voltage and rectified mains voltage with a 470µF DC link capacitor

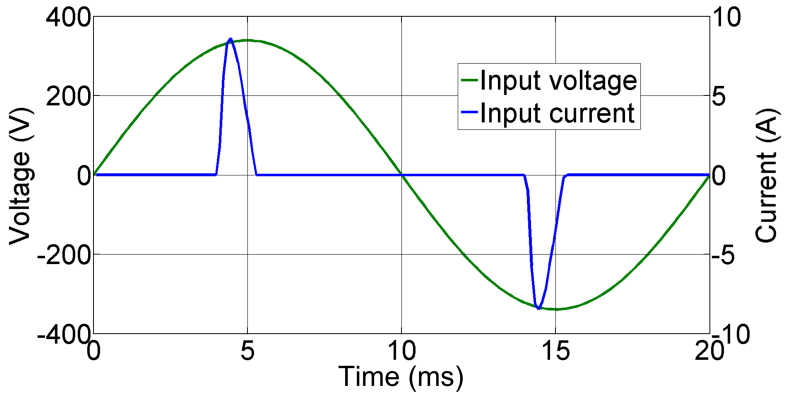

Figure 4.32: Simulated input current and voltage with a 470µF DC link capacitor

As can be seen in Figure 4.34 the scaled BS EN 61000-3-2 Class A limits are greatly exceeded when using a conventional DC link design, and would require heavy filtering or APFC to bring the harmonics under control. The higher frequency motor drive harmonics are however completely eliminated by the DC link capacitor.

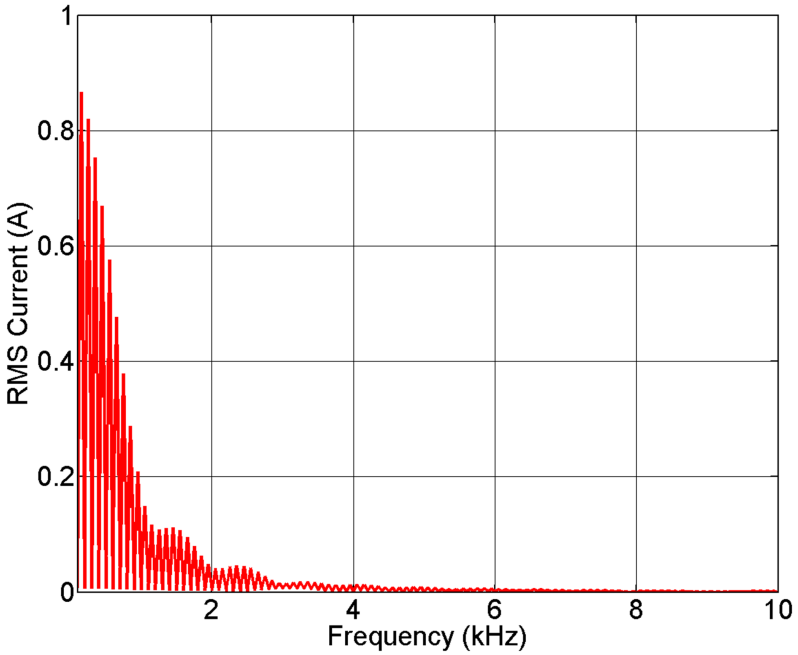

Figure 4.33: Input current harmonics for a conventional smooth DC link

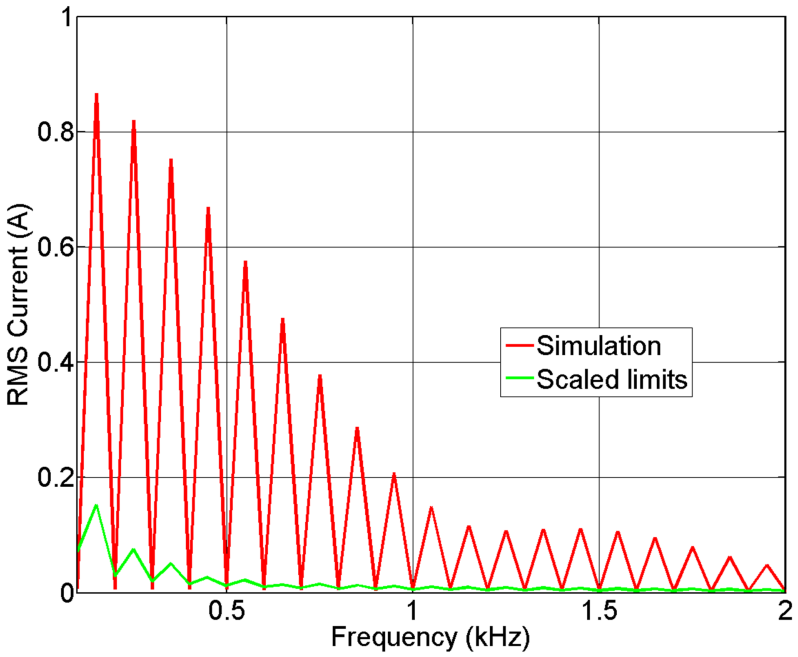

Figure 4.34: Input current harmonics for a conventional smooth DC link shown against scaled BS EN 61000-3-2 Class A limits

An advantage of this approach is that the motor drive can produce a higher power from the same peak DC link voltage, reducing the stress on components and/or allowing lower rated parts to be used. It is also easier to keep the motor at its ideal

operating point as the supply voltage is not constantly changing. The results in this section further demonstrate the necessary trade-off between input and output power quality in a single-phase AC to DC converter. A large amount of energy storage produces a high quality DC output but a poor AC input power factor. Conversely, the earlier results in this chapter show that using a small amount of energy storage produces a higher input power quality but a poorly regulated DC supply.

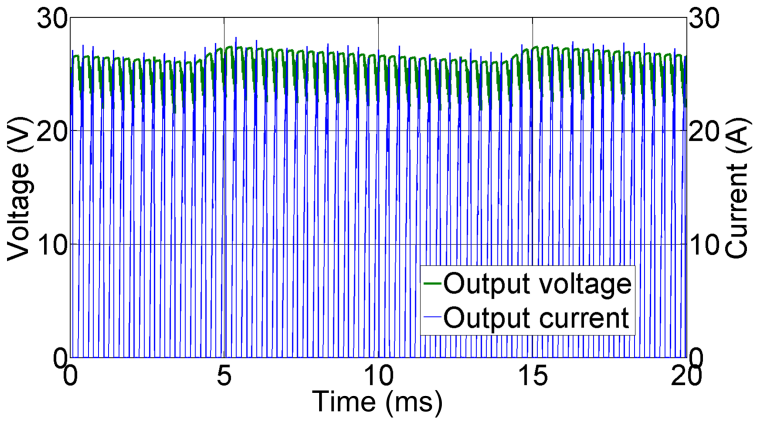

Figure 4.35: Simulated output current and voltage with a 470µF DC link capacitor

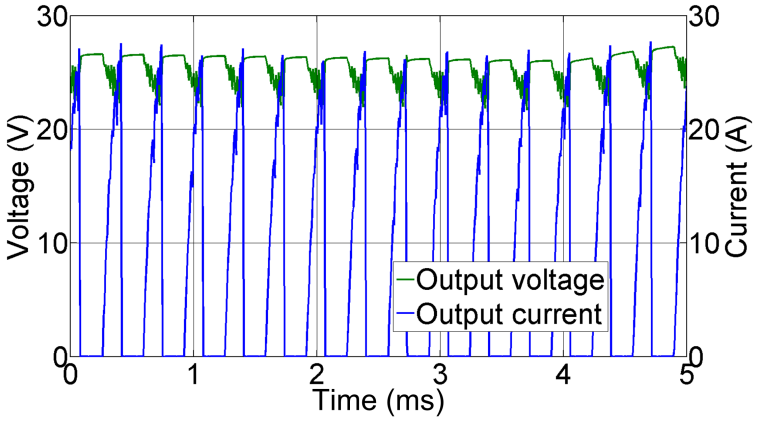

Figure 4.36: Zoomed view of Figure 4.35

The use of a large DC link capacitor alone does not improve the efficiency of the power supply. As it is positioned before the inverter it provides no smoothing of the load current pulsations and therefore the power supply still spends a large proportion of the time unloaded. This can be seen in the zoomed output current waveform in Figure 4.36. As explained in Section 4.5, the inverter switching loss is increased

as the average DC link voltage is higher than that of the reduced capacitance design. In order to improve the efficiency of the basic hard switched converter, a large output filter capacitor would also be required to ensure a constant load on the inverter.

Parameter	Simulation
I_{AC}	$2.34A_{RMS}$
V_{AC}	$230V_{RMS}$
V_{DC}	$321V_{mean}$
V_{out}	$25.7V_{mean}$
I_{out}	$7.50A_{mean}$
P_{in}	245W
P_{out}	182W
Efficiency	74.3%
Power factor	0.45

Table 4.8: Key measurements for the 470µF DC link capacitor simulation

The two capacitors shown in Figure 4.37 are the 1µF film device used in the reduced capacitance power supply and a 470µF electrolytic part for comparison. The electrolytic capacitor is over 13 times the volume and 5 times the cost of the film capacitor, highlighting the benefit of a reduced capacitance design. A further point to note is that electrolytic capacitors are generally limited to 450V to prevent breakdown of the dielectric (the pictured device is rated to 400V). In situations where a boost converter front end is used this may not be high enough, requiring series connected devices and balancing resistors. As the net capacitance is halved in a series connection it is necessary to use four capacitors to achieve the same effect, increasing the volume, cost and manufacturing time without making any gains in performance. The required series/parallel arrangement required is shown in Figure 4.38.

Figure 4.37: Photo showing the size difference between a 1µF 630V film capacitor and a 470µF 400V electrolytic capacitor

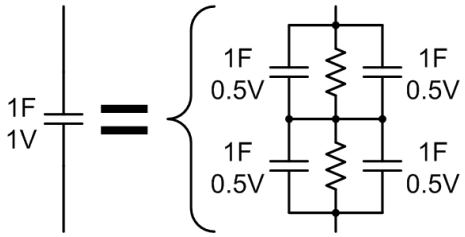

Figure 4.38: The necessary series/parallel arrangement needed to build up a high voltage rating when using electrolytic capacitors

Another important extension to this work would be an investigation into the effect that reduced DC link capacitance has on the motor design. To fully evaluate the benefits of this concept it is necessary to offset the gains in converter power density and power factor against the potentially increased size and/or losses in the motor. A thorough investigation of this issue would however involve significant further work, and is beyond the scope of this research.

4.5 Power Supply Switching Loss Analysis

The preceding hardware and simulation results have consistently highlighted a link between the efficiency of the power supply and the type of load connected. The results suggest that the inverter losses are higher when the power supply is unloaded (zero output current) than when it is loaded (positive output current). To gain a better understanding of the circuit operation, a more detailed analysis of the parasitic effects is necessary. As shown in Figure 4.39 there are three capacitances which affect the switching performance of a MOSFET - the gate-source C_{GS}, gate-drain C_{GD} and drain-source C_{DS} capacitances. The input capacitance C_{ISS} is made up of C_{GS} and C_{GD}, with the output capacitance C_{OSS} made up of C_{DS} and C_{GD}. For the power devices used, $C_{ISS} = 890pF$ and $C_{OSS} = 36pF$.

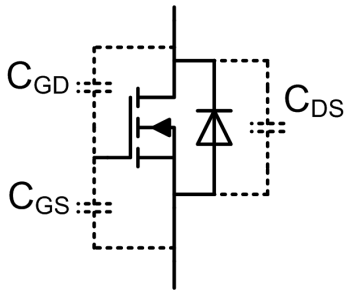

Figure 4.39: The key parasitic capacitances which affect MOSFET switching performance

The parasitic winding capacitance of the transformer is also critical in determining the power supply switching losses. The construction of the planar transformer causes it to have a higher than normal parasitic capacitance as the flat interleaved windings act as parallel plates which subsequently store charge. This is an accepted compromise in order to achieve a high power density and very low leakage inductance. For the planar device used, the parasitic capacitance seen from the primary winding (C_{pri}) is 200pF.

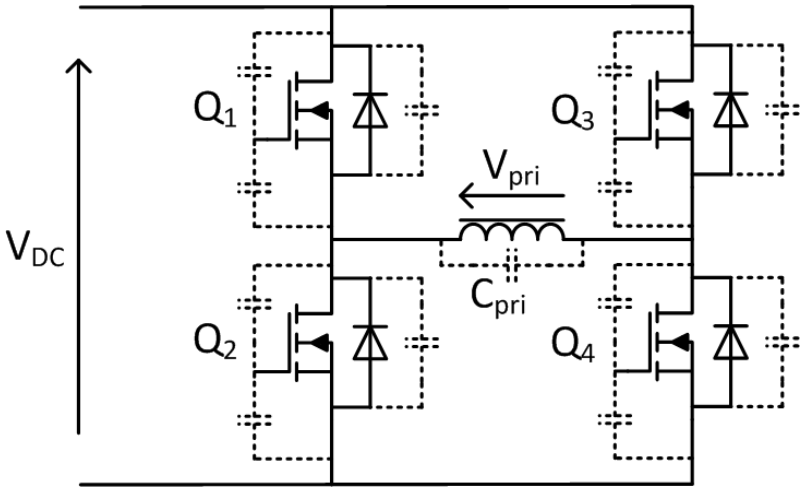

Figure 4.40: Simplified inverter model showing relevant parasitic capacitances

Shown in Figure 4.40 is a model of the inverter including the parasitic capacitances, with the relevant waveforms shown in Figure 4.41. When the inverter is loaded, the waveforms appear as expected with the primary voltage V_{pri} directly following the gate drive inputs. During the dead time period V_{pri} falls to zero as both legs of the inverter apply $\frac{1}{2}V_{DC}$ to the transformer terminals. The primary winding capacitance C_{pri} is completely discharged at this point and the four MOSFET output capacitances C_{OSS} are charged to $\frac{1}{2}V_{DC}$.

Considering the unloaded primary voltage waveform, V_{pri} does not fall to zero during the dead time period unlike the loaded case. The unloaded primary winding appears as an open circuit and all four MOSFETs are off, meaning that there is no path through which to discharge the parasitic capacitances. The primary winding and MOSFET drain-source voltages are therefore static at V_{DC} until the next pair of MOSFETs are turned on (V_{Q1} is shown as an example in Figure 4.41). This was confirmed by the hardware measurement shown in Figure 4.42, with the Q_1 drain-source voltage remaining at zero after the gate-source charge has been removed. It is not until Q_2 is turned on that the Q_1 parasitic capacitance has a current path to charge through, allowing its voltage to rise to V_{DC}. The assertion of negative output voltage across the load causes C_{pri} to discharge from V_{DC} to -V_{DC}.

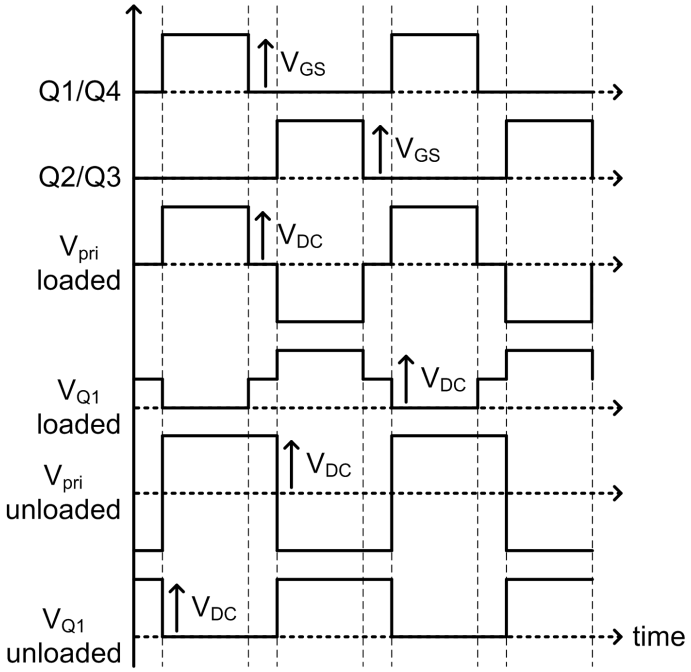

Figure 4.41: Power supply switching waveforms in the loaded and unloaded state

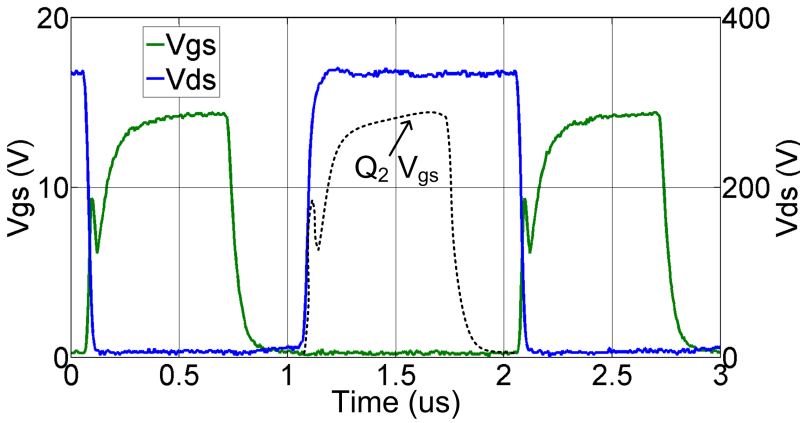

Figure 4.42: Q_1 gate-source and gate-drain voltage with no load on the power supply

The key point to note from the previous observation is that at the switching transition points, the parasitic capacitances are charged to twice the voltage in the unloaded case. When a MOSFET is turned on, its output capacitance is shorted, dissipating the stored energy within the device junction. Similarly, the primary winding capacitance is discharged through a pair of MOSFETs, also dissipating its stored energy in the devices. It is clear that higher parasitic capacitor voltages will therefore cause greater loss in the switches.

The standard formula for estimating MOSFET switching loss [83] is given as:

$$P_{sw}(total) = \quad P_{sw} \quad + \quad P_{COSS} \tag{4.1}$$

Where:

$$P_{sw} = \quad \frac{1}{2} I_{DS}.V_{DS}.(t_{on} + t_{off}).f \tag{4.2}$$

$$P_{COSS} = \quad \frac{1}{2} C_{OSS}.V_{DS}^2.f \tag{4.3}$$

V_{DS} and I_{DS} are the MOSFET drain-source voltage and current, f is the switching frequency and t_{on} and t_{off} are the turn on and turn off switching times. The first term of the equation, 4.2, accounts for the loss due to the simultaneous non-zero current and voltage during the device switching transition. The duration of this period can be approximately determined by the gate drive current (0.75A) and gate charge (31.5nC), giving a transition time of 42ns. The second term, 4.3, accounts for the dissipation of the energy in the parasitic output capacitance.

In order to obtain the full switching loss in this case, the effect of discharging the primary winding capacitance C_{pri} must also be accounted for:

$$P_{CPRI} = \quad \frac{1}{4} C_{pri}.V_{pri}^2.f \tag{4.4}$$

The reason for the $\frac{1}{4}$ term in Equation 4.3 is that the energy stored in C_{pri} is discharged in both conducting switches, with half of the loss occurring in each device.

Another loss mechanism which needs to be accounted for is the conduction loss, determined simply by the average drain current I_{DS} and device channel on-resistance $R_{DS(on)}$:

$$P_{cond} = \quad I_{DS}^2.R_{DS(on)} \tag{4.5}$$

The final factor to be accounted for is the body diode reverse recovery loss P_{RR}. Due to the difficulty of calculating this in isolation, the loss figures were taken directly from the full system simulation which included a fully parameterised body diode model for each of the inverter MOSFETs. At the mean DC link voltage the loss was found to be 0.25W when loaded and 0.31W when unloaded. The total MOSFET loss per device is therefore:

$$P_{loss} = P_{sw} + P_{COSS} + P_{CPRI} + P_{cond} + P_{RR} \quad (4.6)$$

Using the previous equations the loss breakdown was determined as shown in Table 4.9. The calculations are based on the inverter operation with the zero capacitance motor drive load as in Section 4.3. In each case the average DC link voltage was 230V, switching frequency 500kHz and the average primary winding current was 1.11A when loaded.

	P_{sw} (W)	P_{COSS} (W)	P_{CPRI} (W)	P_{cond} (W)	P_{RR} (W)	Total (W)
Loaded	1.37	0.12	1.32	0.52	0.25	3.58
Unloaded	0	0.48	5.29	0	0.31	6.08

Table 4.9: Loss breakdown for individual inverter MOSFETs in the loaded and unloaded states

As discussed previously the zero capacitance motor drive presents a load to the inverter 51% of the time, leaving it unloaded for the remaining 49%. This is the case as the drive is in the conduction phase for 91 degrees and the freewheeling phase for 89 degrees of each motor half-cycle. The average power device switching loss is therefore 4.78W, making the total inverter loss 19.14W for all four devices. This is a fairly close match to the 20.7W figure obtained from the system simulation.

It is clear that hard switched operation at 500kHz is not ideal for this converter design when a highly transient load is connected. The data in Table 4.9 shows that the inverter losses are 69.8% higher when no load is present, due mainly to P_{CPRI}

being four times higher in this situation. The 89.7% efficiency achieved with an RL load shows that in a more conventional scenario the power supply design would provide good performance. However, for this application it is clear that further work is required to achieve an acceptable performance in power factor and efficiency simultaneously. A number of options are available to improve the efficiency of the system, but they all have drawbacks associated with them. Reducing the power loss will of course reduce the cooling requirements, meaning that smaller heatsinks can be used. This must be factored in when deciding on the best overall approach.

1. Reduce the switching frequency of the inverter - transformer and filter component size will increase along with cost
2. Use a transformer with lower winding capacitance - may require the use of a larger/heavier/lower frequency design
3. Use power devices with improved switching performance such as Gallium Nitride based FETs - higher cost and more complex gate drive requirements
4. Use a zero voltage switching topology - challenging to implement with a highly dynamic load and DC link voltage
5. Implement a no-load detection system to shut down or reduce the frequency of the inverter when there is zero output current demand - increased control system complexity.
6. Add a large output filter inductor and capacitor to remove the load frequency harmonic - as well as increasing the system size and cost this will introduce low order harmonics to the input current in the same manner as a large DC link capacitor

4.6 Conclusion

Following on from the literature review research, this chapter has practically evaluated the concept of reduced DC link capacitance. It is clear that for low cost motor drive applications, improvements can be seen in both power factor and power density when minimal energy is stored in the DC link. By allowing the use of film capacitor technology there is also potential for greatly increasing the product lifetime. A technique has been presented for reducing low order harmonics within the motor drive

itself, although as mentioned previously this was adapted from an existing system and is not entirely original research. It has been demonstrated that by limiting the capacitance in the power supply and the load, any transient in one is immediately reflected in the other. The decoupling in the system is sufficient only to remove the power supply switching frequency, having virtually no effect on the load or line frequency components. On the one hand this is desirable, as preserving the line frequency power flow throughout the system is key to producing a high power factor without requiring large reactive components. On the other hand, the load harmonics are present at the mains input, and despite not falling foul of the harmonic standards, they still lead to a significant reduction in power factor. Solving this issue in a low cost and compact manner forms the basis of the next two chapters of this thesis.

Chapter 5

APFC Control System Design

As highlighted in Chapter 4, a problem with the reduced capacitance design was that the load frequency harmonics formed a significant component of the input current, subsequently reducing the power factor. As the issue of low frequency (0-2kHz) harmonics had already been dealt with, it was therefore necessary to find an appropriate method of attenuating the motor switching frequency component. Clearly a solution had to be found which worked with minimal DC link capacitance, otherwise it would undermine the fundamental concept behind the design.

5.1 Filter Energy Storage

A basic but critical observation was made in that to remove a harmonic, it must be possible to store the peak oscillating energy carried by that frequency component. By constantly storing and releasing the oscillating energy, a filter can eliminate the reactive power flow at the target frequency as shown in Figure 5.1.

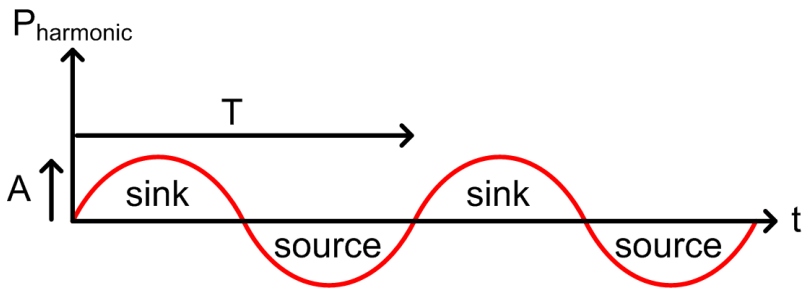

Figure 5.1: Reactive power flow in a filter for complete harmonic cancellation

Having made this observation, the theoretical minimum energy storage capacity of a filter can be deduced. As energy is the integral of power with respect to time, the peak energy storage requirement is equal to the area under $P_{harmonic}$ over half the time period T:

$$E_{filter} = \int_0^{\frac{T}{2}} P_{harmonic}\ \mathrm{d}t \tag{5.1}$$

Where:

$$P_{harmonic} = Asin(\omega t) \tag{5.2}$$

Therefore:

$$E_{filter} = \int_0^{\frac{T}{2}} Asin(\omega t)\ \mathrm{d}t = \frac{A.T}{\pi} = \frac{A}{\pi f} \tag{5.3}$$

Equation 5.3 demonstrates the minimum energy storage capacity required to completely eliminate a harmonic of frequency f and amplitude A. The inverse energy/frequency relationship highlights the advantage of a reduced capacitance converter, which has the input current harmonics concentrated at a higher frequency than a conventional AC/DC converter. This relationship is shown graphically in Figure 5.2, which assumes a harmonic power amplitude $A = 1$.

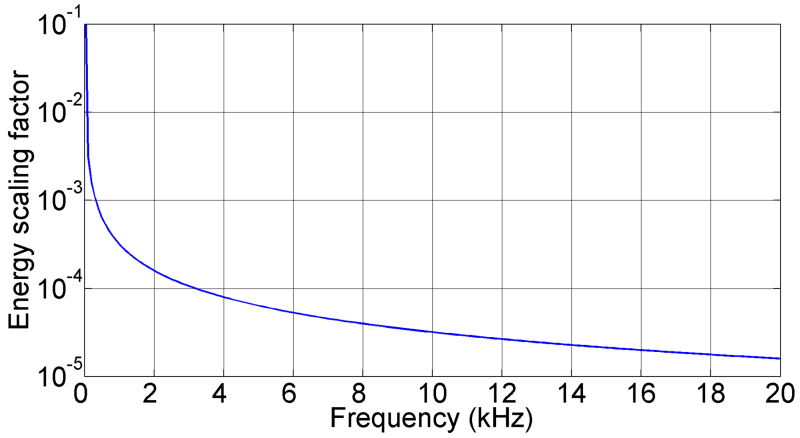

Figure 5.2: Relative filter energy storage requirement vs. harmonic frequency

In order to calculate the value of E_{filter}, the peak power of each load frequency component must be known. As the DC link capacitor is the energy storing component in this case, the load power is that drawn by the DC/DC converter as indicated in Figure 5.3.

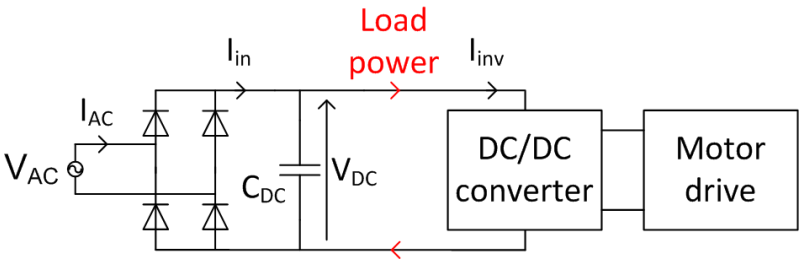

Figure 5.3: Load power measurement point used for the calculation of the minimum filter energy storage

The load power waveform was obtained from the zero capacitance motor drive simulation used in section 4.3. A Fourier Transform was then carried out to reveal the load power frequency spectrum as can be seen in Figure 5.4. As expected, the majority of the load power flow is at the fundamental motor drive switching frequency (3kHz) and harmonics thereof.

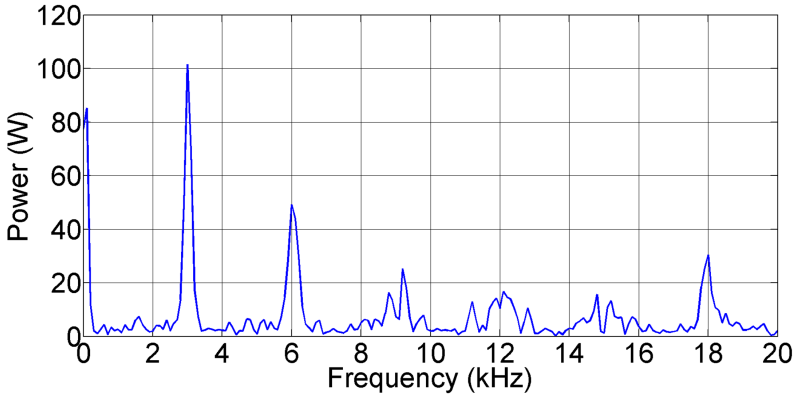

Figure 5.4: Load power spectrum for the reduced capacitance power supply and motor drive system

To evaluate the minimum energy storage requirement for each frequency component, Equation 5.3 was solved for each data point in Figure 5.4, substituting A and f for the power and frequency values respectively. The resulting filter energy spectrum is

shown in Figure 5.5. It can be seen that due to the inverse energy/frequency relationship, the higher frequency components which form a significant portion of the load power do not require a significant amount of filter energy storage. Conversely, for frequency components approaching zero (DC), the energy storage requirement tends to infinity.

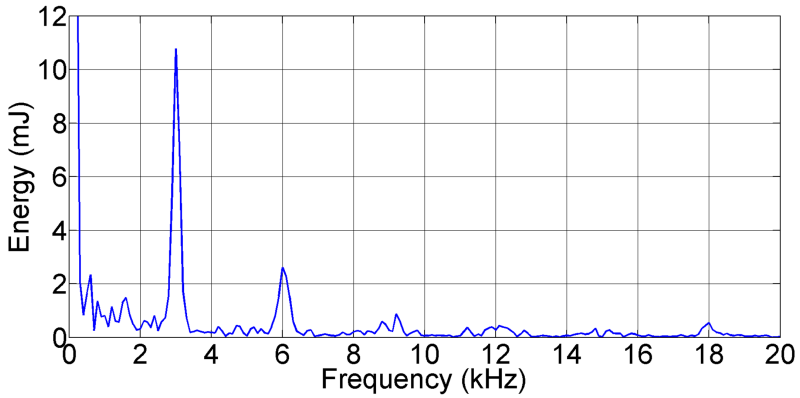

Figure 5.5: Filter energy storage requirement for each component of the load power spectrum in Figure 5.4

The motor conduction angle modulation system (see Section 4.3.1) has been shown to sufficiently reduce the low frequency (0-2kHz) components of the load power, such that they do not require further attenuation. It was therefore not necessary to account for these components when calculating the total energy storage requirement. Given that the full spectrum of load frequency components can exist simultaneously, the filter must be capable of storing their net energy. In the range of 2kHz to 20kHz this gives a total energy storage requirement of 65.9mJ (the sum of the y-axis values in Figure 5.5).

As discussed in Section 2.1.5, the energy utilisation of a passive filter is inversely proportional to its attenuation. A standard DC link capacitor is an excellent example of this; in order to produce a smooth DC link voltage, the ripple on the DC link capacitor must be very small. A small change in the capacitor's voltage subsequently means a small change in its stored energy and therefore poor utilisation:

$$\Delta E_c = \frac{1}{2}C(V_2^2 - V_1^2) \tag{5.4}$$

For example, the simulation model in Section 4.4 using a 470uF DC link capacitor resulted in a mean DC link voltage of 321V with 20V of ripple. This meant that only 12.5% of the energy storage capacity was used in filtering the 100Hz ripple from the mains. It is clear that passive harmonic filtering is not suitable for a reduced capacitance converter. In order to achieve high attenuation with minimal energy storage an active control system is required.

5.2 Active Filter Hardware Design

Having concluded that an active filtering approach was necessary, the next step was to research the hardware and control options. As discussed in Section 2.3.2, a boost converter front end is well suited to an application such as this due to its grounded/low side switch, input side inductor, simple control and low cost. Furthermore, the provision for continuous conduction mode operation reduces input current distortion and EMI. Assuming the DC link voltage is greater than the input voltage at all times, complete control over the input current shape can be maintained by modulating a single active switch.

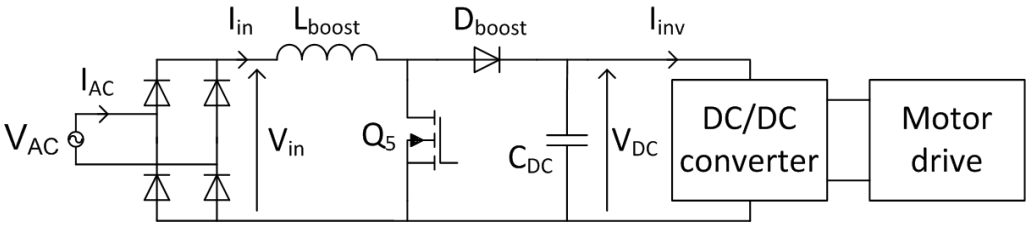

Figure 5.6: Boost converter front-end for the reduced capacitance power supply

Due to the reduced capacitance design it was necessary to adapt the standard rules and formulae to calculate the component specifications. In this case the DC link capacitor size can be calculated based on the harmonic energy storage requirement in Section 5.1. The theoretical minimum energy storage that could be used for harmonic cancellation is 65.9mJ. As a capacitor is used as the storage medium, this means the voltage ripple will be 100%, causing the boost converter to lose control of

the input current when V_{in} exceeds V_{DC}. In practical terms, the minimum energy storage is reached when:

$$V_{DC} = \quad V_{in} + \frac{V_{ripple}}{2} \tag{5.5}$$

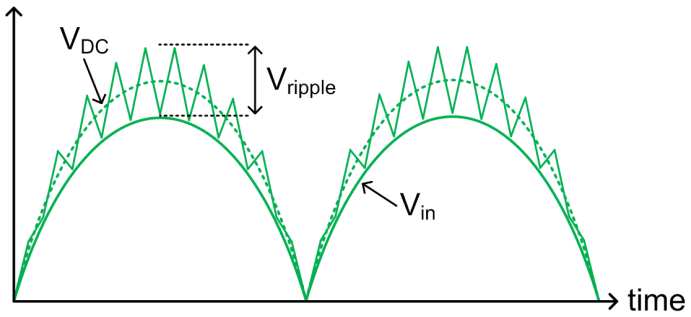

Figure 5.7: Maximum DC link voltage ripple allowing full control over the input current shape

The peak DC link voltage for the power supply was set at 500V to limit the stress on the components and to provide the correct output voltage without requiring a high transformer turns ratio (this is impractical with a planar design). Based on a peak input voltage of 325V ($230\sqrt{2}$) the maximum DC link ripple was therefore 175V. By rearranging Equation 5.4 the minimum capacitor size can be deduced, with $\Delta E_c =$ 65.9mJ, $V_2 = 500$V and $V_1 = 325$V:

$$C = \quad \frac{2\Delta E_c}{V_2^2 - V_1^2} \quad = \quad 913nF \tag{5.6}$$

Based on this calculation, a 1µF DC link capacitor was chosen as the closest available size. Equation 5.6 reiterates the fact that a large ripple voltage is necessary to make the best use of a given capacitor size.

At the initial design stage, the switching frequency was chosen to be 200kHz to give a reasonable balance between boost inductor size and efficiency. This gave a starting point for the selection of the remaining components, but was intended to

be flexible depending on the control system design. Similarly, the choice of input current ripple remained open, initially set to the common value of 20% of the peak line current [46]. Based on the results in Table 4.6, when the power supply is operating at full output power (200W), the input power will be 260W assuming the same efficiency of 76.9%. At $230V_{RMS}$ this gives a peak input current of 1.53A at unity power factor, and therefore a ripple current of 300mA.

Equation 5.7 [46] gives the required inductance based on a peak input voltage of 325V, DC link voltage of 413V, duty cycle D of 27%, switching frequency of 200kHz and ripple current of 300mA:

$$L_{boost} = \frac{\hat{V_{in}}.D}{f.I_{ripple}} = 1.46mH \tag{5.7}$$

Where

$$D = \frac{V_{DC} - V_{in}}{V_{DC}} = 27\% \tag{5.8}$$

Having calculated the key parameters it was necessary to select an appropriate boost diode and MOSFET. Given the switching frequency and current requirements a 600V/5A ultrafast diode (BYV25F-600) was chosen which had a short reverse recovery time (17.5ns) to maintain a high efficiency. As the boost MOSFET would be subjected to very similar operating conditions as the inverter switches, an identical part (IPP65R420) was selected.

5.3 Active Filter Control System Design

As identified in Section 2.3.2, conventional multiplier-based APFC control is not suitable for a reduced capacitance converter. The conventional approach aims to balance the input and output power flow by keeping the DC link voltage constant. The voltage control loop has to be very slow to avoid asynchronous modulation of the input current shape and hence distortion. To compensate for this slow response, a large DC link capacitor is required to stabilise the DC link voltage.

By referring to Figure 5.7, it can be seen that for a reduced capacitance converter, extracting a DC link voltage error signal is virtually impossible given the large ripple

at both 100Hz and 3kHz. It would be necessary to use a 10Hz low pass filter to bring the ripple under 5%, making the control response time much slower than the maximum rate of change of the DC link voltage. The possibility of using a dynamic reference voltage was considered, making the target a rectified sinusoid of fixed amplitude. In this case it would only be necessary to remove the 3.1kHz ripple, but the problem still exists in that the DC link voltage can change much faster than the controller can react. If the DC link voltage were to drop below the input voltage there would be a long delay before this was detected, causing loss of input current control.

A range of open-loop and waveform modification techniques were presented in Section 2.3.2 which avoid the issue of DC link voltage ripple, but none were found to satisfy the requirements of low capacitance, low cost and low current distortion. However, a particularly important observation was the way in which the Antiwave approach [70] directly targeted the load frequency harmonics and allowed the load itself to regulate the power flow. Due to this it was only necessary to keep the DC link voltage within a fixed range rather than having constant regulation. Furthermore, as the motor drive produced minimal low frequency distortion of the input current, this frequency range could be ignored by the APFC control system. These two observations formed the starting point for an APFC control system suitable for a reduced capacitance converter, but which also worked without the load feedback of the Antiwave controller.

5.3.1 Fixed Reference APFC

In a conventional APFC control system (Figure 5.8), the DC link voltage error signal V_{ea} is used to control the amplitude of the reference current and therefore input power. However, for the power system used in this research, the load power is fixed and self regulating, making it possible to operate without voltage error feedback. Instead of deriving the reference current shape directly from the input voltage, a fixed lookup table can be used which prevents the input power from being affected by changes in the RMS input voltage, and hence the feedforward V_{ff} signal is also unnecessary. The use of a lookup table does however require the use of a zero crossing detector to synchronise the reference current to the mains voltage.

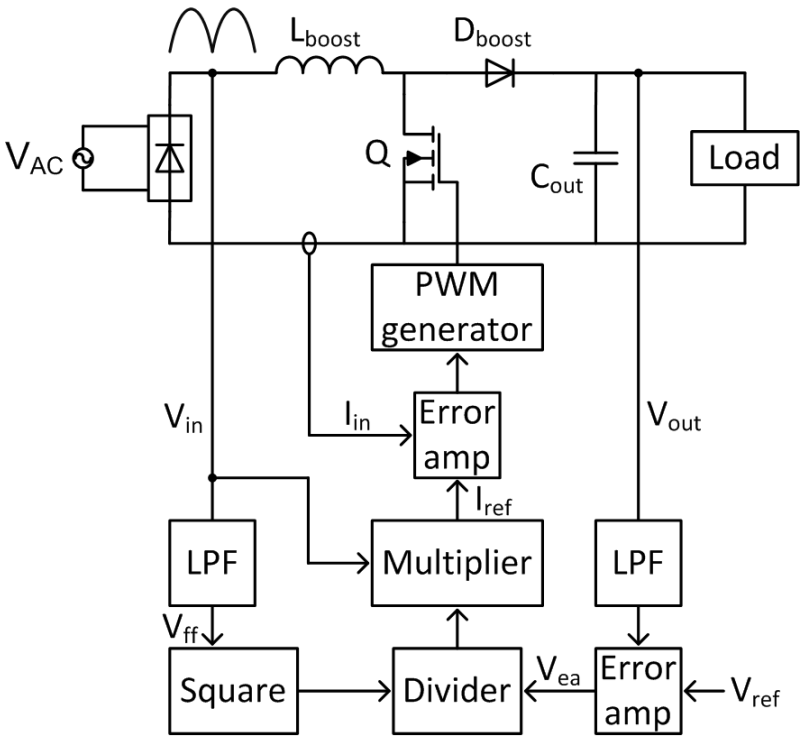

Figure 5.8: Hardware and control for a conventional boost APFC system

A model of the fixed reference APFC control system and the boost converter hardware was added in to the full system simulation as shown in Figure 5.9. For simplicity, the current error amplifier was set up as a hysteresis controller with a 300mA band as per the inductor ripple current calculation. This meant that Q_5 was on when I_{ref} exceeded I_{DC} + 150mA and off when I_{DC} exceeded I_{ref} + 150mA. The reference current lookup table was set as a half sinusoid with a peak value of 1.53A as determined previously. For simulation purposes it was not necessary to model the mains zero crossing detector as the lookup table could be synchronised with the input voltage directly.

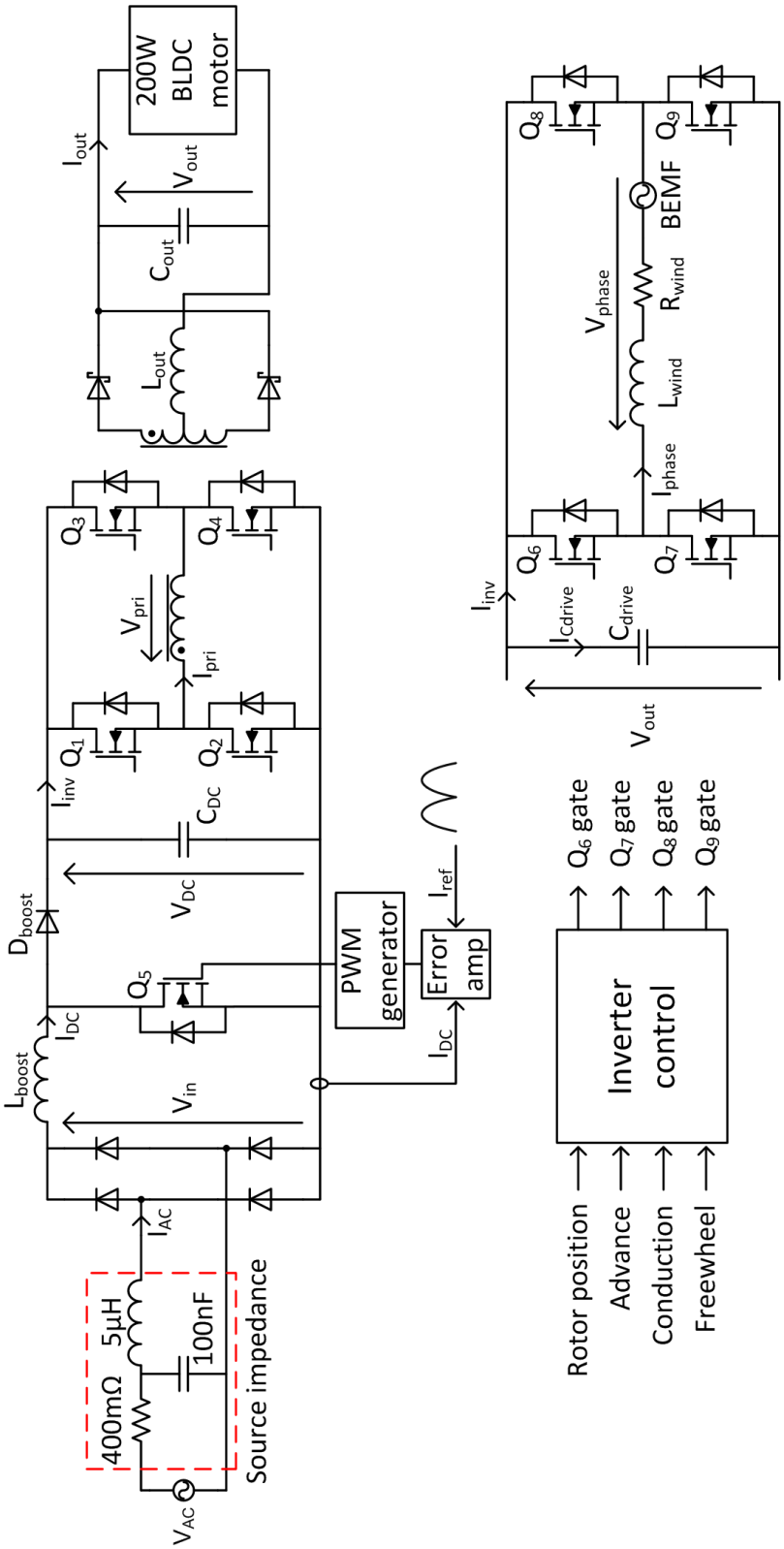

Figure 5.9: Full simulation model of the reduced capacitance power supply and fixed reference APFC system

Zero Capacitance Motor Drive Load

When compared with the unfiltered input current waveform in Figure 4.19 (b), a marked improvement can be seen in input current quality. Figure 5.10 and its respective Fourier transform (Figure 5.12) show a significant drop in the load harmonic amplitude leading to a power factor of 0.966 compared to 0.712 without APFC. Despite this, further improvements are required as load frequency harmonics are still clearly visible in the input current.

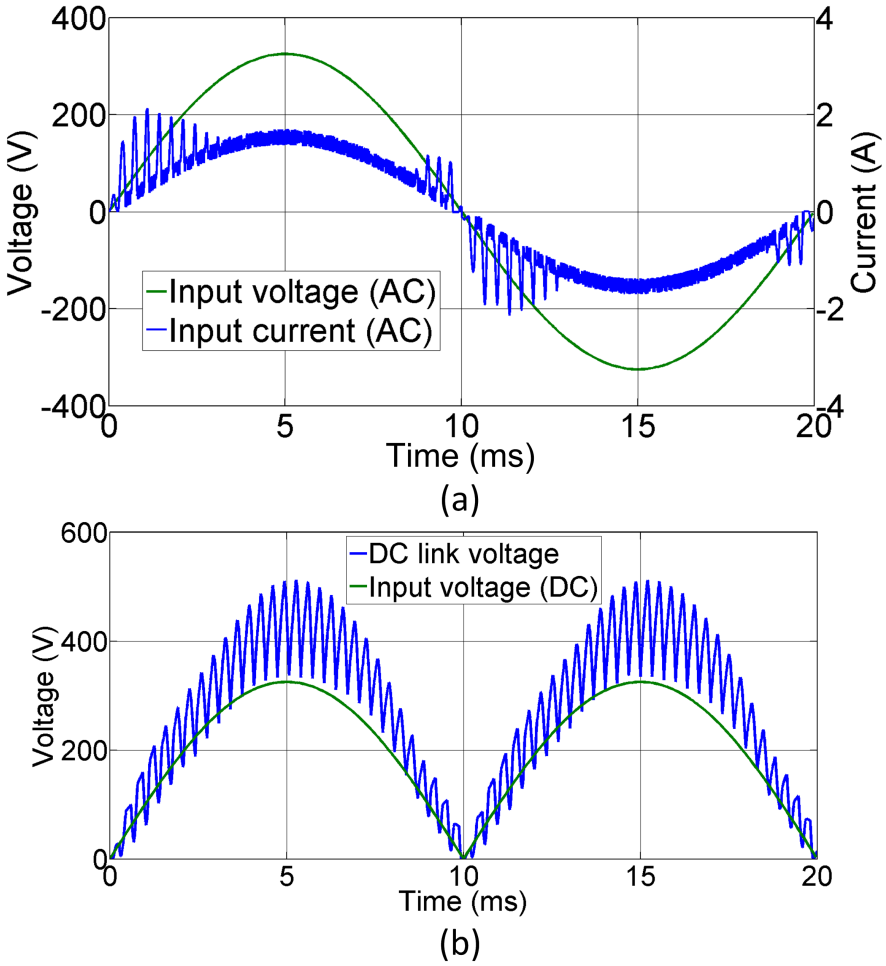

Figure 5.10: (a) AC input voltage and current (b) DC input voltage and DC link voltage for the fixed reference APFC system

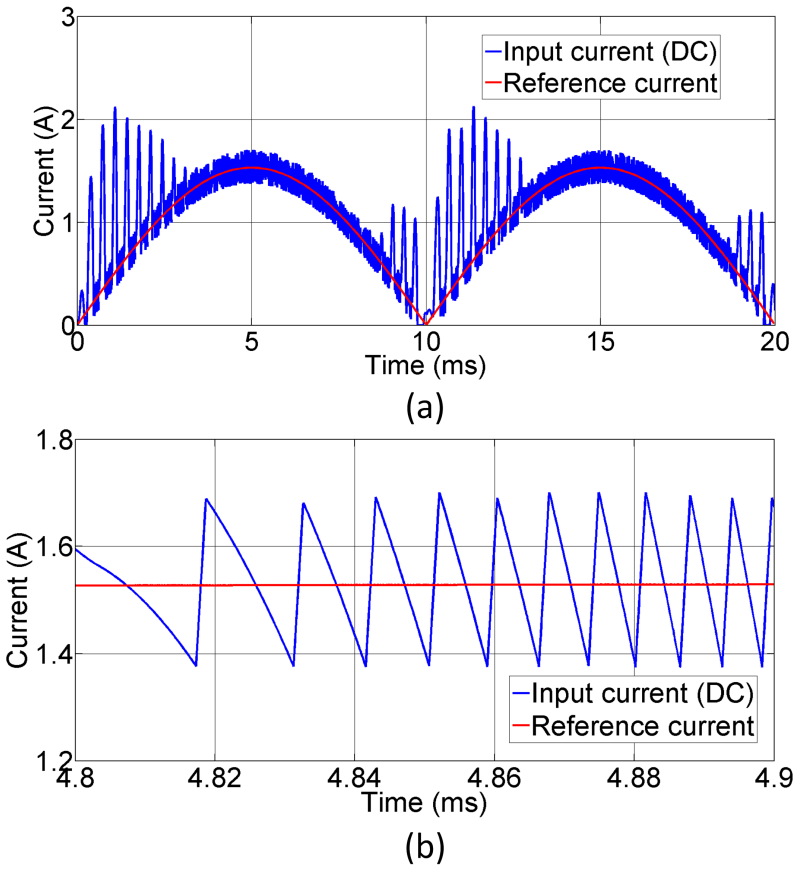

Figure 5.11: Boost inductor current and reference current (a) and zoomed view (b) for the fixed reference APFC system

As discussed previously, the boost converter can only retain control over the input current when V_{DC} is greater than V_{in}. By comparing Figure 5.10 (a) and (b) it can be seen that the input current deviates from the ideal sinusoidal shape when this condition is broken. The hysteresis controller forces the input current to track the reference current as shown in Figure 5.11. The variable frequency nature of this control approach is clear, with $\frac{di}{dt}$ dependent on the load and input voltage conditions. The wide switching frequency range of 0 - 320kHz complicates the EMI filter design and falls within the scope of the conducted EMI emissions standards discussed in Section 2.3.2. An average current mode control system [46] would reduce this problem, particularly if the switching frequency was kept below 150kHz. However, for the purposes of this project hysteresis control is used throughout due to its simpler implementation.

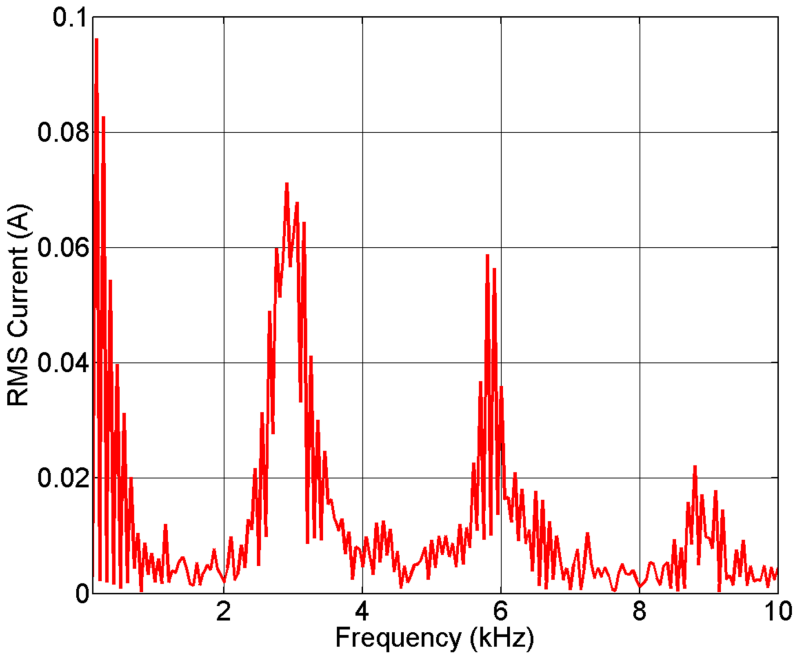

Figure 5.12: Input current harmonics for the fixed reference APFC system

Although a high power factor is achieved, the low frequency harmonic content of the input current still exceeds the scaled Class A limits as shown in Figure 5.13. Clearly the solution to this issue lies in keeping V_{DC} above V_{in}, but the DC link voltage limit of 500V means that increasing the boost duty is not an option. As shown in Figure 5.10 (b), the problem is restricted to the areas where the DC link voltage is relatively low, but the ripple is relatively high due to the load current demand. As discussed in Section 4.3, the constant power nature of the motor drive control system means that the load current demand is not proportional to the supply voltage, causing excessive ripple when the DC link voltage is low. The solution to this is to use the motor conduction angle modulation system discussed in Section 4.3.1 to linearise the load. The improvements resulting from this implementation can be seen in the next section (Figures 5.14 to 5.19).

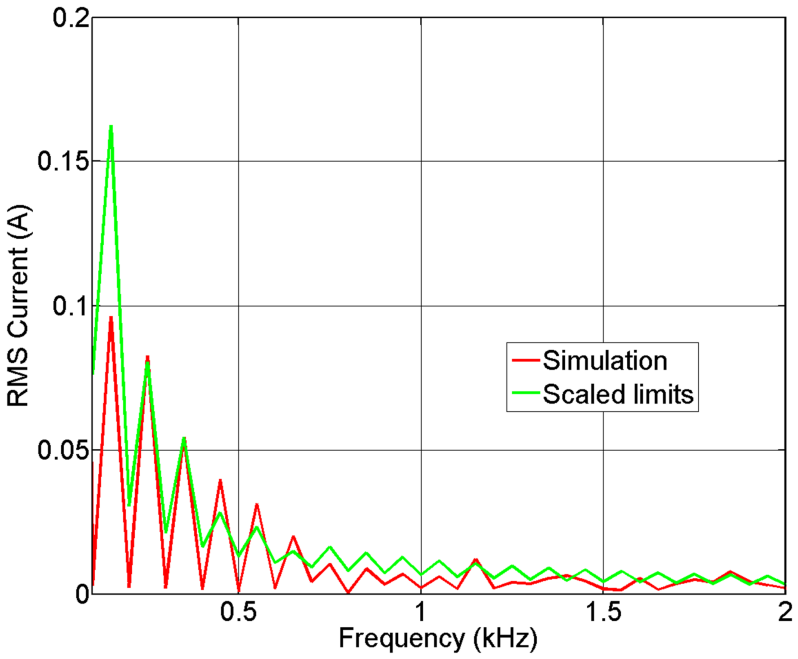

Figure 5.13: Input current harmonics shown with the scaled BS EN 61000-3-2 Class A limits

Parameter	Simulation
I_{AC}	$1.17A_{RMS}$
V_{AC}	$230V_{RMS}$
V_{DC}	$272V_{mean}$
V_{out}	$24.8V_{mean}$
I_{out}	$7.98A_{mean}$
P_{in}	260W
P_{out}	195W
Switching frequency	151kHz (mean)
Efficiency	75.0%
Power factor	0.966
I_{AC} THD	25%

Table 5.1: Key measurements for the reduced capacitance power supply and fixed reference APFC simulation

Zero Capacitance Motor Drive Load with Conduction Angle Modulation

Figure 5.14 shows a notable reduction in the harmonic content of the input current, as V_{in} only exceeds V_{DC} for very brief periods. The improvement is significant enough to pass the scaled harmonic limits (Figure 5.19) and produce an extremely

high power factor of 0.991. However, further improvements could still be made by refining the shape of the conduction angle modulation waveform. Figure 5.14 (b) shows a clear phase shift between the DC link voltage ripple pattern and the input voltage, causing intersections on the rising edge. If a corresponding phase shift was introduced to the conduction angle waveform this would likely eliminate the problem.

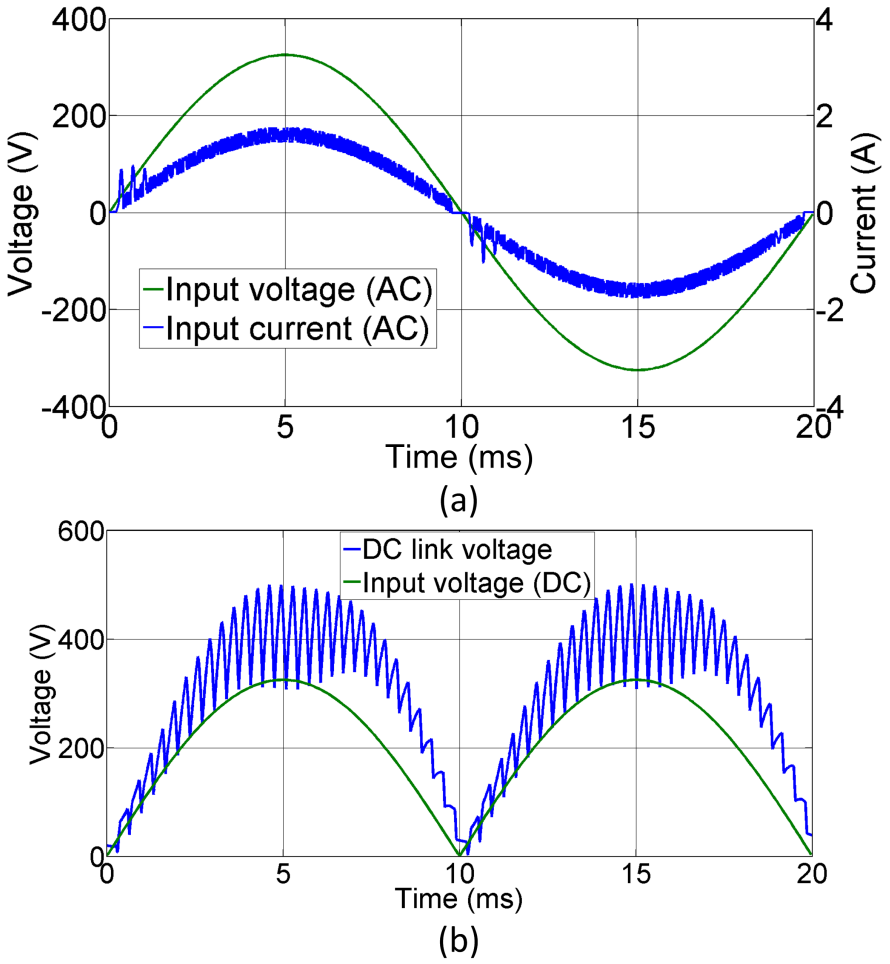

Figure 5.14: (a) AC input voltage and current and (b) DC input voltage and DC link voltage for the fixed reference APFC system with conduction angle modulation

By comparing Figure 5.14 and 5.15 the intended behaviour of the APFC system can be clearly seen. Without APFC (Figure 5.15) the input current contains very significant load-frequency harmonics, whereas the DC link voltage has virtually no load-frequency ripple at all. When APFC is used (Figure 5.14) the opposite is seen; virtually zero load-frequency input current harmonics and a very large DC link voltage ripple. Through active control, the DC link capacitor is forced to absorb the difference between the input and output power of the system, making far greater use of the energy storage available.

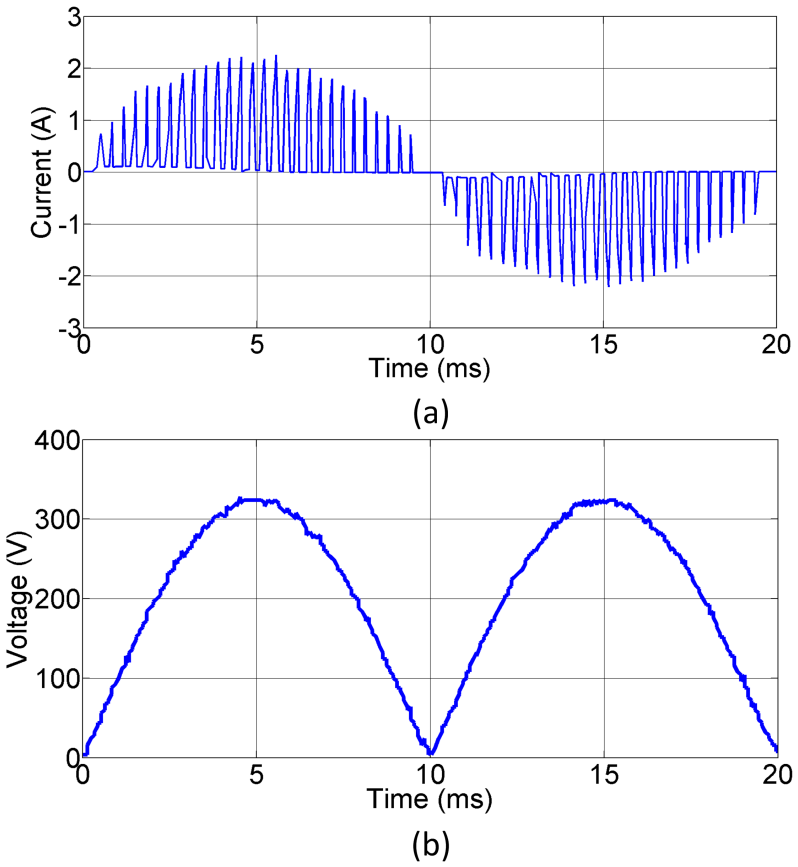

Figure 5.15: (a) AC input current and (b) DC link voltage for the reduced capacitance power system without APFC

Figure 5.16 (a) further demonstrates the improvement made through linearisation of the load, increasing the system's ability to maintain control of the input current. Having said this, a moment of instability can be seen in Figure 5.16 (b) where the input current temporarily exceeds the upper hysteresis band. At this point the load is drawing current directly from the input rather than the DC link capacitor, and hence control is temporarily lost.

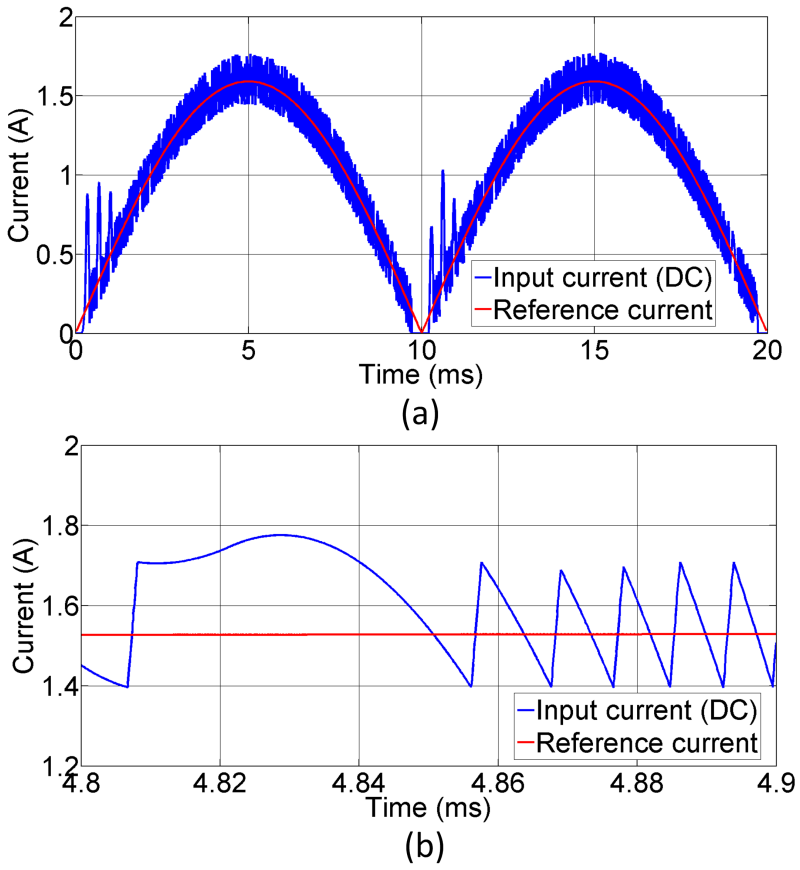

Figure 5.16: Boost inductor current and reference current (a) and zoomed view (b) for the fixed reference APFC system with conduction angle modulation

Figure 5.18 demonstrates the very high input current quality achievable when the fixed-reference APFC system is combined with conduction angle modulation. The same results are shown as in Figure 5.17, except that the fundamental 50Hz component has been included to demonstrate the relative size of the harmonics.

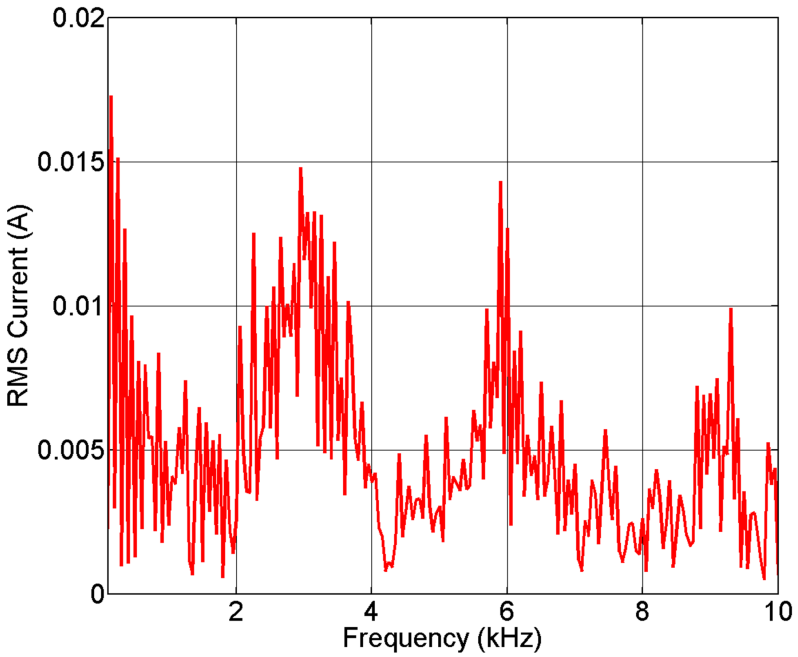

Figure 5.17: Input current harmonics for the fixed reference APFC system with conduction angle modulation

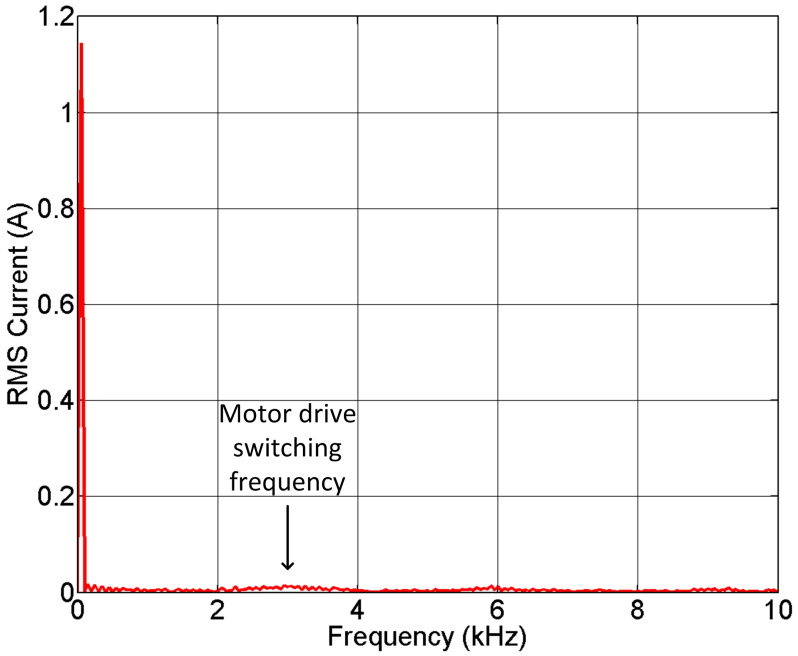

Figure 5.18: Repeated results from Figure 5.17 with the fundamental component included

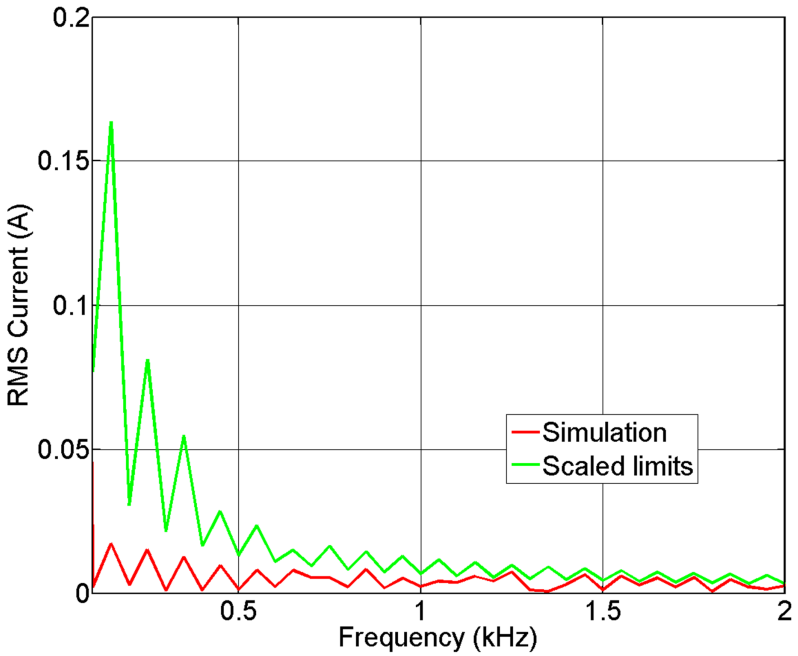

Figure 5.19: Input current harmonics shown with the scaled BS EN 61000-3-2 Class A limits

A downside of the conduction angle modulation system is that the power supply spends a larger proportion of the time unloaded, causing a small reduction in efficiency (75% to 73.3%). This happens because the average conduction angle is lower than for the standard motor drive, which means it draws current in shorter bursts and therefore presents a load to the power supply for less of the time. Furthermore, despite not affecting the peak DC link voltage, the mean is increased by 10%, leading to greater energy storage in the inverter/transformer parasitic capacitances. As discussed in detail in Section 4.5, these two factors lead to higher inverter switching losses.

Parameter	Simulation
I_{AC}	$1.15A_{RMS}$
V_{AC}	$230V_{RMS}$
V_{DC}	$298V_{mean}$
V_{out}	$24.3V_{mean}$
I_{out}	$7.49A_{mean}$
P_{in}	262W
P_{out}	192W
Switching frequency	132kHz (mean)
Efficiency	73.3%
Power factor	0.991
I_{AC} THD	7.2%

Table 5.2: Key measurements for reduced capacitance power supply and fixed reference APFC simulation with conduction angle modulation

A simple alternative to conduction angle modulation would be to increase the DC link capacitance. This would proportionally reduce the load frequency ripple voltage, and therefore the possibility of V_{in} exceeding V_{DC}. In comparison this is an undesirable option as it increases the size of the power supply, whereas conduction angle modulation only requires a control system change.

The input current and DC link voltage waveforms in Figure 5.20 demonstrate the key limitation of the fixed reference APFC system. After the 50% to 100% load step takes place, harmonics appear in the input current as the reference is too small. The open loop nature of the power control means that load changes such as this cannot be accommodated.

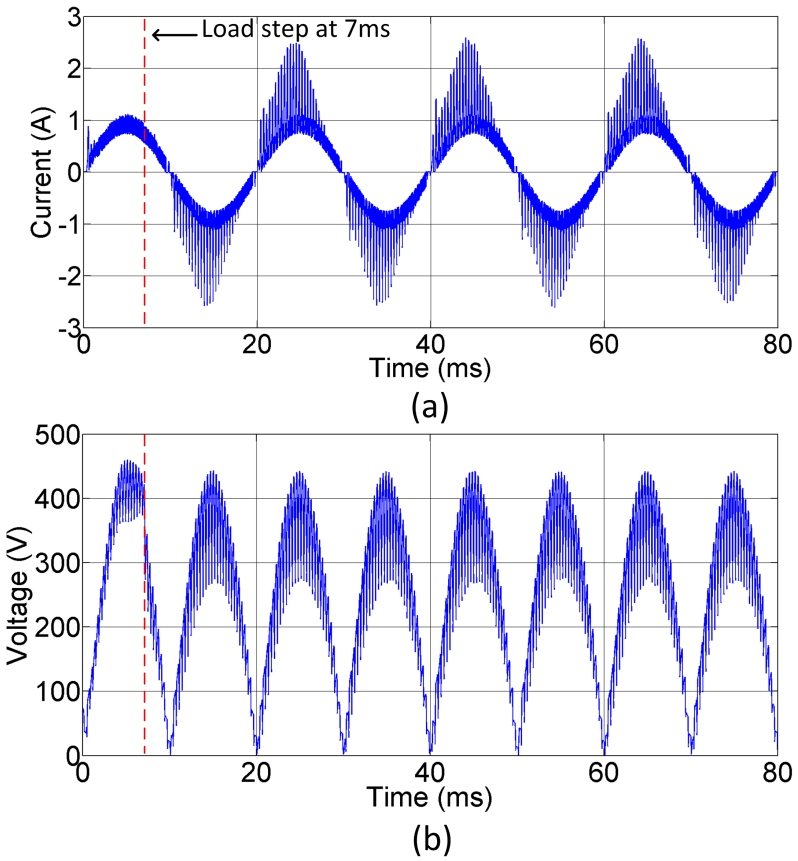

Figure 5.20: (a) Input current and (b) DC link voltage during a load step change from 50% to 100% - fixed reference APFC with conduction angle modulation

Conclusions from the Fixed Reference APFC Simulation

The results in this section have demonstrated that a very simple control system can be used to lower the input current harmonics of a reduced capacitance converter. This led to a significant improvement in power factor, increasing from 0.712 to 0.966 without conduction angle modulation. There are, however, a number of drawbacks which limit the use of this APFC system, many of which stem from having a fixed input current reference.

The first problem is that although the motor drive system is capable of regulating its power, there are situations where this is not possible. Given that the motor drive is intended for a compressor application, the air inlet can be blocked, creating a partial vacuum which reduces the load on the impeller/motor. Furthermore, when the system is started up the motor accelerates, during which time the load is constantly changing. If the reference current amplitude is not changed to reflect the new load power, the DC link voltage will very quickly become too large or too small. Where

the load is under-estimated, the current flow out of the DC link capacitor will exceed that of the input, causing it to discharge and the DC link voltage to drop below the input voltage. At this point the load frequency harmonics will begin to appear in the input current. Where the load is over-estimated, the input current will exceed the current flow out of the DC link capacitor causing it to (theoretically) charge to an infinite voltage. In reality this process will stop when the components become damaged due to over-voltage. For a known load change such as the user selectable power mode function it would be possible to compensate for this by adjusting the reference current amplitude.

The lack of feedback in the control system means that the load has to be accurately characterised in advance, making it more costly to implement in new/different applications. In some situations component and manufacturing tolerances could be enough to upset the control system unless each product is tuned individually. When generating the correct input current reference it is also necessary to know the system losses as well as the actual load power, as these contribute to the total power draw seen by the APFC system.

A further disadvantage of the fixed reference APFC approach is that it requires the use of a microcontroller, as the reference current is derived from a lookup table. Whilst this process is not complex, a reasonably high processor bandwidth is required to allow operation up to 350kHz, and such a part may be prohibitively expensive for this application. Due to the variable nature of the mains frequency it would also be necessary to adjust the frequency of the lookup table so that distortion does not occur. However, given that a relatively powerful processor is already required, compensating for this does not pose a particular problem.

The limitations of this approach make it unappealing for use in a practical application, and a more robust system is required which allows for variations in load power. The design of such a system forms the remainder of this chapter.

5.3.2 Filter-Based APFC

The work in this chapter has revealed that the main challenge is determining the correct scaling factor for the input current reference, and therefore input power to the boost converter. Regardless of whether the reference is derived from the input voltage or a lookup table, its amplitude must be correct to prevent over or under-charging of the DC link capacitor. As a result of this, it was concluded that control of the reference current amplitude was not reasonably possible without DC link voltage error detection. As discussed previously, this is also not a viable option due to the 100% DC link voltage ripple.

In light of this, an alternative approach was taken to removing the harmonics from the input current. It was observed that instead of subtracting a line frequency reference from the input current (Figure 5.21 (a)), a line frequency notch filter could be used to remove the fundamental component of the input current leaving behind only the harmonics (Figure 5.21 (b)). By using the latter, a reference current is not required yet the same error signal is produced. In this case the control system only sees the non-fundamental component, the target for which is always zero and therefore does not need to be scaled with load power. Having generated the current error signal the remainder of the control system can be the same, using either hysteresis or average current mode regulation.

A system operating in this manner offers no control over the fundamental amplitude of the input current, but nor does it need to. The motor drive load itself regulates the current draw to compensate for changes in DC link voltage, keeping the normal operating power constant. However, unlike the fixed reference current approach, deviations from the standard power draw can also be accommodated. In a similar vein, the filter based control system has no control over the phase between the input current and voltage, but again the load takes care of this issue. The voltage follower nature of the motor drive means that the load current inherently tracks the DC link voltage (and therefore the input voltage), ensuring minimal phase displacement.

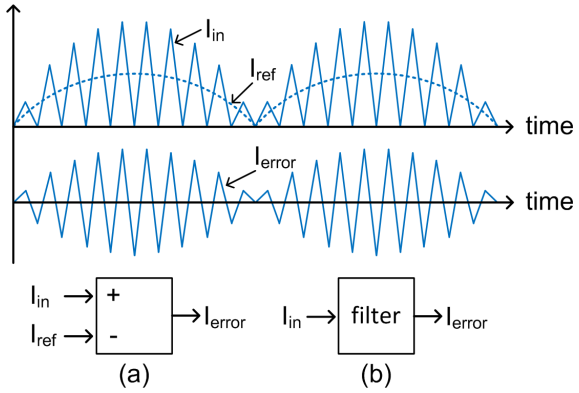

Figure 5.21: Generation of an input current error signal via (a) subtraction of a reference and (b) notch filtering

In order to extract the true harmonic spectrum it is necessary to measure the AC input current on the supply side of the bridge rectifier as shown in Figure 5.22. This is because the process of rectification introduces artificial harmonics to a DC-side measurement which are not actually present in the input current (see Figure 5.23). If the APFC system attempted to correct these artificial harmonics, it would instead generate new harmonics in the input current, which is clearly counter-productive.

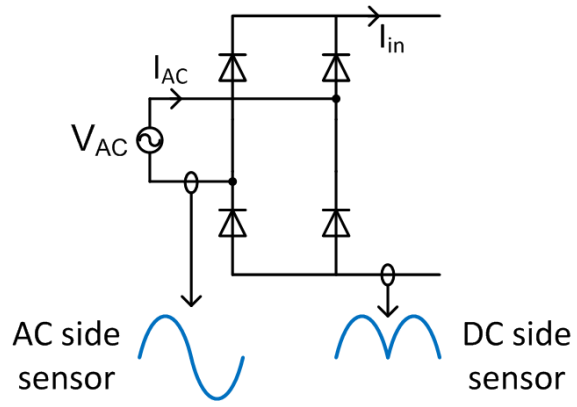

Figure 5.22: AC-side and DC-side current sensors with their respective waveforms

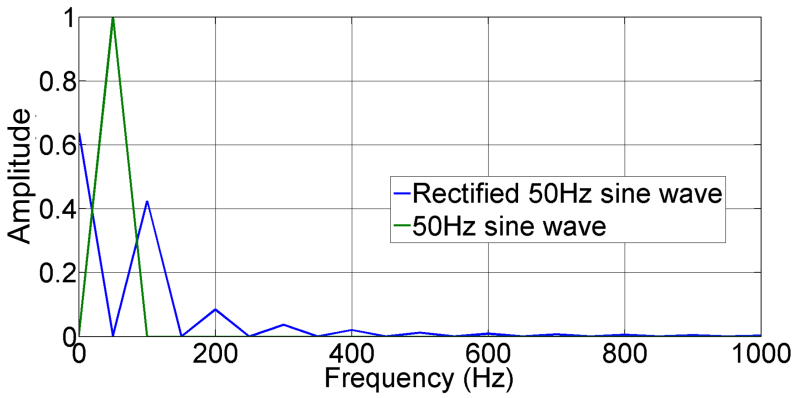

Figure 5.23: Fourier transforms of a 50Hz sine wave and a rectified 50Hz sine wave both of amplitude 1 unit

A minor complication arising from the use of an AC-side current sensor is that the error signal is inverted over each half cycle of the mains. As shown in Figure 5.24, when the input current is negative the hysteresis bands must be inverted to prevent positive feedback occurring. This requires the control system to know the phase of the input current, which can be achieved using a very simple comparator based circuit as explained in Section 6.3.1.

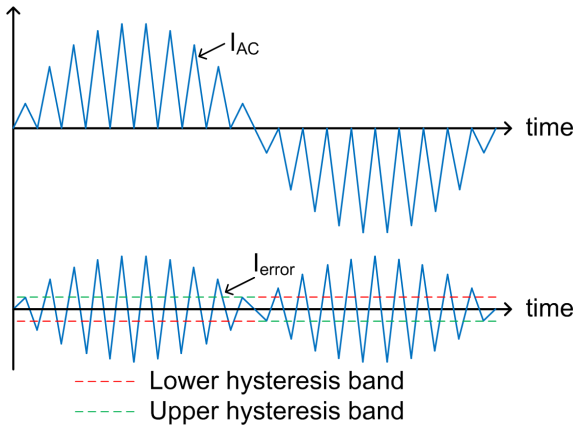

Figure 5.24: Hysteresis band inversion to prevent positive feedback

The control system model for the filter based APFC simulation is shown in Figure 5.25, with the power supply and motor drive models unchanged (Figure 5.9). The hysteresis controller has the same 300mA band as before, with the output inverted when the input current is in the negative phase.

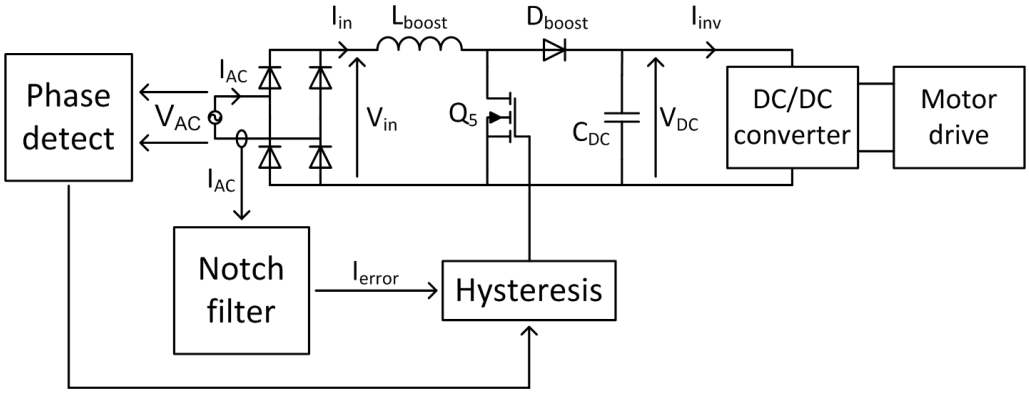

Figure 5.25: Control system model for the filter-based APFC simulation

The notch filter attenuation is important as it controls the level of harmonic rejection in a similar manner to the amplitude of the reference current in the multiplier based APFC approach. A low level of attenuation means that the filter output (I_{error}) will still have a significant 50Hz component, reducing the amplitude of the harmonics seen by the hysteresis controller. This effect is shown in Figure 5.26, with (a) showing low attenuation and (b) showing high attenuation. When the attenuation is low the harmonics barely exceed the lower hysteresis band, causing minimal correction to be applied by the boost converter, thus allowing some of the harmonic content to remain. When the attenuation is high, a larger error is seen resulting in a greater corrective action and therefore less input current harmonics. The notch filter attenuation can therefore be treated similarly to a proportional error feedback coefficient.

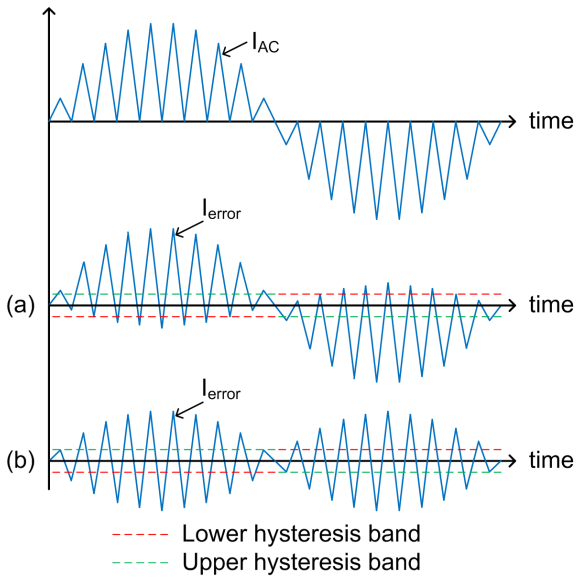

Figure 5.26: Effect of notch filter attenuation on error current waveform seen by hysteresis controller (a) low attenuation (b) high attenuation

A secondary effect of the filter attenuation level is its control over the DC link voltage. As previously explained, high attenuation means greater harmonic cancellation, which requires increased boosting of the DC link voltage. With a high DC link voltage, a large ripple can occur before the boost converter reaches its stability limit of $V_{in} = V_{DC}$. The ability of the system to remain stable with a large DC link ripple voltage subsequently means that large changes in capacitor energy can be permitted. If a large amount of energy can be absorbed by the capacitor, large harmonics can be removed from the input current. It can therefore be seen that obtaining the minimum input current distortion requires the DC link voltage to be as high as possible. For any practical power system, a finite DC link voltage limit will exist, determined by the component ratings, layout as well as any safety considerations.

Before generating a full set of simulation results, it was first necessary to determine the optimum notch filter attenuation setting. Figure 5.27 shows the relationship between filter attenuation, peak DC link voltage and input current distortion as determined by the power system system simulation (conduction angle modulation was not used in this case). As the reduced capacitance power supply was designed with a DC link voltage limit of 500V, the optimum notch filter attenuation was therefore 18dB, leading to a projected input current THD of 23%.

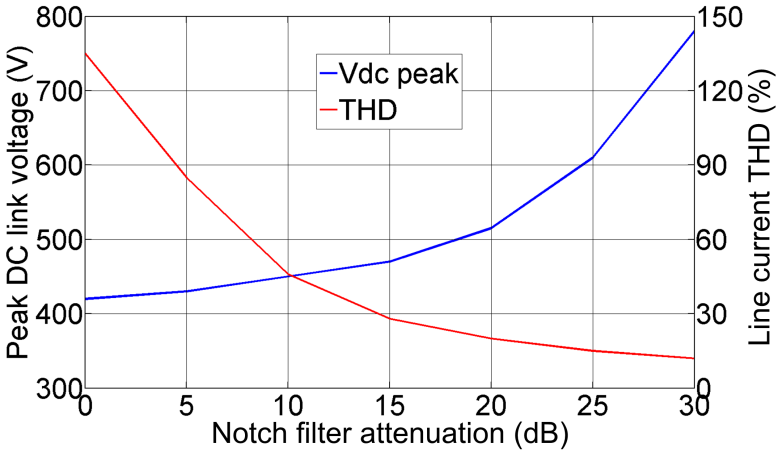

Figure 5.27: Simulation results showing the relationship between notch filter attenuation, peak DC link voltage and input current distortion

A notable observation from Figure 5.27 is that the peak DC link voltage is considerably higher than the peak supply voltage of 325V, even with the filter bypassed altogether (0dB attenuation). The reason for this is despite the boost converter being inactive, the boost inductor is still present in the circuit and thus combines with the DC link capacitor to form a passive lowpass filter. The impedance of the boost inductor limits the rate at which the DC link capacitor can be charged, subsequently causing a ripple in its voltage. The presence of this passive lowpass filter, however, does little to attenuate the 3kHz motor frequency harmonics as its cutoff frequency is 4165Hz. A second observation is the exponential relationship between notch filter attenuation and DC link voltage. The reason for this is simple; the apparently linear x-axis in Figure 5.27 is in fact logarithmic due to the use of decibels as the measure of attenuation.

A Bode plot of the optimum notch filter response (-18dB) is shown in Figure 5.28. This was used for all of the simulation results in the next section of this chapter.

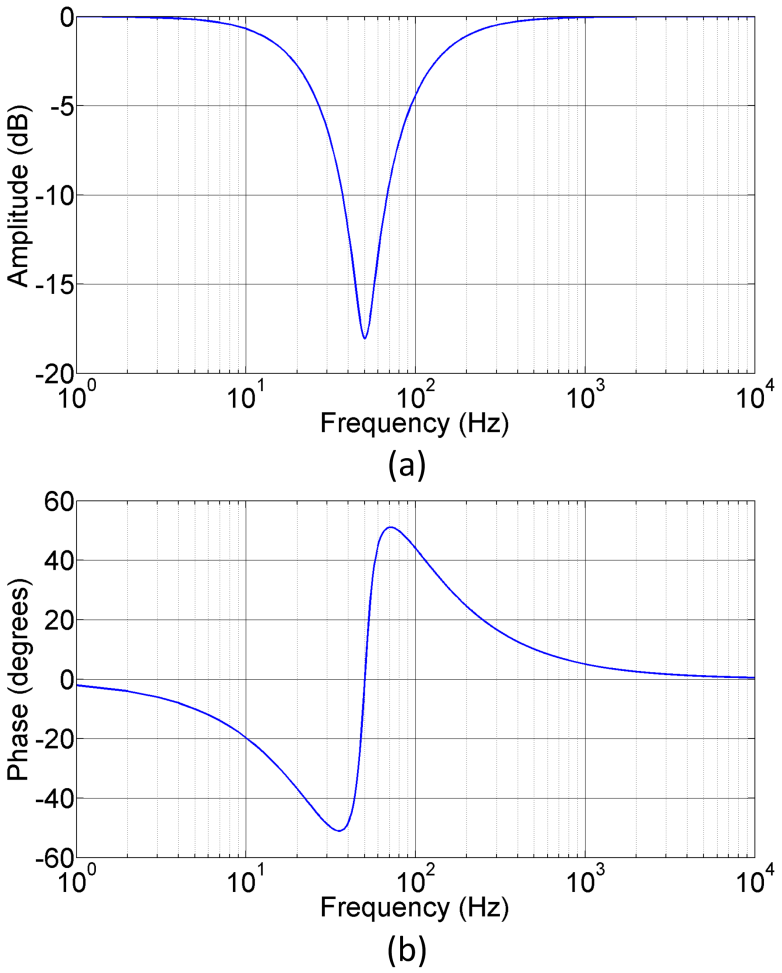

Figure 5.28: Bode plot for the -18dB 50Hz notch filter

Simulation Results

Having changed the boost converter control system as per Figure 5.25, the full system model was simulated to analyse the performance of the filter-based APFC. As can be seen in Figures 5.29 to 5.36 and Table 5.3, the results are virtually identical to those of the fixed reference approach.

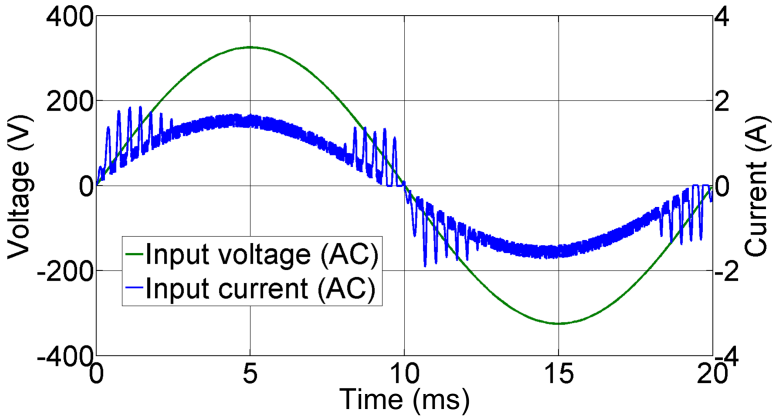

Figure 5.29: AC input voltage and current for the reduced capacitance power supply and motor drive simulation with filter-based APFC

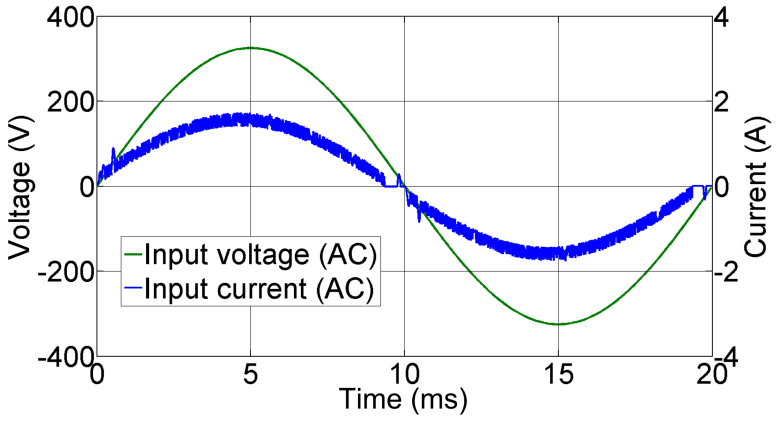

Figure 5.30: AC input voltage and current for the reduced capacitance power supply and motor drive simulation with filter-based APFC and conduction angle modulation

One notable difference is that a phase displacement can be seen between the input current and voltage in Figure 5.29/5.30. As discussed previously, the filter-based APFC system only removes harmonics from the input current and leaves control of the phase displacement to the load. In this case the current leads the voltage by 6 degrees, giving rise to a leading displacement power factor (PF_D) of 0.991. As the effect is so small it does not pose a particular problem, but if necessary the phase displacement could be reduced through refinement of the motor conduction angle modulation. This issue highlights a minor disadvantage compared to the multiplier-based approach, where the the phase of the input current is locked to the input voltage.

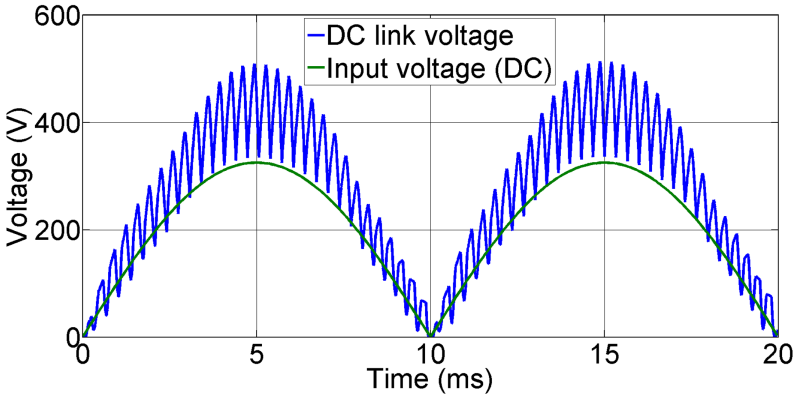

Figure 5.31: DC input voltage and DC link voltage for the reduced capacitance power supply and motor drive simulation with filter-based APFC

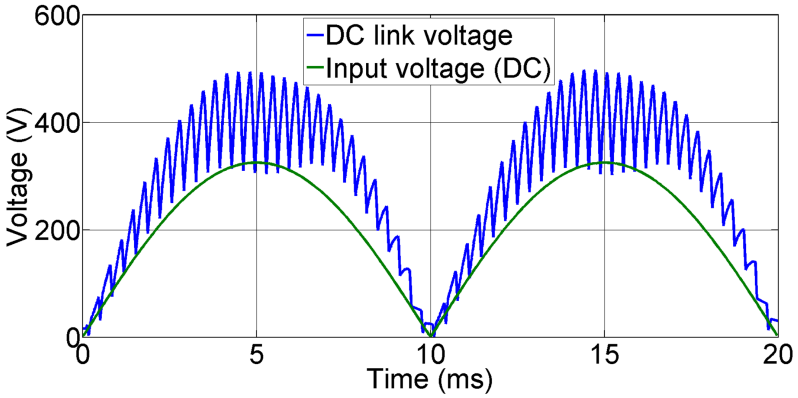

Figure 5.32: DC input voltage and DC link voltage for the reduced capacitance power supply and motor drive simulation with filter-based APFC and conduction angle modulation

The Fourier transforms in Figure 5.33 to 5.36 demonstrate the very low THD achievable by the filter-based APFC system; 24% without conduction angle modulation and 5.8% if this is included. These results are closely comparable to those of the fixed-reference APFC system, which achieved 25% THD without conduction angle modulation and 7.2% with conduction angle modulation. In both cases the scaled EN61000-3-2 limits are met when conduction angle modulation is used.

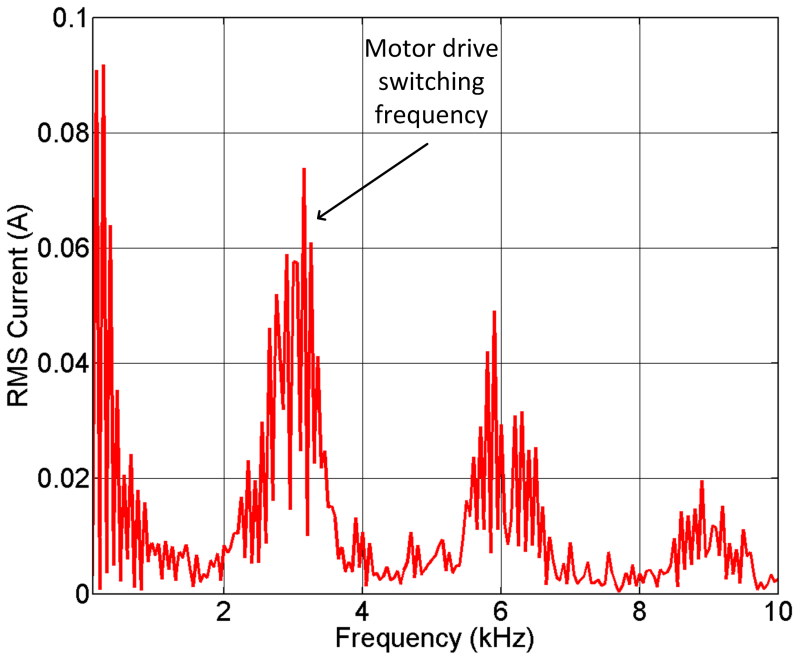

Figure 5.33: Input current harmonics for the reduced capacitance power supply and motor drive simulation with filter-based APFC

As with the Fourier transforms in the previous section, it is necessary to consider the relative amplitude of the harmonic components. For the results in Figure 5.34, all the harmonics have an amplitude less than 2% of the fundamental, demonstrating the high performance of the APFC control system.

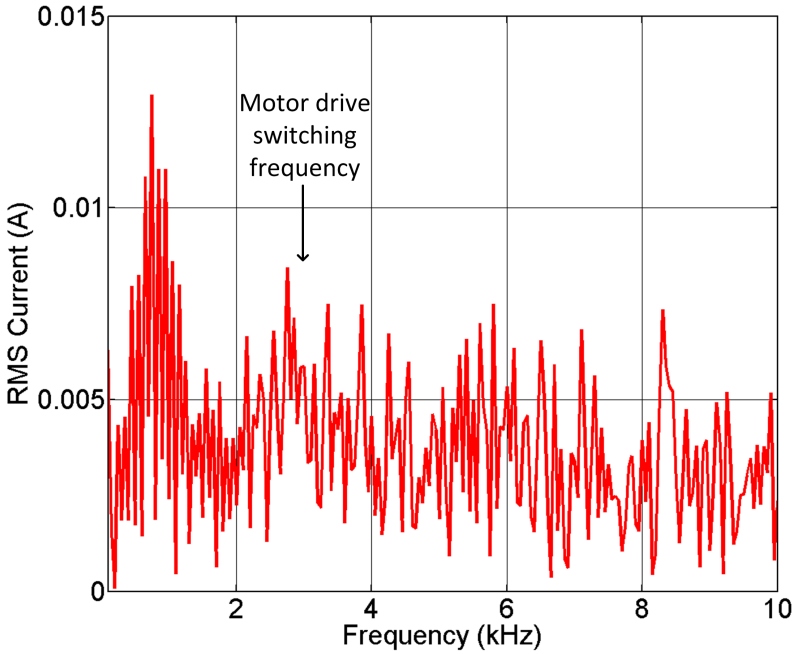

Figure 5.34: Input current harmonics for the reduced capacitance power supply and motor drive simulation with filter-based APFC and conduction angle modulation

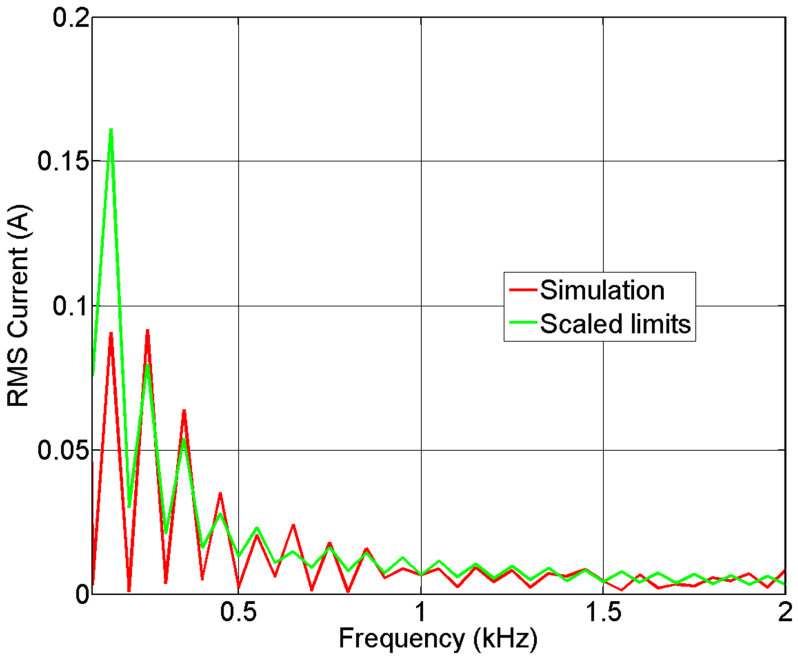

Figure 5.35: Input current harmonics for the reduced capacitance power supply and motor drive simulation with filter-based APFC - shown against scaled BS EN 61000-3-2 Class A limits

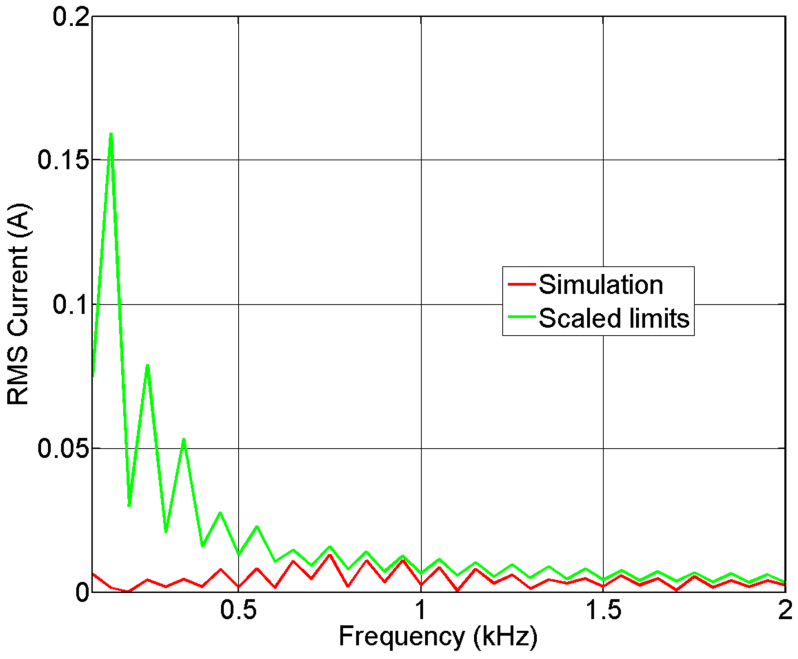

Figure 5.36: Input current harmonics for the reduced capacitance power supply and motor drive simulation with filter-based APFC and conduction angle modulation - shown against scaled BS EN 61000-3-2 Class A limits

Shown in Table 5.3 are further results demonstrating the similar performance between the fixed reference and filter-based APFC control systems. Despite the small reduction in harmonic content (see THD figures), the overall power factor is still slightly lower for the filter-based approach due to the phase displacement between the input current and voltage.

Parameter	No conduction modulation	With conduction modulation
I_{AC}	$1.17A_{RMS}$	$1.12A_{RMS}$
V_{AC}	$230V_{RMS}$	$230V_{RMS}$
V_{DC}	$269V_{mean}$	$288V_{mean}$
V_{out}	$23.0V_{mean}$	$23.3V_{mean}$
I_{out}	$8.41A_{mean}$	$7.42A_{mean}$
P_{in}	258W	255W
P_{out}	193W	182W
Switching frequency	108kHz (mean)	126kHz (mean)
Efficiency	74.8%	71.4%
Power factor	0.959	0.989
I_{AC} THD	24.2%	5.8%

Table 5.3: Key measurements for the reduced capacitance power supply and motor drive simulation with filter-based APFC

Shown in Figure 5.37 is the system response to a load step change from 50% to 100%. It can be seen that initially the larger harmonics appear in the input current, but as the system reacts to cancel them out the DC link voltage is increased, restoring stability (i.e. $V_{DC} > V_{in}$). The reaction time is determined primarily by the notch filter response, a more detailed analysis of which can be found later on in Section 7.5. When compared with the results in Figure 5.20, the load response benefit of the filter-based approach is clear. Furthermore, an instantaneous load step such as this is much more severe than any which could be encountered in practice, meaning that less harmonics would be seen after the power increase. For the real motor drive, acceleration is the worst case scenario where the same load change would take approximately 100ms. It was not feasible to model the full dynamic behaviour of the motor drive, so unfortunately this could not be simulated. However, the hardware test results in Chapter 7 include input current and DC link voltage waveforms during acceleration.

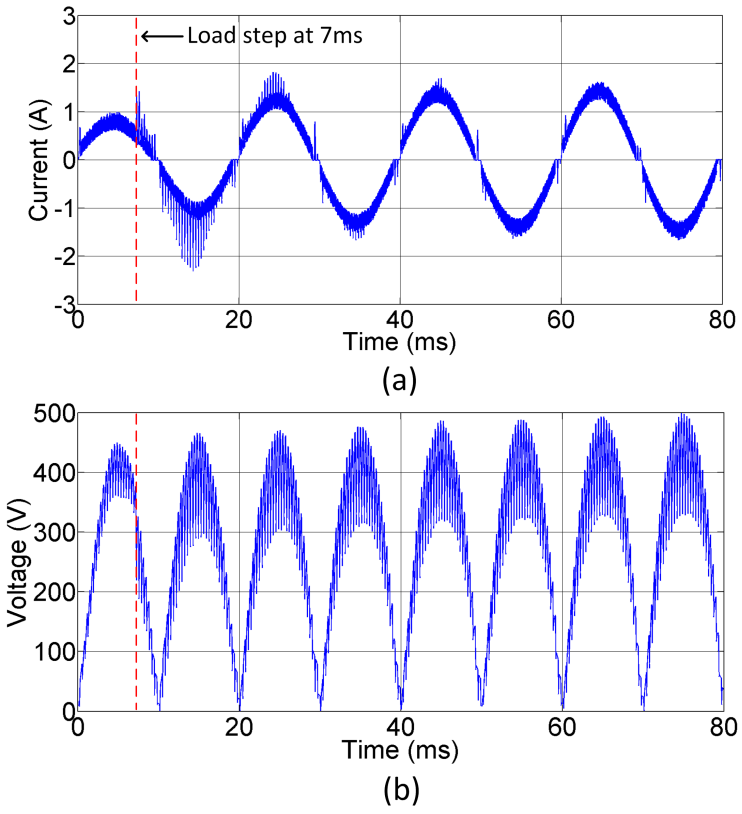

Figure 5.37: (a) Input current and (b) DC link voltage during a load step change from 50% to 100% - filter based APFC with conduction angle modulation

5.4 Conclusion

This chapter began by presenting a critical analysis of filter energy storage requirements, noting that the minimum energy storage capacity is inversely proportional to the target harmonic frequency. Through the use of reduced DC link capacitance and a load optimised for harmonic performance, the lowest frequency component requiring attenuation is the load switching frequency. A method of calculating the total energy storage requirement was proposed based on the sum of load harmonic energies.

In line with findings from the literature review, conventional multiplier-based APFC was deemed unsuitable due to its very low voltage control loop bandwidth. When combined with reduced DC link capacitance, the problem is exacerbated as the DC link voltage can change more quickly. A simple fixed-reference current controller was shown to greatly reduce the input current harmonics, but this is only viable where the load power and input voltage are also fixed. As there are very few scenarios

where these conditions can be relied upon, such a system is not particularly useful. As an alternative to using voltage error feedback, the reference current could instead be modulated based on estimated load power. However, this requires accurate characterisation of the load and more feedback, leading to reduced flexibility and increased complexity. Furthermore, due to the look up table this approach cannot be implemented using analogue hardware. For these reasons it was necessary to carry out further research into improved control system approaches.

It was recognised that the key challenge lay in controlling the reference current amplitude to maintain balanced input and output power. This required knowledge of the DC link voltage error, a very challenging prospect due to the ripple on the DC link voltage. A novel solution to this was proposed using a notch filter to extract the harmonic components of the input current signal (i.e. the error current). The use of this technique allowed a constant relative level of harmonic attenuation with varying load power, whilst removing the need for DC link voltage error feedback. To simplify the filter design, an AC input current sensor was used instead of the conventional DC current sensor. This removed the additional harmonics produced by the rectification process, allowing the use of a single notch filter to remove the fundamental component from the current sensor signal.

The simulation results demonstrated that the notch filter based APFC control system could also produce a low input current distortion. Furthermore, this was coupled with the ability to compensate for varying load power as well as removing the need for a microcontroller. Based on the promising simulation results, the decision was made to design a simple and low cost hardware implementation of the filter-based control system; this forms the basis of the following chapter.

Chapter 6

APFC Hardware Design

6.1 Current Sensor Design

The first stage of the APFC hardware implementation was to develop an appropriate current sensor. From the simulation work in Section 5.3 it can be seen that a bandwidth of 0 - 350kHz is required with a current rating of at least 3A. In keeping with the fundamental principles of this work, minimal size and cost are also necessary for a viable design.

The fact that the current sensor needed to be on the AC side of the diode bridge meant that the output signal had to be isolated before being fed to the controller. The normal solution to this issue would be to use an isolated measurement system such as a current transformer or hall effect sensor. However, without using large and expensive laboratory grade instrumentation neither approach has the necessary bandwidth, with the former only sensing AC signals and the latter only working up to approximately 200kHz. Both approaches also suffer from relatively high cost. A shunt based sensor would have the necessary bandwidth, but is not isolated and therefore would not work without a costly additional power supply and signal isolation system.

A novel solution to this problem was developed as shown in Figure 6.1. A shunt based sensor is placed on the DC side of the diode bridge, allowing it to measure the rectified input current as with a multiplier based APFC system. A very low cost and wide bandwidth differential amplifier can be used which is also referenced to the DC side 0V rail, thus allowing it to be connected directly to the control system without any isolation issues. The output of the sensor is then modulated by the polarity of the input current, multiplying the signal by 1 when the input current

is positive and -1 when the input current is negative. This effectively reverses the rectification process, generating an output identical to that of an AC side sensor. As a polarity detector is already required for control of the hysteresis converter (see Section 5.3.2), very few additional parts are required for the current sensor system.

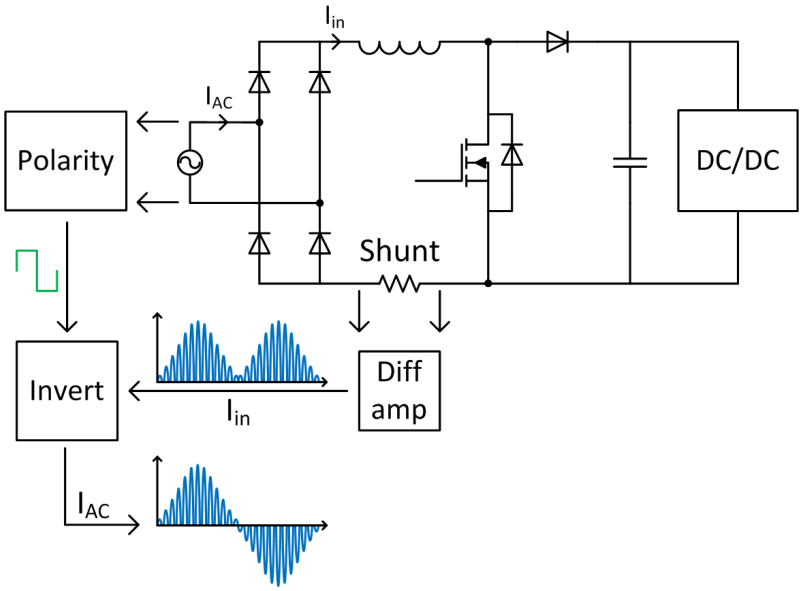

Figure 6.1: Reverse rectification DC to AC current sensing system

6.2 Analogue vs. Digital Implementation

For the remainder of the filter based control system, both analogue and digital methods were considered to perform the current sensor inversion, notch filtering and hysteresis functions shown in Figure 6.2. As the prototype hardware already included a dsPIC microcontroller (see Section 3.5) a digital implementation was considered first. The advantage of this was that all three functions could be carried out entirely in software, removing the need for further ICs and discrete components.

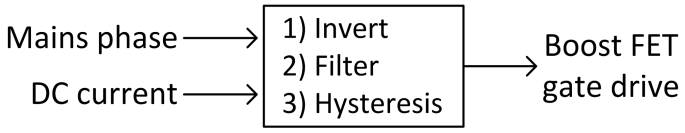

Figure 6.2: Control functions for the filter-based APFC system

For the first step the DC current signal (I_{in}) is sampled by an analogue to digital converter, with the sample values inverted when the mains is in the negative half-cycle. This process effectively generates a digital representation of the AC input current, which can then be digitally notch filtered to remove the line frequency component. By detecting when the resulting digital values fall outside predefined limits, a hysteresis effect is produced which can be used as the input to the boost MOSFET gate drive.

The key advantage to using a digital notch filter is that it is possible to make on-the-fly adjustments to the filter operation. This is particularly useful in the proposed application as the notch frequency can be adjusted to match the precise mains frequency. This allows optimal control to be maintained if the frequency drifts or if the system is used in a country with a 60Hz line frequency. The line frequency can be easily inferred from the time between changes in the phase input signal.

The drawback of this approach is the level of processing power required due to the bandwidth of the current sensor signal. It is necessary for the high frequency switching components (up to 350kHz) to pass through the filter without excessive distortion of their phase or amplitude, otherwise control of the input current will be lost. Upon designing the digital filter software it quickly became clear that the minimum sampling frequency of 700kHz would require a much larger number of filter taps than the dsPIC could handle. The problem stems from the fact that the target filter frequency is four orders of magnitude smaller than the minimum sampling frequency, requiring a very large number of delay steps. The dedicated digital signal processing hardware necessary to perform this function would be far too costly for this application, and it was therefore decided to use an analogue-based control system as discussed in Section 6.3.

6.3 Analogue Control System Design

6.3.1 Mains Polarity Detector

This subsystem was required to produce a digital output corresponding to the polarity of the mains voltage; 1 when positive and 0 when negative. As shown in Figure 6.3, this was achieved by firstly scaling down the live and neutral voltages to a level which could be handled by the control electronics (the 1MΩ and 10kΩ

resistors form a potential divider which reduce the voltage by 100x). After this a 4.8kHz lowpass filter (1kΩ resistor and 33nF capacitor) removes any high frequency noise which could cause false triggering of the comparator. The cutoff frequency had to be kept reasonably high to prevent any significant phase displacement at 50Hz (0.6 degrees in this case), as otherwise the comparator output would be shifted with respect to the mains voltage. The Schottky diodes clamp the scaled live and neutral voltages to prevent them from going below -0.3V and subsequently damaging the comparator. The final stage is a low cost TLC372 comparator which produces a 5V output when the live voltage exceeds the neutral voltage and 0V when the neutral voltage exceeds the live voltage. The 3.9kΩ pull-up resistor is in place due to the open-drain output of the comparator.

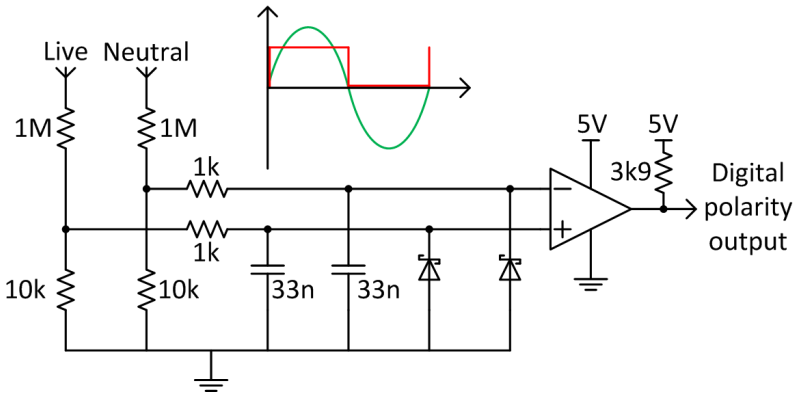

Figure 6.3: Hardware for the mains voltage polarity detector

Shown in Figure 6.4 is an artificial low voltage mains input signal and the corresponding output from the polarity detector. Due to the 100:1 potential divider at the input, the 20V signal amplitude becomes 200mV at the comparator inputs. As the TLC372 can require up to 5mV between the inputs to saturate the output, there is a small phase lag in the detection of the mains zero crossings. However, this lag becomes insignificant when the full mains voltage is applied to the inputs, with the worst case condition coming in at 0.609 degrees including the effect of the low pass filter.

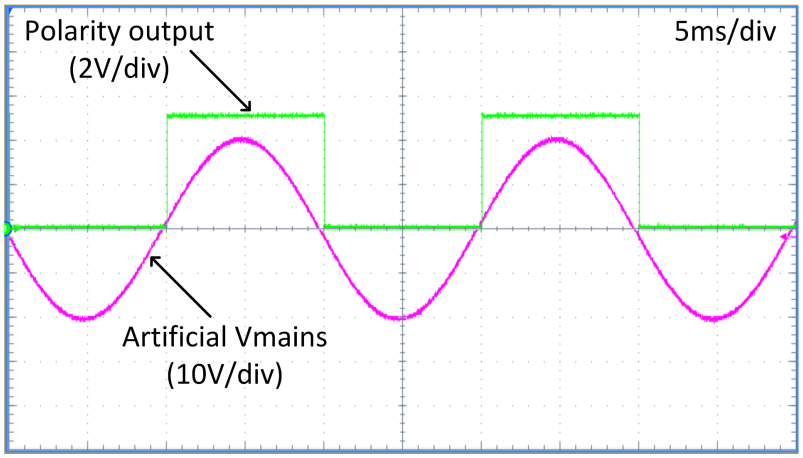

Figure 6.4: Oscilloscope screenshot showing detection of the input voltage polarity using a 20V peak signal from a waveform generator

6.3.2 DC to AC Current Sense Modulator

As explained in Section 6.1 it was necessary to modulate the DC input current sensor signal to generate an AC equivalent suitable for notch filtering. A simple method of achieving this is shown in Figure 6.5, using a DG9415 analogue multiplexer to reverse the shunt resistor connections by driving the output select pin with the mains polarity signal. In doing this, the voltage seen across the shunt is inverted when the mains voltage is negative, producing the necessary AC output. Due to the very high input impedance of the differential amplifier, the 14Ω $R_{DS(on)}$ of the internal multiplexer FETs did not cause any attenuation of the shunt voltage.

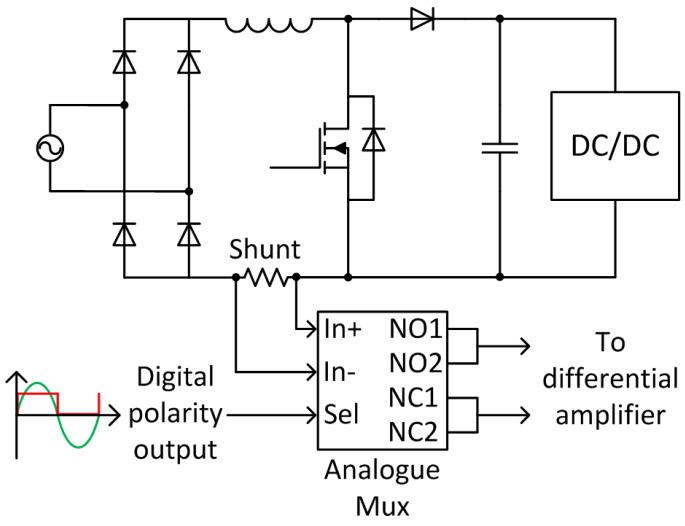

Figure 6.5: Hardware for the DC to AC current sense modulator

In order to test the remaining subsystems of the control hardware it was necessary to generate an artificial shunt voltage waveform which replicated the amplitude and shape of the power supply load current. A waveform generator was used to produce the shunt voltage shown in Figure 6.6, made up of a 3.1kHz sine wave representing the load harmonic which was then amplitude modulated by a rectified 50Hz sine wave. Along with the artificial mains voltage input this allowed the correct operation of the control hardware to be confirmed before it was connected to the boost converter, minimising the risk of damage during development.

Shown in Figure 6.6 are the input and output voltage waveforms from the analogue multiplexer. The output is the AC modulated version of the input signal, demonstrating the correct operation of the circuit. A DC offset of 20mV can be seen in the input signal which is caused by the oscilloscope probe and not the circuit itself. The absolute error is actually very small, but as the measured signal is only 100mV peak the relative error appears to be quite large.

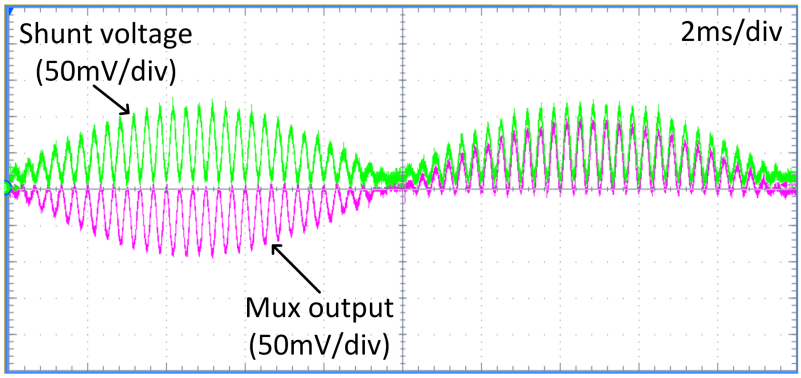

Figure 6.6: Oscilloscope screenshot showing the modulation of the DC current sensor signal producing an AC output

6.3.3 Shunt Differential Amplifier

Having generated the equivalent AC current sensor signal, the next step was to amplify it to a level more suitable for the notch filter and hysteresis controller. This stage could have been left out, but the system would have been much more prone to errors caused by a poor signal to noise ratio. This issue can be particularly severe in a system with very high frequency power switching such as this. A secondary function of the differential amplifier was to level shift the AC current sensor signal to 2.5V, allowing the system to operate from a single 5V supply rail. This was

achieved by connecting the non-inverting input of the ISL28191 op-amp to a 2.5V precision reference source, but to reduce costs a potential divider with 1% tolerance resistors could also have been used.

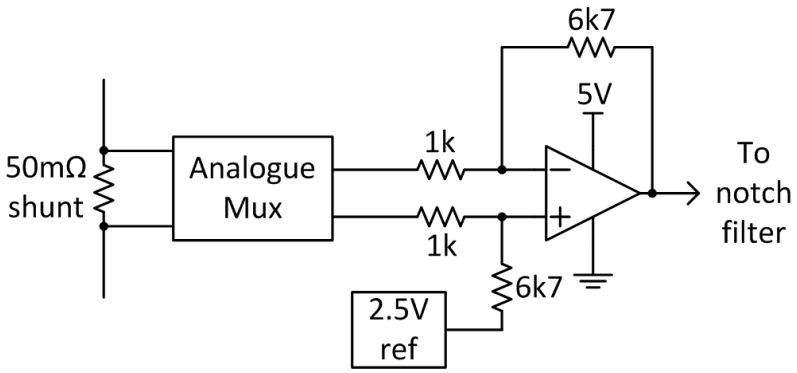

Figure 6.7: Current shunt differential amplifier with level shifting for operation from a single supply

A low inductance 50mΩ shunt resistor was chosen to give a balance between differential voltage and power loss. The current sensor system was designed to measure up to 3A peak to ensure sufficient headroom (See input current measurements in Section 4), leading to a maximum 150mV differential voltage and 450mW power dissipation. It was necessary to use a low inductance sense resistor to minimise any ringing of the shunt voltage which would not correspond to the real input current. A gain of 6.7 was selected for the amplifier giving an effective output of 335mV/A, limiting the output to +/-1V under normal operating conditions. Due to the 2.5V level shifted operation, the peak output range was +/-2.5V before amplifier saturation, allowing abnormal current conditions to be detected. This was necessary as the differential amplifier also provided an input to a hardware overcurrent protection system which was used to limit damage during development. As mentioned previously, the minimum current sensor bandwidth was 350kHz requiring an op-amp with a Gain-Bandwidth Product (GBP) of at least 2.3MHz.

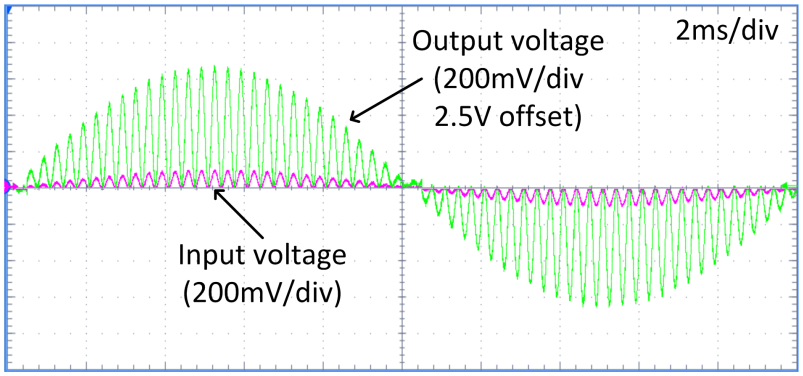

Figure 6.8: Oscilloscope screenshot showing the input and output voltages of the differential amplifier with an artificial shunt sensor signal

Shown in Figure 6.8 are the input and output voltages of the differential amplifier, demonstrating the correct gain of 6.7. The 2.5V level shift is not visible as the oscilloscope probe was given an offset of 2.5V to allow the output signal to be viewed clearly.

6.3.4 Notch Filter

The notch filter stage was required to extract the harmonics from the input current signal as explained in Section 5.3.2. The simulation work indicated that an attenuation of 18dB at 50Hz was required to give the maximum harmonic reduction without exceeding 500V on the DC link. However, during practical testing 500V was found to produce a peak output voltage capable of damaging the motor drive load. To prevent this, the APFC notch filter was re-tuned to 14.6dB, which subsequently produced a peak DC link voltage of 470V. The necessary filter response plot is shown in Figure 6.10.

Figure 6.9 shows the single op-amp notch filter that was employed for this purpose, with the notch frequency set as per Equation 6.1. As with the differential amplifier, a 2.5V reference was fed to the non-inverting input of the op-amp to allow level-shifted operation. Unity gain was set by having R2 equal to R1.

$$f_{notch} = \frac{1}{2\pi RC} = 50Hz \tag{6.1}$$

Where:

$$R = R3 = R4 = 68k\Omega \tag{6.2}$$

$$C = C1 = C2 = 47nF \tag{6.3}$$

Conventionally this filter circuit would require precise component tolerances to achieve the maximum Q factor and therefore maximum attenuation at the notch frequency. However, in this case a relatively low attenuation of 14.6dB was required, and by replacing R3 and R4 with potentiometers the circuit could be de-tuned to give the appropriate response. The values for R3 and R4 were determined through simulation as 80kΩ and 56kΩ respectively, producing the filter Bode plot shown in Figure 6.10.

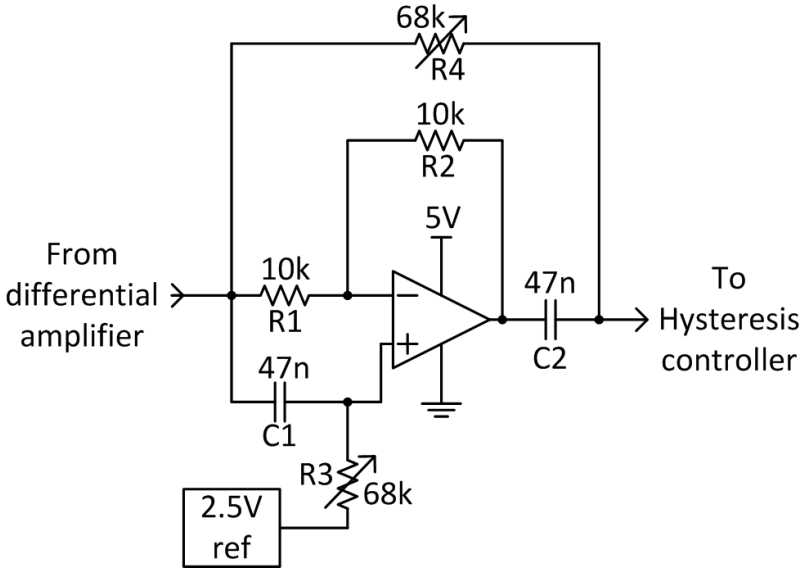

Figure 6.9: Single op-amp notch filter circuit with variable Q factor and level shifting for single supply operation

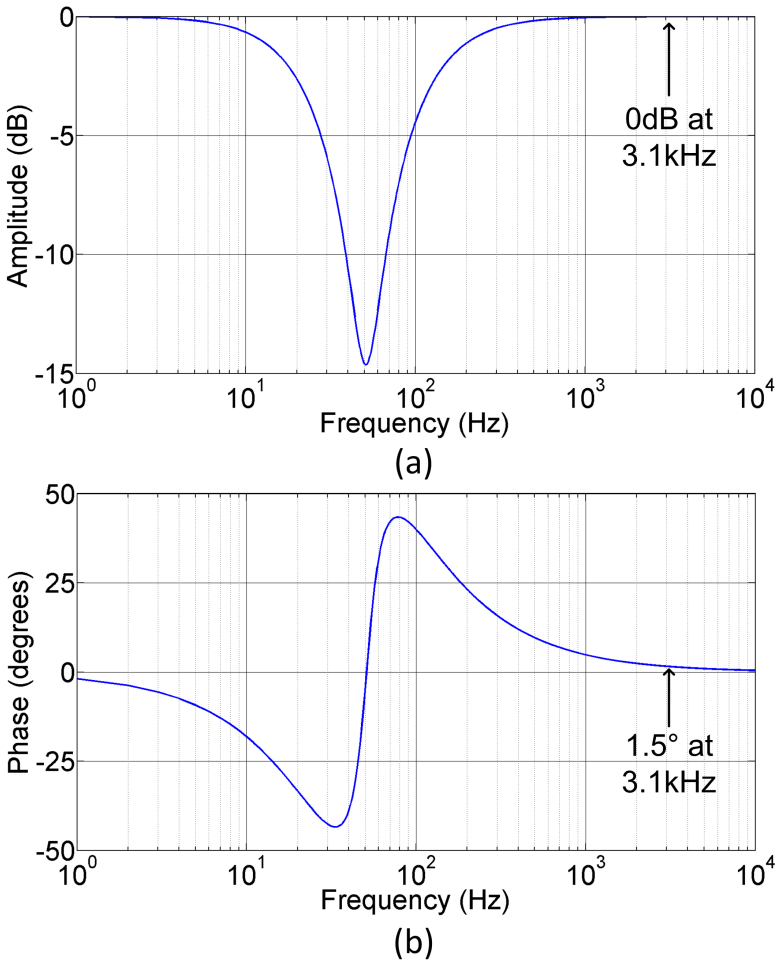

Figure 6.10: Bode plot for the 50Hz notch filter

The oscilloscope screenshot in Figure 6.11 shows the filter input and output voltages, demonstrating the attenuation of the 50Hz component whilst leaving the 3.1kHz harmonic unaffected in terms of amplitude and phase; the intended behaviour of the circuit.

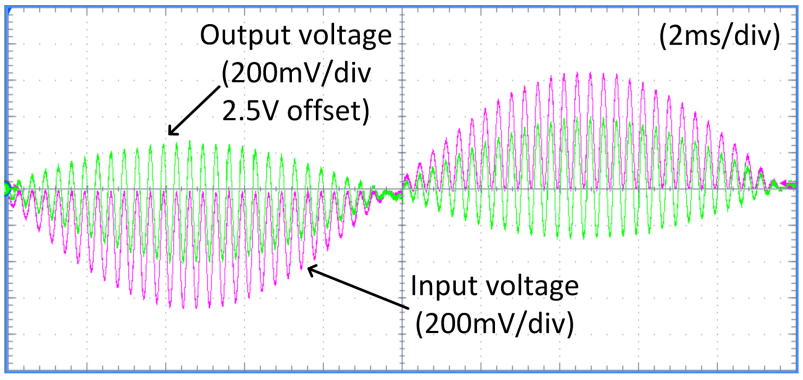

Figure 6.11: Oscilloscope screenshot showing the input and output voltages of the notch filter demonstrating the 50Hz attenuation

6.3.5 Hysteresis Controller

The notch filter output signal in Figure 6.12 is essentially a measure of the input current error. As the fundamental component has been attenuated, everything that remains is unwanted distortion and therefore needs to be removed. From the point of view of the hysteresis controller, the target current is always zero as it can only see the error and not the desired fundamental current. As discussed previously, it is precisely this which allows the filter-based APFC system to function without a voltage control loop. There is no need to scale the target input current relative to the load power, as clearly scaling zero by any factor will always result in zero output.

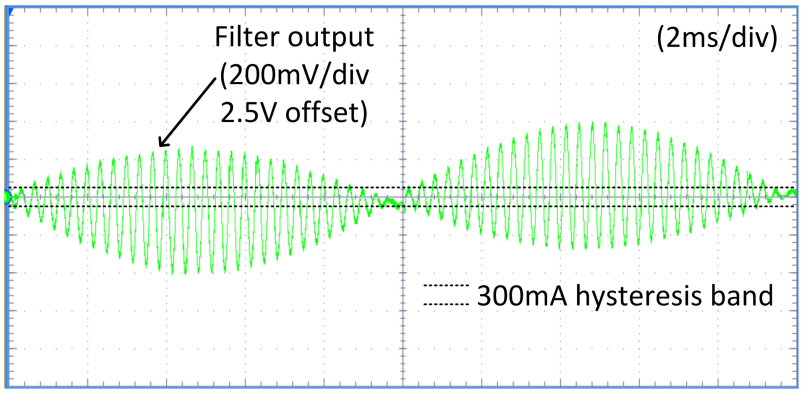

Figure 6.12: Hysteresis controller input waveform shown with the +-150mA bands

The simulation and design calculations in Section 5.3.2 indicated that a 300mA hysteresis band would give a good compromise between boost converter switching frequency and input current ripple. The hysteresis bands were therefore set to +-150mA via the ratio between R2 and R1 in Figure 6.13. As the error current signal is actually a voltage, the bands were set to +-50mV due to the current sensor output of 335mV/A as calculated in Section 6.3.3. A potentiometer was used for R2 to allow the bands to be adjusted during testing. As with the mains polarity detector, a pullup resistor was required on the output (R3) due to the open-drain configuration of the TLC372 comparator.

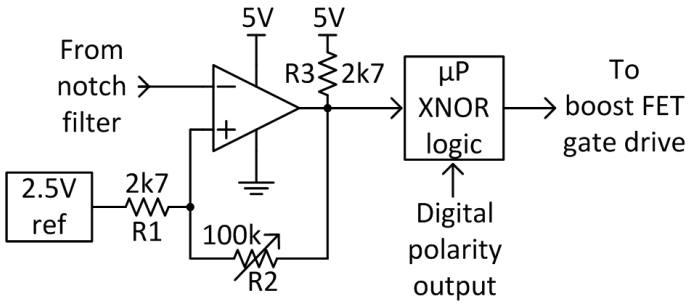

Figure 6.13: Hysteresis controller hardware with XNOR logic to decode output

Figure 6.14 demonstrates the action of the hysteresis controller, with the output going high when the non-fundamental input current (the sum of all harmonics and sub-harmonics) falls below -150mA and stays high until it exceeds +150mA. The effective hysteresis bands have been superimposed on the shunt voltage to show the effect of the notch filter. This demonstrates the equivalence between the subtraction of a reference from the input current and directly filtering the input current as shown in Figure 5.21.

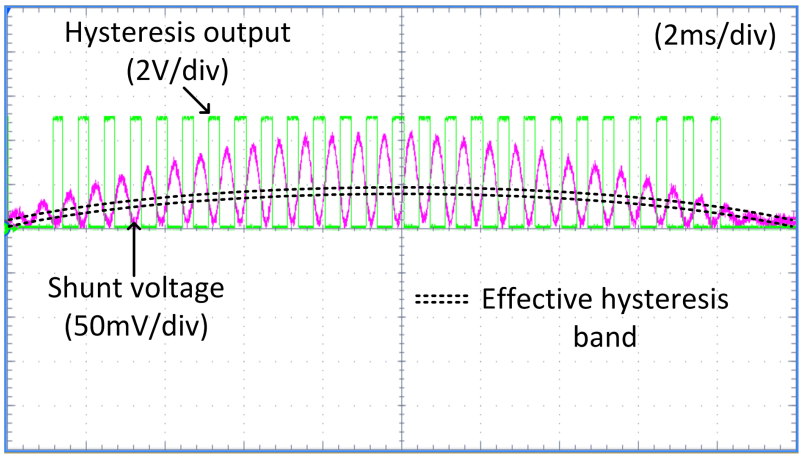

Figure 6.14: Hysteresis controller output shown with the shunt voltage and effective hysteresis bands

Before sending the hysteresis controller output to the boost MOSFET gate drive it was necessary to decode it based on the polarity of the mains. As the hysteresis bands were fixed, the output from the comparator needed to be inverted when the mains voltage was negative. Without this final step positive feedback would occur, turning the boost MOSFET on when the upper hysteresis band was exceeded, thus

making the problem worse. A very simple solution to this was to use an XNOR gate, with one input coming from the polarity detector and the other from the comparator. By observing the truth table in Table 6.1, it can be seen that the comparator signal is inverted when the input voltage is negative (polarity = 0) and left unchanged when it is positive (polarity = 1).

Polarity	Comparator	Output
0	0	1
0	1	0
1	0	0
1	1	1

Table 6.1: XNOR truth table demonstrating the polarity input enabling/disabling the inversion of the comparator input

Rather than implementing this function with a discrete logic gate it was decided to send the polarity and comparator signals to the microcontroller and carry out the logic in software. This was done for two reasons, firstly because the connections were already present on the PCB between the microcontroller and boost MOSFET gate drive, and secondly it allowed additional error checking systems to be put in place. A timeout function was added to the software which prevented the boost MOSFET from remaining in the on-state for over 100µs. This helped to prevent excessive input current in the event of an error or poor control system calibration. A software over-current trip was also added as a backup for the existing hardware over-current system.

The advantages of using software-based logic are largely restricted to the development stage, and so a dedicated XNOR gate would ultimately be used to reduce cost, size and propagation delay. In doing this, the need for a microcontroller would be removed altogether and the control system would use only low performance discrete parts. If such a system were incorporated into an integrated circuit, the cost saving over a digital system would be considerable.

Chapter 7

APFC Hardware Test Results

This chapter contains test results and discussion of the APFC control system hardware outlined in the previous chapter. The simulation developed in Section 5.3.2 is validated wherever possible, giving greater confidence in the tests which could not be corroborated with hardware results.

7.1 Control System Bandwidth

The control system model in Section 5.3.2 used an ideal current sensor, notch filter and hysteresis controller which effectively had an infinite bandwidth. This allowed a constant 300mA input current ripple to be maintained at all times (see Figure 5.29) as there was no delay in the response. However, for the practical control system there was a significant lag in the system response, causing overshoot of the hysteresis bands and therefore a greater input current ripple than intended. By analysing the delay caused by each stage of the control system, the simulation model could be modified to account for this, giving a response matching that of the hardware.

The worst case scenario for overshoot is at the peak of the mains when the input current will change rapidly. By referring to Figure 7.1 it can be seen that when the boost FET is conducting, the boost inductor is shorted across the mains supply allowing the rate of change of input current to be easily deduced:

$$\frac{\delta i}{\delta t} = \frac{V_{AC}}{L_{boost}} \tag{7.1}$$

Equation 7.1 is only valid if there is no voltage drop across the rectifier diodes or boost FET. Whilst this would not be the case in reality, the total voltage drop would only be around 4V; less than 2% of the peak supply voltage and therefore a reasonable approximation.

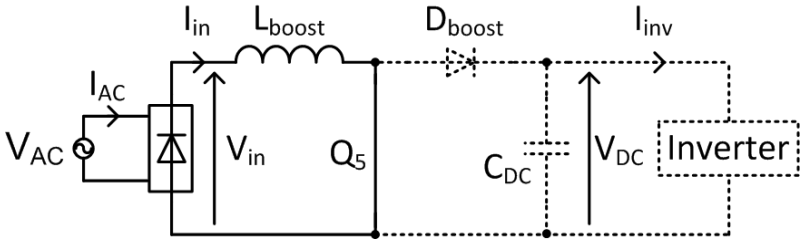

Figure 7.1: Boost converter equivalent circuit when the boost FET (Q5) is conducting

For a peak mains voltage of 325V and a boost inductance of 1.46mH this gives a peak $\frac{\delta i}{\delta t}$ of 0.223A/µs. Having determined this the delay of each stage can be calculated:

1. **DC to AC current sense modulator** - the analogue multiplexer introduced negligible lag as the output selection FETs were simply held in a conducting state to allow the input signal to pass through to the output.

2. **Shunt differential amplifier** - this was based on an ISL28291 operational amplifier with a minimum slew rate of 12V/µs. At a gain of 0.335V/A (see Section 6.3.3) the required slew rate was only 0.075V/µs, meaning that the lag due to this stage was also negligible.

3. **Notch filter** - this also used the ISL28291 operational amplifier at unity gain giving the same slew rate requirement. The phase shift of the notch filter was zero degrees above 10kHz, and therefore this also had minimal impact on the system response.

4. **Hysteresis controller** - the TLC372 comparator used for this was the most significant delay-introducing component, with an output change taking 650ns for a 100mV input step (the effective width of a 300mA current step).

5. **XNOR logic** - the delay of the software-based logic stage was determined by measuring the response time to an input change. The 450ns processing delay can be seen in Figure 7.2.

6. **Boost FET gate drive** - the final stage of the control system was the TC4420 gate driver which has a maximum delay time of 75ns.

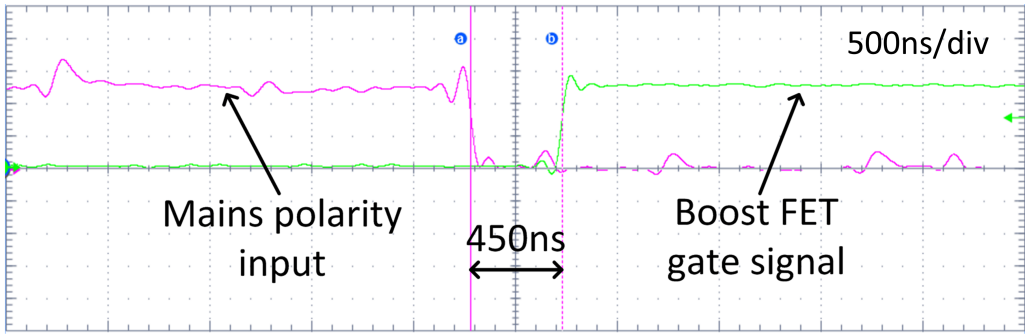

Figure 7.2: Oscilloscope screenshot demonstrating the 450ns processing delay of the microcontroller XNOR logic

The result of this is a total delay of 1207ns between one of the hysteresis bands being exceeded and the appropriate change to the state of the boost FET. The amount of overshoot this causes is dependent on the input current ramp rate, which at the peak of the mains is 0.223A/µs, leading to an overshoot of 267mA. As the mains voltage directly controls the input current $\frac{\delta i}{\delta t}$, it also controls the overshoot, causing the input current ripple to vary over each mains half-cycle as can be seen in Figure 7.4. By adding the hardware delay times into the control system simulation, a close agreement was achieved with the hardware results, as demonstrated in Section 7.2 and 7.3.

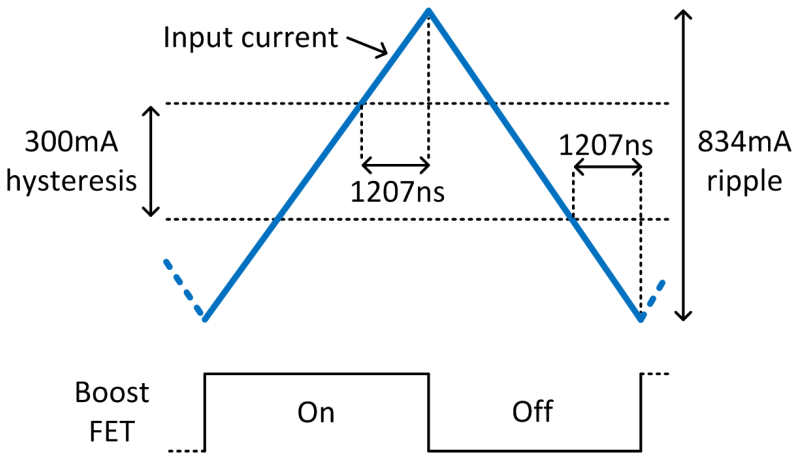

Figure 7.3: Control system bandwidth limitation causing overshoot of the hysteresis bands and increased input current ripple

In the original simulation, the peak switching frequency was 320kHz with a 300mA hysteresis band. With the hardware delay times added in the peak switching frequency was reduced to 110kHz with an effective band of 834mA. A vast improvement on this could be made simply by replacing the hysteresis comparator with a more sensitive and faster device. Comparators with a response time of under 100ns are available very cheaply (under 10 cents), and substituting this part alone would halve the overall delay time. The other major contributor is the software processing delay which could be eliminated by implementing the XNOR logic in hardware. Similarly, low cost discrete logic gates are available with sub-100ns response times.

7.2 Low Attenuation APFC Results

From the simulation (Section 5.3.2) and initial practical tests, the ideal filter attenuation was determined as 14.6dB. This gave the maximum harmonic cancellation without the DC link voltage exceeding 470V, and was subsequently chosen as the initial setting for the APFC hardware tests.

The oscilloscope screenshot in Figure 7.4 clearly demonstrates the ability of the APFC control system in removing the load frequency harmonics. Before the control system is enabled the motor load harmonics pass straight through the power supply and into the mains, leading to very high levels of distortion. At the indicated point a switch was pressed which enabled the microcontroller output to the boost FET

gate driver, thereby allowing control over the input current. From this point on the load harmonics are attenuated significantly, leading to a relatively sinusoidal input current which is in phase with the supply voltage (see Figure 7.5).

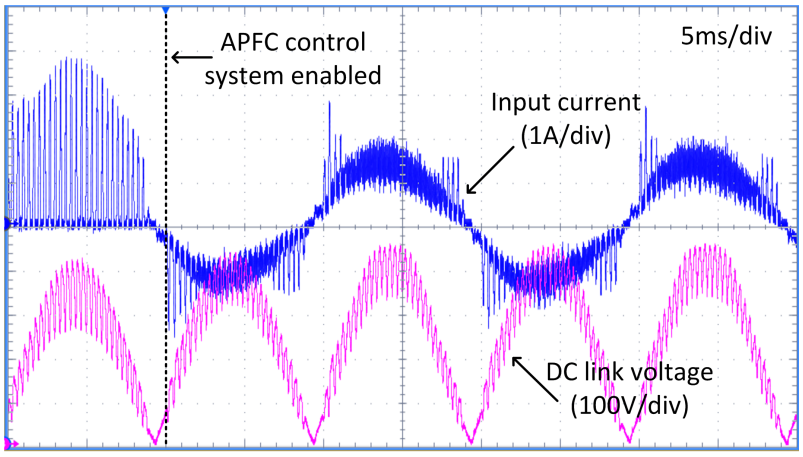

Figure 7.4: Hardware input current and DC link voltage before and after the APFC system is engaged at 14.6dB attenuation

As a consequence of the boost converter operation, the DC link voltage is increased slightly once the APFC system is active. With a low filter attenuation setting, as in this case, the peak voltage is increased from 425V to 465V.

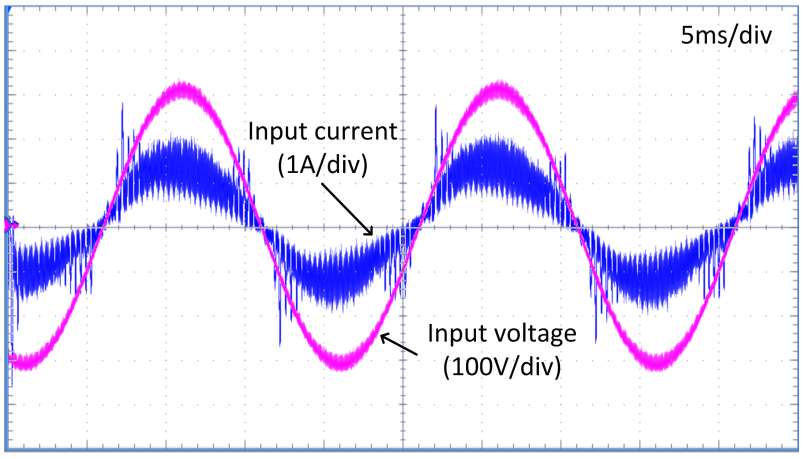

Figure 7.5: Hardware input current and input voltage with the APFC system set to 14.6dB attenuation

Shown in Figure 7.6 is a comparison of the mains input current and DC link voltage for the APFC simulation and hardware. A very close agreement between the results

can be seen, demonstrating the accuracy of the simulation model. The minor discrepancies between the two sets of results are quantified in Table 7.1.

Figure 7.6 shows the downside of having the notch filter set to a low attenuation; intersections between the input and DC link voltages leading to input current distortion around the mains zero crossings. The motor conduction angle modulation system proposed in Section 4.3 is an ideal solution to this problem as it only requires control system changes. Alternatively, the DC link capacitance could be increased, reducing the ripple voltage but of course this requires a larger and more expensive component to be used.

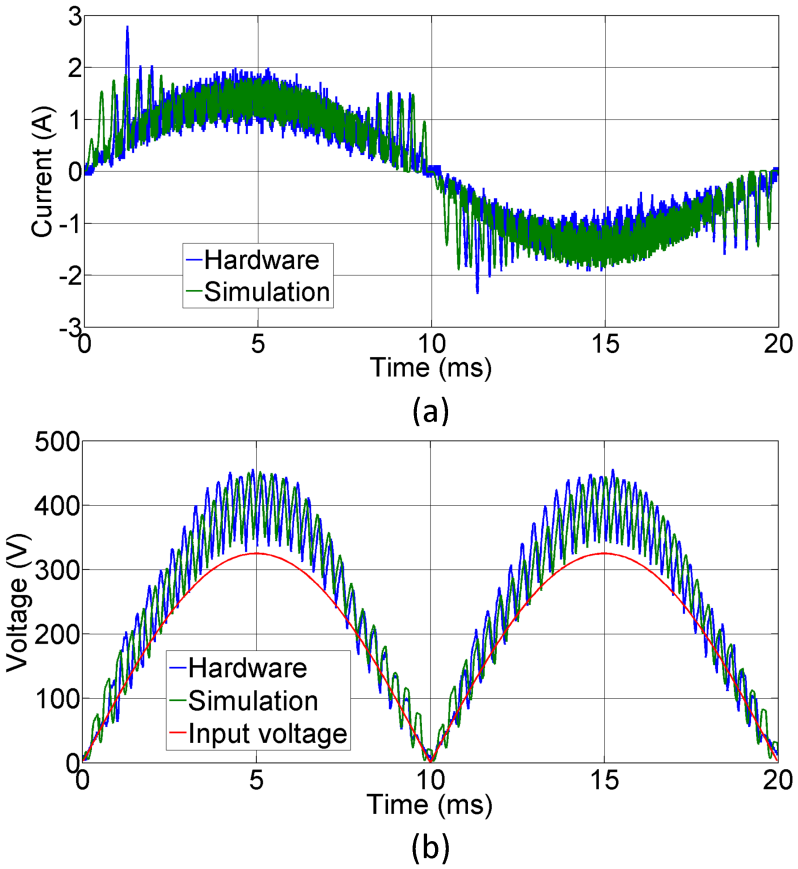

Figure 7.6: Hardware and simulation results for (a) input current and (b) DC link voltage at 14.6dB attenuation

The input current harmonics derived from Figure 7.6 (a) are shown in Figure 7.7. The 3.1kHz load frequency component can be seen along with its second and third harmonics. Due to the actual motor drive operating at a slightly higher speed than in the simulation, a slight offset exists between the results at these frequencies.

There was no direct method by which to control the motor speed, as it is constantly altered by the drive in order to maintain a fixed output power.

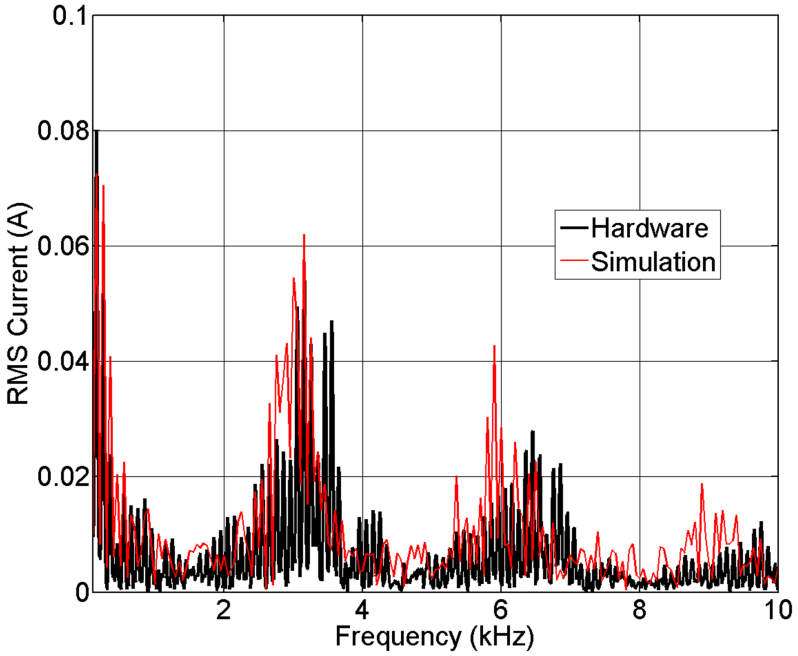

Figure 7.7: Input current harmonic spectrum for the simulation and hardware with the APFC system set to 14.6dB attenuation

Figure 7.8 shows the input current harmonics against the scaled EMC limits. The distortion of the input current around the mains zero crossings means that some of the higher order harmonics still exceed the scaled limits.

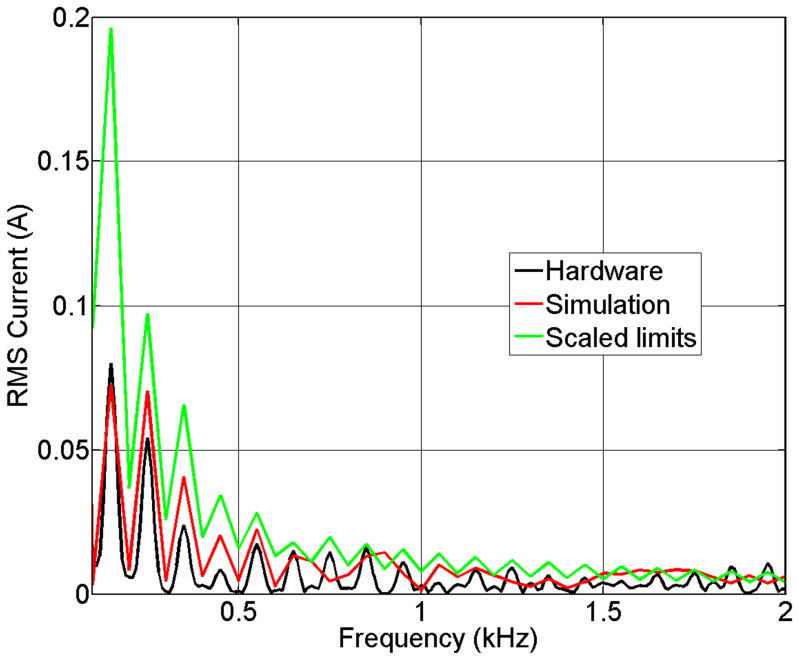

Figure 7.8: Input current harmonic spectrum for the simulation and hardware with the APFC system set to 14.6dB attenuation. Scaled EMC limits are shown for comparison

Shown in Table 7.1 is a summary of the key results from the APFC hardware and simulation tests. A very close correlation is seen between all of the measurements except for the total harmonic distortion based on a 0-10kHz range. As discussed previously, this discrepancy stems from the higher relative error in the FFT measurements.

Parameter	Hardware	Simulation	Error
I_{AC}	$1.07A_{RMS}$	$1.04A_{RMS}$	2.8%
V_{AC}	$230V_{RMS}$	$230V_{RMS}$	0%
V_{DC}	$251V_{mean}$	$246V_{mean}$	2%
V_{DC}	$455V_{peak}$	$451V_{peak}$	1.1%
THD (0-2kHz)	16.4%	16.1%	1.8%
THD (0-10kHz)	27.5%	29.6%	7.1%
Power Factor	0.940	0.942	0.2%

Table 7.1: Key measurements for the APFC tests at 14.6dB attenuation

7.3 High Attenuation APFC Results

To further demonstrate the effect of the notch filter attenuation on input current harmonics, the filter was re-tuned to give a response of -30.5dB at 50Hz. As can be seen in Figure 7.9 and 7.10, this results in almost complete cancellation of the input current harmonics. However, the penalty for this is a very significant increase in the DC link voltage due to the high duty cycle of the boost converter. To prevent the DC link voltage from exceeding 470V with the APFC system active, it was necessary to reduce the AC supply voltage to $130V_{RMS}$. Clearly this is not a realistic operating point for a nominal $230V_{RMS}$ system, but it serves to demonstrate the capability of the control system in attenuating input current harmonics.

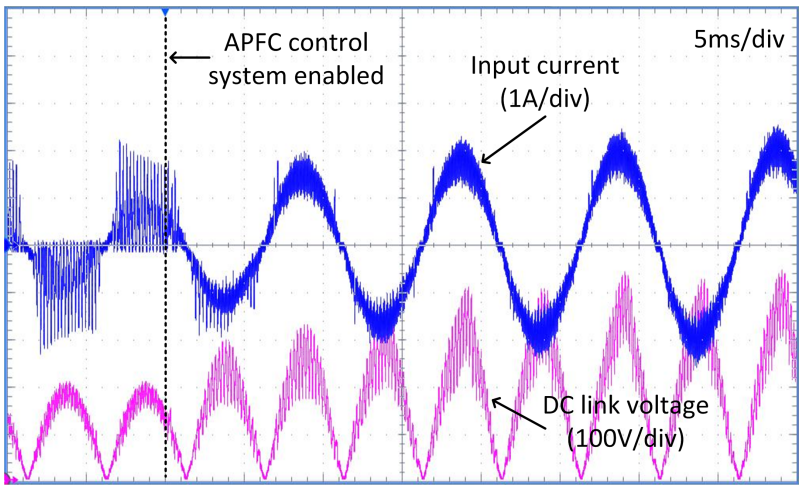

Figure 7.9: Hardware input current and DC link voltage before and after the APFC system is engaged at -30.5dB attenuation

A clear observation can be made from Figure 7.9 in that the amplitude of the fundamental input current increases and then settles at a steady state after the APFC system has been enabled. This happens because initially the supply voltage has been artificially reduced, leading to a lower DC link voltage. As the power supply is unregulated this causes the output voltage to be reduced by the same factor, resulting in a reduced load power (below 16.2V the motor drive cannot sustain full power). When the APFC system begins to boost the DC link voltage, the power supply output increases towards its nominal voltage, allowing the motor to accelerate to full speed. In the 80ms period after the APFC system is engaged, the motor accelerates from approximately 60,000 RPM to 80,000 RPM. This demonstrates the control system's ability to cope with changing load power and load frequency.

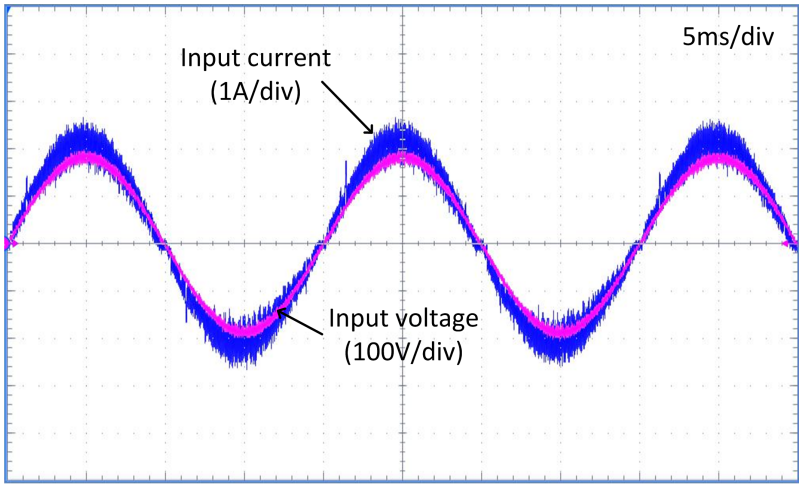

Figure 7.10: Hardware input current and input voltage with the APFC system set to 30.5dB attenuation

The oscilloscope screenshot in Figure 7.10 shows the full performance potential of the filter based APFC system. When a high attenuation setting is used the input current shape is tightly controlled, resulting in minimal low order distortion and a phase shift of almost zero. As mentioned previously, this is made possible by the very high boost factor $\frac{V_{DC}}{V_{in}}$ which virtually eliminates intersections between the input and DC link voltages, allowing control over the input current at all times. At the peak of the mains where the load harmonics are largest, the boost factor reaches 96% as can be seen in Figure 7.11 (b). If the same high attenuation setting were to be used with a $230V_{RMS}$ input, the peak DC link voltage would reach 717V. For any practical design it would therefore be necessary to accept a higher input current distortion to allow a reduction in DC link voltage.

One minor discrepancy can be observed between the simulation and hardware results in this case. Near the mains zero crossings the simulation shows a small amount of load-frequency distortion appearing in the input current which is not apparent in the hardware measurement. By looking closely at the simulation result in Figure 7.11 (b), a greater DC link voltage ripple can be observed around the mains zero crossing, leading to intersections with the input voltage and temporary loss of input current control.

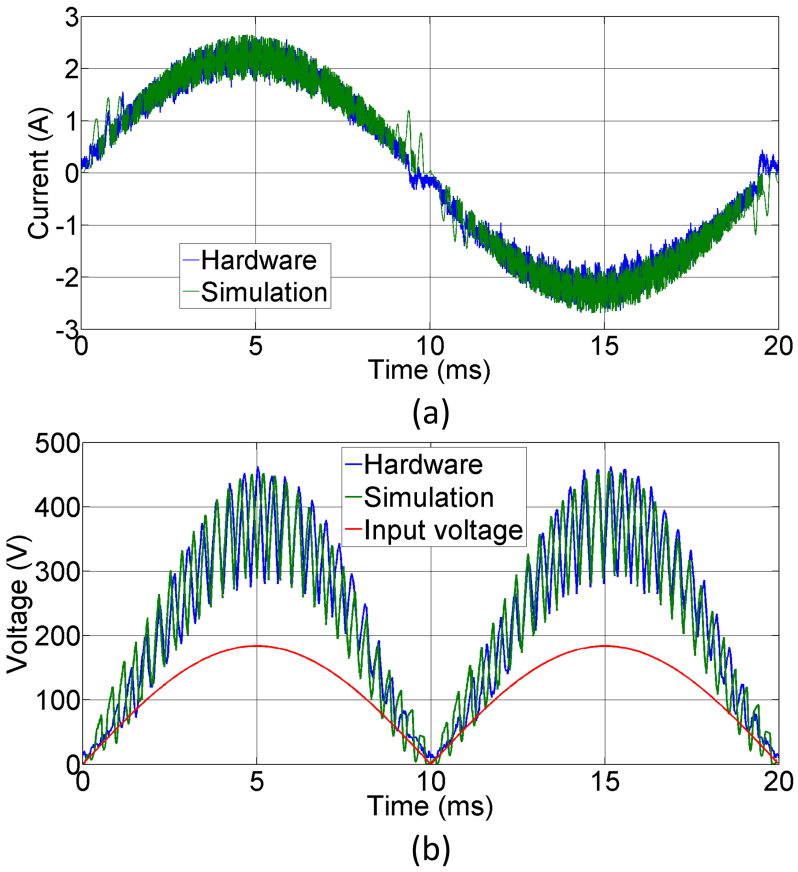

Figure 7.11: Hardware and simulation results for (a) input current and (b) DC link voltage at 30.5dB attenuation

The harmonic spectrum of the input current in Figure 7.11 (a) is shown in Figure 7.12. As with the low attenuation FFT, a precise correlation between the results is not achieved because the relative amplitude of the harmonics to the fundamental is so small. In this case the largest harmonic is less than 2% of the fundamental, making the measurements highly susceptible to error. Despite this, a small but clear peak can be seen at the load frequency, resulting from the harmonics present near the mains zero crossings.

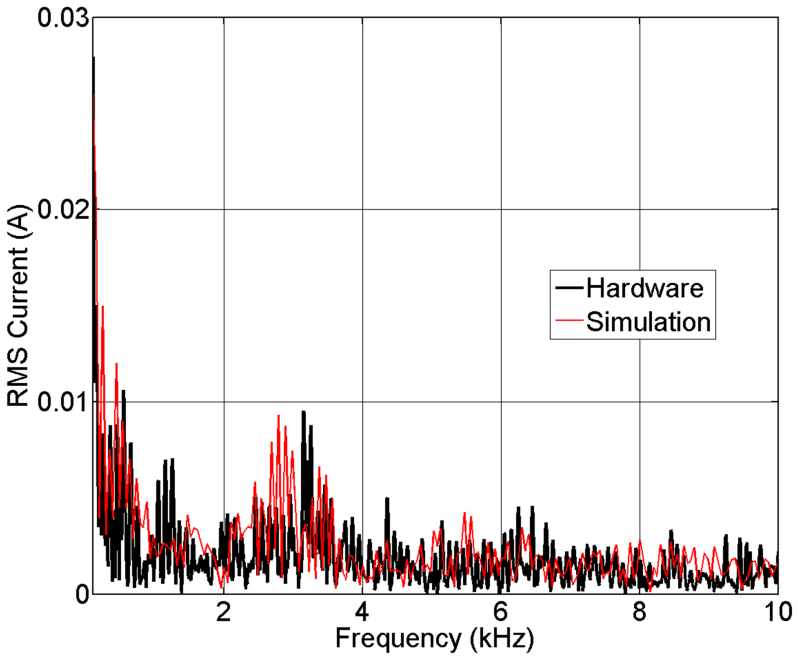

Figure 7.12: Input current harmonic spectrum for the simulation and hardware with the APFC system set to 30.5dB attenuation

The difference in FFT results can also be seen clearly in Figure 7.13. Whilst the individual harmonic amplitudes vary considerably, the general trend of the results are in agreement and ultimately suggest that an EMC test would be passed using the scaled limits. The error between the results is reflected in the THD calculations shown in Table 7.2. This is made particularly clear in the 0-2kHz calculation where the absolute error is very small but the relative error is large.

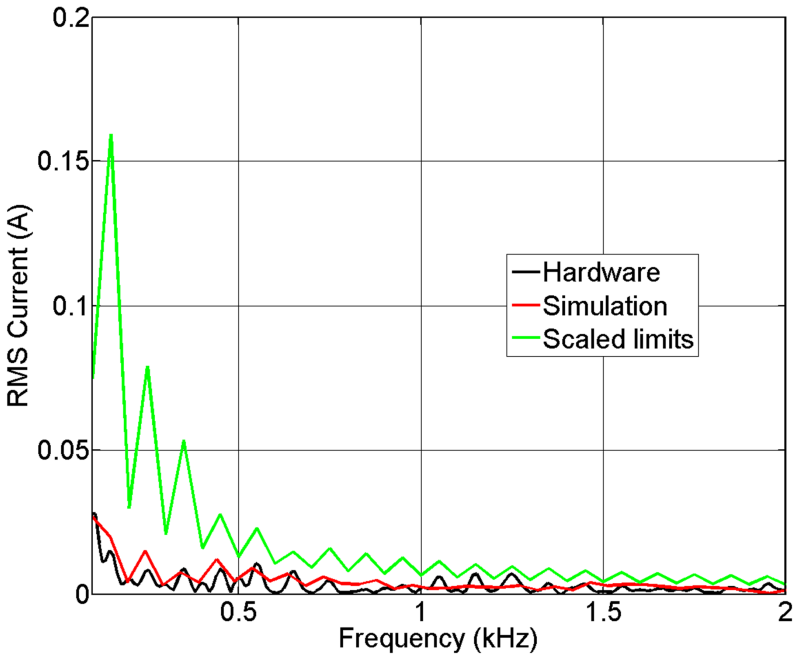

Figure 7.13: Input current harmonic spectrum for the simulation and hardware with the APFC system set to 30.5dB attenuation. Scaled EMC limits are shown for comparison.

Parameter	Hardware	Simulation	Error
I_{AC}	$1.60A_{RMS}$	$1.63A_{RMS}$	1.8%
V_{AC}	$130V_{RMS}$	$130V_{RMS}$	0%
V_{DC}	$258V_{mean}$	$253V_{mean}$	1.9%
V_{DC}	$455V_{peak}$	$451V_{peak}$	0.9%
THD (0-2kHz)	4.20%	5.33%	21.2%
THD (0-10kHz)	10.3%	11.5%	10.4%
Power Factor	0.991	0.983	0.8%

Table 7.2: Key measurements for the APFC tests at 30.5dB attenuation

7.4 Line Frequency Variation

The results in this section demonstrate the effect of line frequency variation on the APFC performance. It is necessary to consider this as the mains supply can deviate slightly from the nominal 50Hz value, and so any connected system must remain stable under worst case conditions. This is covered by European Standard EN50160 governing voltage characteristics for public electricity networks, which states that

the supply frequency must be 50Hz +/- 1% for 99.5% of a year and 50Hz +4% / -6% at all times [84]. The greatest possible deviation is therefore 50Hz -6% which equates to 47Hz.

As a variable frequency source was not available it was only possible to test the system response in simulation. However, given the consistency between the simulation and hardware results throughout this work, it is reasonable to assume this provides a good representation of the hardware behaviour. Shown in Figure 7.14 (a) is the mains voltage and input current when the supply frequency is set to 47Hz. The high filter attenuation setup was used as per Section 7.3 which required the supply voltage to be reduced to 130V_{RMS}. This operating point was chosen as it provides the clearest demonstration of the effect of line frequency variation.

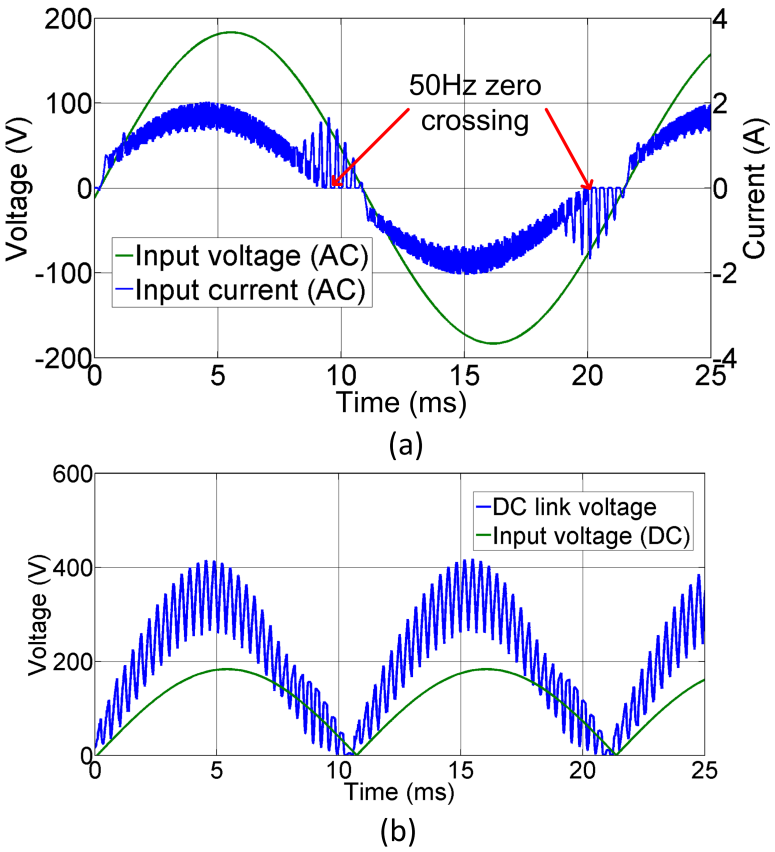

Figure 7.14: Simulated line voltage at 47Hz to show effect of worst case frequency variation. (a) Input current and input voltage (b) DC link voltage and DC input voltage. Supply voltage set to 130Vrms to allow comparison with high attenuation tests.

Figure 7.14 highlights the limitation of having a fixed notch filter frequency; the control system attempts to produce a 50Hz sinusoidal input current regardless of the supply frequency. This is possible up to the point where the effective 50Hz zero crossing occurs as shown in Figure 7.14 (a). Beyond this point the current would have to go negative to maintain a sinusoidal shape, but this is not possible for two reasons. Firstly, the presence of the front-end bridge rectifier forces the input voltage and current to have the same polarity at all times. Secondly, the boost converter only has unidirectional control over the input current and subsequently cannot produce a negative current flow. In a condition where the input current is higher than the required value, the hysteresis controller output simply remains low keeping the boost FET switched off.

The resulting input current harmonics with a 47Hz line frequency are shown in Figure 7.15. This can be directly compared with Figure 7.12 to show the effect of a 6% line frequency variation, as this was the only parameter which was changed between the two tests. Despite the increased harmonic content (particularly at the motor drive switching frequency) the resulting THD was only 21.3% with a power factor of 0.907. Given that this represents the absolute worst case scenario, the system performance under variable line frequency conditions can be deemed satisfactory if not ideal.

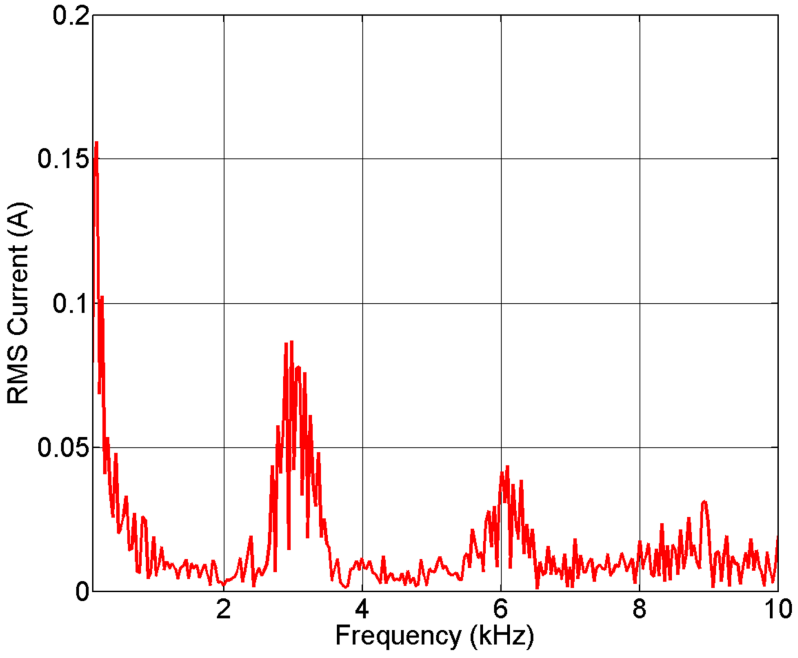

Figure 7.15: Input current harmonic spectrum derived from 7.14 (a)

To show this effect more clearly the same simulation was run but with the line frequency reduced to 25Hz (this is not an operating condition which would ever actually occur). As before, Figure 7.16 demonstrates the control system attempting to produce a 50Hz input current as far as is possible. After 10ms the 50Hz zero crossing point occurs and the hysteresis controller sees a constant negative error, causing the boost FET to remain off until the next mains cycle. Whilst the boost converter is not operating the load harmonics are passed through to the supply causing significant distortion. A key point to note is that whilst the performance reduces with line frequency drift, the response remains stable.

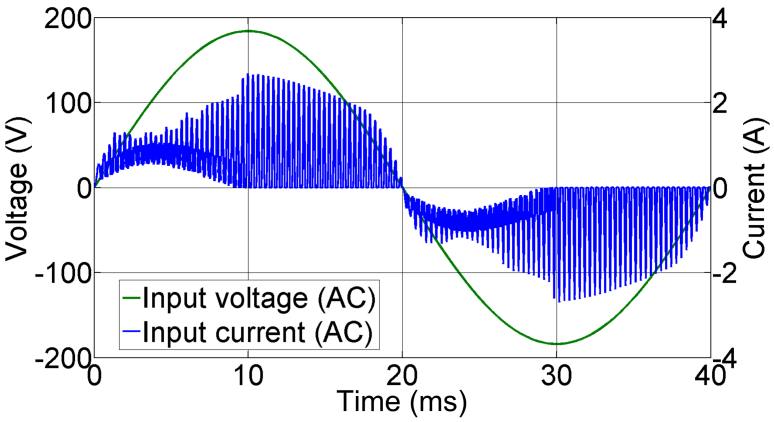

Figure 7.16: Input voltage and input current when the mains frequency is reduced to 25Hz

As discussed in Section 6.2, a digital implementation of the APFC control system would allow the notch filter to be tuned on-the-fly to match the exact supply frequency, maintaining full harmonic cancellation at all times. A further advantage of digital control is the ability to adjust the Q-factor of the filter and thus the attenuation at the notch frequency. As has been shown previously, the filter attenuation controls the level of harmonic rejection and subsequently the DC link voltage. Through control of the Q-factor it would therefore be possible to regulate the peak DC link voltage and maximise the system performance for all supply conditions. For the current analogue implementation it would be necessary for the hardware to be pre-set for a particular market, e.g. 230V/50Hz for Europe or 120V/60Hz for the USA. This does not necessarily pose a problem as many products are currently designed on a per-market basis, but clearly a universal system could be advantageous to both the manufacturer and consumer.

7.5 Load Shutdown

The final test of the APFC system performance was to measure the response to an instantaneous load shutdown. Results for a step load increase (Figure 5.37) and motor acceleration (Figure 7.9) have already been shown previously. For both the simulation and hardware tests in this section, the low notch filter attenuation setup was used (-14.6dB) with a standard 230V/50Hz supply.

Figure 7.17 initially shows the simulated input current and DC link voltage during steady state operation with the APFC system active. At the indicated point the motor drive was switched off, removing the load from the power supply. As a result of this the DC link voltage greatly increases due to the boost converter forcing more charge into the DC link capacitor than is removed by the load. The reason that it does not increase indefinitely is because despite the motor load being removed, the DC/DC converter MOSFETs are still switching. As discussed extensively in Section 4.5, the chosen power supply design has a very high power consumption when unloaded, and so the switching loss alone presents a considerable load to the boost converter. As the APFC system has no knowledge of the DC link voltage, the boost switch is simply modulated in order to perpetuate a 50Hz input current regardless of the power supply/load behaviour. In this case, the DC link voltage stabilises at the point where the power supply switching losses become so large that they equal the power consumption by the system before the load was switched off. This is the reason that the input current amplitude is the same before and after the load shutdown event. In a separate simulation where the power supply was switched off instead of the motor drive, the DC link voltage rapidly increased towards infinity as there was nowhere for the input current to flow other than into the DC link capacitor.

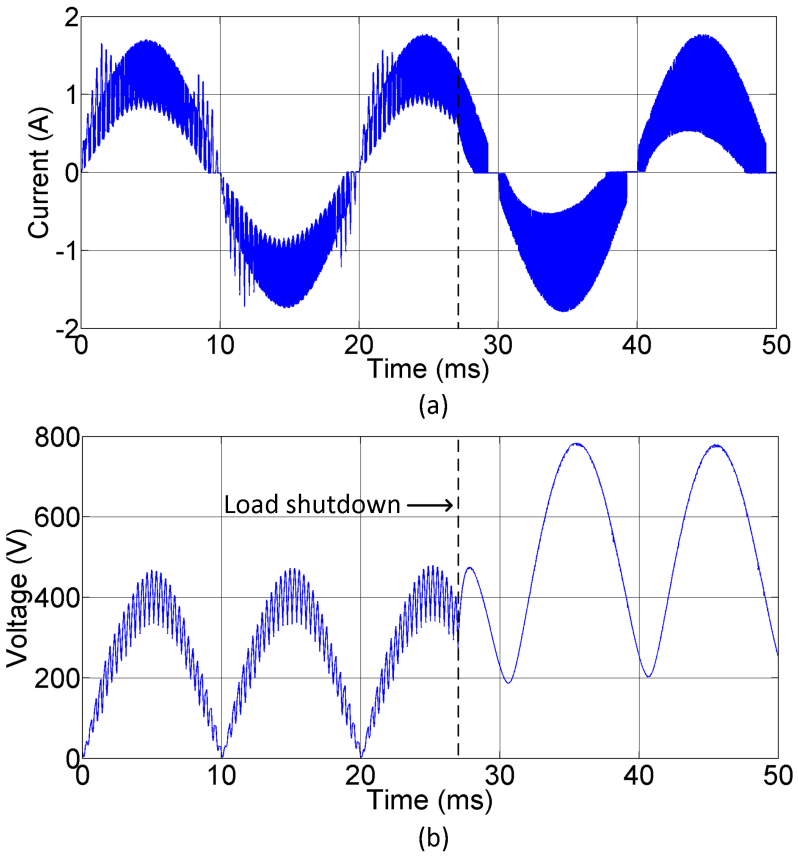

Figure 7.17: Simulated (a) input current and (b) DC link voltage for an instantaneous load shutdown with the APFC system set to 14.6dB attenuation

The simulated load shutdown results are clearly theoretical, as in practice the components would simply be destroyed once the voltage and/or losses reached a certain threshold. However, this situation is easily avoided with over-voltage protection which can be found on almost all power electronic systems, including the low capacitance power supply used for this work. In this case, a comparator monitors the DC link voltage and disables all the power electronic devices when the safety threshold is exceeded. The reaction time for the over-voltage protection hardware is under 1us which is fast enough to prevent any damage. This system can be seen working in Figure 7.18. There appears to be less input current ripple in the hardware results (Figure 7.18) than the simulation (Figure 7.17) because the oscilloscope was set up for a long capture window and therefore the sampling rate had to be reduced.

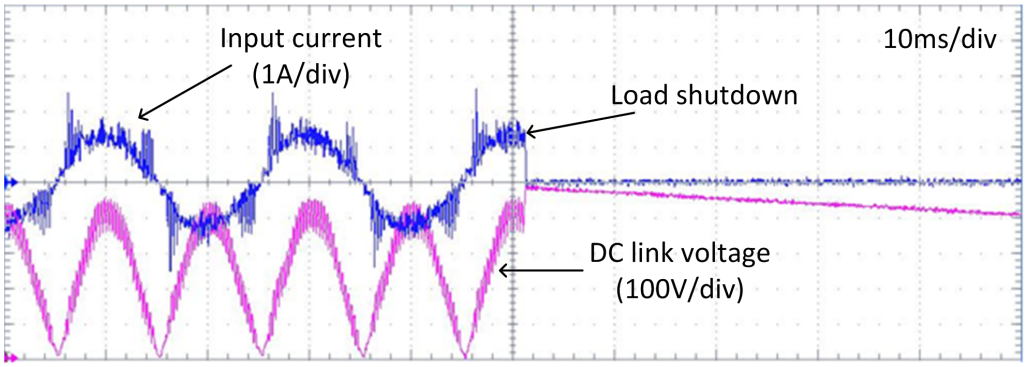

Figure 7.18: Oscilloscope screenshot showing the hardware input current and DC link voltage for an instantaneous load shutdown

Having minimal DC link capacitance clearly diminishes the system's ability to cope with rapid supply or load changes. The less energy it can store, the less time it takes for the DC link voltage to change and subsequently exceed the normal operating limits. This issue would still be faced by conventional APFC controllers which include a voltage control loop, as the slow response necessary to maintain a sinusoidal input current would mean that the DC link voltage could change much faster than the system could react. As discussed in Section 2.3.2, the voltage control loop of a conventional APFC system has a bandwidth of approximately 20Hz and would clearly not have the microsecond-level reaction time required to prevent excessive DC link voltage in a reduced capacitance converter.

To further understand the system behaviour, the notch filter step response was analysed in isolation. Shown in Figure 7.19 is the filter response to a 50Hz 1V step input at the low and high attenuation settings. The 1V input signal lasts for 50ms and then returns to zero. The key observation to be made is the settling time; in both cases the output signal reaches a steady state value after 20ms. It is this which determines the system's response time to load changes, and can be seen by referring back to Figure 5.37 (a) where the APFC system restores complete harmonic cancellation 20ms after the load step. Initially the increased load causes the small DC link capacitor to rapidly discharge below the input voltage, resulting in harmonic currents being drawn directly from the supply. Although the current control loop has a high bandwidth (>100kHz), the harmonics are not immediately attenuated as the filter output does not immediately generate an error signal.

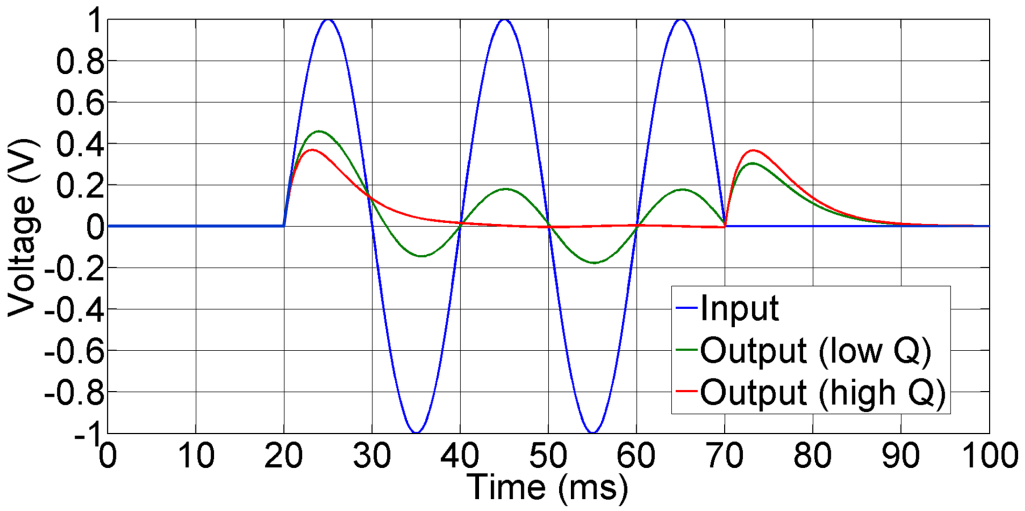

Figure 7.19: Simulated notch filter response to a 50Hz step input applied for 50ms. Outputs shown with filter tuned for high and low attenuation

The fundamental behaviour of the notch filter can be seen as one of the key limiting factors in the performance of this control system. However, as has been noted previously, there is little gain to be made in speeding up the system response any further, as rapid modulation of the input current inherently generates harmonics. This would clearly be an undesirable effect in a system designed with the opposite purpose. Furthermore, in the intended application a step load increase is not an operating condition which would realistically be encountered. A motor acceleration event represents the fastest non-fault load increase the APFC system would have to handle, during which the load is increased over a longer period of time ($\gg$20ms), and thus allows input current control to be maintained (see Figure 7.9). If a fault condition does occur (e.g. jammed rotor or instant load shutdown) it is no longer necessary for the APFC system to provide harmonic attenuation. The most appropriate action at this point is to shut down the entire system as shown in Figure 7.18.

It is worth noting that for compliance with the BS EN 61000-3-2 harmonic standards it is not necessary to meet the limits until 10 seconds after the system has been powered up. Therefore it is not strictly necessary for harmonic attenuation to take place whilst the system is settling into steady state operation, a factor which could be of assistance in certain applications. In this case, the 10 second delay would give ample time to eliminate the motor acceleration phase from the harmonic measurement.

If used with a different load capable of more rapid changes, the suitability of this approach would be in question. Whilst the APFC system maximises the use of the available DC link capacitance, once it is discharged below the input voltage or charged above the safe limit, harmonic compensation can no longer be provided. Similarly, for loads which inherently generate low frequency harmonics, a larger amount of energy storage must be present to maintain an equivalent input current quality.

Chapter 8

Conclusions

The primary aim of this thesis has been to research the effects of reduced DC link capacitance in a single-phase offline power system. This was undertaken because conventional AC to DC converters have considerable drawbacks due to this component, suffering from poor power factor, poor power density, high cost and poor reliability. It is identified that whilst many DC loads require a constant supply of power, there are some which can tolerate the large variation which results from having minimal energy storage. Previous work has shown that low performance motor drives are particularly suited to this; due to the inertia of the rotor, rapid variations in torque do not translate to rapid variations in speed. Having recognised the prior research in this field, the work in this thesis sought to identify the challenges in applying it to a power system with three distinct parts: AC to DC converter, DC to DC converter and BLDC motor load. The most valuable contribution came in the form of a simple and low cost APFC system designed specifically for use with 100% DC link voltage ripple.

A review of literature has shown that the most common application for reduced DC link capacitance is in three-phase motor drive systems. This stems from the fact that, when balanced, three-phase power is constant rather than time varying as with a single-phase system. This fundamental difference means that the use of reduced DC link capacitance is less challenging and subsequently more prevalent in this application. Where a three-phase active rectifier is used, it is possible to simultaneously achieve a high input power factor and a low output torque ripple without the need for significant decoupling. Due to the 30 degree intersections between conducting phases, the maximum DC link voltage ripple is limited to 15% even with an uncontrolled bridge rectifier. The drop in load performance is therefore much less severe than in a single-phase system where the voltage ripple can reach 100%.

In single-phase motor control applications, any system seeking to reduce motor torque ripple will inherently increase input current distortion when there is minimal energy storage present. These two factors are always in contention and so a compromise must be accepted between the two. The work in this thesis has sought to maximise the use of the available capacitance and thus arrive at the best overall design. As well as motor drives, previous work has demonstrated this same principle being applied to a battery charger, whereby the charging power is forced to follow a $\sin^2$ profile matching the instantaneous input power. Through modulation of the conduction angle, such behaviour is enabled in the motor drive used for this research.

It is noted that film capacitors have a number of favourable qualities over electrolytic variants, the most significant of which is increased lifetime. This is a desirable attribute in long-term installations, leading to the use of film capacitors for LED lighting, photovoltaic arrays and electric vehicle chargers. In these applications, power density and or component costs are not necessarily primary concerns, and as such the level of capacitance will be reduced just enough to make film devices viable. This stands in contrast to the domestic/consumer market where cost is the number one consideration and product lifetimes tend to be short.

The active ripple energy storage systems discussed in Chapter 2 highlight the inefficiency of conventional capacitor-based DC link energy storage. As the desired level of voltage ripple reduces, the ratio of stored energy to processed energy increases. By isolating the energy storage capacitor from the DC link, its voltage can vary over a much greater range without affecting the performance of the load. Arguably this represents the ultimate application of reduced DC link capacitance, simultaneously enabling high quality input and output power in a single-phase system. It is unfortunately the cost and complexity of the additional hardware required which prevents this approach from being more widely used.

Research into existing active power factor correction systems revealed none which could produce a low current distortion and work with minimal DC link capacitance. For a conventional system, the problem stems from the need for a voltage error signal which is not distorted by the DC link ripple. Any harmonics contained within this signal will modulate the input current reference and subsequently distort the actual input current. Where a large DC link capacitance is used, this does not pose a particular problem as the voltage feedback signal can be passed through a filter with a cutoff of around 20Hz. Whilst this makes the bandwidth of the voltage

control loop very slow, the large DC link capacitor provides a sufficient buffer to prevent any problems. If a conventional APFC controller is used with minimal DC link capacitance, two significant problems appear. Firstly, the filter cutoff frequency has to be much lower to maintain the same level of distortion in the voltage feedback signal. Secondly, there is no longer any bulk energy storage on the DC link to absorb an imbalance between input and output power. A slower dynamic response will exist where a faster one is required, resulting in poor performance.

Irrespective of the application, conventional APFC controllers are relatively expensive to implement due to the necessary multiplier, divider and squaring functions. Other approaches were analysed including voltage follower and waveform modification techniques, both of which have simpler control methods and less additional hardware. Such systems lend themselves to low power applications, as they can meet the Class A harmonic regulations with a high relative but low absolute level of input current harmonics. Whilst one of these approaches would have been sufficient for the 200W power system used in this thesis, a more universal solution was deemed to have greater value. In part, this provided inspiration for the development of a new APFC control system suitable for use at any power level and with any amount of DC link voltage ripple.

8.1 New Knowledge

The practical and simulation work in this thesis has provided further understanding of the challenges posed by reduced DC link capacitance. In some areas, existing knowledge has been reinforced, whereas in others it is entirely new. The former is best demonstrated by the power supply simulation using a conventional AC to DC converter. Producing a relatively smooth DC link voltage (6% ripple) in an otherwise identical setup required 470µF of capacitance. Despite the use of an electrolytic device, the volume and cost were increased by 1300% and 500% respectively, making the design unfeasible for a compact or low cost application. Furthermore, these figures do not account for the additional filtering that would be required to pass the EN61000-3-2 harmonic limits. The benefit of this approach is of course the constant supply of power available to the motor, allowing it to achieve the same performance from a smaller peak voltage and current.

The early power supply test results showed that with minimal DC link capacitance, the shape of the output current waveform is directly reflected in the input current

waveform. This is clearly demonstrated by all three of the test loads used: resistive-inductive, high capacitance motor drive and zero capacitance motor drive. It is therefore essential that the load is as linear as possible, in order to minimise the harmonic content and subsequently the amount of filtering required. These tests also demonstrated that regardless of location, energy storage in the system will always influence the power flow. When the standard 200W motor drive load was used, its 2000µF of decoupling capacitance was connected in parallel across the output terminals of the power supply. This smoothed the supply voltage to the motor and consequently distorted the input current in the same manner as a large DC link capacitor.

In relation to the previous point, it was also noted that the nature of the load current had a pronounced effect on the efficiency of the DC to DC converter. The zero capacitance motor drive load was the most dynamic, with the demand changing frequently between zero and 25A. The high peak currents and high inverter losses at light load caused the power supply efficiency to be poor in this case. Where the standard motor drive was used, the 2000µF of decoupling capacitance reduced the severity of the load transients and thus the efficiency improved. It is clear that the DC to DC converter stage is not the primary focus of this work, serving largely as a development platform for the APFC system, rather than directly providing a source of novel research. For further investigation it would be beneficial to design a system which is efficient over a very wide supply and load range.

It has been shown that the minimum energy storage requirement for sinusoidal input current is defined by the load behaviour rather than the supply frequency. The power supply tests with a resistive-inductive load demonstrated that when reduced DC link capacitance is used, a linear load will result in harmonic-free input current. Where the load is non-linear, it is therefore only necessary to attenuate the harmonics produced by the load and not by the charging of the DC link capacitor. A higher load frequency will subsequently require less energy storage, helping to improve the system power density. The very high operating speed of the 200W BLDC motor drive causes the fundamental load frequency to be high, making it suitable for a reduced DC link capacitance application. However, this could be improved by re-designing the motor with a higher pole number, more phases or increased operating speed. All of these changes will require faster commutation, leading to an increased load frequency.

Maintaining input current control with a boost converter APFC system requires the DC link voltage to exceed the input (supply) voltage at all times. This ultimately places a limit on the maximum DC link ripple, and therefore minimum DC link capacitance which can be used. As the capacitor size was based purely on the motor drive switching frequency, the APFC system fails to attenuate any lower order harmonics in the load current. Without use of the conduction angle modulation system, distortion occurs around the mains zero crossings as can be seen in the fixed reference and filter-based APFC results. Whilst the stability condition of $V_{DC} > V_{in}$ is also true for a conventional APFC system, it poses far less of a problem as the significant energy storage prevents large variations in DC link voltage from occurring.

Another conclusion to be made is the existence of a trade-off between harmonic attenuation and peak DC link voltage. For the filter-based APFC system, setting the notch filter to a high attenuation is similar to using an error feedback amplifier. A larger harmonic amplitude is seen by the hysteresis controller and therefore a greater compensation current is applied. This means that the boost converter operates at a higher mean duty cycle, which in turn increases the DC link voltage. An advantage of this is that the DC link voltage is much greater than the input voltage, allowing a larger ripple before the two intersect and input current control is lost.

The use of a notch filter to generate the input current error signal results in a harmonic reduction which is proportional rather than absolute. This is the case as the line frequency component of the input current is removed by filtering, meaning that the output signal is always a fixed proportion of the input. For example, an attenuation of 20dB will result in an output voltage which is 10% of the input. Due to this the input current harmonics will always be reduced by a constant factor, removing the need for the power control input conventionally achieved with voltage error feedback. Using standard multiplier-based APFC, the line frequency component of the input current is instead removed by subtraction of a sinusoidal reference. In order to keep the response proportional, the subtrahend must be constantly scaled by the load power (voltage error) feedback signal. The use of attenuation instead of subtraction is what fundamentally distinguishes this work from prior art and forms the most important contribution to knowledge.

8.2 Further Work

A number of useful extensions to this research have been identified, some improving on the existing work and others in related areas. The first of these is to consider the use of a three-phase motor drive load with reduced DC link capacitance (maintaining a single-phase supply). The advantage this offers is that in theory, a three-phase inverter can draw constant current from its supply when powering a balanced load. In practise there will be limitations to this, but at the very least the load will appear less dynamic, reducing the current commutation pulses which generate the majority of the harmonics with a single-phase load. A further advantage is that for an equivalent motor speed, the fundamental load frequency will be three times higher, allowing a further reduction in energy storage.

There are clearly gains to be made in using a motor drive system specifically designed to work with 100% DC link voltage ripple. In particular, a practical implementation of the conduction angle modulation scheme should demonstrate further improvements in power factor. A detailed analysis of the motor performance is required to see the overall volume and cost benefits of using reduced DC link capacitance. As this research focused more specifically on power factor correction, the penalties in terms of motor design have been inferred based on similar work by the industrial sponsor, and must therefore be treated with a degree of caution.

If reduced DC link capacitance is to be used in a power supply application, further work is required on the design of the DC to DC converter. Whilst functional and uncomplicated, the design used in this thesis was under performing in comparison with the APFC system and motor drive. Furthermore, in most applications the DC to DC converter would not be necessary, as a motor designed to work at line voltage would be used instead. The APFC system developed through this work could be used with no modification at all, as the combination of a low voltage motor and DC to DC converter presents exactly the same load as an equivalent high voltage motor.

The topic of EMI filtering was only discussed briefly in this thesis, without any formal measurement or design work taking place. For a complete power system design it will be necessary to consider the conducted and radiated emissions caused by the power device switching. As with the EN61000-3-2 harmonic standards, there are also EMI limits which must be met for compliance with EU law, the most relevant of which is EN55014-1. As mentioned in the literature review, the design and control of the boost APFC stage has a significant effect on the EMI filtering requirements.

Subsequently, determining the total size and cost of the power converter requires these two subsystems to be considered together.

The final and most direct extension of this work would be to further improve the filter-based APFC control system. It has been demonstrated that some of the notable performance limitations stem from the implementation rather than the concept itself. Whilst maintaining a low cost, the purely analogue design prevented the system response from being tuned during operation. As highlighted in the previous chapter, the fixed frequency and attenuation of the notch filter reduced the system performance when the operating conditions deviated from the nominal point. As in many applications, a move to digital control offers a number of advantages, in this case the ability to synchronise the filter and supply frequency, along with DC link voltage regulation through control of the filter attenuation. The key challenge of a digital implementation is achieving sufficient bandwidth to prevent aliasing and distortion of the current sensor signal. Given that one of the aims of this research was to reduce power converter cost, it was not viable to use a high performance digital signal processor. However, as these devices become less expensive over time, the feasibility of this approach will increase.

8.3 Closing Remarks

This work was inspired by the considerable drawbacks arising from the use of a large capacitor in AC to DC converters. It was noted that for certain loads this was not strictly required, offering a fundamentally simple solution; use a small capacitor instead. Having established this at the outset, the essence of the work lay in identifying and solving the new challenges which arose in a system with minimal decoupling. The most significant of these was the presence of load-frequency harmonics which would conventionally have been suppressed by the DC link capacitor. Through critically analysing the operation of harmonic filters, the poor energy utilisation of passive approaches were acknowledged. Subsequently, active control systems were researched to allow complete harmonic attenuation using the smallest possible amount of energy storage. A novel control system was developed to allow the attenuation of input current harmonics without relying on the DC link voltage feedback required by conventional APFC systems. The notch filter based APFC controller was successfully implemented using basic analogue components, helping to maintain a low cost in keeping with the rest of the power system.

An indication of the value of this research can be taken from the sponsor's decision to compile two patent applications; one for the notch filter based APFC controller and another for the current sensor design. Considering the demand for new technology combined with ever-stricter legislation, the need for electrical devices to have a high power density and high power factor is likely to increase. It is therefore hoped by the author that in future, the concepts proposed in this thesis may find their way into systems outside of a laboratory.

References

[1] J. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round, "Pwm converter power density barriers," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, 2007, pp. P–9 –P–29. 2

[2] I. Clelland and R. Price, "Recent advances in capacitor technology with application to high frequency power electronics and voltage conversion," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 2, Mar. 1999, pp. 685 –691 vol.2. 2, 25

[3] P. Krein, R. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *Power Electronics, IEEE Transactions on*, vol. 27, no. 11, pp. 4690–4698, 2012. 2, 21, 22, 23

[4] M. Cacciato, A. Consoli, S. De Caro, and A. Testa, "Using the dc-bus current to improve the power factor in low-cost electric drives," *Industry Applications, IEEE Transactions on*, vol. 41, no. 4, pp. 1084 – 1090, 2005. 3, 13, 26, 33

[5] G. Moschopoulos and P. Jain, "Single-phase single-stage power-factor-corrected converter topologies," *Industrial Electronics, IEEE Transactions on*, vol. 52, no. 1, pp. 23–35, 2005. 3

[6] F. DeWinter and L. Grainger, "A practical approach to solving large drive harmonic problems at the design stage," *Industry Applications, IEEE Transactions on*, vol. 26, no. 6, pp. 1095 –1101, 1990. 3

[7] IEC, *Electromagnetic compatibility (EMC). Limits. Limits for harmonic current emissions (equipment input current up to 16 A per phase)*, British Standards Std. BS EN 61 000-3-2:2006, 2006. 4, 25

[8] B.-G. Gu and K. Nam, "A dc-link capacitor minimization method through direct capacitor current control," *Industry Applications, IEEE Transactions on*, vol. 42, no. 2, pp. 573 – 581, 2006. 8, 9

[9] J. Jung, S. Lim, and K. Nam, "A feedback linearizing control scheme for a pwm converter-inverter having a very small dc-link capacitor," *Industry Applications, IEEE Transactions on*, vol. 35, no. 5, pp. 1124 –1131, 1999. 8, 9

[10] L. Malesani, L. Rossetto, P. Tenti, and P. Tomasin, "Ac/dc/ac pwm converter with reduced energy storage in the dc link," *Industry Applications, IEEE Transactions on*, vol. 31, no. 2, pp. 287 –292, 1995. 8, 9

[11] J. Kim and S. Sul, "New control scheme for ac-dc-ac converter without dc link electrolytic capacitor," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, Jun. 1993, pp. 300 –306. 8, 9

[12] Y. Minari, K. Shinohara, and R. Ueda, "Pwm-rectifier/voltage-source inverter without dc link components for induction motor drive," *Electric Power Applications, IEE Proceedings B*, vol. 140, no. 6, pp. 363 –368, Nov. 1993. 8

[13] B. Gu and K. Nam, "Theoretical minimum dc-link capacitance in pwm converter-inverter systems," *Electric Power Applications, IEE Proceedings* -, vol. 152, no. 1, pp. 81 – 88, 2005. 8

[14] R. Ottersten and J. Svensson, "Vector current controlled voltage source converter-deadbeat control and saturation strategies," *Power Electronics, IEEE Transactions on*, vol. 17, no. 2, pp. 279 –285, Mar. 2002. 9

[15] H. Andersen, R. Tan, and C. Kun, "3-phase ac-drives with passive front-ends with focus on the slim dc-link topology," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 3248 –3254. 10

[16] K. Kretschmar and H.-P. Nee, "An ac converter with a small dc link capacitor for a 15 kw permanent magnet synchronous integral motor," in *Power Electronics and Variable Speed Drives, 1998. Seventh International Conference on (Conf. Publ. No. 456)*, Sep. 1998, pp. 622 –625. 10

[17] H. Haga, I. Takahashi, and K. Ohishi, "Direct torque ipm motor control method to obtain unity power factor using a single-phase diode rectifier," in *Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, vol. 2, 2003, pp. 1078 – 1083 vol.2. 10, 11, 12, 13

[18] J. Kim, I. Jeong, K. Lee, and K. Nam, "Fluctuating current control method for a pmsm along constant torque contours," *Power Electronics, IEEE Transactions on*, vol. 29, no. 11, pp. 6064–6073, Nov 2014. 10

[19] Y. Son and J.-I. Ha, "Direct power control of three phase inverter for grid input current shaping of single phase diode rectifier with small dc link capacitor," pp. 1–1, 2014. 10, 23

[20] H.-S. Jung, S.-J. Chee, S.-K. Sul, Y.-J. Park, H.-S. Park, and W.-K. Kim, "Control of three-phase inverter for ac motor drive with small dc-link capacitor fed by single-phase ac source," *Industry Applications, IEEE Transactions on*, vol. 50, no. 2, pp. 1074–1081, March 2014. 10

[21] W. Thong and C. Pollock, "Two phase switched reluctance drive with voltage doubler and low dc link capacitance," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 3, 2005, pp. 2155 – 2159 Vol. 3. 10

[22] H. Saren, K. Rauma, and O. Pyrhonen, "Dtc driven single phase fed voltage source inverter with small dc-link capacitor," in *Industrial Electronics, 2005. ISIE 2005. Proceedings of the IEEE International Symposium on*, vol. 2, 2005, pp. 411 – 415 vol. 2. 10, 11, 12

[23] H. Lamsahel and P. Mutschler, "Permanent magnet drives with reduced dc-link capacitor for home appliances," in *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, 2009, pp. 725 –730. 10, 13

[24] L.-R. Chen, S.-L. Wu, D.-T. Shieh, and T.-R. Chen, "Sinusoidal-ripple-current charging strategy and optimal charging frequency study for li-ion batteries," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 1, pp. 88–97, 2013. 13

[25] M. Uno and K. Tanaka, "Influence of high-frequency charge discharge cycling induced by cell voltage equalizers on the life performance of lithium-ion cells," *Vehicular Technology, IEEE Transactions on*, vol. 60, no. 4, pp. 1505–1515, 2011. 13

[26] S. Bala, T. Tengner, P. Rosenfeld, and F. Delince, "The effect of low frequency current ripple on the performance of a lithium iron phosphate (lfp) battery energy storage system," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, 2012, pp. 3485–3492. 13

[27] M. Rosekeit and R. De Doncker, "Smoothing power ripple in single phase chargers at minimized dc-link capacitance," in *Power Electronics and ECCE Asia*

(ICPE ECCE), 2011 IEEE 8th International Conference on, 2011, pp. 2699–2703. 14, 15, 16

[28] L. Xue, D. Diaz, Z. Shen, F. Luo, P. Mattavelli, and D. Boroyevich, "Dual active bridge based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 1920–1925. 14, 15, 64

[29] K. Yao, M. Xu, X. Ruan, and L. Gu, "Boost-flyback single-stage pfc converter with large dc bus voltage ripple," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 1867–1871. 16, 17

[30] L. Gu, X. Ruan, M. Xu, and K. Yao, "Means of eliminating electrolytic capacitor in ac/dc power supplies for led lightings," *Power Electronics, IEEE Transactions on*, vol. 24, no. 5, pp. 1399–1408, 2009. 16, 17, 19, 20

[31] H. Ma, W. Yu, C. Zheng, J.-S. Lai, Q. Feng, and B.-Y. Chen, "A universal-input high-power-factor pfc pre-regulator without electrolytic capacitor for pwm dimming led lighting application," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, 2011, pp. 2288–2295. 16, 17

[32] W. Chen and S. Hui, "Elimination of an electrolytic capacitor in ac/dc light-emitting diode (led) driver with high input power factor and constant output current," *Power Electronics, IEEE Transactions on*, vol. 27, no. 3, pp. 1598–1607, 2012. 16, 17

[33] *A Review of the Literature on Light Flicker: Ergonomics, Biological Attributes, Potential Health Effects, and Methods in Which Some LED Lighting May Introduce Flicker*, IEEE Std. P1789, 2010. [Online]. Available: http://grouper.ieee.org/groups/1789/ 17

[34] A. Kyritsis, N. Papanikolaou, and E. Tatakis, "A novel parallel active filter for current pulsation smoothing on single stage grid-connected ac-pv modules," in *Power Electronics and Applications, 2007 European Conference on*, 2007, pp. 1–10. 21, 22

[35] H. Wang, H.-H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the dc-link capacitance in a capacitor-supported system," *Power*

Electronics, IEEE Transactions on, vol. 29, no. 3, pp. 1163–1175, March 2014. 21

[36] R. Wang, F. Wang, D. Boroyevich, R. Burgos, R. Lai, P. Ning, and K. Rajashekara, "A high power density single-phase pwm rectifier with active ripple energy storage," *Power Electronics, IEEE Transactions on*, vol. 26, no. 5, pp. 1430–1443, 2011. 21, 22, 23

[37] R. Wang, F. Wang, R. Lai, P. Ning, R. Burgos, and D. Boroyevich, "Study of energy storage capacitor reduction for single phase pwm rectifier," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, 2009, pp. 1177–1183. 21, 22

[38] G. Buiatti, S. Cruz, and A. Cardoso, "Lifetime of film capacitors in single-phase regenerative induction motor drives," in *Diagnostics for Electric Machines, Power Electronics and Drives, 2007. SDEMPED 2007. IEEE International Symposium on*, 2007, pp. 356 –362. 23

[39] Epcos, *Film Capacitors - General Technical Information.*, Epcos AG, 2009. 24

[40] J.-S. Lai, H. Kouns, and J. Bond, "A low-inductance dc bus capacitor for high power traction motor drive inverters," in *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, vol. 2, 2002, pp. 955 – 962 vol.2. 24

[41] R. Grinberg and P. Palmer, "Advanced dc link capacitor technology application for a stiff voltage-source inverter," in *Vehicle Power and Propulsion, 2005 IEEE Conference*, 2005, p. 6 pp. 24

[42] Panasonic, *NHG Electrolytic Capacitor Datasheet*, 2009. 24

[43] (2009) Key product criteria for energy star qualified computers. [Online]. Available: http://www.energystar.gov/ 25

[44] B. Singh and S. Singh, "Single-phase power factor controller topologies for permanent magnet brushless dc motor drives," *Power Electronics, IET*, vol. 3, no. 2, pp. 147–175, 2010. 26

[45] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *Power Electronics, IEEE Transactions on*, vol. 18, no. 3, pp. 749–755, 2003. 26, 31

[46] P. Todd, "Uc3854 controlled power factor correction circuit design application note," Unitrode/Texas Instruments, Tech. Rep., 1999. 29, 30, 110, 115

[47] Y.-T. Feng, G.-L. Tsai, and Y.-Y. Tzou, "Digital control of a single-stage single-switch flyback pfc ac/dc converter with fast dynamic response," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, vol. 2, 2001, pp. 1251–1256 vol.2. 30

[48] J. Williams, "Design of feedback loop in unity power factor ac to dc converter," in *Power Electronics Specialists Conference, 1989. PESC '89 Record., 20th Annual IEEE*, 1989, pp. 959–967 vol.2. 30

[49] B. Singh, B. Singh, and S. Dwivedi, "Performance comparison of high frequency isolated ac-dc converters for power quality improvement at input ac mains," in *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, 2006, pp. 1–6. 31

[50] L. Caruso, A. Consoli, G. Scarcella, and A. Testa, "A switched reluctance motor drive operating at unity power factor," in *Industry Applications Conference, 1996. Thirty-First IAS Annual Meeting, IAS '96., Conference Record of the 1996 IEEE*, vol. 1, 1996, pp. 410–417 vol.1. 31

[51] D. Maksimovic, Y. Jang, and R. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *Power Electronics, IEEE Transactions on*, vol. 11, no. 4, pp. 578–584, 1996. 31

[52] J. Rajagopalan, F. Lee, and P. Nora, "A general technique for derivation of average current mode control laws for single-phase power-factor-correction circuits without input voltage sensing," *Power Electronics, IEEE Transactions on*, vol. 14, no. 4, pp. 663–672, 1999. 31

[53] T. Ohnishi and M. Hojo, "Dc voltage sensorless single-phase pfc converter," *Power Electronics, IEEE Transactions on*, vol. 19, no. 2, pp. 404–410, 2004. 31

[54] O. Garcia, J. Cobos, R. Prieto, P. Alou, and J. Uceda, "Simple ac/dc converters to meet iec 1000-3-2," in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, vol. 1, 2000, pp. 487–493 vol.1. 32

[55] T.-S. Kim, G.-B. Koo, G.-W. Moon, and M.-J. Youn, "A single-stage power factor correction ac/dc converter based on zero voltage switching full bridge topology with two series-connected transformers," *Power Electronics, IEEE Transactions on*, vol. 21, no. 1, pp. 89 – 97, jan. 2006. 32

[56] S. Li and G. Moschopoulos, "A simple ac-dc pwm full-bridge converter with auxiliary transformer winding," in *Telecommunications Energy Conference, 2003. INTELEC '03. The 25th International*, oct. 2003, pp. 216 –223. 32

[57] G. Moschopoulos, "A simple ac-dc pwm full-bridge converter with integrated power-factor correction," *Industrial Electronics, IEEE Transactions on*, vol. 50, no. 6, pp. 1290 – 1297, dec. 2003. 32, 33

[58] M. Qiu, G. Moschopoulos, H. Pinheiro, and P. Jain, "Analysis and design of a single stage power factor corrected full-bridge converter," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual*, vol. 1, mar 1999, pp. 119 –125 vol.1. 32

[59] L. Rossetto, G. Spiazzi, and P. Tenti, "Boost pfc with 100-hz switching frequency providing output voltage stabilization and compliance with emc standards," *Industry Applications, IEEE Transactions on*, vol. 36, no. 1, pp. 188–193, 2000. 32

[60] T. Ninomiya, C. feng Jin, M. Shoyama, and T. Ohmae, "Line-harmonics reduction techniques for consumer electronics and low-power electronic equipment," in *Industrial Electronics Society, 2000. IECON 2000. 26th Annual Confjerence of the IEEE*, vol. 2, 2000, pp. 766–770 vol.2. 32

[61] S. Kim and P. Enjeti, "A parallel-connected single phase power factor correction approach with improved efficiency," in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, vol. 1, 2002, pp. 263–269 vol.1. 32

[62] L. Rossetto and S. Buso, "Single-phase ac/dc integrated pwm converter," in *Telecommunications Energy Conference, 2000. INTELEC. Twenty-second International*, 2000, pp. 411 –418. 32, 33

[63] H. Li-Jun, Y. Yue-feng, S. Bin, L. Zheng-yu, and Q. Zhao-ming, "A fully digital controlled 3kw, single-stage power factor correction converter based on full-bridge topology," in *Power Electronics and Motion Control Conference, 2006. IPEMC 2006. CES/IEEE 5th International*, vol. 1, aug. 2006, pp. 1 –5. 32

[64] B. Lu, W. Dong, S. Wang, and F. Lee, "High frequency investigation of single-switch ccm power factor correction converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 3, 2004, pp. 1481 – 1487 Vol.3. 34

[65] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost pfc," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 7, pp. 2574–2587, 2009. 34

[66] Z. Yan and G. Zhu, "Voltage ripple across the capacitor in dc side of shunt apf," in *Power System Technology (POWERCON), 2012 IEEE International Conference on*, 2012, pp. 1–6. 34

[67] I. Colak, R. Bayindir, E. Irmak, and O. Kaplan, "A comparative study of harmonic extraction methods for single phase shunt active power filter," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2011 International Conference on*, 2011, pp. 1–4. 34, 35

[68] L. Meng, L. Changxu, Z. Kai, and C. Xiaoming, "A kind of single-phase active power filter based on the principle of power balance," in *Computer Science and Information Processing (CSIP), 2012 International Conference on*, 2012, pp. 557–561. 34

[69] Y. Wang, J. Li, and J. Yu, "Comprehensive analysis and design for one-cycle controlled dc side apf," in *Industrial Technology, 2006. ICIT 2006. IEEE International Conference on*, 2006, pp. 750–755. 35

[70] K. Smith, "Power supply quality in brushless drives," Ph.D. dissertation, Newcastle University, 2011. 36, 111

[71] M. E. Leaver, B. Mecrow, A. Jack, A. Steven, and K. E. Austin, "High-speed drives for mass market products," in *Power Electronics, Machines and Drives, 2006. The 3rd IET International Conference on*, 2006, pp. 586–590. 42

[72] M. K. Kazimierczuk, *High-Frequency Magnetic Components*. John Wiley & Sons Ltd, 2009. 50, 59

[73] L. Balough, C. Bridge, and B. Andreycak, "Unique cascaded power converter topology for high current low output voltage applications," in *SEM-1300 Power Supply Design Seminar, Unitrode Corporation*, 2000. 52, 53, 54, 55, 58

[74] L. Huber and M. Jovanovic, "A design approach for server power supplies for networking applications," in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, vol. 2, 2000, pp. 1163 –1169 vol.2. 52

[75] Q. Zhao and F. Lee, "High-efficiency, high step-up dc-dc converters," *Power Electronics, IEEE Transactions on*, vol. 18, no. 1, pp. 65 – 73, Jan. 2003. 52

[76] S. Park and T. Jahns, "A self-boost charge pump topology for a gate drive high-side power supply," *Power Electronics, IEEE Transactions on*, vol. 20, no. 2, pp. 300 – 307, 2005. 53

[77] R. Petkov, "Optimum design of a high-power, high-frequency transformer," *Power Electronics, IEEE Transactions on*, vol. 11, no. 1, pp. 33 –42, Jan. 1996. 54

[78] M. Sayani, R. White, D. Nason, and W. Taylor, "Isolated feedback for off-line switching power supplies with primary-side control," in *Applied Power Electronics Conference and Exposition, 1988. APEC '88. Conference Proceedings 1988., Third Annual IEEE*, Feb. 1988, pp. 203 –211. 55

[79] N. Mohan, T. Undeland, and W. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley & Sons Ltd, 2003. 56, 57, 63

[80] S. Maniktala, *Switching Power Supply Design and Optimization.* McGraw-Hill, 2004. 57

[81] Z. Ouyang, O. Thomsen, and M. Andersen, "Optimal design and tradeoffs analysis for planar transformer in high power dc-dc converters," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 3166 –3173. 59

[82] J. Cobos, O. Garcia, J. Uceda, J. Sebastian, A. Martinez, and J. Arau, "Compact ac/dc converter with low output voltage (3.3 v) and power factor correction," in *Power Electronics Congress, 1995. Technical Proceedings. CIEP 95., IV IEEE International*, Oct. 1995, pp. 8 –13. 63

[83] Z. Shen, Y. Xiong, X. Cheng, Y. Fu, and P. Kumar, "Power mosfet switching loss analysis: A new insight," in *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE*, vol. 3, Oct 2006, pp. 1438–1442. 100

[84] CENELEC, *Voltage characteristics of electricity supplied by public electricity networks*, CENELEC Std., 2010. 166