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Series Capacitor Compensated AC Filterless Flexible LCC HVDC with Enhanced Power Transfer under Unbalanced Faults

Ying Xue, *Member, IEEE*, Xiao-Ping Zhang, *Senior Member, IEEE*, and Conghuan Yang

***Abstract*—This paper introduces significant performance enhancements to the AC filterless LCC HVDC [1] by including fixed series capacitors at primary side of converter transformer. In terms of technical performance, 1）the amount of active power that can be transmitted is increased by more than 60% compared with AC filterless LCC HVDC, especially under severe unbalanced fault such as single-phase fault (most common fault in power systems); 2）the required voltage level of the controllable capacitor for Commutation Failure (CF) elimination is reduced by more than 70%, which leads to considerable reductions of the associated costs and losses. In terms of economic performance, due to the reduction of the required voltage from controllable capacitors (hence the number of power electronic devices), the cost of the proposed converter station is lower than that of the AC filterless LCC HVDC. Theoretical analysis is presented to illustrate the performance enhancements and select the size of the series capacitor. Simulation results for various kinds of faults and cost analysis are presented to validate the technical and economic performances of the proposed method. Comparisons are made with AC filterless LCC HVDC. Finally various practical issues and possible solutions are discussed.**

***Index Terms*—HVDC, LCC HVDC, Flexible LCC HVDC, commutation failure, active power transfer, energy storage.**

I. Introduction

The adverse impacts of Commutation Failure (CF) on power system are originated from the resulting disruption or cessation of active power transfer of LCC HVDC link [2, 3]. For CF that does not cause converter blocking, the transient reduction of transferred active power leads to frequency fluctuations. For CF that causes converter blocking, 1) the cessation of active power transfer can lead to considerable supply and demand mismatch of the AC system at the inverter side. This could then result in reserve activation at the inverter side and tripping of generators at the rectifier side [2]; 2) the transfer of active power to the parallel AC lines can cause overloading problem to those AC lines [3] and even trigger cascaded protection tripping. One of the severe consequences of such cascaded tripping is partial blackout of the AC system. As more LCC HVDC links are being built, the above adverse impacts are posing significant challenges to the power system.

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Therefore in addition to the elimination of CF, it is of practical and fundamental importance that the amount of active power transfer through a LCC HVDC link can be increased under transient conditions, so that the adverse impacts on the AC system can be minimized. In particular this should be achieved for unbalanced fault such as single-phase fault as it is the most frequent type of fault in power system, and is also more likely to cause CF than balanced faults [4-6]. Moreover, it would certainly be attractive that such performance improvement can be achieved with lower investment costs.

Most of the previous research has been focusing on the mitigation or elimination of CF while there is a lack of focus on increasing the active power transfer during fault (which is the main reason that CF is causing concerns for power system operation). In fact, some of the proposed methods may lead to a reduced active power transfer. For example, advancement of inverter firing angle [7, 8] and reduction of rectifier DC current [9] after fault detection both result in a lower DC power. This is understandable as a higher DC current or a higher DC voltage (both contribute to higher DC power transfer) is not favorable for the success of commutations. Recently, reference [10] proposed a method to use DC voltage control at rectifier side together with inverter DC current control to increase the short-term power transfer capability of LCC HVDC. The method works by estimating the DC voltage reference (using the DC power reference at inverter side) and transmitting it to rectifier side through telecommunication links. However the method is focusing on allowing the HVDC link to respond to higher DC power reference rather than improving the power transfer capability during fault conditions.

Some other research that relates to the control of DC power has been focusing on the frequency control using LCC HVDC [11-13]. The idea is to add a contribution proportional to the instantaneous frequency deviation to the power or current order of the LCC HVDC. It enables wind farms or interconnected AC systems to participate in the primary frequency control of the AC system at the other end. However, the active power transfer under inverter fault condition is not considered.

This paper, based on the AC filterless LCC HVDC [1], presents a further major development of increasing the amount of active power transfer during faults, and at the same time to reduce the cost of the scheme. It will be shown in the rest of the paper that the new development can be achieved by including fixed series capacitors at the primary side of converter

transformer. It should be mentioned that although the idea of adding series capacitors at primary side of converter transformer was already discussed in [1], it cannot achieve the same performances as those achieved with the proposed method. In other words, it is the combination of controllable capacitors, parallel capacitors and series capacitors that achieves the aforementioned superior performances.

The rest of the paper is organized as follows. Section II presents the topology of the proposed method. Theoretical analysis is presented in Section III to explain the benefits of adding series capacitors. Section IV, based on the theoretical analysis in Section III, selects the capacitance of series capacitors and estimates the required voltage level from controllable capacitors for CF elimination. Then calculations are carried out on the level of active power increase during faults. In Section V, simulation studies and cost analysis in comparison with AC filterless LCC HVDC are carried out to validate the technical and economic performance of the proposed method. Finally the potential issue and solutions of ferrorresonance are discussed. Section VI concludes the paper.

II. Proposed Circuit Configuration

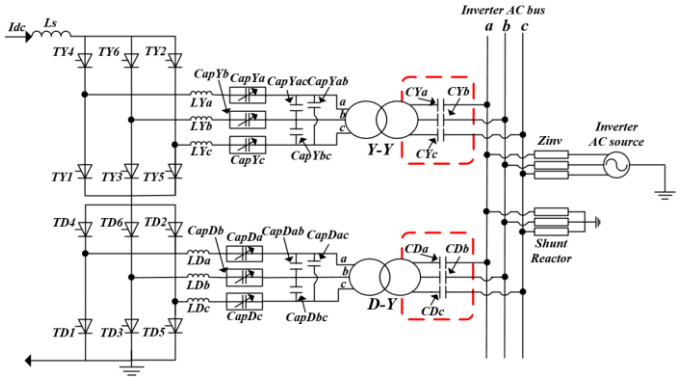


Fig. 1. Circuit configuration of the proposed system.

Fig. 1 shows the circuit configuration of the proposed system based on the CIGRE benchmark model [14] where I_{dc} is the DC current; *TY(D)1-TY(D)6* are thyristor valves; *LY(D)a-LY(D)c* and *CapY(D)a-CapY(D)c* are current limiting inductors and controllable capacitors respectively; *CapY(D)ab*, *CapY(D)bc* and *CapY(D)ac* are parallel capacitors; *CY(D)a-CY(D)c* are series capacitors; Z_{inv} is the AC system impedance. The commonly adopted grounding conditions for 12-pulse schemes are applied [15]: the Y-Y converter transformer is grounded at grid side and un-grounded at valve side; the Y-Δ converter transformer is grounded at grid side. Shunt reactor may be needed to absorb the extra reactive power generated by the parallel and series capacitors. The main difference between the proposed method and the AC filterless LCC HVDC is that fixed series capacitors are installed at the primary side of converter transformer.

The main contributions of this paper are:

1. System Topology: The system topology is new compared with any of the previously proposed HVDC systems. It needs to be pointed out that although the idea of including series capacitor at primary side of converter transformer has been studied in [16], the method proposed in this paper is not only different in terms of system topology, but also fundamentally different in terms of operating principles and system characteristics, and significantly better in terms of system performance especially under unbalanced fault conditions.
2. Technical performance: The significant increase of active power transfer during unbalanced fault cannot be achieved with any of the existing method. This improvement is of significance to power system considering that around 95% of the faults in power systems are unbalanced faults [17] and most of the CFs are caused by unbalanced faults [6].
3. Economic performance: The significant technical performance improvements are achieved with much lower voltage rating of controllable capacitors. This leads to considerable reductions of equipment cost and capitalized cost of losses, which largely increase the applicability of the proposed method.
4. Theoretical development: The above performance improvements have been theoretically explained in detail in this paper. The theoretical development provides a valuable insight into this new type of HVDC system.

In theory, the controllable capacitors can be employed to realize the enhancement of active power transfer during fault. This can be achieved by increasing the amount of time that the controllable capacitors are inserted during fault to reduce the drop of DC voltage, hence increasing the active power transfer. However this would cause large variations of capacitor voltage due to the high fault current, and the potential overvoltage of capacitors is undesirable. This problem can be mitigated by considerably increasing the voltage rating of controllable capacitors (i.e., adding more capacitor submodules) but would increase the investment cost and losses of the HVDC scheme. Therefore it is not economical to employ controllable capacitors to improve the active power transfer during fault.

In contrast, as will be shown in this paper, 1) the fixed series capacitor can provide commutation voltage that depends on the level of fault current (i.e., the higher the fault current the larger the actual commutation voltage); 2) the series capacitor delays the actual commutation voltage during fault. The first characteristic helps reduce the drop of DC voltage, and the second characteristic reduces the required level of voltage insertion from controllable capacitors. Further considering the much lower cost, lower losses and mature technology of series capacitor compared with controllable capacitors, the choice of using series capacitor is techno-economically more favorable.

III. Theoretical Analysis

This section consists of two parts. The first part analyzes the impact of series capacitors on the performance of converter. The derived relationships will be used in Section IV to 1) select the capacitance of series capacitors and 2) estimate the required voltage level of controllable capacitors for CF elimination. The second part, based on the results from the first part, illustrates how the level of active power transfer during faults can be increased with the help of series capacitors.

A. Circuit Analysis

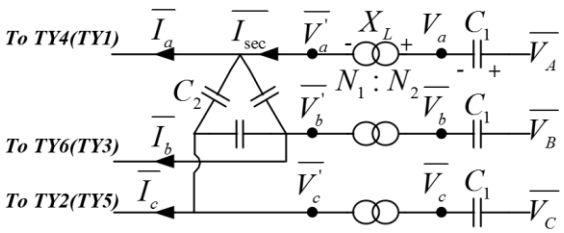
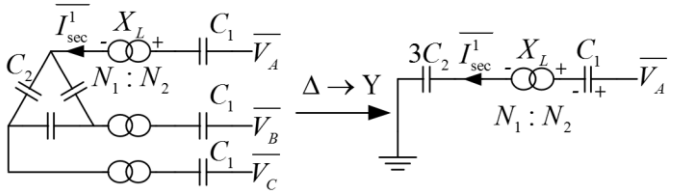


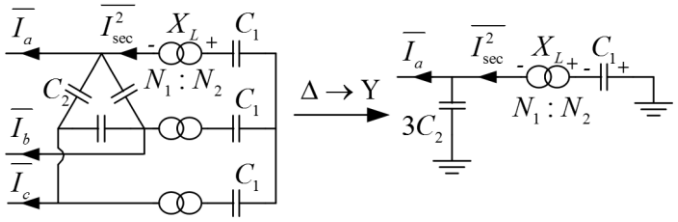
Fig. 2. Equivalent circuit.

Fig. 2 shows the equivalent circuit for analysis. Only the fundamental frequency is considered in the following discussion as harmonics are filtered out by the parallel capacitors [1]. The controllable capacitors are not considered at this stage as they do not affect the electrical variables that need to be analyzed. In Fig. 2, $\overline{I_a}$, $\overline{I_b}$, $\overline{I_c}$ are the phasor values of line currents in phase A, phase B and phase C at valve side; $\overline{I_{\text{sec}}}$ is the phasor value of phase A line current at the secondary side of converter transformer; X_L is the reactance of converter transformer; $\overline{V_a'}$, $\overline{V_b'}$, $\overline{V_c'}$ are the phasor values of phase voltages at secondary side of converter transformer; *N1:N2* is the turns ratio of converter transformer; $\overline{V_a}$, $\overline{V_b}$, $\overline{V_c}$ are the phasor values of three phase voltages between series capacitor and converter transformer; $\overline{V_A}$, $\overline{V_B}$, $\overline{V_C}$ are the three phase voltages at inverter AC bus; C_1 and C_2 are the capacitances of series and parallel capacitors. The positive polarities of voltages across series capacitors and transformer reactance are also shown in the figure. The inputs to the circuit shown in Fig. 2 are the current injections from valve side ($\overline{I_a}$, $\overline{I_b}$, $\overline{I_c}$) and grid voltages ($\overline{V_A}$, $\overline{V_B}$, $\overline{V_C}$). The rest of the electrical variables can be obtained by calculating the contribution from each of the two inputs. For the sake of simplicity, phase A is considered in the following calculations. Phasor diagrams will be drawn to visualize the relationships between electrical variables and to highlight the impact from series capacitor.

Fig. 3(a) and Fig. 3(b) show the equivalent three-phase and single-phase circuits for calculating the contribution to $\overline{I_{\text{sec}}}$ from inverter AC bus voltage ($\overline{I_{\text{sec}}^1}$) and valve side current injection ($\overline{I_{\text{sec}}^2}$), respectively. The delta-star transformation is applied to obtain the equivalent single-phase circuit where the system is assumed to be under steady-state balanced condition.



(a) Contribution from the inverter AC bus voltage



(b) Contribution from the valve side current injection

Fig. 3. Equivalent circuits for calculating I_{sec}.

From Fig. 3(a), the contribution from the inverter AC voltage can be calculated as

$$\overline{I_{\text{sec}}^1} = \frac{\overline{V_A} \times (N_1/N_2)}{jX_L + 1/(3j\omega C_2) + (1/j\omega C_1) \times (N_1/N_2)^2} \tag{1}$$

where ω is the AC system angular frequency.

From Fig. 3(b), the contribution from the valve side current injection can be calculated as

$$\overline{I_{\text{sec}}^2} = \overline{I_a} \times \frac{1/(3j\omega C_2)}{jX_L + 1/(3j\omega C_2) + (1/j\omega C_1) \times (N_1/N_2)^2} \tag{2}$$

Then $\overline{I_{\text{sec}}}$ can be obtained as

$$\overline{I_{\text{sec}}} = \overline{I_{\text{sec}}^1} + \overline{I_{\text{sec}}^2} \tag{3}$$

With the calculated $\overline{I_{\text{sec}}}$, the voltage across the series capacitor ($\overline{V_{C_1}}$) and the voltage across the transformer reactance ($\overline{V_{X_L}}$) can be calculated as

$$\overline{V_{C_1}} = \overline{I_{\text{sec}}} \times (N_1/N_2) \times (1/j\omega C_1) \tag{4}$$

$$\overline{V_{X_L}} = \overline{I_{\text{sec}}} \times jX_L \tag{5}$$

Finally the voltages at the primary and secondary side of converter transformer can be obtained:

$$\overline{V_a} = \overline{V_A} - \overline{V_{C_1}} \tag{6}$$

$$\overline{V_a'} = \overline{V_a} \times (N_1/N_2) - \overline{V_{X_L}} \tag{7}$$

The above relationships can be graphically illustrated using the phasor diagrams as shown in Fig. 4. The phasor diagrams for both the proposed method and the AC filterless LCC HVDC are shown for comparison. It can be seen from Fig. 4 that for the proposed method, $\overline{I_a}$ is lagging $\overline{V_A}$ by approximately the firing angle α (the overlap angle is small with parallel capacitors). This is because according to the operation of converter, the firing of thyristor valves effectively delays the line current at valve side by approximately the value of firing angle with respect to the grid side reference voltage [18]. Then according to (1) and (2) and using the system parameters of 10μF for C_1 [1] and 13.45 Ω for X_L [14], $\overline{I_{\text{sec}}^1}$ is calculated to be leading $\overline{V_A}$ by 90^0, and $\overline{I_{\text{sec}}^2}$ to be in phase with $\overline{I_a}$. Therefore, as shown in Fig. 4, $\overline{I_{\text{sec}}}$ (phasor summation of $\overline{I_{\text{sec}}^1}$ and $\overline{I_{\text{sec}}^2}$) for the proposed method is lagging $\overline{I_a}$ by an angle of θ. The voltage of $\overline{V_a}$ is lagging $\overline{V_A}$ by β due to the voltage across series capacitor ($\overline{V_{C_1}}$). $\overline{V_a}$ is then advanced by an angle of γ to get $\overline{V_a'}$ due to the voltage drop over the transformer reactance ($\overline{V_{X_L}}$).

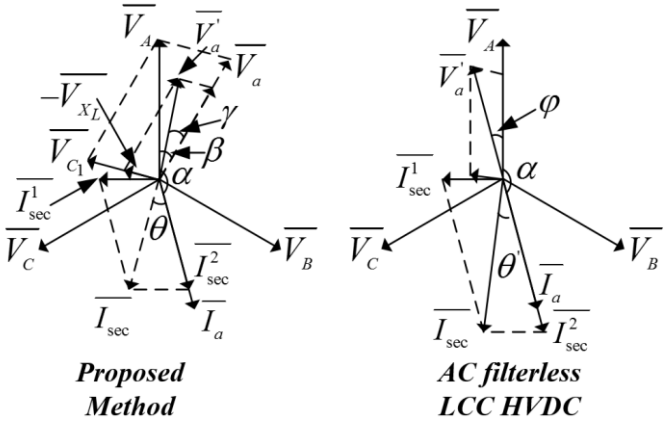


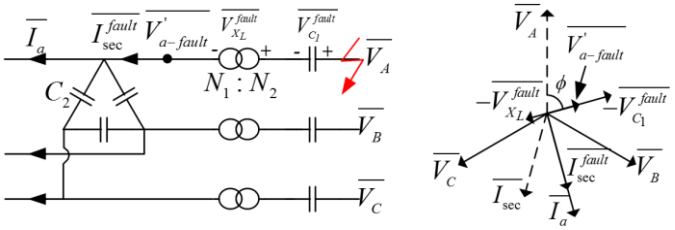
Fig. 4. Phasor diagrams of the electrical variables in the proposed method and AC filterless LCC HVDC.

By comparing the phasor diagram of the proposed method with that of the AC filterless LCC HVDC, it can be observed that the series capacitor affects the converter performance from two main aspects. Firstly, it reduces the magnitude of $\overline{I_{\text{sec}}^2}$. This is beneficial as it leads to a smaller current that flows into the converter transformer (therefore lower power losses). At the same time, it increases the phase difference between $\overline{I_{\text{sec}}}$ and $\overline{I_a}$ (θ is larger than θ'). Secondly, $\overline{V_a'}$ is lagging $\overline{V_A}$ for the proposed method while it is leading $\overline{V_A}$ by φ for the system without series capacitor. This phase lag is advantageous to commutation as it provides an increased commutation margin. As will be demonstrated in the following subsection, it is even more beneficial to commutation under fault conditions due to the fact that the commutation margin becomes even larger.

B. Single-Phase Fault

Zero impedance single-phase (phase A) fault is considered in this section to illustrate how the series capacitor can increase the level of active power transfer during fault. To simplify the analysis, DC current is assumed to be controlled at the rated value during fault (which will be demonstrated through simulation results in Section V), and phase B and phase C voltages are maintained at the pre-fault values.

It is important to point out that the actual commutation voltages in the proposed method are no longer the line-to-line voltages at inverter AC bus, but the line-to-line voltages at secondary side of the converter transformer (e.g., $\overline{V_a'} - \overline{V_b'}$). As a result, the commutation overlap angle is now determined by the current limiting inductor rather than the equivalent inductor from converter transformer.



(a) Equivalent circuit (b) Phasor diagram

Fig. 5. Equivalent circuit and phasor diagram during phase A fault.

Fig. 5 shows the equivalent circuit and the corresponding phasor diagram under phase A fault where $\overline{I_{\text{sec}}^{fault}}$ is the phase A line current at the secondary side of the converter transformer; $\overline{V_{X_L}^{fault}}$ and $\overline{V_{C_1}^{fault}}$ are the voltages across the transformer reactance and series capacitor; $\overline{V_{a-fault}'}$ is the phase A voltage at the secondary side of the converter transformer. Because of the fault, $\overline{V_A}$ is dropped to zero and therefore its contribution to $\overline{I_{\text{sec}}}$ is also reduced to zero. So $\overline{I_{\text{sec}}^{fault}}$ only has the contribution from $\overline{I_a}$, i.e.,

$$\overline{I_{\text{sec}}^{fault}} = \overline{I_{\text{sec}}^2} \tag{8}$$

and it is in phase with $\overline{I_a}$ (Fig. 5(b)) as discussed in last subsection. So the contribution to actual commutation voltage from phase A during fault can be calculated as

$$\overline{V_{a-fault}'} = -\overline{V_{C_1}^{fault}} \times \left(N_1/N_2\right) - \overline{V_{X_L}^{fault}} \tag{9}$$

which is shown in Fig. 5(b). $\overline{V_{a-fault}'}$ is lagging $\overline{V_A}$ by an angle ϕ that is calculated as:

$$\phi = \alpha - 90^0 \tag{10}$$

By comparing Fig. 5 with Fig. 4, the following observations can be made:

- The phase lag of the actual commutation voltage during fault is larger than that under the normal operating condition. This characteristic is particularly beneficial as a larger commutation margin is critically needed to counteract the unfavorable advancement of voltage zero crossing point due to unbalanced faults. It leads to significant reduction of the required insertion voltage from the controllable capacitor.
- The contribution to actual commutation voltage from phase A ($\overline{V_{a-fault}'}$) is nonzero even though the inverter bus voltage drops to zero. This means that the drop of DC voltage is decreased, which in turn increases the amount of active power transfer during the fault. In other words, the installation of the series capacitor minimizes the impact of the AC fault on the DC side. An added benefit is that the actual commutation voltage will be automatically increased with higher fault current, and therefore further minimizes the adverse impact on the DC system.

The average DC voltage during the fault can be calculated with reference to Fig. 6 which shows the waveforms of commutation voltages during fault.

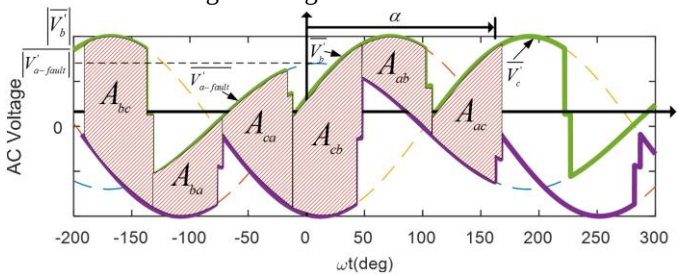


Fig. 6. Inverter AC voltages and commutation process.

The three-phase inverter AC voltages that are used to obtain the actual firing instants are defined as:

$$V_A = V_m \cos(\omega t + 60^0)$$
$$V_B = V_m \cos(\omega t - 60^0) \quad (11)$$
$$V_C = V_m \cos(\omega t - 180^0)$$

where V_m is the voltage magnitude. As previously discussed, under phase A fault, the phase lags occurred on the actual commutation voltages of phase A, phase B and phase C are ϕ, $\beta-\gamma$ and $\beta-\gamma$, respectively. So the average DC voltage can be calculated as:

$$V_{dc}^{fault} = \left(A_{ac} + A_{ab} + A_{ba} + A_{bc} + A_{ca} + A_{cb}\right)/2\pi \quad (12)$$

where A_{ac}, A_{ab}, A_{ba}, A_{bc}, A_{ca}, A_{cb} are the voltage-time areas during fault as shown in Fig. 6 and are calculated as (short overlap angles are not considered for simplicity):

$$A_{ac} = A_{ca} = \int_{-60^0+\alpha}^{\alpha} \left(\overline{V_{a-fault}^{'}} \cos(\omega t + 60^0 - \phi)\right) d\omega t - \int_{-60^0+\alpha}^{\alpha} \left(\left|\overline{V_c^{'}}\right| \cos(\omega t - 180^0 - \beta + \gamma)\right) d\omega t \quad (13)$$

$$A_{ab} = A_{ba} = \int_{-120^0+\alpha}^{-60^0+\alpha} \left(\overline{V_{a-fault}^{'}} \cos(\omega t + 60^0 - \phi)\right) d\omega t - \int_{-120^0+\alpha}^{-60^0+\alpha} \left(\left|\overline{V_b^{'}}\right| \cos(\omega t - 60^0 - \beta + \gamma)\right) d\omega t \quad (14)$$

$$A_{cb} = A_{bc} = \int_{-180^0+\alpha}^{-120^0+\alpha} \left(\left|\overline{V_c^{'}}\right| \cos(\omega t - 180^0 - \beta + \gamma)\right) d\omega t - \int_{-180^0+\alpha}^{-120^0+\alpha} \left(\left|\overline{V_b^{'}}\right| \cos(\omega t - 60^0 - \beta + \gamma)\right) d\omega t \quad (15)$$

These equations will be used in next section to estimate the level of active power that can be transmitted during single-phase fault.

IV. Parameter Selection & Required Voltage Level from Controllable Capacitor

There are two parameters that need to be determined for the proposed system. The first is the capacitance of the series capacitor and the second is the required voltage level of the controllable capacitor. The selection of both parameters is discussed in this section. In addition, the amount of power that can be transmitted during single-phase fault is calculated.

A. Capacitance of Series Capacitor

The following four aspects are considered for the selection of capacitance for the series capacitor:

- Magnitude of line current as calculated in (3). This is because a smaller line current indicates lower transformer losses.
- Voltage magnitude of series capacitor as calculated in (4). This is because the minimum protective level of series capacitor is directly determined by the maximum steady-state voltage across the capacitor [19]. So a lower voltage across the capacitor can potentially reduce its protective level, thereby reducing the number of Metal Oxide Varistor (MOV) blocks that are connected in series, leading to cost savings [20].
- Reactive power generation from the series capacitor. This is because the cost of series capacitor is directly related to the rating (reactive power generation) of the capacitor [21].
- *LC* resonance between series capacitor and transformer leakage reactance. The resonant frequency needs to be away from the fundamental frequency of the AC system so it will not adversely affect the actual commutation voltage.

The magnitude of line current ($\overline{I_{\text{sec}}}$) is used to quantitatively select the series capacitor. The selection criterion is that the addition of series capacitor does not increase the steady-state line current compared with the HVDC system without parallel and series capacitors. This is because an increased line current is undesirable as it not only require a larger transformer (higher cost), but also increase the transformer losses. Mathematically the above criterion can be expressed as:

$$\left|\overline{I_{\text{sec}}^1} + \overline{I_{\text{sec}}^2}\right| \le I_{\text{sec}}^0 \quad (16)$$

where I_{sec}^0 is the RMS value of the rated secondary side line current in the Benchmark system. By solving (16) together with (1)-(3) using the parallel capacitance of 10μF [1], the range of series capacitance that meets the criterion can be calculated as

$$C_1 \le 109\mu F \quad (17)$$

Therefore, as an example, the capacitance of 100μF is selected for C_1 in this paper for the simulation studies. By substituting it back to (3), the magnitude of $\overline{I_{\text{sec}}}$ is calculated to be 2.092kA.

According to the analysis in Section III, the reactive power from the series capacitor is

$$Q_{C_1} = \left(\left|\overline{I_{\text{sec}}}\right| \times \left(N_1/N_2\right)\right)^2 \Big/ \left(\omega C_1\right) \quad (18)$$

which is 59MVar with the selected value of C_1.

It is then important to make sure that the *LC* resonant frequency between series capacitor and transformer reactance is away from the fundamental AC system frequency. With the selected capacitance of C_1, the *LC* resonant frequency is 1.41 times the fundamental frequency of the AC system. This is similar to that in [16] and [22] where the *LC* resonant frequencies are 1.45 and 1.42 times the fundamental frequency of the AC system. Simulation studies from both [16] and [22] show that the series capacitors with the above natural *LC* resonant frequencies do not adversely affect the commutations. The only problem that has been observed is the ferroresonance which can be successfully de-tuned by bypassing the capacitor units [16] or by modifying the inverter controller [22]. For the proposed method, although no adverse impact from the selection of C_1 has been observed, the two methods mentioned above can be adopted upon detection of resonance. Alternatively, the series capacitance can be decreased to move the *LC* resonance frequency further away from the fundamental frequency.

Fig. 7 further shows the line current magnitude, the voltage magnitude of the series capacitor and the reactive power generation from the series capacitor as a function of C_1 using (3), (4) and (18). It can be seen from Fig. 7 that an increasing capacitance of C_1 leads to an increase of the current flowing into the converter transformer, a decrease of the voltage across C_1 and a decrease of the reactive power generated by C_1.

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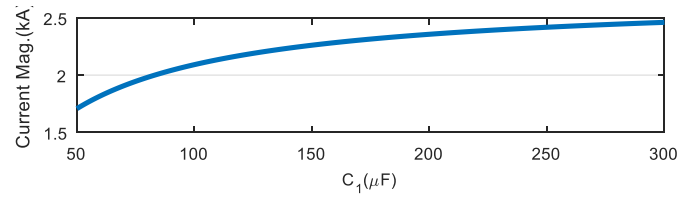
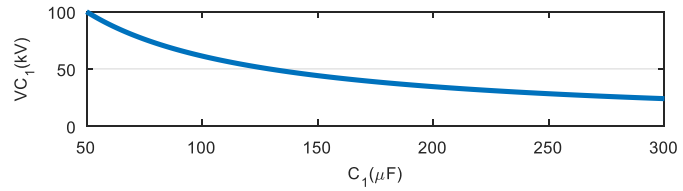
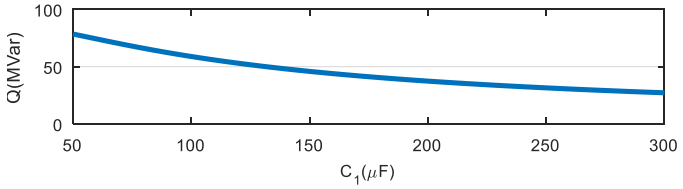


(a) Magnitude of $\overline{I_{\text{sec}}}$ as a function of C_1



(b) Magnitude of $\overline{V_{C_1}}$ as a function of C_1



(c) Reactive power of series capacitor

Fig. 7. Electrical performances with varying values of C_1.

With the selected capacitance of C_1, the percentage of the DC power transfer under single-phase fault can be calculated as $V_{dc}^{fault}/A_0 = 0.667$ using (12)-(15) with a firing angle of 161^0. It means that theoretically about 66.7% of the rated active power can be transmitted during zero impedance single-phase fault with the proposed method. For the Benchmark system rated at 1000MW, it is 667MW which is more than 60% of increase compared with AC filterless LCC HVDC [1].

B. Required Voltage Level from Controllable Capacitor

The commutation from *TY4* to *TY6* under the same phase A fault is considered in the following analysis. With the phase relationships discussed in Section III, the instantaneous line currents at the secondary side of converter transformer for phase A (i_{a-sec}) and phase B (i_{b-sec}) and the instantaneous voltages across the series capacitor of phase A (v_{C_1-a}) and phase B (v_{C_1-b}) can be expressed as:

$$i_{a-sec} = \left|\overline{I_{\text{sec}}^{fault}}\right| \cos(\omega t + 60^0 - \alpha) \tag{19}$$

$$i_{b-sec} = \left|\overline{I_{\text{sec}}}\right| \cos(\omega t - 60^0 - \alpha - \theta) \tag{20}$$

$$v_{C_1-a} = \left(\left|\overline{I_{\text{sec}}^{fault}}\right| N_1 / \omega C_1 N_2\right) \cos(\omega t + 60^0 - \alpha - 90^0) \tag{21}$$

$$v_{C_1-b} = \left(\left|\overline{I_{\text{sec}}}\right| N_1 / \omega C_1 N_2\right) \cos(\omega t - 60^0 - \alpha - \theta - 90^0) \tag{22}$$

The actual commutation voltage of the proposed method (line-to-line voltage at secondary side of converter transformer) can then be calculated as:

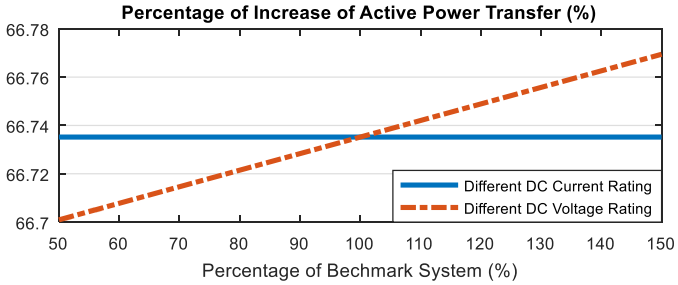
$$\begin{aligned} v_{commutation} = &\left(-v_{C_1-a} \times N_1/N_2 - L_c\left(di_{a-\text{sec}}/dt\right)\right) \\ &-\left(\left(V_B - v_{C_1-b}\right) \times \left(N_1/N_2\right) - L_c\left(di_{b-\text{sec}}/dt\right)\right) + 2V_0 \end{aligned} \tag{23}$$

where L_c is the equivalent inductance of converter transformer and V_0 is the voltage of the controllable capacitor. For the success of commutation, the following condition should be satisfied:

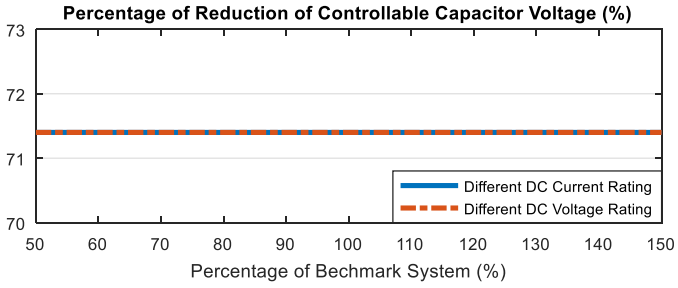
$$v_{commutation}(\alpha + \mu)\big|_{I_d = I_{dmax}} \geq 0 \tag{24}$$

where μ is the overlap angle and I_{dmax} is the transient peak DC current during fault. With an overlap angle of 4^0 and a peak DC current of 4kA, the minimum value of V_0 is calculated to be 20kV. It is more than 70% reduction compared with the AC filterless LCC HVDC (70kV). It also means that the required number of capacitor submodules is significantly reduced, which leads to significant reduction of the cost and associated losses (discussed in more detail in Section V).

C. HVDC System with Different System Parameters



(a)



(b)

Fig. 8. Performance improvements of the proposed method for HVDC systems with different system parameters.

To demonstrate the performance improvements of the proposed method compared with AC filterless LCC HVDC for HVDC systems with different system parameters, Fig. 8 is presented to show the results of theoretical calculations. Fig. 8(a) shows the increase of active power transfer for HVDC systems with different rated DC current and DC voltage where the value of 100% on the *x*-axis represents the base case of CIGRE benchmark system. Fig. 8(b) shows the reduction of voltage level of controllable capacitors. The method described in Section III is used to obtain Fig. 8(a) and the method described Subsection B of Section IV is used to obtain Fig. 8(b). It can be seen from Fig. 8 that the proposed method can achieve similar performance improvements for HVDC systems with different system parameters.

The following aspects have been considered in the calculations. For HVDC systems with different DC current ratings, the transformer ratings are modified accordingly to reflect the change of power rating. For HVDC systems with different DC voltages ratings, the turns ratio and the ratings of transformer are modified to reflect the change of DC voltage rating and power rating. For both scenarios, the value of C_1 is calculated using the method described in Section IV, and the

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value of C_2 is linearly modified to maintain similar harmonic filtering performance while simplifying the calculations (e.g., a proportionally larger C_2 is used for HVDC system with higher DC current).

To understand the calculation results, a HVDC system with different DC current rating is considered first. As mentioned above, this change of current rating indicates a proportional change of transformer rating and the capacitance of C_2 for both the AC filterless LCC HVDC and the proposed method. The capacitance of C_1 is then calculated, which is changed with the same proportionality. By observing (1)-(7), the above changes of parameters result in the same actual commutation voltage and the same phase angles (β and γ) compared with the base case (Benchmark system). Therefore from (12)-(15) it can be seen that the same levels of increase of active power transfer can be achieved (Fig. 8(a)). Furthermore, considering that 1) the increase of line current and the decrease of equivalent transformer inductance leads to the same voltage drop across the transformer and 2) the commutation voltage provided by the series capacitor (as shown in (4)) is the same, the same level of reduction of controllable capacitor voltage can be achieved (Fig. 8(b)).

For HVDC system with different DC voltage rating, based on the same considerations as described above, it can be calculated that the line current and the voltage across series capacitor are the same as the base case, and the actual commutation voltage changes linearly with the change of DC voltage, leading to the same phase angles (β and γ). So from (12)-(15) it can be seen that the increase of active power transfer is linearly related to the change of DC voltage rating (Fig. 8(a)); from (19)-(23) it can be seen that the percentage of reduction of controllable capacitor voltage (Fig. 8(b)) is the same.

For a more accurate analysis of performance improvements with other HVDC systems, detailed simulation studies are needed. This is because the aspects of harmonics, fast fault transients and the changes of overlap angle (although very small in the proposed method) are not considered in the calculations.

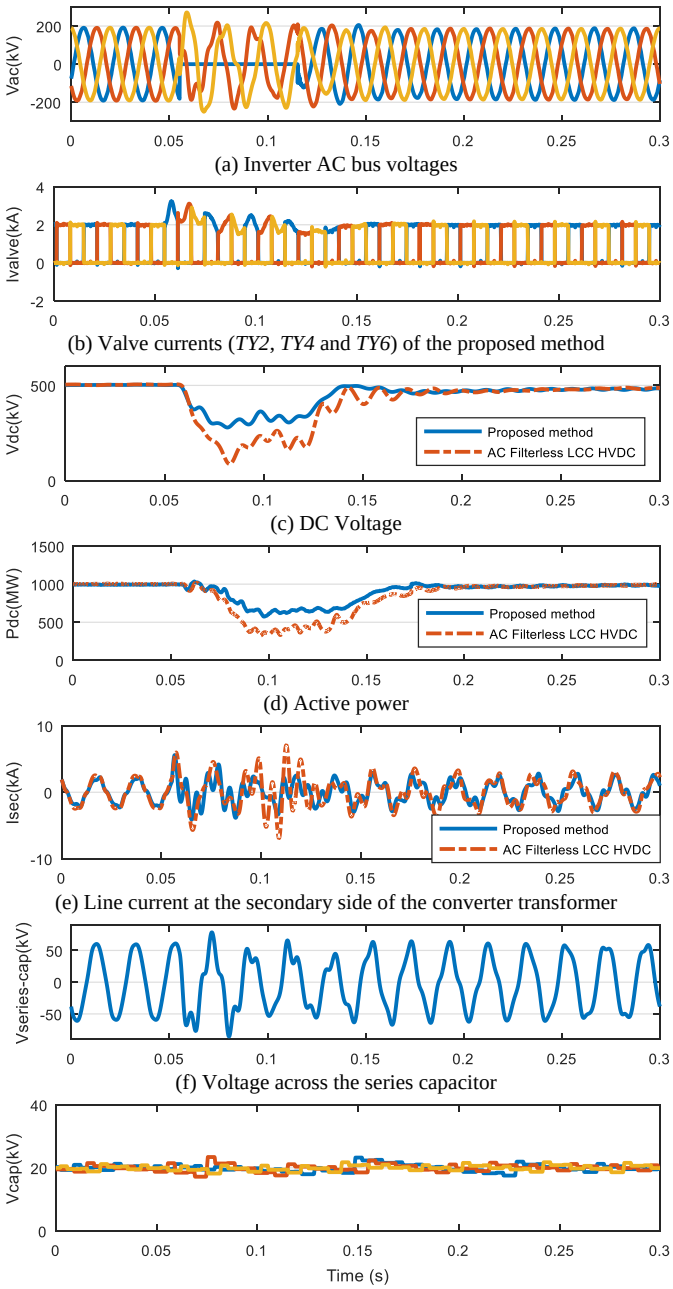
V. Simulation Results

As the most common type of fault in power system, single-phase to ground fault is simulated first to demonstrate the effectiveness of the proposed method. In addition, to further demonstrate the performance, a double-phase to ground fault and a three-phase to ground fault (although less frequent than single-phase fault) are simulated. Moreover, to provide further insights of the proposed method, the average power transfer against the level of voltage during fault are presented for the above three types of fault. Comparisons are made between the proposed method and the AC filterless LCC HVDC for all the cases.

Then cost analysis of the proposed method in comparison with AC filterless LCC HVDC is presented and the potential issue and solutions of ferroresonance are discussed.

A. *Case 1 – Single-Phase Fault*

Fig. 9 shows the system performance under 60ms zero impedance phase A to ground fault.



(a) Inverter AC bus voltages

(b) Valve currents (*TY2*, *TY4* and *TY6*) of the proposed method

(c) DC Voltage

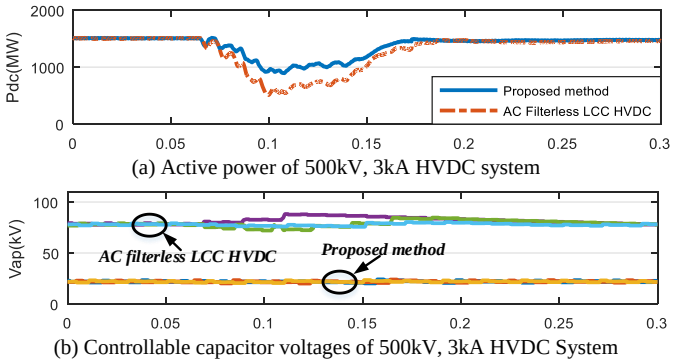
(d) Active power

(e) Line current at the secondary side of the converter transformer

(f) Voltage across the series capacitor

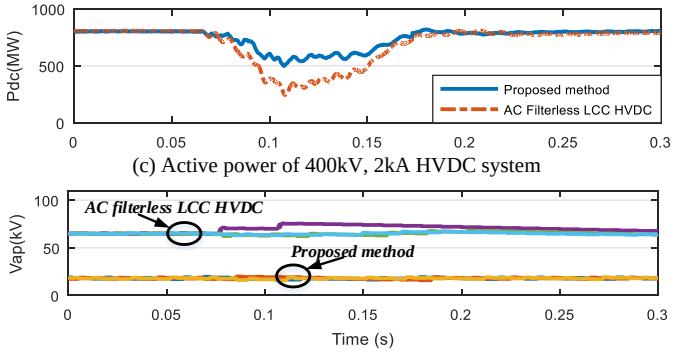
(g) Voltage of the controllable capacitor

Fig. 9. System response under zero impedance single-phase fault.



(a) Active power of 500kV, 3kA HVDC system

(b) Controllable capacitor voltages of 500kV, 3kA HVDC System



(c) Active power of 400kV, 2kA HVDC system

(d) Controllable capacitors voltages of 400kV, 2kA HVDC System

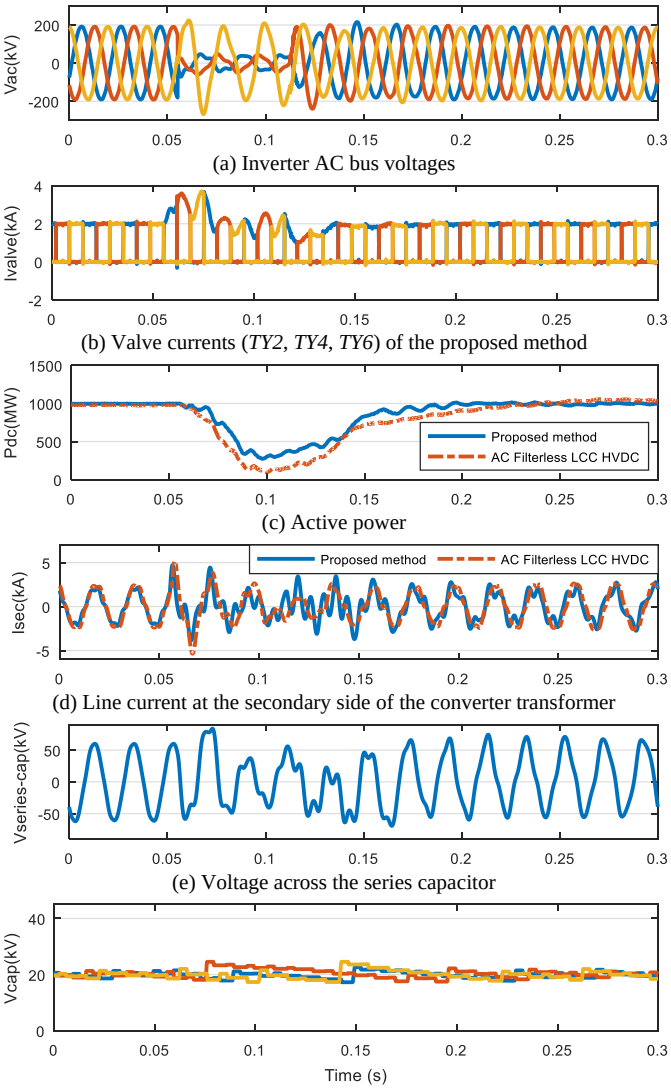
Fig. 10. System response with different HVDC systems.

It can be seen from Fig. 9(a) that phase A voltage drops to zero during fault but the commutations are still successful as shown in Fig. 9(b). Fig. 9(b) also shows that the average DC current is controlled around the rated value. From Fig. 9(c) it can be seen that the drop of DC voltage in the proposed system is much less than that in the AC filterless LCC HVDC as discussed in Section III. As a result, as shown in Fig. 9(d), an average active power of about 650MW can be transmitted during the fault while in contrast about 400MW with the AC filterless LCC HVDC can be transmitted (more than 60% of increase). At the same time, the speed of fault recovery is also faster with the proposed method. From the perspective the of inverter side AC system, it means that the level of power disruption caused by the fault is decreased. From the point of view of the DC system, it decreases the level of the DC voltage drop. Fig. 9(e) shows the dynamics of $\overline{I_{sec}}$ for phase A. Under steady-state, it can be seen that the magnitude of $\overline{I_{sec}}$ in the proposed method is less than that in the AC filterless LCC HVDC and the phase is slightly lagging, both agree with the analysis in Section III. Also it can be seen from Fig. 9(e) that $\overline{I_{sec}}$ experiences less overcurrent in the proposed system. Fig. 9(f) shows the voltage across the series capacitor in phase A. It can be observed that the steady-state voltage magnitude is about 60kV, and the overvoltage during fault is not significant. Finally, as can be seen from Fig. 9(g), the voltages of the controllable capacitors are well controlled throughout the fault.

To demonstrate the effectiveness of the proposed method for HVDC systems with different system parameters, Fig. 10 shows the simulation results of a 60ms zero impedance single-phase fault for two HVDC systems that have different system parameters from the Benchmark system (rated at 500kV and 2kA). Fig. 10(a) and Fig. 10(b) show the simulation results of the system rated at 500kV and 3kA. For this system, the series capacitance of 150μF is calculated and the controllable capacitor of 22kV is determined through simulation studies for the proposed method. Similarly, the controllable capacitor of 78kV is obtained for AC filterless LCC HVDC. Fig. 10(c) and Fig. 10(d) show the simulation results of the HVDC system rated at 400kV and 2kA. Series capacitance of 80μF and controllable capacitor of 19kV are obtained for the proposed method and the controllable capacitor of 68kV is obtained for AC filterless LCC HVDC.

It can be seen from Fig. 10(a) and Fig. 10(c) that similar levels of increase of active power transfer during fault can be achieved (increase of average power transfer from 620MW to 1000MW for Fig. 10(a) and 330MW to 560MW for Fig. 10(c)). Fig 10(b) and Fig. 10(d) show that the increase of active power transfer is achieved with similar levels of voltage reduction of controllable capacitors.

B. *Case 2– Double-Phase Fault*



(a) Inverter AC bus voltages

(b) Valve currents (*TY2*, *TY4*, *TY6*) of the proposed method

(c) Active power

(d) Line current at the secondary side of the converter transformer

(e) Voltage across the series capacitor

(f) Voltage of the controllable capacitor

Fig. 11. System response under low impedance double-phase to ground fault.

Fig. 11 shows the system performance under a 60ms low impedance double-phase (phase A and phase B) to ground fault. It can be seen from Fig. 11(a) that the voltages of phase A and phase B are dropped by about 80% but again the commutations are successful (Fig. 11(b)). Fig. 11(c) shows that due to the support from series capacitor, the amount of active power transfer during the fault is doubled with the proposed system. From Fig. 11(d), it can be seen that the line current is comparable to that in the AC filterless LCC HVDC during the fault. The current is higher at the start of recovery but is of short duration. From Fig. 11(e) it can be seen that the voltage across series capacitor experiences an initial increase when fault is

initiated and stays at lower values during the fault. Similar to Case 1, the voltages of controllable capacitors are well controlled (Fig. 11(f)).

C. *Case 3– Three-Phase Fault*

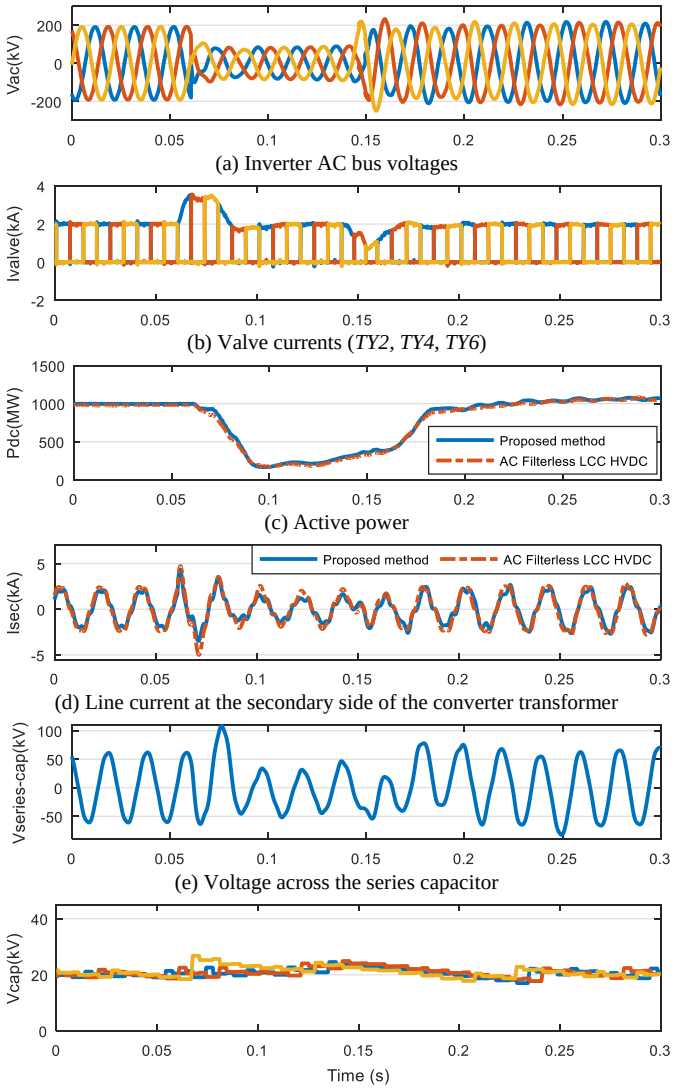


Fig. 12. System response under low impedance three-phase to ground fault.

Fig. 12 shows the system performance under 100ms low impedance three-phase to ground fault. As can be seen from Fig. 12(a), the three-phase voltages drop by about 60% but the commutations are successful (Fig. 12(b)). By observing Fig. 12(c), it can be seen that the transmitted active power is similar between the proposed method and the AC filterless LCC HVDC. This is because on one hand the series capacitor provides additional commutation voltage that helps increase the DC voltage. On the other hand, the phase lag introduced by the series capacitor to the actual commutation voltage reduces the DC voltage. With reference to Fig. 4, when V_A, V_B, V_C are significantly decreased and V_{C1} is increased (due to increased line current) during the fault, the zangle of $\beta-\gamma$ will be increased. It is this additional phase lag that causes an additional reduction of DC voltage. Fig. 12(d) shows that the line current at the secondary side of converter transformer is similar for both systems because the reduction of current contribution from inverter AC bus voltage is similar. In Fig. 12(e), it can be seen that the capacitor voltage experiences a short-period increase at the start of the fault and then stays at a lower value throughout the fault. Fig. 12(f) again shows that the voltages of the controllable capacitors are well controlled.

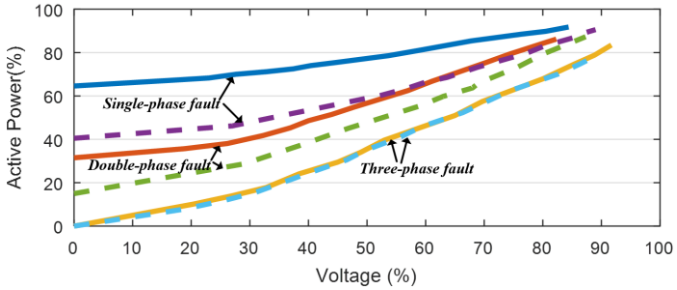


Fig. 13. Active power transfer vs. voltage level during faults.

To further demonstrate the benefits of the proposed method, Fig. 13 shows the average power transfer (as a percentage of the rated power) against the level of voltage during the fault (as a percentage of the rated voltage). The results for all the three types of fault are presented. The solid lines are for the proposed method and dashed lines are for the AC filterless LCC HVDC. It can be clearly seen from Fig. 13 that for single-phase and double-phase faults, more active power can be transmitted with the proposed method at all levels of the voltage drop. Although the performance improvement with three-phase fault is not obvious, it is important to point out that unbalanced faults account for about 95% of the faults in the transmission systems, while three-phase faults are very rare in occurrence, accounting for only about 5% [17]. Moreover, most of the CFs are caused by unbalanced faults [6] where active power can be transmitted through the healthy phases. Under the most severe three-phase faults when the voltage drops to very low values, it becomes impossible to transmit active power. Therefore the potential benefits by improving active power transfer under unbalanced faults are much higher than that for three-phase fault. Further considering that the majority of the power system faults (60% - 80%) are transient in nature [18], the proposed method can provide much more active power support (given the high power rating of LCC HVDC) to the inverter AC system during fault when active power is critically needed to support the AC system frequency. At the same time, it helps reduce the level of spinning reserve activation and load shedding (thereby achieve cost savings).

D. *Cost Analysis*

The previous case studies validated the technical performance of the proposed method. It is important that such superior technical performance is achieved without significant extra cost. It would be even more attractive if it is achieved with less cost compared with the AC filterless LCC HVDC. Therefore this section estimates the cost of the proposed method in comparison with the AC Filterless LCC HVDC. Extra cost is coming from the additional series capacitors, and cost saving is coming from the reduction of voltage level of

controllable capacitors. These two aspects are considered in the following analysis.

For the cost of series capacitor, it is reported in [21] that the cost ranges from $10/kVAr to $30/kVAr ($ represents US dollar). Using the average value of $20/kVAr, the extra cost of series capacitor in the proposed method can be estimated to be $20/kVAr×6×60MVar=M$7.2 (60MVar of reactive power from each series capacitor as calculated in Section IV).

For the cost reduction from the controllable capacitor, the cost of a MMC converter station is considered as reference. As an example, the ±525kV Nordlink converter stations (with half-bridge capacitor submodules) cost about M€400 [23] so each converter station costs about M€200. It indicates a cost of M€61 for the valves as the valve group accounts for 30.5% of the converter station cost [24]. By assuming that the full-bridge converter station costs 20% more (i.e., 200×20%=M€40) than the half-bridge converter station [25] and that this 20% extra cost is coming from the valves (30.5%) and control & protection (8.5% [24]), the cost of full bridge valves at ±525kV can be calculated as M€(61+40×30.5%/(30.5%+8.5%)) =M€92.28. Therefore the cost saving from the reduced number of power electronic devices (70kV-20kV=50kV) can be calculated as M€(92.28×50/525)=M€8.8.

The reduced voltage rating of the controllable capacitors also reduces the capitalized cost of losses which is normally evaluated at €4000 to €5000 per kW [15] (€4500 is used for following calculation). Note that the additional losses introduced by the series capacitor are very small and is therefore neglected [20]. Considering that the loss is about 2.2MW for 140kV of controllable capacitor [4], the saving from the reduced losses is €(2200×4500×50/140)=M€3.54. Therefore the total cost saving from the controllable capacitor is M€(8.8+3.54)= M€12.34, which is about M$14.5. So it can be seen that the cost saving (M$14.5) is about two times the extra cost from the series capacitors (M$7.2). It is clearly attractive and advantageous as the superior performance of the proposed method is achieved at lower cost.

E. Discussions on Practical Applications

1) Ferroresonance

One potential issue with the proposed method is the ferroresonance between the series capacitor and the saturating magnetic circuits of converter transformer. It can be excited by a system switching or an AC fault and cause overvoltage problems. Two kinds of methods can be adopted to effectively mitigate the problem. The first is to bypass the series capacitors upon detection of ferroresonance [16]. This can be achieved without considerable extra cost as the bypass mechanism as a way of protection function is normally equipped for the series capacitors. The second is by adding supplementary control signals to the HVDC control systems [22]. This method is also cost effective as only controller modification is needed without additional hardware investment.

2) Unbalanced Capacitor Voltages

Unbalance between three-phase capacitor voltages can happen due to a variety of reasons (e.g., transient change of DC current). The result of unbalanced capacitor voltages is that the commutation voltage provided by the series capacitor will be different for different valves in the converter. One method to reduce the risks to commutation from unbalanced voltages is to increase the voltage rating of controllable capacitors. In this way, the potential adverse impact caused by unequal commutation voltages from fixed series capacitors can be mitigated by the higher voltage insertion from controllable capacitors. Another method is to modify the firing angles upon detection of a capacitor unbalance so as to speed up the restoration to balanced voltages. Significant unbalanced capacitor voltages due to equipment damage need to be fixed through replacement or maintenance.

3) Harmonics

The use of fixed series capacitor reduces the overlap angle and slightly increases the steady-state AC and DC harmonics [26]. In practice, harmonic filters can be installed similar to that in CCC HVDC systems [26] in order to satisfy the harmonic requirements at both AC and DC sides. For potential resonance problems due to series capacitor (e.g., ferroresonance as mentioned above), they can be effectively mitigated by either bypassing the series capacitor or modifying the converter control systems.

4) Capacitor Overvoltage

Protection schemes similar to that for series compensation [20] can be adopted to protect the overvoltage of series capacitors. Normally, series capacitors are protected against overvoltage by Metal Oxide Varistors (MOVs) which are connected in parallel with the capacitors. The varistors provide overvoltage protection of the capacitor by conducting a large part of the fault current. MOVs are then protected by the spark gap against excessive energy absorption. Bypass circuit breaker, which are connected in parallel with the capacitor bank and the overvoltage protective circuit, can be used for emergency bypass of the capacitor.

Overall, given the wide applications and mature technology of fixed series compensation in power system, similar protection arrangements can be adopted in the proposed method to handle the potential practical issues.

5) Valve Voltage Stress

During the process of power reversal at inverter, the decrease of firing angle would lead to an increase of voltage stress across thyristor valves [27]. The peak voltage across the thyristor can be high when the firing angle is close to 90 degrees. This adverse impact can be reduced by reducing the level of DC current during power reversal. It is because a reduced DC current reduces the current flowing through series capacitor hence a lower voltage from series capacitor is added to the thyristor valves. In addition, the series capacitor can be bypassed under low current to further minimize the valve voltage stress during power reversal [27].

VI. CONCLUSION

The series capacitor compensated AC filterless LCC HVDC has been proposed in this paper. It has been theoretically explained that the inclusion of the series capacitors 1) considerably increases the commutation margin to counteract the unfavorable phase shift caused by the unbalanced fault and

2) provides extra commutation voltage to reduce the level of DC voltage drop due to AC faults. As a result, the proposed system can significantly 1) decrease the required voltage level from controllable capacitors for CF elimination and 2) increase the amount of active power that can be transmitted under unbalanced AC faults, minimizing the adverse impact on the connected AC system. Simulation results for single-phase, double-phase and three-phase faults have been presented to validate the technical performance of the proposed method. The average power transfer at different levels of voltage during fault is further presented to demonstrate the performance. From the economic perspective, cost analysis of the proposed method has also been carried out to show that the superior technical performance can be achieved with reduced cost. This is mainly due to the reduced equipment cost and reduced capitalized cost of losses from the controllable capacitors. Finally the possible solutions for various practical issues have been discussed.

As this paper is focused on the point to point HVDC system, one future research direction is the evaluation and application of the proposed method in multi-infeed HVDC systems, where detailed technical and economical performances will be further analyzed.

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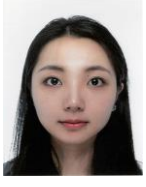

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