70 Gb/s 0.87 pJ/bit GeSi EAM Driver in 55 nm SiGe BiCMOS

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Abstract *We present a differential EAM driver with on-chip DC-biasing, capable of delivering 2 Vpp to a lumped 50 μm GeSi EAM, resulting in 4 dB extinction ratio. 70 Gb/s NRZ transmission over 2 km SSMF (1560 nm) with record low power consumption of 61 mW is demonstrated.*

Introduction

The ever growing popularity of cloud based applications is putting the servers and links inside data centers under continued pressure. Industry is therefore considering 800 Gb/s and 1.6 Tb/s links[1], which will require optical transceivers built from densely integrated parallel channels that operate at high bitrates ($>$ 50G/s) with extremely low power consumption. Silicon photonic microring modulators and electro-absorption modulators (EAM)[2] have a small footprint and hence a very low intrinsic capacitance. Despite their low extinction ratio (ER), their high speed capabilities make them a good match for intra-datacenter links. It has been shown in ref[3] that GeSi EAMs in a silicon photonic integrated circuit (PIC) can achieve 100 Gb/s non-return-to-zero (NRZ) transmission over 2 km fiber (C-band), however, without a dedicated compact low-power driver. Low power $>$50 Gb/s microring modulator drivers have been reported[4], but although EAMs and microring modulators both behave as small capacitors, these inverter based microring drivers are not suited to drive EAMs. EAMs add complexity because they produce a considerable amount of photocurrent that needs to be sunk by the driver, which could distort the output signal or reduce the transmitter speed if no proper measures are taken in the driver circuit. Moreover, this undesirable photocurrent also complicates the modulator biasing. AC-coupling the output to bias the modulator with a simple on-chip RC bias-T[5] is typically not possible with EAMs due to a large voltage drop caused by the EAM photocurrent over the resistive DC-feed and an off-chip LC bias-T[6] requires too much space in the package. A microring, on the other hand, is easier to bias, but on the downside, it requires wavelength stabilization and has a narrower optical bandwidth with respect to an EAM.

In this paper, we present a transmitter consisting of a fully differential ultra-low power (61 mW) DC-coupled driver in a SiGe BiCMOS technology, delivering up to 2 Vpp to a lumped unterminated (purely capacitive) EAM. The driver is able to sink up to 4 mA absorption photocurrent and properly reverse bias the EAM up to 1.5 V while operating at a record high bit rate (70 Gb/s) with sub-pJ/bit efficiency.

Differential driver topology

Typically, high-speed NRZ drivers use a static current source which is switched to either the anode of the modulator, when transmitting a one, or to a dummy supply rail or load when transmitting a zero. The high-speed switching is done using a so-called differential pair. This scheme is known as single-ended driving, and allows for straightforward biasing of the modulator by connecting its cathode to a suitable DC bias voltage[7,8]. The current in the dummy supply rail or load is not contributing to the modulation, however, still consuming a significant amount of power. When driving differentially, we also drive the cathode when transmitting a zero, instead of dumping this current in a dummy load. This improves the driver performance in two areas: power consumption and drive voltage. For the same drive voltage, we have half the power consumption (e.g. 20 mA static current in the differential driver versus 40 mA in the single ended case). In addition, large currents require large transistors, making the driver and predriver slower.

The differential drive scheme, however, poses a problem: reverse biasing the modulator. Both output terminals of a differential pair have the

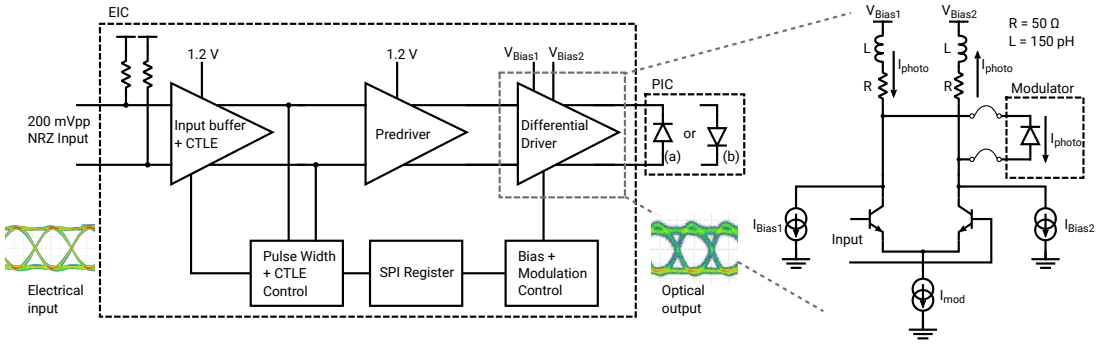

Fig. 1: Left: Driver block diagram with two modulator configurations (a) and (b), Right: simplified schematic of differential output driver with modulator biasing. For simplicity of the figure, only configuration (a) of the modulator is shown.

same DC output voltage, leading to 0 V bias over the modulator. While this is not a problem for some modulators, microring modulators and EAMs in most cases require a reverse bias.

Here, we propose a differential drive scheme that does not have this problem (Fig. 1), because it uses a modified supply network to DC-couple and bias the modulator. The modulator is biased by the difference between the two bias voltages V_{Bias1} and V_{Bias2}. In configuration (a) we take $V_{Bias1} > V_{Bias2}$ to reverse bias the modulator and in configuration (b) $V_{Bias1} < V_{Bias2}$. Thanks to the proposed differential driver topology, the sign of the bias voltage can be selected, resulting in flexibility during packaging. As stated before, for a conventional differential pair, $V_{Bias1}=V_{Bias2}$. For simplicity only one configuration is shown in the output stage schematic. The analysis can be repeated for the other modulator configuration. The EAM photocurrent (I_{photo}) for configuration (a) is annotated on Fig. 1. This I_{photo} lowers the effective bias voltage applied to the EAM by $2RI_{photo}$. Typically R (around 50 Ω) is much smaller than the resistive DC-feed of a bias-T (e.g. 10 kΩ) making the voltage drop (~200 mV) acceptable. Two current sources I_{Bias1} and I_{Bias2} were added to fine tune the bias voltage and to compensate for the transistor second order effects due to the voltage difference. For configuration (a) we turn on I_{Bias2} and for (b) we turn on I_{Bias1}.

ASIC implementation

Fig. 1 shows the proposed driver architecture realized in a SiGe 55nm BiCMOS technology. A 200 mVpp differential NRZ signal is applied to the 50 Ω matched inputs. A continuous time linear equalizer (CTLE) is used to compensate for transmission line and cable losses at higher frequencies. After the input buffer, the signal is amplified by the predriver and fed to the differential output driver. To reduce the power consumption, the input buffer and the predriver are placed on a lower supply voltage (1.2 V) than the output stage. The EAM is DC-coupled between the two output terminals of the differential driver. As the EAM is extremely compact, it can be driven lumped without a 50 Ω termination on the PIC avoiding power dissipation in the resistor.

The value of the output impedance R=50 Ω is a trade-off between bandwidth (BW) versus power consumption. A lower output impedance increases bandwidth at the expense of higher power consumption for a given output swing. To increase the BW, shunt inductive peaking is used (L=150 pH). The maximum EAM current we can sink before the driver starts to distort the signal is 4 mA, which is sufficient for all normal use cases. The driver's active area measures 0.4 mm^2.

Electro-optical experiments

We assembled the SiGe BiCMOS driver to a 50 μm long GeSi EAM[2] fabricated in imec's silicon photonics platform (Fig. 2). The EAM is based on the Franz-Keldysh effect and has a measured insertion loss (IL) of 5 dB. We used a tunable laser at 1560 nm, where the EAM has best ER versus IL trade-off.

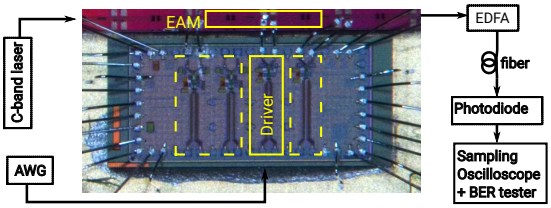

Fig. 2: Measurement setup: Parts of the electrical chip in dashed boxes are not used in the measurements.

We applied the electrical 200 mVpp differential input signal to the driver by a GSSG 67 GHz RF probe. The light (10 dBm) is coupled into and out of the optical chip by grating couplers (IL ~6 dB) and the estimated power into the EAM is ~4 dBm. After the second grating coupler the average optical power is -7 dBm. An erbium-doped fiber amplifier (EDFA) was used to compensate for the grating coupler losses and to overcome the reduced sensitivity due to the lack of a suitable high-

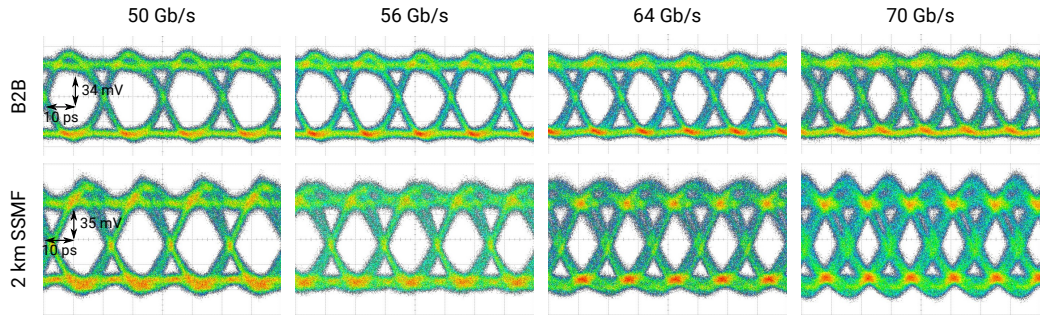

Fig. 3: Measured eye diagrams back-to-back and after 2km of SSMF for 50 Gb/s, 56 Gb/s, 64 Gb/s and 70 Gb/s.

speed transimpedance amplifier (TIA). Instead, a 70 GHz commercial 50 Ω matched photodiode with a responsivity of 0.6 A/W was used. The average power into the photodiode was 9 dBm. With a high speed TIA, no EDFA should be needed.

The EAM is reverse biased around 0.9 V, created by placing V_{Bias1} of the driver at 2 V and V_{Bias2} at 3 V. The average EAM current (I_{photo}) that is sunk by the driver is around 1.5-2 mA.

Fig. 3 shows the measured optical eye diagrams from 50 Gb/s to 70 Gb/s for back-to-back (B2B) transmission and after 2 km standard single mode fiber (SSMF) captured by a 50 GHz sampling oscilloscope. The EAM bias voltage was not changed between the B2B and 2 km transmission experiments. The small overshoot in the eyes is caused by the wirebonding inductance. We used pseudorandom binary sequence (PRBS) 2^9-1, limited by the memory of our 92 GS/s arbitrary waveform generator (AWG) used as pattern generator. 70 Gb/s was also the maximum bitrate at which the AWG still generated a clean input eye. The eyes are clearly open, even after 2 km of SSMF. The measured ER is 4 dB. The driver consumes 61 mW, leading to 0.87 pJ/bit (at 70 Gb/s).

To verify the real-time performance, we performed bit-error ratio (BER) analysis with a commercial BER tester. The transmitter is error free with a BER $< 10^{-13}$ after 2 km SSMF for 56 Gb/s, the highest rate at which the BER tester could be operated. However, with clear open eyes, we can still expect BERs well below the conventional forward error coding limit for data center applications beyond 56 Gb/s. Tab. 1 compares this work with other 56 Gb/s+ EAM drivers showing that this work has the lowest power consumption while transmitting the highest bit rate.

Tab. 1: Comparison of reported EAM drivers with optical experiments (Bit Rate $>$ 56 Gb/s)

Ref.	Power	Speed	Swing	EAM term.
6	1 W	56 Gb/s*	1.2 Vpp	50 Ω
7	84 mW	56 Gb/s	1.3 Vpp	50 Ω
8	1.4 W	56 Gb/s	1.7 Vpp	50 Ω
This work	61 mW	70 Gb/s	2 Vpp	-

*: 28 Gbaud PAM4

Conclusions

In this paper, we proposed a 70 Gb/s fully differential EAM driver with a novel biasing scheme. We showed that the driver is able to effectively bias the GeSi EAM, while sinking 2 mA photocurrent. The driver consumes only 61 mW at 70 Gb/s (0.87 pJ/bit) and the eyes are still open after 2 km of SSMF. Error free operation was verified up to 56 Gb/s, which was the maximum operation speed of the commercial BER tester.

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References

[1] Ethernet Alliance,"The 2018 Ethernet Roadmap," https://ethernetalliance.org/the-2018-ethernet-roadmap (April 2018).

[2] M. Pantouvaki et al.,"Active Components for 50 Gb/s NRZ-OOK Optical Interconnects in a Silicon Photonics Platform," JLT, Vol. **35**, no. 4, p. 631 (2017).

[3] J. Verbist et al., "First Real-Time 100-Gb/s NRZ-OOK Transmission over 2 km with a Silicon Photonic Electro-Absorption Modulator," OFC, Th5C.4, Los Angeles (2017).

[4] H. Ramon et al.,"Low-Power 56Gb/s NRZ Microring Modulator Driver in 28nm FDSOI CMOS," PTL, Vol. **30**, no. 5, p. 467 (2018).

[5] H. Li et al.,"A 25 Gb/s, 4.4 V-Swing, AC-Coupled Ring Modulator-Based WDM Transmitter with Wavelength Stabilization in 65 nm CMOS," JSSC, Vol. **50**, no. 12, p. 3145 (2015).

[6] T. Kishi et al.,"56Gb/s Optical Transmission Performance of an InP HBT PAM Driver Compensating for Nonlinearity of Extinction Curve of EAM," JLT, Vol. **35**, no. 1, p. 75 (2017).

[7] J. H. Choi et al., "Ultra-low power SiGe driver-IC for high-speed electroabsorption modulated DFB lasers," OFC, Th3G.3, Los Angeles (2017).

[8] T. Tatsumi et al.,"1.3 um, 56-Gbit/s EML module target to 400GbE," OFC, OTh3F.4, Los Angeles (2012).