

# Transfer printing for silicon photonics transceivers and interposers

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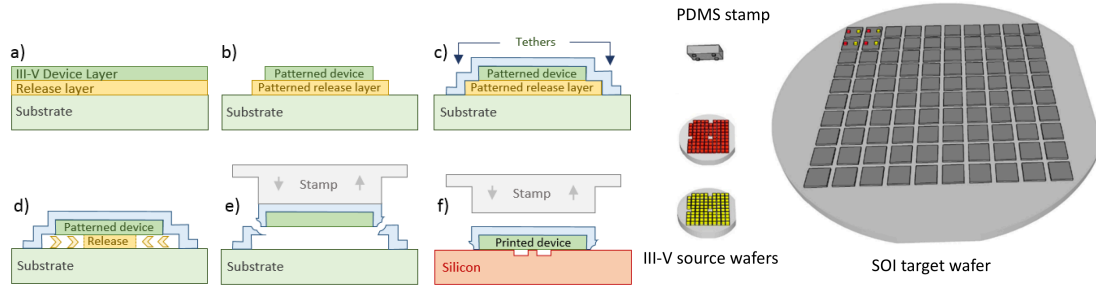
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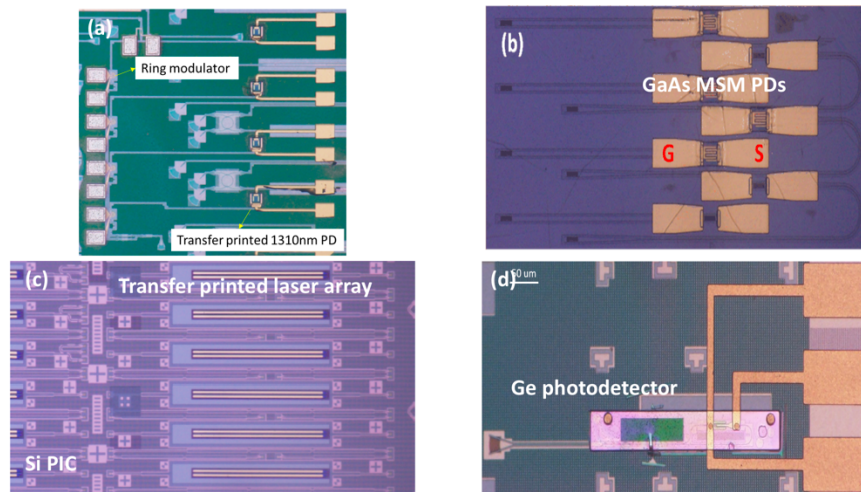
**Abstract:** We present transfer printing as an enabling technology to realize heterogeneous photonic integrated circuits. The approach enables a cost-effective and intimate integration of III-V lasers on advanced high-speed Si PICs. It also enables the integration of III-V and silicon-based opto-electronic components on a passive Si/SiN interposer.

Silicon photonics is now considered as a mainstream approach for the realization of high-speed transceivers. Also, high-performance passive waveguide circuits can be realized on such a platform, especially when exploiting low-loss SiN waveguide structures. However, the integration of the laser sources and/or optical amplifiers on a silicon photonic platform remains problematic. Several approaches are being pursued, each with their own advantages and drawbacks, as well as different TRL levels. There is a consensus that monolithically integrated Group IV lasers are very far from being a practical light source for silicon photonics, and that III-V semiconductor materials and devices need to be used. Currently, the III-V laser integration approach that has the highest maturity – pioneered by Luxtera – is the use of a micro-packaged laser, comprising a III-V laser diode on a micro-optical bench and including a ball lens, isolator and mirror to focus the light on a grating coupler defined in the Si PIC [1]. While this approach has several advantages (use of mature InP technology, wafer-level assembly, packaging, test and burn-in, integration on the back-end stack of a silicon photonic wafer), the complexity of the laser itself and its sequential active alignment on the silicon photonic wafer make it an expensive solution. Moreover, the fact that a grating coupler structure is used limits the coupling efficiency and bandwidth, and no waveguide-in/waveguide-out components such as semiconductor optical amplifiers (SOAs) – key components in advanced photonic integrated circuits – have been integrated using this approach. Therefore, more intimate integration approaches are being pursued, ranging from flip-chip integration over III-V die-to-wafer bonding to hetero-epitaxial growth. While front-end hetero-epitaxial growth of III-V semiconductors represents the ultimate way to integrate light sources on silicon photonics and proof-of-concept devices have been demonstrated [2], the technology is still in its infancy and many hurdles still need to be overcome, before this can be considered as a viable technology for light source integration on an advanced silicon photonics platform. Flip-chip integration and die-to-wafer bonding approaches are maturing, however there are still drawbacks associated with these integration methods. The most notably are that flip-chip integration still is a sequential operation, thereby reducing the laser integration throughput, while for die-to-wafer bonding the back-end of line processing of the silicon wafers in the CMOS fab is compromised. In this paper we are proposing the use of transfer printing technology for the integration of III-V opto-electronic components on a full-platform silicon photonic wafer, a technique that combines best of both worlds (i.e. it allows for a massively parallel integration of the III-V opto-electronic components on silicon photonic wafers with the full back-end stack processed on it). We also propose this as an integration approach for photonic interposers, where the waveguide circuit is purely passive (Si or SiN based) and therefore low-cost, onto which III-V opto-electronic components and silicon photonic high-speed devices are integrated by transfer printing. The transfer printing process, as shown in Fig. 1, starts with the definition of the III-V opto-electronic components (e.g. SOAs, lasers) on the III-V source wafer. The III-V source wafer comprises the epitaxial layer stack grown on top of a release layer (e.g. InGaAs in the case of the InP material system). After patterning of the device and the release layer, the structures are encapsulated and the release layer is selectively etched, leaving the III-V opto-electronic components only attached by tethers to the III-V substrate. This enables to use of a stamp to (selectively) pick-up arrays of III-V opto-electronic components from the source wafer and print them onto the silicon photonic target wafer, after which the encapsulation is removed and the III-V devices are electrically contacted on a wafer-scale. This approach enables pretesting of the III-V devices on the source wafer, alike flip-chip integration, and the massively parallel integration of the devices, alike a die-to-wafer bonding approach. As the devices that are transferred are micro-scale, the standard silicon photonics back-end flow is not disturbed. Only a local opening needs to be made in the back-end stack to reach the silicon device layer, similar to a flip-chip integration approach.



**Figure 1** Transfer printing integration approach.

Examples of the use of transfer printing technology for silicon photonic integrated circuits are shown in Fig. 5 [3-6], showing the versatility of the integration approach, including a) integration of O-band III-V photodiodes on an iSIPP25G full platform silicon photonic IC; b) 850 nm GaAs MSM photodetectors on a SiN waveguide circuit; c) C-band etched facet laser integration on a passive Si waveguide circuit; d) a silicon-waveguide coupled Ge high-speed photodiode integrated on a passive silicon waveguide circuit. These and other results will be discussed in detail during the conference.



**Figure 2** Demonstrations of the transfer printing technique for photonic integrated circuits: a) integration of O-band photodiodes on an iSIPP25G full platform silicon photonic IC; b) 850 nm GaAs MSM photodetectors on a SiN waveguide circuit; c) C-band etched facet laser integration on a passive Si waveguide circuit; d) a silicon-waveguide coupled Ge high-speed photodiode integrated on a passive silicon waveguide circuit.

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