Electronic ICs for Silicon Photonic Transceivers

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***Abstract*— We present progress on high-speed electronic ICs for Silicon Photonic transceivers. The design freedom offered by Silicon Photonics is exploited to generate multilevel modulation formats, reduce power consumption and physical footprint or increase speed. We show drivers and receivers integrated in CMOS and SiGe BiCMOS processes.**

Keywords—CMOS and SiGe BiCMOS integrated circuits

I. Introduction

Data center traffic is continuing to grow rapidly, which is driving an unprecedented demand for high capacity optical transceivers for short-reach intra data center links. The IEEE 802.3 Working Group has answered to this need with its recently updated roadmap towards 800Gb/s and 1.6Tb/s speeds [1]. Such capacities can be achieved by increasing baudrate, multiplexing more channels or using higher-order modulation formats. The main constraint will be to fit the 800Gb/s or 1.6Tb/s transceivers in approximately the same footprint as today's 400Gb/s modules. This brings significant challenges in terms of integration density and power consumption.

Silicon Photonics (SiPh), with its capability to densely integrate complex photonic functions into a small photonic integrated circuit (PIC) is an excellent candidate for such transceivers. Dedicated electronics are required to interface with the modulators and detectors. As monolithic integration of photonics and electronics into a sufficiently small CMOS node to achieve >28Gbaud speed is difficult, the electronics are typically realized as separate electronic ICs (EICs). This also offers the potential to stack EICs and PICs, reducing module footprint. This paper gives examples of recent driver and receiver circuits intended to interface with SiPh components.

II. CMOS Electronics

Realization of the driver and receiver electronics in a CMOS process offers the advantage of monolithic integration with large-scale digital chips. The low (<1V) breakdown voltage of the transistors in deep sub-micron CMOS nodes limits the achievable drive voltage, which may limit the optical modulation amplitude. At the receiver side, it can be difficult to achieve low-noise, high gain and wideband amplification. Integration into a large-scale digital chip will require consideration of crosstalk due to logic switching activity.

A. 65nm CMOS PAM-4 driver

To achieve high baudrates (>28Gbaud), travelling wave Mach-Zehnder modulators (MZMs) can be used. However for intermediate baudrates (up to 28Gbaud) it is interesting to use lumped MZMs, as these require significantly less PIC area. From the electrical point-of-view, a lumped MZM is a capacitor. To efficiently generate multi-level modulation formats, this capacitor can be combined into a switched capacitor bank: an example how to generate PAM-4 is shown in Fig. 1. This structure has the potential to achieve very low power consumption as energy is only required when switching capacitors, unlike conventional driving approaches which continuously draw current through load and termination resistors. One implementation using 65nm CMOS is given in [2]; up to 18Gbaud PAM-4 was demonstrated at 5.4pJ/bit. The EIC was flip-chipped onto the Si PIC using 50µm solder jetted microbumps [3]. Further improvements are possible using a faster CMOS process and re-design of on-chip retiming logic.

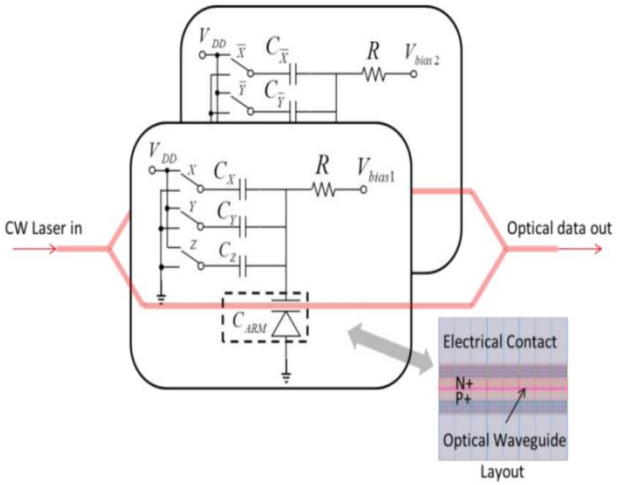

Fig. 1 – Switched capacitor PAM-4 driver concept.

B. 28nm FDSOI CMOS inverter based microring driver

As MZMs are large structures that can have significant capacitance (in the lumped case) or need transmission lines (resulting in power dissipation in the termination resistors), ultra-small devices such as microring or electro-absorption modulators (EAMs) have drawn significant attention. Microrings offer the advantage of extremely small footprints and requiring relatively small drive voltages, although their resonance wavelength is highly sensitive to temperature and process variations. The small capacitance (<30fF) and low drive voltages lend itself well to realizing the driver as a simple CMOS inverter. One example was provided in [4], in which 56Gb/s was achieved at 710fJ/bit using a 28nm FDSOI CMOS technology and careful circuit topology optimization.

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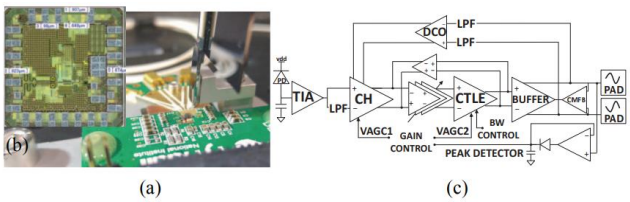

(a) (c)

Fig. 2 (a) Packaged receiver with vertically coupled fiber (b) inset, micrograph of EIC, (c) receiver architecture.

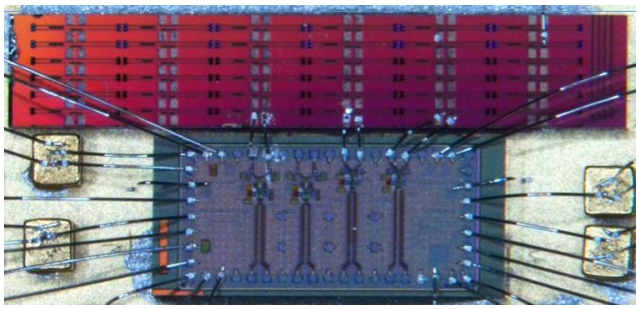

Fig. 3. 56Gb/s 4-channel SiGe BiCMOS driver wirebonded to SiPh PIC with GeSi EAMs.

C. 65nm CMOS linear transimpedance amplifier

The low gain available from deep sub-micron CMOS transistors do not lend these well to implementing low-noise, high gain and linear transimpedance amplifiers (TIAs). In [5], these challenges were addressed using a combination of peaking inductors (implemented as small 3D solenoids) and addition of a continuous-time linear equalizer (CTLE). The topology of each stage was selected carefully to ensure linearity, making the receiver suitable for PAM-4 signals; the chip was realized using 65nm CMOS. At 20Gbaud PAM-4, the sensitivity was measured to be better than −10dBm (optical modulation amplitude) at a bit-error rate of 10^{-3}, using a Ge photodiode integrated into a Si PIC. The TIA was flip-chipped onto the Si PIC using 50µm microbumps. Power consumption was 80mW, resulting in 2pJ/bit energy efficiency.

D. Drivers for segmented modulators

Generation of multi-level modulation formats using conventional single or dual electrode optical modulators require either linear drivers or power digital-to-analog converters (DACs), both of which can be complex and power hungry electronic components. An alternative is to use segmented modulators and more specifically segmented MZMs. In such a structure the electrode(s) of the MZM is (are) split into segments (of well-chosen lengths), and each of the segments is driven by a simple binary driver circuit. A dedicated driver IC for a 5-bit segmented InP modulator was demonstrated in [6]: the chip contained 10 output channels with tunable delay cells to match the optical signal propagation along the modulator; each output stage consists of CMOS inverters capable of providing up to 1.1V swing. The chip was fabricated in a 40nm CMOS process; up to 15Gbaud 2-ASK-2-PSK and 4-ASK-2-PSK modulation was demonstrated. These concepts can be readily extended to SiPh segmented MZMs.

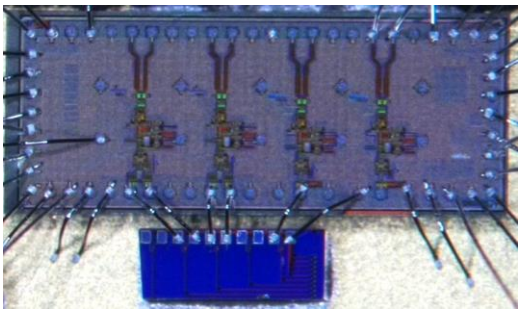

Fig. 4. 56Gb/s 4-channel SiGe BiCMOS TIA wirebonded to SiPh PIC with Ge photodiodes.

III. SiGe BiCMOS Electronics

Through the addition of heterojunction bipolar transistors (HBTs) to a CMOS node, improvements in speed, noise (for the receiver) and bandwidth can be realized.

A. 4-channel SiGe BiCMOS EAM driver

GeSi EAMs are promising modulators for inclusion on SiPh PICs due to their small size, robust optical transfer characteristics, low insertion loss and high modulation bandwidth [7]. Compact EAM drivers need to provide dc-bias without bulky biastees, while sinking the absorption current and providing sufficient modulation swing (~2V). A 4-channel NRZ 56Gb/s driver IC capable of these specifications is shown in Fig. 3; it was realized in a 55nm SiGe BiCMOS process.

B. 4-channel SiGe BiCMOS TIA

One of the main challenges associated with SiPh is to achieve the required optical budget. TIAs therefore need to have as low noise as possible. Fully differential operation while being able to correctly bias the photodetectors is then essential. An example of a 4-channel TIA that can provide such functionality is given in Fig. 4: the TIA was fabricated using a 55nm SiGe BiCMOS process, and wirebonded to Ge photodiodes on a SiPh PIC.

IV. Conclusion

Recent examples of driver and receiver circuits optimized for interfacing with SiPh components have been provided.

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