Vertical-Cavity Silicon-Integrated Lasers by Bonding and Transfer Printing

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***Abstract**: We present the design and performance of the first current-driven hybrid-vertical-cavity silicon-integrated laser with in-plane waveguide emission. We also show results from preliminary work on transfer printing for large-scale integration of such light sources on silicon photonic integrated circuits.*

1. INTRODUCTION

Photonic circuits on silicon would benefit from an integrated and efficient on-chip light source [1]. With the vertical-cavity surface-emitting laser (VCSEL) being the most efficient low-current/low-power semiconductor laser available, we explore heterogeneous integration of hybrid-vertical-cavity lasers and demonstrate the first current-driven vertical-cavity silicon-integrated laser (VCSIL) with in-plane waveguide emission [2]. We also explore transfer printing as a technology for massively parallel integration of such lasers on silicon photonic circuits with high throughput.

2. VCSIL DESIGN AND FABRICATION

The short wavelength VCSIL (Fig.1, left) is built by bonding an epitaxial "half" GaAs-based VCSEL structure (upper p-DBR, active region, and intra-cavity n-contact layer) to a dielectric DBR (Ta_2O_5/SiO_2) and SiN/SiO_2 waveguide on silicon. This forms a hybrid-vertical-cavity with an intra-cavity waveguide [3]. An oxide aperture in the upper part of the cavity provides transverse confinement of the vertical cavity field. A grating etched in the intra-cavity waveguide taps off power from the vertical cavity for bi-directional waveguide emission. The grating also enforces transverse single mode operation and sets the polarization state of the vertical cavity field for controlled in-plane emission [4].

After adhesive bonding of the epitaxial structure to the dielectric DBR/waveguide/grating and removal of the GaAs substrate [3], the VCSIL is fabricated by mesa etching, selective oxidation, and contact deposition/annealing (Fig.1, right). Electron beam lithography is used for grating definition and laser lithography is used to precisely position the VCSIL aperture over the grating. Grating couplers at the ends of the waveguide are used to monitor the power in the waveguide in the two directions.

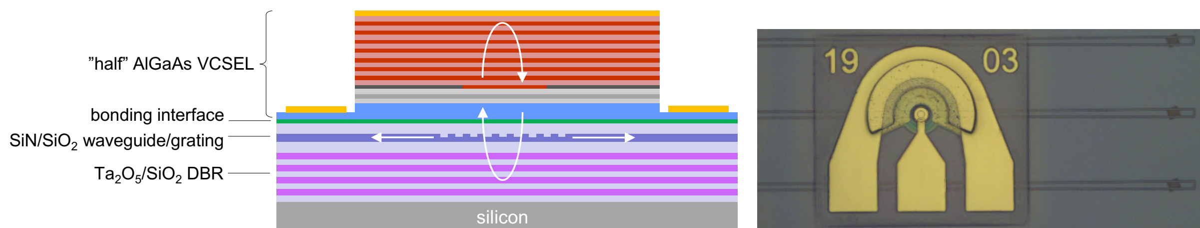

Fig.1 Left: Cross-section of the VCSIL showing the hybrid-vertical-cavity and the intra-cavity waveguide/grating for in-plane emission. Right: Microscope image of a VCSIL with the intra-cavity waveguide and one of the grating outcouplers visible.

3. VCSIL PERFORMANCE

The performance of VCSILs with a 5 µm oxide aperture and emitting at 857 nm is shown in Fig.2. A VCSIL with a 525 nm grating period has a threshold current of ~1 mA and emits a maximum single-ended waveguide power of 73 µW. The powers emitted in the two directions are equal, as expected from the symmetry of the device. The dependence of the slope efficiency on the grating period is consistent with simulations [4]. The ~30 dB side-mode suppression demonstrates the ability of the grating to suppress higher order transverse modes of the vertical cavity and enforce single mode operation.

While the present device has a low threshold current, it is higher than expected and the slope efficiency (0.085 W/A single-ended) is lower than predicted by simulations (0.4 W/A). This is due to unexpected cavity loss attributed to additional scattering loss and/or absorption. In addition, the maximum output power is limited by early thermal rollover caused by the high thermal impedance (11.8 K/mW). With reduced cavity loss and lower thermal impedance (by using metallic heat spreaders or thermal shunts), significant performance improvements are expected.

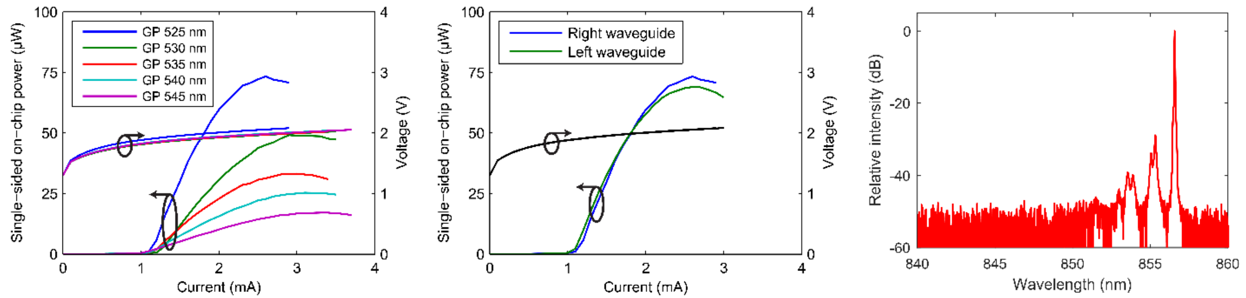

Fig.2 Left: Waveguide coupled power (single-sided) and voltage vs. current for different grating periods (GPs). Middle: Single-ended waveguide coupled power (right and left) vs. current with GP=525 nm. Right: Emission spectrum at 2.5 mA (GP=525 nm).

4. TRANSFER PRINTING

In the fabrication process used, device processing is done after die-to-wafer bonding of the epitaxial structure to the target substrate. With millimeter-scale minimum die size, the efficiency of material use is poor. This also prohibits dense co-integration of different III-V epitaxial layer structures. Transfer printing [5], on the other hand, allows the manipulation of micron-sized thin films such as III-V material or pre-processed device coupons, realized on their native substrate in a dense array, such that they can be printed in a massively parallel way to another substrate, leading to improvement in material use and increase in throughput.

To enable transfer printing, a sacrificial release layer is inserted between the GaAs substrate and the epitaxial “half” VCSEL structure. Fabrication starts with processing of the VCSIL (contact deposition, mesa etching, selective oxidation) on the native GaAs substrate (Fig.3a). This is followed by etching through the sacrificial layer (Fig.3b), attachment of polymer tethers and under-etching to release the coupon (Fig.3c), and transfer printing of the coupon to the target substrate using a PDMS stamp. Fig.3d shows a VCSIL coupon successfully printed on a silicon wafer.

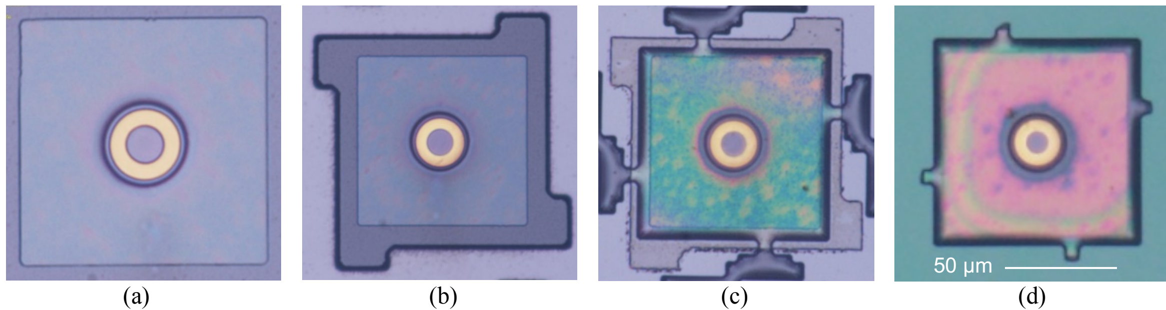

Fig.3 a) Processed VCSIL on source (GaAs) substrate, b) etching through sacrificial layer, c) definition of tethers and under-etching to release coupon, and d) transfer of coupon to target (Si) substrate through transfer printing.

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