Comparator hysteresis compensation for decision feedback equalisers

O.E. Mattia✉, D. Guermandi, G. Torfs and P. Wambacq

High-speed comparators are extensively used in serial link receiver designs. Some comparator architectures can show significant hysteresis that degrade the sensitivity of the receiver, increasing the bit error rate. In this Letter, a comparator hysteresis compensation strategy that re-uses the first tap of a decision feedback equaliser to shift the comparator input voltage, increasing the decision margin is proposed. An updated equaliser coefficient adaptation scheme is also introduced. The proposed technique can be used for binary and multi-level modulations.

Introduction: As serial link data rates are pushed into several tens of Gbit/s, complex equalisation schemes become necessary at the receiver side. A common equaliser is the decision feedback equaliser (DFE), shown conceptually in Fig. 1*a* and schematically in Fig. 1*b*. The basic idea of a DFE is that the comparator makes a decision that represents an estimate of the data. The coefficients on the feedback path form a finite impulse response filter that emulates the channel impulse response (CIR) at I_{TAPS}, which is subtracted from the actual channel output I_{MAIN}, cancelling the inter-symbol interference (ISI). If the CIR estimate is correct then V_{COMP} has no ISI.

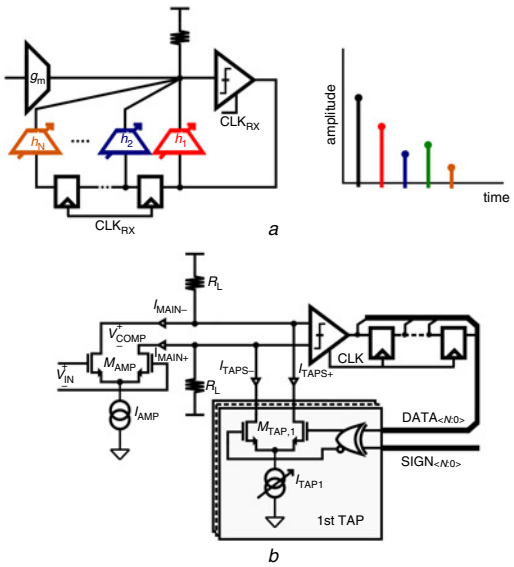

Fig. 1 *Traditional binary decision feedback equaliser*
a concept and channel impulse response
b DFE schematics

The comparator's propagation delay limits the maximum speed at which the DFE loop can be closed [1]. Comparator hysteresis cancellation schemes usually need a reset phase to erase the previous bit decision, decreasing the available time for sensing and comparing. This Letter instead proposes the use of the DFE first tap coefficient to compensate for this hysteresis, as next.

Hysteresis compensation: The basic concept is illustrated in Fig. 2, and consists in shifting the current analogue input signal based on the previous bit decision, maintaining the same 'decision margin'.

In Fig. 2*a*, the decision margin presented to the ideal comparator is equal to $|V_{IN}|$. In Fig. 2 *b*, this margin has been degraded by the hysteresis, and has now become $|+V_{IN}-V_{LH}|$ and $|-V_{IN}+V_{HL}|$, being V_{HL} and V_{LH} the high-to-low and low-to-high thresholds, respectively. In Fig. 2*c*, the hysteresis is compensated by the first DFE tap, shifting the input levels by $V_{HYST}=(V_{LH}+V_{HL})/2$ based on the *previous* bit decision to increase the *next* bit decision margin, as given by $V_{COMP}[k]= R_L(I_{MAIN}[k]-DATA_0[k-1]I_{TAP1})$, where k represents data samples spaced by CLK_{RX}. This results in a higher decision margin for V_{COMP} equal to $|+V_{IN}+V_{HYST}-V_{LH}|$ and $|-V_{IN}-V_{HYST}+V_{HL}|$ for the cases where the incoming data sequence is 01 and 10, respectively. A higher decision margin has a further advantage of decreasing the comparator delay time.

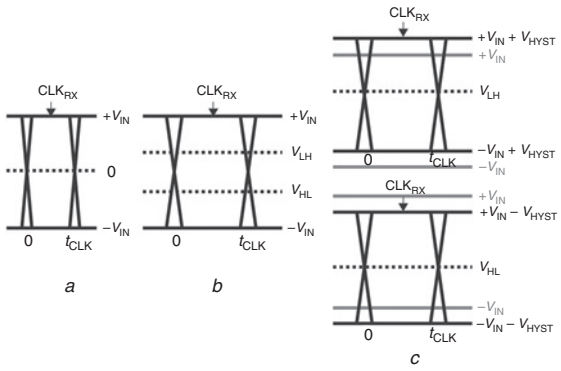

Fig. 2 *Hysteresis compensation by shifting the input voltage to maintain the same decision margin*
a No hysteresis
b With hysteresis
c First tap compensated

Coefficient adaptation: In practice, the DFE taps must be continuously adapted to changes in the environment that result in variations of the CIR. A common way to implement such adaptation consists of an auxiliary comparator C_{AUX} with threshold voltage V_{IN}, that monitors the input eye diagram and correlates its output with the data using a Sign-Sign LMS algorithm [2], as shown in Fig. 3*a*. Suppose the DFE is adapting to a CIR that contains only one tap of post-cursor ISI $k1$. According to the previously described hysteresis compensation scheme, the correct value for the tap coefficient should be overestimated to $h1=k1+V_{HYST}$. However, since the threshold of C_{AUX} is set to V_{IN}, the DFE will converge to the tap value that minimises the error around V_{IN}, resulting in the wrong value of $h1=k1$ and the equalised eye diagram of Fig. 3*b*.

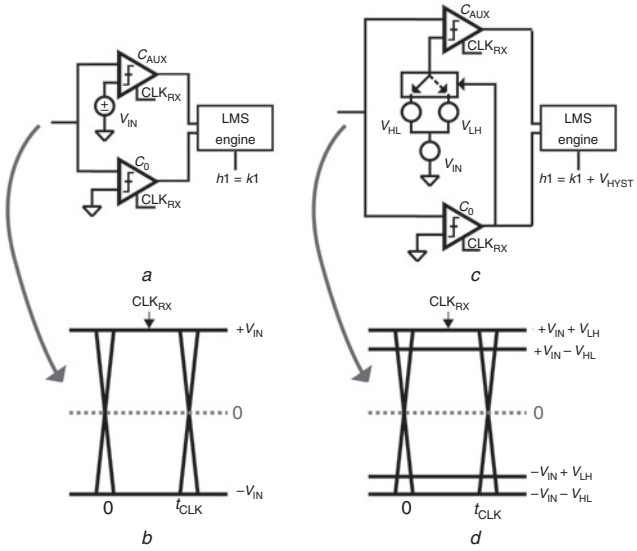

Fig. 3 *DFE adaptation for hysteresis compensation*
a Traditional auxiliary comparator with fixed threshold
b Resulting eye-diagram
c Proposed auxiliary comparator with variable threshold
d Resulting eye-diagram with hysteresis compensation

Instead, we propose the use of a novel adaptive threshold auxiliary comparator, as shown in Fig. 3*c*. The main comparator C0 output is used to shift the adaptive comparator's threshold to that of $V_{IN}\pm V_{HL}/V_{LH}$, resulting in the equalised eye diagram of Fig. 3*d* and thus compensating for the hysteresis of comparator C0, as described previously at Fig. 2*c*. This scheme assumes that the auxiliary comparator C_{AUX} does not have hysteresis. Since the adaptation engine can operate at a fraction of the speed of the data path, the addition of a reset phase is less impactful here.

Simulation results: The proposed hysteresis compensation and tap adaptation scheme was implemented in a behavioural model using Matlab, both for NRZ and PAM4 signal modulations. A 5-tap CIR was assumed, to be compensated by a 5-tap DFE. Shown in Fig. 4*a* is

the actual and estimated CIR, while Fig. 4*b* shows the coefficient evolution over time for the NRZ case. The PAM4 case produces similar results. Note that the first tap is adapted to a higher value than the CIR to compensate for a normalised hysteresis of 0.15.

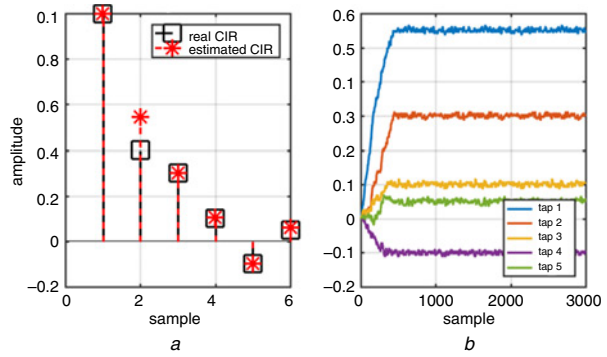

Fig. 4 *DFE adaptation results*
a real and estimated CIR
b coefficient evolution over time

Fig. 5 shows the comparator input voltage during DFE adaptation, for the (a) NRZ and (b) PAM4 cases. Note how initially there is no visible eye margin, while after about 500 samples the input of the comparator converges to the two eye levels described in Fig. 2. In the PAM4 case each DFE tap produces two adittional levels due to the previous data extra possibilities, meaning the hysteresis is fully for half of the data bits, and only partially compensated for in the other half.

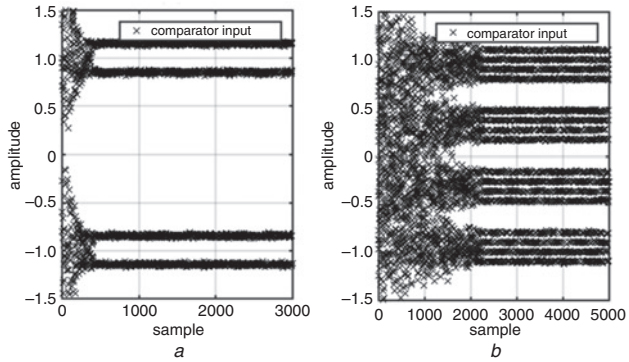

Fig. 5 *Comparator input during DFE adaptation, with hysteresis compensation*
a NRZ
b 4PAM

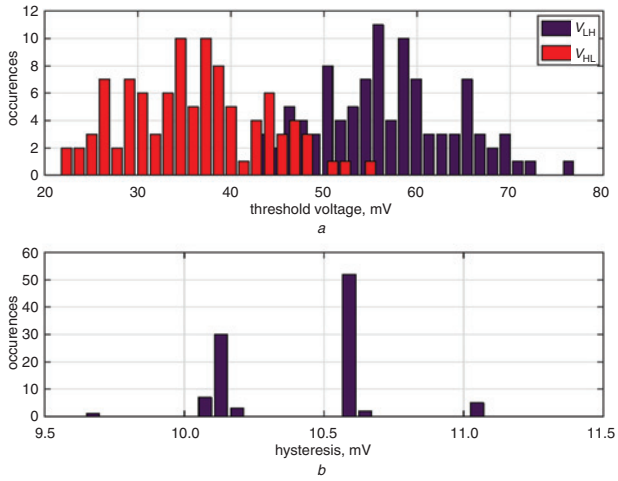

Fig. 6 *Variability results for 100 Monte Carlo runs*
a comparators' threshold voltage
b hysteresis

Experimental results: A hardware implementation of the proposed technique has been demonstrated in a 18/36 Gbit/s QPSK/16-QAM 5-tap DFE fabricated in 28 nm CMOS for mmWave wireless communication. After down-conversion on a homodyne RX, the signal is presented as two I/Q components each containing a NRZ/4-PAM signal [3]. In this design each comparator had a hysteresis of about 10% of the maximum eye level, due to kickback of the CML slave latch and therefore independent of frequency. Shown in Fig. 6 is 100 Monte Carlo simulation runs for both average global effects and local mismatch. Note that even though the offset has a standard deviation of 10 mV the hysteresis is practically insensitive to fabrication variations.

An on-chip PRBS9 generator and checker was used to measure the BER bathtub curves. Shown in Fig. 7 are the experimental results for QPSK and 16QAM signals at the maximum 9 GHz clock frequency.

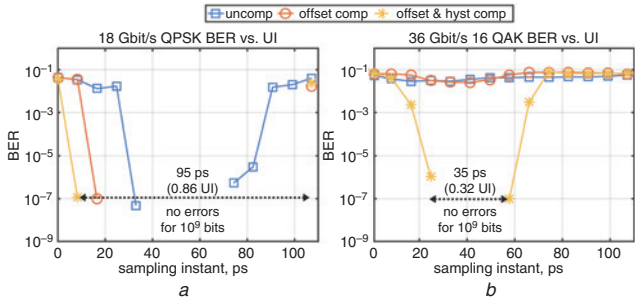

Fig. 7 *Measurement results for 18 Gbps GPSK and 36 Gbps 16 QAM DFE in 28 nm CMOS*

After the comparators' offset has been manually tuned the first tap of the DFE was used to compensate for the expected 10 mV hysteresis. The horizontal eye opening is increased for both cases, demonstrating the effectiveness of the technique using the first DFE tap. Only offset compensation was not enough to receive error-free LSBs on the 16QAM mode due to limited bandwidth of the PRBS generator at the maximum speed. The same measurement was repeated with the same first tap setting but at lower clock speeds of 4 and 1 GHz, to avoid this bandwidth limitation, and including different channel CIRs [3].

Conclusion: This work presented a novel comparator hysteresis compensation scheme for DFE-based serial-link receivers, that allows for a higher receiver sensitivity and lower BER. A novel DFE coefficient adaptation scheme is also introduced to account for the comparator hysteresis. It is demonstrated for NRZ and PAM4 modulations by using a behavioural model and a hardware implementation in 28 nm CMOS.

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One or more of the Figures in this Letter are available in colour online.

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