SWITCHED-CAPACITORS AS LOCAL CONVERTERS FOR SNAKE PV MODULES: A COST/EFFICIENCY EXPLORATION

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ABSTRACT: In order to reduce the negative effect of partial shading and other sources of current mismatch within a module, smart reconfigurable modules allow altering the connections between groups of cells (cell-strings). With a proper algorithm managing these connections, we can make sure that the majority of the cells are operating close to their MPP, even when a part of the module is shaded. Such a smart reconfigurable module consists of some extra components. Switches are needed to change the interconnection scheme. Small, local converters collect power from multiple cell-strings. They step-up the voltage to reduce the current on the central bus they are connected to. At the end where we connect to the string-level bus, a module converter further regulates the voltage for the grid or the PV array. This topology was presented before where we showed that a smart reconfigurable module could recover up to 70% of the power lost to partial shading. In this paper we take a closer look at the local DC-DC converter. More precisely, we present a cost-efficiency analysis of different converter topologies. Taking into account practical limitations (economical limitations, number of components, maximum switch currents, maximum capacitance values, etc..) we estimate efficiency and projected cost. We show that Dickson pump (CR3) with 30-35mΩ switches is the best candidate. This would result in a chip cost of about €1.5

Keywords: DC-DC-Converter, Economic Analysis, Energy Performance, Shading, Configurable Topology

1 INTRODUCTION

A standard silicon photovoltaic (PV) module consists of typically 60 or 72 cells connected in series. While this series connection might result in a more practical voltage-current profile, it is also the cause of the large drop in output power when such a PV panel is partially shaded. A local current mismatch will limit the total PV module current to the one of the shaded cell. The current solution, inserting three bypass diodes [1] in anti-parallel between substrings, is an improvement but is ultimately sub-optimal: (a) even if only one cell of a substring is shaded, the generated power of the entire substring is bypassed, (b) bypass diodes themselves have to carry a large current which leads to additional power loss and possibly heating issues [2] and (c) the insertion of bypass diodes reshape the power-voltage curve creating local maxima [3], requiring more complex Maximum Power Point Tracking (MPPT) algorithms able to track the global maximum. Simple MPPT algorithms [4] such as the Open Circuit Voltage method typically have a low MPPT efficiency (< 90%). More complex algorithms, e.g. Perturb & Observe (P&O), can result in higher efficiency, but require sensing of both voltage and current and might still miss the global MPP. In any case, multiple local MPP and especially fast changing shading patterns are difficult to deal with for these MPPTs. These conditions occur especially in domestic PV plants or urban-integrated PV arrays, such as Building Integrated PV (BIPV).

Another approach to mitigating this issue, one that is evidenced at recent Solar Industry exhibitions, is the move towards so-called 'smart PV modules'. In these smart modules, the power optimizers or micro-inverters are integrated at module level, and not at the array level. The MPPT is performed at module level as well, resolving the inter-module current mismatch problems. Intra-module current mismatch can be addressed by replacing bypass diodes with local optimizers [5]. However, the granularity is still fairly limited and comes at a relatively high cost.

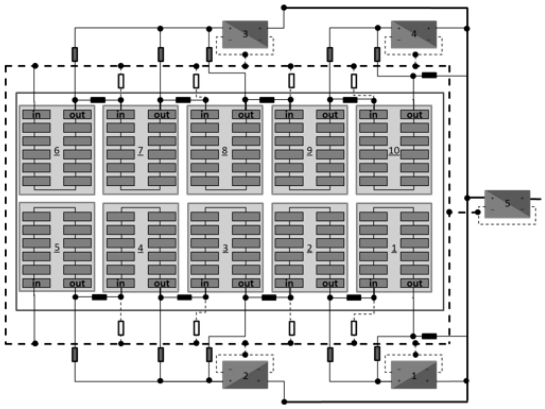

Figure 1: Smart reconfigurable module topology, using switches (small boxes), local converters (boxes 1, 2, 3, 4)

Going a step further, we arrive at the concept of reconfigurable topologies. In such a topology, multiple run-time configurations are enabled, depending on the current operating condition, thus allowing the majority of the cells operation at their MPP. Ideally, every cell can be connected to every other cell, but this would require an unreasonable amount of connections, switches, etc. The most suitable granularity level has to be explored by taking into account the increased manufacturing cost, the increased losses due to resistivity and addition of dynamic elements such as the switches and local DC-DC converters. While some approaches to a reconfigurable smart PV module have been presented in literature [6], the optimal trade-off between realization cost and improved energy output is still not clear. We previously published an approach that takes these aspects into account [7] (Figure 1). These modules are able to establish different interconnection schemes along small groups of cells (cell-strings). These connections can be either in parallel or in series by use of switches. The intra-module converters ensure suitable current and voltage level and allow a direct

control of the operating point of the cell-string. They are connected in parallel to the module level converter via a central bus. The module converter can be used for the connection with either the grid or the rest of the PV array. Under non-uniform conditions, this reconfigurable topology can recover up to 70% [8] [9] of the power that was lost in a traditional configuration. It is clear that these topologies are only relevant if we succeed in keeping the cost of the different elements as low as possible. Also here there is a clear trade-off between cost and efficiency. In this paper we take a closer look at the cost-efficiency optimization of the local converter. We examine different converter topologies and estimate their cost and efficiency.

2 TOPOLOGIES

2.1 General

The goal of the local converter is to have a very cheap (~€1) solution that regulates the cell-strings output current to be conformable with the module converters specifications. A lower current on the central bus also implies lower resistive losses. It is important to note that since the outputs of these local converters are connected in parallel, such converters will not integrate any output voltage control algorithm. This voltage will be determined instead by the module converter. The local converters conversion ratio will thus determine the cell-string voltage.

We are aiming at a low-cost fully integrated solution (PowerSoC). As inductors are bulky and integrated inductors are costly, we opt for a switched-capacitor solution. In the following sections, we take a closer look at the investigated topologies. Different topologies have different conversion ratios, number of components (switches, capacitors), require different current levels, generate different switching losses, etc.. Higher conversion ratios typically mean lower bus currents and module converter currents, but higher converter complexity and cost.

2.2 Ladder converter

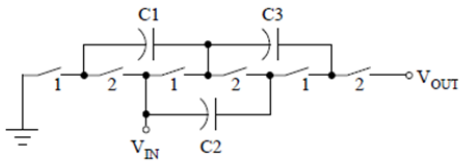

Figure 2: Ladder topology with conversion ratio 3

The ladder topology (Figure 2) achieves a fixed conversion ratio for a specific input node. Changing the input source (Vin) can alter the conversion ratio. This topology is suitable also for non-integer conversion ratios m:n. The odd-numbered switches are turned on during phase 1, the even-numbered switches during phase 2. The number of capacitors and switches needed to achieve a conversion ratio of n is 2n-3 and 2n respectively. All capacitors and switches support a voltage equal to the input. For smaller conversion ratios, this topology uses few switches, but quite a lot of capacitors.

2.3 Dickson charge pump

The Dickson charge pump is mostly known for 1:n conversion ratios. Like the ladder, the odd-numbered switches turn on during phase 1 and the even numbered

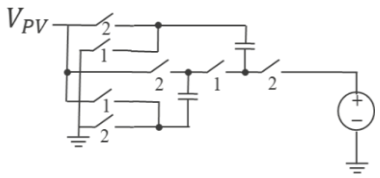

Figure 3: Dickson charge pump with conversion ratio 3

switches turn on during phase 2. The Dickson topology has the advantage of using fewer capacitors for the same conversion ratio compared to the Ladder topology. In general, for a fixed conversion ratio n, the Dickson pump uses n-1 capacitors and n+4 switches. The capacitor in the lowest stage supports the input voltage, while the rest support twice the input voltage. The blocking voltage of the switches is either the input voltage or twice the input voltage.

Other topologies such as the series-parallel converter, connecting all capacitors in parallel to the input voltage in the first stage and connecting them in series in the second stage, typically require too many switches to be cost-effective here

3 METHODOLOGY

3.1 Cost

In a switched-capacitor converter, the cost is defined by the cost of the capacitors and switches. As we are aiming for an integrated converter, we assume a HV planar integration chip technology for the MOSFET switches. A very rough estimate puts the cost on €0.1/mm² die area. When designing for low on-resistances (larger area of MOSFET), we can assume that the die area is inversely proportional to the on-resistance (about 69Ωmm²). Therefore we can state that the main drivers of the cost are the MOSFETs' on-resistance and the number of components. The cost of the capacitors will mainly be determined by their number, not so much by their exact value. Note that the switches will dominate the cost, well above the other components. See also Figure 5.

3.2 Efficiency

The different topologies are simulated using realistic models for the capacitors and switches. The main contributors to the power losses are the conduction losses and the switching losses. Eq. (1), with R_{ON} the on-resistance of the MOSFET, ESR_{CAP} the series resistance of the capacitor, N_{SW} and N_{CAP} the number of switches and capacitors respectively and I_{PV} the PV input current, and Eq. (2), with V_{SW} the voltage swing of the switches, I_{SW} the current through the switches and f_s the switching frequency, represent the conduction losses and the switching losses of a ladder with conversion ratio 2, respectively.

$$P_{loss,Cond} \approx \left(N_{SW} \cdot \frac{R_{ON}}{2} + N_{CAP} \cdot ESR_{CAP}\right) \cdot I_{PV}^2 \quad (1)$$

$$P_{loss,Switch} \approx g(R_{ON}, V_{SW}, I_{SW}) \cdot N_{SW} \cdot f_s \quad (2)$$

It is clear from these equations that factors that increase the efficiency, will also increase the cost, which is why this cost-efficiency analysis is useful for further development of the local converter. It is worth to note that, for the value of capacitance we need, in the order of tenths of µF, and the RMS current they have to process, low ESR capacitors will be used. Thus, their impact on the converter losses is significantly lower than the one of the MOSFETs'

on-resistance.

4 RESULTS

Even though Eq. (1) and Eq. (2) refer specifically to a ladder with conversion ratio 2, they can be used to make some observations that can be extended to any of the switched-capacitors topologies we studied, helping to reduce the solution space. The conductions losses can be lowered by reducing the input current, which is done by using half-cells (See Figure 1). It is also clear that the number of components (N_{SW}, N_{CAP}) should be as low as possible; this not only lowers the power loss, but also reduces the cost of the converter. For this reason, we limit ourselves to the conversion ratios 2, 3, and 4. The on-resistance of the MOSFET affects not only the conduction loss, but also the switching losses. A lower on-resistance seems beneficial, but also increases the cost. On top of that, large MOSFETS with a low on-resistance have a large gate, requiring a larger current to be driven at a certain frequency. The frequency itself also poses limitations on the system: a smaller frequency requires larger capacitors; a higher frequency requires larger gate currents. For practical reasons we want the capacitors to be smaller than 100µF, and a gate current in the 250mA to 500mA range. Figure 4 shows achievable switching frequencies for a certain maixmum gate current. For switches of 30-35mΩ, the switching frequency will be around 200kHz.

For a conversion ratio of 2, the ladder topology reduces to a simple H-bridge, with 1 capacitor and 4 switches. Simulation showed that a conversion ratio of 3 and 4 was more efficient using the Dickson charge pump, using 7 and 8 switches respectively. An extra capacitor is needed at the input to smooth the voltage ripple. The projected cost of these converters is depicted in Figure 5.

For all topologies we assumed an irradiance of 1000W/m². Upper and lower boundaries were defined by connecting the local converter to a single cell-string, or to a double cell-string (2 cell-strings in parallel, doubling the current, see Figure 1). For each topology, we determined a solution point were the balance between MOSFET on-resistance, cost and efficiency is optimal. Table I collects the results.

For each topology, the module converters (MC) input voltage is shown. This is the voltage that the module converter should fix, in order for the cell-string to operate

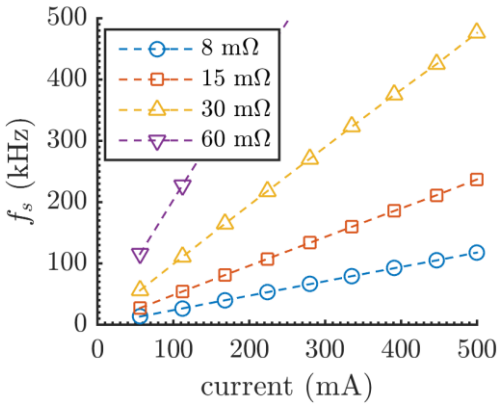

Figure 4: Maximum switching frequency versus the needed maximum gate current for MOSFETS with different on-resistances

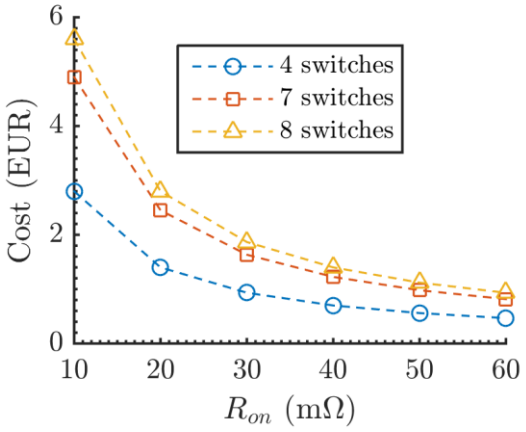

Figure 5: Projected converter cost for converter with different amounts of switches and their on-resistances

at its MPP. Together with this, also the MOSFET maximum current is shown, allowing us to estimate the feasibility of a fully integrated converter.

The results above are for an irradiance of 1000W/m² but they can be easily reprojected for other irradiance levels. The whole point of the reconfigurable module is to only activate the local converters when there is an partial shading. This implies that the local converters will often work in conditions lower than 1000W/m². Simulation shows that the efficiencies in Table 1 increase by 1-2% when the irradiance is decreased due to lower conduction losses. For very low irradiances (<300W/m²) this effect is less obvious mainly due to the larger relative effect of the switching losses (See Figure 6).

5 CONCLUSION

The above analysis effectively uses a worst-case scenario to select the most promising solutions for the local converter in the smart reconfigurable module. The selection is based on chip cost, converter efficiency, requirements and limitation due to cell-string and module converter characteristics. At the same time, the converter parameters as MOSFET on-resistance, switching frequency and capacitor sizing are determined for the

Table I: Overview of the optimization results for conversion ratios 2, 3, and 4. Underlined values indicate corresponding extremes of the range

Topology	Ladder (CR2)	Dickson (CR3)	Dickson (CR4)
Capacitors	1 (2) <70µF	2 (3) <100µF	3 (4) <120µF
Switches	4	7	8
R_on (mΩ)	[20 ÷ 36]	[30 ÷ 35]	[32 ÷ 34]
η_min @MPP (%)	[89 ÷ 93]	[89 ÷ 91]	[89 ÷ 90]
Chip cost (€)	[0.76 ÷ 1.37]	[1.37 ÷ 1.60]	[1.61 ÷ 1.95]
MC volt. @MPP (V)	[10.4 ÷ 11.6]	[15.5 ÷ 17.5]	[20.5 ÷ 23.5]
SW current @MPP (I)	[8.5 ÷ 9]	[11 ÷ 13]	[11 ÷ 13]

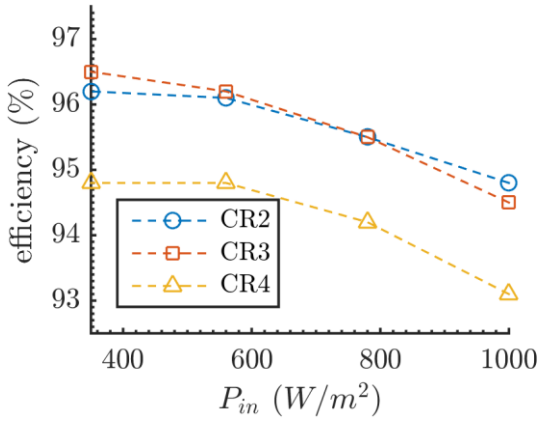

Figure 6: Converter efficiencies as a function of input power

selected topologies. Ladder and Dickson topologies allow for a lower number of components, reducing the cost and related losses. To reduce the constraints posed on the module converter, a conversion ratio of at least 2 should be considered. With this, we show that Dickson pump (CR3) with 30-35mΩ switches is the best candidate. This would result in a chip cost of about €1.5. The downside of this approach is the fixed conversion ratio. In future work, we are looking at topologies for multiple conversion ratios. This may require more components, but the energy trade-off will be larger as well.

5 ACKNOWLEDGEMENTS

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6 REFERENCES

[1] E. Diaz-Dorado, A. Suárez-García and C. Carrillo, "Influence of the shadows in photovoltaic systems with different configuration of bypass diodes," in *2010 SPEEDAM*, 2010.

[2] K. Kim and P. Krein, "Reexamination of Photovoltaic Hot Spotting to Show Inadequacy of the Bypass Diode," *IEEE J. Photovolt.*, vol. 5, no. 5, pp. 1435-1441, 2015.

[3] B. A. Alsayid, S. Y. Alsadi, J. S. Jallad and M. H. Dradi, "Partial Shading of PV System Simulation with Experimental Results," *Smart Grid and Renewable Energy*, vol. 4, no. 6, pp. 429-435, 2013.

[4] A. Reisi, M. H. Moradi and S. Jamasb, "Classification and comparison of maximum power point tracking techniques for photovoltaic system: A review," *Renewable and Sustainable Energy Reviews*, vol. 19, pp. 433-443, 2013.

[5] Jinko, "http://www.jinko-smart.com/maxim.html".

[6] R. Dorn, "Photovoltaic module utilizing a flex circuit for reconfiguration". Patent WO/2008/076301, 2006.

[7] M. Baka, F. Catthoor, D. Soudris and A. Papanikolaou, "Configurable Module Topology to Recover Power Lost due to Current Mismatch," in *29th EUPVSEC*, Amsterdam, 2014.

[8] M. Baka and F. S. D. Catthoor, "Smart PV Module Topology with a Snake-Like Configuration," in *31st EUPVSEC*, Hamburg, 2015.

[9] P. Bauwens, J. Govaerts, M. Baka, F. Catthoor, K. Baert, G. Vandenbroeck, H. Goverde, D. Anagnostos, J. Doutreloigne and J. Poortmans, "Reconfigurable Topologies for Smarter PV Modules: Simulation, Evaluation and Implementation," in *32nd EUPVSEC*, Munich, 2016.