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ASIC Design to Support Low Power High Voltage Power Supply for Radiation Monitoring Applications

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ASIC DESIGN TO SUPPORT LOW POWER HIGH VOLTAGE POWER SUPPLY FOR RADIATION MONITORING APPLICATIONS

by

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ASIC DESIGN TO SUPPORT LOW POWER HIGH VOLTAGE POWER SUPPLY FOR RADIATION MONITORING APPLICATIONS

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A low power high voltage power supply is designed for use in a long duration radiation monitoring system. The supply employs a flexible pulse frequency modulation switching controller implemented in a 0.35 μm CMOS technology. The controller drives and regulates a flyback transformer driven 12-stage Cockroft-Walton voltage multiplier chain. The chain provides bias for the dynodes of a photomultiplier tube. The supply voltage is selectable via a 12-bit on-chip digital to analog converter. The system is designed for low power operation and immunity to supply voltage variation as the application is battery-powered.

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Chapter 1

Introduction

1.1 Radiation Monitoring

Radiation monitoring systems are used to detect ionizing radiation and quantize the rate of irradiation as well as characterize the source of the radiation based on the collected energy. These systems generally consist of a detector, a charge amplification device which may require high voltage biasing, an analog front end, and a digital processor. In a radiation detector, the individual radiation particles, such as alpha particles and gamma-ray photons, interact with the material or device. Depending on the detector, several different interactions occur that produce a quantifiable charge pulse. In gas-filled radiation detectors, the gas is ionized and produces a measurable current. Semiconductor detectors use specially doped reverse biased diodes to detect radiation that produces free electrons and holes. In scintillation based detectors, the incident radiation causes the material to produce lower energy photons as shown in Figure 1.1. Some of these photons are then converted to photoelectrons by a photocathode. The power supply described in this thesis is designed for this type of detector. The amount of photons and, consequently, the amount of photoelectrons

produced is proportional to the energy of the incident radiation particle.

A photomultiplier tube (PMT) is then used to multiply this photocurrent produced by the photocathode. A PMT consists of a sealed vacuum tube with a sensitive photocathode at one end, a focusing electrode, and a series of metal plates known as dynodes arranged as an electron multiplier that terminate in an anode at the opposite end. The dynode closest to the focusing electrode is biased at a potential ˜100 volts relative to the electrode. Each dynode in the multiplier is biased at a similar voltage relative to the preceding one. This bias voltage draws the photoelectrons to the first dynode. The electrons strike the dynode and are multiplied by secondary emission. This repeats at each dynode stage to produce a total gain of up to $\tilde{}10^6$. The anode is held at the highest potential and is where the resulting charge pulse is measured.

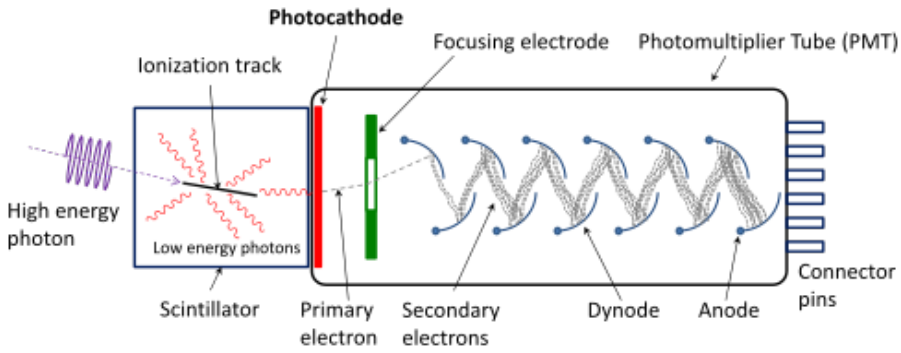


Figure 1.1: Scintillator coupled to a Photomultiplier Tube

A sensitive analog front end (AFE) is then used to amplify and shape the pulse before it is sampled and quantized. The digital processor uses the rate and height of these pulses to characterize the incident radiation. A pulse height histogram can be used to estimate the energy content or spectrum of the collected radiation and identify the isotope of the source. In the desired application for this work, a custom ASIC multichannel analyzer (MCA) integrates a microcontroller with several low power AFEs so the processing can be done at the source [1].

1.2 Photomultiplier Tube Biasing

Each dynode in a PMT must be held at a constant DC voltage. The voltage applied to each dynode directly impacts the gain of a PMT. Any variation will result in a modulation of the overall gain and, therefore, the signal amplitude. This effect can be ignored to some extent in pulse counting applications. However, when creating a pulse height spectrum, modulation of the signal amplitude will smear signal height peaks of the collected histogram, reducing the certainty of the peak location. Figure 1.2 shows a typical biasing scheme for a PMT. A high voltage DC supply is applied to a string of resistors configured as a voltage divider. Each stage of the PMT is biased by a separate tap of the divider. The resistors are sized such that the time constant of the dynode capacitance and resistive divider is much less than the length of an expected charge pulse. For this reason, the resistive divider dissipates a significant amount of power on the order of 1 W. This leads to a significantly shorter run-time for battery powered monitoring applications. This excludes this design from consideration even without considering the power dissipation and efficiency of the high voltage DC supply itself.

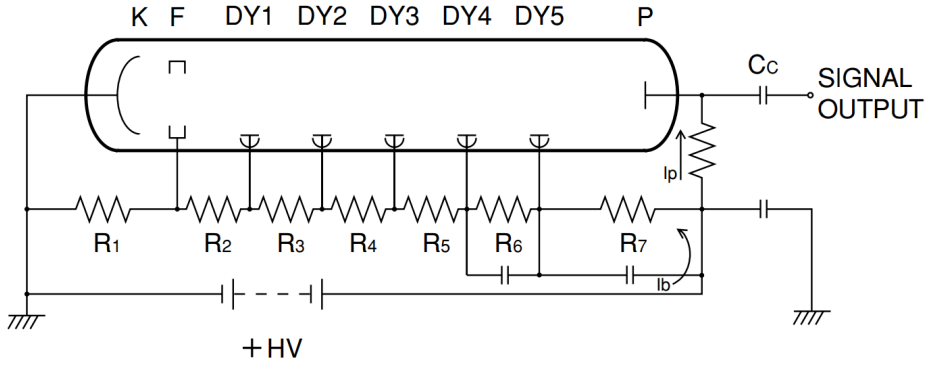


Figure 1.2: Common PMT biasing scheme

1.3 High Voltage Supply Designs

The high voltage DC supply required to bias the PMT stages must meet several requirements for a battery-powered radiation monitoring application. It must have low output ripple. Any ripple on the output will result in some degradation of the pulse height spectra. The supply must be efficient and consume very low power. In a monitoring application designed to run for weeks at a time using a compact battery, the total power drawn is limited to milliwatts.

There are a few common schemes used in converting a low voltage to a high voltage. The first and most common is the boost converter. The scheme stores energy in one phase by charging an inductor as shown in Figure 1.3. The current flow is then interrupted by the switch opening. The magnetic field in the inductor collapses and it attempts to maintain current flow in the same direction by raising the voltage connected to the diode with respect to the input. When this voltage across the inductor rises to a greater voltage than the output voltage plus the diode voltage, the capacitor is charged with the energy stored in the inductor. With proper component selection and switching frequency, this topology can efficiently generate a voltage with low ripple.

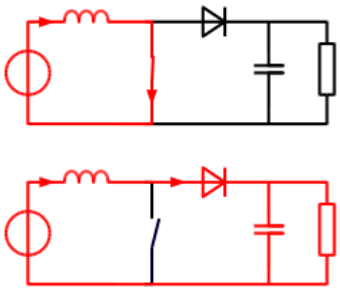


Figure 1.3: Boost converter switching states.

However, battery-powered radiation applications need to be provided a voltage up

to 1kV from a coin cell battery voltage ˜3V. Achieving this from a boost converter would require a combination of odd part sizes as well as large input current that most batteries cannot sustain.

Replacing the inductor in the boost converter with a transformer results in what is know as a flyback converter. The operation of this converter is shown in Figure 1.4. Like in the boost converter, first energy is stored in the primary. No current can flow in the secondary, however, due to the diode. The primary circuit is then interrupted and again the primary develops a voltage across it to maintain the same current flow. This voltage is coupled through the flux linkage of the transformer core to the secondary. The magnitude of the voltage is stepped up or down according to the turns ratio of the transformer. This voltage increases until the diode is forward biased and the energy is transferred from the secondary to the output capacitor.

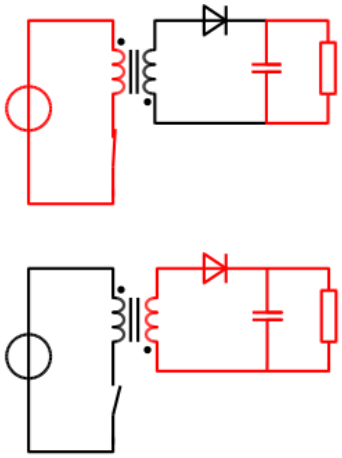


Figure 1.4: Flyback converter operation.

When using a step-up transformer, this enables the generation of higher voltages than a boost converter at a given input current. Again, this input current becomes much too large at when considering generating 1kV from a coin cell. Additionally, the load current of the resistive divider used for PMT biasing would consume more

power than the topology could provide at high voltages.

In order to overcome the limitations of the coin cell battery, high voltage necessary for PMT biasing, efficiency, and low ripple requirements, the work detailed in the following combines a flyback converter with what is known as a Cockcroft-Walton voltage multiplier. This scheme generates the high voltage required for the the final anode bias of the PMT as well as each dynode bias inherently without the use of a dissipative resistive divider.

1.4 Organization of Thesis

The following chapters discuss the architecture and design of the high voltage power supply. First, the switching supply topology is discussed and reasons are given for choosing it. Next, an overview of the switching power supply controller ASIC architecture and design is given. The design of the reference DAC used to set the output voltage is highlighted in the next section. Then, the circuit boards used to test the design are discussed briefly. Following that, a chapter is dedicated to examining simulation and testing results. Finally, the concluding chapter summarizes the design and results as well as how the supply may be used in future work.

Chapter 2

Architecture and Design

2.1 Cockcroft-Walton Voltage Multiplier Switching Supply Topology

The high voltage supply is based on a Cockcroft-Walton voltage multiplier switching converter similar to [2]. This is implemented using a custom ASIC that switches an external MOSFET which drives the primary of a 1:50 transformer. The secondary of this transformer is connected to a cascade of capacitors and diodes in the configuration shown in Figure 2.1. This is known as a Cockcroft-Walton multiplier. The pulse delivered from the low voltage primary to the secondary through the coupled inductors is stepped up ˜50 times to a high voltage. This voltage pulse on the secondary rings and swings from positive to negative. This alternately charges each capacitor through the string of diodes.

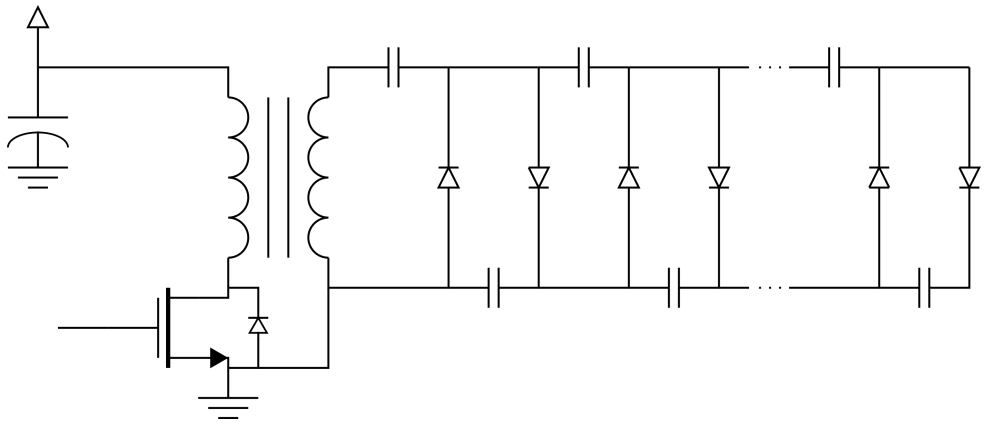


Figure 2.1: Cockcroft-Walton Voltage Multiplier Schematic.

2.1.1 Primary Section

To begin to understand how this topology works, we will first look at the primary side. To transfer energy to the secondary, we first store that energy in the primary coil. This is done by connecting one side to a battery and bypass capacitor and the other to the drain of a high speed, low on-resistance NMOS transistor as shown in Figure 2.2. This allows for the control of when and how much energy is stored in the primary through switching the voltage at the gate of the transistor on and off. This control is achieved via the ASIC that is the focus of this work.

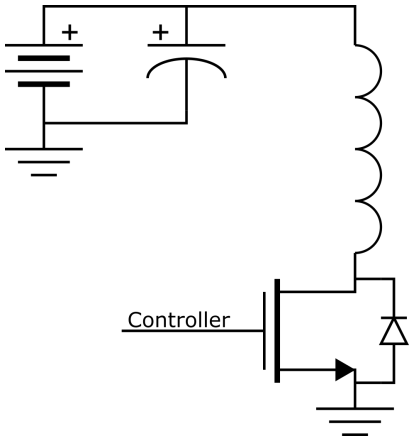


Figure 2.2: Schematic of the primary section of the supply.

Several considerations must be made when designing this circuit and the controller for it. Each component must be selected with the desired power consumption, power delivery, efficiency, and application in mind. Since the application uses a coin cell battery, a limited amount of current can be delivered and, thus, a limited amount of energy can be stored in the primary coil. However, the primary itself can only handle a certain amount of current. With this in mind, the control circuit must be designed to limit the time the MOSFET is on so as to not overheat the primary coil or overload the battery.

2.1.2 Secondary Cockcroft-Walton Voltage Multiplier

The secondary section is shown in Figure 2.3. The pulse from the primary is coupled to the secondary. However, due to the difference in the number of coils, the voltage is multiplied by about 50 resulting in 75V-150V across the secondary. The secondary is connected to a Cockcroft-Walton Voltage Multiplier circuit in order to multiply this voltage up to the voltage needed by the PMT anode.

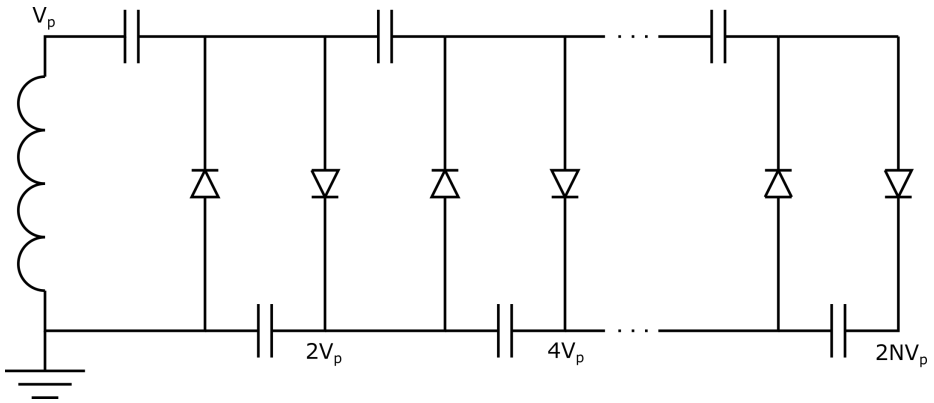


Figure 2.3: Schematic of the secondary section that utilizes a Cockcroft-Walton Voltage Multiplier topology.

Fortunately, the Cockcroft-Walton Voltage Multiplier also produces a voltage at roughly integer multiples of the input voltage which are used to bias the intermediate

dynode stages of the PMT. This eliminates the need for a voltage divider circuit that is normally needed to bias the dynodes and which dissipates a significant amount of wasted power.

The circuit functions by alternately charging different sides of the capacitors in each stage via the diodes. Lets consider a single stage as shown in Figure 2.4.

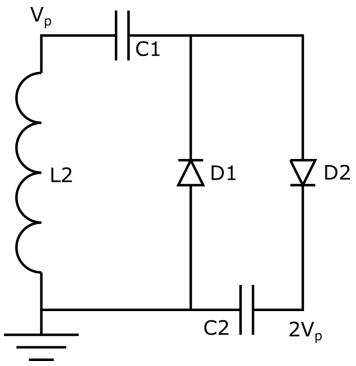
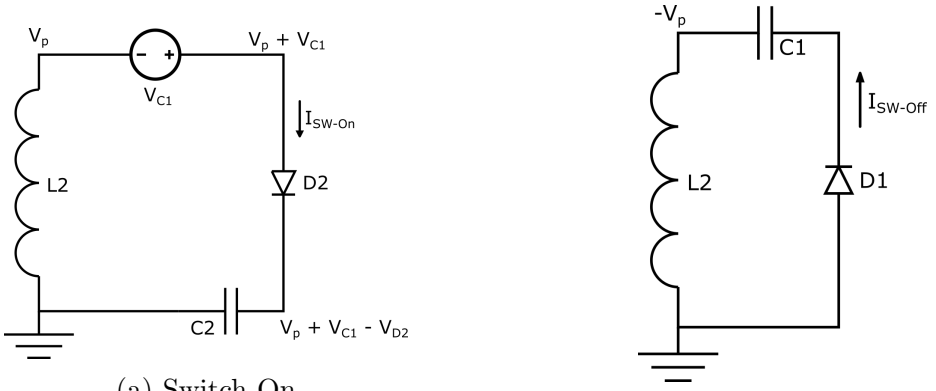


Figure 2.4: Single stage of Cockcroft-Walton Multiplier.

When the gate of the MOSFET is switched on, the first stage, in isolation from the other stages, has an effective circuit shown in Figure 2.5a. A voltage appears across the primary and is coupled to the secondary as a much higher voltage. This voltage is positive with respect to ground and biases the second capacitor with a positive voltage. This leads the left plate of the capacitor to lose charge to ground and thus "charge" up to a positive voltage with respect to ground. During this time, the primary is storing energy in its magnetic field.

At the end of the switching period, the MOSFET is turned off and the voltage across the primary collapses. This is mirrored in the secondary. However, since the secondary coil still has energy stored in its magnetic field, the voltage swings below ground and then back above and so on until the energy is dissipated. This is known as ringing. When the voltage swings below ground, the first capacitor effectively has a positive voltage bias across its plates as shown in 2.5b. This causes the right plate



(a) Switch On

(b) Switch Off

Figure 2.5: Switching states of Cockroft-Walton multiplier stage.

of the capacitor to charge up to a positive voltage with respect to ground.

This charging process continues so long as the ringing voltages are larger than the current capacitor voltages plus the diode voltage drops.

2.2 Switching Power Supply ASIC Design

The unique application required the design of an application specific integrated circuit (ASIC) to control the switching of the MOSFET in order to regulate the output voltage of the supply. Switching controllers are a very common and widely available integrated circuit. However, none were found that were flexible enough to meet the lower power and small load requirements of this application.

Common switching controllers use a voltage feedback scheme to monitor the voltage they are regulating. However, they generally do so using resistive voltage dividers that dissipate more power than our entire application. Therefore, a different, current based, feedback design was conceived. This design uses a very high resistance feedback resistor to generate a feedback current that is summed with a reference current in order to generate an error current. This error current is subsequently used to deter-

mine the switching rate. This feedback current is still the dominate power dissipation in the design but is significantly less than that of a resistive voltage divider and allows the controller to achieve a reasonable efficiency.

It is also common for switching controllers to use a constant frequency variable pulse width scheme to drive the MOSFET. In this way, the pulse width determines the amount of energy transferred during each period. However, this limits the efficiency at lower loads as the switching losses in the inductors and switches are constant. Instead, this design implements a pulse frequency modulation scheme. This limits the switching losses at low load at the expense of output voltage ripple [3]. Ripple can be mitigated to some extent using external resistors and capacitors.

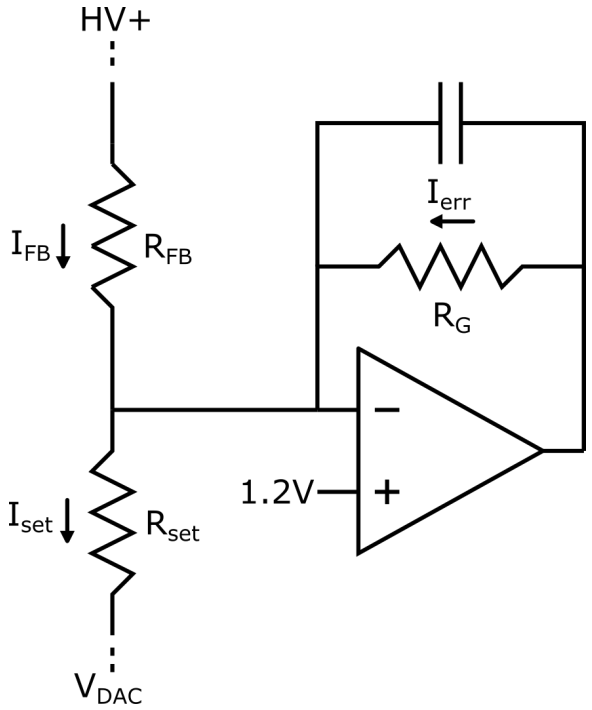


Figure 2.6: Switching Controller Error Amplifier

In this design, shown in Figure 2.6, the inverting terminal of an operational amplifier is used to sum the feedback current from the output via R_{FB}, the reference current generated by a user controlled DAC and resistor R_{set}, and the error current

that is delivered via a resistor R_G from the output of the amplifier. The non-inverting terminal is connected to a band gap reference with a voltage of 1.2 V. In this way, the amplifier is in the common non-inverting configuration and therefore attempts to maintain the same voltage on both terminals. If the output voltage is above or below the desired set point, there will be a difference between the feedback current and the reference current. To maintain the inverting terminal at 1.2 V, the output of the amplifier will swing low or high in order to sink or source the error current through the amplifier's feedback resistor. All of these resistors are off-chip and can be selected to match the desired output voltage range to the reference DAC voltage range. The amplifier feedback resistor value sets the error voltage magnitude and, as will be seen, the frequency and response of the controller. An on-chip capacitor is added across R_G to maintain stability.

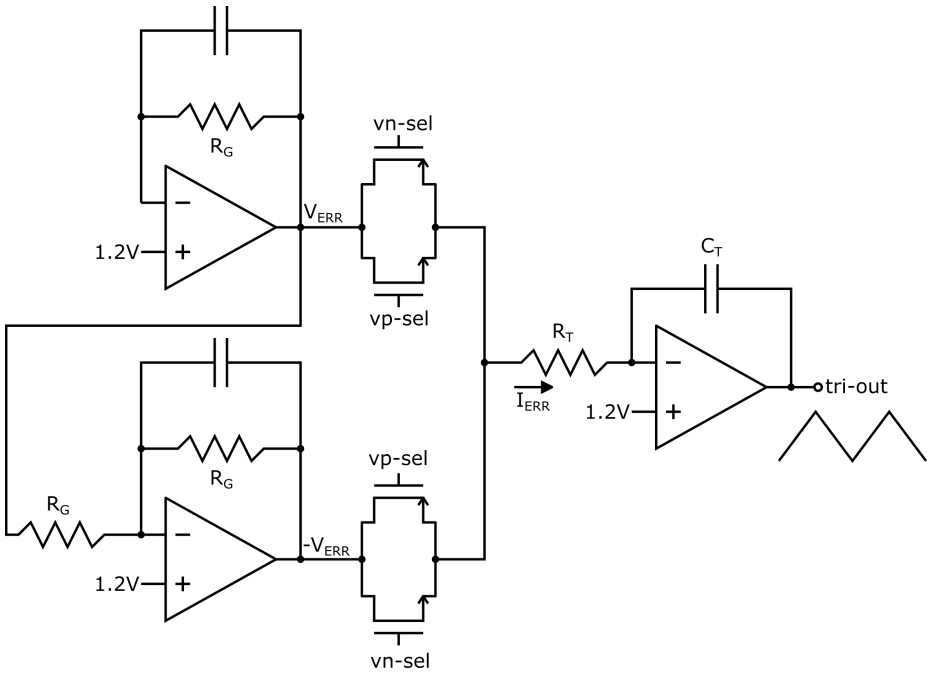


Figure 2.7: Triangle wave generator with frequency proportional to error voltage.

The error voltage is fed to another op amp to be inverted. The bipolar error

voltage is then used to control a voltage-controlled oscillator. This is achieved via a triangle wave generator as shown in Figure 2.7. Depending on the current state, a finite state machine (FSM) selects either the positive or negative error voltage to be connected to one end of an on-chip 10k resistor R_T via two transmission gates. The other end of R_T is connected to the inverting input of a third operational amplifier. An off-chip capacitance C_T is then connected from the inverting terminal to the output of the op amp. The 1.2 V band gap reference is again connected to the non-inverting terminal of this op amp. This results in what is known as an integrator. The difference between the error voltage and the band gap voltage creates a current through the 10k resistor. This causes the output of the op amp to produce an identical current that charges or discharges the output side of the capacitor. This produces an approximately triangular waveform at the output. C_T controls the charging rate and, thus, the frequency range of the controller.

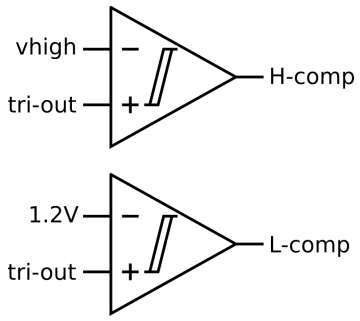


Figure 2.8: Comparators to monitor triangle wave voltage.

This triangle voltage is monitored by two comparators shown in Figure 2.8. One, the low comparator, is set to trip at the band gap voltage for when the triangular waveform is decreasing and the other, the high comparator, is set to an off-chip determined value set between the band gap voltage and the positive supply rail. A small amount of digital logic implements the FSM that takes these comparator outputs as inputs. The state transition diagram is shown in Figure 2.9.

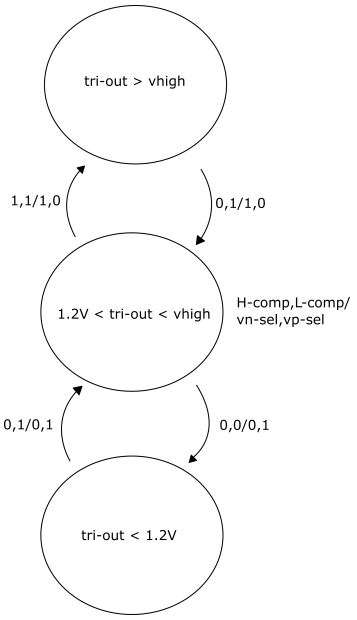


Figure 2.9: State transition diagram of triangle wave generator FSM.

When the control signals to the transmission gates change state, the FSM generates a short pulse to a monostable circuit shown in Figure 2.10 which latches one end of an off-chip capacitor to ground while the other is connected to the positive supply rail through an off chip resistor. This circuit also turns the external MOSFET on. The capacitor charges up to the turn on point of a digital logic gate which then sets the output to the MOSFET low. In this way, the external RC combination sets a fixed pulse width and, thus, an approximately constant amount of energy through the transformer and into the Cockcroft-Walton voltage multiplier chain to charge the output.

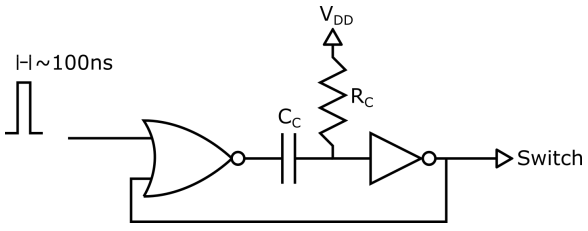


Figure 2.10: Monostable pulse circuit for driving the external MOSFET.

Selection of several external components allow this controller to be used and tuned for a variety of applications. The reference, feedback, and error current magnitudes can all be set via external resistors. Both the positive and its generated negative error voltage magnitudes can be set by external resistors. This magnitude, combined with the external capacitor used in the integrator and the high comparator set voltage control the limits of the switching frequency. Finally, the external resistor-capacitor circuit controlled by the digital logic sets the pulse width of the switching pulse. All of these must be carefully selected based on output voltage, power consumption, load, load regulation, EMI, and other factors specific to the application.

2.3 DAC Design and Implementation

The reference current used to set the desired output voltage in initial versions of the controller chip was determined via an off-chip digital-to-analog controller (DAC) and resistor combination. The application processor communicates with the DAC to set a voltage at its output. The difference between this voltage and the 1.2 V band gap voltage maintained at the inverting terminal of the error amplifier generates a reference current proportional to the resistance used to connect the voltages. This DAC consumes 750 μW and so, in long term battery testing, lowered the run time of the application. It is also desirable to have a more compact one chip solution for the controller. So, it was determined the reference DAC could be implemented on-chip in order to lower the power consumption and fit it more closely to the application.

2.3.1 DAC Requirements Overview

Due to application constraints, the DAC has to meet several requirements and specifications, some unique. As this was designed to be coupled with a specific MCA and

application, testing was done to determine the number of bits needed to control the output voltage with the required precision. The 12-bit reference DAC was used to shift the bin location of a Cs-137 peak which is generally used for calibration. The resulting bin shift normalized to our 10-bit MCA is shown in Figure 2.11.

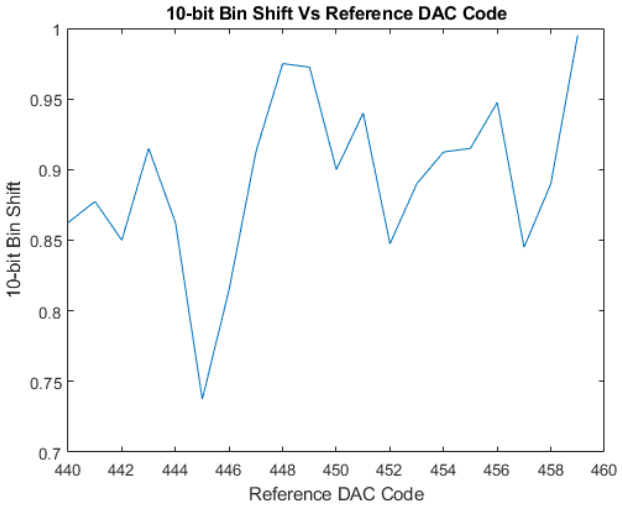


Figure 2.11: Reference DAC code and the resulting bin shift in the CS-137 histogram.

It can be seen that there is ˜1 bin shift per code. Each code corresponds to a 800 μV change in reference DAC voltage. In order to be able to shift an energy peak by 1 bin, the reference DAC will need to have a voltage resolution of 500 μV which corresponds to a change in output voltage of 0.5 V.

As the application is battery powered and the supply rail is potentially unregulated, the reference current must be designed with immunity to this shift in voltage. As there is already a band gap generator used in the design, it is used to determine the full range of the DAC. A potential problem with this is that it limits the references currents to those corresponding to a positive output voltage. However, in the particular application we are able to strictly use positive voltages.

Another consideration is the power consumption of the DAC. The overall system must be below 1 mA in order to meet the required battery powered run time. So, any

additional components added to the chip must not increase the power consumption substantially and must certainly be below or competitive with off-chip alternatives.

Process, voltage, and temperature (PVT) variations limit the performance of the DAC. Process variations are the result of small differences in manufacturing from wafer to wafer as well as from one part of the wafer to another. Temperature differences originate from external temperature fluctuations and from self-heating of the die. These can be mitigated by careful layout to average the effects over the whole DAC. Voltage variations come from supply voltage noise and, in our application in particular, changes in battery voltage. These can be addressed by proper supply bypassing and deriving the DAC voltages from the supply voltage and the relatively temperature immune bandgap reference as discussed previously.

The resolution or number of bits a DAC can achieve is primarily determined by the architecture chosen. Some architectures can only achieve an effective number of 10 bits due to variations in PVT. Others are intractably large, especially in the fairly mature 0.35 μm technology used for this design. So, several different architectures were explored to determine which fit the specific application.

The DAC must also be monotonic. This means that a positive change in code value always results in a positive change in output voltage. This is related to the value of adjacent codes. If each step in output voltage is not the same, this is characterized as nonlinearity. Specifically, the change in step between codes is the differential nonlinearity (DNL). The DAC must have low maximum DNL and be monotonic so that the MCA may calibrate a peak location to any desired bin.

Additionally, the DAC must have some interface to the host processor for control. Since the DAC voltage range is fixed, the only control needed by the application processor is over the output voltage. So, a simple Serial Peripheral Interface (SPI) bus compliant shift register was designed for control of the DAC output.

2.3.2 Evaluating DAC Architectures

Numerous architectures exist for implementing a DAC. Due to the above mentioned constraints, these architectures were narrowed down to a few for evaluation. Each considered architecture was evaluated to see if it met the above requirements.

The first architecture examined is the common resistor string DAC (also known as a Kelvin divider). This architecture is shown in Figure 2.12. It consists of a string of 2^N equal size resistors connected from the desired maximum voltage and ground. One of an equal number of switches connects each node of the string to the output depending on the decoded input digital code. A similar architecture creates an output current using 2^N current sources connected in parallel with switches to an operational amplifier connected as a current to voltage controller. These topologies are inherently monotonic and simple to implement. They also have very low glitch characteristics that cause distortion as each code change only changes the state of two switches.

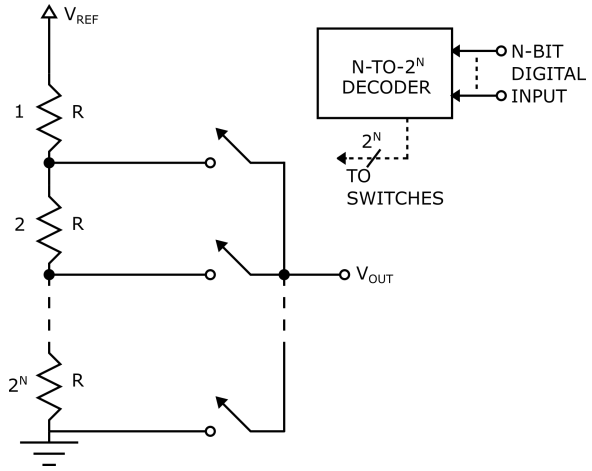
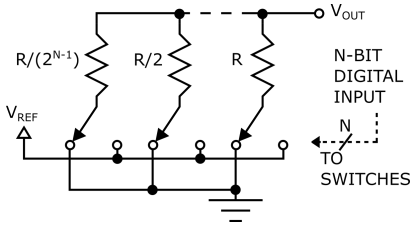


Figure 2.12: Resistor String DAC

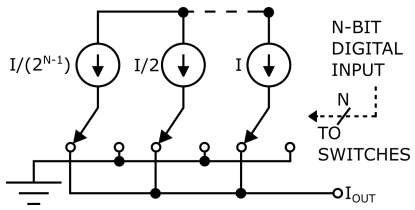
However, at our required resolution, a large number of resistors and switches would be needed. Each of these resistors would need to be matched to one another very well in order to mitigate the effects of PVT variation. This is impractical at this

resolution and the nonlinearity would be severe without trimming that is too costly for this application.

Another architecture to consider is the binary weighted DAC. Similar to the string DAC, this topology consists of an array of resistors or current sources. A voltage output version of this is shown in Figure 2.13a while the corresponding current output version is shown in Figure 2.13b. Each array has a binary weighting. The advantage of this architecture is that the interface requires almost no decoding. It is not inherently monotonic and can be quite nonlinear as it is hard to match each resistor or current source due to the large size of the most significant bit element. The output impedance also varies depending on the input code.



(a) Voltage Output Binary DAC



(b) Current Output Binary DAC

Figure 2.13: Binary DAC topologies

The next topology we will consider is the R-2R DAC [4]. This is a very common topology that uses resistors of only two values in a network shown in Figure 2.14.

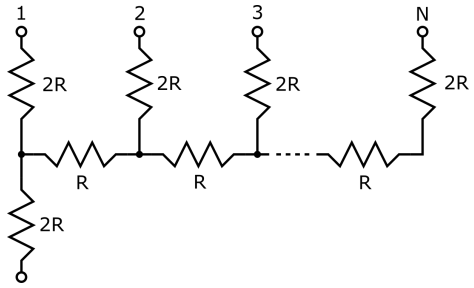


Figure 2.14: R-2R Ladder Network

The voltage mode version of the DAC is shown in Figure 2.15. An N-bit DAC

requires only 2N resistors that can be trimmed or easily matched. In this way, very high resolution DACs can be designed in a relatively small area [5]. Since each resistor is some combination of the unit resistance R, this resistor can be distributed in the layout to more closely match the other resistances. In the voltage mode, due to the properties of the R-2R ladder network, the output impedance is equal to R and independent of the code. Switches must operate over a wide range and the reference voltage must have a low impedance to source the wide range of current that varies with code.

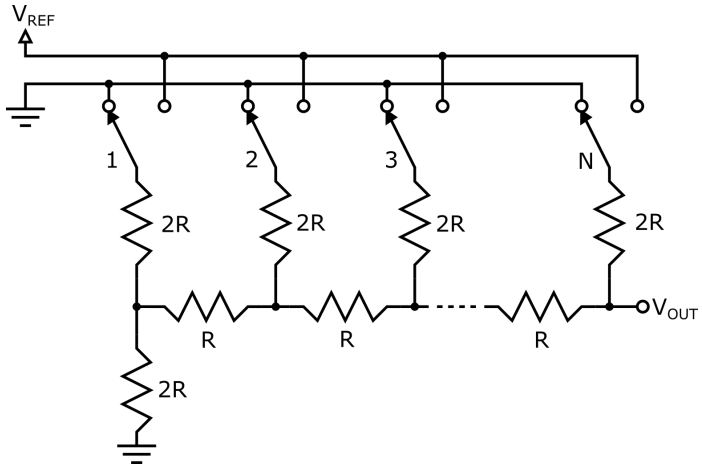


Figure 2.15: R-2R Voltage DAC

Finally, the W-2W current steering DAC was considered [6]. This design is shown in Figure 2.16. A reference current generates a gate voltage that is distributed to N equal sized transistors accompanied by N transistors with twice the width. The transistors are biased in the linear region and so they behave as resistors. Depending on the code, each leg is switched via digital switches to either the reference voltage or the output which is maintained at the reference voltage by the error amplifier. A benefit of this configuration is that it has a high output impedance so long as the error amplifier and reference voltage source can source the current required. It also has a simple interface like the R-2R DAC. Each transistor can be made from a

unit transistor or parallel combination. However, it is very sensitive to variations in threshold voltage. It is also difficult to generate the smallest current of 500 pA.

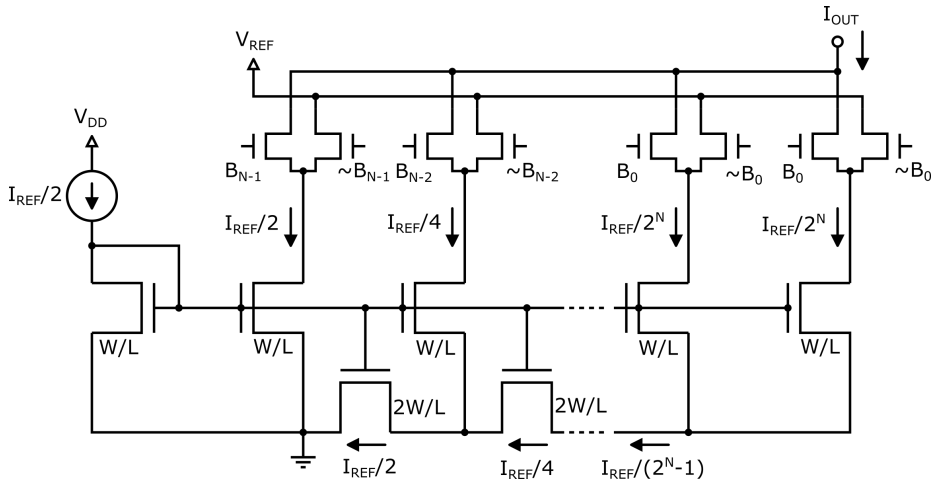


Figure 2.16: W-2W Current Steering DAC

Evaluating the properties of each architecture and the specifics of our application, some conclusions were made. The string DAC, though simple, would be difficult to implement while ensuring good matching of components. For similar reasons the binary DAC topologies were eliminated from consideration. The W-2W DAC seemed promising but, as described, the vulnerability to changes in threshold voltage were too great a risk. So, the R-2R voltage DAC was chosen for its relative simplicity (to interface with and implement), ease of matching components which helps to ensure monotonicity, and code-independent output impedance.

2.3.3 DAC Implementation and Simulation

With an architecture chosen, the components were designed to fit our application. With a desired minimum voltage step of about 500 μV, the number of bits required

over the 1.2 V reference range is

$$N = ceiling(log_2(1.2V/500\mu V)) = 12 \tag{2.1}$$

With this in mind, a 12-bit DAC was designed. To add flexibility and leverage external component tolerances, the DAC was split into two identical 6-bit R-2R voltage DACs. One handles the the most significant 6 bits (the MSBDAC) and the other the 6 least significant bits (the LSBDAC). Each has its own external resistor to determine the range of reference currents it can produce. These currents are then summed at the inverting terminal of the error amplifier to create the reference current. In this way, the ranges can overlap in order to allow a greater number of distinct reference currents. They can also function like a normal 12-bit DAC by selecting a 64-to-1 resistor ratio. This segmentation is shown in Figure 2.17.

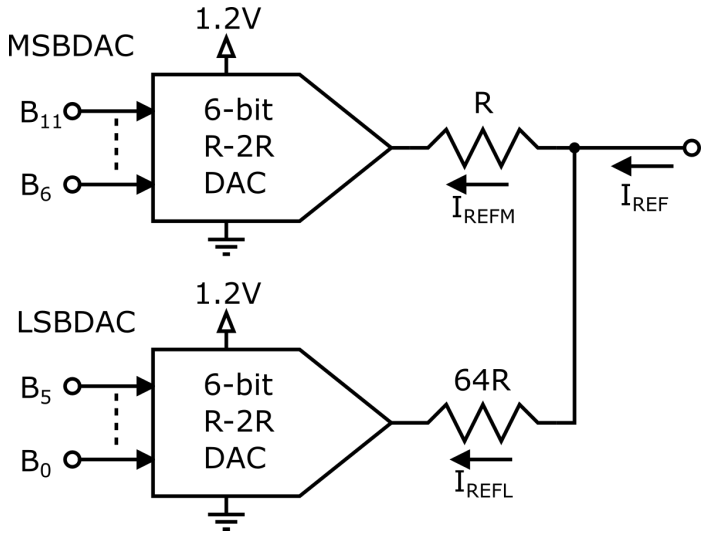


Figure 2.17: 12-bit Segmented R-2R DACs

Next, the unit resistance R of the DAC was chosen. This resistance is also the output impedance of the DAC. It determines the power consumption and, thus, the current drawn from the voltage reference. The output resistance must be much smaller

than the smallest external reference resistor. To achieve a maximum supply voltage of 1.2 kV, the smallest resistor connected to he MSBDAC corresponding to the largest reference current was determined to be

$$R_{EXT} = (R_{FB}/1.2kV) * 1.2V = 1M\Omega \tag{2.2}$$

48 kΩ was chosen for R in the initial version of the ASIC. This results in minimal gain and offset error in the DAC voltage due to its small magnitude relative to the smallest R_{EXT}. The DAC also presents a reasonable load to the reference voltage at the nominal supply voltage of 3 V with the worst-case code. An operational amplifier was configured as a unity gain buffer for the reference voltage to increase its current sourcing capability. The first version was fabricated and tested. The DAC performed well at the nominal supply voltage but the reference voltage buffer was unable to supply the required current at lower supply voltages when the system's battery voltage decreased as it discharged. With these tests in mind a more thorough simulation of the DAC design at lower supply voltages was done. Both DACs were connected to the reference voltage buffer and set to the code that generated the largest load to the buffer. The supply voltage was then swept from the nominal battery voltage ˜3V down to 2V. R was then increased until the buffer could supply the worst-case load at a discharged battery voltage. Some results for R values of 48kΩ, 96kΩ, 192kΩ, and 288kΩ are shown in Figure 2.18. Simulation (following the work in [7]) of the current drawn from the reference supply at each code is shown in Figure 2.19 for the different R values.

Based on this data, 288kΩ was chosen for R. The buffer can support worst-case load from the DACs down to ˜2.1V giving some head room beyond the expected minimum battery voltage of 2.5V. This is due to only drawing 7.5 μA from the

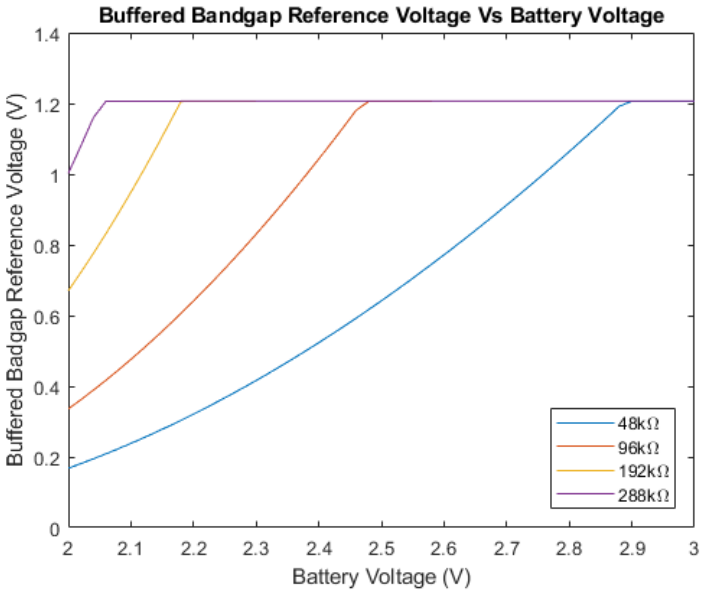


Figure 2.18: Buffered Bandgap Reference Voltage Vs Battery Voltage for R = 48kΩ, 96kΩ, 192kΩ, and 288kΩ.

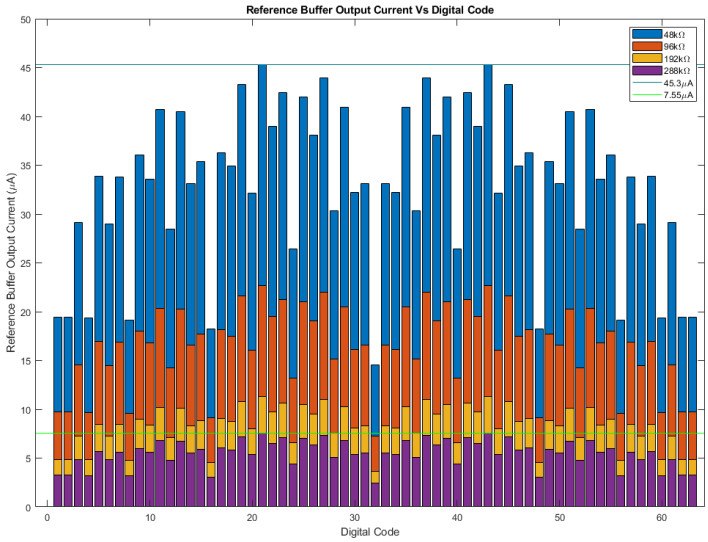


Figure 2.19: Reference Buffer Output Current Vs Digital Code for R = 48kΩ, 96kΩ, 192kΩ, and 288kΩ.

reference buffer worse case versus 45 μA in the first version. This R value dramatically increases the output resistance of the DACs which causes significant gain and offset

error in the DAC with the smaller external resistor. This enhances the effect of noise as each minimum voltage step is compressed. The range of bias current remains the same as it is dependent on an external resistor value and the voltage swing. An output buffer was considered but it would have led to a significant increase in power dissipation.

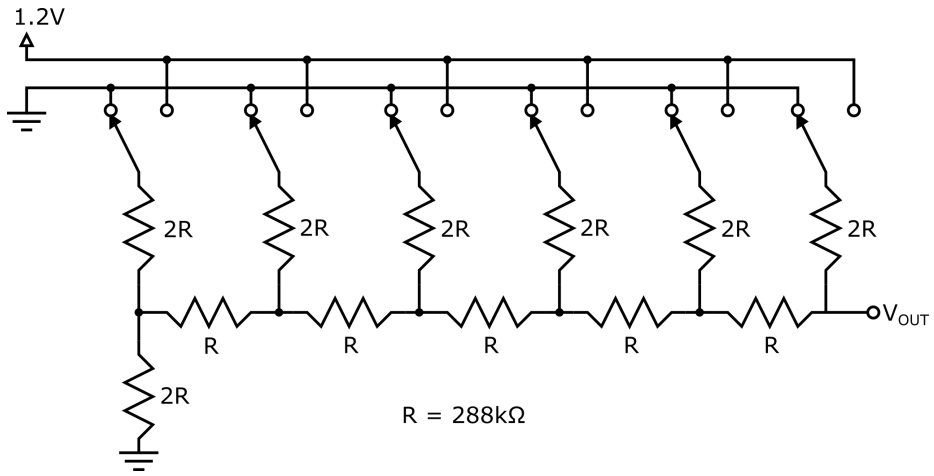


Figure 2.20: 6-bit R-2R Voltage DAC

The schematic of one of the 6-bit DACs is shown in Figure 2.20. Each of the switches shown is implemented via a single-stage inverter sized to handle the current of each path of the resistor ladder. This gives a simple way to switch each path from ground to the buffered bandgap reference. The inverters do not present a large enough capacitive load to affect the stability of the buffer. Since this is a reference DAC, each is not expected to switch quickly or often which relaxes the sizing requirements. By driving the switches with a binary counter, a simulation of the ideal DAC voltage range is shown in Figure 2.21.

Figure 2.22 shows the offset and gain error caused by the ratio of the output impedance and the external bias resistor compared to the ideal shown in Figure 2.21. The smallest voltage step is reduced to ˜18 mV for the first version where R was 48kΩ from the ideal ˜18.8 mV. With R set to 288kΩ in the second version, the voltage step

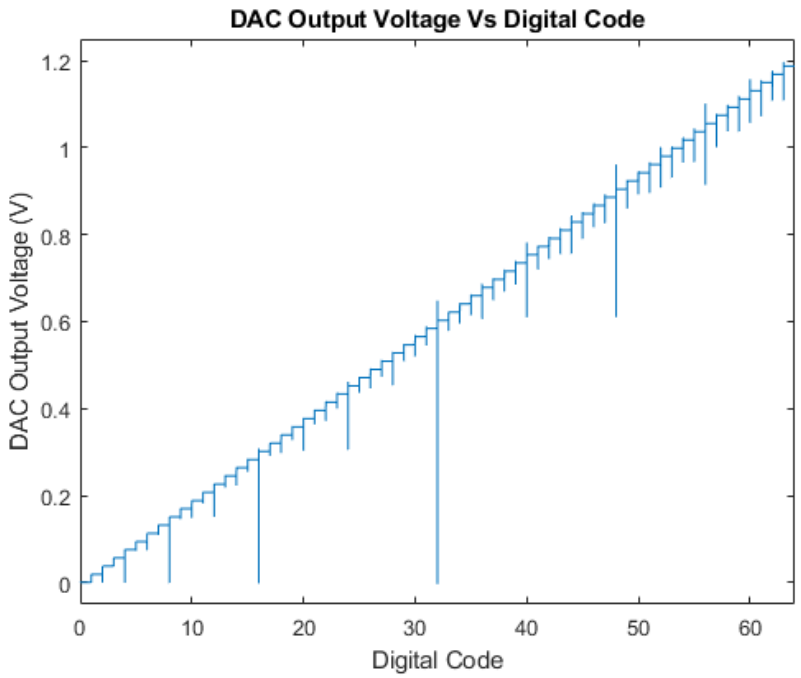
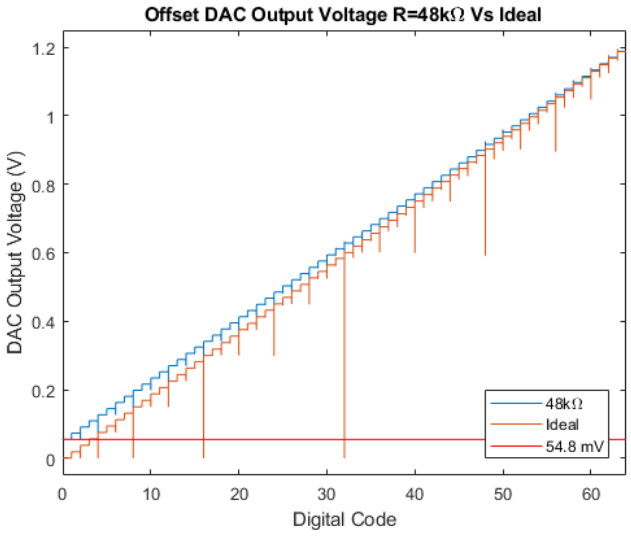


Figure 2.21: Simulation of 64 DAC Value Range.

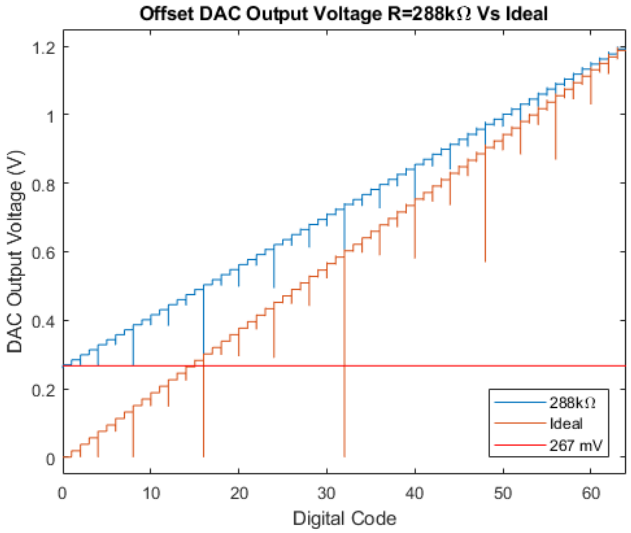
is reduced to ˜14.5 mV. As shown in Figure 2.22a, the first version had a ˜54.8 mV offset while Figure 2.22b shows the second version has an offset of ˜267 mV. This offset reduces the swing range of the DAC and thus makes the design less immune to noise. However, each voltage step still produces a significant change in DC voltage bias (˜14.5 mV) especially when compared to a non-segmented architecture with the same number of bits(11-bit ->1.2 V / 2048 = ˜586 μV).

To interface with a microcontroller a simple Serial Peripheral Interface (SPI) compliant shift register was designed. A chip select signal is brought low and a common clock shifts 12 bits into D flip-flops. The flip-flops feed latches whose inverted outputs are connected to the R-2R DAC inverter switches. After the data is clocked in, the chip select signal is brought high to latch the data out to the DACs.

With operation verified via simulation, the layout of the design was performed using a 0.35 μm CMOS technology. The error amplifier and triangle wave generator



(a) R = 48kΩ



(b) R = 288kΩ

Figure 2.22: Offset and gain error due to output impedance compared to ideal.

are mostly composed of silicon verified components (the op amps, bandgap reference, etc). Each of these is placed on one side of the chip designated for analog components. The FSM was routed and placed on the digital side. Each domain was given its own ground and supply voltage domain to isolate the digital switching noise from the analog circuitry.

The DAC required special care in layout to ensure immunity to PVT. Several considerations must be made in order for each resistor in the R-2R ladders to match each other. Variations in temperature and doping profiles can be modeled locally as an approximately linear gradient. For this reason, components that need to be matched should be placed closely to one another and as far away from components that dissipate significant power as possible. The close placing of components is known a common-centroid layout. By placing the centers of matched components as close together as possible, effects of linear gradients can be canceled out. Additionally, each component can be broken into equal size parts and laid out in a symmetrical fashion. In this way, with thoughtful placement, every component can be matched to another by sharing a common centroid.

This idea was applied to the layout of each identical DAC. In the CMOS technology used, resistors are fabricated by specially doping polysilicon to have a high resistivity. Each resistor consists of a strip of this polysilicon with metal contacts at each end. The sheet resistance of the polysilicon is consistent over fabrication runs and so each resistor has a resistance determined by its length divided by its width multiplied by this sheet resistance. For example, a 1 μm wide resistor that is 5 μm long with a sheet resistance of 200 Ω/sq will have a resistance of 1 kΩ. A sample resistor is shown in Figure 2.23.

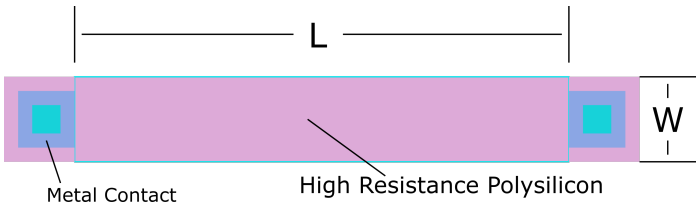


Figure 2.23: Sample layout of high resistance polysilicon resistor.

In the first version, each R was split into four separate resistors. The second version extended this to eight resistors per R due to the significant increase in resistance.

To achieve a common centroid layout each piece is placed in a symmetric layout about both a horizontal and vertical axes [8]. Figure 2.24 shows an example layout where one resistor is split into four and laid out in this symmetric pattern around a center point. A linear gradient from any angle of temperature or doping profile will cancel out due to the symmetry.

This same concept was applied to the entire resistor ladder in each DAC. Every resistor shares the same center point and is symmetric across both axes. The most significant bit resistors are at the center to ensure they have the closest matching as any error due to mismatch will lead to the largest nonlinearity in the DAC output voltage. From the center, each resistor is split into parts. The first piece is placed in the top left, the second piece in the bottom right, the third piece in the bottom left, the fourth piece in the top right, the fifth piece in the top left, and so on similar to Figure 2.24. This results in an array of closely spaced, symmetrically distributed resistors as shown in Figure 2.25.

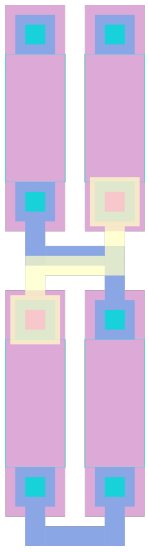


Figure 2.24: 2D common-centroid layout of single resistor.

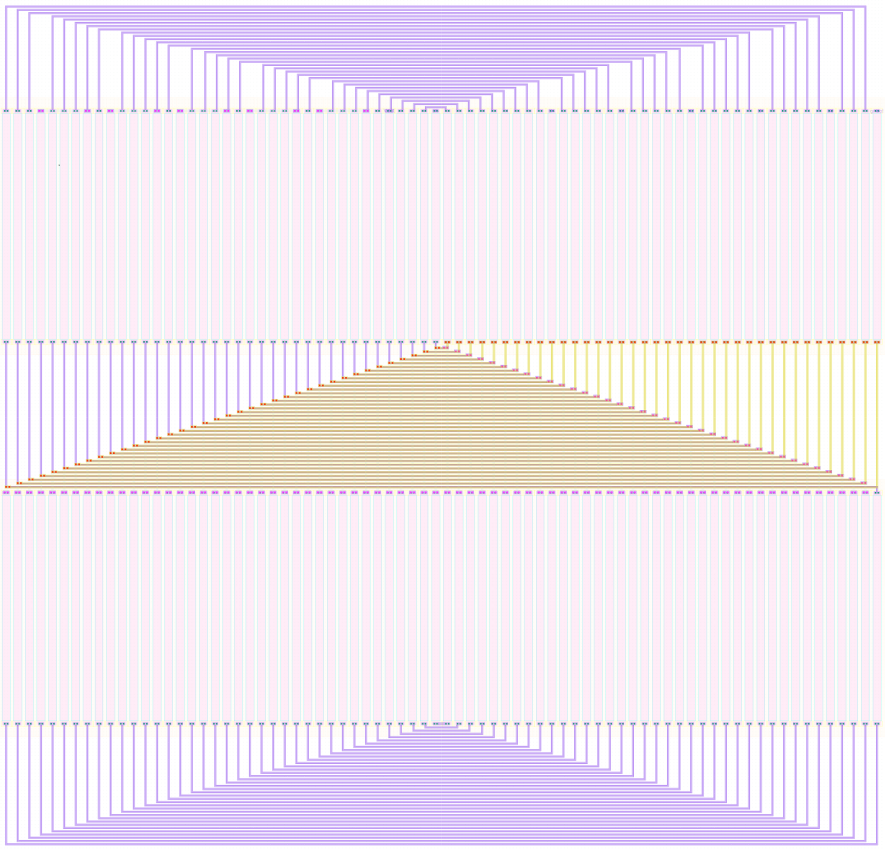
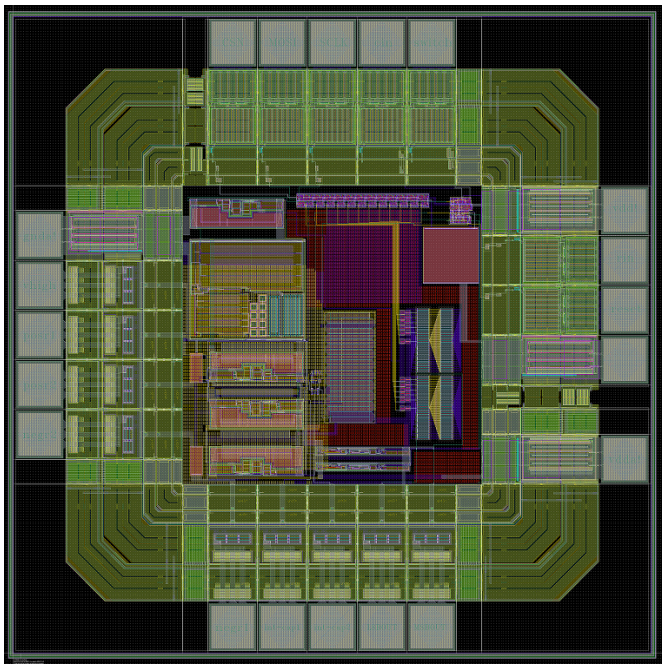
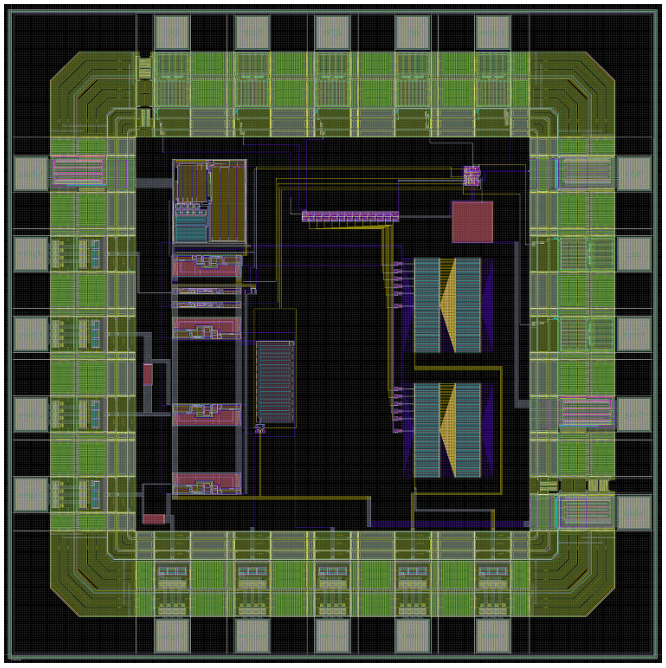


Figure 2.25: Common-centroid layout of one 6-bit R-2R ladder.

Two of these arrays were placed between the analog and digital sections of the chip along with the inverter switches. The layout of the first and second versions of the controller chip are shown in Figure 2.26. The first version occupied an area of 1300.8μm x 1300.8μm or 1.69 mm^2. The second version occupied a slightly larger area due to the increased DAC area at 1780.8μm x 1780.8μm or 3.17 mm^2.



(a) Layout of the first version of the switching controller ASIC.



(b) Layout of the second version of switching controller ASIC.

Figure 2.26: First and second versions of the ASIC layout.

2.4 Circuit Board Design

Throughout the project, several printed circuit board (PCB) assemblies were designed to evaluate the performance of the power supply design and the overall radiation monitoring system. Figure 2.27 shows a selection of PCB assemblies developed over the course of the project.

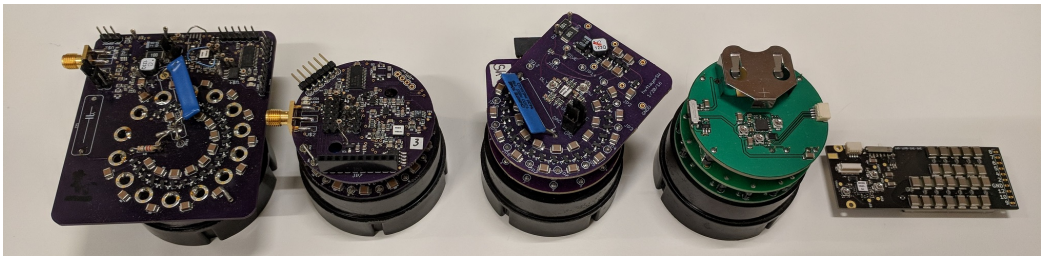
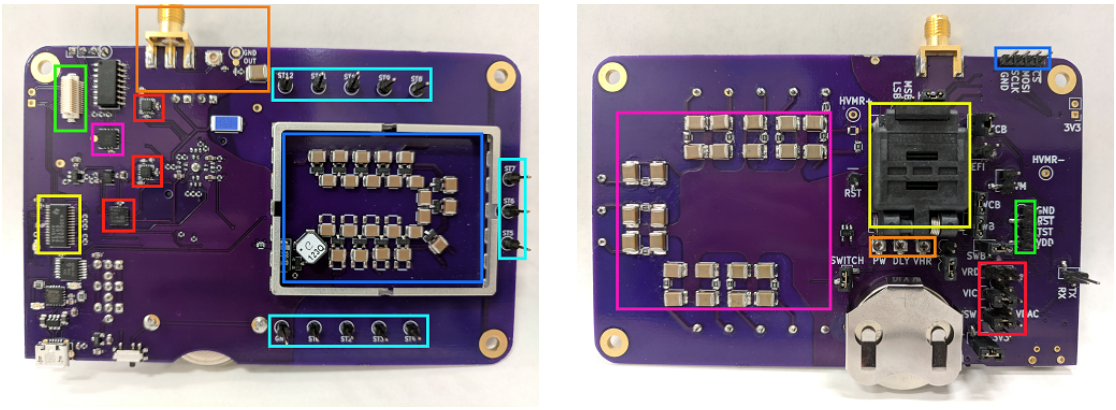


Figure 2.27: Evolution of power supply PCB assembly.

Apart from these boards intended for the actual application, a test PCB was designed specifically to evaluate the performance of the switching controller chip and power supply configurations. This PCB is shown in Figure 2.28. A zero insertion force socket (back,yellow) is included so multiple controller chips can be tested with the same board. A USB interface as well as a microcontroller (front,yellow), programmed using a simple header (back,green), are included in order to monitor and modify the operation and performance. Switches and digital controlled resistors (front,red) are provided to test the effects of different external component values on switching frequency range and pulse width. The external pulse width resistor and the comparator high threshold voltage as well as the resistance connected to the gate of the MOSFET can be adjusted via potentiometers (back,orange). A reference DAC (front,pink) can be controlled by either the on-board microcontroller, the application MCA board via a board-to-board connector (front,green), or a using an SPI header (back,blue). These same SPI lines are isolated from the supply used for the controller and connected to

the SPI register of the on-chip DACs. A jumper selects whether the reference DAC or internal DACs are connected to the error amplifier inverting terminal.



(a) Front (b) Back

Figure 2.28: Test PCB for testing switching controller operation and power supply performance.

The MOSFET, transformer, and Cockroft-Walton chain (front,blue) are contained within a metal shield (removed for photo) to limit EMI. Each stage is bypassed via large high voltage rated capacitors (back,pink) to limit voltage ripple. The supply voltages for the reference DAC, controller chip, and switching converter section can each be independently selected via jumpers (back,red) to be sourced from the battery, a 3.3 V regulator generated from the USB interface, or from a on-board 12-bit DAC. In addition to this functionality, the stages of the Cockroft-Walton chain can be connected using common 0.1" jumper wires (front,teal) in any order or taper a particular PMT may require. This enables one board to interface with many types of PMTs and explore gain and linearity resulting from different tapers. The signal from the anode is coupled to the output with a large high voltage capacitor and can be extracted via a SMA or U.FL connector (front,orange).

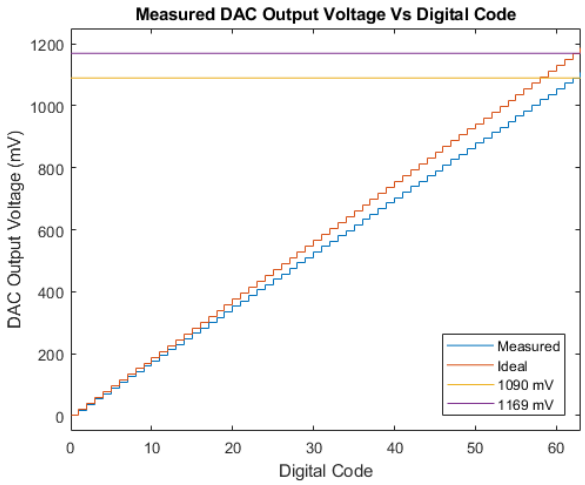
Chapter 3

Simulation and Testing

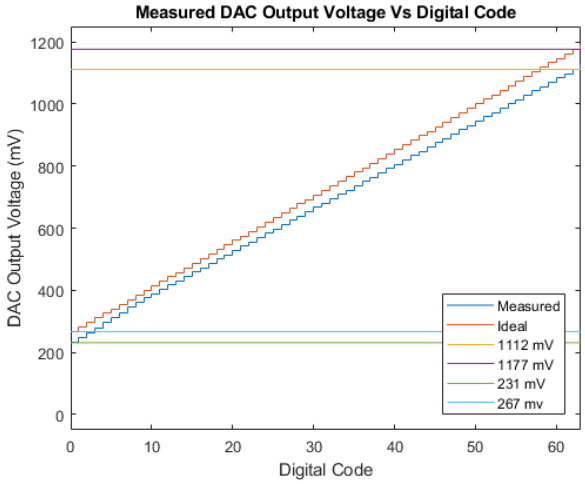
3.1 DAC Testing and Performance

To measure DAC performance, a microcontroller and ADC were used to interface with the SPI register for the DAC and measure the output voltage for each code. This was done both with the output disconnected from and with the output connected (via a 1 MΩ resistor) to the error amplifier. The average results of testing the batch of chips is shown in Figure 3.1. Figure 3.1a shows the case with the output disconnected from the error amplifier and compared to the ideal operation. The output is linear with some variance in full scale range or gain error of ˜79 mV.

Figure 3.1b shows the measured output when the DAC is connected to the error amplifier. This results in an offset as expected that varies from simulation by ˜36 mV. There is also a gain error that is ˜29 mV after subtracting offset. A summary of the measurements of the DAC are included in Table 3.1. Differential nonlinearity (DNL) is a measurement the difference between one DAC code and the next. To ensure monotonicity, this must be limited to less than 1 LSB. We see that in each configuration, even the maximum deviation from an ideal voltage step is much less



(a) Measured DAC output compared to ideal operation.



(b) Measured DAC output compared to expected when connected to error amplifier.

Figure 3.1: Average measured DAC output when open circuit and when connected to error amplifier.

than one LSB. Integral nonlinearity (INL) is a measurement of the deviation of the DAC output from a straight line. For a code, it is equal to the sum of all DNL of the previous codes. The maximum INL of 1.12 LSB when connected to the error amplifier indicates linear performance.

By setting the DAC output to 0, the output resistance could be measured to be ˜275.7 kΩ. This gives an average measurement of the resistance of each R in

Table 3.1: DAC Measurement Summary

	Open Circuit	Connected to Error Amp
Resolution(mV)	17.5	14.2
DNL_{max}(LSB)	0.13	0.16
INL_{max}(LSB)	0.13	1.12
Offset(mV)	0	36
Gain Error(mV)	79	29
R(kΩ)	275.7	275.7

the ladder as they all contribute to this resistance when switched to ground at this code. This value is less than the design and explains why the offset is lower than the expected value. Across the sample of measured DACs, this value only varied by ˜2 kΩ or 0.7%. Considering this and given that the sheet resistance used to fabricate the resistors was ˜1.33 kΩ/sq, the resistors in each ladder appear to be well matched.

3.2 ASIC Measurements and Testing

Table 3.2 gives a summary of the ASIC operating range and power consumption. V_I(V) is the supply voltage, $I_Q(\mu A)$ is the current consumption of the ASIC itself, $P_Q(\mu W)$ is the power consumption of the ASIC, and f_{SW}(Hz) is the switching frequency range. Operation has been verified down to a supply voltage of 2.5 V. At this voltage, the ASIC consumes only 317 μW. The switching frequency range will vary depending on how the external components are configured. The given range is what was found to give the lowest power operation when used in the desired application.

3.3 Supply Testing and Performance

After initial testing to verify DAC operation, the controllers were integrated with the test boards. Coupled with a PMT and the application MCA board, Figure 3.2 shows

Table 3.2: Switching Controller ASIC Specifications

	Min	Max
V_I(V)	2.5	3.2
$I_Q(\mu A)$	126.9	327.5
$P_Q(\mu W)$	317	1048
f_{SW}(Hz)	100	20k

the testing setup.

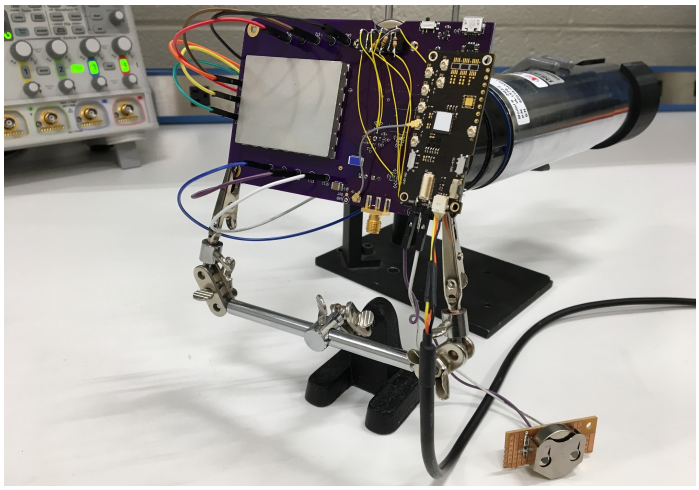


Figure 3.2: Test setup used to verify supply operation [1].

Table 3.3 gives a summary of the supply operating range at a typical battery voltage of 2.8 V. Using the test board configuration, an output voltage range from 0 V to 983 V was achieved. This allows a large range for tuning the application PMT gain.

Table 3.3: HV Supply Operating Range and Characteristics

	Min	Max
V_O(V)	0	983
I(mA)	0.2	1.293
P(mW)	0.56	3.07
η(%)	0	31.5

The feedback resistor from the output voltage to the error amplifier is the dominant load on the output. Figure 3.3 shows a graph of the efficiency with respect to this load of the supply over a range of output voltages. Clearly the lower battery voltages achieve higher efficiency. This is also dependent on the tuning of the external components. The highest efficiency is achieved across the desired output voltage range.

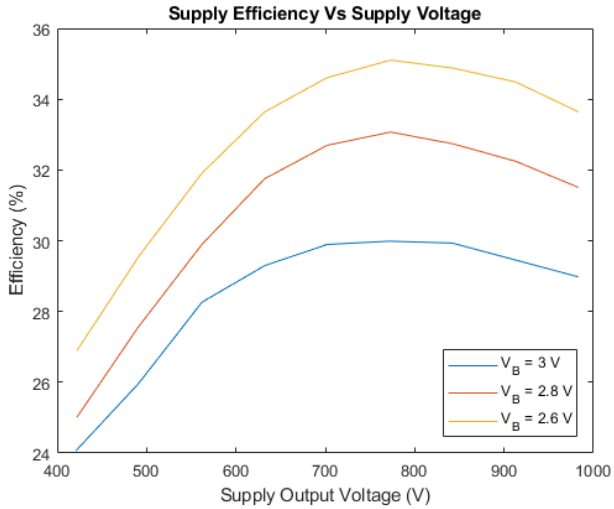


Figure 3.3: Supply efficiency over a range of output values and battery voltages.

To verify that the DAC resolution was sufficient to finely adjust the PMT gain, a sweep of the DAC voltages was performed. The results are shown in Figure 3.4. The MCA is able to adjust the PMT gain to shift the MCA ADC bin of a peak by ˜1 bin/LSB.

Using the test board, a long duration battery test was performed. The supply was connected to a battery and set to ˜700 V. A standard tapering configuration was used to connect it to a PMT. The battery voltage and current were periodically measured and logged. The output of the PMT was also monitored to ensure that the peak location did not drift significantly over time. A graph of the battery voltage and current over the test is shown in Figure 3.5. The test ran for close to 1100 hours

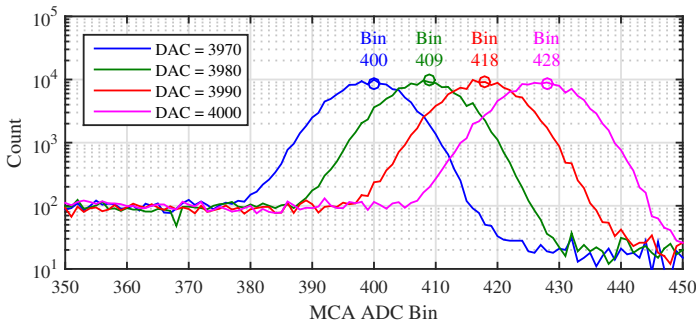


Figure 3.4: PMT gain control using the MCA [1].

or 45 days before the supply could no longer maintain the output voltage.

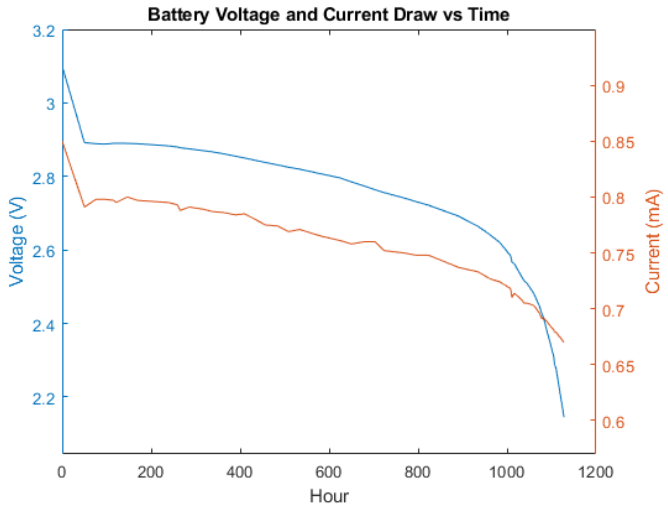


Figure 3.5: Battery voltage and current over a long duration battery powered test.

Chapter 4

Conclusion and Future Work

A low power high voltage supply has been designed to operate in a long term radiation monitoring application. A novel flyback transformer driven Cockroft-Walton voltage multiplier converter topology is designed to provide bias voltages for a PMT. Using a 0.35 μm CMOS process, a pulse frequency modulation switching controller is designed to regulate the supply. Within the controller, a 12-bit segmented R-2R reference DAC has been designed to set the desired output voltage and can be controlled via an external microcontroller. Test circuit boards were designed and extensive testing performed to verify supply operation. Tests also included verifying battery powered operation. Long duration testing ensured supply stability with constant 1k count per second PMT loading.

Where this work was designed for an application with relatively light loading, future work might explore supply operation under heavy loading and the design and configuration challenges this may present. This supply design might also be suited to power multiple detectors simultaneously. The flexibility of the design could allow it to be modified for use in other applications where low power high voltage biasing is needed.

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