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Forecasting Reject Rate of Tested LSI Chips

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Abstract—The reject rate of LSI chips due to incomplete fault coverage of the tests is the fraction of faulty chips among the chips that pass the tests. This reject rate, which is a measure of the tested chip quality, contributes to the field returns. It is, however, difficult to determine the tested chip quality from the field return data which may also include rejects due to handling damages, infant mortality, etc. Also, a large number of chips must be in use in the field before an adequate amount of field return data can be obtained. This paper gives a method of forecasting the reject rate from the test data alone before any field trials are made.

BACKGROUND

In a recent paper [1], the reject rate of the tested chips was obtained as

$$r(f) = \frac{(1-f)(1-y)e^{-(n_0-1)f}}{y+(1-f)(1-y)e^{-(n_0-1)f}} \quad (1)$$

where f = fault coverage of tests

n_0 = average number of faults on a defective chip (as explained in [1], n_0 is different from the defect density that is normally used in yield analysis)

and y = true yield of good chips.

For computing $r(f)$, the yield was assumed to be known and the parameter n_0 was evaluated from test data. In today's rapidly changing technology, however, the yield is not always known. In fact, true yield can be estimated only after the chip has been in production for some time. This paper presents an application of a forecasting technique for evaluation of yield and reject rate from the test data.

BASIC IDEA

A complete fault coverage is usually not possible for LSI tests. Typical experimental data are shown in Fig. 1 (see Table 1 of [1]). This graph shows the fraction of the manufactured chips that are rejected as the fault coverage is increased. In this case the testing stops at 65% fault coverage. The basic idea behind the present work is to predict or forecast how the fraction of rejected chips will continue to grow if testing was extended to 100% fault coverage. Using the parameters y and n_0 , as defined above, the theoretical probability of rejecting a chip with tests having a fault coverage f was obtained in [1] as

$$P(f) = (1-y) [1 - (1-f)e^{-(n_0-1)f}]. \quad (2)$$

We will now estimate y and n_0 such that the forecast error in $P(1)$ is minimized.

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WEIGHTED LEAST MEAN SQUARED ESTIMATION

The mean squared error for fitting $P(f)$ to the experimental data is defined as [2]

$$\text{MSE} = \sum_{i=1}^k [P(f_i) - P_i]^2 \cdot a^{100(f_{\max} - f_i)}, \quad (3)$$

where (f_i, P_i) , $i = 1, \dots, k$, are the experimental data as shown in Fig. 1 and f_{\max} is the maximum fault coverage up to which experimental data are available (0.65 in Fig. 1). The last factor is known as the weighting factor. Notice that $a = 1$ corresponds to the unweighted mean squared error while $0 < a < 1$ weights the error nearer to f_{\max} , heavier. From (2), since $P(1) = 1-y$, we should select the value of the weighting parameter, a , such that the variance of y is minimized. There are several procedures which minimize (3) and then find the variance of estimated parameters [3]. In practice, many nonlinear search computer routines are available. We will illustrate the procedure by using the nonlinear estimation program known as NLIN (Non-LINear regression) [4]. The program first performs a coarse search of the parameter space to determine starting values, and then uses an iterative method to minimize the weighted mean square error. For the data of Fig. 1, this program gave the values of y and n_0 , which minimize (3), as shown in Fig. 2. The program also provides the 95% confidence intervals for the parameters shown as the shaded region in the figure. As the value of the weighting parameter a was reduced, the 95% intervals continue to become narrower until at $a = 0.55$, the parameter values and their ranges are

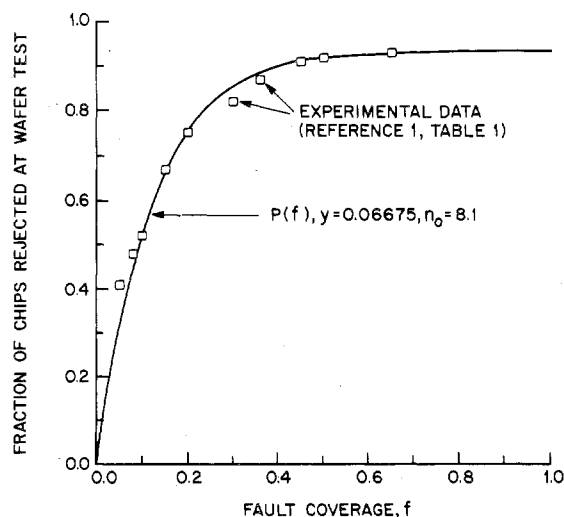


Fig. 1. Wafer test data: fraction of chips rejected as a function of fault coverage of tests. The continuous curve corresponds to the probability of rejecting the chip computed from the estimated parameters $y = 0.06675$ and $n_0 = 8.1$.

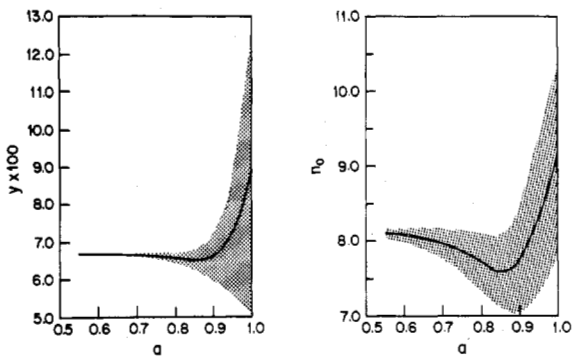


Fig. 2. Estimated parameters y and n_0 (solid curves) and their 95% confidence intervals (shaded regions) as functions of the weighting parameter a .

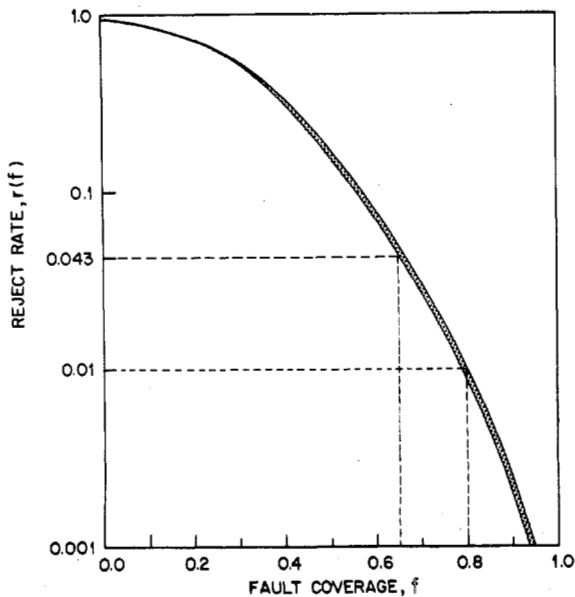


Fig. 3. Reject rate as computed from the estimated parameters. For 95% confidence interval of parameters, $y = 0.06675 \pm 0.00015$ and $n_0 = 8.10 \pm 0.09$, the reject rate lies in the shaded region.

stabilized and no further change in a was considered necessary. The best fit values of the parameters are $y = 0.06675$ and $n_0 = 8.1$ with the 95% confidence ranges being ± 0.00015 and ± 0.09 , respectively. The best fit $P(f)$, as computed from (2), is shown in Fig. 1 as the continuous curve.

Figure 3 shows the reject rate as computed from (1). For the 95% range of y and n_0 , the reject rate would be in the shaded region in the figure. This gives a 4.3% reject rate for the 65% fault coverage. The fault coverage should be increased to 80% for a 1%, and to 95% for a 0.1% reject rate. These results are substantially in agreement with those obtained in [1]. We have, however, removed the need for the prior knowledge of the yield. In fact the estimated yield of 6.6% is fairly close to the yield of 7% used in [1].

CONCLUSION

A nonlinear parameter estimation is used to forecast the reject rate of the tested LSI chips from the functional test data. In this procedure the chip yield is also estimated. This method can be used to study the LSI test quality even before the product is sent into the field. The result also helps in deciding whether the fault coverage of tests is adequate or needs to be improved.

ACKNOWLEDGMENT

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