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Analog Sensing Front-End System for Harmonic Signal Classification

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***Abstract*— This paper presents the design of an Analog-to-Information spectral decomposition scheme suitable for parallel low-power analog and mixed-signal VLSI implementation. The novel scheme extracts sufficient information to achieve good back-end signal detection and classification performance while using less power than purely digital spectral techniques such as FFT. Simulations of a prototype system in a mixed-signal $130\,\mathrm{nm}$ CMOS process show a feasible solution space given an on-line self-calibrating system.**

I. Introduction

Wireless sensor systems rely on very low power operation to extend service lifetimes. Transmission of sensor node data is the largest portion of a node's active-energy budget. Systems reduce the required transmission bandwidth by performing a portion of the processing on each node, only transmitting the results instead of raw sampled sensor data.

On-node computation in the digital domain requires a relatively high-rate ADC to first sample the sensed waveforms for subsequent processing. If, however, the initial signal processing is performed in the analog domain, the system ADC can be moved later in the signal chain and operated at a lower rate. Such processing operations serve to remove redundancy in the signal and extract relevant information for back-end use.

Sensor systems for detection and classification typically use spectral techniques to achieve good performance. Extraction of spectral information typically uses the Discrete Fouriér Transform (DFT) after sampling the sensed waveform. Calculating the transform, even with the efficient Fast Fouriér Transform (FFT) algorithm, uses the most system power next to data transmission. Reported power measurements using Crossbow's Mica2 sensor node module in an acoustic vehicle classification application show power usage of $23.9\,\mu\mathrm{W}$ for a 512-point FFT versus $0.28\,\mu\mathrm{W}$ for the feature selection and classification function using Support Vector Machines [1]. AdaBoost-based classification is adapted to an analog front-end in [2].

Classification systems involving rotating machinery such as moving vehicles or ball bearings use the periodic nature of the signal source to select only the harmonically-related spectral coefficients to build a harmonic model. Calculation of the model parameters (fundamental frequency, and magnitude/phase of each harmonic) for the Harmonic Line Association [3] technique requires narrow frequency spacing $\approx 1\,\mathrm{Hz}$ to reliably resolve harmonic and non-harmonic components. This requires both a long acquisition time and many-point FFT. It is noted here that only a small fraction of the coefficients are used in constructing the model parameters, the rest are discarded.

Analog computation of a signal transform has the potential to reduce overall power consumption by using less energy itself and also by moving the system's ADC to low-rate conversion of the extracted spectral coefficients. Sampled analog systems such as [4] implement the Cooley-Tukey "butterfly" structure with tunable transconductors in a continuous-valued calculation of the FFT. Another proposed approach generates the DFT coefficients by spatially distributing a sampled waveform over one boundary of a passive *L-C* lattice and using diffractive and refractive propagation effects to transform the signal [5]. Analog to Information conversion with random basis functions using *Compressive Sensing* (CS) theory has also been proposed for analog systems [6].

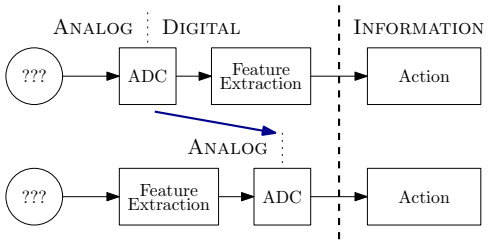

Fig. 1. Top: Mixed analog/digital computation of signal features. Bottom: Analog-to-Information's direct feature extraction.

An Analog to Information (AtoI) spectral feature extraction technique suited for extremely low-power parallel analog implementation is presented in this work. Unlike the FFT, this novel scheme calculates only the coefficients utilized in subsequent processing, with large potential power savings. This technique, like the analog schemes, also moves the system ADC later in the signal chain. Unlike CS schemes, the basis functions are not required to switch faster than the signal's Nyquist frequency and time- and/or frequency-domain reconstruction is simply calculated (if required at all). The top of Figure 1 shows a FFT-based system diagram while the

bottom illustrates the proposed concept of directly extracting spectral features ("information") from the analog domain.

The rest of this paper is organized as follows. Section II describes the AtoI scheme. Section III presents a hardware architecture and an example design. Section IV discusses simulated system performance in a military vehicle classification application including estimated fabrication errors. Finally Section V concludes the paper.

II. Analog to Information Scheme

Time-windowed and band-limited signals may be represented by their Fouriér Series (FS) coefficients given by

$$s(t) = \sum_{k=1}^{N} \left[a_k \cos(2\pi k f_0 t) + b_k \sin(2\pi k f_0 t)\right] \quad \text{with} \quad (1)$$

$$a_k = \int_0^{t_p} s(\tau) \cdot \cos(2\pi k \tau / t_p) d\tau, \quad (2)$$

$$b_k = \int_0^{t_p} s(\tau) \cdot \sin(2\pi k \tau / t_p) d\tau, \quad (3)$$

where t_p is the analysis period and $f_0 = 1/t_p$.

Calculation of the FS coefficients is a continuous-time, continuous-valued projection of the signal onto the orthogonal set of sinusoids. Direct analog implementation requires generation of a phase-coherent set of quadrature sinusoids, four-quadrant multiplication, and windowed integration. An analog computer implementation in [7] requires accurate coefficient tuning.

The AtoI scheme replaces the basis sinusoids with their sign functions only, e.g. $\cos(2\pi kt/t_p) \rightarrow \text{sgn}(\cos(2\pi kt/t_p))$, anti-podal waveforms of ± 1. Fouriér Series coefficients may be calculated from the modified projections through a simple back-substitution as the matrix connecting the two coefficient vectors is both sparse and unipotent [8]. However, [8] also reported minimal classification performance degradation when using the AtoI coefficients directly for vehicle and bearing fault applications.

Characteristics of the AtoI scheme include:

- Reduction of the 4-quadrant multiplier to a double-pole double-throw analog switch. The multiplier no longer sets the noise and linearity performance of the system. Low source and high load impedances reduce charge injection effects and switch driving power is proportional to basis frequency.
- Collapsing of the basis function waveform generation requirements to timing information only. Synchronous digital circuits are well-suited for this task.
- Moving most amplifiers except the input buffer to operate as integrators or baseband low-pass filters allowing power dissipation to be proportional to frequency resolution instead of signal bandwidth.
- Allowing calculation of only the coefficients used for back-end processing (possibly determined adaptively) instead of calculating all coefficients and discarding irrelevant outputs. Each projection section shares only the common input signal and timing information and may be implemented as a parallel bank of identical channels.
- Moving the system ADC later in the signal path to operate at reduced rate. Under the AtoI scheme, ADC sample rate is approximately N_{coef}/t_p where N_{coef} is the number of coefficients used in back-end processing and t_p is the analysis period. Conversion immediately after sensor conditioning, to use the FFT, requires a sample rate double the entire signal bandwidth.

Sample rate reductions can be dramatic for small frequency resolution and large signal bandwidths. For example, a system measuring a harmonic signal with fundamental frequency of 100 Hz to the 10^{th} harmonic at 1 Hz resolution would operate at a sample rate of at least 2 kHz and use a 2048-point FFT. An AtoI system would use 10, 1 Hz resolution (1 s integration time) quadrature projection channels and sample the outputs at an average rate of 20 Hz, yielding a two order-of-magnitude reduction in ADC rate.

III. System Design and Implementation

Figure 2 shows the projection system block diagram, illustrating the parallel nature of the L channels. An input buffer pre-conditions and distributes the sensor signal to L harmonic projection channels. The Main Control block supervises the system, sets input amplifier parameters, configures each projection channel for basis frequency and operation mode, controls integration timing, and performs channel calibration. Output of the system is L-pairs of projection voltages in rectangular form.

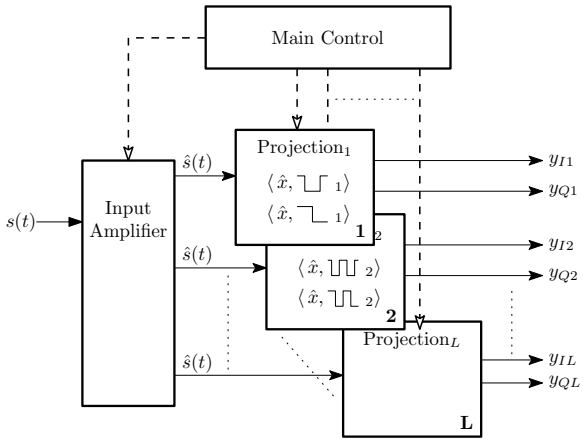

Fig. 2. System Block Diagram

Each quadrature channel structure is shown in Figure 3. Multipliers are transmission gates connected as a double-pole double-throw switch to either pass-through or invert the differential signal. Basis waveforms for multiplier switch timing are generated by a numerically-controlled oscillator (NCO). The most-significant bit of the NCO's 16-bit phase accumulator (PA) is used as one waveform. Quadrature output is obtained from adding a constant of 2^{14} to the PA output, representing a $\pi/2$ shift. Average frequency is controlled by setting the PA's 14-bit increment per clock cycle. Each channel's digital

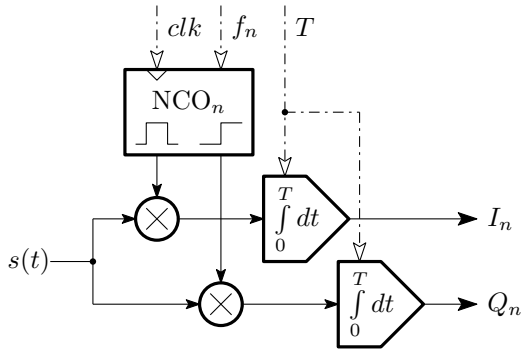

Fig. 3. Projection channel architecture.

block also includes a serial register interface used by the main control block to set mode, NCO, and OTA tuning values.

Integration is performed by an OTA-C amplifier. The example vehicle classification application described in Section IV uses integration times on the order of 500 ms, requiring extremely long on-chip C/g_m time constants. To allow practical on-chip integration capacitors on the order of tens of pF, corresponding OTA transconductances are extremely low, on the order of pS.

Deep sub-threshold transistor operation is then required for the OTAs. Figure 4 shows the implemented OTA. It utilizes a current divider approach to achieve low transconductance [9]. Transistors Ma and Mb linearize the transconductance for weak inversion operation of M1 and M2. Sub-threshold operation also makes OTA power dissipation inversely proportional to time constant and directly proportional to frequency resolution.

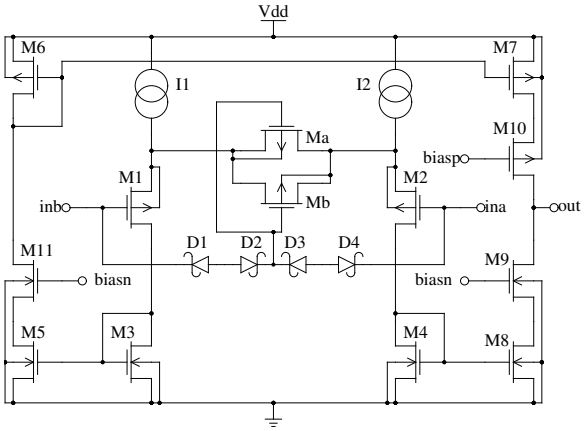

Fig. 4. Implemented current mirror OTA topology with linearization and gain/offset tuning.

Current sources I_1 and I_2 are independently variable and implemented as a current-steering DAC for post-fabrication calibration and offset cancellation by the main control block. The 12-bit DAC value is partitioned into a 4-bit bias level k_g and 8-bit signed bias skew k_o to fine-tune transconductance and offset, respectively. The two branch currents are then represented as

$$I_{1,2} = \left(1 + \frac{k_g}{16} \pm \frac{k_o}{128}\right) i_{\text{ref}}, \tag{4}$$

Figure 5 shows simulations of the integrator output for the first harmonic channel with an integration time of 2 fundamental periods. The top row is the projection with an input sinusoid at the harmonic frequency. Next rows are the projections with input sinusoids at $2\times$ and $3\times$ the fundamental frequency, respectively. The figure shows characteristic $1/n$ response to input frequencies at odd multiples of the basis frequency, matching the expected response.

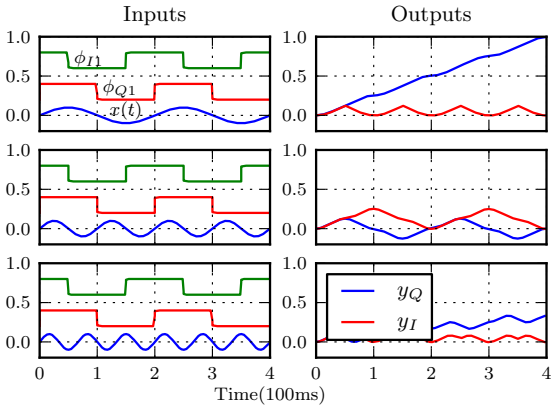

Fig. 5. Simulated channel outputs in response to input frequencies at multiples of the basis frequency.

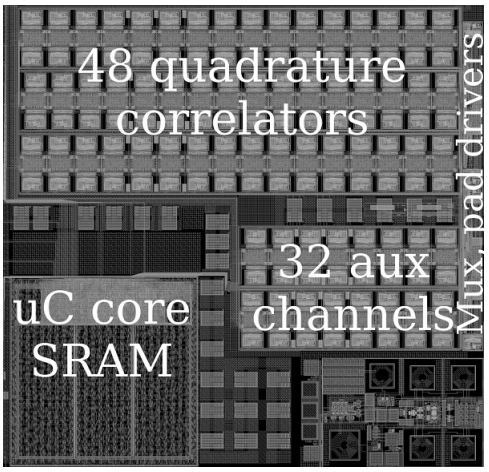

Fig. 6. Chip layout floorplan.

A prototype VLSI chip in a 130 nm mixed-signal CMOS technology was designed and includes 48 projection channels, shown in Figure 6. Main control functions are provided by an on-die custom microcontroller core, timers, and I/O hardware designed by the authors. Earlier projects have verified the processor macro in 0.35 μm and 0.18 μm technologies [10]. Sensor pre-conditioning and the ADC were not included on-chip. Table I gives some relevant specifications obtained from simulations of the chip.

TABLE I
CIRCUIT SPECIFICATIONS.

Process:	130 nm
Channel, μC core, Total Area:	0.087 mm^2, 1.77 mm^2, 16 mm^2
Supply Voltages:	2.5 V_{analog} / 1.2 V_{digital}
Analog Power Consumption:	200 nW/channel, 5 μW total

IV. Vehicle Classification Application

A. System classification performance

Acoustic recordings of 9 vehicles passing two fixed sensor stations were used to evaluate the feasibility of the AtoI approach for a peace-keeping military vehicle classification application [8]. Recorded signals were partitioned into $400\,\mathrm{ms}$-long events and sent to a signal energy detector to determine the presence of a vehicle. Detected events were transformed with the AtoI scheme with $f_0 = 5\,\mathrm{Hz}$ and 50 harmonics. Each 50-element harmonic magnitude vector was presented to a 3-layer neural network with 9 outputs corresponding to the vehicle types.

Neural network training used $1/3$ of the vehicle-present events with the remaining used for testing. Average single-event correct classification rate for this scheme was 87.7%. The time-domain harmonic amplitude (TDHA) technique [8] achieved a better average rate of 92.1%. Previously published results using the data set achieved 89.0% classification [11]. Both TDHA and the other approach include fundamental frequency estimation techniques and substantial digital computation complexity while AtoI assumes a fixed fundamental, is simply implemented, and performs comparably.

B. Classification including PVT errors

The range of circuit-induced errors which maintain acceptable classification performance was determined using the simulation model of Figure 7 to account for noise, offset, and nonlinearity effects on the projected values. Random signals noise_i and noise_h have spectral density simulated from transistor-level simulations. The memoryless nonlinearity function was directly extracted from the simulated OTA i_{out} vs. v_{in} curve. Aggregation of all other PVT errors are simply modelled as Gaussian random variables gain_L and offset_L with means 1 and $0\,\mathrm{V}$ respectively.

Classification performance was found to be insensitive to inter-channel G_m variations up through $\sigma_{\mathrm{gain}} = 25\%$. To maintain classification rates above 75% integrated offset standard deviation must be $< 4\,\mathrm{mV}$ and $10\,\mathrm{mV}$ at input SNRs of $10\,\mathrm{dB}$ and $20\,\mathrm{dB}$ respectively. Maximum output voltages of $\pm 1.2\,\mathrm{V}$ for the system therefore impose severe offset requirements of $\sigma_{\mathrm{os}} \approx 3\%$.

Statistical modelling of the implemented design using foundry-provided mismatch models was performed to estimate the hardware calibration performance. Figure 8 plots pre- and post-calibration output-referred voltage offset from a typical Monte Carlo run with $N = 100$. The designed tuning DAC was sized for small gate area and all transistor models were set for maximum mismatch (non-adjacent layout) to pessimistically estimate offset.

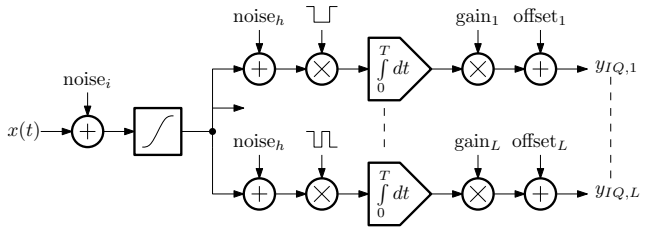

Fig. 7. Circuit error modelling in system-level simulation.

Un-tuned offset was $40.9\,\mathrm{mV}$ and would result in unacceptable classification. However, after simulated post-fabrication calibration, the resulting offset standard deviation is reduced to $< 1\,\mathrm{mV}$. This easily exceeds the requirement of $\sigma_{os} < 4\,\mathrm{mV}$ and therefore the system is expected to achieve classification rates better than 75%.

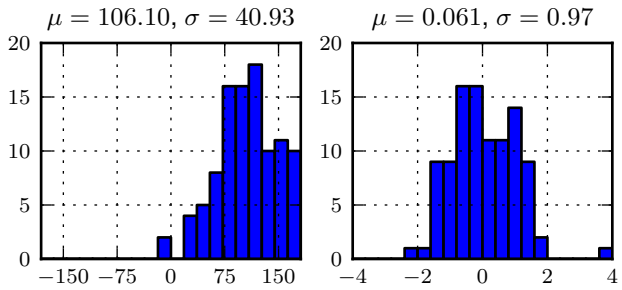

Fig. 8. Monte Carlo histogram comparing pre- and post-calibration output-referred offset in mV. Note the difference in horizontal scales.

V. Conclusion

An Analog to Information spectral decomposition scheme targeted for low-power parallel mixed-signal implementation has been presented. System architecture targeted for sub-micron technologies was described. Prototype design in a $130\,\mathrm{nm}$ CMOS technology was summarized. The chip is currently in fabrication, with measurements available for the presentation.

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