Load-pull Circles Analysis Method for Aplying the Outphasing Technique in Power Amplifier Design

Yolanda Jato, Amparo Herrera
Dpto. De Ingeniería de Comunicaciones
Universidad de Cantabria
Santander, España
Yolanda.jato@unican.es

Francis C. Huin
ACCO Semiconductors
Rue de la Princesse, 36-38
Louveciennes, France

***Abstract*—This paper presents a simple way of analyzing the suitability of a power amplifier for its use in an outphasing system. Simple steps are presented, allowing the designer to decide in advance if the outphasing technique will improve the efficiency versus back-off characteristic of the amplifier. For validating the method, an outphasing system for a Class AB amplifier has been designed, simulated and measured. In addition, a Class D amplifier has been also simulated to make a comparison of the results.**

Keywords—power amplifier; outphasing; Chireix combiner; high efficiency.

I. INTRODUCTION

Modern wireless communications systems use complex digital modulation techniques to obtain high data rates in a limited bandwidth. Consequently, power amplifiers must deal with signals with high PAPR (Peak to Average Power Ratio) or crest factors, requiring high linearity. The linearity is achieved by maintaining a large back-off between the average and peak RF power, which results in a degradation of the average efficiency of the power amplifier.

The challenge is then to preserve high linearity and high efficiency. To solve this problem, several methods have been proposed in the literature. Some are based on supply-voltage modulation, such as EER (Envelope Elimination and Restoration) and ET (Envelope tracking), another on load modulation, such as outphasing and Doherty [1]. All these techniques have their own limitations and they have been tested in practical applications. One of the most promising and most used in new applications is outphasing [2]-[3], since it can maintain high efficiency at back-off.

The objective of this paper is to show the application of this technique to amplifiers that has been already fabricated and tested, but need an improvement in efficiency vs. back-off in order to meet linearity specifications. Many papers explain the outphasing technique and demonstrate its behavior through power amplifiers designed specifically for the application. In this paper the starting point is an amplifier already designed and tested with a worst linearity than expected, which efficiency vs. back-off characteristic want to be improved with the outphasing technique.

We will show how to analyze the amplifier to implement the ouphasing circuit as well as how to know in advance if the amplifier is suitable for being used with this technique. This will save time and effort in the design process as we can decide prior to the design of the complete outphasing system if it is interesting to continue or not.

In Section II, the technique is applied to a Class D amplifier, which is the most used in the outphasing systems [4]-[5] together with the Class E. Section II presents a CMOS Class AB amplifier which efficiency want to be improved through the outphasing technique. In Section III the application of this analysis will be shown and in Section IV the simulation and measurements are presented. Finally, the conclusions are shown in Section V

II. CLASS D AMPLIFIER

To confirm the previous statements, a Class D amplifier from the ADS library has been simulated. In theory, this kind of amplifier is more suitable for the outphasing technique because it is less sensitive to load variations than the Class AB described in the next sections.

Fig.1 presents the load-pull circles of the class D amplifier. As can be seen, the area of the maximum PAE circle is quite

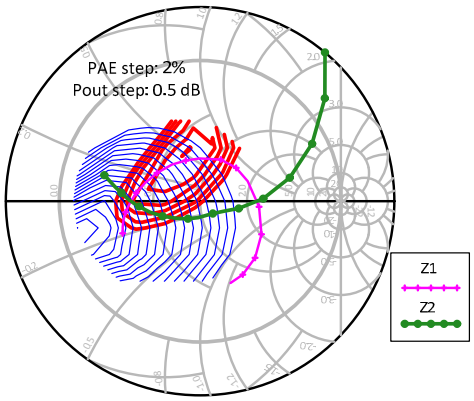

Fig.1 Input impedances of the Chireix combiner vs.amplifier load-pull circles (PAE in narrow line, Output power in thick line).

big, and it is cut by several ouput power circles giving the guarantee of a wide dynamic range. A Chireix combiner was designed for this amplifier; the impedances that are seen by the amplifier (Z1 and Z2) are represented in Fig. 1. Continuous wave simulations were performed to test if the results are what we expect. Fig. 2 (a) shows the comparison of the efficiency versus back-off of the amplifier alone and the outphasing system. It can be seen a great improvement in the back-off, preserving an efficiency of around 90% for a back-off of -6 dB. Fig.2 (b) shows the variation of the output power and the efficiency with the outphasing angle. In this case, the efficiency is maintained nearly constant from 25º to 60º and the variation of the output power within this range is of 5 dB.

III. WCDMA Power Amplifier

The power amplifier we want to improve is a class AB that has been designed in CMOS technology for 4G wireless communications and operates at 900 MHz. The Class AB amplifier is implemented due to its high linearity, very important in this kind of systems. The use of CMOS technology enables low cost and small size designs which are the most important requirements in this type of applications.

The amplifier has been fabricated and measured, the simulation and measurement results for the efficiency vs. the input power are shown in Fig.3. As can be seen in the figure, the PA obtain a maximum efficiency of 56% in simulation while in measurement the value is lower, around 50%.

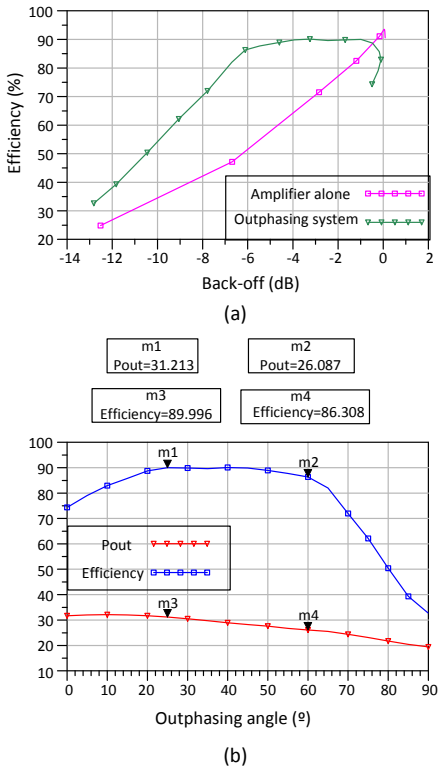

Fig.2. (a) PAE vs. back-off of the Class D amplifier alone and of the amplifier withing the outphasing system, (b) Variation of the PAE and the output power with the ouphasing an

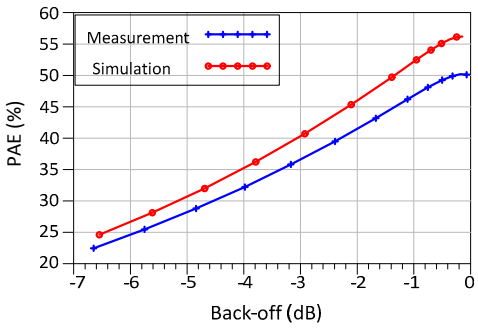

Fig.3. PAE vs. back-off of the WCDMA Class-AB power amplifier.

The difference between simulation and measurement is due to the higher current consumption in the fabricated amplifier that decrease the value of the efficiency. If we take the measured values as a reference, the amplifier is linear (with an ACLR< -40 dBc) until Pin=0 dBm. This input power value lead us to an efficiency of around 20%, value which is quite low, operating at a back-off of around -7 dB to have linear operation.

With the application of the outphasing technique, we look for an improvement in the efficiency versus back-off, which will allow the amplifier to operate with a higher back-off to meet linearity specifications without losing efficiency.

IV. Outphasing technique

In an outphasing system an input signal containing both amplitude and phase modulation is divided into two constant envelope phase-modulated signals, that when combined, reproduce the original signal. As the input signal to the amplifiers has constant envelope, they can operate in saturation with maximum power efficiency and in principle good linearity.

For combining the signal two classes of combiners can be used, the hybrid or the Chireix [6]. The Chireix seems to be the best option, it is an unmatched, lossless and non-isolating combiner that presents time-varying impedances to the PA as the phase difference between the branches change. This combiner is composed of two λ/4 transmission lines and two susceptances in parallel of opposite values in each line [7].

A. Design of the Chireix combiner.

The combiner was designed using microstrip lines instead of lumped components. The compensating susceptances were implemented using microstrip stubs and an SMD capacitor soldered between one of the stubs and ground. The value of the capacitor can be changed to modify the value of the compensating element.

One important step in the design of the combiner is to represent the input impedances versus the PAE and output power load-pull circles of the amplifier. By doing this, we can optimize the combiner to have the best possible response and obtain the maximum efficiency of the system.

For representing the impedances of the Chireix combiner two CW signals were introduced, making a sweep of the phase-shift between them (outphasing angle), with the objective of emulating the behavior of the typical input signal in this type of systems.

Fig. 4. Shows the load-pull circles of the amplifier versus the impedances of the combiner. This is an undesirable result since the impedances presented to the power amplifier with the variation of the outphasing angle do not cut perpendicularly the output power circles. They are somewhat parallel, so the variation of the output power with the angle will be small as well as the dynamic range we want to enlarge.

B. Modified Chireix combiner.

In order to solve the problem presented in the previous section, a new Chireix combiner has been designed. In this new configuration an additional transmission line has been added at the input of the combiner. With the addition of this line, the load impedance curves of the combiner rotates, so optimizing the length and impedance of the line, an optimum solution can be found. The load impedances curves cut the output power circles perpendicularly to obtain high dynamic range, and besides that, the impedances are within the circle of maximum PAE. Fig. 5 shows the new load impedances curves vs. the load-pull circles that achieve the wanted results.

As can be seen in Fig.5, there are several impedances that fall into the maximum PAE circle. Moreover, the widest dynamic range that we can achieve with this amplifier is obtained as all the output power curves are cut. However, and due to the characteristics of this amplifier, the dynamic range won't be very wide because the variation of the output power is only around 1 dB.

V. Simulation and Measurement Results

The outphasing system was simulated in ADS and evaluated by sweeping a continuous wave (CW) single tone at 880 MHz. At this frequency the outphasing angle was swept in order to modulate the output power. Fig.6a presents the efficiency versus back-off of the outphasing system.

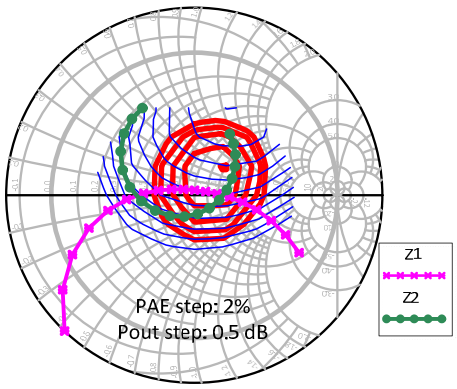

Fig.4. Input impedances of the Chireix combiner vs.amplifier load-pull circles (PAE in narrow line, Output power in thick line).

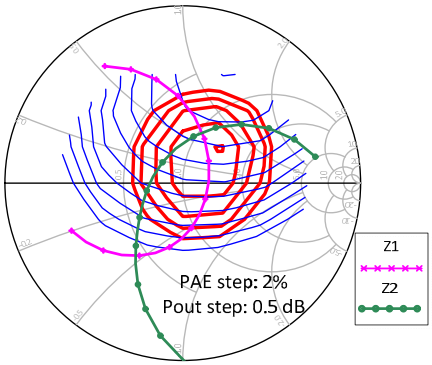

Fig.5. Input impedances of the modified Chireix combiner vs.amplifier load-pull circles (PAE in narrow line, Output power in thick line).

As we had predicted from the load-pull circles, the dynamic range is small but there is a little improvement in the PAE at a back-off of -4 dB of around 5%.

Fig. 6b shows the PAE and the Pout versus the outphasing angle. It can be seen that the maximum PAE is achieved for an angle between 25º and 40º, however, in this range, the variation of the output power is only 1 dB, which leads to a poor dynamic range.

In order to test the real behavior of the outphasing system, a test setup was built consisting of two CMOS power amplifiers as presented in Section III and a Chireix combiner fabricated with microstrip lines.

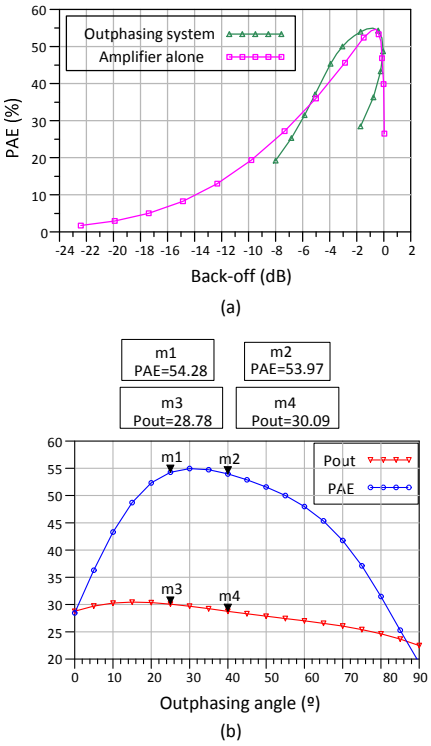

Fig.6. (a) PAE vs. back-off of the amplifier alone and of the amplifier within the outphasing system, (b) Variation of the PAE and the output power with the ouphasing angle.

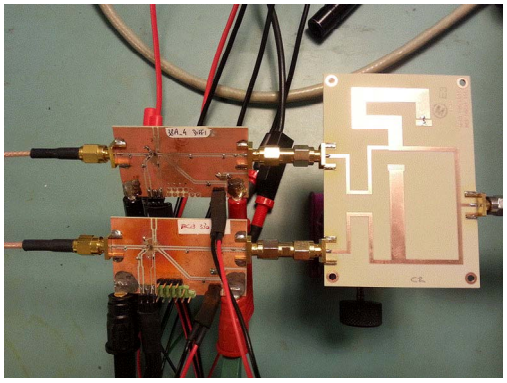

Fig.7. Photograph of the measurement setup.

A Rogers RO4003 high-frequency substrate with εr=3.3 was used for the combiner, and the value of the SMD capacitor placed in one of the stubs was fixed to 56 pF. Fig.7. shows the photograph of the combiner plus amplifiers used in the test.

For the measurements, two MXG-5182B RF vector signal generators were used to introduce the two continuous wave input signals with a sweeping of the phase shift between them. The results are presented in Fig. 8 where simulations and measurements of the amplifier alone and of the complete outphasing system are compared.

The maximum value of efficiency in the simulation results of the outphasing system has decreased compared to that shown in Fig.5; the reason is that in this case, the simulation was performed using the EM model of the combiner instead of the ideal circuit. With this model, the combiner behavior is more close to reality, resulting in higher losses and consequently, a degradation of the efficiency.

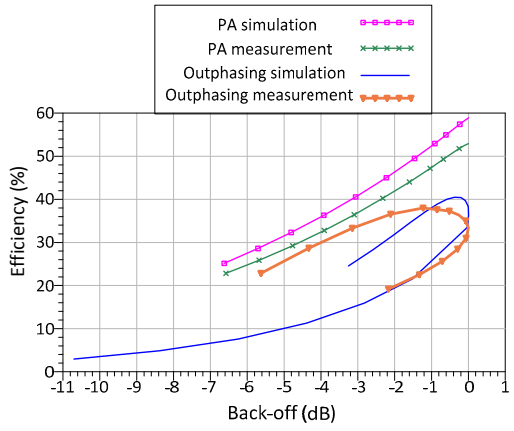

Fig.8. Efficiency vs. back-off of the PA alone and of the outphasing system for simulation and measurement.

If we compare the simulation and the measurement results of the outphasing system it can be seen that are quite close, with a maximum efficiency of 38 % and a back-off of -3 dB, obtaining a wider dynamic range than in the simulation. With lower substrate losses, closer results between simulation and measurement would have been obtained.

To summarize, the final conclusion can be that the amplifier we want to improve, is not suitable for the outphasing technique due to its own characteristics. The best way to know in advance if an amplifier is suitable for using the outphasing technique is by the inspection of the load-pull circles of the amplifier. The maximum PAE circle should have the biggest possible area in order to maintain this value during the widest range of outphasing angles. Moreover, this area must be cut by the maximum number of output power circles to guarantee the widest dynamic range.

If these requirements are met, the amplifier is suitable for applying the outphasing technique with a good result. Otherwise it is not worthy to continue with the design process because the efficiency versus back-off won't be improved.

VI. CONCLUSIONS

The ouphasing technique is a good method for improving the efficiency versus back-off in power amplifiers, but not all of them are appropriate for this kind of technique. A careful inspection of the load-pull circles will help the designer to decide in advance if the implementation of this technique will improve the efficiency of the amplifier or if it is better to use an alternative one such as envelope tracking.

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