

## Characterization of HV-CMOS detectors in BCD8 technology and of a controlled hybridization technique

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Radiation detectors built in high-voltage and high-resistivity CMOS technology are an interesting option for the large area pixel-trackers sought for the upgrade of the Large Hadron Collider experiments.

A characterisation of the BCD8 technology by STMicroelectronics process has been performed to evaluate its suitability for the realisation of CMOS sensors with a depleted region of several tens of micrometer. Sensors featuring  $50 \times 250 \mu\text{m}^2$  pixels on a  $125 \Omega\text{cm}$  resistivity substrate have been characterized.

The response to ionizing radiation is tested using radioactive sources and an X-ray tune, reading out the detector with an external spectroscopy chain. Irradiation tests were performed up to proton fluences exceeding  $5 \cdot 10^{15} \text{p/cm}^2$  and they show the depletion and breakdown voltages increases with irradiation.

A hybridization process for capacitive coupling has been developed. Assemblies have been performed using the ATLAS FE-I4 readout ASIC and prototype CMOS sensors. Measurements show a planarity better than  $1.5 \mu\text{m}$  peak-to-peak on the 5 mm length of the HV-CMOS chip. To evaluate more precisely the achievable uniformity dummy chips of FE-I4 sizes have been made on 6-inch wafers. The measurement of the 24 capacitors on each chip is expected to achieve a precise estimation of the real thickness uniformity. The goal is to achieve less than 10% variation on the glue thickness ( $\sim 0.5 \mu\text{m}$ ).

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## 1. Introduction

Hybrid semiconductor pixel detectors are a well established technology in the high energy physic field; large tracking detectors have been built and operated in different experiments at colliders. These detectors feature complex readout functions: this is possible since the sensor and the electronics are located on separated devices, connected through a bump bonding process, which is known to be suitable for this application but has the drawback of being expensive.

In view of the High Luminosity LHC upgrade, the experiments are studying upgrades for their tracking systems which will require several square meters of pixel detectors (*e.g.* the ATLAS experiments is planning a tracking detector with a total area of 8 – 12 m<sup>2</sup> of silicon [1]). For this reason it is important to explore new technologies that can reduce the cost and the production time of the sensors. These technologies have to be qualified to a dose of 0.1 – 1 Grad and to a NIEL equivalent to a fluence of 10<sup>15</sup> – 10<sup>16</sup> 1 MeV *n*/cm<sup>2</sup> (the higher limit corresponds to the innermost layers, the lower one to the outermost).

One of the proposed solution for the ATLAS upgrade is the use of a high-voltage CMOS technology, with a high resistivity substrate (HV-CMOS), in order to create a depleted region [2]. Using an high voltage technology, charge can be collected by drift, so these devices can provide a faster and larger signal with respect to the common active CMOS sensors and should guarantee a good radiation hardness. This kind of sensor can be capacitively coupled, instead of being bump-bonded, to their readout chip.

In this paper the suitability of the BCD8sP process by STMicroelectronics is investigated: this process is introduced in section 2, then the characterization of the sensor prototype is described in section 3. Furthermore, a new technique for controlling the capacitance of the coupling between the sensor and the front-end chip is presented in section 4.

## 2. BCD8sP technology

The STMicroelectronics BCD8sP [3, 4] is 160 nm technology and consists of a combination of bipolar, CMOS and DMOS devices. It allows to build low voltage (1.8 V) devices featuring a high voltage (up to 70 V) insulation. It is one of the major production lines for STM automotive products.

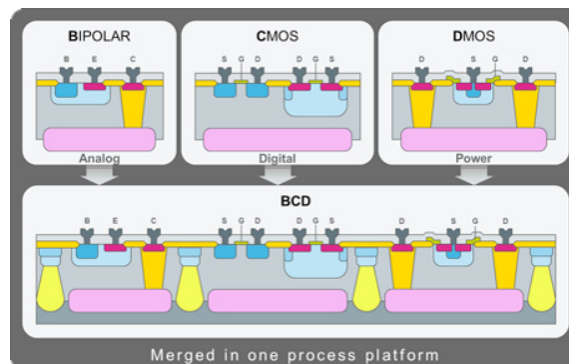


Figure 1: Scheme of the BCD8sP technology

This technology is based on a  $p$ -epitaxial growth on a  $p$ - or  $p$ + substrate; active devices are insulated from the substrate with a  $n$ -type buried layer implanted on the wafer, which act as cathode for the sensor diode. The NMOS transistors are placed in a  $p$ -well above the buried layer and the PMOS ones are in a second  $n$ -well: this allows the collection node to have a large fill factor, which, in turn, favors charge collection within a short drift distance, limiting the lateral drift and reducing traps recombination in irradiated devices.

### 3. Characterization of the KC53A prototype

In order to assess the suitability of the BCD8sP process for HV-CMOS detectors, a pixel sensor prototype, the KC53A, has been produced using a substrate with resistivity  $\rho = 125 \pm 25 \Omega \text{ cm}$ . It features twelve  $50 \times 250 \mu\text{m}^2$  pixels, 8 of which are active, *i.e.* they contain a charge sensitive amplifier, a buffer and a current injection circuit. The remaining 4 are passive sensors, *i.e.* the buried  $n$ -well (cathode of the sensor) is connected to a pad and there is no electronics above the pixel. The passive pixels have been tested: current-voltage (IV) and capacitance-voltage (CV) measurements have been performed on irradiated and non-irradiated devices; furthermore, some radioactive sources spectra measurements have been performed on non-irradiated chips.

The irradiation has been performed with a 62 MeV proton beam at Laboratori Nazionali del Sud (LNS), Catania, up to a dose of 119 Mrad. The characterization has been performed on a sample irradiated up to 57 Mrad, equivalent to a fluence of  $0.8 \cdot 10^{15} \text{ 1 MeV } n_{\text{eq}}/\text{cm}^2$ .

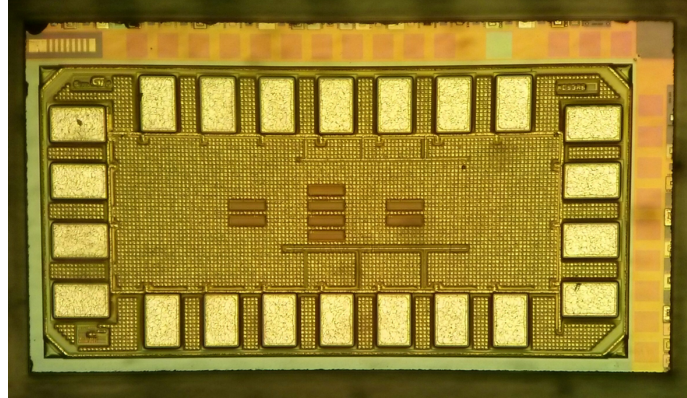


Figure 2: The KC53A chip.

#### 3.1 IV measurements

The current-voltage measurements have been performed at room temperature with a probe station and a Keithley 6517A electrometer. Particular attention has been kept in order to avoid to measure the current flowing through the protection diodes of the pads. The results are reported in figure 3 (a) and they show a good uniformity among the pixels. The measured leakage current is 1.2 pA per pixel at  $-50 \text{ V}$  bias. The breakdown voltage have been measured to be  $-70 \pm 1 \text{ V}$  for every pixel.

The IV curve has been measured after the irradiation too. The results are reported in figure 3 (b). A relevant increase of the leakage current to  $100 \div 120 \text{ nA}$  at  $-50 \text{ V}$  bias can be noticed.

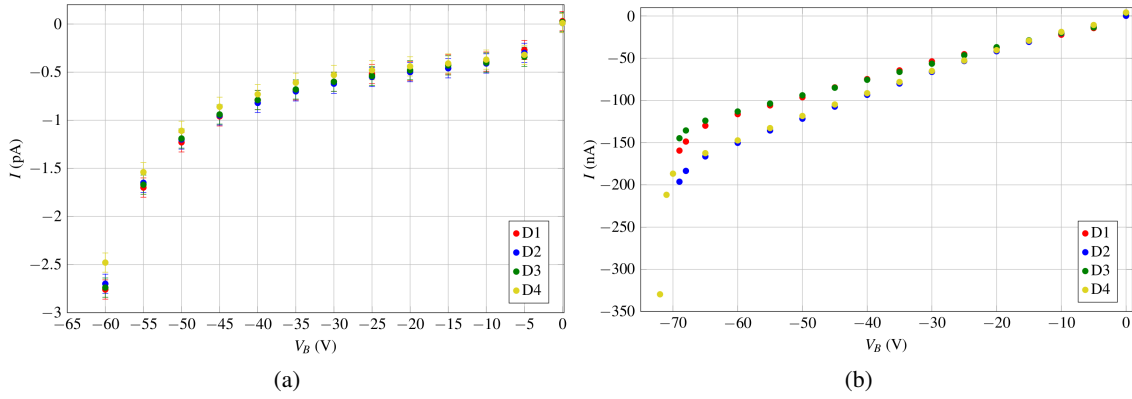


Figure 3: IV characteristics of the for diode of the non-irradiated chip (a) and of the irradiated chip (b).

The ATLAS FE-I4 chip can tolerate a maximum current input of 100 nA per pixel, so this value can be considered acceptable since the measurements have been performed at ambient temperature (20 °C) while irradiated sensors are usually operated at temperatures below 0 °C: a temperature variation of  $-20$  °C is enough to bring the leakage current to an acceptable level [7].

### 3.2 CV measurements

The capacitance-voltage measurements have been performed in the same conditions of the IV ones with an HP 4280A CV meter. The obtained results have been fitted with the following curve:

$$C(V_B) = C_P + \frac{1}{\sqrt{k(-V_B + V_0)}} \quad \text{with} \quad k = \frac{2\mu\rho}{\epsilon A^2}$$

in order to describe a constant parasitic capacitance ( $C_P$ , due to pads, connections, etc.) and the diode capacitance, which depends on the holes mobility  $\mu$ , the substrate resistivity  $\rho$ , the area of the sensor  $A$  and the built-in voltage  $V_0$ . The obtained results are reported in figure 4 (a) while the results of the fit are reported in table 1.

From this capacitance measurement it is possible to calculate the depletion depth using the parallel planes capacitor formula  $d = \epsilon A / C$ , obtaining  $d = 14 \div 16$   $\mu\text{m}$  at  $V_B = -50$  V. The result is not in good agreement with the simulations, which foresee a depletion depth of about 23  $\mu\text{m}$ . This contrast may be due to the fact that the parallel plane capacitor is not a good approximation of this sensor, since the contact for the bias voltage is on the top surface of the chip.

The measurements have been repeated after the irradiation and the results are reported in figure 4 (b). One can notice a decrease of the sensor capacitance which is consistent with a neutralization of the acceptors due to the radiation induced defects: this implies a decrease of the effective  $p$ -doping concentration, leading to an increase of the depleted zone.

### 3.3 Radioactive sources spectra

Sensitivity to energy deposition has been tested with photons emitted by a  $^{241}\text{Am}$  source, a  $^{55}\text{Fe}$  source and by a 50 kV X-ray tube. The sensor has been read out with a low-noise spectro-

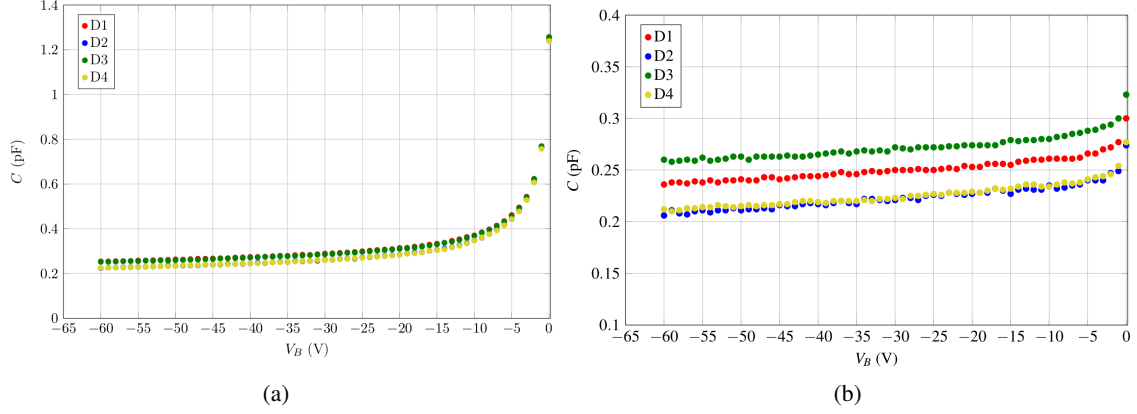


Figure 4: CV characteristics of the four diodes of the non-irradiated chip (a) and of the irradiated chip (b).

Table 1: Diode capacitance fit results. In the last column the sensor capacitance of the non-irradiated sample at  $V_B = -50$  V is reported.

	$C_P$ (pF)	$k$ ( $V^{-1} pF^{-2}$ )	$V_0$ (V)	$C - C_P$ (pF)
D1	$0.161 \pm 0.001$	$3.26 \pm 0.05$	$0.414 \pm 0.007$	$0.079 \pm 0.001$
D2	$0.125 \pm 0.001$	$2.82 \pm 0.06$	$0.46 \pm 0.01$	$0.087 \pm 0.001$
D3	$0.157 \pm 0.001$	$3.22 \pm 0.06$	$0.415 \pm 0.008$	$0.081 \pm 0.001$
D4	$0.126 \pm 0.001$	$2.90 \pm 0.06$	$0.45 \pm 0.01$	$0.085 \pm 0.001$

scopic chain consisting of a 4.25 mV/fC gain charge sensitive preamplifier and a shaper with a time constant of 1  $\mu$ s.

Since the  $^{241}\text{Am}$  spectrum features various peaks, this source has been used to calibrate the chain: the five visible peaks have been fitted with a Gaussian curve (see figures 5). The obtained calibration curve is  $E = (0.014 \cdot \text{channel} + 0.3)$  keV, the energy resolution is 0.6 keV on the highest energy peak.

After calibrating the chain, then spectra of the  $^{55}\text{Fe}$  and of the X-ray tube have been taken. In figure 5 (c) is reported the spectrum of the iron source: its peak corresponds to the expected energy deposition of a minimum ionizing particle in the depleted region of the diode (assuming a depletion depth of 23  $\mu$ m, obtained from simulations); in figure 5 (d) is reported the spectrum of the X-ray tube: the fluorescence lines of molybdenum (anode of the tube) and copper (this metal was present in front of the chip) can be noticed. The energy resolution on these lines is consistent with the  $^{241}\text{Am}$  measurement and their count rate as a function of the bias voltage is compatible with the increase of the depletion volume as  $\sqrt{V}$ .

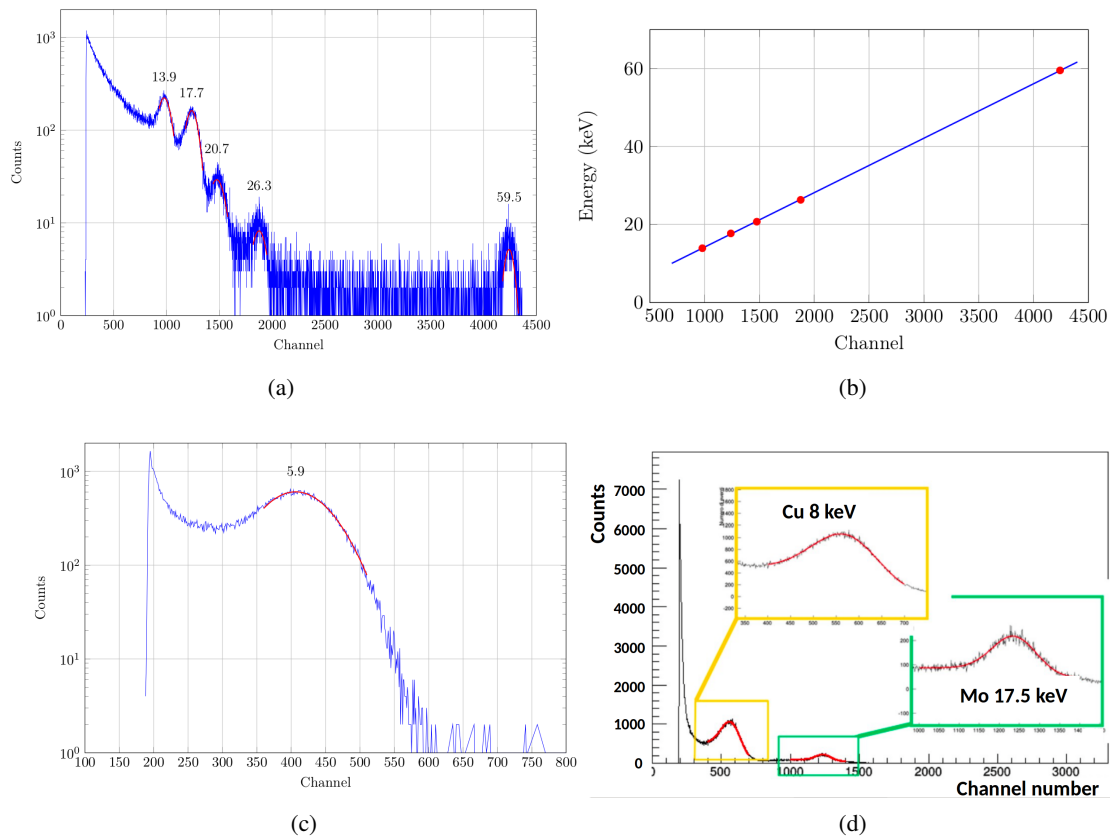


Figure 5: Spectra of the  $^{241}\text{Am}$  source (a), the  $^{55}\text{Fe}$  source (c), the X-ray tube (d) and the calibration curve (b). The numbers in figures (a) and (c) represents the peaks energies in keV.

#### 4. Hybridization process

A possible technique to connect a CMOS sensor to the readout chip is to glue the two devices with a dielectric adhesive, in order to form capacitor with their facing pads. This type of coupling is expected to be less expensive than the common bump bonding because it does not require the deposition of the metal bumps on one of the devices. However it is critical to control the glue layer thickness in order to have a uniform response all over the detector.

One possible approach is to use spacers distributed on the surface of the readout chip: a thin film of SU8 photoresist can be applied to the device by spinning and then pillars can be etched out. The pillars height can be tuned by the spinning speed: in our case  $5\ \mu\text{m}$  pillars have been deposited on FE-I4 chips [5] and they shows a good uniformity. Then an hybridization with HV2FEI4 chips [6] have been performed and the backside chip displays a planarity of better than  $1.5\ \mu\text{m}$  peak-to-peak over the 5 mm of the chip.

The pillars deposition at wafer lever is now being testes at Leonardo SpA (previosly Selex SI, Rome) on a production of test structures containing capacitors (see figure 7) which will allow to measure the glue thickness uniformity. The test structures size is approximately  $2 \times 2\ \text{cm}^2$  and when they will be glued together, the facing pads will form 3-7 pF capacitor, depending on the glue

electrical permittivity and planes separation.

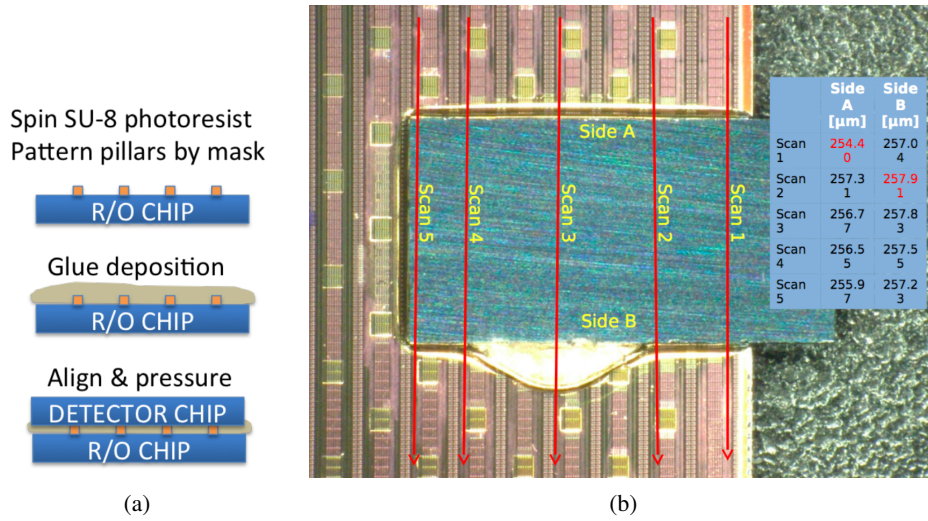


Figure 6: A simplified sketch of the hybridization technique (a) and a picture of a small CMOS sensor glued on a FE-I4 chip to test the planarity of the assembly (b). The red arrows show the direction of the scans, the table shows the height of the two sides of the CMOS sensor with respect to the FE-I4 chip.

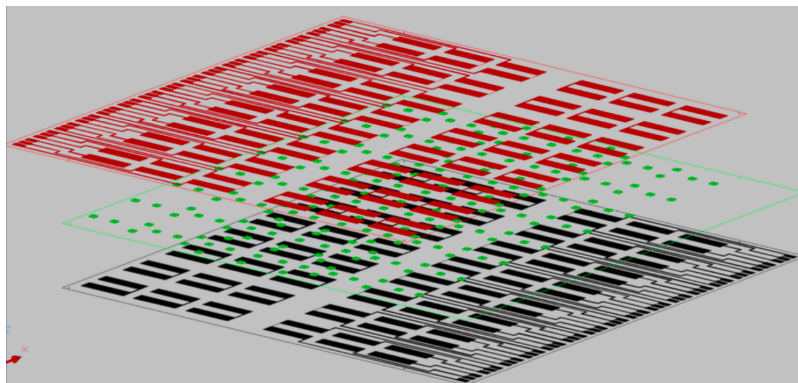


Figure 7: Scheme of the test structures: in red and black are reported the metal layers which forms the pads of the capacitors, in green the position of the SU8 pillars.

### 5. Summary

The suitability of the BCD8sP technology by STMicroelectronics for the development of CMOS pixel detectors has been tested. Sensors build on a 125  $\Omega\text{cm}$  substrate have been realized and the depleted region is wide enough to provide a measurable signal for a minimum ionizing particle. After a proton irradiation up to 119 Mrad an increase of the depletion region have been observed, as expected from acceptor neutralization.

A process for controlling the thickness of the glue layer coupling an active CMOS sensor and its readout chip is being developed. It is based on the deposition of SU8 pillars spacers and appears to be possible to obtain a 10% or better uniformity in the separation distance between the chips.

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