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CMOS IC RADIATION HARDENING BY DESIGN

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Abstract. *Design techniques for radiation hardening of integrated circuits in commercial CMOS technologies are presented. Circuits designed with the proposed approaches are more tolerant to both total dose and to single event effects. The main drawback of the techniques for radiation hardening by design is the increase of silicon area, compared with a conventional design.*

Key words: *radiation hardening, CMOS technology, integrated circuits*

1. INTRODUCTION

Commercial integrated circuits (ICs) may not have an adequate level of immunity to radiations to guarantee good reliability in harsh environments. Radiation hard circuits undergo a set of qualification tests, before being used in space (satellites) or in nuclear applications (high energy physics, nuclear power plants, medical equipments for radiology and radiotherapy). However, is worth remarking that every electronic equipment can be affected by low dose rate radiation, due to various sources: e.g., natural radioactivity in materials, high energy cosmic rays, X-ray scanners in airports, etc.

The evolution of IC fabrication technology towards ever more dense integration scale has a twofold effect on radiation tolerance: at modern nano-scale size, devices are more tolerant to cumulative (long-term) effects, but on the other hand they are more prone to soft errors due to single events. Therefore, design of complex integrated systems should account for such effects.

In recent years, specific techniques have been developed to obtain integrated circuits with a high immunity to radiations. Radiation tolerance can be increased either by modifying the fabrication process (RHBP: Radiation Hardening By Process), or by adopting design techniques (RHBD: Radiation Hardening By Design).

In this paper, RHBD techniques are presented, to achieve a satisfactory tolerance to both total dose and single event effects in MOS devices and circuits.

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2. INTERACTION BETWEEN RADIATION AND SILICON

The interaction between external radiation (photons like X-rays and γ-rays, charged particles like protons, electrons, and heavy ions, or neutral particles) and a semiconductor may cause two main phenomena: ionization and displacement.

2.1 Ionization phenomenon

When radiation interacts with the semiconductor material, an electron in the valence band may acquire enough energy to pass in the conduction band. Therefore, an electron-hole pair (HEP) is generated: a free electron is present in the conduction band and a hole in the valence band. If an electric field exists in the ionization region (e.g., in biased devices), HEPs are separated and carriers move within the semiconductor, giving an extra (parasitic) current. Then, the carriers may recombine, or remain trapped, or drift into an electrode.

The ionization phenomenon is measured with the Linear Energy Transfer (LET). The LET indicates the quantity of energy lost by the incident particle along its path into the target material. The LET depends on atomic number of the particles and on energy of the particle, target material and the collision location:

$$\mathrm{LET} = \frac{dE}{\rho \cdot dx} \quad \left[\mathrm{MeV} \cdot \frac{\mathrm{cm}^2}{\mathrm{mg}}\right] \tag{1}$$

where ρ is the density of the target material, and $\frac{dE}{dx}$ indicates the average energy transferred into the target material per length unit along the particle trajectory.

Ionization effects can be divided into two main categories:

- **temporary ionization effect** is due to HEP separation and generation of a parasitic current;
- **fixed ionization effect** is due to trapping of carriers in insulators, where the mobility of carriers is lower than in the semiconductor, or at the interface between insulator and semiconductor; when positive charges are trapped, a shift of device parameters occurs, and circuit performance may be affected.

2.2 Displacement

When a neutral particle interacts with the silicon lattice, it transfers energy to lattice atoms. A transferred energy greater than 20 eV can displace a silicon atom, which moves toward an interstitial position, and the displaced atom man displace other atoms along its trajectory.

Defects due to atom displacement in the silicon lattice act as energy levels within band-gap. These levels alter electric properties of semiconductor (e.g., life time of minority carriers, doping density, mobility, etc.).

3. RADIATION EFFECTS ON ICS

Damaging effects due to radiation can be divided into two major categories: **cumulative effects** due to a long-time exposure to radiation, and **single event effects** due to the interaction with a single particle.

3.1 Cumulative effects

From the viewpoint of circuit performance, cumulative effects can be divided into **total ionizing dose (TID)** effects, caused either by charged particles (e.g., electrons or protons), or by photons (X-rays and γ-rays), and **displacement damage dose (DDD)** effects, caused by massive particles (e.g., neutrons, protons, or heavy ions).

In CMOS integrated circuits, the most sensitive region to cumulative effects is the gate oxide. When a single particle collides with the oxide, HEPs are generated; if the ionized region is crossed by an electric field, electrons and holes are separated. Electrons are quickly collected by neighboring electrodes because their mobility is approximately 20 $cm^2/(Vs)$, while holes move slowly by hopping transport toward the SiO_2-Si interface, because their mobility ranges from 10^{-4} $cm^2/(Vs)$ to 10^{-11} $cm^2/(Vs)$. These holes remain trapped into the oxide for a long time (approximately from 10^3 s to 10^6 s) [1].

The trapped holes can be seen as fixed positive charges, which obviously introduce a negative shift in threshold voltage ΔV_{OT}, given by:

$$\Delta V_{OT} = -\frac{q}{c_{ox}}\Delta N_{OT} = -\frac{q}{\varepsilon_{ox}} t_{ox}\Delta N_{OT} \tag{2}$$

where q is the elementary charge, $C_{OX} = \varepsilon_{OX}/t_{OX}$ is the oxide capacitance per unit area, N_{OT} is the density of trapped holes into the oxide, ε_{OX} is the dielectric constant of the oxide, t_{OX} is the oxide thickness.

At the first degree of approximation, ΔV_{OT} is proportional to t_{OX}^2. For very thin gate oxide (e.g, for thickness lower than approximately 3 nm), threshold shift becomes negligible [2]. However, field oxides are thick (approximately in the range from 100 nm to 1000 nm) and trap positive charged particles. Charge trap effects occur especially in the Shallow Trench Isolation (STI) regions at the transition between field thick oxide and gate thin oxide. The region on the side of an STI can be modeled as a parasitic transistor in parallel to the MOS transistor channel. Parasitic transistors have the same length as designed transistors, however their voltage threshold is larger, due to thick oxide, so the parasitic transistors are normally turned off.

However, positive charged particles are trapped in the thick oxide region attract negative carriers, and this charge can be seen as a fixed charge on the gate of parasitic transistors that could turn on, thus creating a parasitic path between drain and source, in parallel with the MOS transistor channel. In an NMOS transistor, TID may induce a parasitic channel between the source and the drain, leading to a leakage current when the NMOS device is in the "off" state (Fig. 1). Furthermore, channel carriers can be trapped at the Si-SiO_2 interface [3], decreasing carrier mobility and transconductance.

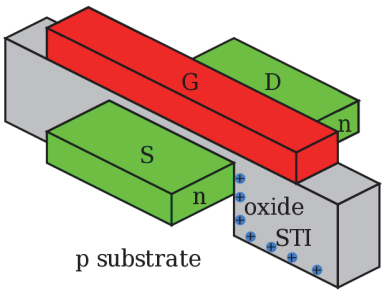


Fig. 1 Holes trapped in the shallow trench isolation (STI)

In a PMOS transistor, TID causes an increase of the threshold voltage and a reduction of the effective channel width. The latter effect is negligible for usual transistor sizes; however, for very narrow PMOS devices (with $W/L \ll 1$), this effect must be taken into account [4].

DDD effects are due to collisions between neutral particles and nuclei of silicon belonging to the lattice structure [5]. Lattice defects at Si-SiO_2 interface introduce energy states in the band-gap, which may trap channel carriers. The voltage threshold shift is:

$$\Delta V_{IT} = -\frac{Q_{IT}}{C_{OX}} \tag{2}$$

Where Q_{IT} is the trapped charge at the interface, which depends on device biasing.

Moreover, trap states due to lattice defects facilitate electron transitions between valence band and conduction band, and the carrier mobility decreases [6]:

$$\mu = \frac{\mu_0}{1+\alpha \cdot \Delta N_{IT}} \tag{3}$$

Where μ_0 is the pre-irradiated mobility, α is a parameter dependent on the chosen technology, N_{IT} is the number of charges trapped at interface.

It is important to point out that nowadays TID effects are negligible in the IC core. Therefore, only the circuit at the IC periphery (pad ring) require a special care, due to the higher voltage and the thicker oxide of the periphery transistors.

3.2 Single event effects

Single event effects (SEE) are due to charge generation in a reverse-biased p-n junction in the CMOS IC. The junction may be part of a MOS transistor (drain-body of source-body), or may be a well-substrate junction.

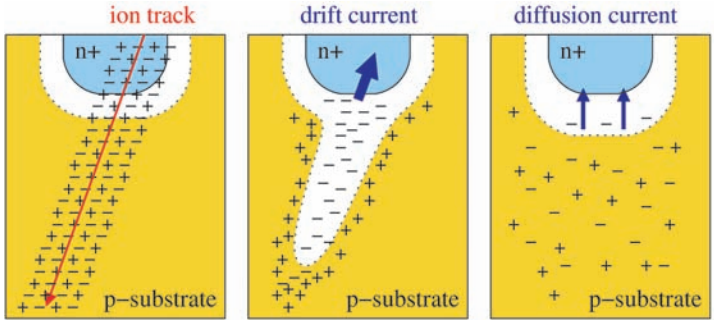


Fig. 2 Charge generation and parasitic current in a reverse-biased p-n junction

The electric field in the reverse-biased p-n junction separates electrons and holes. The generated carriers are collected by neighbouring electrodes, thus giving a parasitic current with a peak due to carrier drift, followed by a tail due to carrier diffusion (Fig. 2).

From a functional viewpoint, the current due to SEE may cause a **soft error**, which is a non-destructive and temporary effect, or a **hard error**, which cause irreversible effects and is destructive.

A soft error is a non destructive SEE, i.e., an effect that do not cause a permanent damage to the IC [7]. Soft errors occur when the total parasitic charge generated is larger than the critical charge of the affected node.

A **single event transient (SET)** is a transient glitch which affects the voltage of a node in combinational logic. Transients are temporary, however they may propagate to adjacent nodes where the effect of other SET can be added. Sometimes, the sum of SET can trigger damaging effects [8].

A **single event upset (SEU)** occurs when a SEE changes the logic value of a memory cell (e.g., a latch), or when SET propagation toggles the data stored into a memory [9]. If a SEU affects two or more memory cells, a **multiple bit upset (MBU)** occurs. A SEU in the control logic may lead to a **single event functional interruption (SEFI)**.

A **single event latch-up (SEL)** is due to a SEE that triggers on a positive gain loop due to parasitic bipolar transistors in CMOS technology, leading to a high current intensity in the loop, which may damage the IC interconnections if the device is not turned off promptly [10].

Other destructive SEE are the **single event burnout (SEB)**, which occurs in high voltage devices when an avalanche multiplication mechanism is triggered by a parasitic charge in a p-n junction reverse biased [11], and **single event gate rupture (SEGR)**, when the displacement effect combined with a high parasitic gate current can result in an oxide gate rupture [12]. SEB and SEGR occur in power MOS transistors, and are not a concern for CMOS logic. Hence, they will not considered in the following sections of the paper.

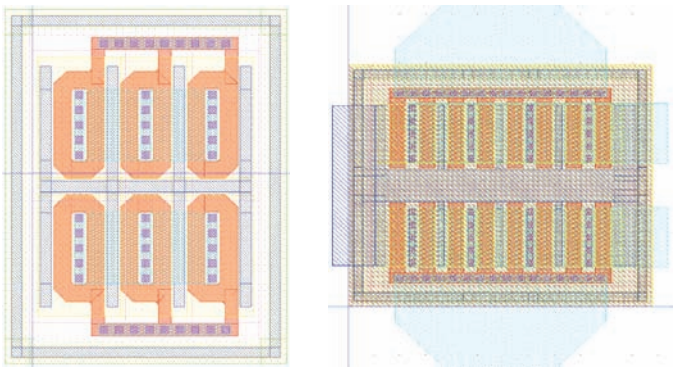
Sensitivity versus SEE is measured with the cross section (in square centimeters), which represent sensitive area of device.

4. Design of Radiation-Hardened MOS Devices

Special design techniques can be adopted to improve device tolerance to radiation.

4.1 NMOS transistors

Edge-less transistors (ELT) are MOS transistors with annular gate shape. This geometry was proved to reduce current leakage due to cumulative effects in NMOS transistors, even at very high total doses, at the expense of a larger area, as shown in Fig. 3(a) [13]-[14].



(a) (b)

Fig. 3 Layout of (a) NMOS ELTs; (b) conventional PMOS transistors

When using ELTs, the internal side of the ring-shaped transistor should be used as the drain terminal of the MOS device, and the external side should be the source terminal. In this way, the design minimizes the area of the drain, which is the most sensitive node for SEE, thus reducing the cross-section.

4.2 PMOS transistors

PMOS transistors are not prone to current leakage, since hole trapping do not attract channel carriers. Therefore, PMOS transistors do not require ELT shape, and they can be designed with conventional geometry, as shown in Fig. 3(b), in order to save area and to maintain the ratio between pull-up and pull-down transistor sizes.

4.3 Guard rings

The use of double guard rings around p-wells and n-wells, biased to constant voltages, prevents SEL [14].

Moreover, the use of guard rings around transistors of the same type biased at different voltages reduces inter-device leakage, since positive charges trapped in the STI oxide cannot induce a parasitic channel between n-type diffusions at different voltages (Fig. 4).

Fig. 5 shows a detail of the layout of a logic circuit employing both guard rings and ELTs.

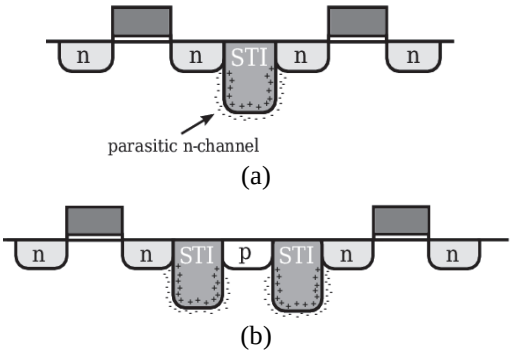


Fig. 4 Cross-section of two NMOS transistors: (a) without guard rings; (b) with guard rings between the two transistors

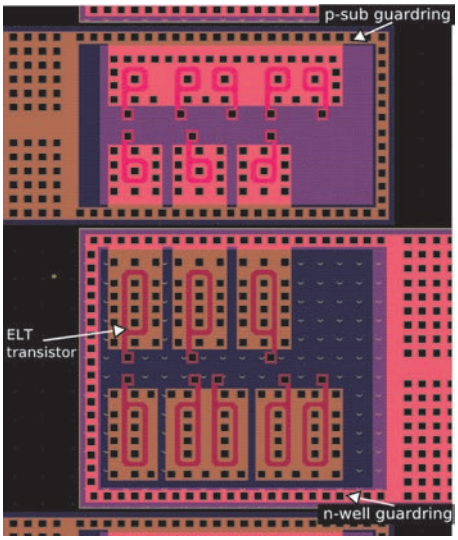


Fig. 5 Portion of a layout with ELTs and guard rings

Compared to conventional layout design, ELTs and guard rings require a larger silicon area. Therefore, a higher level of radiati

There are no sources in the current document.n tolerance can be achieved only at the expense of a larger area [15].

5. Design of Radiation-Hardened CMOS Circuits

An IC designer may use other radiation hardening techniques, such as redundancy and error correcting codes at the architectural level, and optimization of logic cells at circuit level.

5.1 Architectural solutions

At architectural level, radiation hardness can be improved by using redundant logic, such as ECC (error correcting codes).

Another example is the "scrambling" in a memory array: the physical location of bits do not correspond to the logical bit position, to avoid logical Multiple Bit Upset (MBU) due to SEE. A further improvement can be obtained by storing each bit of a byte into a different memory array, and by providing each memory array with separate bit-line and word-line decoders, to avoid MBUs due to address upset [15].

5.2 Logic circuits

Sensitivity to SEE can be analyzed through injection of "soft faults" in different circuit locations [17]. Simulation results demonstrate the most sensitive nodes with respect to SET are the circuit nodes which are not directly connected to voltage supplies. Therefore, SET sensitivity can be reduced by using fully CMOS logic and by minimizing the number of transistors which are not directly connected to supplies [18].

To mitigate SEFI, the numbers of feedback loops in the circuits must be minimized.

6. Conclusion

This paper has presented an overview of the effects due to the interaction between radiation and ICs. The overview also emphasizes some design techniques developed to avoid or to mitigate radiation effects.

It is important to remark that design solutions to improve radiation hardness lead to an increase of the IC area. Nevertheless, they should be adopted when robustness in radiation environment is an important parameter.

In addition, RHBD techniques in comparison with other approaches (shield or component selections) can be applied to different fabrication processes in order to increase the overall radiation hardening.

References

[1] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors," *Appl. Phys. Lett.*, vol. 48, pp. 133–135, Jan. 1986.

[2] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation effects in MOS capacitors with very thin oxides at 80 K," *IEEE Trans. Nucl. Sci.*, vol. 31, pp. 1249–1255, Dec. 1984.

[3] F. B. McLean, "A framework for understanding radiation-induced interface states in SiO2 MOS structures," *IEEE Trans. Nucl. Sci.*, vol. 27, pp. 1651–1657, Dec. 1980.

[4] M. Gaillardin, V. Goiffon, S. Girard, M. Martinez, P. Magnan, and P. Paillet, "Enhanced radiation-induced narrow channel effects in commercial 0.18 μm bulk technology," *IEEE Trans. Nucl. Sci.*, vol. 58, pp. 2807–2815, Dec. 2011.

[5] G. Baccarani and M. R. Wordeman, "Transconductance degradation in thin-oxide MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, pp. 1295–1304, Oct. 1983.
[6] J. R. Schwank, F. W. Sexton, M. R. Shaneyfelt, and D. M. Fleetwood, "Total ionizing dose hardness assurance issues for high dose rate environments," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 1042–1048, Aug2007.
[7] T. C. May, "Soft errors in VLSI: Present and future," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 2, pp. 377–387, Dec. 1979.
[8] J. L. Andrews, J. E. Schroeder, B. L. Gingerich, W. A. Kolasinski, R. Koga, and S. E. Diehl, "Single event error immune CMOS RAM," *IEEE Trans. Nucl. Sci.*, vol. 29, pp. 2040–2043, Dec. 1982.
[9] L. T. Clark, K. C. Mohr, K. E. Holbert, X. Yao, J. Knudsen, and H. Shah, "Optimizing radiation hard by design SRAM cells," *IEEE Trans. Nucl. Sci.*, vol. 54, pp. 2028–2036, Dec. 2007.
[10] Johnston, "The influence of VLSI technology evolution on radiation induced latchup in space systems," *IEEE Trans. Nucl. Sci.*, vol. 43, pp. 505–521, Apr. 1996.
[11] J. H. Hohl and K. F. Galloway, "Analytical model for single event burnout of power MOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 34, pp. 1275–1280, Dec. 1987.
[12] F. Wheatley, J. L. Titus, and D. I. Burton, "Single-event gate rupture in vertical power MOSFETs; an original empirical expression," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2152–2159, Dec. 1994.
[13] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Floria, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: practical design aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, pp. 1690–1696, Dec. 1999.
[14] Calligaro, V. Liberali, A. Stabile, M. Bagatin, S. Gerardin, and A. Paccagnella, "A multi-megarad, radiation hardened by design 512 kbit SRAM in CMOS technology," in *Proc. IEEE Int. Conf. on Microelectronics (ICM)*, Cairo, Egypt, Dec. 2010, pp. 375–378.
[15] M. Benigni, V. Liberali, A. Stabile, and C. Calligaro, "Design of rad-hard SRAM cells: A comparative study," in *Proc. IEEE Int. Conf. on Microelectronics (MIEL)*, Niš, Serbia, May 2010, pp. 279–282.
[16] Stabile, V. Liberali, and C. Calligaro, "A radiation hardened 512 kbit SRAM in 180 nm CMOS technology," in *Proc. Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Hammamet, Tunisia, Dec. 2009, pp. 655–658.
[17] Do, V. Liberali, A. Stabile, and C. Calligaro, "Layout-oriented simulation of non-destructive single event effects in CMOS IC blocks," in *Proc. Eur. Conf. on Radiation and Its Effects on Components and Systems (RADECS)*, Bruges, Belgium, Sep. 2009.
[18] Stabile, V. Liberali, and C. Calligaro, "Design of a rad-hard library of digital cells for space applications," in *Proc. Int. Conf. on Electronics, Circuits and Systems (ICECS)*, Malta, Sept. 2008, pp. 149–152.