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Temperature Sensitivity based on Channel Length of FinFET Transistor

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ABSTRACT

This paper presents the temperature sensitivity of the gate length-based fin field effect transistor (FinFET) and the possibility of using such a transistor as a nano-temperature sensor. The multi-gate field effect transistor (MuGFET) simulation tool is used to investigate the temperature characteristics of FinFET. Current–voltage characteristics with different temperatures and gate lengths (Lg = 25, 45, 65, 85 and 105 nm) are initially simulated, then the metal oxide semiconductor diode mode connection to measure FinFET temperature sensitivity is considered. The best temperature sensitivity of the FinFET is observed on the basis of the largest ΔI at the working voltage V_{DD} range of 0–5 V. Furthermore, temperature sensitivity of the FinFET increased linearly with channel length at the range of 25–105 nm.

1. Introduction

Many new field effect transistor (FET) structures have been extensively explored given that the metal oxide semiconductor FET (MOSFET) technology has continued to approach its downscaling limits. One of the relatively newer FETs is the FinFET (Fig. 1) [1], a transistor-structured FET that is a popular research topic in the academic field and semiconductor industry [2-5].

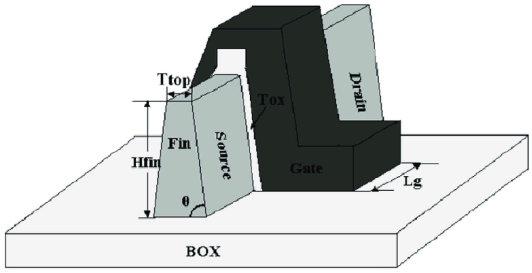

Fig. 1 FinFET structure [1]

The best example of sensors for subsumed electronic applications (i.e. used within an equipment) is the semiconductor temperature sensor [6]. Transistor-based temperature sensors are designed on the basis of the temperature characteristics of current–voltage curves of nanowire transistors [7-10]. A bipolar transistor can be used as a temperature sensor by connecting its base and collector and operating them in diode mode. Similarly, a transistor with MOSFET structure can be used as a temperature sensor by connecting the gate with either the source or drain (Fig. 2). Electronic devices, such as diodes, transistors, capacitors and resistors, with nano-dimensions have recently become popular in the electronics industry due to their extremely small electronic circuits.

The performance of new devices, which may correspond to a wide array of new applications, will likely depend on the nano-dimensional characteristics of such devices. The chip generation of these relatively new and powerful electronic devices with ultra-small transistors may be even regarded more trustable when new findings from future research are consolidated. However, the new nano-dimensional FET designs and structures are still considered novel technologies and thus necessitate further study and improvement, and they require further innovations despite the limitations in the field of MOSFET science.

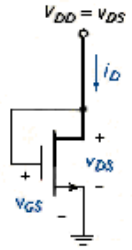

Fig. 2 MOSFET as a temperature sensor (Vg = Vd = V_{DD})

Electronic device simulation has become increasingly important in understanding the physics behind the structures of new devices. Thus, simulation tools are adopted in this research for the analysis and evaluation of the performance limits of nanowire structures. Experimental work can be supported by simulation tools to further explore the development of MuGFETs for nano-dimensional characterisation [11]. Simulation tools can also help identify device strengths and weaknesses and retrenchment costs and illustrate the extensibility of these devices in the nm range [12, 13].

2. Experimental Methods

In this research, MuGFET is used as the simulation tool to investigate the characteristics of the FinFET transistor. The output characteristic curves of the transistor under different conditions and with different parameters are considered.

The effects of variable values, namely, temperature and gate length, on the nanowire transistor are determined on the basis of the I–V characteristics derived from the simulation. The MuGFET [14] simulation tool used for the FET with nano-dimensional structure is developed and designed by Purdue University (USA).

MuGFET can select either PADRE or PROPHET for simulation, in which both simulates are developed by Bell Laboratories. PROPHET is a partial differential equation profiler for one, two or three dimensions, whereas PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry [14]. The software can generate useful characteristic FET curves for engineers, especially to fully explain the underlying physics of FETs. MuGFET can also provide self-consistent solutions to Poisson and drift-

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diffusion equations [15] and can be used to simulate the motion of transport objects when calculating channel characteristics (Fig. 1) [1].

In this research, the Id–Vg characteristics of FinFET at the temperatures of 250, 275, 300, 325, 350, 375 and 400 K are simulated with the following parameters: channel width = 30 nm, channel concentration (P-type) = 10^{16} cm^{-3}, source and drain lengths = 50 nm, source and drain concentration (N-type) = 10^{19} cm^{-3} and oxide thickness = 2.5 nm. The gate length values are Lg = 25, 45, 65, 85 and 105 nm.

3. Results and Discussion

Figs. 3 to 7 show the change in ΔI when the temperature increased at the V_{DD} range of 0–5 V at 0.25 V steps for the Lg values of 25, 45, 65, 85 and 105 nm. As shown by the figures, the maximum sensitivities (max ΔI) are at the relatively lower temperatures, and the values decreased linearly as temperature increased for all V_{DD}. Figs. 3 and 4 present the maximum temperature sensitivity values at V_{DD} = 1.5 V (Lg = 25 nm) and V_{DD}=2.75 V (Lg = 45nm); followed by Figs. 5 and 6 at V_{DD} = 3.75 V (Lg = 65 nm) and V_{DD} = 4.25 V (Lg = 85 nm; and finally, Fig. 7 at V_{DD}=5 V (Lg = 105 nm).

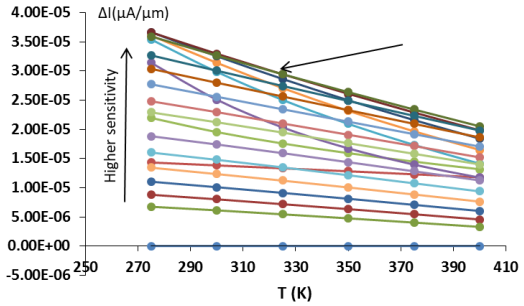

Fig. 3 ΔI–Temperature characteristics of FinFET (Lg = 25 nm)

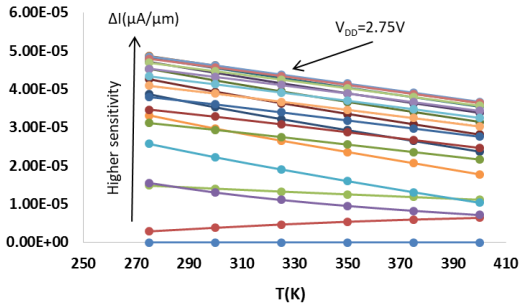

Fig. 4 ΔI–Temperature characteristics of FinFET (Lg = 45 nm)

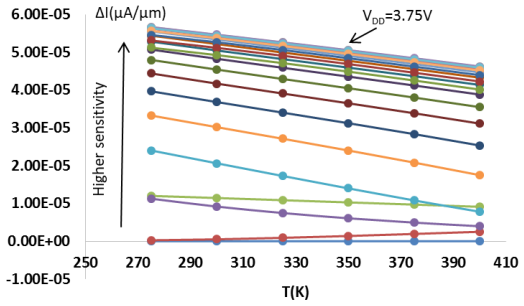

Fig. 5 ΔI–Temperature characteristics of FinFET (Lg = 65 nm)

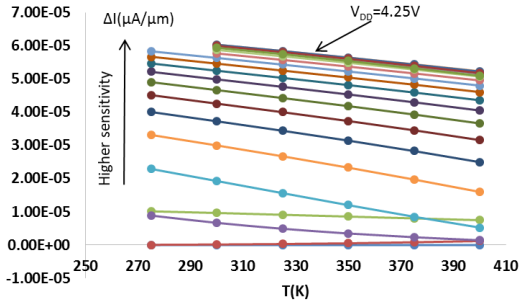

Fig. 6 ΔI–Temperature characteristics of FinFET (Lg = 85 nm)

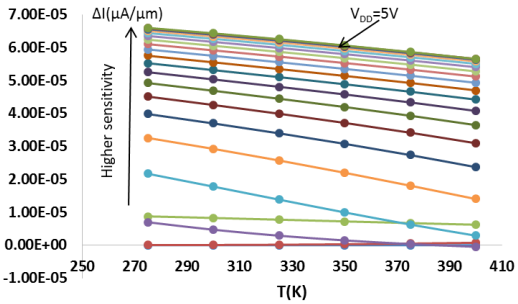

Fig. 7 ΔI–Temperature characteristics of FinFET (Lg = 105 nm)

Figs. 8 to 12 show the changes in ΔI with decreasing V_{DD} at T = 250, 275, 300, 325, 350, 375 and 400 K and Lg = 25, 45, 65, 85 and 105 nm. The following maximum sensitivities (max ΔI) were observed: V_{DD} = 1.5 V (Lg = 25 nm), V_{DD} = 2.75 V (Lg = 45 nm), V_{DD} = 3.75 V (Lg = 65 nm), V_{DD} = 4.25 V (Lg = 85 nm) and V_{DD} = 5 V (Lg = 105 nm).

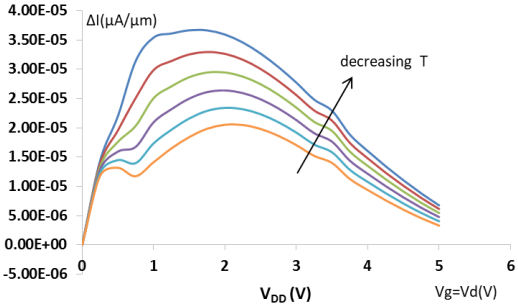

Fig. 8 ΔI–V_{DD} characteristics of FinFET (Lg = 25 nm)

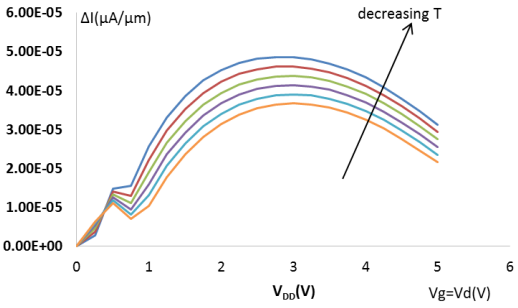

Fig. 9 ΔI–V_{DD} characteristics of FinFET (Lg = 45 nm)

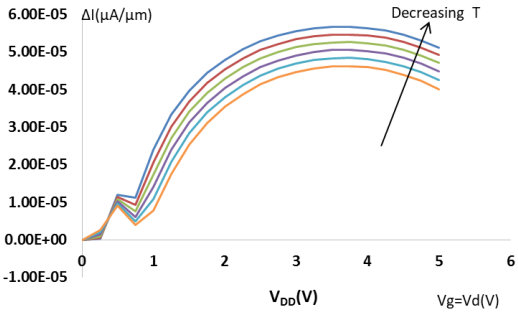

Fig. 10 ΔI–V_{DD} characteristics of FinFET (Lg = 65 nm)

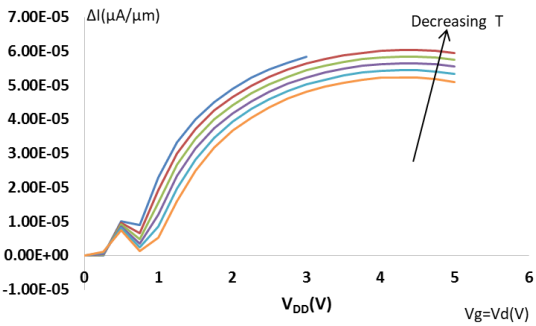

Fig. 11 ΔI–V_{DD} characteristics of FinFET (Lg = 85 nm)

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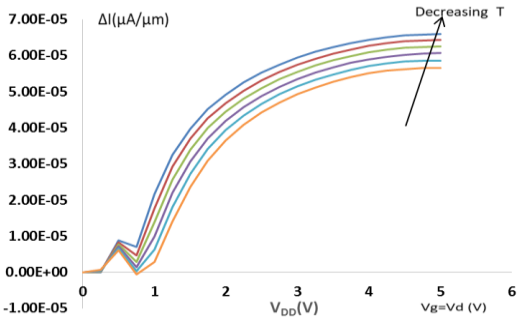

Fig. 12 ΔI–V_{DD} characteristics of FinFET (Lg = 105 nm)

Fig. 13 shows the optimised operating voltage V_{DD} based on the best temperature sensitivity and channel length, in which the optimised V_{DD} is related to the temperature sensitivity peaks shown in Figs. 8–12. Temperature sensitivity increased remarkably until channel length reached 105 nm and increased only slightly from 65 to 85 nm. Finally, a linear increasing relationship is observed between temperature sensitivity and channel length beyond 85 nm.

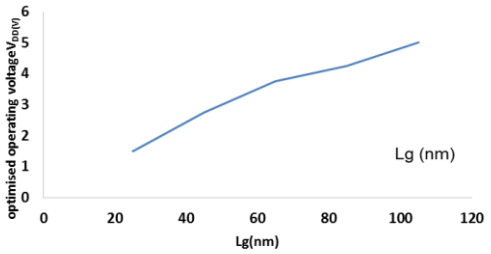

Fig. 13 Optimised operating voltage V_{DD} with different channel lengths based on best temperature sensitivity

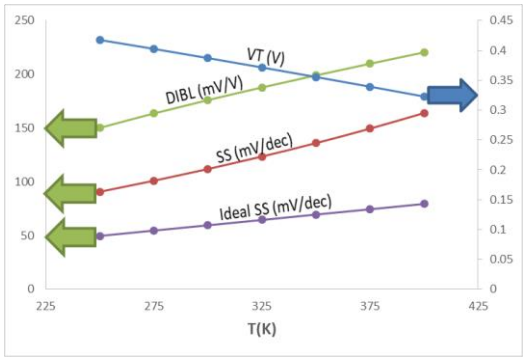

Fig. 14 V_T, SS and DIBL at Lg = 45nm

Fig. 14 presents the temperature characteristics of threshold voltage (V_T), subthreshold swing (SS) and drain-induced barrier lowering (DIBL) of the FinFET, in which the characteristics are obtained at T = 250, 275, 300, 325, 350, 375 and 400 K at Lg = 45 nm. V_T decreased linearly with increasing the temperature, i.e. V_T = 0.42 V at the lower temperature of 250 K and V_T = 0.32 V at the higher temperature of 400 K. Meanwhile, SS started at 90.74 mV/dec at the lowest temperature (the nearest value to the ideal SS at 49.6 mV/dec) at 250 K and increased until it reached 163.98 mV/dec (the farthest value from the ideal SS at 79.4 mV/dec) at 400 K. Finally, DIBL increased as temperature increased.

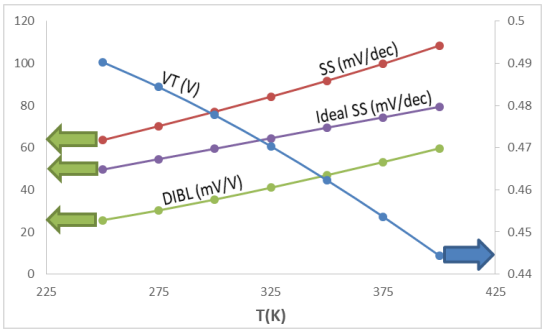

Fig. 15 V_T, SS and DIBL at Lg = 65 nm

Fig. 15 illustrates the V_T, DIBL and SS characteristics of the FinFET at T = 250, 275, 300, 325, 350, 375 and 400 K at Lg = 65 nm. This linear relationship further implies that fat reduces fermentation from 250 K to 400 K at V_T = 0.49 and 0.44 V, SS = 63.58 and108.42 mm/dec and DIBL = 25.60 and 59.66 mm/V, respectively. In addition, when temperature increased to 400 K, SS = 63.58 mm/dec (the farthest value from the ideal SS = 49.6 mm/dec).

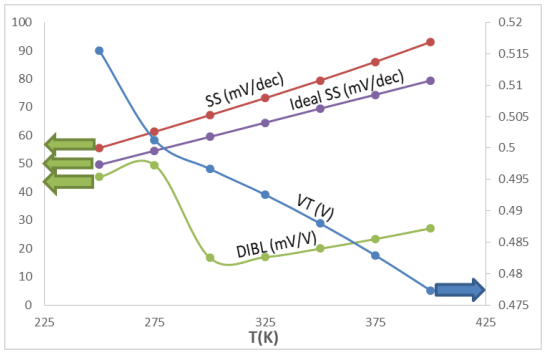

Fig. 16 V_T, SS and DIBL at Lg = 85 nm

Fig. 16 presents the changes in V_T, SS and DIBL and their effects on FinFET properties when temperature increased from 250 K to 400 K at Lg = 85 nm. V_T decreased linearly with increasing temperature. From 250 K to 400 K, V_T = 0.515 and 0.47 V, SS = 55.54 and 93.04 mV/dec and DIBL = 45.32 and 27.12 mV/V, respectively. The figure also illustrates that SS = 55.54 mV/dec (the farthest value from the ideal SS = 49.6 mV/dec at 400 K).

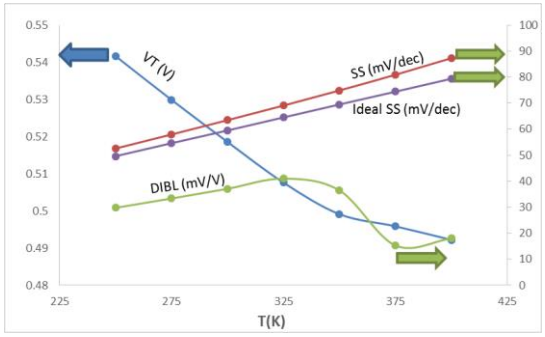

Fig. 17 VT, SS and DIBL at Lg = 105 nm

Fig. 17 shows the change properties of V_T, SS and DIBL and their effect on FinFET properties when temperature increased from 250 K to 400 K at Lg = 105 nm. The values of V_T, SS and DIBL decreased with increasing temperature. This figure particularly represents the limits of the decrease from 250 K to 400 K for V_T = 0.541 and 0.49 V, SS = 52.53 and 87.29 mV/dec and DIBL = 29.76 and 18.005 mV/V, respectively. SS values increased with increasing temperature until they are being away to the ideal values.

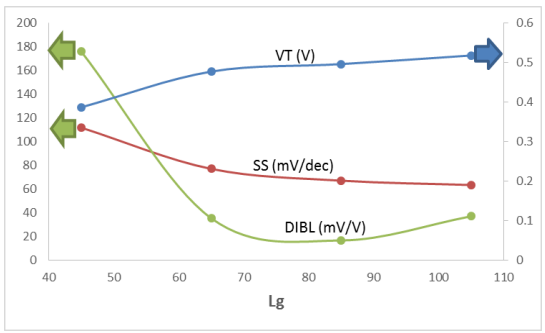

Fig. 18 VT, SS and DIBL characteristics Lg

Fig. 18 shows the V_T, SS and DIBL characteristics with increasing FinFET channel length with 45–105 nm at 20 nm steps at T = 300 K. V_T increased with increasing channel length and almost reached saturation beyond 65 nm; SS decreased and nearly reached the ideal value beyond 65 nm; and DIBL decreased strongly as it approached 65 nm and increased slightly beyond 65 nm. Thus, as presented by this figure, the perfect channel length for the FinFET under the conditions considered in this research is 65 nm.

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4. Conclusion

The effects of different temperatures (250, 275, 300, 325, 350, 375 and 400 K) on FinFET characteristics are studied by considering different channel lengths (Lg = 25, 45, 65, 85 and 105 nm). For the diode mode transistor connection, the best increments for the current (ΔI) in relation to temperature can be achieved by increasing channel length to 105 nm, beyond which the values become stable regardless of channel length. The V_T, SS and DIBL characteristics with increasing FinFET channel length with 45–105 nm at 20 nm steps at different temperatures (250, 275, 300, 325, 350, 375 and 400 K) was studded. V_T increased with increasing channel length and almost reached saturation beyond 65 nm; SS decreased and nearly reached the ideal value beyond 65 nm; and DIBL decreased strongly as it approached 65 nm and increased slightly beyond 65 nm. Thus, as presented by this study, the perfect channel length for the FinFET under the conditions considered in this research is 65 nm.

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