Chip-Integrated Voltage Sources for Control of Trapped Ions

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(Received 24 October 2018; published 5 February 2019)

Trapped-ion quantum-information processors offer many advantages for achieving high-fidelity operations on a large number of qubits, but current experiments require bulky external equipment for classical and quantum control of many ions. We demonstrate the cryogenic operation of an ion trap that incorporates monolithically integrated high-voltage complementary metal-oxide semiconductor (CMOS) electronics (±8 V full swing) to generate surface-electrode control potentials without the need for external analog voltage sources. A serial bus programs an array of 16 digital-to-analog converters (DACs) within a single chip that apply voltages to segmented electrodes on the chip to control ion motion. Additionally, we present the incorporation of an integrated circuit that uses an analog switch to reduce voltage noise on trap electrodes due to the integrated amplifiers by over 50 dB. We verify the function of our integrated electronics by performing diagnostics with trapped ions and find noise and speed performance similar to those that we observe using external control elements.

DOI: 10.1103/PhysRevApplied.11.024010

I. INTRODUCTION

Quantum computers and simulators based on trapped atomic ions have great potential to allow for the execution of complex algorithms but, to date, experiments have been limited to tens of ion qubits. Increasing the size of linear chains of ions presents experimental challenges including optical addressing and control of individual ions, arbitrary reordering of ion positions during complex protocols, and limited lifetimes of long chains [1,2]. Alternatively, array-based designs that naturally solve these issues have been discussed recently [3,4]. The array architecture has a clearer path toward increasingly complex designs and might also benefit from modern semiconductor fabrication techniques. These architectures will require integration of control elements into the vacuum chamber to reduce the number of required interconnects. Off-the-shelf electronics have been modified and attached to trap hardware in vacuum [5,6], but as array architectures expand beyond tens of control zones, the required circuitry for electrode control within a zone will occupy significantly more area than the footprint of an array site. Integrating devices into the trap array itself could potentially solve this scaling problem but this design will require a trade-off among device area, power, speed, and noise. Beyond quantum-information processing, other chip-based technologies, such as miniature atomic clocks [7] or sensors [8], could also benefit from these highly integrated low-power control systems.

In this work, we advance the integration of control voltages to the microscopic level by presenting a design for a voltage source, with performance similar to modern external sources, that is incorporated into the substrate beneath the electrodes of an ion trap. Surface-electrode ion traps are typically fabricated in custom lithographic processes that involve deposition and patterning of a few metal layers [9–14]. Recently, it has been shown that planar ion traps can also be manufactured in commercial complementary metal-oxide semiconductor (CMOS) processes, which offer improved design reproducibility and can reduce fabrication costs of more complex devices [15]. Here, we extend the foundry-produced ion-trap design to include voltage sources integrated into the semiconductor substrate. The addition of active electronics in such close proximity to the trap presents a challenge, since ions are sensitive to both the static and fluctuating electric fields generated within the integrated circuit. We carefully characterize the noise and speed of these chip-integrated devices for quantum-information applications;

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the architecture may also be of general interest in deployable systems, due to the high repeatability and functionality afforded by CMOS technology. Explorations such as this, which evaluate the performance of quantum systems with advanced classical control, are key to assessing the utility of modern control technology for future quantum sensors, simulators, and computers.

II. DESIGN OF A HIGH-VOLTAGE DIGITAL-TO-ANALOG CONVERTER

Voltages are derived from an *R*-2*R* resistor-ladder digital-to-analog converter (DAC) [16] with 12 bits of resolution and an output range of approximately ±8 V(see Fig. 1). The DAC accepts a 12-bit code word that it translates to an analog voltage on its output [see example data in Fig. 1(e)]. We program the DACs using an integrated serial-peripheral-interface (SPI) bus, controlled by an external field-programmable gate array (FPGA) running custom firmware. The ion trap has 16 control electrodes, with one DAC to independently bias each one. Data is serially daisy chained through the SPI bus, for a total of $16 \times 12 = 192$ bits of voltage data. In order to update the voltage on any or all electrodes, the full 192-bit string is sent to the chip.

The devices are fabricated as part of a multiproject wafer through the MOSIS service in the GlobalFoundries CMHV7SF 180 nm node. We choose this process for its

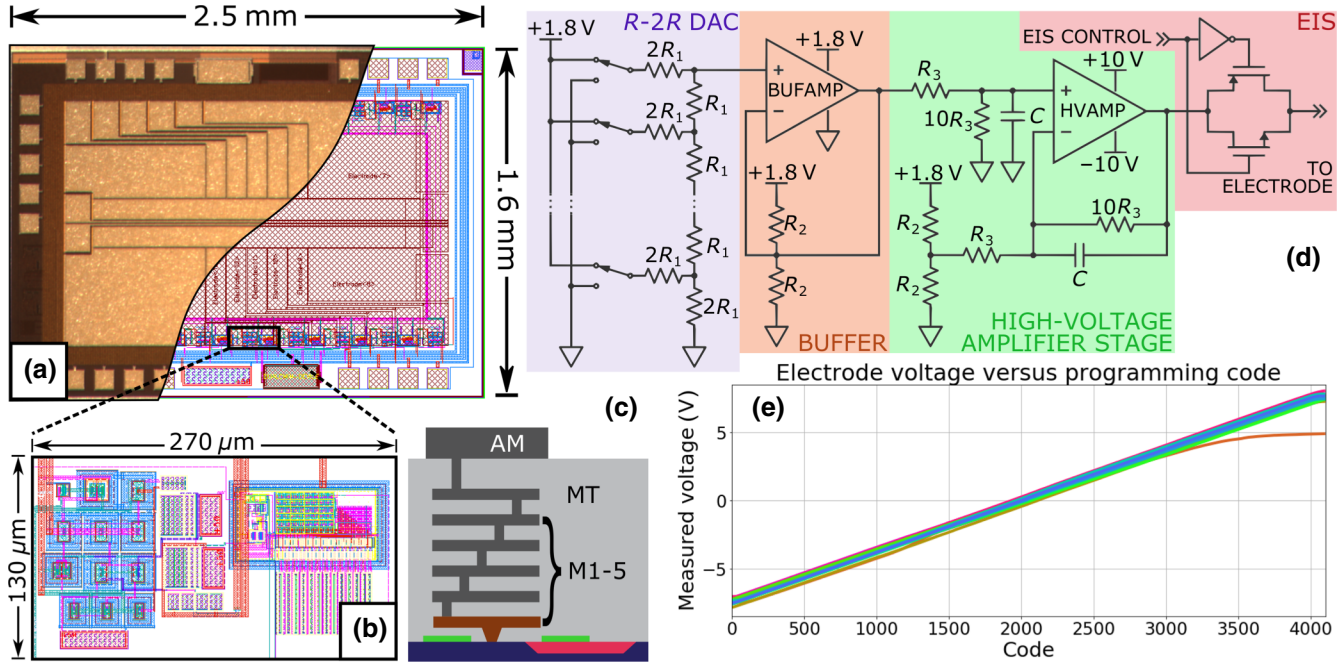

FIG. 1. (a) A micrograph of the top metal layer of the chip. The small squares around the edge of the chip are wire-bond pads for connecting power (four redundant groups of four) and digital control (one group of five). The two largest parallel electrodes in the center of the trap are the radio-frequency (rf) electrodes, which provide ponderomotive radial confinement and are controlled by an external source. The other 14 electrodes at the top and bottom of the chip plus two additional electrodes in the middle of the trap are the dc electrodes, which provide axial confinement and are controlled by the integrated voltage sources. The cutaway reveals the layout of the circuit in the internal layers. The different colors in the figure represent different signal planes. (b) The layout of one complete digital-to-analog-converter (DAC) block shown in the schematic in (d). There are 16 such blocks on the chip. The integrated devices fit beneath the trap electrodes and take up 15% of the total device area. The squares on the left side of the diagram are the high-voltage field-effect transistors (FETs); each is approximately 27 μm × 29 μm. (c) The layer stack-up for the CMHV7SF 180 nm node (not to scale). The total thickness of the lithographic layers is about 15 μm. The trap electrodes are defined in the topmost metal layer (AM). The lowest metal layer (M1) is made of copper, unlike the other (aluminum) metal layers, and has a higher current capacity. M1 is used for routing power around the edge of the chip. Active devices (e.g., DACs and amplifiers) are patterned in the silicon layers at the bottom of the diagram. (d) A schematic illustrating the four stages of each integrated circuit block. The *R*-2*R* DAC converts a 12-bit digital code into an analog voltage from 0 V to 1.8 V. A serial-peripheral-interface (SPI) bus (not shown) programs the state of the switches in the *R*-2*R*. A unity-gain buffer (BUFAMP) follows the DAC and isolates the resistor ladder from the rest of the circuit. The high-voltage amplifier (HVAMP) circuit has a gain of approximately 9× and also centers the output range at 0 V. The output electrode isolation switch (EIS) isolates the trap electrode from noise in the amplifier. The values of the components in the circuit are $R_1 = 70$ kΩ, $R_2 = 2$ kΩ, $R_3 = 8$ kΩ, and $C = 200$ fF. (e) The output voltage as a function of the 12-bit digital code sent to the DAC, for each of the 16 electrodes, measured while the trap is installed in the cryostat. There is some variability in the voltage output between electrodes on the order of 1 V and one of the electrodes has significant nonlinearity at 3 V and above. Both of these effects are calibrated *in situ* by using wire bonds to monitor the electrode voltages.

compatibility with high voltages (up to ±10 V), which are necessary to achieve ion-trapping frequencies around 1 MHz for Ca^+ in typical ion traps. The process includes seven metal layers [Fig. 1(c)]. The topmost metal layer (AM), consisting of 4 μm-thick aluminum, is used to define the trap electrode geometry, which is designed to trap ions at a height of 50 μm. The next lower layer (MT) forms a ground plane to isolate the ion from digital and power supply noise in the internal layers of the DAC, to isolate the DAC from pickup due to the large rf voltage on the top of the chip, and to shield the ion from laser-induced effects of carrier generation in the silicon substrate [15]. The remaining metal layers route digital and analog signals between the CMOS transistors defined in the silicon substrate and the serial inputs and control electrodes on the top metal. Since each high-voltage transistor is comparatively large [approximately 800 μm^2, about 2% of the total DAC block area in Fig. 1(b)], we try to use as few as possible. Hence, the first two stages of the circuit, depicted in Fig. 1(d), are formed using only smaller low-voltage CMOS devices. The number of transistors in the high-voltage amplifier (HVAMP) is also minimized, which reduces input impedance and limits the output range to ±8 V instead of the full-scale ±10 V set by the power supplies. Due to the low input impedance, a low-voltage buffer amplifier (BUFAMP) is added between the *R*-2*R* DAC and the high-voltage amplifier stage so that current in the DAC does not leak into the HVAMP.

III. DAC CHARACTERIZATION

In our apparatus, we cool the ion trap to cryogenic temperatures (approximately 4 K), since this has been shown to reduce electric-field noise from the trap surface and also removes the need to bake the vacuum chamber for several days to reach ultrahigh vacuum [17,18]. Cryogenic operation comes with challenges in the integrated circuit performance, since the specifications provided by the CMOS foundry do not characterize behavior at temperatures below 220 K. Thus we sacrifice some of the reproducibility usually afforded by CMOS and must ensure basic operation at our chosen temperature. We first test the DACs on the bench by connecting the trap chip to an interposing circuit board. The test assembly is immersed in liquid nitrogen or helium while we perform a sweep of programming codes and measure the resultant voltage on the output. We find that some DAC channels lose the requisite linearity between programming code and output voltage as they cool to cryogenic temperature, as in Fig. 1(e). For this reason, we add wire bonds to the edge of each electrode so that DAC voltages may be monitored and calibrated while conducting experiments with ions. In future designs, we plan to add an internal multiplexer for routing the voltages to a single diagnostic pad, obviating the need for the extra bonds.

We can correct for dc-voltage error in the DAC output by simply adding an offset to the programmed value. Noise at the output of the high-voltage amplifier, which cannot be calibrated away, presents a more fundamental concern for quantum logic gates based on shared motional states of chains of ions [19]. We characterize the noise of the integrated voltage source in an external test fixture (Fig. 2(b), the green [upper] trace). The extrapolated unfiltered noise at 1 MHz (the dashed green [upper] line), approximately 1 $\mu V/\sqrt{Hz}$, is a few orders of magnitude above state-of-the-art integrated circuits with similar update speeds, which have voltage noise as low as 8–30 $nV/\sqrt{Hz}$, though in a larger footprint [20]. Noise on external voltage sources can be mitigated using commercial low-pass filter arrays with several orders of magnitude of suppression at relevant ion frequencies. On the integrated device, filtering options are limited, since we cannot define arbitrary inductors and capacitors on chip due to the small size of the circuit. Standard passive filtering also permanently reduces the overall bandwidth of the system and places a limit on the speed of ion-transport operations. To solve these problems, we have designed a switchable filter by placing a complementary pair of high-voltage field-effect transistors (FETs) between the output of the amplifier and the trap electrode, shown in the schematic of Fig. 1(d). For clarity, we will refer to this device as the electrode isolation switch (EIS).

The EIS approximates the function of a mechanical relay, in which no current flows and the noise voltage is perfectly attenuated when the EIS is open. More precisely, the EIS is a voltage-variable resistance that is approximately 3.3 kΩ when closed and in the teraohm range when open. On the bench, we measure a noise-power attenuation of up to 6 orders of magnitude after opening the EIS. This measurement is limited by the noise floor of our instruments [see Fig. 2(b)], so the actual isolation may be much higher. Since trap electrodes behave as capacitors with very low leakage, we can quickly manipulate trap voltages with the EIS closed and then effectively disconnect the electrodes from the amplifier noise by opening the EIS, while the trapping voltages are maintained. In more complex designs, the EIS could also be used for switching between multiple integrated voltage sources, which has been shown to be useful in experiments with fast ion transport [21,22].

IV. OPERATION WITH TRAPPED IONS

During experiments with ions, we operate the trap in a cryogenic vacuum apparatus (described in Ref. [14]). The ion trap is thermally anchored to the cold head of a cryostat via a ceramic pin grid array (CPGA) and a custom printed circuit board. An rf signal with an amplitude of 45 V at 45 MHz provides ponderomotive confinement of ions in two (radial) dimensions. The

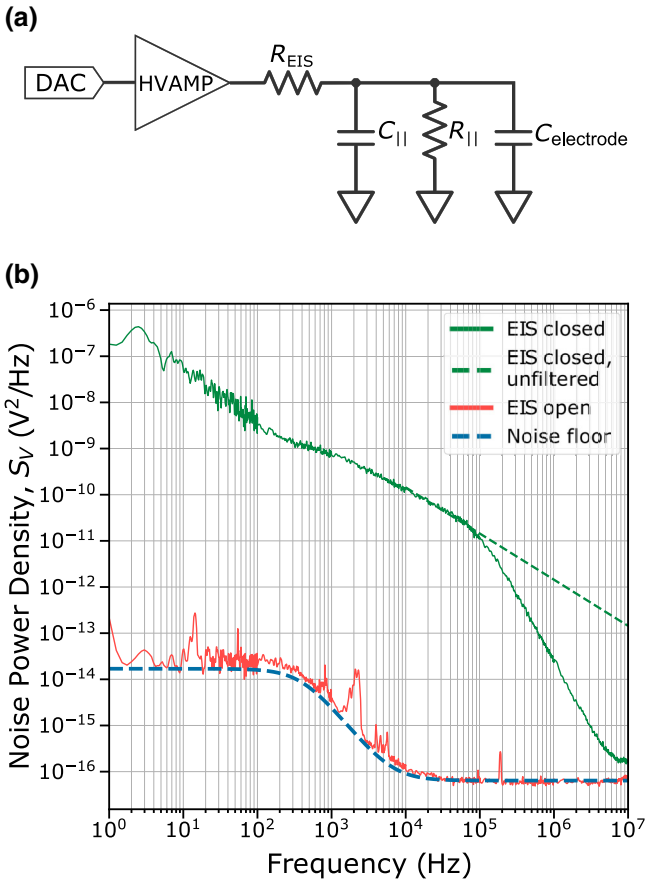

FIG. 2. (a) A simplified schematic of the measurement configuration. The capacitance of the electrode, $C_{electrode}$, set by the trap geometry and the thickness of the internal layers, is approximately 1 pF. The parallel capacitance $C_{||}$ is the sum of any external capacitance added for filtering and any capacitance from signal wires or instruments. The parallel resistance $R_{||}$ is only present when the electrode noise is being measured by the spectrum analyzer. (b) The measured noise power density (the square of the voltage-noise spectral density) on one of the trap electrodes. The voltage-noise spectrum is measured using an HP89410A fast Fourier transform (FFT) analyzer while the trap is immersed in liquid nitrogen ($T = 77$ K). As discussed in the text (see Sec. IV), the temperature of the trap reaches approximately 50 K on the cryostat, so the measured noise at 77 K should be representative of the noise *in situ*. The noise measurement with the EIS open is limited by the noise floor of the spectrum analyzer (the dashed blue [lower] line). The shape of the EIS-open curve is due to the Johnson noise of the 1 MΩ input resistance of the analyzer (130 nV/$\sqrt{\text{Hz}}$) rolling off to the noise floor (8 nV/$\sqrt{\text{Hz}}$) due to a pole created by the analyzer's input resistance ($R_{||} = 1$ MΩ) and parallel input capacitance ($C_{||} =$ 400 pF). This parallel capacitance also causes the measured noise to roll off when the EIS is closed, due to the pole formed at 120 kHz with the finite "on" resistance of the FETs in the EIS ($R_{EIS} = 3.3$ kΩ). The unfiltered noise is extrapolated from data taken at frequencies below this pole, assuming a $1/f$ frequency scaling (the dashed green [upper] line). At the ion's axial frequency of 1.5 MHz, the unfiltered noise from the DACs would be 0.98 μV/$\sqrt{\text{Hz}}$.

dc voltages programmed by the DACs define the trapping potential along the third (axial) direction. Neutral ^{40}Ca atoms are introduced into the region above the trap by accelerating a precooled cloud of atoms in a 2D magneto-optical trap (MOT) with a resonant "push" beam [23]. We trap $^{40}Ca^+$ after two-photon photoionization via excitation at 423 nm and 375 nm. Ions are Doppler cooled with light at 397 nm to about 1 mK. A repumping laser at 866 nm prevents shelving in the long-lived $D_{3/2}$ state (for an illustration of the electronic energy levels of $^{40}Ca^+$, see, e.g., [24]). A stable and narrow laser at 729 nm addresses the quadrupole $S_{1/2} \leftrightarrow D_{5/2}$ transition, which we use to read out the ion's motional state and perform resolved motional-sideband cooling close to the ground state of axial motion (approximately 20 μK) [25].

After applying the relatively high-voltage rf potential to the chip, we confirm that the DACs are still operational by sweeping through all possible programming codes while monitoring the voltage on each electrode via the monitor wire bonds. We find no difference in performance, even when applying rf voltages of up to 80 V. We program the DAC voltages to demonstrate trapping of calcium ions at axial frequencies from 800 kHz up to 1.6 MHz. We also perform rudimentary ion transport over a distance of 80 μm at 2 mm/s by writing a continuous stream of voltages to trap electrodes at a SPI clock speed of 200 kHz. To move ions, we vary the voltages on the electrodes at the center of the trap only; longer transport distances could be achieved with a more detailed simulation of electrode voltages along the entire trap axis. Ion motion is verified by watching ion fluorescence on an electron-multiplying charge-coupled-device (EMCCD) camera while the ion is repeatedly shuttled back and forth by varying the DAC voltages with the EISs closed. Ions are shuttled over hundreds of cycles without loss. When the DAC voltages are fixed, trap lifetimes are similar to those that we observe in standard planar traps controlled by external voltages sources (>30 s without cooling lasers and several hours with Doppler cooling). We finely adjust the internal voltages to trim out stray electric fields, due primarily to charging from photoionization lasers [26,27], in order to eliminate excess micromotion induced by the rf potential [28]. We verify that trap voltages do not drift when the EISs is open by monitoring the trapped ion's position and trapping frequency and find that we can leave the EISs open for several minutes with no noticeable effect on the potential at the ion's location.

Voltage noise on the trap electrodes heats the average motional state, $\bar{n}$, of the ion in the trap potential, reducing the fidelity of quantum logic gates between ion qubits [31,32]. We can quantify this effect using standard techniques for measuring the heating rates of trapped ions [30]. The relationship between the voltage-noise power and the

heating rate of the motional mode, $\dot{\bar{n}}$, is given by

$$\dot{\bar{n}}(\omega_t) = \frac{q^2}{4m\hbar\omega_t}\frac{S_V(\omega_t)}{D_{\text{eff}}^2}, \tag{1}$$

where m and q are the mass and charge of the ion, ω_t is the (angular) trap frequency, S_V is the square of the voltage-noise spectral density, and D_{eff} is a geometric factor determined by the distance from the ion to the trap and the shape of the control electrodes [33]. We calculate the value of D_{eff} using a finite-element electrostatic simulation to determine the electric field at the ion's position for a given voltage applied to the trap electrodes. From measurements of $\dot{\bar{n}}$ with the EISs open and closed, we can determine the voltage noise and thus quantify the isolation of the EISs.

In Fig. 3, we present the average motional state of the ion as a function of delay after resolved-side-band cooling, from which we determine the heating rate. With the EISs closed, we can compare the heating rate and voltage noise, derived via Eq. (1), with the bench measurement in Fig. 2(b), but we must account for additional filtering seen by the ion. The wire bonds that we use to monitor DAC voltages put the trap electrodes in parallel with extra capacitance from a filter board ($C_{||} = 1$ nF). The filter capacitor alone makes a pole at 48 kHz when the switch is closed ($R_{\text{EIS}} = 3.3$ kΩ) and reduces the expected voltage noise from 0.98 $\mu\text{V}/\sqrt{\text{Hz}}$ to 32 $\text{nV}/\sqrt{\text{Hz}}$ at 1.5 MHz. This is in agreement with the voltage noise obtained from the heating rate in Fig. 3, 1090 ± 20 quanta/s $\rightarrow 18.2 \pm 0.2$ $\text{nV}/\sqrt{\text{Hz}}$, within a factor of 2. With the EIS open, the voltage noise is below the noise floor of our spectrum analyzer [Fig. 2(b)], so we expect a heating rate of 180 quanta/s or lower. The measured heating rate with the EISs open, 120 ± 30 quanta/s, is below this limit, but the noise is not reduced by as much as expected, given the high isolation of the EIS at lower frequencies.

To further investigate the limitations to the heating rate with the EISs open, we attach a temperature-sensing diode to the surface of the chip. We find that the temperature of the chip increases from 4 K to just above 50 K when powered on in the CPGA mount. This temperature increase is due to the power dissipation of the chip-integrated DACs (500 mW), the limited cooling power of the cryostat, and the thermal resistance of the CPGA heat sink [34]. At 50 K, we expect anomalous electric-field noise, arising from the surface of the electrode metal, rather than technical noise in the voltage sources, to limit the heating rate to 30–130 quanta/s [18,30], which is in agreement with our measurement in this work. With some modification to the connection between the trap and the cold head, it should be possible to reduce the thermal resistance and achieve a lower temperature in our apparatus. However, in a room-temperature experiment, which can generate much higher cooling power, dissipating the heat of this circuit would not present as much of an engineering challenge.

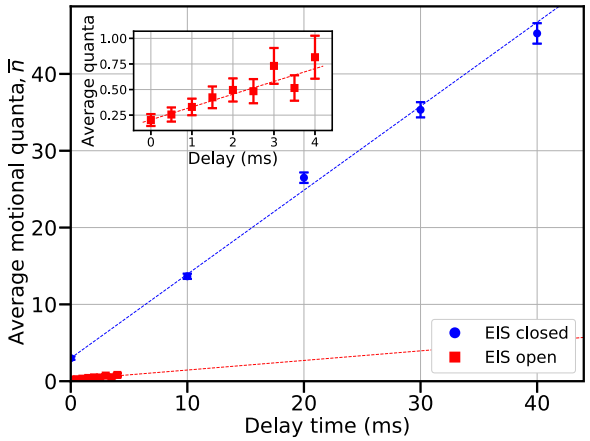

FIG. 3. The axial heating rates of a single $^{40}Ca^{+}$ ion with a trapping frequency of 1.5 MHz. The heating rate measured with the EISs open [closed] is 120 ± 30 quanta/s [1090 ± 20 quanta/s], which corresponds to a voltage noise of 6.0 ± 0.8 $\text{nV}/\sqrt{\text{Hz}}$ [18.2 ± 0.2 $\text{nV}/\sqrt{\text{Hz}}$]. The ion's motional state with the EISs closed is determined by fitting the amplitude of the Rabi oscillation on the $S_{1/2}$ to $D_{5/2}$ transition [29], while the state with the EISs open is determined using the side-band amplitude-ratio technique [30]. These two methods work best in different ranges of motional quanta. To facilitate the plotting of both results on the same scale, the linear fit for the EISs-open data is extended and the experimental data are presented on a smaller scale in an inset.

In applications that do not require dynamical control of voltage sources, the heating rate with the EISs open is the only relevant quantity, since the EISs may be left open after adjusting voltages, with only occasional updates to recharge the electrodes. For experiments with time-dependent trapping potentials, the amount of energy imparted to the ion from voltage noise depends on both the heating rate with the EISs closed and the total time that the EISs is held closed. Noise from the amplifiers can be mitigated by quickly closing and opening the EISs while updating voltages.

V. THE OUTPUT BANDWIDTH AND FILTERING

Finally, we consider the maximum update rate of the voltage sources. Serialization of the input data comes with a speed trade-off, since the trap voltages may only be updated after sending 12 bits to each of the 16 DAC channels. From SPICE ("Simulation Program with Integrated Circuit Emphasis") simulation [35], we determine the highest data rate of the SPI bus to be in the gigahertz range (a maximum voltage update rate of approximately 10 MHz, due to the length of the 192-bit input string); however, in our experiment, we achieve SPI data rates of 50 MHz (a voltage update rate of 250 kHz). Above

this speed, there is a sharp decrease in the fidelity of the digital-to-analog conversion. We presume that this limit comes from reflections in the data lines into the vacuum chamber, since this has previously been a source of error in our experience with this SPI bus design. The use of controlled-impedance lines and terminations at the chip would help to reduce these reflections.

In practice, any voltage updates on the trap electrodes are ultimately limited by the pole at 48 kHz created by the "on" resistance of the EIS ($R_{\mathrm{EIS}} = 3.3\ \mathrm{k}\Omega$) and the capacitance on the filter board ($C_{||} = 1$ nF). The relatively large resistance of the EIS is not fundamental and can be reduced in subsequent design revisions. We could also improve this bandwidth by reducing the parallel-filter capacitance, $C_{||}$, but this requires careful consideration. This capacitor also attenuates the Johnson noise associated with the large (teraohm-range) "off" resistance of the EIS; however, at relevant ion frequencies around 1 MHz, for parallel capacitance of even a few attofarads, this noise source is much smaller than that due to the resistance of the electrode metal and the equivalent series resistance of the capacitor. More significantly, the additional capacitance to ground shunts leakage from the rf electrode onto the control-electrode surfaces by forming a capacitive voltage divider with the effective capacitance between the electrodes [36]. From electrostatic simulation, we find that approximately 10% of the rf voltage, if present on the other trap electrodes, can significantly reduce the depth of the potential well seen by the ion. Acting conservatively, we might choose to keep the rf leakage below 1%. The simulated capacitance between the rf and dc electrodes is between 0.1 and 0.5 pF, so this requires a shunting capacitance of 10–50 pF. With these values, we would expect the bandwidth with the EIS closed to be 1–5 MHz and the isolation with the EIS open to be >160 dB, which should suppress the DAC technical noise to the same level as the Johnson noise due to the resistance of the trap metal, far below the level of electric-field noise due to anomalous heating for traps of this size [30]. On our chip, a 10 pF capacitor could be integrated in the lower metal layers for each of the trap electrodes without increasing the total device area.

VI. CONCLUSION

We demonstrate the operation of an ion trap with electrode-control voltage sources embedded into the trap substrate. With the addition of the electrode isolation switch, these sources approach the noise level of standard voltage sources. The development of these DACs is an important milestone on the way to realizing more complex trapped-ion-system architectures, and our characterization of their performance will be key to assessing their potential for future quantum-information-processing applications.

ACKNOWLEDGEMENTS

We thank Hernan Castro and George Fitch for layout assistance, Peter Murphy, Chris Thoummaraj, and Lee Mailhiot for assistance with chip packaging, and Terry Weir and Gerry Holland for assistance with the bench test setup. This work was sponsored by the Assistant Secretary of Defense for Research and Engineering under Air Force Contract No. FA8721-05-C-0002. The opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

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