Development of electrical characterization techniques for lifetime prediction and understanding defects in InGaAs-based III-V transistors

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Abstract

Combining the advanced complementary metal-oxide-semiconductor (CMOS) technique, faster and highly packaged circuits have continuous developing for more than fifty years. During this period time, engineers focus on higher electrical field and accelerate the degradation to make the highly performance of advanced CMOS devices with better and smaller size than before. At this moment, there are plenty of issues are found which can affect the performances of device. For example, for the new material technique, people prefer use III-V materials to instead of the traditional silicon, and for the traditional CMOS device, the main reliability issue is bias temperature instability (BTI), NBTI for pMOS and PBTI for nMOS. Therefore, this thesis will talk about investigating the NBTI/PBTI and III-V device performance and lifetime prediction issues.

For the whole of thesis, it can be divided by 4 chapters to describe the details, the first chapter would be the introduction of background knowledge and current understanding for how the traditional CMOS device works, and why the new materials could be instead, like III-V device, it shows the advantages and disadvantages for each of them. Moreover, there are some other information would be explained, such as Discharging-based multiple pulse (DMP) method, and hot carrier stress. Those are also topics and directions related this thesis for the further research.

Chapter 2 shows a new measurement method, which called Fast reliability screening technique

method (VSS). It compared the conventional measurement method, which is constant voltage stress (CVS), is faster and only use a single device. And it also combined the measurement details and results to show that method is more efficiently, which includes the benefits and parameters discussion in the different conditions.

Chapter 3 shows a separation traps method of III-V devices with in $In_{0.53}Ga_{0.47}As$ channel. In this chapter, firstly, it shows the introduction of III-V devices for the basic theory and working function, then there are some experiments, which include both AC and DC measurements to show the III-V devices have very fast recovery abilities. Then because the recovery ability, the devices would work well after charging and discharging even after heavily stress and long stress time. Moreover, combine the different discharge voltage levels to get the whole border trap energy distribution. After that, the chapter 3 shows how to separate the traps into two different types, type A and type B. there are experiments results and details to show how it is divided. Then it also mentioned the method can work with different stress time, channel thickness and temperature dependence.

In Chapter 4, the discussion and a summary about previous work has been given, which also points out the future research plans and directions. It includes the lifetime prediction under slow and fast measurements for III-V devices.

List of symbols

Symbol	*Description*	*Unit*
μ_{eff}	Effective mobility	$cm^{-2}/V\text{-}s$
ε_{SiO2}	Dielectric constant of SiO_2	
ε_{Si}	Dielectric constant of Si	
ε_0	Electric permittivity of vacuum	F/cm
ε_{IL}	Dielectric constant of the interfacial layer	
C_{ox}	Oxide capacitance	F
$C_{s,lf}$	Low-frequency substrate capacitance	F
E_f	Fermi level	eV
E_{eff}	Effective surface field in the Si substrate	MV/cm
f	Frequency	Hz
g_d	Drain conductance	S
g_m, G_m	Transconductance	S
I_d	Drain current	A
I_g	Gate current	A
J_g	Gate current density	A/cm^2
L	Mask channel length	µm
L_D	Debye length	cm
N_A	Substrate doping density	cm^{-3}
N_{it}	Interface trap density	cm^{-2}
n_i	Intrinsic carrier concentration in Si substrate	cm^{-3}
N^0	Total density of Si-H bonds	
$N_H(0)$	Free H_0 at the interface	
q	One electron charge	C
Q_{inv}	Inversion charge density	C/cm^2

Table of Contents

1 Introduction

1.1 Background

Combining the Moore's law and reality, for the integrated circuit, the numbers of transistors could increase approximately doubled in every unit device for every two years. It requires high-mobility semiconductors with steady state. At this moment, people using the silicon to produce the wafers has reached to the limited. To keep the high-speed developing for integrated circuit, people could use other materials to instead of silicon, or look for new understandings to use conventional material to improve the performance. Therefore, there are two situations should be mentioned respectively, the first one is the degradation issues which can affect the performance of silicon, and the second one is finding a new material to instead.

First of all, defects of silicon, Bias temperature instability (BTI), which is the major concern about the degradation for silicon semiconductor manufacturing. There are two types of BTIs, negative bias temperature instability for p channel metal oxide semiconductor (PMOS), and positive bias temperature instability for n channel metal oxide semiconductor (NMOS), respectively. The first one, negative bias temperature instability (NBTI), which is a phenomenon happens in positive channel metal oxide semiconductor device. Combining the performance of device, when the device has been applied a negative gate voltage under

different temperature, which the typical temperature range is form 100 degrees to 250 degrees [1]. Then the absolute drain current, Id_sat, and trans-conductance gm will decrease, the absolute off current, Ioff, and threshold voltage, Vth, will increase. Therefore, either big or small value of those parameters could affect the performance of device under different condition. Actually, it keeps struggle people for long time, it is one of the earliest instabilities identified for metal oxide semiconductor field effect transistor. It studied from 1967 by Deal, the original technological motivation for NBTI was about the threshold voltage for p channel NMOS. [2] However, NBTI is not the only important role of electrical stress which involved instability, but also the hot carrier induced instability as well. In addition, NBTI is getting more and more important in recent research, because for the new generation of CMOS process, both electrical field and using temperature increase, and the dielectric constant has been increased. For example, a gate oxide thinner than 3.5 nm, the NBTI could be more important than hot carrier as the limiting mechanism for device performance and lifetime. Also, the hot carrier issue could be difficult for the reliability.

Secondly, new materials to instead of traditional silicon, high-k dielectric, with high mobility and good reliability. For example, III-V materials, InGaAs and Ge for n type and p type MOSFETs respectively. In other words, the high-k materials, it used for consideration to instead of traditional silicon materials, as dielectric materials in the future. As mentioned, the InGaAs channel can regard as a based transistor, the main difference between III-V device and traditional silicon device is its high electrons mobility. Which with extremely high-speed

microwave capabilities. For details, InGaAs, Indium gallium arsenide, which is a kind of alloys made by group 3 and group 5 combination. Indium and gallium come from group 3, and arsenic comes from the periodic table group 5. However, unlike GaAs and InAs, the properties of InGaAs is between GaAs and InAs. Therefore, InGaAs is not the nature material, which similar as silicon, the single crystal InGaAs need electronic and photonic procedures, then varied ratio of material could change its optical and mechanical properties, just like $In_xGa_{1-x}As$, moreover, no matter the ratio is varied, almost InGaAs material use indium phosphide (InP) as its substrate at this moment. Except the substrate, the advance technology can change the thickness of InGaAs channel layer, for example, 15nm, 10nm, 5nm, and even 3nm. Then Al_2O_3 could be the oxide layer as InGaAs surface, as mentioned the varied value mixed, $In_{0.53}Ga_{0.47}As$ is used for matching the lattice constant and mechanical strain. And its optical absorption edge is 0.75eV, which corresponding it has cut-off wavelength at 1.68um at room temperature. Then for the different value of X, in order to match the lattice constant and avoid the mechanical strain, the cut-off wavelength should increase about to 2.6um.

Furthermore, as known one of single crystal material can deposited another single crystal substrate of InGaAs semiconductor when the lattice parameter match together, and there are some options can choose, such as GaAs, InAs and InP. Then the match role is the lattice constant of substrate only allow the single crystal properties should has the limitation variation in a few percent. However, the properties of extended material of InGaAs grown GaAs and InAs are very similar to GaAs and InAs, because it is not allowed the pure substrate grown on

two similar materials. Therefore, substrate should choose InP. Moreover, the InGaAs combination, it has linearly relationship for the lattice parameter with the concentration of InAs, just like figure 1 and 2 shows. In addition, all the value of X in this thesis is 0.53, which mean 1-X is 0.47. and the substrate of InGaAs device is InP.

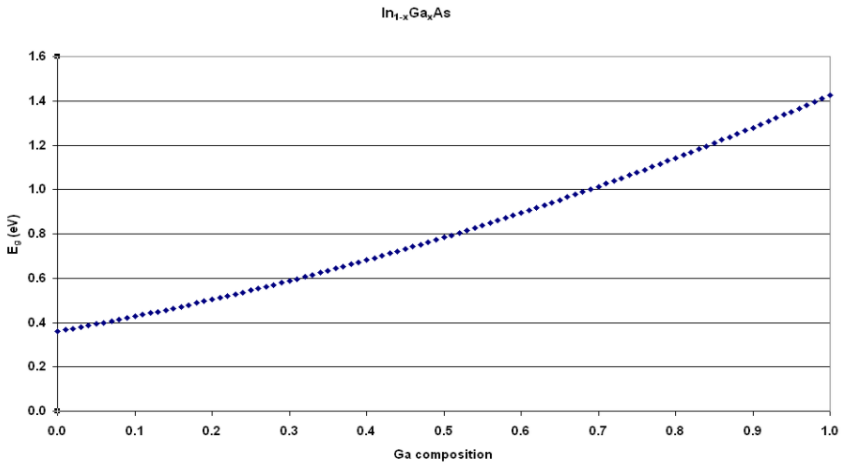

Figure 1. energy gap vs gallium composition for InGaAs, in order to fit the energy gap equal to 0.75 eV, and based on the value in the graph, so the factor of gallium is 0.47, the factor of Indium equal to 0.53.

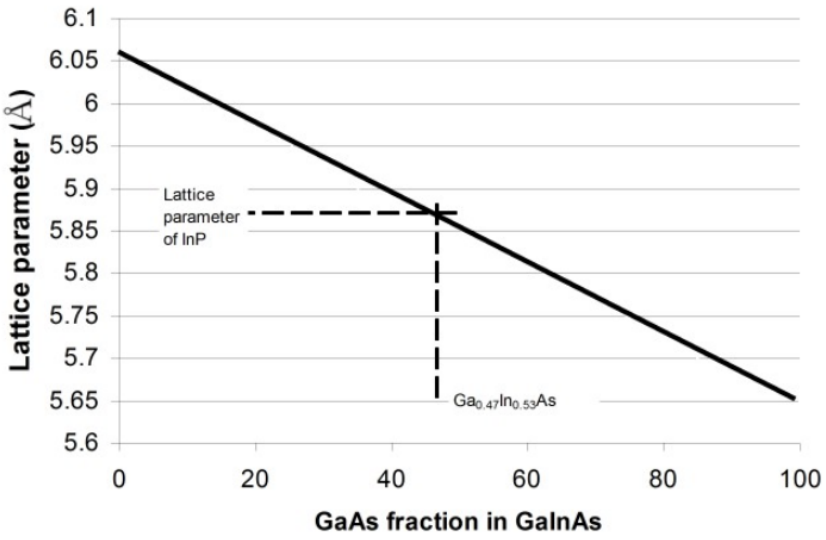

Figure 2. lattice parameter VS GaAs alloy content and use InP as a reference factor.

From figure 2 shows, the lattice parameter of $In_{0.53}Ga_{0.47}As$ is 5.869 Å. Then once the material is confirmed, there are some parameters should be mentioned, the band gap of $In_{0.53}Ga_{0.47}As$ is 0.75 eV at room temperature, the band gap is between Si and Ge, and it determined by the maximum value photoluminescence spectrum. But it changed by temperature as well, as figure 3 shows the comparison performance for both N type and P type under different temperature.

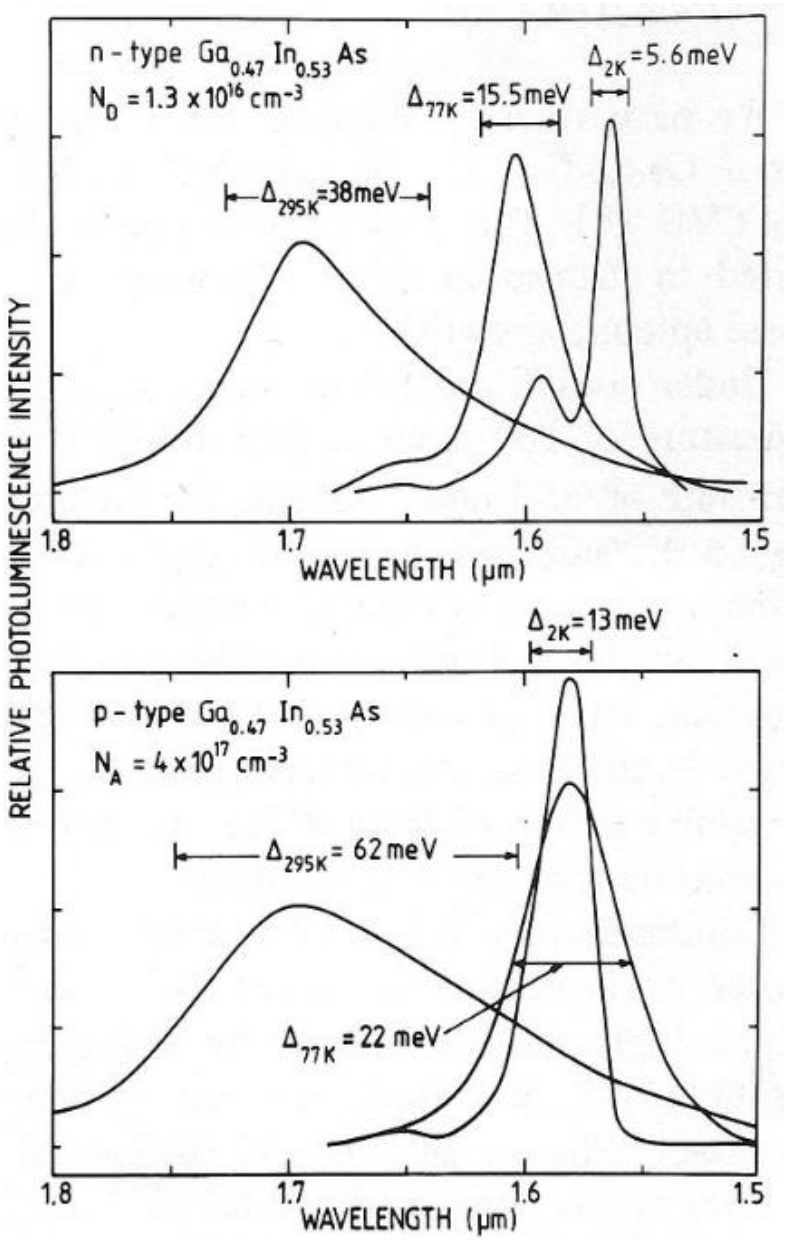

Figure 3. band gap variation for both N and P type under different temperature

Furthermore, the electron effective mass of $In_{0.53}Ga_{0.47}As$ is 0.041, which is the smallest value for all of semiconductor materials with the band gap larger than 0.5 eV, (which is 0.75 eV), and it is determined from the curvature of energy-momentum relationship, that means small number of electron effective mass has high carrier mobility. Because larger curvature translate ratio goes to lower effective mass and larger radius of delocalization. This is also the main reason why choose III-V material to instead of traditional silicon material. Then it is also determined that there are two type of charge carriers, one is light hole and another one is heavy hole. And the effective mass is 0.051 and 0.2 correspond to each other. But the optical and electrical properties for the main factor by the heavy holes, because the density of heavy hole is much large the light hole. Even though it also affects by temperature. Therefore, temperature is a dependence factor could affect the performance of device. It is also detailed discussed during the section 3 in this thesis report.

Toward for the low electron effective mass, the electron mobility is a large number for III-V device. Actually, electron and hole mobilities are the most important factor for design and performance. It matters why people prefer use III-V material to instead of silicon, even though silicon has a better band gap. Combining traditional silicon reach the limitation by Moore's law or reality daily-use, people are more interested the III-V material because of the large number of mobility value. Then the electron mobility of $In_{0.53}Ga_{0.47}As$ is 10x1000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and hole mobility is 250 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature, which is the largest value for all of exist semiconductor materials. By physical reason, the mobility corresponds to the carrier

conductivity, which means, the larger mobility can give the shorter responding time, moreover, it also has smaller resistance and it can improve the efficiency of device, reduce the noise and power consumption. Likewise, the minority carrier diffusion constant is corresponding to the carrier mobility. The hole mobility at 250 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which means the diffusion constant for electrons is 250 $cm^2 \cdot s^{-1}$, and it is larger than Si, Ge, GaAs and InP. Therefore, the ratio of electron to hole mobility result is the largest one for all of others existing semiconductors material.

Therefore, InGaAs as III-V channel material has a lot benefits, people has been used it in daily life widely, for example, photodetectors, lasers, photovoltaics and transistors. In this thesis, the main part talked about is transistor, such as, HEMT device is one of widely using for InGaAs channel, which is high-electron-mobility transistor, it also called heterostructure FET (HFET) or modulation-doped FET (MODFET), because its variation value and different band gaps as the channel to instead of traditional doping region.

Overall, the most important part of background of InGaAs is high mobility, which people use it to instead of silicon to make transistors and continue to follow the Moore's law, or use it to be a high efficiency photovoltaics and photodetectors. And it is widely used in daily life more and more common.

1.2 Discharging-based Multiple Pulse (DMP) method

Discharging based multiple pulse (DMP) is a method, which would use in chapter 3 to separate III-V device traps. It could be regard as charging and discharging two parts. The charging part allows the device has been fully charged by higher gate bias, and discharging part shows the device has been discharged by lower gate bias. As mentioned the higher or lower energy level are determined by the big or small gate voltage applied, which means if the device has been applied a constant voltage for enough time, all the traps border could be totally discharged. This progress also can be regard as trapping or detrapping. Therefore, combining change the discharging level could absorb the whole of energy border levels. So, the whole of DMP method progress could show as figure 4 and 5. And there is a critical point, which is the threshold voltage value. From the beginning, the device has been charging until the traps filling is saturation, then go to the discharge part, the gate bias value of discharge should be getting lower and lower, as figure 4 shows. When the gate bias is lower than the threshold voltage, the waveform should be inverted as figure 5 shows.

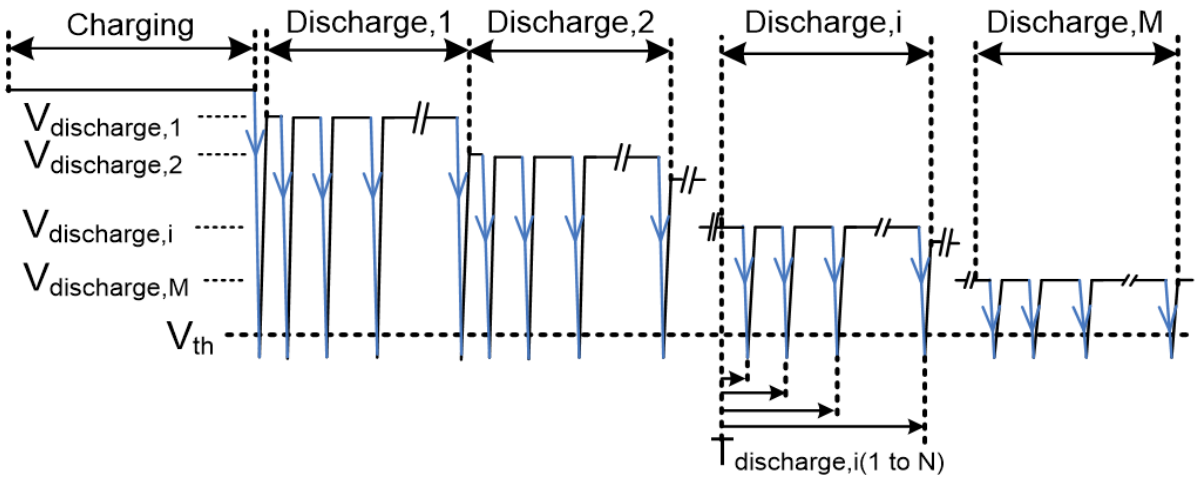

Figure 4. gate bias more than threshold voltage, $V_{discharge}>V_{th}$, the low voltage is applied to discharge traps and the new traping level is absorved, then discharge is interrupted and measure the next level of threshold voltage.

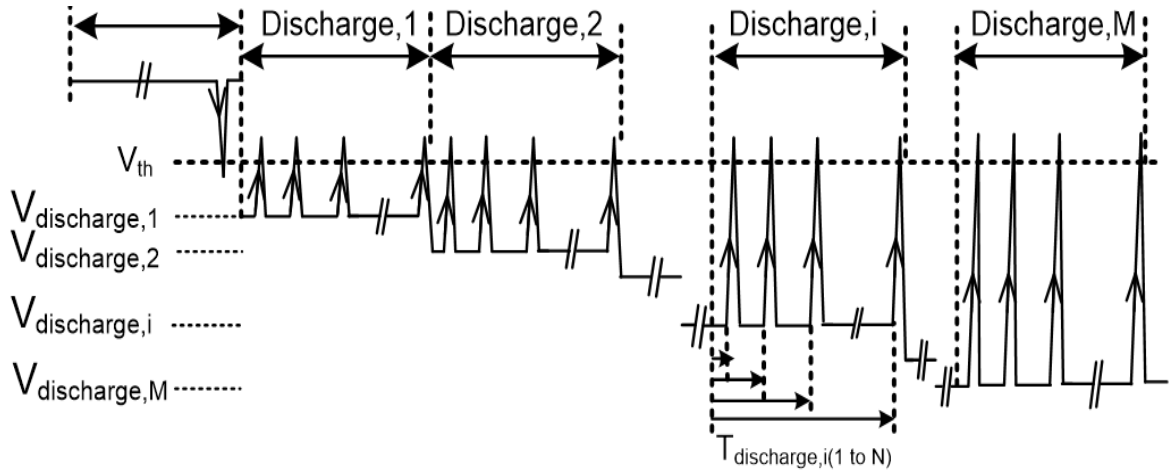

Figure 5. when gate bias less than threshold voltage, $V_{discharge}<Vth$, the pulse measure Vth from pulse edge which is oppsite previous direction.

Then combing figure 4 and figure 5, both below and above threshold voltage can be measured. And figure 6 shows the procedure of discharge based multi-pulse method, there is one condition should be concerned, the threshold voltage get by the end of each discharge level, which also

used as the initial threshold voltage of next discharge level.

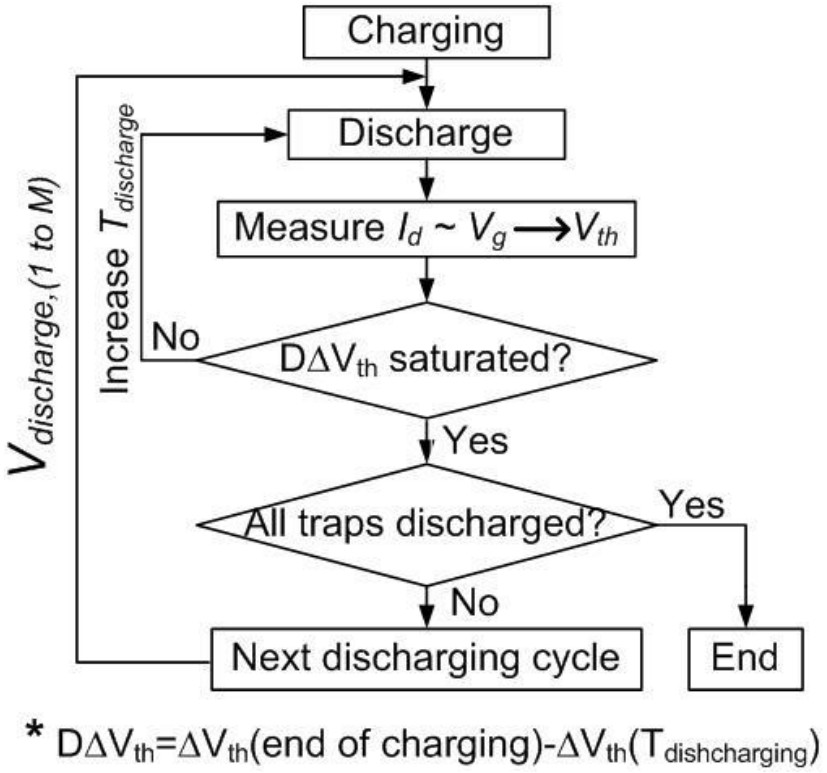

Figure 6. DMP test procedure, following this procedure, the thresold voltage are measured at the end of the previous dischage stage and used for next discharge level.

Overall, the Discharge-based multi-pulse technique (DMP) can be used as trap and detrapped electrons to get whole of energy border of device. It becomes the main test method for separate III-V device traps in chapter 3. And it could take measurements from fresh devices to get traps separation to avoid degradation of device, then using the separation to get lifetime prediction for the further analysis.

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2 Fast reliability screening technique

2.1 Introduction

In order to check the quality of devices, people normally use lifetime to define the devices reliability well or not. Typically, the lifetime of devices in truly life could be more than 10 years, but it is hard for people to take reliability measurement for 10 years, therefore, people normally use critical conditions to instead of working condition to reduce measurement time, which means higher voltage and higher temperature are used to simulate the lifetime result. Moreover, because of device to device variation, it would use several devices to take average, then get the results to show the reliability of deivces. Even though, the traditional method to predict the lifetime could use several days and devices to finish the prediction. Therefore, people need a more efficient method to qualify a device is reliable or not.

As described above, the fast reliability screening technique during processing could become more and more important. So one of biggest challenges is reduce the total measurement time, which is shorten the timing during process of experiment [1, 2]. Moreover, bias temperature instability (BTI) is one of main degradations [3, 4, 5], which can recover very fast, however, there is little degradation caused after recovery, which means there is a delay after recovery when people use the fast method to predict the lifetime. Therefore, besides measurement time,

the slow measurement is also still used around world [6]. In addition, there is an equation shows the power law of degradation by time against voltage [7], which shows the relationship between lifetime and voltage as equation 1.

$$\Delta Vt = A * Vg^{m} * t^{n} \quad \textbf{(equation 1)}$$

A means pre-factor.

m means voltage exponent.

n means time exponent.

Furthermore, it shows the conventional method for accelerating under constant voltage stress (CVS) [8], which is shown figure 7. Also, this constant voltage stress method required the multiple same devices and long measurement time about several days, which means the devices are stressed under same voltage to get value of n, then change to the voltage Vgst for each level of time exponent. After that, combine the equation 1, n and m can be calculated. Then get the stress time against Vgst in figure 8, it fits as the equation 1 as perfect power law.

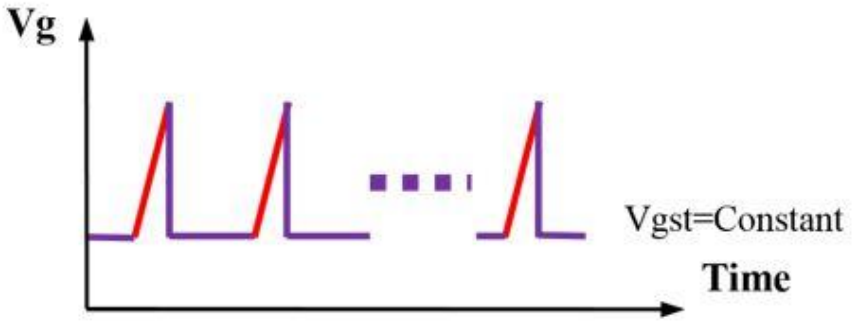

Figure 7. Conventional constant voltage stress (CVS) method, the Vgst schematic waveform vs timing factor, it is performed at certain determined intervals and threshold voltage was measured by constant current at Id= 100 nAxW/L

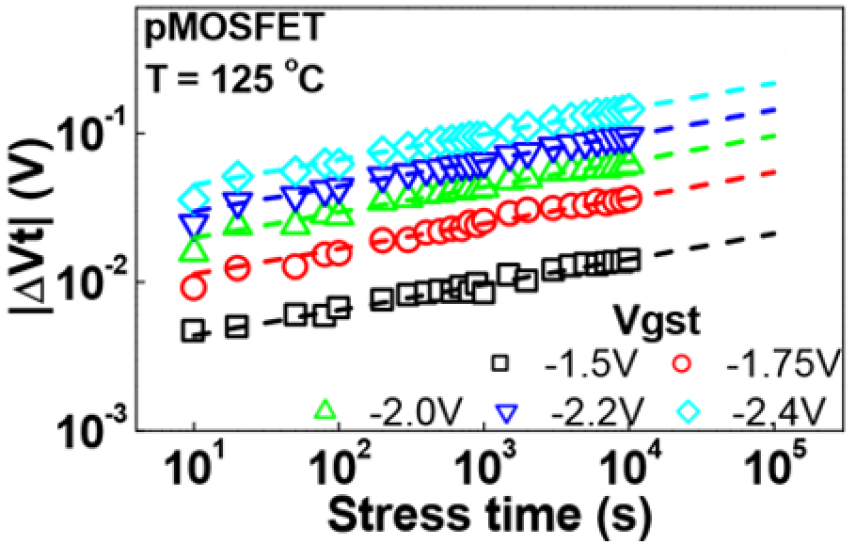

Figure 8. stress time vs Vgst for Conventional voltage stress, the typical measurment resutls shown as dashed lines and fitted with the power law, and CVS method take long time and multiple identical devices are required.

As described above, the constant voltages stress needs complex measurement condition which need both long time and multiple devices. Obviously, it is not obeying the fast screen process development. Then in order to reduce the measurement time, a technique has been proposed which called voltage ramping [9]. It need devices under different voltage to stress with shorten time for predicting lifetime. But also needs multiple device to do the test. And another method for single device also has been processed, but with long measurement time [10]. At the end, the advanced technique solves all of problems. Voltage Step Stress technique, this method only need one device and within shorten time. And it is a wafer-level reliability qualification methodology. It is fast reliability screening for single device measurement and only take two or three hours to get the prediction.

In other words, this technique can save time and commercial equipment to test. Furthermore, this method is working on different processes. Even the most advanced 28nm process. Therefore, the VSS technique could be an effective method for fast reliability screening.

2.2 Measurement details

Firstly, the device used for voltage step stress measurement is the sample with a TiN gate and a channel length and width of 1μm and 10 μm. The gate dielectric stack is HfO_2 with an Al_2O_3 cap layer and the equivalent oxide thickness is 1.45nm. In order to check the applicability of the new method on different technology processes, the advanced 28nm processes with ultra-thin SiO_2 and high-k gate stack are also used.

Then the test procedure of new technique is shown as figure 9. For the details of procedure, compare with conventional method, constant voltage stress. The new method is not using the same voltage for each stress level anymore, and it uses the step to step different stress voltage instead. As figure 9 shows, the voltage could increase by different stress level, but the stress time are equally for each single step. This is also the reason for the name of method comes from, voltage step stress.

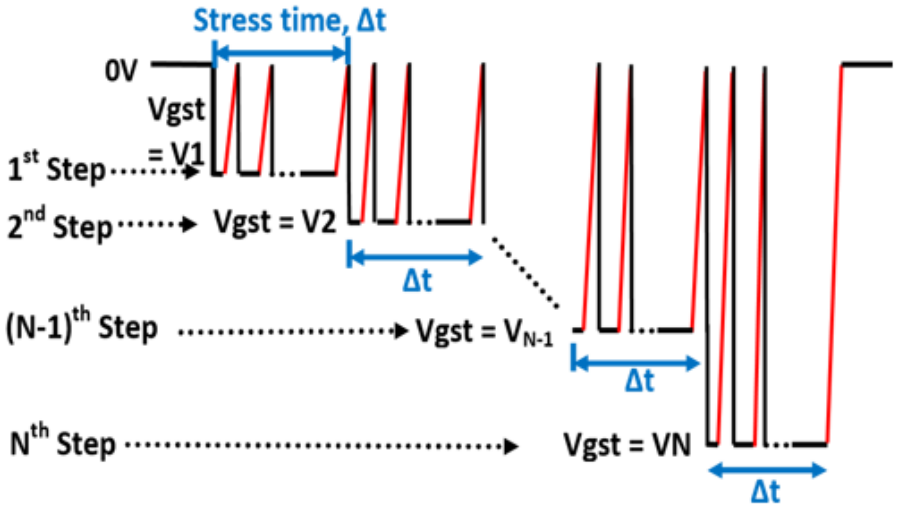

Figure 9. VSS test procedure, Vg waveform of VSS method, |Vgst| increases in steps by a factor of k, k>1, with each step for Δt, stress time. Id-Vg measurements were performed at certain intervals for each step.

Before measurement, it should select a reference Id-Vg curve to compare which Vd equal to -25 mV. And then for each step, the stress time are same and preset by computer program. And during the whole of the measurement, the temperature should under T=125 C, which obey the high temperature to get shorten time to prediction lifetime. For each step, the relationship between stress voltage of current step and next step is constant value, k, which means a factor, k>1. And the relationship can be expressed by equation 2 and table 1 as shown below.

$$\mathbf{Vt = Vt * (K * V) = V (t+1) (next\ step)} \qquad \textbf{(equation 2)}$$

K is a factor, which k>1

Vt is stress voltage of gate

Step	Vgst	Stress time
1	V_1	Δt
2	$V_2 = k*V_1$	Δt
...	...	Δt
N	$V_N = K_{(N-1)}*V_1$	Δt

Table 1. Stress voltage calculation, Vgst, in VSS method, the stress time is applied for each step calculate by equations, |Vgst| increases in steps by a factor of k>1.

2.3 Parameters extraction and discussion

Overall, as equation 1 shows, it can be determined any one of three values. And combine with figure 10, which is ΔVt against stress time in double log scale under NBTI stress (PMOSFET). The condition of figure 10, K=1.1, V1=-1.5V, Temperature=125C, stress time Δt is 1000s and the device is a PMOSFET with HKMG process. And the EOT, width, length of device is 1.45nm, 10μm and 1μm respectively. Combine the result shown as figure 10, it can draw a conclusion, the voltage step stress method fits a very good power law at step 1, which also fits the dash line. In fact, up to step 1, it is total the same as the conventional method, constant voltage stress (CVS). But after step 1, it also fit well for step 2, step 3 and so on, because it applied the increase voltages as a factor k. And the extracted power factor n is 0.165, which comes from slope and the intercept at 1s respectively from the first step. Therefore, from the reference curve of fresh device to stressed device for step 5, the degradation would follow the power law relationship against stress time because of double log scale.

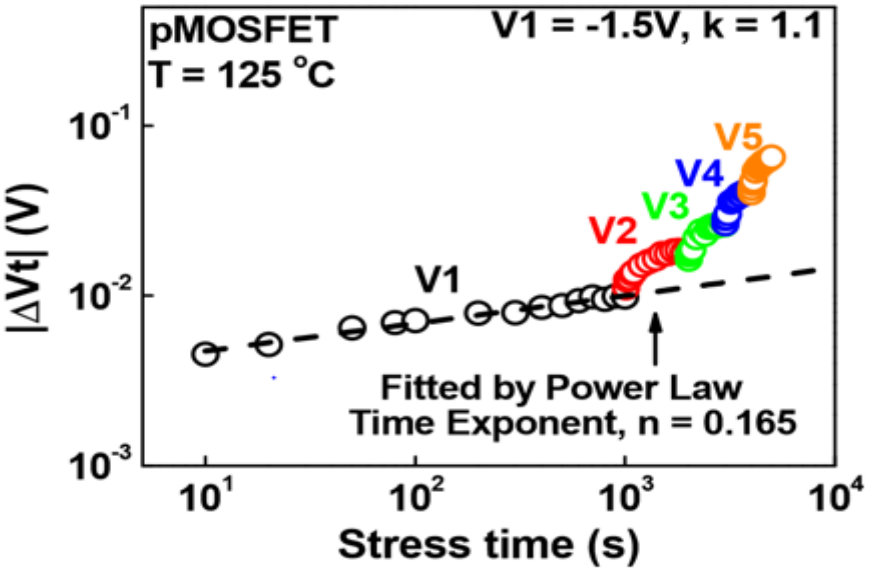

Figure 10. NBTI lifetime prediction, the result get by typical VSS measurement, it devided as 5 steps with a proportional factor, k, and k equal to 1.1. Device is a PMOSFET with HKMG process, which width is 10μm and length is 1μm. and every step measurement takes 1000 seconds.

Furthermore, for the stressed higher voltage under the same stressed time, it can generate more defects which compared with first step. It means the stress time Δt, transfer to effectively stress time (Δteff) at higher voltage is different with the Δteff of lower voltage. And also, the effectively stress time (Δteff) of each different voltage are not the same.

As mentioned before, the stress time of each step could be as same as each level of voltage's stress time. Therefore, calculate the Δteff for each level could let the result fit the power law well. Based on equation 1, for same degradation under $V1*k^{(s-1)}$ for Δt at step #s can achieve by stressing under V1, and it can draw a relationship with formula as shown equation 3.

$$A\,V\cdot 1^{m}\cdot t^{n} = A\,V\cdot [1\cdot k^{(s-1)}]^{m}\cdot \Delta t\_eff^{\,n} \qquad \textbf{(equation 3)}$$

Which can transfer the step #s for Δt to the step #1 with an equivalent time as equation 4.

$$\Delta t\_eff^{\,n} = k^{(m/n)\cdot(s-1)}\cdot \Delta t \qquad \textbf{(equation 4)}$$

In equation 4, in order to get the value of Δteff, it is depending on the value of m, which is voltage exponent. Therefore, figure 11 (a, b, c) are shown the m= 2, 5, 7.7 respectively. When if the value of m is too large than the right one, the transformed curve could below the power law line. And the value of m is too small than the right one, the transformed curve could above the power law line. Only the value of m is in acceptable region, the transformed curve could fit the power law line which continuously from the step #1. Therefore, the correct value of m can be obtained when the best agreement is reached. Based on figure 11, it can be known m=5 is suitable value for m.

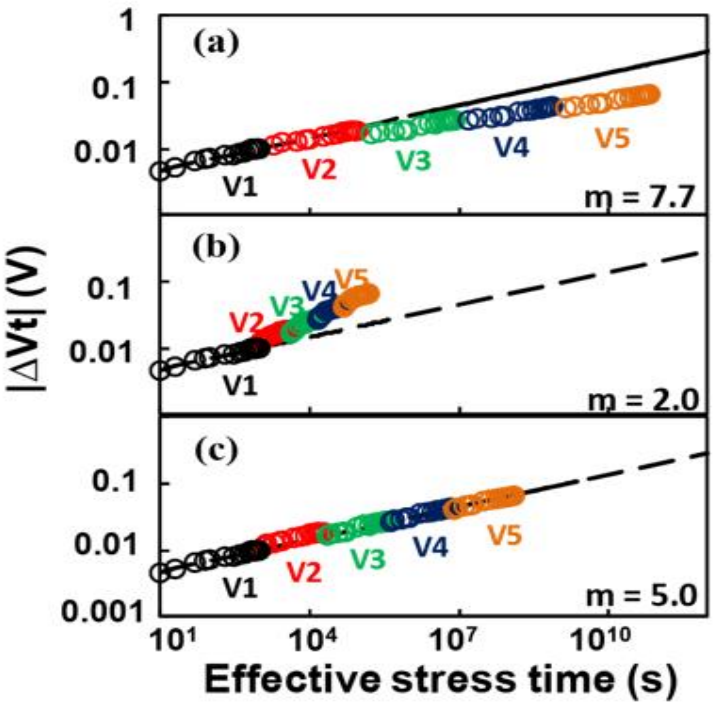

Figure 11. (a), (b) and (c) stand for the value of m are 7.7, 2.0 and 5.0 repectivtily. It shows stress time transformation with different voltage expoent, m.

And combined this method, it can calculate the least square error mathematically, which using two curve and value of m to find the minimum error point, just as figure 12 shown. Then the pre-factor A also can be solved by $A*V1^m$, which was determined in the step #1 using equation 1. And another benefit is this method is not only work under NBTI stress condition, because the devices used is a pMOSFET, but also be used for PBTI stress condition [11]. As mentioned, all points are coming from figure 10 to extract transformed curves for least square error.

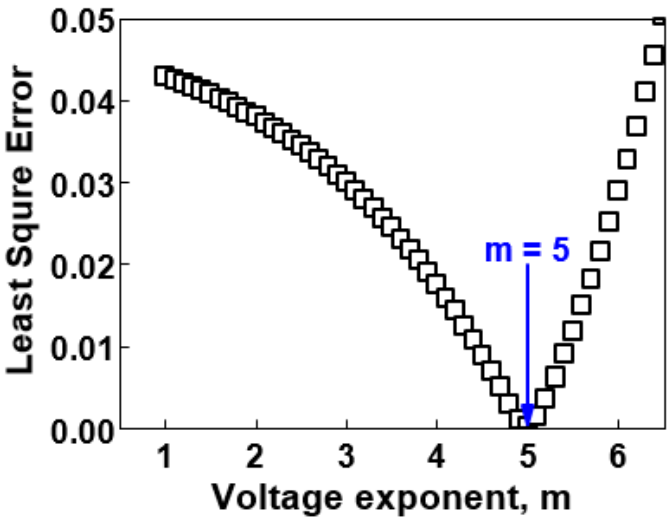

Figure 12. voltage expoent vs least square error, compare with figure 11, it indictes only when voltage expoent vaule, m, equal to 5.0, the least square error is closet to 0, and it follow the prediction and measurment result with dashline in figure 11.

After using this new fast reliability screening technique, even though the measurement itself only use single device and within shorten time. But at least, it predicted result should the same as truly slow measurement result, and the conventional method can confirm the result is right or wrong. Therefore, there are two things need to confirm. The first one is that the calualtion value by using voltage step stress method fits or not with truly measurement values. Then the

second one is using the constant voltage stress method to do a comparison for prediction lifetime of device. So figure 13 [3] and figure 14 [3] show measurement results after stress bias and lifetime respectively. So, it can draw conclusions for that prediction of voltage step stress technique fits the truly measurement results under different stress biases. And both constant voltage stress and voltage step stress technique are in good agreement for lifetime prediction. In figure 13 [3], the lines stand for calculation using parameters extracted from voltage step stress technique and the points stand for measured data by using slow measurement.

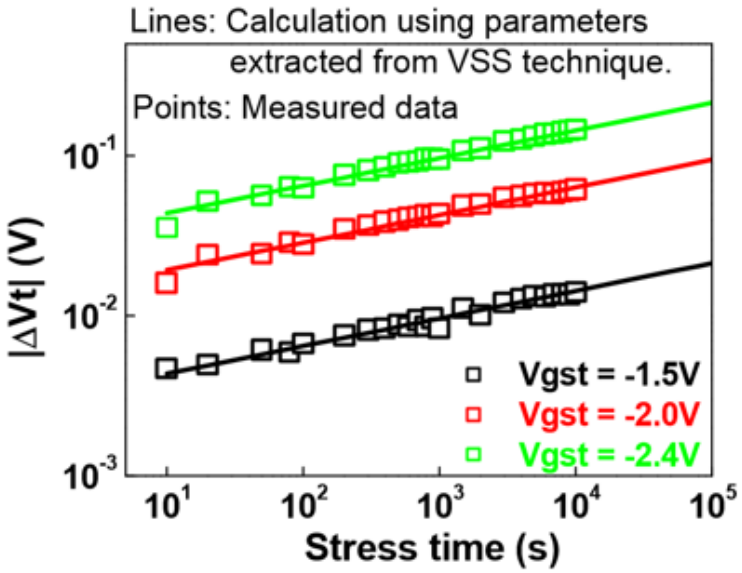

Figure 13. summary of comparison bewteen measured and calculation data, using ΔVt to compare continvental voltage stress and votlage step stress, and it has a good argreement under different Vgst.

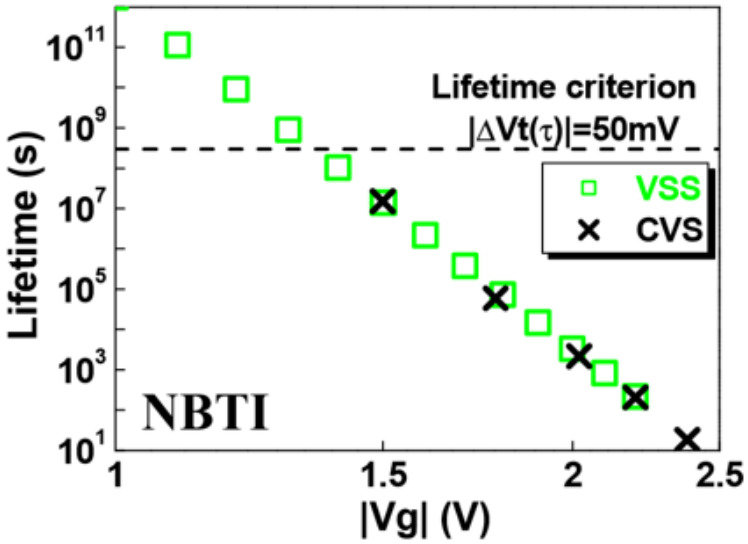

Figure 14. summary of lifetime comparison by using continvental voltage stress ('X') and votlage step stress ('□') methods.

The data of both figure 13 [3] and figure 14 [3], the devices are HKMG process. And EOT, width, length are 1.45nm, 10μm and 1μm respectively. And figure 14 [3] shows the both two techniques are agree well for lifetime prediction. 'X' stands for the NBTI of conventional voltage stress technique. And '□' stands for the NBTI voltage step stress.

After confirmed the voltage step stress technique can work under NBTI for HKMG process with V1=-1.5V, k=1.1. And there are four things can adjust the result for voltage step stress technique. Stress time (Δt), start voltage (V1), factor, the value (k) greater than 1, and time exponent (n). Based on those adjustable parameters, if voltage step stress technique stable and useful for other models, the prediction lifetime would not affect by those parameters. But if the results are changed, which means the fast reliability screening technique is not reliable. Therefore, table 2 [3] lists those four adjustable parameters and figure 15 [3] show that those

parameters changed randomly to check the stability of voltage step stress technique. And calculate the lifetime under Vg=-1.1V.

	#1	#2	#3	#4
Δt	1ks	5ks	2ks	1ks
V1	-1.5	-1.6	-1.7	-1.6
k	1.1	1.1	1.1	1.2
N	6	4	4	3

Table 2. a group of measurement by using VSS method, only change different sets of parameters, the calculated lifetime under Vg = -1.1V is shown in Fig15.

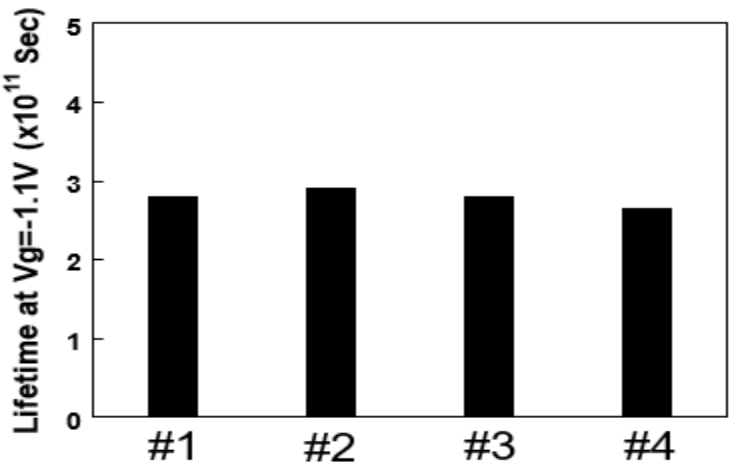

Figure 15. The extracted lifetime under Vg=-1.1V using VSS technique with the 4 set of parameters listed in Table 2.

As figure 15 [3] shows the new fast reliability screening technique is very stable under NBTI with PMOSFET and HKMG process because there is almost no change in the prediction of lifetime. Therefore, the next step is checking the PBTI with NMOSFET and different device

processes. As similar method with NBTI and PBTI checking should do the measurements under high temperature, 125 C, to compare conventional voltage stress with voltage step stress technique performances. Therefore, figure 16 (a-b) [3] show those results respectively.

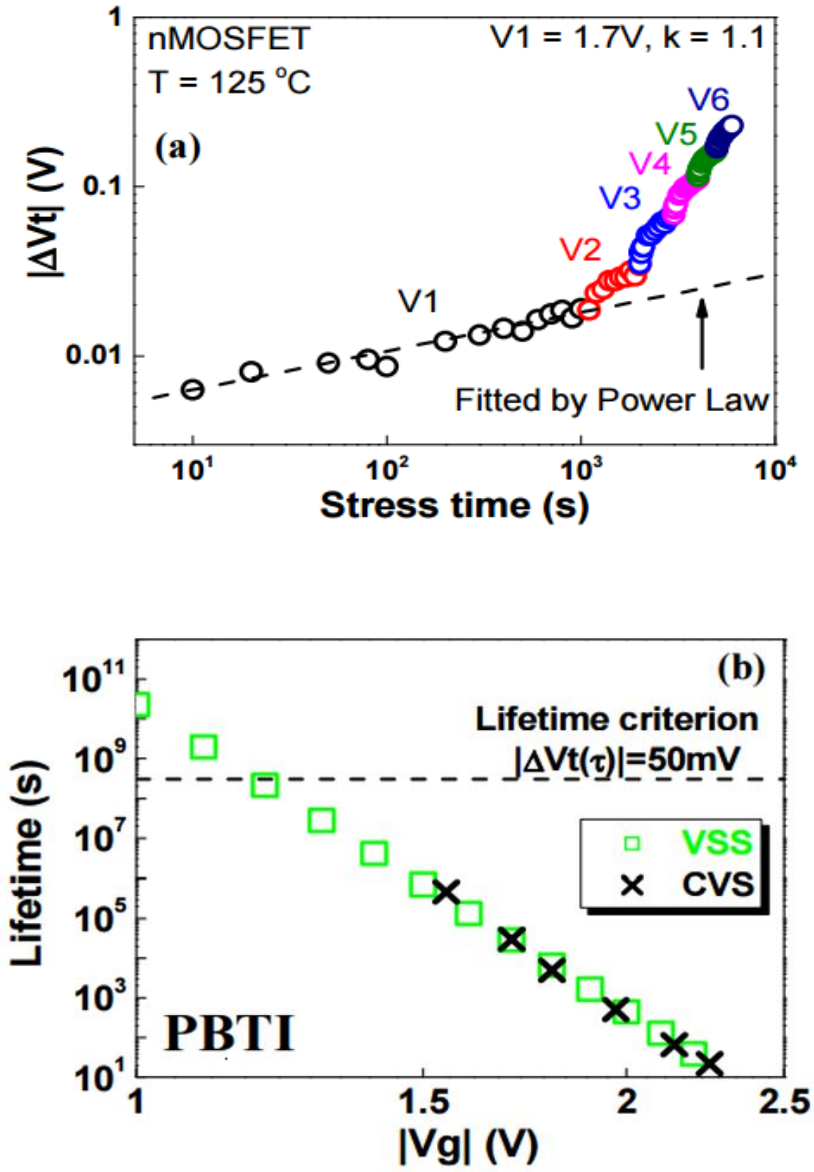

Figure 16. both (a) and (b) present the VSS technique with PBTI stress mode. Figure 16(b) PBTI lifetime prediction comparison between VSS technique (‘’) and conventional CVS (‘X’) method. The samples are with HKMG process. The EOT is 1.45nm.

As figure 16 (a-b) [3] show voltage step stress technique also works for PPBT with NMOSFET devices. It is a clear evidence in figure 16 (b) [3], which shows the both two techniques are agree well for lifetime prediction. ‘X’ stands for the PBTI of conventional voltage stress technique. And ‘□’ stands for the PBTI voltage step stress.

Moreover, for different processes, it also need to check the applicability for new technique. Therefore, using different processes samples to check out if it works or not. Previous measurements are using HKMG process devices. So it could try on other types of gate stacks. There are two of samples fabricated with the advanced 28nm processes. The first one is ultra-thin SiON and another one is high-k gate stack.

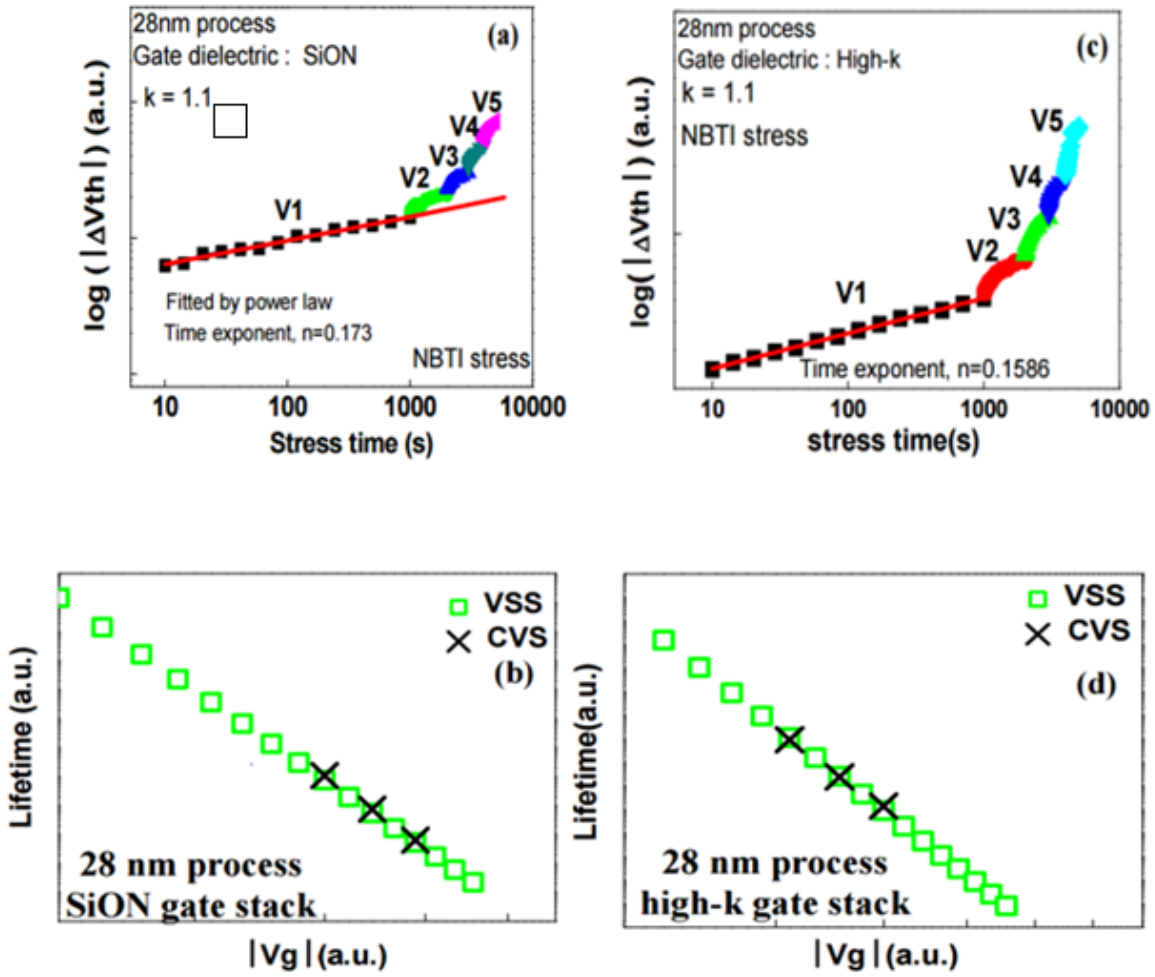

Figure 17. (a) [3] and figure 17 (c) [3] show typical measurements result using by voltage step stress technique. Then figure 17 (b) [3] and figure 17 (d) [3] show the comparison between voltage step stress technique and constant voltage stress technique. And 'X' stands for the PBTI of conventional voltage stress technique. '□' stands for the PBTI voltage step stress. As results shown, there is a perfect agreement for those two techniques under both ultra-thin SiON and high-k gate stack, which means voltage step stress technique is reliability one which can apply on different processes and gate stacks for both NBIT and PBTI.

2.4 Conclusion

After considering all the situations could affect the results, the new fast reliability screening technique, voltage step stress is robust and applicable, which can get lifetime prediction under different processes and materials (both NBTI and PBTI). And the benefits of technique itself could save time and commercial equipment to test. It only required within two hours and single device. Therefore, it could be an effective tool for fast process screening for lifetime prediction.

2.5 Reference

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3 Separate traps of III-V MOSFETs with in $In_{0.53}Ga_{0.47}As$ channel

3.1 Introduction

Comparison with regular silicon devices and III-V devices, the main difference is mobility. Combine the Moore's law, the size of devices is getting smaller and smaller, but the speed of device is getting faster and faster. Thus, it requires high mobility and reliability. InGaAs is one of III-V group material which is a strong candidate for n-channel. Specially, it can provide the high densities. However, at this moment, people do not know the properties of InGaAs devices very well. In this section, it would explain the theory of devices how it works and use measurements to proof it.

Firstly, the samples are made by $In_{0.53}Ga_{0.47}As$ channel and Al_2O_3 gate oxide and investigated using the discharging-based energy profiling technique. Those devices have border traps in nMOSFETs. In this section, those traps are divided into two different type of traps, type A and type B. the reason of that the performance of devices can be analyzed by trap energy distribution between charge and discharge under different gate biases. Then depend on energy distributions could identify what type of traps they are.

Moreover, the measurement results are depended by different temperature and charging time. And because III-V devices can fully recovery in shorter time than regular silicon devices, so about discharging time, it is not a dependence factor which could affect results. Also the variation of channel thickness performance could include in this chapter, which means after identifying these different types of traps can improve that people get better understanding of III-V devices and keep long-term reliability modelling and lifetime projection.

For the background of InGaAs device samples come from, since ITRS has predicted a 0.72V power supply on transistors in high performance logic applications in 2018 [1]. Therefore, people would focus on using high mobility channel materials such as InGaAs for n type MOSFETs and Ge for p type MOSFETs. And the development of InGaAs devices has huge progresses recently. In addition, high intrinsic electron mobility of 3000 $cm^2/V{\cdot}s$ has been demonstrated by several groups [2, 3]. With Al_2O_3 as gate oxide, a low interface state density (e.g. $2x10^{11}$ $cm^{-2}eV^{-1}$ [4]) and a subthreshold swing of 75mV/dec [2] was obtained. However, intolerable number of border traps are found in the oxide, resulting in I-V hysteresis and C-V frequency dispersion [5]. Which means those traps for InGaAs materials of PBTI could affect the lifetime of device to an unacceptable level. Based on situations which described above, the III-V MOSFETs with in $In_{0.53}Ga_{0.47}As$ channel has been processed, and this technique are used for all of devices which variable different thickness dependence used in this chapter.

Furthermore, people normally use the border traps to investigate by using multi-frequency charge pumping (CP) technique [7]. The device with InGaAs channel is different with bulk-Si FETs, it only has three terminals and grows on insulating substrate. Therefore, the multi-frequency charge pumping technique cannot applied in InGaAs channel materials easily. So, there are plenty of methods have tried on InGaAs channel process. Such as based on noise [8, 9], pulsed Id-Vg measurements [10] and spectroscopy by charge injection and sensing (TSCIS) technique [11]. For the details, the noise-related methods extract trap information from the fluctuation of drain current due to trapping/de-trapping-induced variations in carrier number or mobility [8]. And the pulsed Id-Vg method investigates the drain current response to gate pulses. The Trap Spectroscopy by Charge Injection and Sensing (TSCIS) technique [11], it is proposed to extract the energy distribution of border traps based on charging under the assumption. In another word, the charging of TSCIS technique could through flexible tunneling, which does not apply to III-V devices. Based on those technique cannot use on InGaAs channel device, the process problem could become more urgent. Because the III-V devices are dependence on the charging time and temperature as mention before, so the extraction method should extract the border traps under different charging gate voltage at different levels, which means the method itself could identify the different traps for different origins. After comparison, there is a suitable technique which called discharging-based energy profile technique [12]. Which can analysis the trap energy distribution and identify different types of border traps, and there are only two types of border traps, type A and type B. it would help people to understanding the trap of InGaAs channel material specifically.

Moreover, based on the structure of device, the border traps and interface states can be traced as figure 18 (a). The interface traps are defect at oxide layer interface and the effective density of border traps depends on the bias condition [27]. And figure 18 (b) shows the energy band could change if apply positive voltage which used in the measurement process for InGaAs channel. It shows the difference between border traps and interface states. And the further analysis in this chapter used for getting total traps for InGaAs channel device and how to separate the different types of traps.

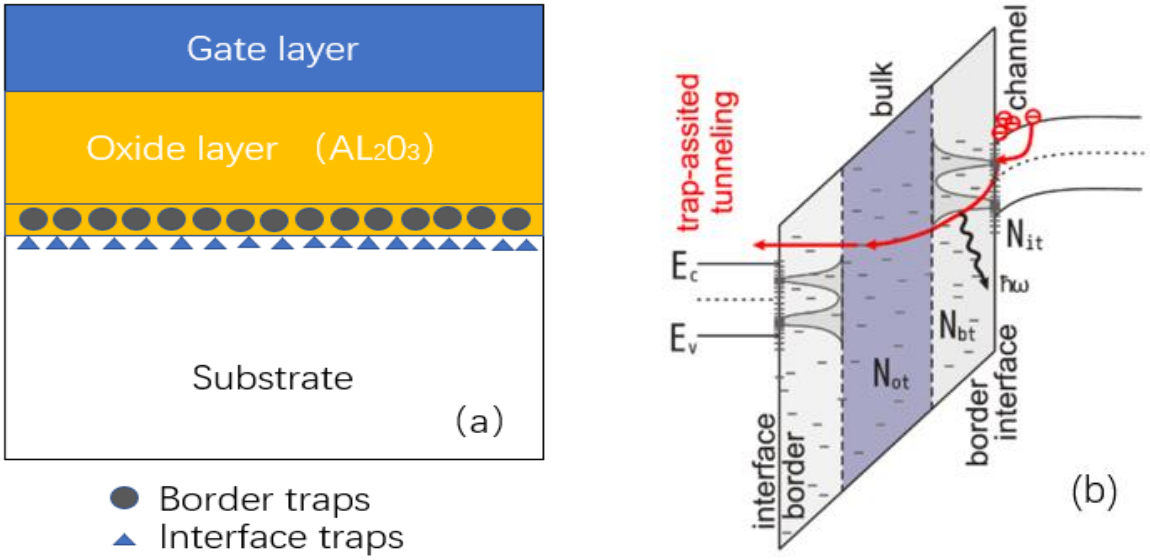

Figure 18. (a) indicates the structure of device to determine difference of location of border traps and interface traps. (b) indicates the border, interface and oxide bulk traps energy band diagram, the interface states with the corresponding concentration N_{it} depend on the coordinate along the interface [28]. and trap-assisted tunneling is present by red arrows [29]. The gate oxide leakage has been confirmed that not only include the stress-induced leakage current in degraded dielectric layer, but also for tunneling transport through the oxide and SiO2/high-k gate stacks [30].

In this chapter, all of measurement details of test procedure would be introduced, and technique of energy distributions extraction are also explained. After that, using the measurement result to analysis border traps and interface states, then getting two different types traps separately. Based on those two different types traps, the thickness, charging time and temperature dependence would discussed respectively.

3.2 Device and experiment details

As described before, the devices used in this chapter get from IMEC company, it made by InGaAs channel material, n type MOSFET, III-V device. It has 3nm, 5nm, 10nm for different thickness variation. And the device received a $(NH_4)_2S$ treatment prior to the gate oxide deposition. The gate oxide is a 10 nm ALD Al_2O_3 with a TMA initial surface cleaning. This ALD process reduces Ga and As oxidation on InGaAs channel surface and thus yields a good quality interface. Then the devices have been annealing before production. Forming gas anneal condition is at 370 C was performed on the finished devices. There is the specific information of device below. Figure 19 (a) [1] shows the fabricated device structure, and figure 19 (b) [1] shows TEM micrograph of the gate stack on the 15nm channel device showing no interlayers between Al_2O_3 and InGaAs surface.

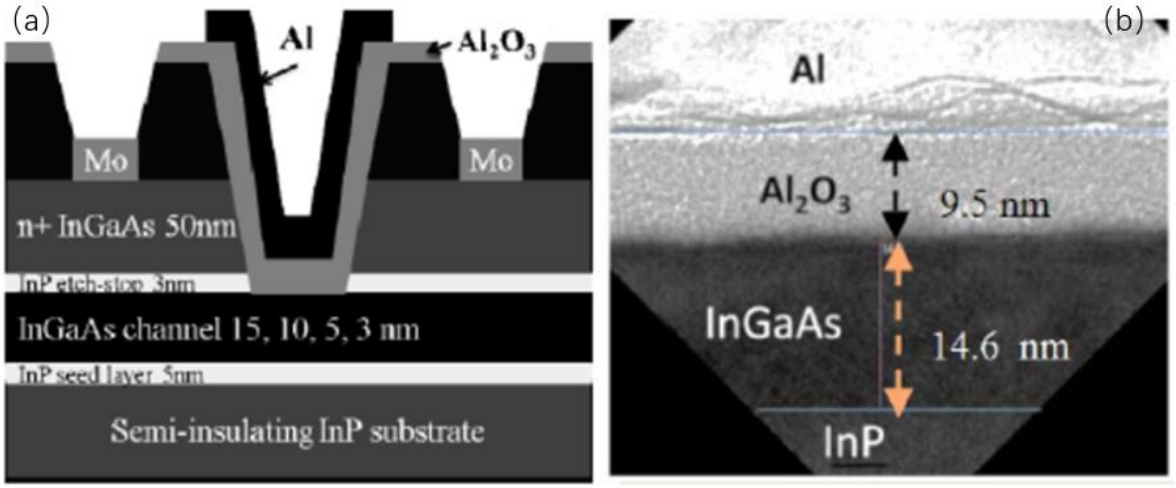

Figure 19. (a) The fabricated device structures. (b) TEM micrograph of the gate stack on the 15nm channel device showing no interlayers between Al_2O_3 and InGaAs surface.

In addition, as mentioned above, the method of investigating border traps is discharging-based energy profiling technique. And the waveform of measurement procedure is shown by figure 20 [1]. For details, gate voltage applied on device would raise to a certain charging level Vg_charging for pre-specified time to fill all the traps to make sure the device under fresh condition. Then gate voltage lower down to Vg_dicharging1, and the degradation would be recorded and used for against discharge time until the voltage become too small to extract traps. For example, less than 2 mV. After Vg_charging transferred to Vg_discharging1, the voltage would lower down the value again to Vg_discharging2 with the same procedure. In order to get the whole trap energy location and distribution, the process of reducing voltage should contain both within and beyond the InGaAs band gap. Which means Vg_discharging should smaller than threshold voltage (Vth). After that, the direction of pulse need to be reversed.

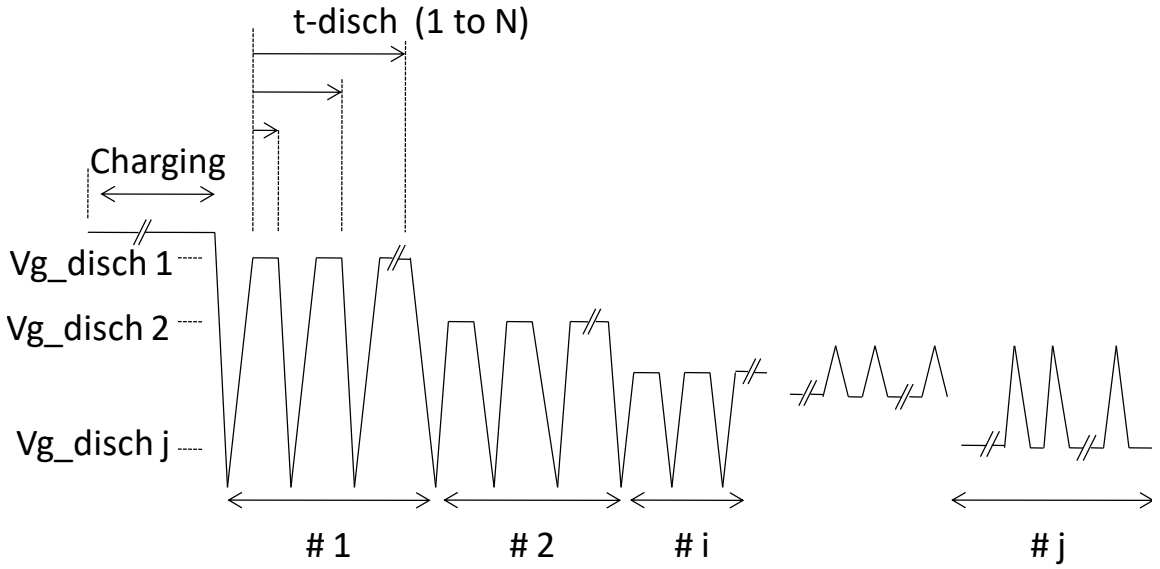

Figure 20. process for DMP method

In addition, during the Id-Vg measurements with a speed of 3μs [13, 14] and Vth is evaluated using constant current method with the level around fresh Vth0 [15]. Here it should identify which pulse edge need to extract threshold voltage because each pulse has two edges, it called ON-to-OFF and OFF-to-ON. And each of those two could lead the results are different as figure 21 (b) shows, there is only three terminals, gate, source, drain as mentioned before. And before experiment, based on layout of device as figure 21 (a) shows, it should pick a good condition device which need to check the reliability of device-to-device variation because this is new technique with new material. It also would lead the results to another way, as figure 21 (c).

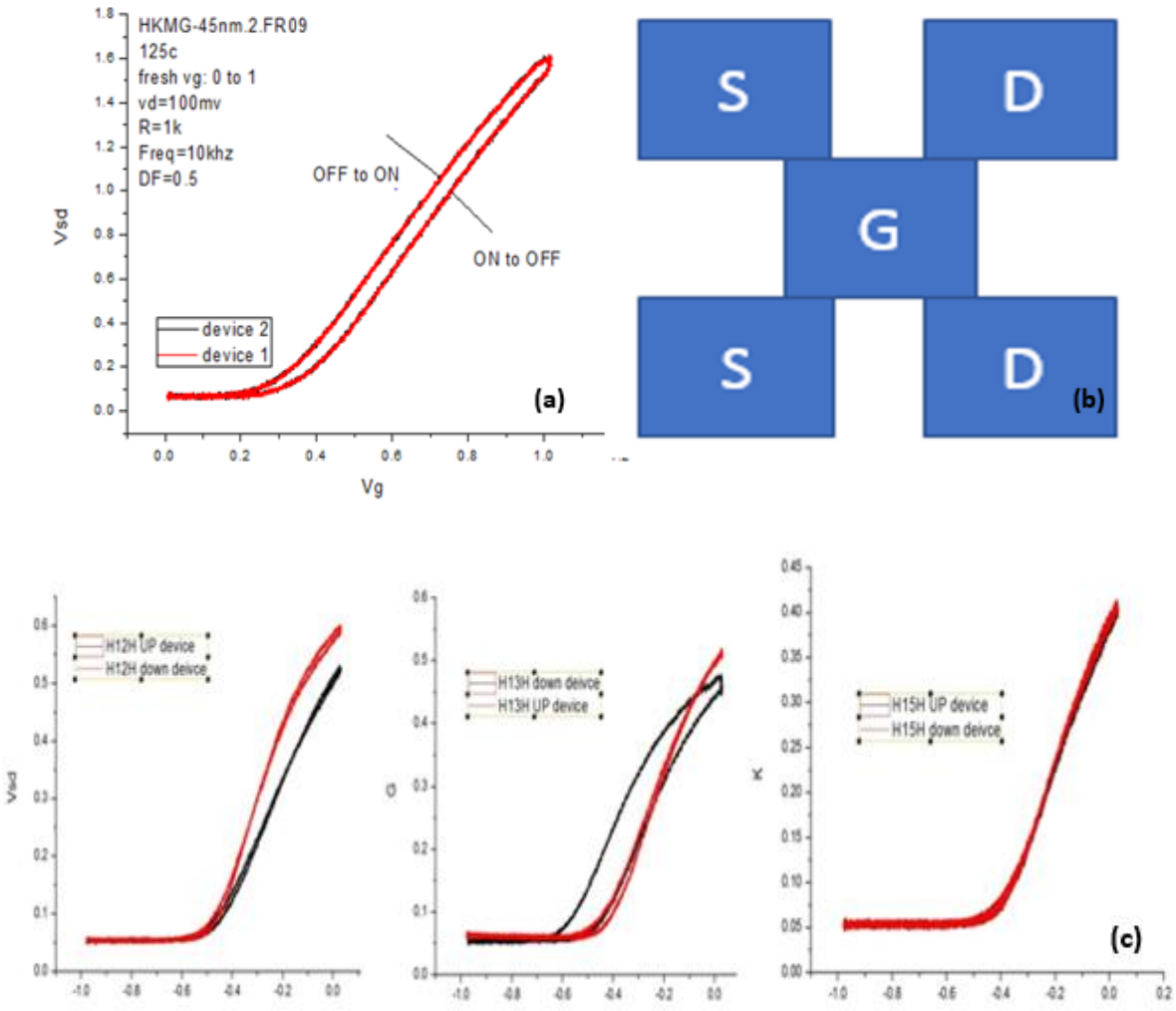

Figure 21. (a) presents two edge of the measurement pulse, measurement speed is 3μs, and it need be determined clear which edge is used in the measurement. Figure 21(b) shows the layout of device, two sources, two drain and one gate in same pad. and figure 21(c) is trying to avoid the device to device variation issues. Just make sure the device is working well and using it.

In addition, in whole procedure of experiment, it repeats charging and discharging all the time because InGaAs channel device can fully recovery in shorten time, as figure 22 (a) shows. Even after long time stress, the devices itself still can recovery back, as figure 22 (b) shows, in figure 22 (b), there are three different thickness, 3 nm, 5 nm, 10 nm to proof this conclusion. All of

measurement included both ON-to-OFF and OFF-to-ON states. And figure 22 (c) shows the experiment procedure.

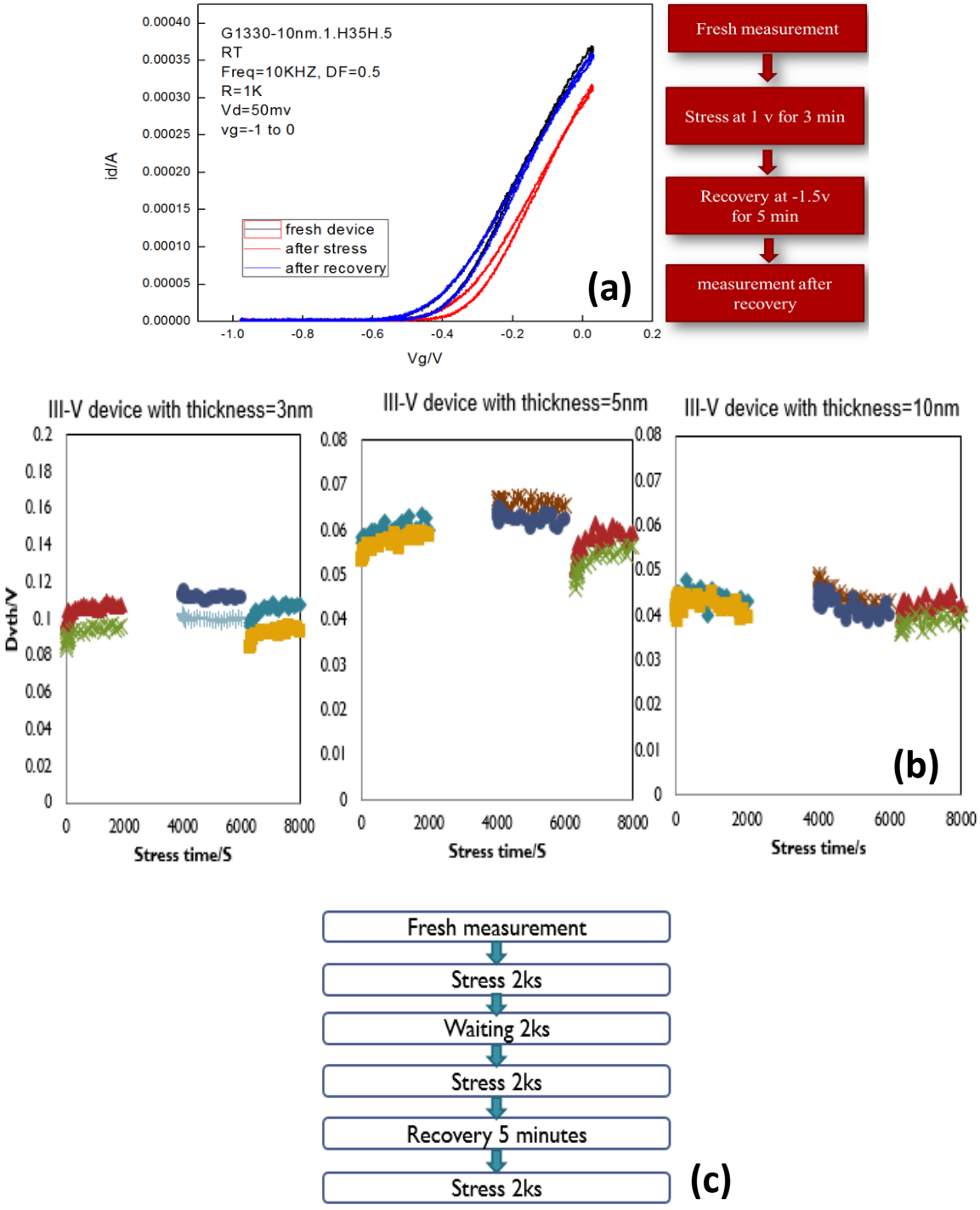

Figure 22. (a) shows the comfirmation of III-V device has good revoery ability different device. (b) shows since the thickness is a vary factor to affect the perfromance, so thickness with long time stress and recovery ability also need confirm. (c) test produrce for stress and recovery.

Moreover, after confirming all the external situations could affect experiment results, a typical measurement results are shown as figure 23 [1]. Again, InGaAs channel device can recovery in shorten time, which is also the reason why the pulse divided in two different edges, ON-to-OFF and OFF-to-ON. Actually, for silicon devices, there is no need to do that sort of thing because both of two edges of pulse can be regarded as equally to each other. As preparation of experiment knows, the discharge time of InGaAs devices could be with 1 s, so for the programming of test is set for 1 s for each of Vg_discharging step.

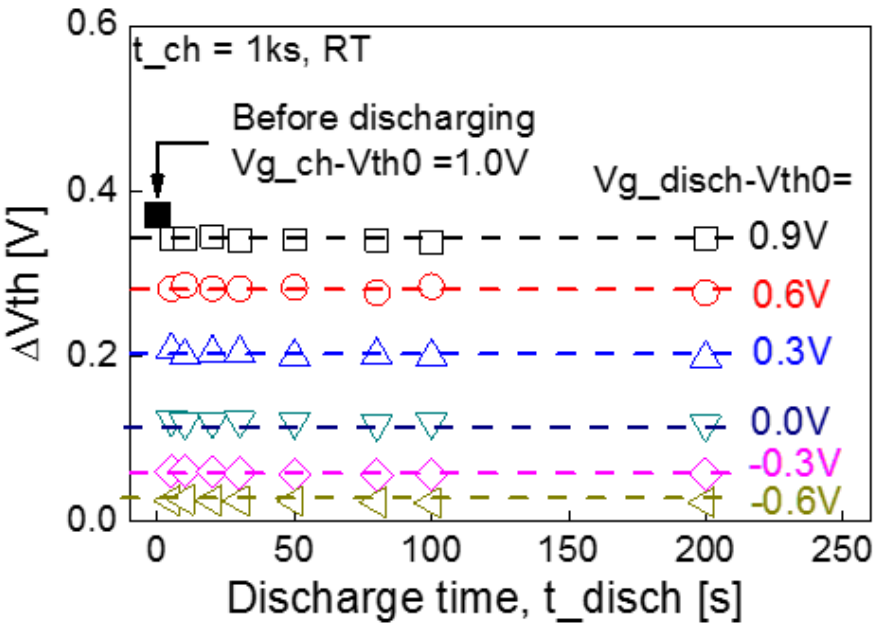

Figure 23. Typical results for discharging under different Vg_disch. The device was charged at Vg_ch – Vth0 = 1.0 V under room temperature for 1ks. The total threshold voltage shift before discharge is given by the symbol "■". The dash lines are guides to the eye.

3.3 Border traps identification and separation traps for III-V

In order to obtain the whole border trap energy distribution, the ΔVth after discharging which the last point of figure 23 [1] for each dotted line, it converted to the effective charge density, ΔNot. And using ΔNot against Vg_discharging as figure 24 (a) [1]. Which means Energy profiling extraction ΔNt in (a) is the charged electron traps after completing discharging at each Vg_disch. Then convert Vg=Vg_discharging to corresponding energy level, which means Ef against Ec of the InGaAs at the surface, Ef-Ec, as shown figure 24 (b) [1]. For details, Ec is the conduction band of InGaAs at the interface and the shaded area denotes the charged electron traps.

Combining 1D Schrödinger-Poisson solver [16], the relationship between Vg and Ef can express by figure 24 (c) [1] with quantum effect consideration together. Here Vg−Vth and Vth = Vth0+Vth shows varies during discharging. So figure 24 (c) [1] shows Ef-Ev against Vg-Vth form 1 D Poisson simulator [15]. Furthermore, the values of x-axis of figure 24 (c) [1] and the values of y-axis of figure 24(a) [1], ΔNot against Ef-Ec, which can extract the border traps energy distribution. Then at the surface, the contributions should be under all the Vg_discharging since the fermi level under sensing is kept constant. Therefore, the distribution would increase in parallel as Sillicon device if the interface states has generation [12, 17]. However, figure 24(d) [1] indicates the discharging can be zero which means there is no generation at the interface states. And also the extracted energy distribution of charging electron

traps after charging under Vg_charging-Vth0 = 1 V at the room temperature for 1000 seconds in figure 24 (d) [1].

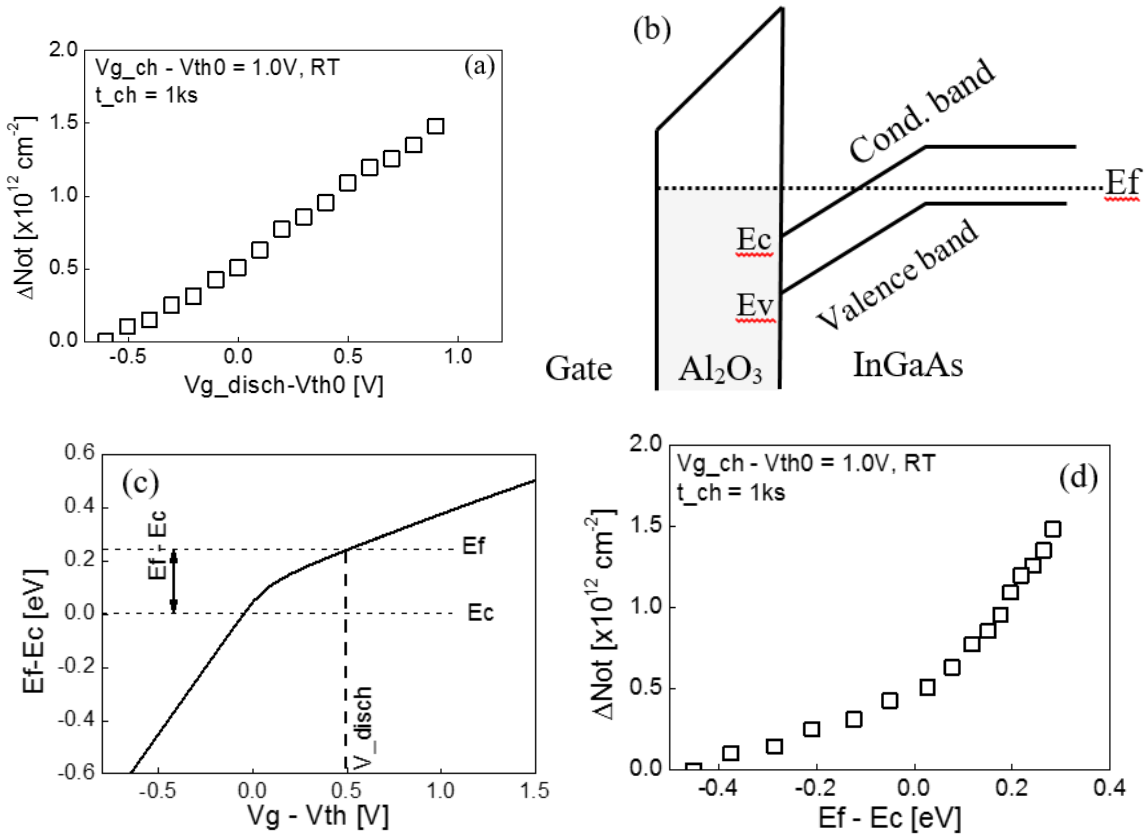

Figure 24. Energy profiling extraction ΔNt in (a) is the charged electron traps after completing discharging at each Vg_disch. The data is taken from the last point of each trace in Fig.2b. (b) Illustration of the relationship between Ef-Ec and the energy level of the charged electron traps. Ec is the conduction band of InGaAs at the interface and the shaded area denotes the charged electron traps. (c) The Ef-Ev against Vg−Vth from 1D Poisson simulator [15] for converting each Vdischarge to an Ef-Ev. (d) The extracted energy distribution of the charged electron traps after charging under Vg_ch-Vth0=1.0V for 1000 seconds.

After getting a conclusion about there is no generation at interface of InGaAs channel device, which means the border traps are extracted under different Vg_charging. Therefore, the border traps distribution after charging under different levels for 3 second at room temperature, and figure 25 (b) [1] shows in total, figure 25 (a) [1] and figure 25 (c) [1] show the distributions of two of highest and three of lowest Vg_charging levels, respectively. In details, figure 25 (c) [1] indicating the electrons traps have been charged to saturation state in shorten time.

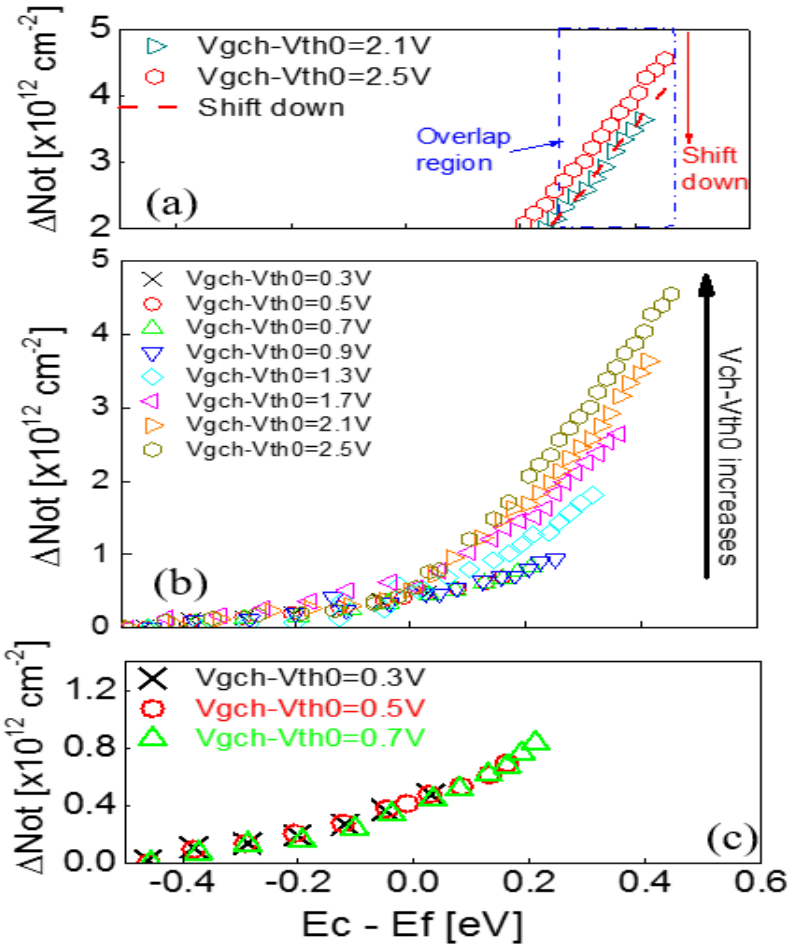

Figure 25. Trap energy distribution after charging under different levels, Vg_ch for 3sec at room temperature. The distribution traces under all Vg_ch are shown in (b). The distribution traces under two highest Vg_disch and three lowest Vg_disch are enlarged and shown in (a) and (c) respectively.

Furthermore, the same value of ΔNot and the same value of Ef-Ec after charging at different levels could indicate that all the traps between their charging level E(Vg_ch) and Ef-Ec will get discharged under Ef-Ec. So these traps may not the switchable traps, called gorund state traps. And the switchable trap which called charged state traps. In other words, the ground state traps cannot shift locations from ground level to lower energy level after charging as shown in figure 26 (a), which can identify as type A traps. And charged state traps can shift locations from ground level to lower energy level after charging as shown in figure 26 (c), which can identify as type B traps. And figure 26 (b) and figure 26 (d) show the well diagram of type A and type B, respectively.

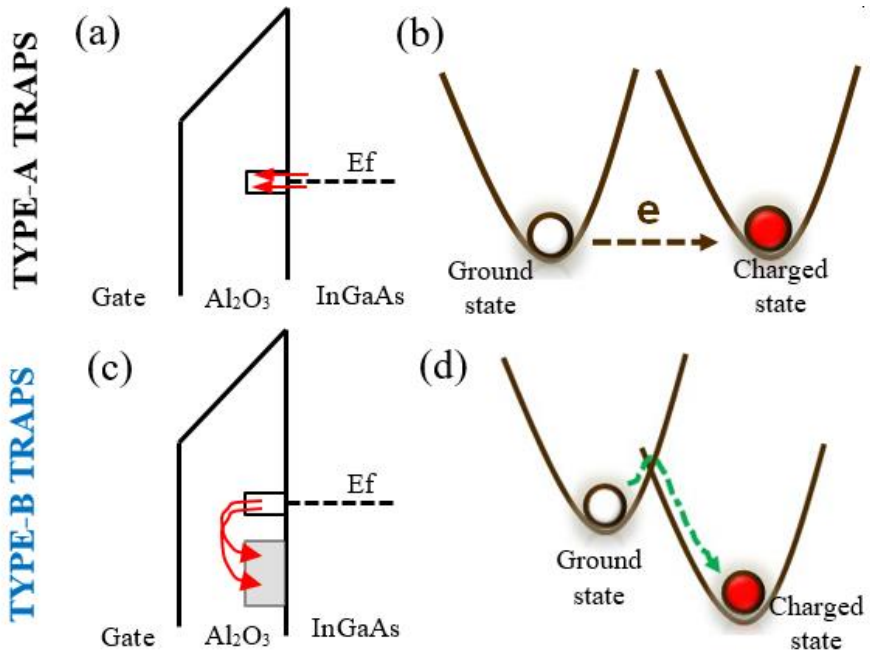

Figure 26. Illustration of charging Type-A (a) and Type-B (c) traps. After charging at Ef, Type-B traps drop from the ground states to the charged states at lower energy level. The well diagram is shown in (b) and (d) respectively.

For details, when Vg_charging increase, the distribution trace lines are not fit together anymore. Which means all type A traps have been extracted and start to extract type B traps. With higher Vg_charging, there are more charged traps can get from same Ef-Ec. Which the difference is a constant when Ef-Ec is close to the charging level and getting decrease when Ef closer Ec. And it means at higher charging level, the charged state traps can switch from ground level to lower charged levels, just like the identification it is. Obviously, there are more traps can switch than ground state traps, but there is an energy gap between those two states. Overall, the charged state trap do not discharge in the region close to charging level and the observed traps should be ground state traps, which the type A defect is independent and type B defect is dependent. In order to separate these two different traps, because the type A defect is independent, so using the parallel shifting all the voltage levels together. And the covered trace line can regard as the type A. this processing can be manually and align these curves by a constant number for each line. And type B equals to the total types minus type A traps, as figure 27 (a, b) and figure 28 (a, b) shown as below.

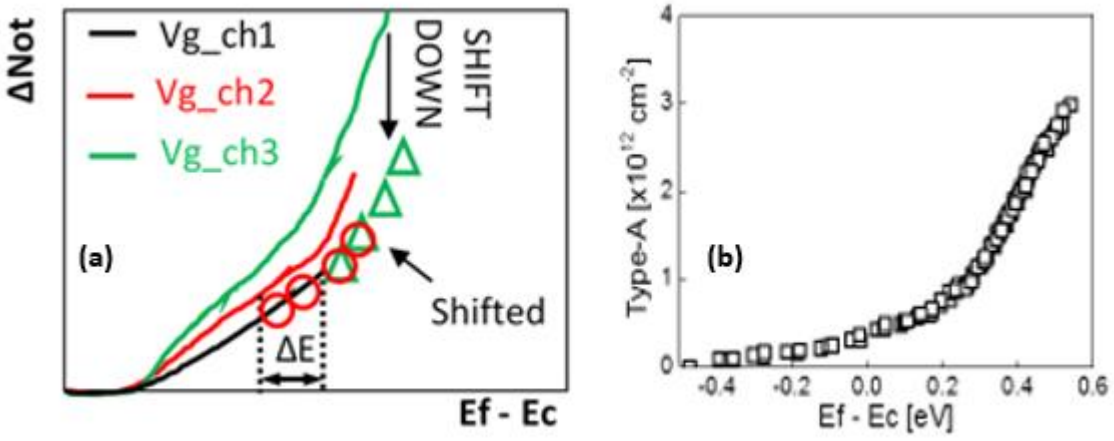

Figure 27. (a) Illustration for Type-A traps extraction. The Solid lines denote the total trap distribution under different Vg_ch level. Aligning two distributions between Vg_ch1 and Vg_ch2 to assure the region within ΔE away from Vg_ch1 overlap each other ('**O**'), Type-A traps in the energy range between Vg_ch1 and Vg_ch2 can be extracted. By following the procedure, the entire Type-A traps distribution can be obtained. (b) The Type-A traps extracted from the real measured data shown in Figure 25 (b).

In details, the solid line stands for total traps extraction under different Vg_charging level. And shifting the higher level down to the lower one as figure 27 (a) shows, after aligning, the type A can be extracted as figure 27 (b) shows. So, type A could regard as a constant value for each level voltage.

From figure 28 (a), the total traps shown under different Vg_charging, and the type A trace also marked in the graph, it clear to get type B defect for each voltage level traps. And figure 28 (b) shows the type B only, which indicates type B is dependent defect by Vg_charging. Moreover, because type A is a certain value for different voltage levels, the extracted distribution represents the ground state traps are certain value. Then the rest of traps are charged state traps. And the differences could show the border traps of energy distribution between each voltage level.

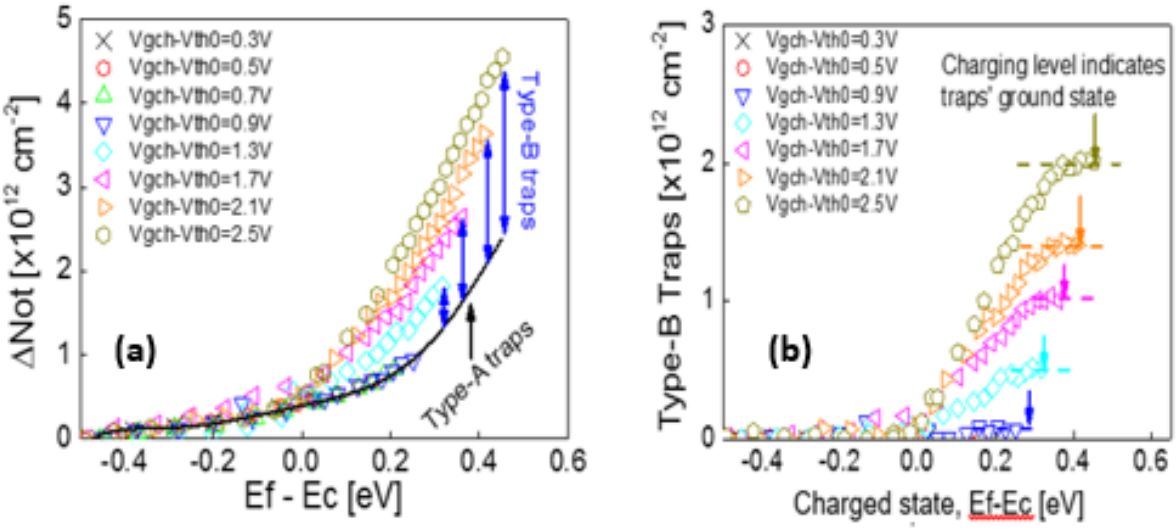

Figure 28. (a) shows type B is extracted from total traps minus type A, and (b) shows type B defects are extracted from the same data shown as figure 25(b).

In addition, comparing the total type B traps, ΔNot, and trap density per eV, ΔDot, using both these two values against Ef-Ec as figure 29.

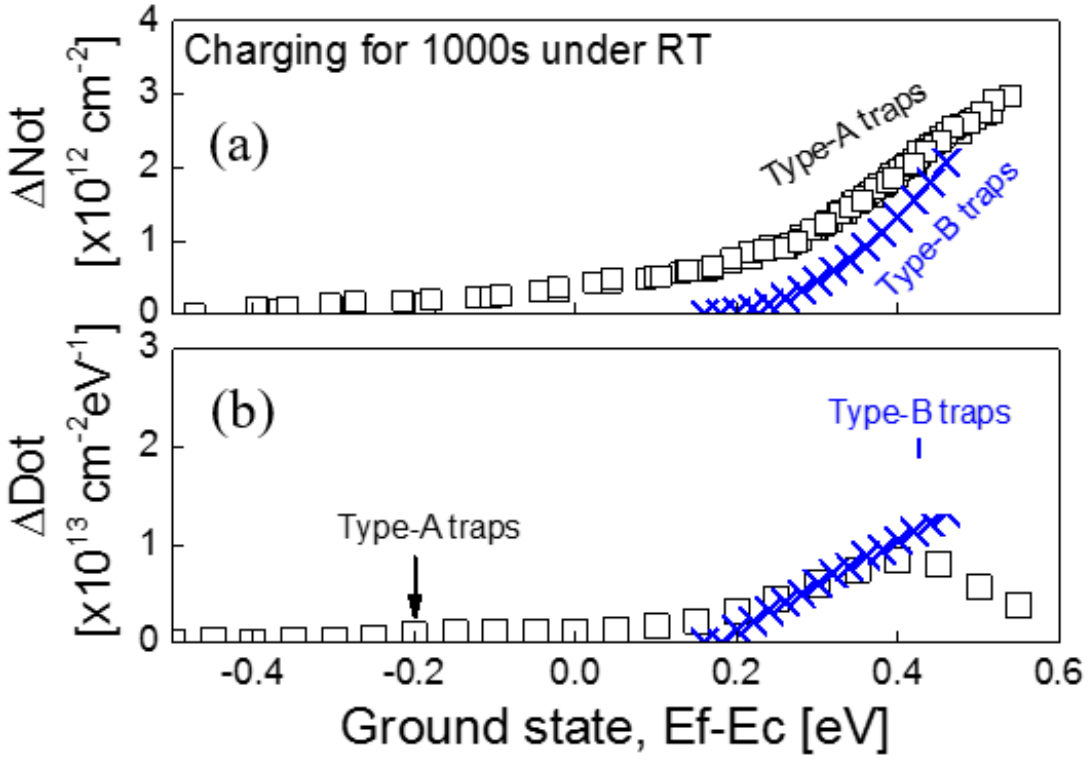

Figure 29. (a) shows energy distribution of type A and ground state of the type B, which taken form the highest trapping level for each different Vg_charging. And figure 29 (b) shows trap density by differentiating figure 29 (a). So type A have a peak value around 0.4 eV Ec of InGaAs, and type B trap would increase depend on the voltage level.

3.4 Dependence factors of trap defect separation

As mentioned before, there are some factors could affect the results. For example, the thickness of device, charging time, charging voltage, temperature, discharging time and so on. But for the defect separation, charging time, temperature and thickness of device are main three factors could impact the performance of devices.

For charging time dependence, figure 30 [1] shows under different charging time, the type A defect still is a certain value which can be aligned together, but for type B are depended by charging time. In figure 30 [1], the blue, red, black lines represent the charging time are 3 s, 100s, 1000s at room temperature, respectively. Based on result shown, the longer charging time charged, the more traps of type B trapped.

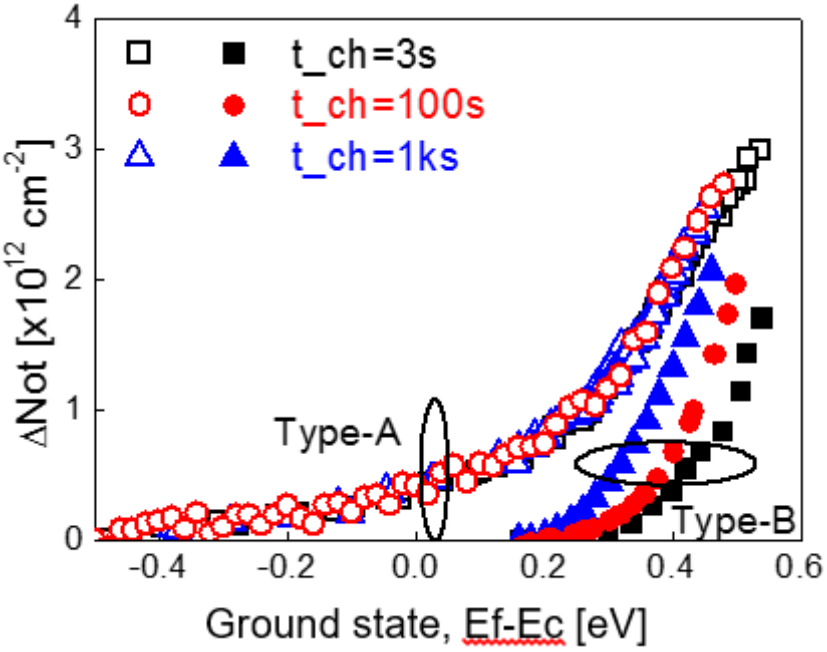

Figure 30. summary of charging time dependence of type A and type B trap at room temperature, device with channel thickness of 5nm are used.

For temperature dependence, figure 31 [1] shows the performance of InGaAs channel device under different temperature but keep all other conditions are same, device thickness is 5nm and charging time is 3s. In theory, because type A traps do not switch their energy level after charging, it means type A should be independent under high temperature or low temperature. And type B, it should be dependent by temperature because switching energy level which thermally factor could have accelerated the switching speed [18]. Therefore, for type B, the higher temperature used, the more charged traps have been extracted. For type A, no matter how high the temperature used, the traps are keep in certain level as figure 31 shown below.

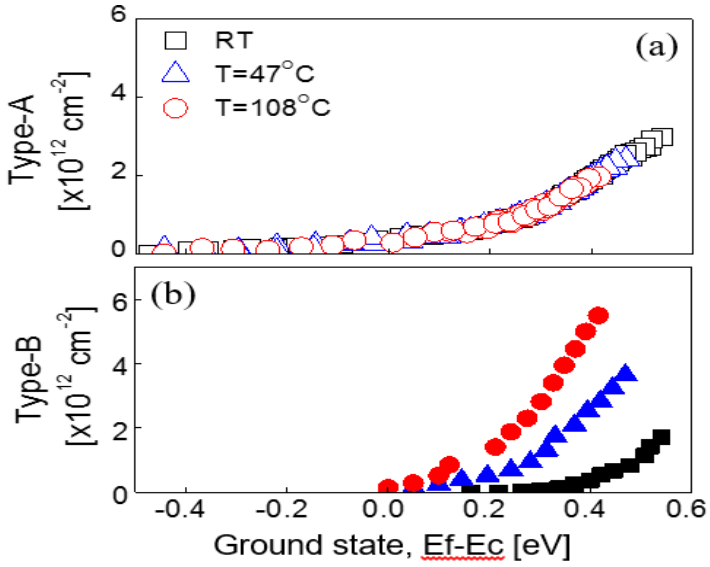

Figure 31. summary of Different temperature dependence after charging 3s. (a) and (b) present type A and type B respectivly. and deivce with channel thickness of 5nm are used.

For thickness of device dependence, figure 32 [1] shows the comparison of different thickness, based on results, both type A and type B are dependent by different thickness. Even keep other conditions are same as each other, charging time equal 3 s under room temperature.

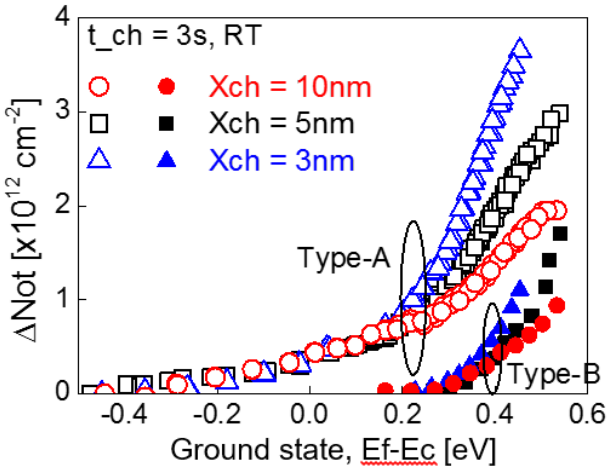

Figure 32. summary of comparison type A and type B under different thickness after charging 3s. And deivce with channel thickness of 3nm, 5nm, and 10nm are used under room temperature.

3.5 Conclusion

An investigation on border traps in III-V MOSFET with an Al_2O_3 as gate oxide and InGaAs channel has been processed and using the discharging-based energy profiling technique to analysis extracted trap energy distribution. Then two different types of traps are identified, which type A traps would not switch to lower charged levels, and type B traps would. After comparison of dependence factor, the type A is independent for charging time and temperature. And type B is dependent for that two factors. But both type A and type B are dependent for thickness of device. Overall, separate the border traps could help people understanding for new materials and process optimization. It also can improve more reliable modelling and projection.

3.6 References

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4 Discussion, conclusion and future work

4.1 Discussion

Combining the one-year researching period, especially under Dr. Ji's continuous help, I realized the process and details to do the research work, it is not a knowledge level, but also the logical level from beginning to end. Again, I really appreciate what he has done for me. This kind of experience would affect my entire life all the way done.

Back to research results, based on the direction, it focuses on solving measurement of degradation of CMOS device and new material for III-V device. Therefore, it has been divided into two parts to discuss the current results and future work. And for the device using for the discussion are same as previous work.

First of all, the voltage step stress (VSS) technique compare with conventional method, VSS can be finished within 2 or 3 hours and for single device, then it could use prediction lifetime line to get the similar results for comparing with measurement results. In other words, it uses different stress voltages to get prediction within short time for both nMOS and pMOS. And for the future work for this new technique, how to predict lifetime under either BTI or HC stress condition for fast measurement. Because unlike BTI stress, the degradation under HC stress is not only depend on the Vg, but also depends on Vd, for the past method, the lifetime is extracted

by gate current and substrate current. And the degradation of HC is indicted lucky-electron model, which means the worst case of degradation condition is Vg=(1/2)*Vd, but if the size of gate length is scaling down 0.25 um, the worst case of degradation condition could become to Vg=Vd. It can be modelled with hydrogen reaction and diffusion by electron-electron scattering. As show as the equation 5 below.

$$\Delta V_{th}(\mathrm{t}) = \frac{q}{C_{ox}} K_1 \sqrt{Q_i} \exp\left(\frac{E_{ox}}{E_0}\right) \exp\left(K_2 * \frac{E_m - \varphi_{it}}{\lambda}\right) t^n$$

(Equation 5)

K1, K2 is fitting parameters

Qi is charge carrier density during the channel

Eo is the activation energy

Eox is vertical electric field

Em is the lateral electric field

Therefore, this equation can be simplified as much as only three parameters affect threshold voltage as shown equation 6 below.

$$\Delta V_{th} = a \cdot exp\left(\frac{V_{gs}}{m}\right) t^n$$

(Equation 6)

Secondly, about the trap separation for the III-V device, in chapter 3, it uses DMP method to get the whole border of energy traps, then separate the defect traps, and also been discussed about the temperature and channel thickness dependence, which shows type A defect is independent of temperature and thickness, it maybe control by elastic tunneling, But type B defect is dependent for those parameter, it maybe control by multi-phonon. therefore, the deivce

should be used in high temperature condition to minimized the effect to get optimiztion. As figure 33 shows.

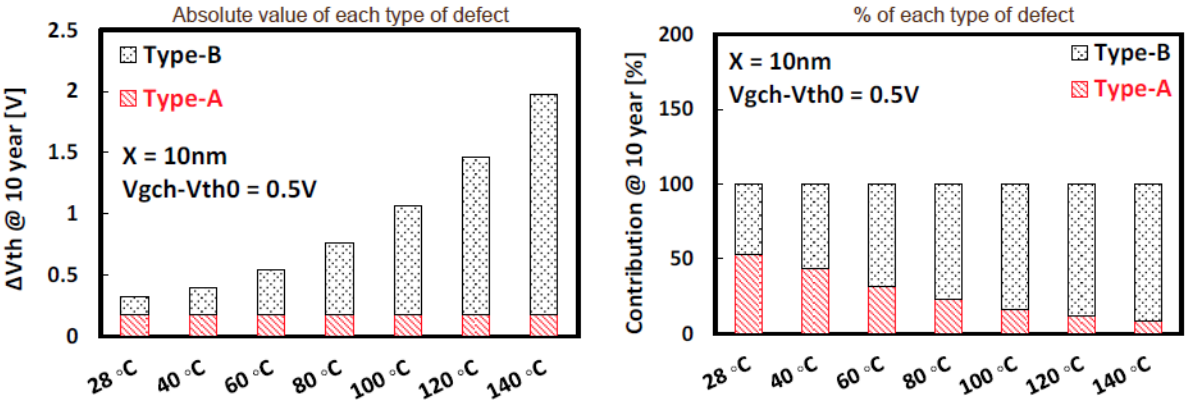

Figure 33. summary of optimization effect under different temperature with type A and type B, deivce with channel thickness of 10nm are used.

Furthermore, the temperature dependence can describe as equation 7 as below, temperature dependence of time exponent (n), acceleration factor (ŋ) and pre-factor (A0) can be extracted.

$$\Delta Vth(Type-B) = A \cdot (V_g - V_{th0})^{\eta} \cdot t^{n} \qquad \text{(equation 7)}$$

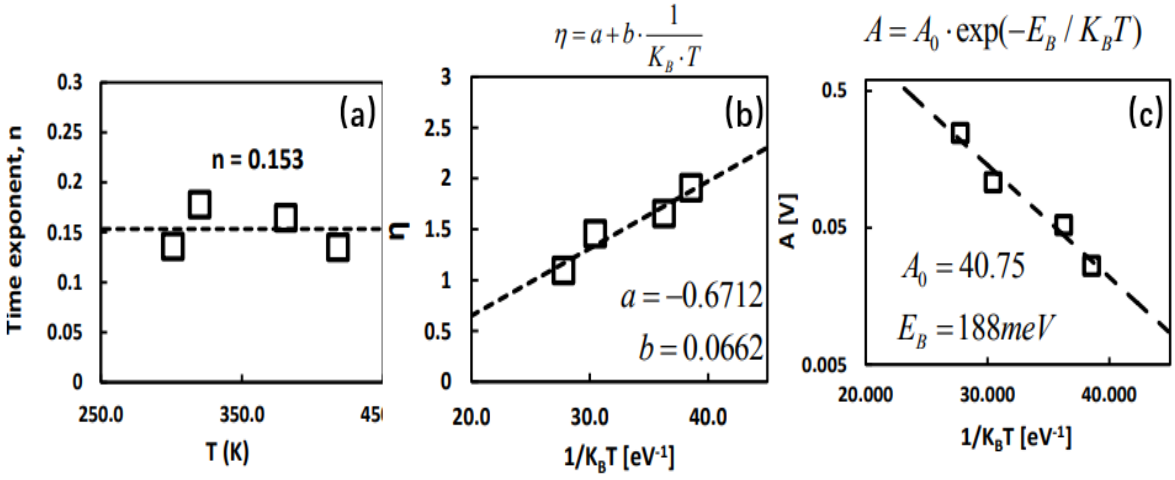

Figure 34. summary of temperature dependence experssion, type B defects are extracted from the same data shown as figure 25(b). figure 34(a) shows the n value could be roughly constant when the temperature changed, and the value is similar as silicon. Which is around 0.153.

As the figure 34 (b) ŋ is not a constant, and because ŋ=a+b*(1/K_B*T), a = -0.6712, b= 0.0662. therefore, ŋ could decrase when the temperature increase. And figure 34 (c) shows when A0 follow exponential relationship against 1/K_B*T.

Moreover, because both ŋ and A0 are changing with various temperature, it could get voltage dependence, as figure 35 shows.

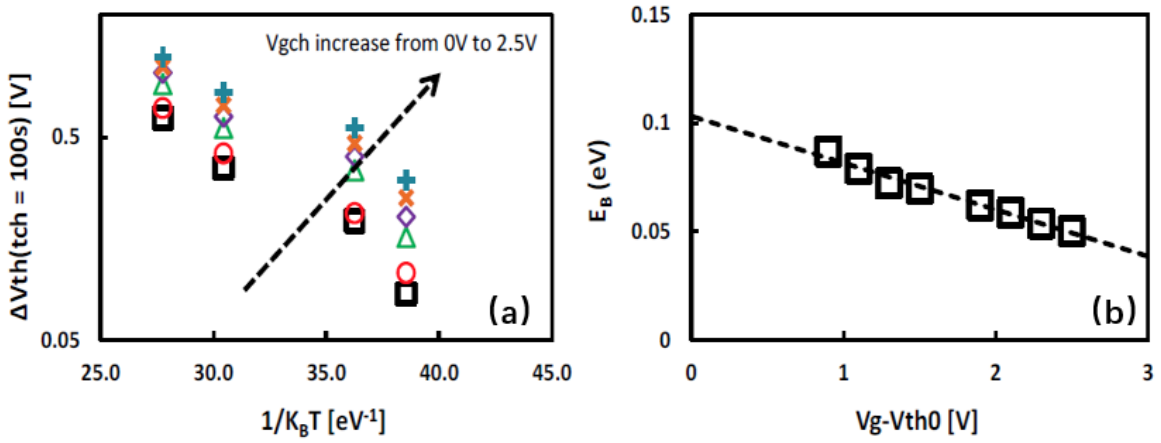

Figure 35. voltage dependence summary. type B defects are extracted from the same data shown as figure 25(b) as well. Figure 35(a) shows 1/K_B*T is not a constant but reduces when delta of Vth (charging time equal to 100s) increases. And using the conventional method to measure the lifetime can extract the activation energy (E_B) of type B traps, and figure 35(b) shows larger Vg-Vth0 would decrease the E_B (eV).

Overall, there are five parameter for lifetime predictin at different temperature, A0=40.75, E_B=0.188, a=-0.6712, b=0.0662, n=0.153. and equation 8 shows as below.

$$\Delta Vth(Type-B) = A_0 \cdot \exp(-E_B / K_B T) \cdot (V_g - V_{th0})^{a+b\cdot\frac{1}{K_B \cdot T}} \cdot t^n$$

$$\Delta Vth = \Delta Vth(Type-A) + \Delta Vth(Type-B) \qquad \text{(equation 8)}$$

And the parameter n, ŋ(γ), E_B also be extracted with slow measurement as figure 36.

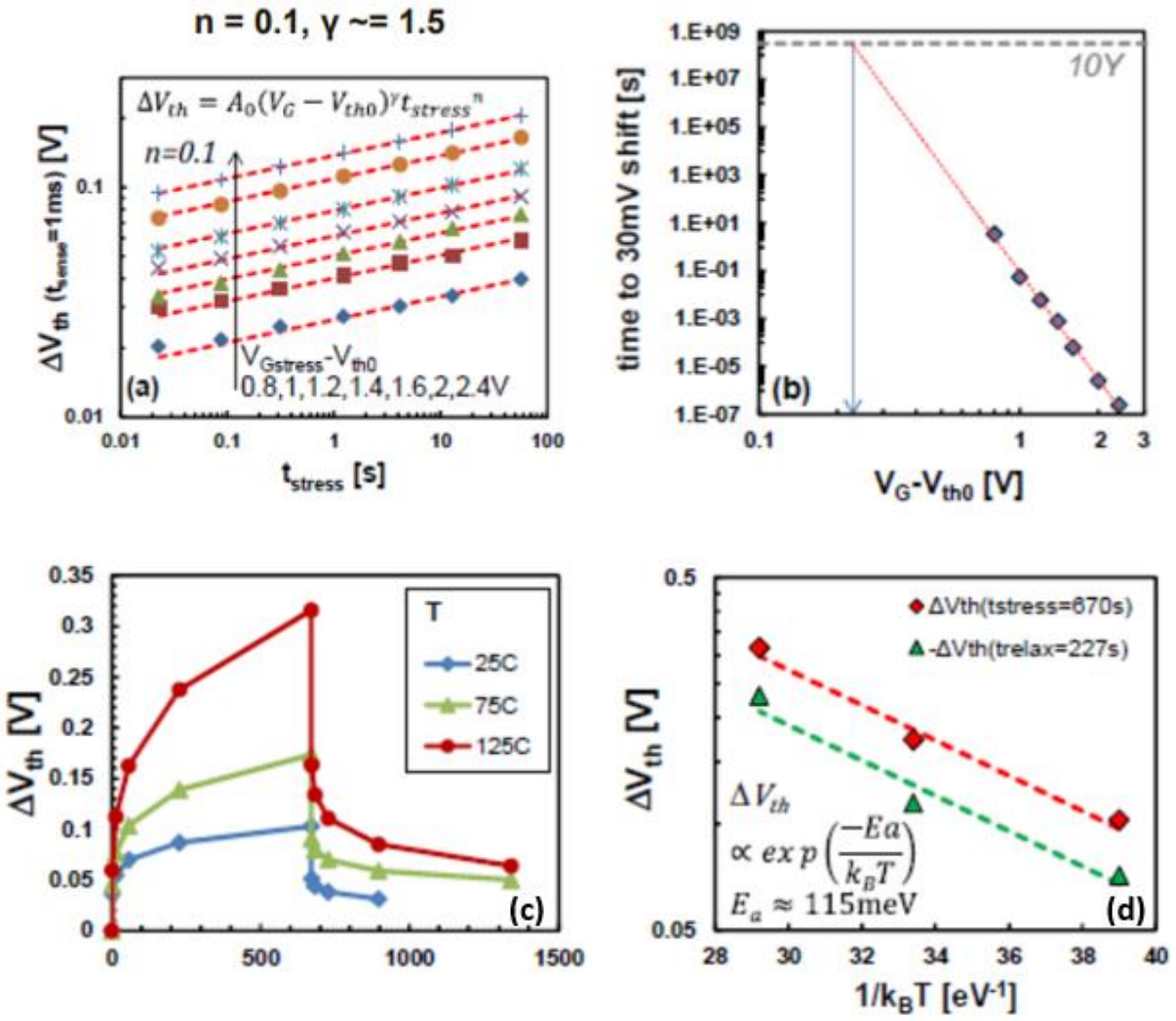

Figure 36. (a) n, γ, E_B for slow measurement, n = 0.1, γ ~= 1.5. (b) shows the lifetime can be extracted from power law extrapolatioin. (c) show EB ~= 115 meV Similar for charging and discharging stages. (d) shows the comparison with stress and recovery pararmeters.

Based on the results, the parameters which extracted fro type B traps by fast teachnique is simialr as the slow measurement, it indicate that the difference measured by slow and fast measurement is due to the dischargeing of type A traps. There are some evidences to show the conculsion as shown on figure 37, the little difference is independent of stress time, which indicating this recoverable part in only due to type A traps. And type A can be discharged faster than type B under Vg=Vth0.

COMPARISON

	Slow Meas.	Type-B from Pulse Meas.
n	0.1	0.13 ~0.15
γ	1.5	1 ~ 2
E_B	0.115	0.05 ~ 0.12

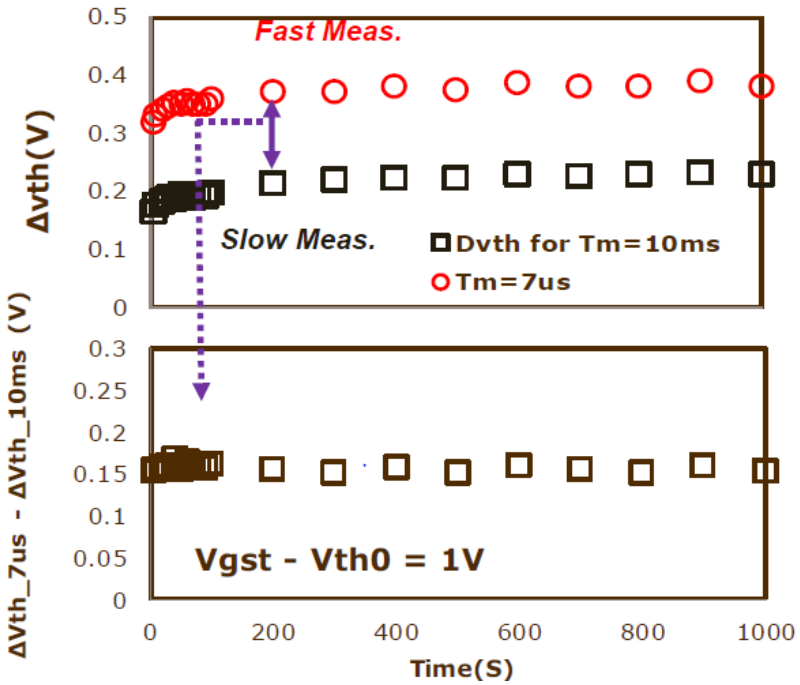

Figure 37. parameters comparison for slow and fast measurement, for the fast measurment, the stress timing equal to 7us, and for the slow measurement, the timing is 10ms. And the difference of fast and slow measurement is roughly constant.

Then combining the simulation results and experimental results under Vch=0V condition, there are good agreement can be reached. As figure 38 shows below, which means the experiment result is similar as the simulation results.

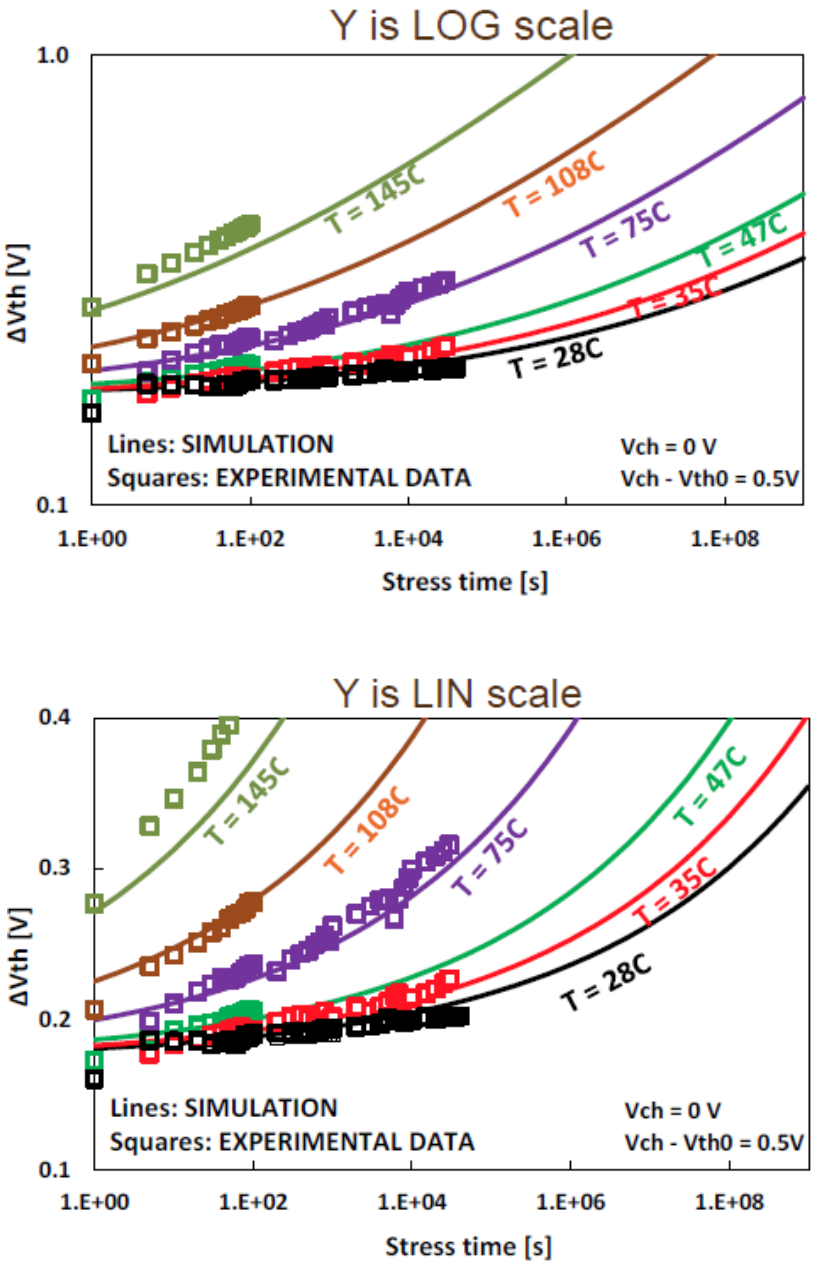

Figure 38. simulation and experimental result comparison under linear and log scale for threshold voltage. the ‘squares’ stand for experimental data, and ‘lines’ stand for simulation reuslts, it has good agreement for each other.

4.2 Conclusion and Future work

In this chapter, it would be a summary and a further plan. combining the one-year studying research, the most important harvest for me is insist. No matter how complicate project it is, it all start from a little step. And just keep effort to finish it again and again. Just based on the project mentioned in this thesis, I divide this chapter into two sections, one is for the VSS measurement method, another is defect separation and more understanding of III-V device.

For the VSS measurement method, it can measure device fast and separately, which means it only require a single device and shorted in two hours, it should widely use in measure for fast reliability screen. But it just suitable for the DC measurement by changing voltage applied. Even the method is suitable for predict the lifetime of device, and it has been confirmed with traditional measurement and simulation. Therefore, for the further direction should be add some AC pulse to same measurement system to get the capacitance value together for the device. Or in another way, using its fast and simple requirement property, people should have a try for using the method for DC measurement to get separate defect for the device. Because it has very specific power law. Such as if the defect of device measurement result follows the linear relationship it could regards as one kind of defect. And if the result follows the power law, it should regard as another defect.

About III-V device, it investigated the border traps in the NMOSFET, it used AL2O3 as the

oxide layer, and three different thickness InGaAs channel, 3nm, 5nm, 10nm. In this thesis report, and use the method of discharging-based energy profiling technique, and by analyzing the extracted trap energy distribution, then defect separated into two different types of defect, it called type A and type B. which type A is independent defect part, but type B is dependent defect part, which could be a varied value to change by thickness of channel, temperature and charging time. Those external factor could change the performance of type-B. separation of defect is not only could help to optimization of process, but also help for long term reliability modelling.

However, since III-V materials are still new, there are some parameters are still unclear and not confirmed. For example, there are three of topics should process. The first one is hot carriers, it maybe need shorter channels to remove the effect of hot carrier. And the second one is the device to device variation, it also could be problem because the InGaAs channel is too short as 3nm, which need more reliability to procedure from fab end. The third one should be lifetime prediction by using the defect separation. Using the different part of defect to do the fast and slow measurement combination to predict the lifetime.

Moreover, the simulation and experimental investigation on process dependence also could be the direction for future technology optimization.

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