

**UCC Library and UCC researchers have made this item openly available. Please [let us know](#) how this has helped you. Thanks!**

<b>Title</b>	Switched capacitor charge pump voltage-controlled current source
<b>Author(s)</b>	Avallone, Luca; Napoli, Ettore; Kennedy, Michael Peter
<b>Publication date</b>	2018-12-24
<b>Original citation</b>	Avallone, L., Napoli, E. and Kennedy, M. P. (2018) 'Switched capacitor charge pump voltage-controlled current source', 29th Irish Signals and Systems Conference (ISSC 2018), Belfast, UK, 21-22 June. doi:10.1109/ISSC.2018.8585387
<b>Type of publication</b>	Conference item
<b>Link to publisher's version</b>	<a href="https://ieeexplore.ieee.org/document/8585387">https://ieeexplore.ieee.org/document/8585387</a> <a href="http://dx.doi.org/10.1109/ISSC.2018.8585387">http://dx.doi.org/10.1109/ISSC.2018.8585387</a> Access to the full text of the published version may require a subscription.
<b>Rights</b>	<b>© 2018, IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.</b>
<b>Item downloaded from</b>	<a href="http://hdl.handle.net/10468/7525">http://hdl.handle.net/10468/7525</a>

Downloaded on 2021-11-27T08:43:09Z



**UCC**

University College Cork, Ireland  
Coláiste na hOllscoile Corcaigh

# Switched Capacitor Charge Pump Voltage-Controlled Current Source

Luca Avallone<sup>1,3</sup> Ettore Napoli<sup>2</sup> Michael Peter Kennedy<sup>1,3</sup>

<sup>1</sup>Microelectronic Circuits Centre  
Ireland, Tyndall National Institute  
Cork, IRELAND  
Email: luca.avallone@ucdconnect.ie

<sup>2</sup>Università degli Studi di Napoli,  
Federico II  
Naples, ITALY  
ettore.napoli@unina.it

<sup>3</sup>School of Electrical and Electronic  
Engineering, University College Dublin  
Belfield, Dublin 4, IRELAND  
peter.kennedy@ucd.ie

**Abstract**—This manuscript describes a switched-capacitor current source for applications such as driving high brightness LEDs and lasers. By introducing a third phase of operation into a two-phase charge pump DC-DC converter, the proposed design offers a potential solution to the excessive power typically consumed in regulating the diode or laser current. This results in a highly integrable voltage-to-current regulator.

**Index Terms**—high brightness LED driver, switched capacitor DC-DC converter, current source

## I. INTRODUCTION

With recent improvements in LEDs and semiconductor lasers in terms of reduced size and increased output power capabilities, drive currents of higher than 1A can be required, outputting over 1W of light per solid-state device [1], [2]. As these devices are commonly used in portable electronic systems, high efficiency and highly integrable power converters must be used. In this context, inductor-based Buck/Boost converters are starting to be replaced by switched capacitor DC-DC converters [3]– [6].

LEDs and lasers need to be driven by a constant current to eliminate problems associated with variations in the voltage supply and temperature that can shift their I-V curve and, in the worst case, cause thermal runaway. To achieve this, a current regulating transistor biased in saturation is often used. Unfortunately, such a series transistor can dissipate a large amount of power, and result in significant degradation of power efficiency in these systems.

The goal of this work is to present a switched capacitor charge-pump power converter which regulates current through the inherent design of the charge pump itself and not through a separate means of regulation. Furthermore, the proposed solution is compatible with the current trend of implementing converters for series connections of multiple devices, as current only needs to be regulated for one path.

The proposed solution has been simulated, design rules have been found and a prototype has been constructed.

In Section II we describe the architecture. Design rules are presented in Section III. We compare theoretical and simulated results in Section IV. The results of the constructed model have been proposed in Section V.

The analysis and the experimental results obtained in this

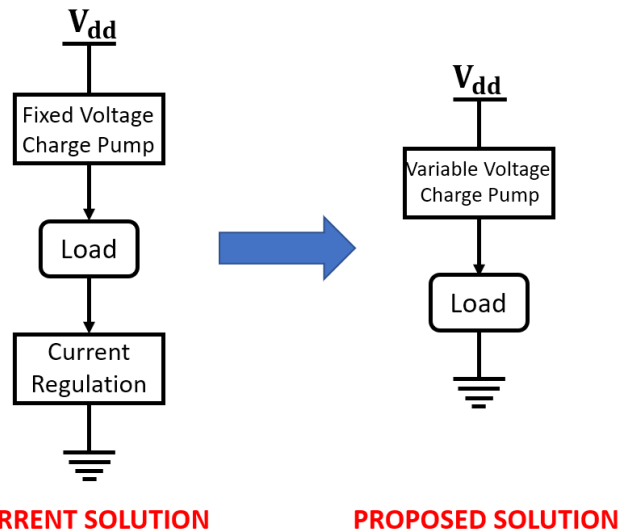


Fig. 1. Currently implemented solution (left) and proposed solution (right)

paper are mainly based on the theoretical background provided in [7].

## II. ARCHITECTURE

Fig. 1 shows on the left a conventional current source based on a charge pump [8]– [11]. The current  $I_{bias}$  that is delivered to the load by the Charge Pump, is controlled by Current Regulation block. In most cases, the current regulator is a simple transistor biased in saturation. Consequently, there is a voltage drop across it,  $V_{DS}$ , that results in a power loss,  $P_{loss}$ , defined by:

$$P_{loss} = V_{DS}I_{bias}, \quad (1)$$

where  $I_{bias}$  is the current flowing through the transistor.

The proposed design (shown in Fig. 1 on the right) avoids this problem by removing the large regulating transistor. Instead, the current is regulated within the charge pump itself. The architecture of the switched-capacitor current source introduced in this work is shown in Fig. 2.

Charge is transferred from a voltage source (denoted  $V_{dd}$  in Fig. 2) to a load (shown as a resistor  $R_2$  in Fig. 2) via a flying

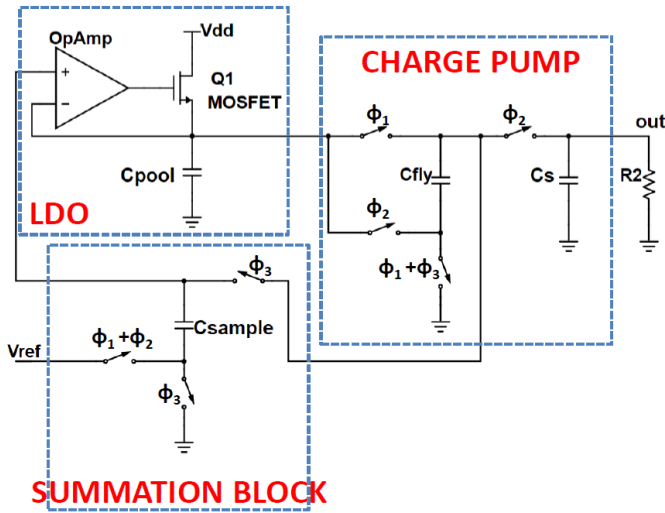


Fig. 2. Block diagram of the charge pump voltage-to-current converter

capacitor  $C_{fly}$ . After a start-up transient, the circuit reaches equilibrium when the charge delivered to  $C_{fly}$  during the first clock phase (denoted  $\phi_1$ ) equals the charge delivered to the load during the second phase (denoted  $\phi_2$ ).

The circuit in Fig. 2 can be divided into three main parts:

- A charge pump that doubles the voltage on  $C_{pool}$ ;
- A summation block that adds the sampled voltage on  $C_{fly}$  to a reference voltage  $V_{ref}$ ;
- A low-dropout (LDO) regulator that acts as a peak detector of the voltage on the non-inverting input of the operational amplifier (OpAmp), called  $V_{sum}$ .

Unlike conventional switched capacitor circuits, three non-overlapping phases  $\phi_1$ ,  $\phi_2$  and  $\phi_3$  are employed, as shown in Fig. 3. The charge transfer phases  $\phi_1$  and  $\phi_2$  are approximately half a cycle long; the measurement phase  $\phi_3$  can be much shorter, as only the sampling of the voltage on  $C_{fly}$  is required in this phase.

Fig. 4 shows the circuit topology during clock phase  $\phi_1$ . The potential on node  $X$ , called  $V_{sum}$ , is the sum of the voltage on  $C_{sample}$  (that is the sampled voltage on  $C_{fly}$  in  $\phi_3$ ) and  $V_{ref}$ . It is applied to the LDO that acts as a peak detector. Therefore,  $C_{pool}$  and  $C_{fly}$  are charged to the value of  $V_{sum}$  that it is assumed maximum and constant during  $\phi_1$  and  $\phi_2$  in this first order analysis. Meanwhile,  $C_s$  is discharging into the load; as a result,  $V_{out}$  is decreasing.

Fig. 5 shows the circuit topology during clock phase  $\phi_2$ . During  $\phi_2$ , only one function is performed, namely driving the load via  $C_{fly}$ . The voltage on  $C_{pool}$  can be considered constant because the LDO keeps the potential on node  $Y$  (shown in Fig. 4) constant and equal to the one on node  $X$ , that is assumed constant too in  $\phi_2$ .

Fig. 6 shows the circuit topology during clock phase  $\phi_3$ . During  $\phi_3$ ,  $C_{sample}$  measures the remaining charge on  $C_{fly}$  at the end of  $\phi_2$ . Also in this phase,  $C_s$  is discharging into the load, resulting in a decrease in  $V_{out}$ .

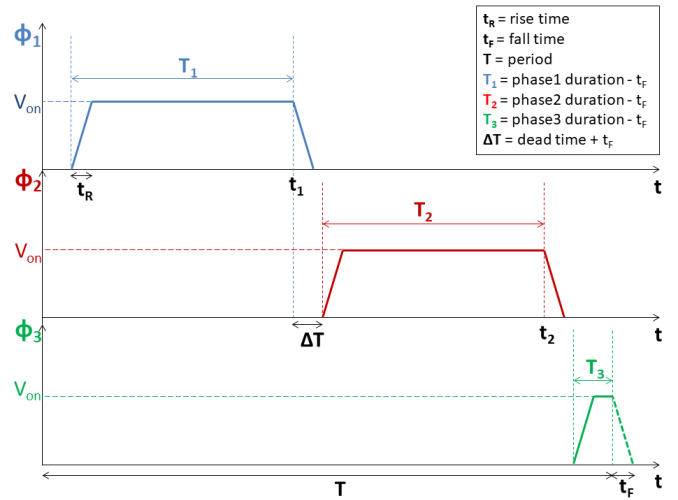


Fig. 3. Clock phases

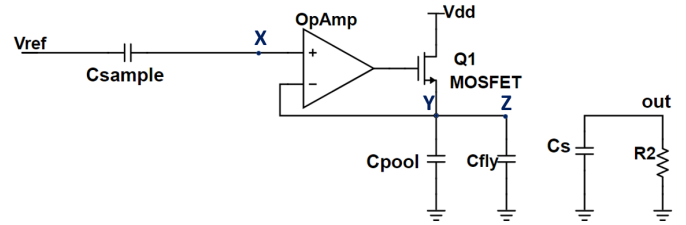


Fig. 4. Circuit topology in  $\phi_1$

### III. DESIGN RULES

Qualitatively, the system adds the reference voltage  $V_{ref}$  to the output voltage on each cycle, while the output is decaying at the load. After the transient, the output decreases at the same rate at which  $V_{ref}$  is being added to it. At this point, one can

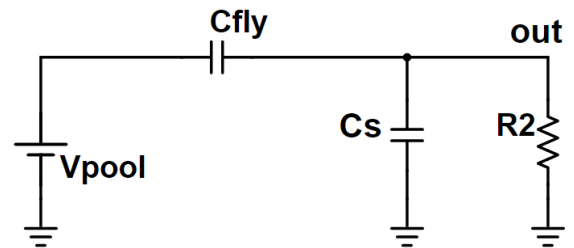


Fig. 5. Circuit topology in  $\phi_2$

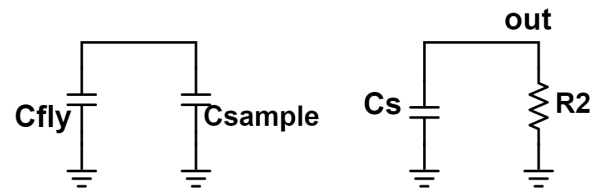


Fig. 6. Circuit topology in  $\phi_3$

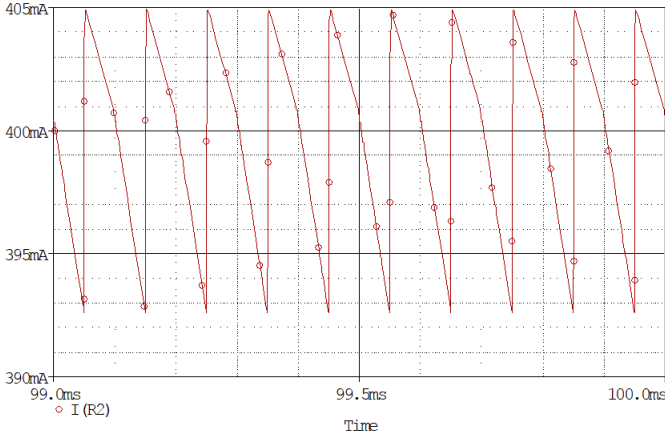


Fig. 7. Output current waveform, showing ripple

determine the charge being delivered to the load per period, and subsequently the current, as it is directly proportional to the reference voltage  $V_{ref}$ .

#### A. Average output current

The average current delivered to the load is defined by

$$I_{out,av} = \frac{Q}{T}, \quad (2)$$

where  $Q$  is the charge transferred during a period  $T$ .

In particular,

$$Q = C_{fly} V_{ref}. \quad (3)$$

With the values of  $C_{fly}$  and  $T$  fixed, the average current delivered to the load is proportional to  $V_{ref}$ , namely

$$I_{out,av} = \left( \frac{C_{fly}}{T} \right) V_{ref}. \quad (4)$$

While the total charge per cycle,  $Q$ , is delivered during  $\phi_2$ , the smoothing capacitor  $C_s$  gives apparent continuous operation. Nevertheless, the output current exhibits ripple, as shown in Fig. 7

#### B. Ripple

A set of four equations that describes the behaviour of  $V_{out}$ , the output voltage, and  $V_{pool}$ , the voltage on  $C_{pool}$ , in a period in steady-state has been derived. It also allows us to estimate the peak-to-peak ripple of the output current waveform, as we will see in this section.

Note that the times denoted in Fig. 8 as  $t_1$ ,  $t_2$ , and  $t_3$ , indicate respectively the end of  $\phi_1$ ,  $\phi_2$  and  $\phi_3$ .

Looking at the configuration of the circuit in  $\phi_2$ , shown in Fig. 5:

$$V_{fly}(t_2) = V_{out}(t_2) - V_{pool}(t_2), \quad (5)$$

where  $V_{fly}$  is the voltage on  $C_{fly}$ .

Looking at the configuration of the circuit in  $\phi_3$ , shown in Fig. 6, and assuming that  $C_{fly} \gg C_{sample}$  (we will explain this assumption later):

$$\begin{aligned} V_{sum}(t_3) &= V_{fly}(t_2) \\ V_{sum}(t_3) &= V_{out}(t_2) - V_{pool}(t_2). \end{aligned} \quad (6)$$

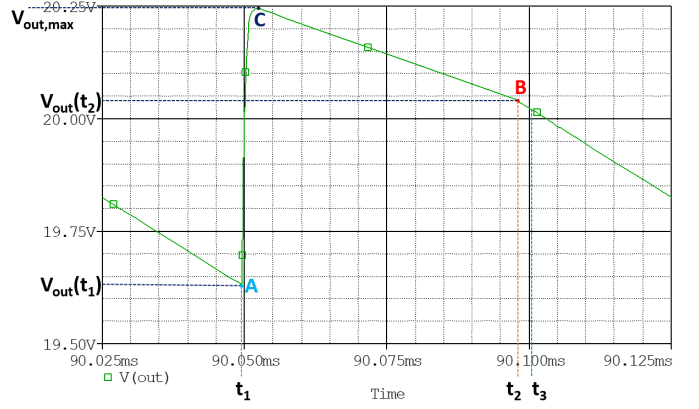


Fig. 8. Output voltage waveform in a period

Looking at the configuration of the circuit in  $\phi_1$ , shown in Fig. 4:

$$V_{sum}(t_1) = V_{sum}(t_3) + V_{ref}. \quad (7)$$

Substituting  $V_{sum}(t_3)$ , found in (6), into (7):

$$V_{sum}(t_1) = V_{out}(t_2) + V_{ref} - V_{pool}(t_2). \quad (8)$$

Since the LDO works as the peak detector of the voltage  $V_{sum}$ , that is assumed maximum and constant in  $\phi_1$ ,  $V_{pool}$  is assumed constant over the entire period:

$$V_{pool}(t_2) \simeq V_{pool} = V_{sum}(t_1). \quad (9)$$

It means that Equation (8) can be written as follows:

$$\begin{aligned} V_{pool} &= V_{out}(t_2) + V_{ref} - V_{pool} \\ V_{pool} &= \frac{V_{out}(t_2) + V_{ref}}{2}. \end{aligned} \quad (10)$$

The relationship between  $V_{out}(t_2)$  and  $V_{out}(t_1)$  can be easily found as follows:

$$V_{out}(t_1) = V_{out}(t_2) \exp\left(-\frac{(T - T_2)}{(R_2 C_s)}\right). \quad (11)$$

Furthermore, at the end of  $\phi_1$ , the voltage on  $C_{fly}$  is approximately  $V_{pool}$ . Therefore, at the beginning of  $\phi_2$ , the potential on the node denoted as  $Z$  in Fig. 4, is equal to  $2 \times V_{pool}$ , that is greater than  $V_{out}(t_1)$ . It means that, ideally, the voltage  $2 \times V_{pool} - V_{out}(t_1)$  is distributed instantaneously between the two capacitances  $C_s$  and  $C_{fly}$ :

$$V_{out,max} = V_{out}(t_1) + \frac{(2V_{pool} - V_{out}(t_1))C_{fly}}{(C_s + C_{fly})}. \quad (12)$$

After reaching its maximum value at the beginning of the second phase, the output voltage decreases (as shown also in Fig. 8) with a time constant, that has been evaluated using the open circuit time constant method:

$$\tau = R_2 C_s + R_2 * C_{fly} = R_2 (C_s + C_{fly}).$$

Therefore, the relationship between  $V_{out,max}$  and  $V_{out}(t_2)$  is as follows:

$$V_{out}(t_2) = V_{out,max} \exp\left(\frac{-T_2}{R_2 (C_s + C_{fly})}\right). \quad (13)$$

TABLE I  
PARAMETER VALUES FOR TWO CASES

PARAMETER	CASE I (SLOW)	CASE II (FAST)
$C_{pool}$	$50\mu F$	$5\mu F$
$C_{fly}$	$40\mu F$	$4\mu F$
$C_s$	$50\mu F$	$5\mu F$
$C_{sample}$	$2\mu F$	$2\mu F$
$T_1$	$48.5\mu s$	$485ns$
$T_2$	$48\mu s$	$480ns$
$T_3$	$2\mu s$	$20ns$
$T$	$100\mu s$	$1\mu s$
$R_2$	$50\Omega$	$50\Omega$
$\Delta T$	$0.5\mu s$	$5ns$
$t_r = t_f$	$100ns$	$1ns$
$V_{dd}$	$12V$	$12V$

The system of the four equations (10)–(13), returns the values of  $V_{out}$  in the points denoted as  $A$ ,  $B$  and  $C$  in Fig. 8 and  $V_{pool}$  in steady-state conditions, given the values of  $V_{ref}$ ,  $R_2$ ,  $T$ ,  $T_2$ ,  $C_s$  and  $C_{fly}$ . *MATLAB* has been used to solve it. This set of equations can also be used to estimate the peak-to-peak ripple of the output current waveform, as  $V_{out,max}$  and  $V_{out}(t_1)$  are respectively the maximum and minimum values of  $V_{out}$  in a period:

$$I_{ripple} = \frac{V_{out,max} - V_{out}(t_1)}{R_2}. \quad (14)$$

#### IV. SIMULATION RESULTS

The circuit has been simulated with *PSpice* using the parameter values of Table I. Case I is a slow clock; the clock in Case 2 is a hundred times faster. The times associated with the three phases are as indicated in Fig. 3. All switches are assumed ideal, with on and off resistances of  $10m\Omega$  and  $1M\Omega$ , respectively, and no parasitic capacitance. For more accurate results, better switch models have been used, as we will see later in this section.

Fig. 9 shows the output current and the output voltage with  $V_{ref}$  varying from 0V to 1.00V in steps of 0.25V (a) and from 0V to 0.100V in steps of 0.025V (b), respectively.  $R_2 = 50\Omega$  in both cases.

The plots are almost identical for other loads, once the voltage required to drive the specified current does not exceed the maximum voltage that the charge pump can deliver. The minor variations in both response time and ripple are as a result of the difference in time constants between the load and output smoothing capacitor. However, the average current delivered is identical for both cases and is accurately predicted by (4). Note also that the output current varies linearly with  $V_{ref}$ , as expected.

In Section III, we have assumed that  $C_{fly} \gg C_{sample}$ , but the values of these two capacitances in the two cases shown in Table I (specially in the fast one), do not satisfy this assumption. However, the circuit still works well. Once the system reaches steady-state,  $C_{sample}$  will already have an initial voltage across it (from the last cycle) that will be

TABLE II  
SIMULATED RESULTS VS PREDICTED RESULTS IN THE SLOW CASE

Variable	Equation	Simulation	Error (%)
$I_{out,av}$	$400.0mA$	$398.8mA$	0.3
$V_{pool}$	$10.527V$	$10.523V$	< 0.1
$V_{out}(t_1)$	$19.644V$	$19.631V$	< 0.1
$V_{out,max}$	$20.270V$	$20.249V$	< 0.1
$V_{out}(t_2)$	$20.053V$	$20.040V$	< 0.1
$I_{ripple}$	$12.523mA$	$12.315mA$	1.7

TABLE III  
SIMULATED RESULTS VS PREDICTED RESULTS IN THE FAST CASE

Variable	Equation	Simulation	Error (%)
$I_{out,av}$	$400.0mA$	$400.1mA$	< 0.1
$V_{pool}$	$10.053V$	$10.062V$	< 0.1
$V_{out}(t_1)$	$19.964V$	$19.976V$	< 0.1
$V_{out,max}$	$20.027V$	$20.037V$	< 0.1
$V_{out}(t_2)$	$20.005V$	$20.019V$	< 0.1
$I_{ripple}$	$1.219mA$	$1.258mA$	3.2

very close, if not identical, to that across  $C_{fly}$ . As a result, only a small charge, if any, will need to be transferred in  $\phi_3$  between the two capacitances in order to reach the same potential. Therefore, even if the assumption  $C_{fly} \gg C_{sample}$  is not satisfied, Equation (6) is still valid with a very good approximation.

#### A. Output current and ripple

Tables II and III compare the predicted and simulated results respectively in the slow case (with  $V_{ref} = 1V$ ) and the fast case (with  $V_{ref} = 0.1V$ ) of Table I. They confirm that the equations describe very well the normal operation of the circuit. Note that they do not work well under particular operating conditions, for example when the charge pump saturates. In fact,  $V_{dd}$  does not appear in any equation.

#### B. Ideal switches vs real MOSFETs

Further simulations have been performed replacing the ideal switches with real MOSFETs in order to obtain more accurate results and to find the operating limits of the circuit.

The Power MOSFETs produced by Infineon Technologies, called IRF1010EZ (its datasheet is presented in [12]), has been chosen for its low ON resistance ( $8.5m\Omega$ ) and robust handling capabilities.

The two main consequences of this replacement are:

- Due to the presence of an inherent body diode in Power MOSFETs, current is blocked in just one direction when the MOSFET is OFF. As a result, if the MOSFET Drain is not always at a higher potential than its Source, as happens for the three switches circled in red in Fig. 10 on the left, we are forced to replace the ideal bi-directional switch with two Power MOSFETs in a back-to-back configuration, shown in Fig. 10 on the right.
- Due to the high parasitic capacitances of these MOSFETs, the circuit does not work properly if the capacitance values of  $C_{fly}$ ,  $C_{pool}$  and  $C_{sample}$  are too small.

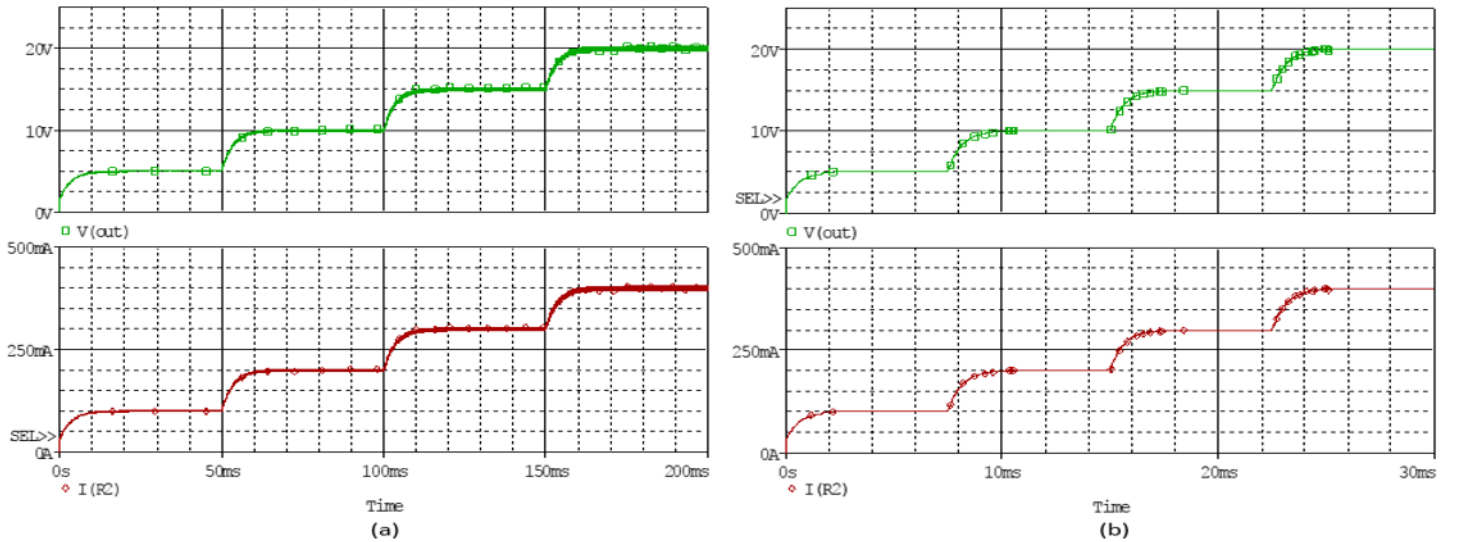


Fig. 9. Output voltage (green) and current (red) in response to linear step increase in  $V_{ref}$  in CASE I (a) and in CASE II (b)

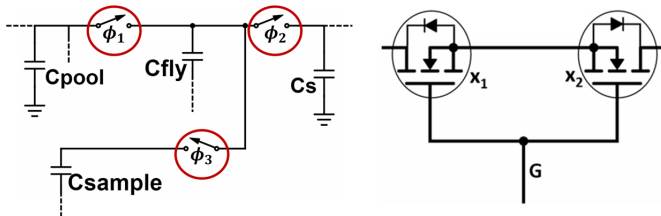


Fig. 10. The three critical switches circled in red (left) and the back-to-back configuration (right)

In particular, simulations show that the value of  $C_{sample}$  (and therefore also the values of  $C_{fly}$  and  $C_{pool}$ , since they have to be greater than it) cannot be smaller than  $1\mu F$ . This is the reason why from the slow case to the fast one, all the capacitance values are scaled except for the one of  $C_{sample}$ .

The simulation results are almost identical to the ones shown in Fig. 9, obtained using ideal switches, and they are consistent with the mathematical analysis too.

## V. PROTOTYPE

The constructed prototype is depicted in Fig. 11. The device operates effectively as a current source. Any changes in the load result in a maximum of  $3mA$  change to the drive current, once the output is not saturated at its maximum possible output voltage. This prototype has been demonstrated driving a string of four high power LEDs [13] within a variable current range of  $0-400mA$ . The output current could be linearly changed by varying the applied  $V_{ref}$  voltage. Fig. 11 shows the prototype constructed on breadboard along with oscilloscope, ammeter, and dual voltage supply. The  $V_{dd}$  supplied to the circuit is  $10.3V$  allowing for a maximum drive voltage of  $20.6V$ . The clock pulses are driven at  $26.7V$  to ensure high-side driving of the NMOS transistors dealing with the highest potentials

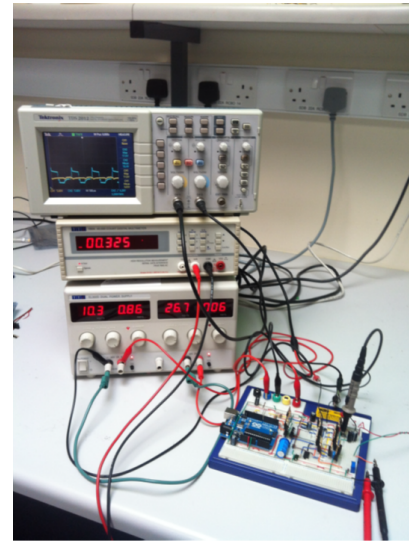


Fig. 11. Prototype setup

in the circuit. In total, eleven IRF1010EZ have been used to implement the seven switches (two for each critical switch) and the MOSFET driven by the OpAmp.

Fig. 12 and Fig. 14 show, on the right, the four high brightness LEDs driven respectively at  $152mA$  and  $312mA$  and, on the left, the corresponding instrument displays. In particular, the blue and yellow voltages (shown on the oscilloscope) are the potentials on the nodes denoted respectively as  $Z$  and  $Y$  in Fig. 4 and the output current is shown on the ammeter. The displayed results have been obtained by choosing the following discrete capacitances and frequency for the prototype:  $C_{fly} = C_{pool} = 47\mu F$ ,  $C_s = 470\mu F$ ,  $C_{sample} = 2.2\mu F$ ,  $f = 3.268kHz$  ( $T \simeq 300\mu s$ ).  $V_{ref}$  has been doubled from  $1V$  to  $2V$  to show the linear dependence of the output current.



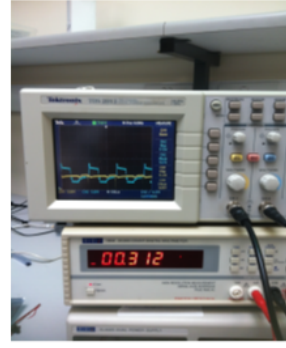
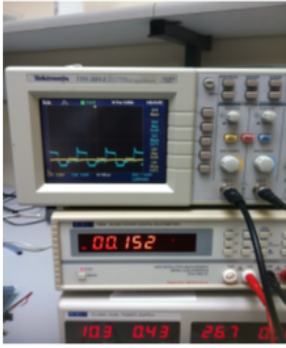


Fig. 12. Four LEDs driven at  $152\text{mA}$  (right) and the correspondent instrument readings (left)

Fig. 14. Four LEDs driven at  $312\text{mA}$  (right) and the correspondent instrument readings (left)

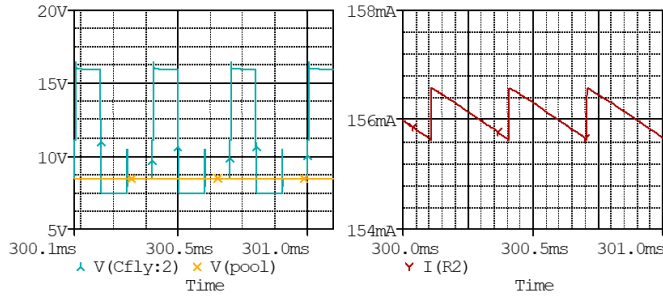


Fig. 13. *PSpice* reproduction of the results shown in Fig. 12: voltages on node  $Z$  (blue) and  $Y$  (yellow) on the left and the output current (red) on the right

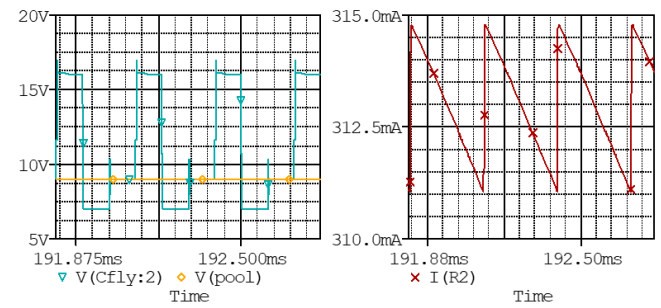


Fig. 15. *PSpice* reproduction of the results shown in Fig. 14: voltages on node  $Z$  (blue) and  $Y$  (yellow) on the left and the output current (red) on the right

These results have been reproduced using *PSpice* simulations reported in Fig. 13 and Fig. 15. The values of the prototype have been used and the effective load values,  $102\Omega$  and  $51\Omega$ , have been estimated as follows:

$$R_{on,N} = \frac{V_{f,max}N}{I_{out,av}}, \quad (15)$$

where  $N$  is the number of LEDs (4 in our case),  $V_{f,max}$  is the maximum forward voltage of each LED ( $3.99\text{V}$  from datasheet) and  $I_{out,av}$  has been evaluated by (4).

Finally, the operation of the prototype is consistent with the theoretical analysis and the simulation results shown in the previous sections.

## VI. CONCLUSION

We have presented a switched-capacitor current source in which the current regulating function is built into the charge pump. A third phase of the clock is used to measure the residual charge on the flying capacitor. There are several advantages to this design over currently implemented topologies. It can provide large output currents, suitable for driving LEDs and semiconductor lasers. Furthermore, it is highly efficient (low line impedance) and highly integrable (no inductors).

## ACKNOWLEDGMENT

This work was supported in part by Science Foundation Ireland and Enterprise Ireland under grants 13/IA/1979 and 13/RC/2077, and TC-2015-0019, respectively.

## REFERENCES

- [1] Nichia NDB7875 445nm Blue Laser Diode
- [2] 100W White LED, Wayjun Technology Co., Ltd
- [3] Vincent Wai-Shan Ng and Seth R. Sanders, "Switched capacitor DC-DC converter: superior where the Buck converter has dominated," PhD Thesis, University of California Berkeley, August 17, 2011.
- [4] T. Van Bruesseghem and M. Steyaert, "Monolithic capacitive DC-DC converter with single boundary-multiphase control and voltage domain stacking in 90 nm CMOS," July 2011, IEEE Journal of Solid-State Circuits, Vol. 46, No. 7, pp. 1715-1727.
- [5] Y. Ramadass, A. Fayed and A. Chandrakasan, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45nm CMOS," December 2010, IEEE Journal of Solid-State Circuits, Vol.45, NO. 12.
- [6] H. Jeon and Y. Kim, "A fully-integrated switched-capacitor DC-DC converter with dual output for low power application," 2012, Northeastern University, Boston MA.
- [7] N. Ellis, "A switched capacitor charge pump current source," 2013
- [8] Linear Technology, LTC3215, 700mA Low Noise High Current LED Charge Pump
- [9] Texas Instruments, White LED Charge Pump Current Source With PWM Brightness Control, TPS60231
- [10] Analog Devices, 1.0 Amp LED Flash Drive with I2C-Compatible Interface, ADP1649
- [11] Semtech, Charge Pump LED Driver, SC624, SC653, SC622A, et al.
- [12] <http://www.infineon.com/dgdl/irf1010ezpbf.pdf?fileId=5546d462533600a4015355da68861885>, Technical Datasheet IRF1010EZ, Infineon Technologies
- [13] <http://www.farnell.com/datasheets/32813.pdf>, Technical Datasheet Luxeon Rebel Green LED