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Bachelor of Science in Micro and Nanotechnology Engineering

Parameter extraction, modelling and circuit design for electrolyte-gated transistors on paper

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Abstract

Flexible and paper electronics have been getting a lot of attention in the last years. Not only from the scientific community, but also from the end consumer. This ultimately converges in efforts pushing towards the discovery of new and better materials for the TFT technology. With this fast development of new devices, compact models for circuit simulation based on older FETs become obsolete. The availability of fast and accurate models is an essential part of going from single, proof-of-concept devices, to fully operational circuits.

In this work, done in the Department of Engineering of the University of Cambridge, the electrical characterization and parameter extraction of state-of-the-art electrolyte-gated transistors (EGT) on paper substrate, fabricated at UNINOVA/I3N, led to the development of a compact model capable of describing the behaviour of the devices.

A detailed overview of the model is provided throughout this work, from the characterization of the device, to simple circuit simulations using a dozen of devices. This, together with the provided Verilog-A code for CAD software implementation, will allow both new and experienced users in circuit design to simulate simple circuits with these EGTs or any other TFT device with similar behaviour with simple tweaks on the model.

Keywords: Paper electronics; TFT; EGT; Parameter extraction; Compact model; Verilog-A.

Resumo

Eletrónica flexível e em papel tem ganho muita atenção nos últimos anos, não só por parte da comunidade científica, mas também por parte do consumidor final. Esta junção de interesses acaba por convergir num esforço dirigido para a descoberta de novos e melhores materiais para aplicação na tecnologia de transístores de filme fino. Graças a este rápido desenvolvimento de novos dispositivos, modelos para simulação de circuitos baseados em tecnologias de transístores mais antigas acabam por se tornar obsoletos. A disponibilidade de modelos rápidos e precisos é uma parte essencial da passagem de simples demonstração de novos dispositivos, para a efetiva criação de circuitos operacionais.

Neste estudo, executado no Departamento de Engenharia da Universidade de Cambridge, a caracterização elétrica e a extração de parâmetros de EGTs em substrato de papel, fabricados no UNINOVA/I3N na Universidade NOVA de Lisboa, culminou na criação de um modelo compacto capaz de descrever o comportamento elétrico destes dispositivos.

É apresentada uma visão detalhada sobre o modelo ao longo deste estudo, desde a caracterização até à simulação de circuitos simples. Isto, juntamente com o código de Verilog-A apresentado para implementação em ambiente de simulação de circuitos, permitirá a utilizadores pouco ou mais experientes simular circuitos simples com estes EGTs ou qualquer outro tipo de TFT com comportamento semelhante, com os devidos ajustes ao modelo.

Palavras-chave: Eletrónica em papel; Transistor de filme fino; EGT; Extração de parâmetros; Modelo compacto; Verilog-A.

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List of Symbols

ΔL	Channel length modulation parameter.
μ_{FE}	Field-effect mobility.
μ_{SAT}	Saturation mobility.
C_{DL}	Double layer capacitance per area.
C_i	Gate dielectric capacitance per area.
C_{ox}	Gate oxide capacitance per area.
I_{DS}	Current between drain and source.
I_{GS}	Current between gate and source.
I_{OFF}	Current at the off-state of the transistor.
L	Transistor channel length.
L_{eff}	Effective channel length.
L_{ov}	Channel length overlap.
R_C	Parasitic resistance on the contact of the transistor.
R_D	Parasitic resistance on the drain contact of the transistor.
R_{DS}	Parasitic resistance on the drain and source contacts of the transistor.
R_S	Parasitic resistance on the source contact of the transistor.
SS	Sub-threshold Slope.
VNM_H	Voltage noise margin high.
VNM_L	Voltage noise margin low.
V_{DS}	Voltage between drain and source.
V_{GS}	Voltage between gate and source.
V_H	Largest value of gate-to-source voltage measured.
V_{OH}	Output high voltage.
V_{OL}	Output low voltage.
V_{ON}	Turn-on voltage.
V_T	Threshold voltage.
V_{in}	Input voltage.
V_{out}	Output voltage.

W Transistor channel width.

Acronyms

a-Si:H	Hydrogenated Amorphous Silicon.
CAD	Computer Aided Design.
CGC	Cambridge Graphene Centre.
CHE	Cellulose-based Hydrogel Electrolyte.
EDL	Electrical Double Layer.
EGT	Electrolyte-Gated Transistor.
FET	Field Effect Transistor.
HDL	Hardware Description Language.
I3N	Instituto de Nanoestruturas, Nanomodelação e Nanofabricação.
IGZO	Indium Gallium Zinc Oxide.
ITO	Indium Tin Oxide.
LCD	Liquid Crystal Display.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
poly-Si	Polycrystalline Silicon.
TFT	Thin Film Transistor.
TOS	Transparent Oxide Semiconductor.
UCAM	University of Cambridge.
UNINOVA	Instituto de Desenvolvimento de Novas Tecnologias.

CHAPTER 1

Motivation and Objectives

With the growing interest in the flexible electronics area, in the last years there has been a big development of the Thin Film Transistor (TFT) technology and the materials used in those. All the improvements in the technology make possible applications never thought before, ranging from fully transparent displays to biochemical sensing devices. [1–8]

On the other hand, this evolution also constitutes a challenge when trying to simulate the behaviour of complex systems, as those require the use of Computer Aided Design (CAD) tools. In order to achieve high speed and accuracy in a CAD environment, a capable model device is required. [9]

This master thesis is the result of a collaboration under the BET-EU project between the NOVA University of Lisbon (through the Instituto de Desenvolvimento de Novas Tecnologias (UNINOVA) and the Instituto de Nanoestruturas, Nanomodelação e Nanofabricação (I3N)) as the home institution, and the Department of Engineering of the University of Cambridge (UCAM) as the host. The goal of this thesis was to analyse novel devices fabricated inside the UNINOVA/I3N group and apply fitting models developed in the UCAM.

This important task of knowledge exchange may ultimately result in a better understanding of both the devices' physical behaviour and the validation/improvement of the existing transistor models.

To accomplish the main objectives of this work, some critical tasks must be performed:

1. Electrical measurements on the devices, including transfer and output characteristics;
2. Extract all of the device physical parameters needed for the models to be tested with mathematical software;
3. Obtain the empirical parameters from best fitings and approximations;
4. Validate the chosen model by writing it into Verilog-A code, design the component and simple circuits to simulate.

CHAPTER 2

Introduction

In this chapter a brief introduction on the relevant topics of this thesis will be given, with special focus on Field Effect Transistor (FET) technologies such as the TFT and the Electrolyte-Gated Transistor (EGT), compact device modelling and TFT models.

2.1 The history of the thin film transistor

The first TFT dates from as early as 1962[10], about two years after the fabrication of the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET). But it was only in 1973, with the demonstration of the first TFT Liquid Crystal Display (LCD)[11], that the direction of the TFT technology research and development was defined for the following generations.

The necessity to improve the process of fabrication and at the same time produce higher quality devices led to a development in the semiconductor materials being used.[1]

With the development of the Hydrogenated Amorphous Silicon (a-Si:H) TFT in the late 1970s [12], the stability and performance of TFTs was greatly improved. These developments ultimately improved the quality of the semiconductor over large surface areas, leading to the first commercially available TFT-LCDs more than two decades after being reported for the first time.

In the following years improvements of silicon based semiconductor materials like Polycrystalline Silicon (poly-Si) represented an improvement in the overall electrical performance of the transistors, but the uniformity of this solution was an issue for the application in large area displays. Organic semiconductor materials surged as a strong alternative for low temperature fabrication [13] but the attentions eventually turned to oxide materials.

The first showing of the impressive results of using oxide materials was in 2003 when Hideo Hosono and his group reported the first Indium Gallium Zinc Oxide (IGZO) TFT [14] and 2004 when the same group reported the amorphous-IGZO-TFT[15]. For the first

time a TFT using a Transparent Oxide Semiconductor (TOS) showed a great performance for practical applications. The high mobility, good transparency and uniformity over large areas as well as low temperature fabrication are the main reasons why IGZO is now considered a standard for fully transparent devices when combined with Indium Tin Oxide (ITO) or other transparent conductors. [6, 8]

2.1.1 TFT structures and operation principle

The TFT is a FET composed by three terminals (gate, drain and source), a semiconductor layer and a dielectric layer. The semiconductor is located between drain and source, overlapping both terminals while the dielectric layer is located between the gate terminal and the semiconductor, overlapping both.

The architecture of the device depends on the position of the terminals between themselves, the most common ones are represented in figure 2.1.

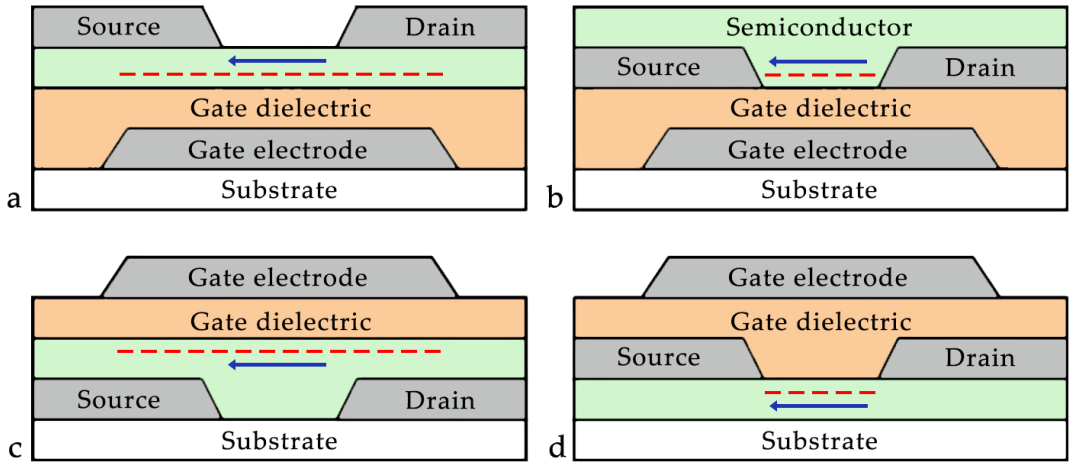


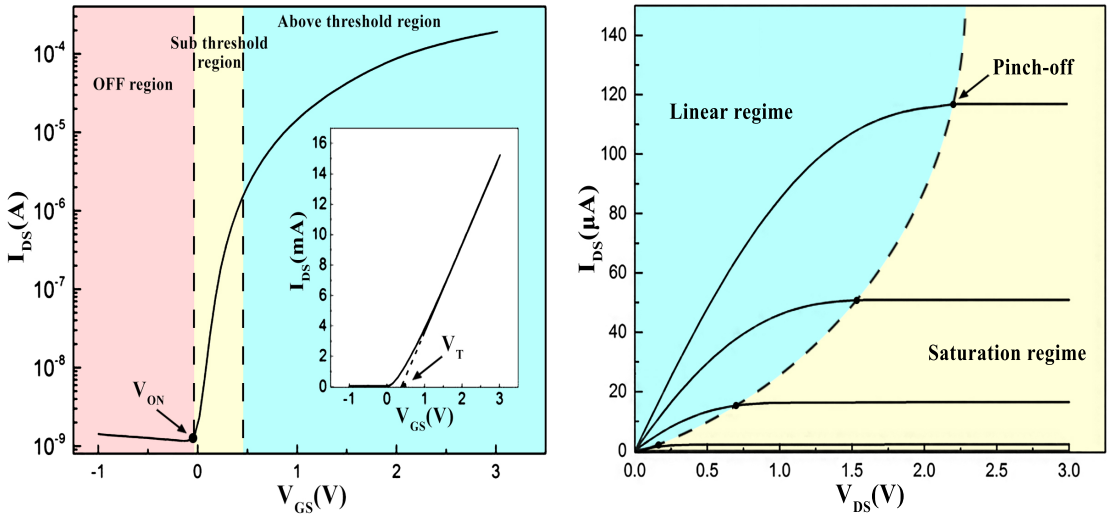
Figure 2.1: Schematic crosssections of the four principle n-type TFT architectures. The carrier channel is schematically shown in red. (a) Bottom-gate (inverted) staggered TFT. (b) Bottom-gate (inverted) coplanar TFT. (c) Top-gate staggered TFT. (d) Top-gate coplanar TFT. Adapted from [16]

The operation method of the TFT is similar to other FET devices such as the MOSFET in a sense that the voltage applied in the gate (V_{GS}) will control the current flowing between the drain and source contacts (I_{DS}).

Considering a n-type device, the operation principle can be defined as an enhancement mode (also called as normally-off) or depletion mode (normally-on) according to the threshold voltage (V_T) value, with the first one having a positive (V_T) and the second one a negative (V_T). Depletion mode devices require the application of a gate voltage to turn the transistor off, meaning normally-off devices are usually preferred in order to minimize power dissipation and facilitate circuit design. [17]

Provided there is a positive drain voltage (V_{DS}) applied, when $V_{GS}>V_T$ the dielectric layers starts acting like a capacitor and a conductive channel is created, allowing current

to flow between the drain and source electrodes, resulting in the on-state of the device. In the same line of thought, when $V_{GS} \ll V_T$ the device is in its off-state, as the dielectric-semiconductor interface is depleted of electrons resulting in very low I_{DS}. Depending on the V_{DS}, the on-state of the TFT can be defined by two different regimes as shown in the output (I_{DS} vs. V_{DS}) characteristics in figure 2.2b.



(a) Transfer characteristics

(b) Output characteristics

Figure 2.2: Typical characteristic curves of a n-type TFT

The linear regime occurs when $V_{DS} \ll V_{GS}$-V_T and can be described by the following equation:

$$I_{DS} = \frac{W}{L} C_i \cdot \mu_{FE}((V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2) \tag{2.1}$$

where C_i is the gate dielectric capacity per area in F/cm^2, μ_{FE} is the field-effect mobility in $cm^2/(V.s)$ and W and L are the width and length of the TFT channel, respectively.

The saturation regime occurs when $V_{DS} > V_{GS}$-V_T. In this regime, the semiconductor close to the drain becomes depleted and a phenomenon called pinch-off happens and leads to the saturation mode. Ideally I_{DS} is independent of V_{DS} in this regime and can be described by the following equation:

$$I_{DS} = \frac{W}{2L} C_i \cdot \mu_{SAT}(V_{GS} - V_T)^2 \tag{2.2}$$

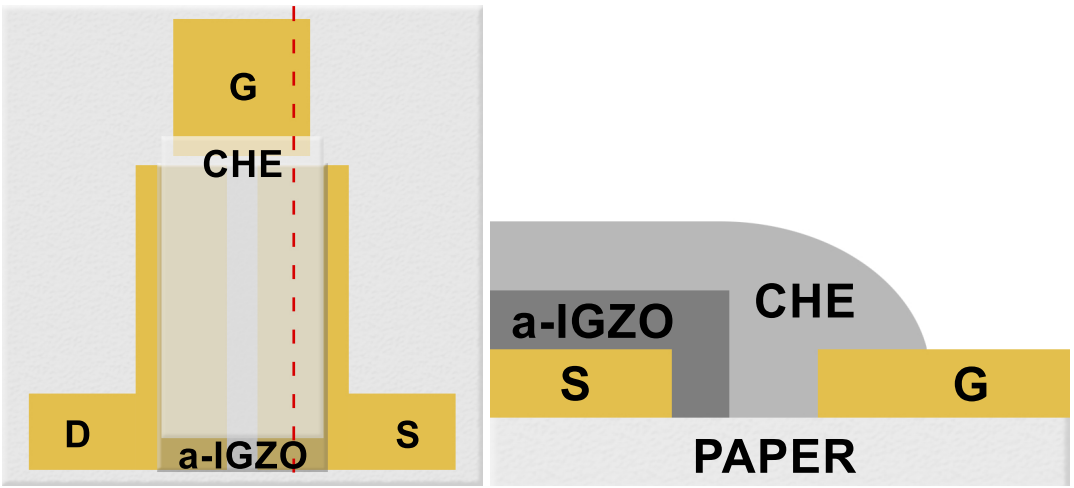
where μ_{SAT} is the saturation mobility in $cm^2/(V.s)$.

2.1.2 Electrolyte-gated transistor

Another type of FET is the EGT where a high capacitance electrolyte is used as gate insulator instead of a conventional dielectric material. [18, 19]. The usage of electrolyte-gates in TFTs allows for operating voltages lower than 2V making it possible to explore new transistor architectures. Some drawbacks of this technology are the high parasitic capacitances, high leakage currents (I_{GS}) and a big hysteresis.

The EGTs used in this work consist of a planar configuration based on Titanium/Gold bottom electrodes (gate, drain and source) deposited on multilayer-coated paper (Felix Schoeller type 3), sputtered amorphous IGZO as the active oxide semiconductor and a reusable Cellulose-based Hydrogel Electrolyte (CHE) sticker film applied as the gate dielectric as represented in figure 2.3.

These EGTs were developed by Cunha et al. and work by the principle of an Electrical Double Layer (EDL), meaning that when a potential is applied to the gate electrode, an EDL is formed in both the gate/CHE and the CHE/semiconductor interfaces. [20]



(a) Top view (b) Cross view

Figure 2.3: Schematic illustration of the CHE-gated IGZO EGTs used in this thesis

2.2 Device modelling

Nowadays device modelling plays a major part in the electronic circuits field. Design engineers resort to many CAD tools such as Spectre, HSpice and others for both designing and analysing circuits. These kinds of software contain mathematical models able to describe the behaviour of several electronic devices, allowing the engineers to predict and improve the quality of the final circuit before fabrication. [21, 22] The evolving complexity of the devices makes the accuracy of the mathematical compact models a concern, as new phenomena and non-linear behaviour become more common, entirely physical models are no longer enough. [23, 24]

The semiconductor devices compact models can then be split into three categories:

- **Physical models:** the behaviour of the device is expressed using parameters with physical meaning, such as the dimensions of the device.
- **Empirical models:** the behaviour of the device is expressed using complex mathematical equations with parameters that do not have any physical meaning.

- **Semi-empirical models:** the behaviour of the device is expressed using both parameters extracted from the device physics and empirical parameters for a better fitting in all of the device regions.

The compact models used in this thesis fall under the category of semi-empirical models.

2.2.1 TFT and EGT models

Due to the high variety of devices structures and materials used, TFT compact modelling is far behind the MOSFET when it comes to available models. In recent years some semi-empirical models have been reported for EGTs and showed accurate results for simple simulations. [25–28]

While efforts have been made to achieve TFT models with less empirical parameters and with a bigger focus on the device's physics as shown in [29], the amount of parameters required compromises the speed of simulations and semi-empirical models are still preferred for circuit simulations purposes.

In 2014 Nathan's group proposed a model [30] that uses a single, unified expression that describes both the above-threshold and sub-threshold operation regions of a TFT. This makes for simpler Verilog-A description and faster simulations as there is no need to unite different sets of multiple parameters for each sub- and above-threshold like it happens in more traditional approaches. [29]

This model uses physical parameters extracted from the $\log(I_{DS})$ vs. V_{GS} curves such as the gate voltage when the transistor transitions from the off-state to the on-state and I_{DS} starts increasing (V_{ON}) and the current on the off region (I_{OFF}).

The equations for the linear and saturation regimes are as follows:

$$I_{DS}^{lin} = G_0^{lin} \frac{W}{L_{eff}} exp\Big(\kappa_{lin}(V_{GS} - V_{ON})^{\alpha_{lin}}\Big) V'_{DS} + I_{OFF} \tag{2.3}$$

$$I_{DS}^{sat} = G_0^{sat} \frac{W}{L_{eff}} exp\Big(\kappa_{sat}(V_{GS} - V_{ON})^{\alpha_{sat}}\Big) \cdot \Big(V_{GS} - V_{ON}\Big) + I_{OFF} \tag{2.4}$$

Where G_0, κ, and α are empirical parameters extracted from the transfer characteristic curves through fittings.

To describe the transition from linear to saturation on output characteristics, a smoothness parameter (m) is added to combine equations 2.3 and 2.4 by harmonic averaging:

$$I'_{DS} \equiv \left(\left(I'^{lin}_{DS}\right)^{-m} + \left(I'^{sat}_{DS}\right)^{-m} \right)^{-1/m} \tag{2.5}$$

This unified model will be explored into detail and optimized for the EGT technology throughout this thesis.

CHAPTER 3

Methodology

In this chapter, the characterization, followed by the parameter extraction and the development/optimization of the compact model processes will be described.

3.1 Device Characterization

The measurements for this thesis were performed in the Royce Laboratories at the Cambridge Graphene Centre (CGC) (Department of Engineering - Divison B) in the University of Cambridge.

The EGTs developed by Cunha et al. [20] according to the fabrication process described in section 2.1.2 were always prepared instants before the measurements. This is a simple process where a small sticker of the CHE is applied on top of the IGZO layer, slightly overlapping the gate electrode. For a better understanding of this step, Appendix A shows the devices before and after applying the electrolyte sticker according to the suggested layout found in Figure 2.3a.

To measure the characteristics of the devices, a set-up of two KEITHLEY 2410 SourceMeter attached to a Cascade Microtech Tesla 200 using three microprobes was used in ambient temperature and humidity conditions. Using the LabTracer 2.9 software, several continuous voltage sweeps were performed while measuring I_{DS}:

- Between -2 V and 4 V of applied V_{GS} with a fixed V_{DS} of 0.2 V so the device is operating in the linear regime;
- Between -2 V and 4 V of applied V_{GS} with a fixed V_{DS} of 1.2 V so the device is operating in the saturation regime;
- Between 0 V and 4 V of applied V_{DS} for five V_{GS} incremental steps of 1 V between 1 V and 5 V, inclusive.

The source terminal was grounded for every measurement.

These measurements were repeated for several EGT sizes consisting of two devices with a channel width of 2000μm and lengths of 100 and 200μm, and three with a W of 1000μm and Ls of 40, 100 and 200μm.

3.2 Parameter Extraction

The task of extracting the physical and empirical parameters was performed in the offices of the CGC using both OriginPro 2016 and Matlab R2018a softwares.

3.2.1 Physical Parameters

3.2.1.1 Threshold Voltage

While the unified model doesn't use the V_T of the device for it's equations, the extraction of this value is of major importance to extract the contact resistance (R_C) and the channel length parameter (ΔL). [31]

There are several methods of extracting V_T [32], but a better understanding of the physical meaning of the threshold voltage parameter allows us to decide that the second derivative method is the one that works best for a TFT given it's independence of the resistance induced by the terminal electrodes. [33] This method takes into account the ideal model of a FET where I_{DS}=0 for $V_{GS} \leqslant V_T$ and increases linearly for $V_{GS} > V_T$. The first derivative will be a step function and the second derivative will show it's maximum at V_{GS}=V_T.

3.2.1.2 Contact Resistance and Channel Length Enlargement

In equation 2.3 we can observe an unknown coefficient V'_{DS}, this is effective drain voltage defined as $V_{DS}-2R_C I_{DS}$, where R_C is the contact resistance. The contact resistance is defined as the parasitic resistance caused by the electrodes (R_S and R_D). For simplification purposes we can assume R_S=R_D=R_C and define $2R_C$=R_{DS}. A schematic view of V'_{DS} in a TFT equivalent circuit when considering R_{DS} can be observed in figure 3.1.

Another unknown coefficient in both I_{DS} equations used in the unified model is the effective channel length (L_{eff}). Here L_{eff}=L+ΔL, where L is the measured channel length (using optical microscope imaging and the software ImageJ) and ΔL is the channel length enlargement parameter.

A commonly used method to extract the R_{DS} and ΔL values is to plot $R_T W$ vs. L for several $V_{GS}-V_T$, where R_T is the total resistance of the device and can be defined as V_{DS}/I^{lin}_{DS}. It is an important task to normalize the voltages values using V_T, as this value can be very different between devices.

Fitting linearly the points with the same $V_{GS}-V_T$, all of the fitted lines would ideally intercept in the same point that would correspond to $R_{DS}W$ and ΔL as observed in figure 3.2.

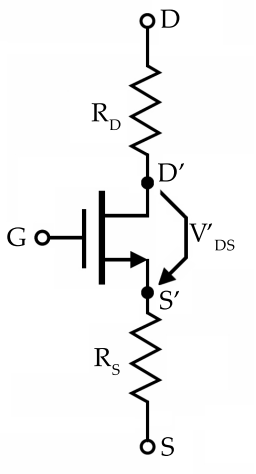


Figure 3.1: Schematic of a TFT symbol including contact resistances

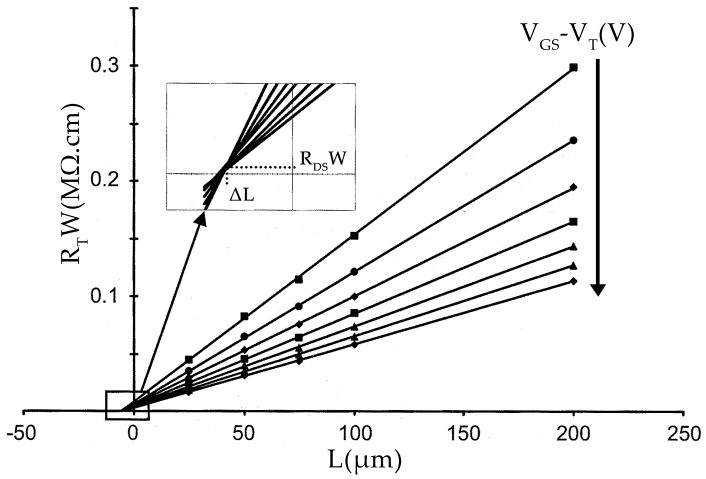


Figure 3.2: Schematic of R_{DS}W and ΔL extraction

However, due to possible variations in the fabrication process or some V_{GS} bias dependence in the above parameters, in order to obtain the actual contact resistance and ΔL, a new graph must be plotted using the values of the slopes (A) and interceptions (B) from the fitted lines as *Bvs.A* since

$$R_T W = AL + B \tag{3.1}$$

where

$$B = R_{DS} W + A\Delta L \tag{3.2}$$

As observed in equations 3.1 and 3.2, the slope of a linear fit of the points in the *Bvs.A* plot will now give us the value of ΔL and the interception $R_{DS}W$. [31]

3.2.1.3 Turn-On Voltage and OFF-State Current

The extraction of the turn-on voltage (V_{ON}) and the off current (I_{OFF}) is a more straight forward task as it only requires the observation of the point where the current starts increasing, as mentioned previously. This is an easy process as illustrated by figure 3.3.

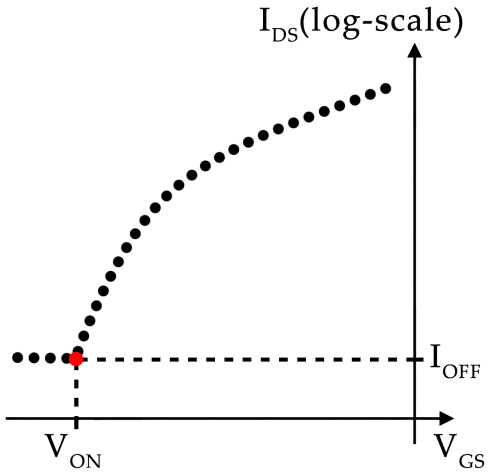


Figure 3.3: Schematic of V_{ON} and I_{OFF} extraction

3.2.2 Empirical Parameters

3.2.2.1 Alpha and Kappa Parameters

Having the physical parameters extracted, the extraction of the empirical ones is now required. The unknown α and κ coefficients for both linear and saturation regime can be obtained by rewriting equations 2.3 and 2.4 as:

$$U_{lin} = \frac{I'_{DS}/V'_{DS}}{d(I'_{DS}/V'_{DS})/dV_{GS}} = \frac{1}{\alpha_{lin}\kappa_{lin}}(V_{GS} - V_{ON})^{1-\alpha_{lin}} \tag{3.3}$$

$$U_{sat} = \frac{I'_{DS}/(V_{GS} - V_{ON})}{d(I'_{DS}/(V_{GS} - V_{ON}))/dV_{GS}} = \frac{1}{\alpha_{sat}\kappa_{sat}}(V_{GS} - V_{ON})^{1-\alpha_{sat}} \tag{3.4}$$

where $I'_{DS} \equiv I_{DS} - I_{OFF}$.

In equation 3.3, $1 - \alpha_{lin}$ and $ln(1/(\alpha_{lin}\kappa_{lin}))$ are the slope and intercept in the plot of $\ln(U_{lin})$ vs. $\ln(V_{GS} - V_{ON})$. Using equation 3.4 we can extract α_{sat} and κ_{sat} in a similar way.

3.2.2.2 G0 Parameter

The remaining parameters in the I_{DS} equations of the model are G_0^{lin} and G_0^{sat}. These are extracted by solving the following equations at the largest value of V_{GS} measured (V_H):

$$G_0^{lin} = \frac{I'_{DS}(V_{GS} = V_H)}{(W/L_{eff})exp(\kappa_{lin}(V_H - V_{ON})^{\alpha_{lin}})V'_{DS}} \tag{3.5}$$

$$G_0^{sat} = \frac{I'_{DS}(V_{GS} = V_H)}{(W/L_{eff})exp(\kappa_{sat}(V_H - V_{ON})^{\alpha_{sat}})(V_H - V_{ON})} \tag{3.6}$$

This concludes the extraction of parameters for the unified model purposed by [30].

3.2.3 Harmonic Average with Smoothness Parameter

According to the unified model, to describe the transition from linear to saturation regimes on the output characteristics, equations 2.3 and 2.4 should be combined by harmonic averaging using a smoothness parameter m defined as:

$$m \equiv \frac{1}{log_2(I_{sat}/I_s)} \tag{3.7}$$

where I_{sat} is I'^{sat}_{DS} at $V_{DS} = V_{DS}(\max)$ and I_s is the drain current when $I^{lin}_{DS} = I^{sat}_{DS}$, as observed in figure 3.4.

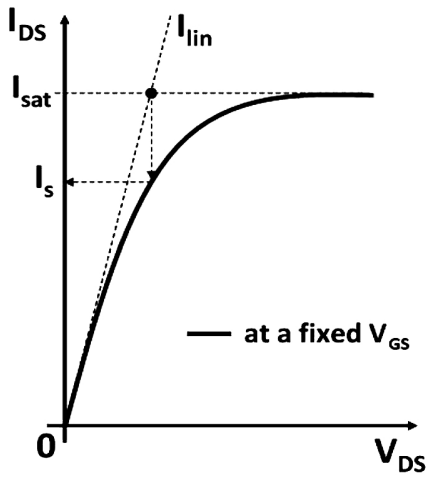


Figure 3.4: Schematic of the extraction of I_s from an output characteristic curve. Adapted from [30]

The value of I_{DS} will then be described by equation 2.5.

This total I_{DS} will be to fit both the transfer and output characteristics of our devices, as this will make for a simpler description model when writing it for circuit simulation software.

3.2.4 Model Improvements

After extracting and fitting the model according to equation 2.5, special attention will be given to the areas where the curves will not match the measured device's characteristics within a reasonable margin of error.

It is expected that a model built for more traditional TFTs might not fit a novel device like the EGT in study with perfection and additional parameters should be added in this case. If additional empirical parameters are not enough, a new term might be considered

for either the above-threshold or sub-threshold regions, keeping the total I_{DS} equation from the unified model as the other term.

While adding a new term might improve greatly the accuracy of the model, it will have implications in the speed of simulation as discussed previously, so compromises must be ultimately made in accordance to the experimental results.

3.3 Circuit Simulation

Having the final equations for the mathematical model, it's time to write the code for the Verilog-A compact model. This process requires some understanding of the principles behind the language, as Verilog-A is a Hardware Description Language (HDL). These are intended for high-level behavioural modelling and are less focused on the math and more on the physics when compared to Matlab.

The EKV MOSFET model will be used as a starting point for the EGT compact model and documentation like the The Designer's Guide to Verilog-AMS [34] or the Verilog-AMS Language Reference Manual [35] become important supports as preparation for this step.

For this process, a Cadence software license was used including the Virtuoso Schematic Editor. This license belonged to the Department of Engineering of the UCAM and was accessed using a SSH client through the CGC network.

Once the code is written and the symbol is created, simple circuits will be designed. First a simple circuit where voltage is applied to the gate and drain terminals while source is grounded to test if the compact model code is correct. If everything is working as intended, a simple inverter and ring oscillator using the inverter will be designed and their results analysed.

CHAPTER 4

Results and Discussion

In this chapter, the methods described in chapter 3 will be applied to the devices in study and the results will be analysed and discussed into detail if necessary for a better understanding of the work done throughout this thesis.

4.1 Unified Model

4.1.1 Threshold Voltage

The 2nd derivative method was used for I_{DS} in the linear regime (V_{DS} = 0.2 V) for every device. This process was made using OriginPro's integrated differentiate tool and the settings used were the direct second order derivative with a Savitzky-Golay smoothing method of the third polynomial order. Similar values were obtained between devices, with V_T ranging from 2 V to 2.2 V. The method of extraction is exemplified in figure 4.1. While some noise might be present using this method, overall the main peak is evident and seems visually aligned with what we would get using a less accurate method like the linear fitting.

4.1.2 Contact Resistance and Channel Length Enlargement

The contact resistance was extracted from the transfer curves of the five devices in the linear regime. This required a normalization of the drain current between the two different widths (W $\simeq$ 1mm and W $\simeq$ 2mm). After normalizing I_{DS}, the mean value of I_{DS} for the same $V_{GS} - V_T$ was calculated for the two devices with L $\simeq 40\mu$m and the two with L $\simeq 200\mu$m. For device with L $\simeq 100\mu$m this process was not required due to having just one sample size.

The three sets of values ($L \simeq 40\mu$m; $L \simeq 100\mu$m and $L \simeq 200\mu$m) were then divided by the applied V_{DS} of 0.2 V and ploted against the lengths (R_TW vs. L) as shown in figure 4.2a.

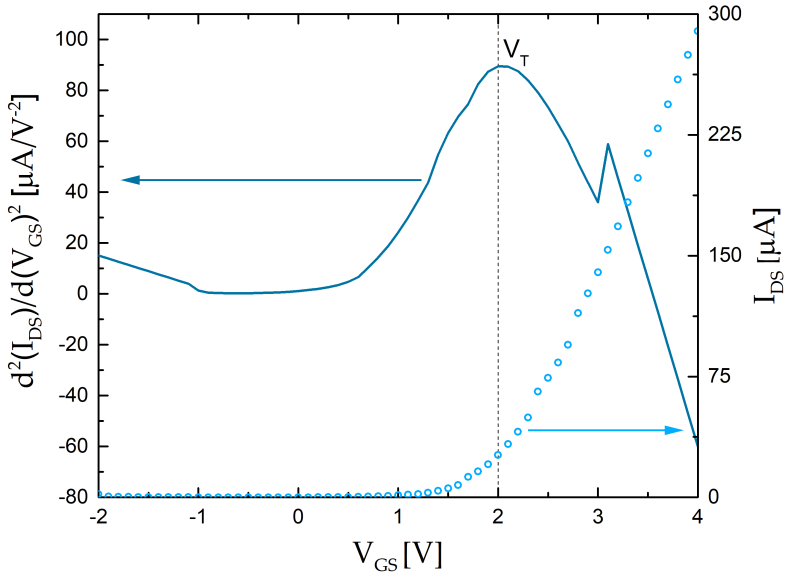
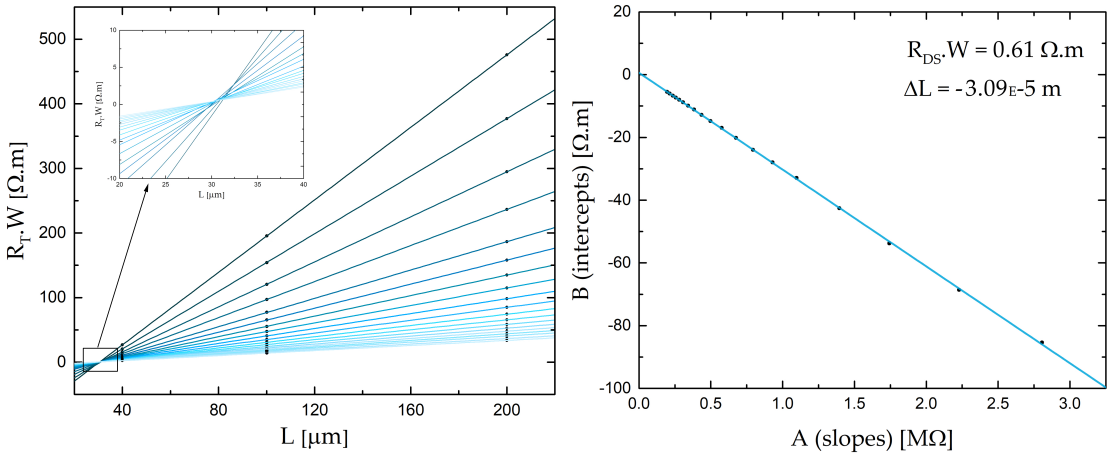


Figure 4.1: Example of V_T extraction for a device with W $\simeq$ 2mm and L $\simeq$ 40μm. The plot in light blue circles is I_{DS} vs. V_{GS} and the dark blue line is it's second derivative.

Then, following the procedure described in section 3.2.1.2, the interceptions with the abscissas axis (B) and the slopes (A) of every linear fit will be plotted as B vs. A and the best linear fit of this plot will give us the the values for $R_{DS}W$ and ΔL.



(a) R_TW as a function of L for different values of $V_{GS} - V_T$ with best linear fittings

(b) B as a function of A and best linear fitting

Figure 4.2: Functions for R_{DS}W and ΔL extraction

As observed in figure 4.2b, the extracted values are $R_{DS}W \simeq 0.61$ Ω.m and $\Delta L \simeq -30.86\mu$m. While R_{DS} is a small value that will make V'_{DS} feel rather consistent for a span of V_{DS} values, the ΔL is a large value that might harm the accuracy of the model between different device dimensions.

4.1.3 Turn-On Voltage and OFF-State Current

As discussed previously on section 3.2.1.3, the extraction of V_{ON} and I_{OFF} is very simple and only requires the observation and selection of one point on the transfer curves.

Figure 4.3 illustrates the selection process for these parameters.

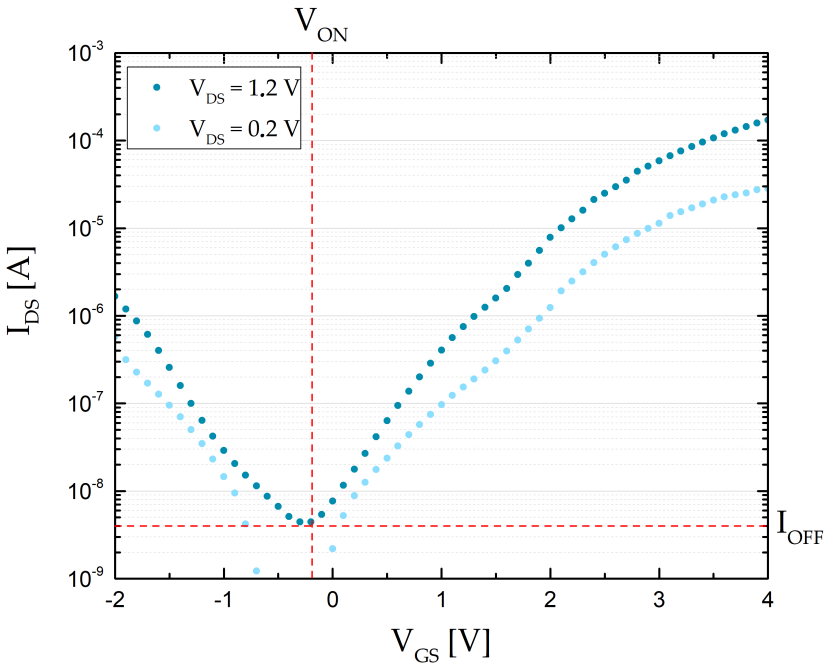


Figure 4.3: Transfer characteristics of a device with W ≃ 1mm and L ≃ 100μm highlighting the values of V_{ON} and I_{OFF}. The blue dots are the measured values of I_{DS}^{lin} and the dark blue ones are I_{DS}^{sat}.

The value of V_{ON} was not always the same for different device dimensions, but for simplifications purposes a single mean value of $V_{ON} = -0.1$ V was selected. This will make for a more simple model and due to expected sub-threshold adjustments the differences on the final model caused by slightly different V_{ON} would not be too relevant for the accuracy of the model.

Something similar happens to I_{OFF}, where the value is slightly different across the board. This variance not only happens for different devices sizes, but also for different operation regimes as the I_{OFF} region is dominated by the leakage current (I_{GS}), which varies with V_{DS}.

In this case the selected value of $I_{OFF} = 4$ nA was not a mean, but rather a rounded down value of said mean. This is due to the fact that in the total I_{DS} on the unified model equation (eq. 2.5) the I_{OFF} value will increase and choosing a value lower than observed for the parameter leaves some leverage for latter adjustments.

4.1.4 Alpha and Kappa Parameters

Having extracted the physical parameters, we can now extract the values of α and κ for both linear and saturation regimes.

This process was already described in section 3.2.2.1 and consists of plotting ln(3.3) and ln(3.3) vs. ln($V_{GS} - V_{ON}$). The device with W $\simeq$ 1mm and L $\simeq$ 100μm was considered for this plot and figure 4.4 shows the results of the best linear fits for each regime, with the respective slopes and intercepts.

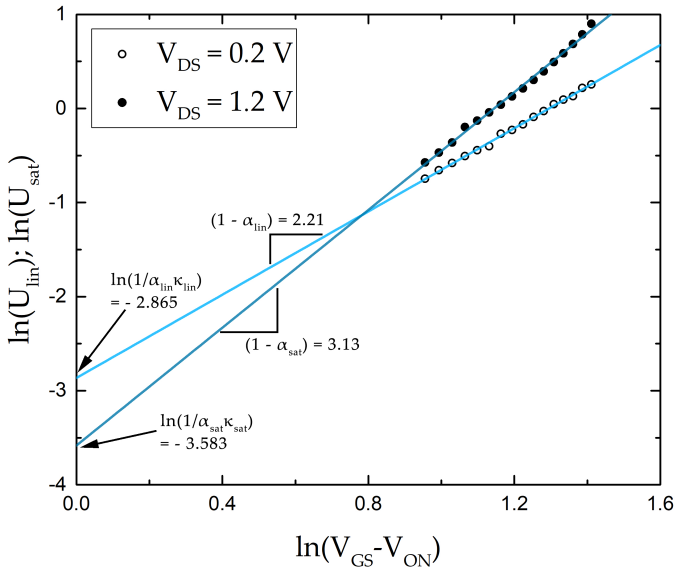


Figure 4.4: Best linear fit of ln(U_{lin}) and ln(U_{sat}) vs. ln($V_{GS} - V_{ON}$) for α and κ extraction.

From solving the equations shown in figure 4.4, we can obtain the desired values. These are $\alpha_{lin} \simeq -1.21$; $\kappa_{lin} \simeq -14.47$; $\alpha_{sat} \simeq -2.13$; $\kappa_{sat} \simeq -16.89$.

4.1.5 G0 Parameter

With all the previous parameters known, we can now extract G_0^{lin} and G_0^{sat} by solving equations 3.5 and 3.6.

The chosen value for V_H is the largest measured in the transfer characteristics (V_H = 4 V) and for the first time the terms $L_{eff} = L - \Delta L$ and $V'_{DS} = V_{DS} - R_{DS}I_{DS}$ will be used.

The extracted values are $G_0^{lin} \simeq 1.66{\times}10^{-4}\Omega^{-1}$ and $G_0^{sat} \simeq 7.38{\times}10^{-6}\Omega^{-1}$.

4.1.6 Harmonic Average with Smoothness Parameter

Having all the parameters extracted for the for linear and saturation regimes equations, we can now combine both by harmonic averaging. For this we need to introduce the smoothness parameter m.

An extracted value of m = 3.80 according to the method described in section 3.2.3 will be used.

Since the I_{OFF} value will be applied in both terms of equation 2.5, an I_{OFF}^{total} will be used instead for when $V_{GS} < V_{ON}$.

$$I_{OFF}^{total} = \left(2 \times (I_{OFF})^{-m}\right)^{-1/m} \tag{4.1}$$

4.2 Unified Model Fitting Results

Now that we have all the required parameters for the unified model, represented in table 4.1, we can draw the curves obtained by the model and compare them with the measured ones.

Table 4.1: Unified model extracted parameters.

Physical			
Parameters		Values	Units
ΔL		-30.86	μm
R_{DS}.W		0.61	Ω.m
V_{ON}		-0.1	V
I_{OFF}		4	nA
Empirical			
Parameters		Values	Units
Linear	α_{lin}	-1.21	-
	κ_{lin}	-14.47	$V^{-\alpha}$
	G_0^{lin}	1.66×10^{-4}	Ω^{-1}
Saturation	α_{sat}	-2.13	-
	κ_{sat}	-16.89	$V^{-\alpha}$
	G_0^{sat}	7.38×10^{-6}	Ω^{-1}
m		3.80	-

For a faster and user-friendly visualization method, a Matlab app was designed - screenshots can be found on Appendix B while the relevant part of the code is found on Appendix C.

Comparing the fitting using the unified model with the measured values, from figures 4.5 and 4.6 one can say the results seem very satisfying and well within what was expected.

The fact that we are using the total I_{DS} equation for linear and saturation regimes instead of the separate respective equation means that a slight deviation might be present, but this doesn't seem to influence much the final result as the relative error of the above-threshold region is below 10% in every device.

The speed Matlab processes the calculations for the model fitting is also a good indicator that the simplicity of the model will be an advantage when it comes to required processing power for circuit design and simulation.

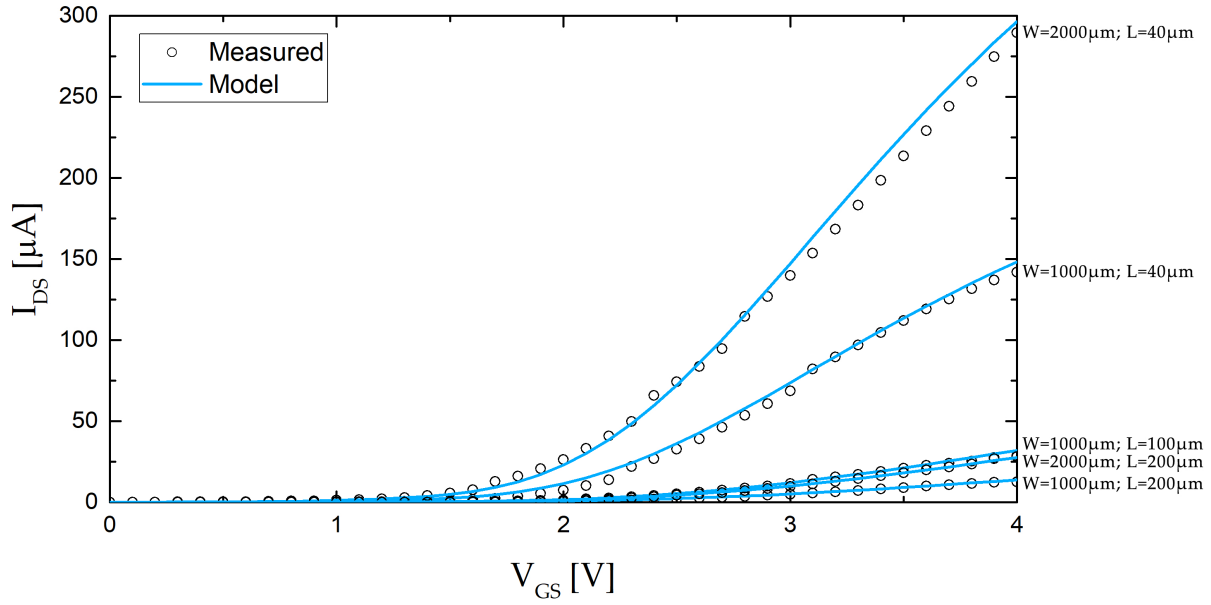


Figure 4.5: Comparison between measured characteristics for the linear regime of all five device sizes and the model applied. The circles are the measured transfer characteristics for V_{DS} = 0.2 V and the blue line the model for the same drain bias voltage.

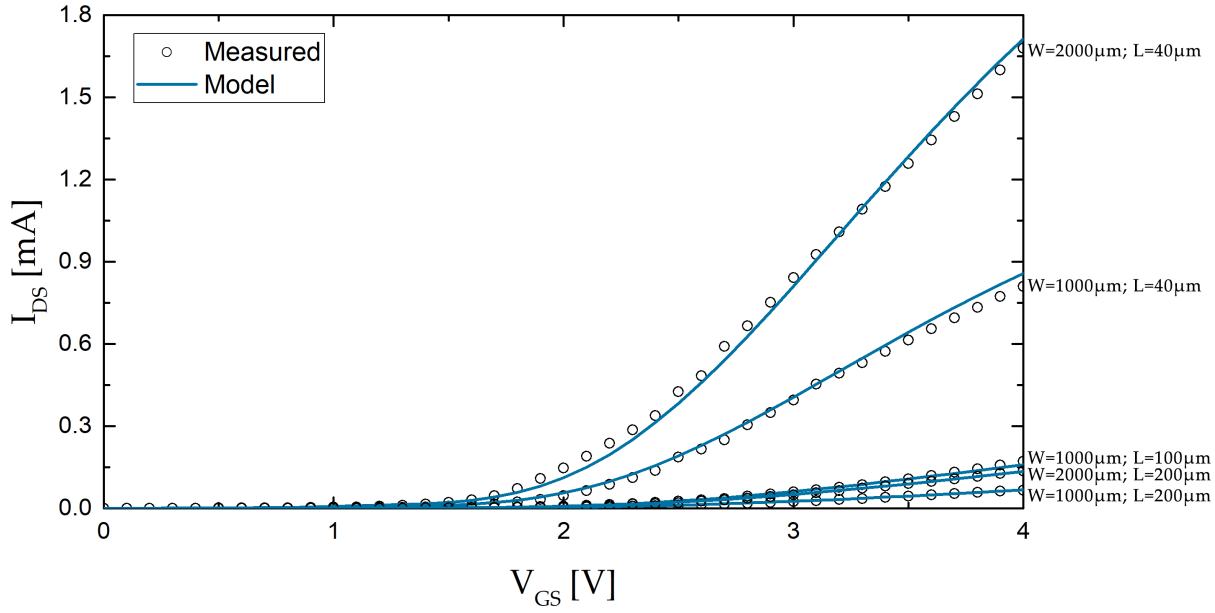


Figure 4.6: Comparison between measured characteristics for the saturation regime of all five device sizes and the model applied. The circles are the measured transfer characteristics for V_{DS} = 1.2 V and the dark blue line the model for the same drain bias voltage.

When comes to the output characteristics is where the harmonic average method seems to shine, providing a smooth transition between linear and saturation regimes as observed in figure 4.7. However, the downwards behaviour that the curve gets after reaching saturation and then a slight increase is not possible to replicate with this model and requires further study of the device's proprieties.

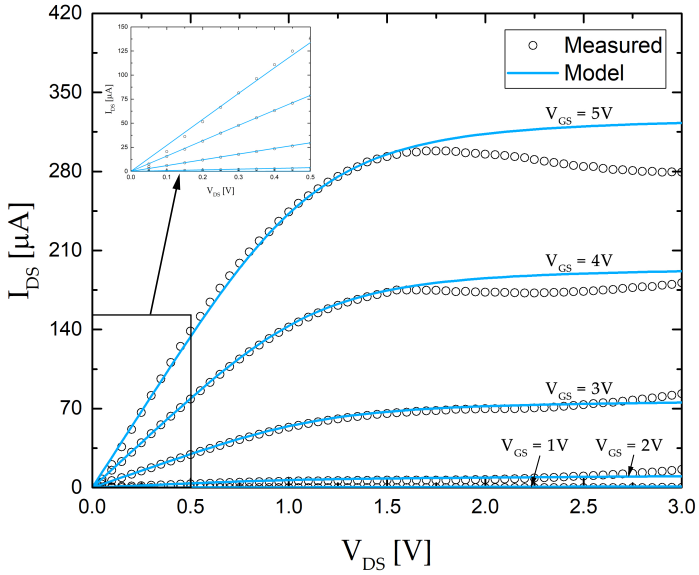


Figure 4.7: Comparison between measured output characteristics and the model applied for a device size of W ≃ 1mm and L ≃ 100μm. The circles are the measured values for five values of V_{GS} between 1 V and 5 V and the blue line the model for the same V_{GS} steps.

Overall, the results seem interesting and rather accurate for the most part. This was expected giving the heavy empirical component of the model.

4.3 Model Improvements

While the results look enough on the linear scale, when it comes to device modelling, it is highly important to make sure the model works for every operation region, and the observation of the transfer characteristics in the logarithmic scale is a good way to do this.

From figure 4.8 it is evident that the terms used in the model are not sufficient to describe the behaviour of our EGTs in the sub-threshold region.

The sub-threshold slope seems less steep in the deep sub-threshold region, a behaviour not usually found on other FET devices. A possible explanation for this phenomenon could be the EDL not being completely formed when V_{GS} is close to V_{ON}. This would result in the effective capacitance C_{ox} in the deep sub-threshold region being effectively reduced. In FET devices the sub-threshold slope is normally described by the following equation:

$$SS = \frac{\kappa_B T ln(10)}{q}\left(1 + \frac{C_t}{C_{ox}}\right) \tag{4.2}$$

where SS [V/dec] is the sub-threshold slope, κ_B is Boltzmann's constant $\simeq 1.38\times10^{-23}$ J/K, T is the absolute temperature in K, q is the elementary charge $\simeq 1.60\times10^{-19}$ C and C_t is the transition capacitance in F.

From equation 4.2 we can observe that when C_{ox} decreases, SS increases, resulting in the less steep slope near the V_{ON} region.

It is also important to note that the OFF-state region does not assume a constant value always equal to I_{OFF}, however, for the purpose of this work, it is safe to consider the OFF region as a constant I_{OFF} as it will not harm the simulations intended. This does not mean that further improvements on the model should ignore this as it is an integral part of the EGTs electrical behaviour.

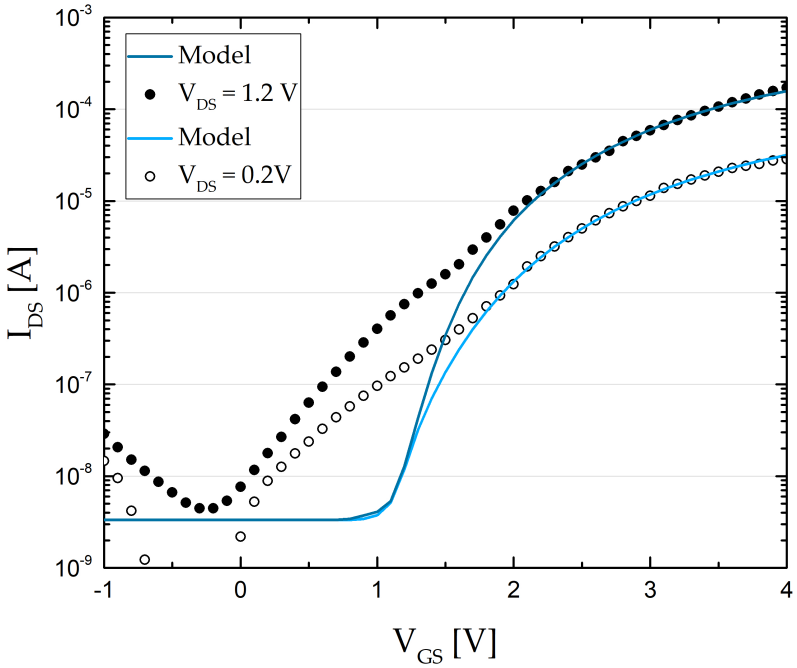


Figure 4.8: Comparison between transfer characteristics and the model applied on the logarithmic scale for a device with a size of W $\simeq$ 1mm and L $\simeq$ 100μm. The circles are the measured values of I_{DS}^{lin} while the dots are I_{DS}^{sat}. The lines are the model for the respective regime.

To improve the sub-threshold region, a new term will be added to the end of the unified model. While this may cause the model to be slower and more demanding, the improvements in accuracy will overweight the disadvantages. This new term is described by the following equation:

$$I_{DS}^{sub} = G_0^{sub}\frac{W}{L_{eff}}\left(1+tanh\left(\frac{(V_{GS}-V_{REF})log(10)}{2SS}\right)\right)\left(1-exp\left(-\frac{V_{DS}}{\eta V_{th}}\right)\right) \tag{4.3}$$

where G_0^{sub} [Ω^{-1}] and V_{REF} [V] are empirical values, SS [V/dec] is the additional sub-threshold slope, η is an ideality factor and V_{th} [V] is the thermal voltage (i.e., κ_BT/q). [36]

The new parameters were extracted by fitting and their values are represented in table 4.2

Table 4.2: New model extracted additional parameters.

Sub-threshold term		
Parameters	Values	Units
G_0^{sub}	38×10^{-9}	Ω^{-1}
V_{REF}	1.15	V
SS	0.50	V/dec
η	1	-
V_{th}	0.025	V

And the new model equation will be the total I_{DS} unified model plus the new term as shown in the following equation:

$$I_{DS}^{new} \equiv \left(\left(I_{DS}^{'lin} \right)^{-m} + \left(I_{DS}^{'sat} \right)^{-m} \right)^{-1/m} + I_{DS}^{sub} \tag{4.4}$$

4.4 Final Model Results

It is now time to test the new model from equation 4.4 and observe the results for the linear regime in figure 4.9, the saturation regime in figure 4.10.

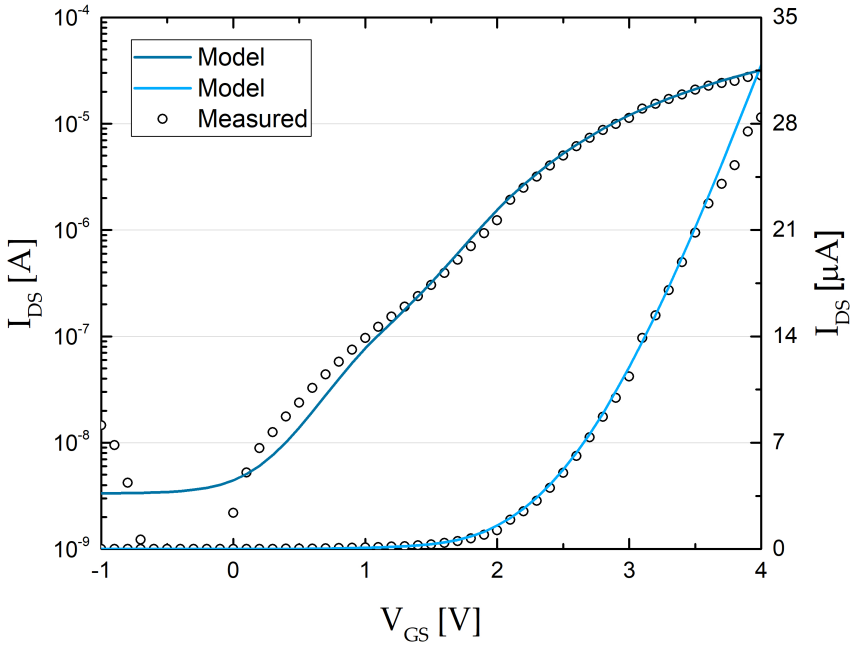


Figure 4.9: Final model on the linear regime. Linear and logarithmic scales are displayed for a device with a size of W $\simeq$ 1mm and L $\simeq$ 100μm. The circles are the measured values of I_{DS}^{lin} and the lines are the final model.

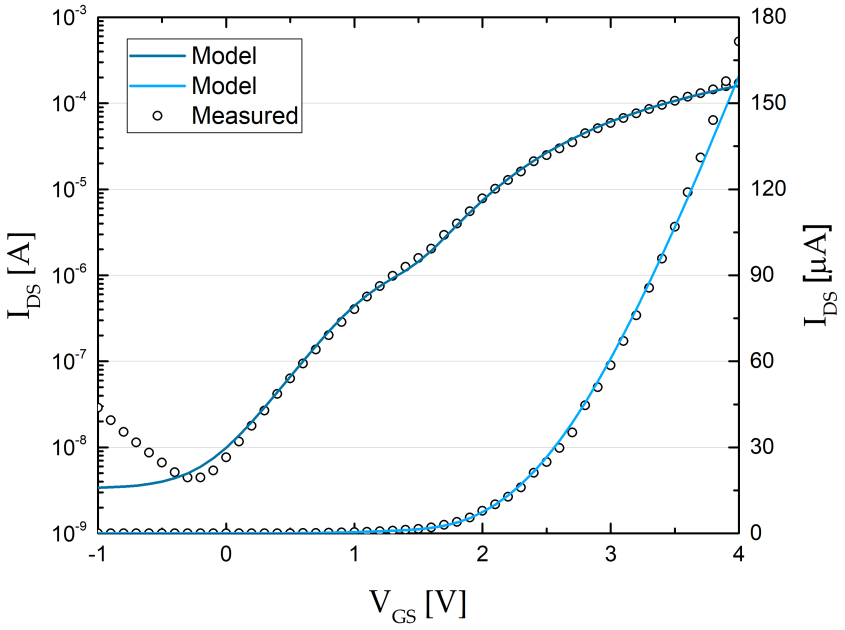


Figure 4.10: Final model on the saturation regime. Linear and logarithmic scales are displayed for a device with a size of W ≃ 1mm and L ≃ 100μm. The circles are the measured values of I_{DS}^{sat} and the lines are the final model.

It's clear that the new additional term for the sub-threshold regime makes for a much more accurate model for the EGTs in study.

The simulation speeds will not be very different for simple circuit design and we have now a relative error of 5% for the saturation regime throughout the sub and above threshold regions, and a slightly higher but still lower than 15% error on average for the linear regime as observed in figure 4.11.

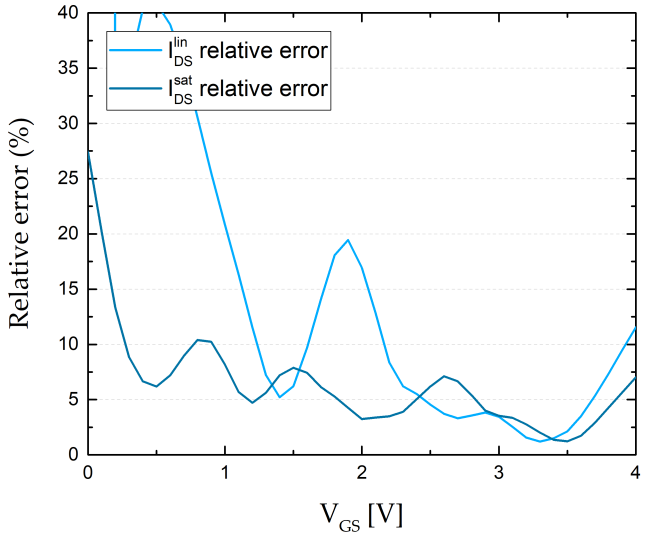


Figure 4.11: Relative error of the final model on the linear (blue line) and saturation (dark blue line) regimes.

While there is always room to improve in the future, the results obtained in this section give confidence to proceed to the next stage of this thesis project.

4.5 Circuit Simulation

The new model is now written in Verilog-A language and the code can be found on Appendix D. After writing the code, the symbol is designed and simple tests are made to prove the code for the compact model.

To create accurate simulations with more than one device, it is important to add a few extra parameters such as the $C_i = C_{DL} = 5\ \mu\text{F}/cm^2$ found in literature [20] an validated by simple C-V measurements with the devices used for the parameters extraction; and $L_{ov} = 100\mu\text{m}$ for the channel length of $L = 100\mu\text{m}$ which was used in the following simulations.

The first circuit designed was a NMOS-like inverter, as shown in figure 4.12, where the load EGT as a W/L ratio of 1:1 and the driver has a ratio of 10:1.

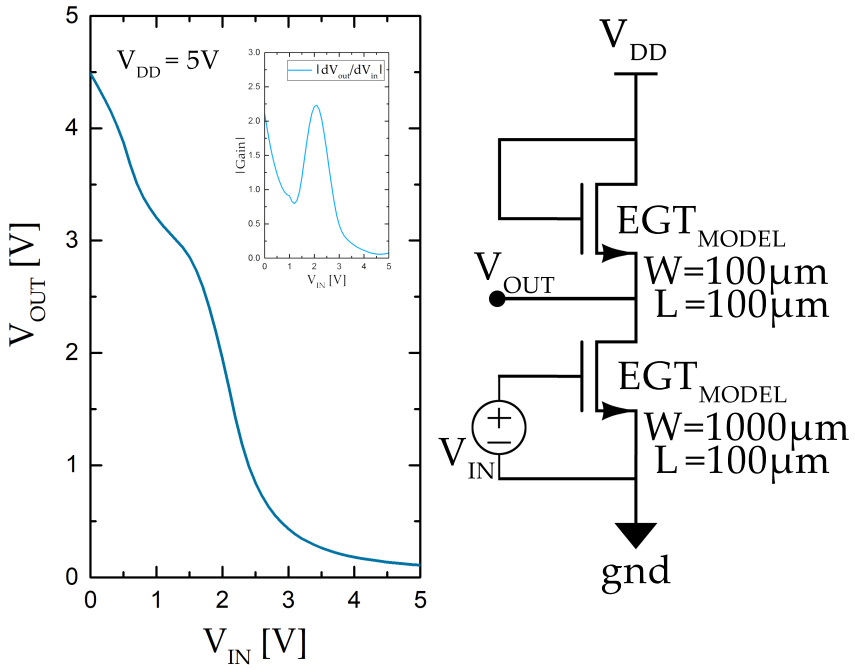


Figure 4.12: Inverter simulation on Cadence. Left is the output curve with the voltage gain in the inset; right is the schematic of the circuit.

The graph in figure 4.12 show us the transfer curve of the inverter as well as the voltage gain ($|dV_{out}/dV_{in}|$) in the inset. The absolute value of the gain is $\simeq 2.25$. As the shape of the transfer curve is somewhat inconsistent in the V_{OH} region, something expected to be related to the sub-threshold region of the transistors used, the gain value allow us to calculate the value of $V_{OH} \simeq 3.1$ V and $V_{OL} \simeq 0.1$ V. With these values, a noise margin analysis can be performed, showing results as large as $VNM_H \simeq 2$ V and $VNM_L \simeq 0.9$ V. These values mean there will be a limitation in the number of logic gates used in possible digital circuits.

After the inverter, a five stage ring oscillator was designed. The inverters used for this design are the same as the one analysed in figure 4.12 and the results and layout of the ring oscillator can be observed in figure 4.13.

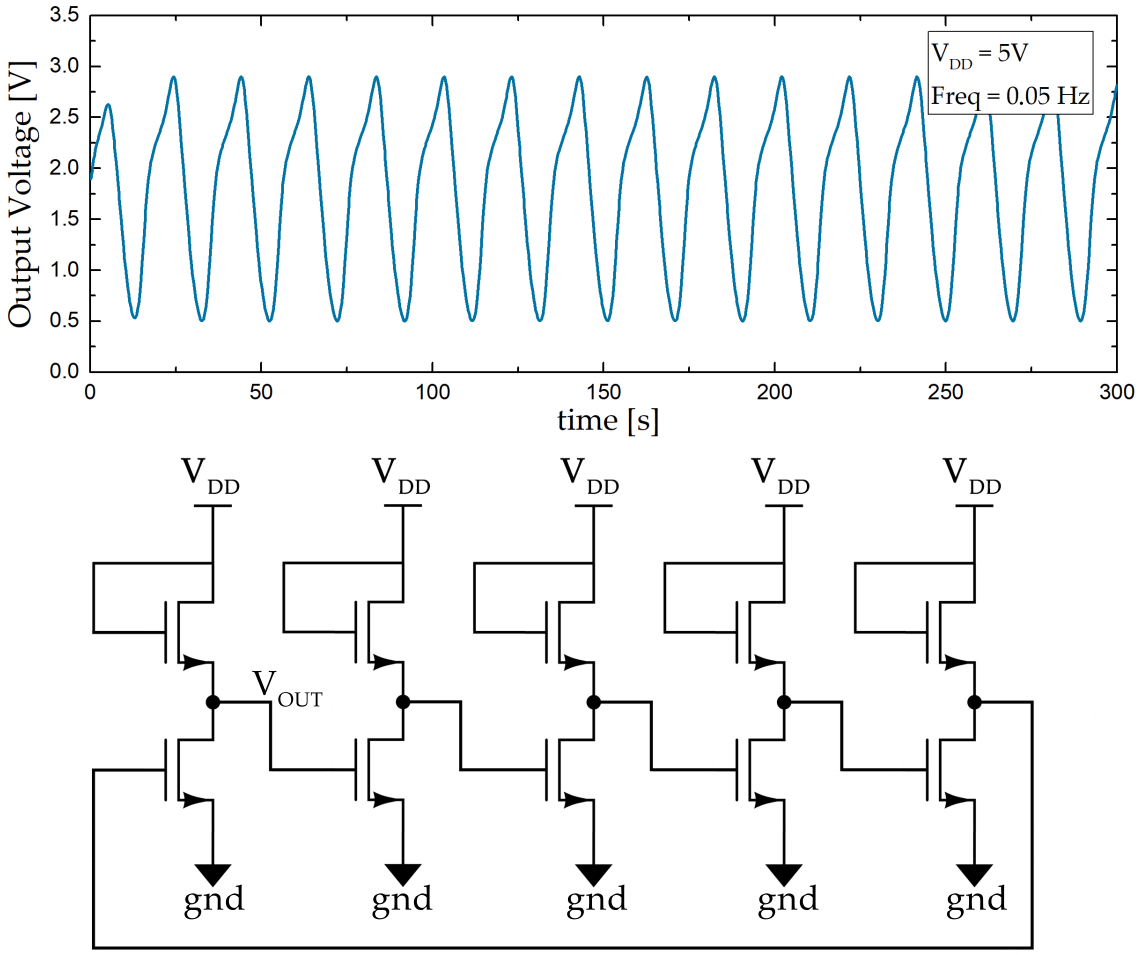


Figure 4.13: Ring oscillator simulation on Cadence. On top is the output curve; bottom is the schematic of the circuit where the top transistors have W = 100μm and L = 100μm and the bottom ones have W = 1mm and L = 100μm and V_{DD} = 5 V

Due to the low number of stages, the output curve is not a square one. This could be improved by designing a ring oscillator with more inverters, however this would lower the frequency of operation. The operation frequency shown for the 5-stage oscillator is a low 0.05 Hz for V_{DD} = 5 V. This would mean the propagation delay for the inverters used is a rather large value of around 2 seconds.

CHAPTER 5

Conclusions and Future Perspectives

The work done for this dissertation was mainly focused on the development of a compact model capable of accurately simulate the behaviour of a state-of-the-art EGT device. For this to be achieved, a better understanding of the device's electrical performance and the line of thought behind the creation of compact models needed to be acquired.

Before all of the work presented, the first step was to study the panorama of device modelling, more specifically the recent work published on TFT device modelling by the University of Cambridge and their research groups.

Models with more physical (and complex) parameters required a deep understanding of the physics and fabrication process of the device and the electrolyte and that would deviate from the goals of this thesis, so a simpler, more simulation-focused model was chosen as the starting point of the envisioned compact model.

The characterization task, which was similar for every developed model created to date, focused on the extraction of parameters from the linear regime I-V curves and a few other from the saturation and output curves. So this became the first step for the characterization of the device. Linear, saturation and output characteristic measurements were performed for the EGTs on paper substrate.

The data was analysed and the better working devices (less signal noise, continuous curves, etc.) of each size were chosen for the parameter extraction process. This task was performed giving special attention to existing literature describing the best processes to extract certain parameters on devices similar to the ones used. The R_{DS} and ΔL values are an indication that either the fabrication process can be improved or the method of extracting is not the most accurate for the EGTs in study giving their structure.

Some of the chosen physical parameters were different between devices, but in the developed model they were all used as constant values only dependent on W/L, this is certainly a cause for less accuracy in the final model. Parameters like V_{ON} seemed quite inconsistent between device sizes and it would be interesting to use different values for

different fittings however, due to expected adjustments in the sub-threshold region, there was no need to focus too much on these small details.

The unified model turned out to be more accurate than first expect, with good results (relative errors below 10%) for both the linear and saturation regimes in the above-threshold region. The sub-threshold region is where the unified model was not enough to properly model our devices, as the SS was too steep and I_{DS} was equal to I_{OFF} for too high V_{DS} value. To the lack of sub-threshold current and optimize the model, a new term was added and good results for the whole ON-State region of the device were achieved.

The first step to validate the model achieved was to implement it in Verilog-A and simulate simple circuits like an inverter and a ring oscillator. These results seemed interesting and provided enough information to let us know that the model was correctly imported into a simulation environment. However, to properly validate the conceived model, the fabrication of circuits like the ones simulated is essential and a comparison between results will provide a lot of data to further improve the model.

Using the results presented in this thesis as a starting point, the next steps for a better model for EGTs should be either of the following tasks/projects:

- Elaborate a well thought electrical characterization plan for a newer generation of CHE-EGTs with measurements on several samples of each transistor size, with the goal of obtaining a model with more physical parameters and possibly less empirical;

- Design simple circuits and then simulate and fabricate them, comparing both results in order to optimize the existing model with new empirical parameters, with the goal of obtaining a very accurate model (<5% relative error in every region) for the EGTs in study.

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APPENDIX A

EGTs Microscope Images

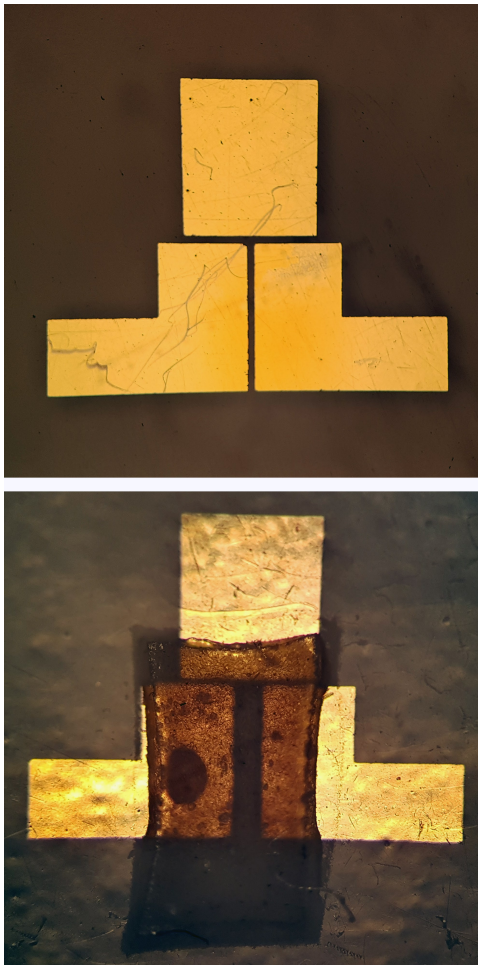

Figure A.1: Images extracted from the optical microscope. Top: EGT with W=1mm and L=40μm without CHE applied. Bottom: EGT with W=1mm and L=100μm with CHE applied.

APPENDIX B

Matlab App for Model Fitting Visualization

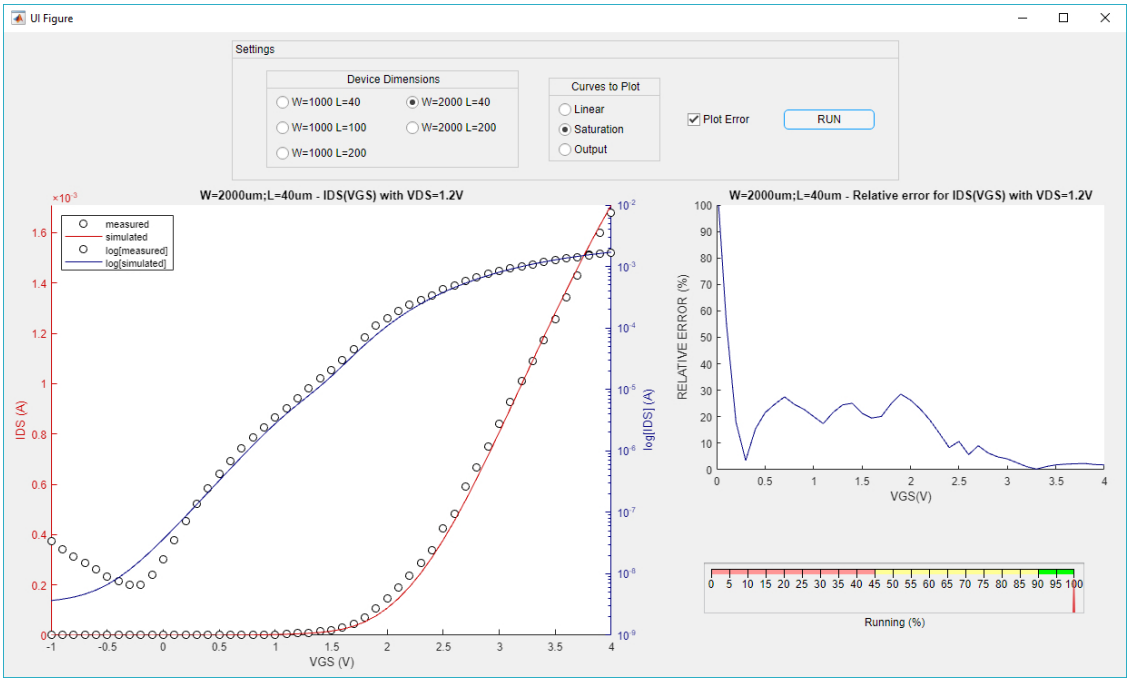

Figure B.1: Example 1 of the Matlab UI created for the model visualization

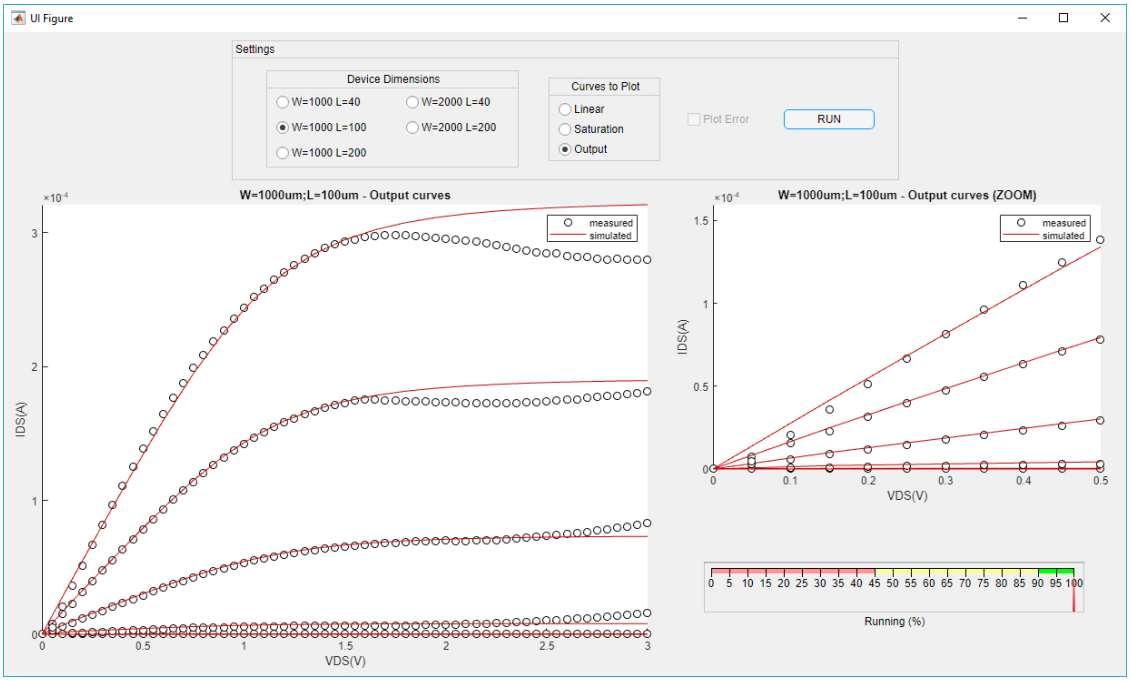

Figure B.2: Example 2 of the Matlab UI created for the model visualization

APPENDIX C

Matlab Scripts for Model Fitting Visualization

Listing C.1: RUN Button script

```
% SELECT TRANSISTOR (t)
if app.W1000L40.Value == 1
  t = 1;
elseif app.W1000L100.Value == 1
  t = 2;
elseif app.W1000L200.Value == 1
  t = 3;
elseif app.W2000L40.Value == 1
  t = 4;
elseif app.W2000L200.Value == 1
  t = 5;
end

% SELECT REGIME (c)
if app.Output.Value == 1
  curve = 1;
elseif app.Linear.Value == 1
  curve = 2;
elseif app.Saturation.Value == 1
  curve = 3;
end

%%%%%%%%%%%%%%%%%%%%%%%% MODEL PARAMETERS %%%%%%%%%%%%%%%%%%%%%%%%
%% EMPIRICAL
% LINEAR
ALIN  = (-1.21238);
KLIN  = (-14.47242);
GOLIN = (1.65605E-4);
% SATURATION
```

```
ASAT  = (-2.13085);
KSAT  = (-16.89114);
GOSAT = (7.38033E-6);
% SUBTHRESHOLD ADJUSTMENT PARAMETERS
GOSUB = 38E-9;
VREF = 1.15;
SS = 0.5;
n=1;
Vth=0.025;
%% PHYSICAL
% DIMENSIONS AND CONTACT
RDSW = 0.60955;
w = [1000E-6;1000E-6;1000E-6;2000E-6;2000E-6];
W = w(t);
l = [40E-6;100E-6;200E-6;40E-6;200E-6];
L = l(t);
dL = -3.08586E-5;
Leff = L+dL;
RDSW = 0.60955;
RDS = RDSW/W;
% ON/OFF
VON = -0.1;
IOFF = 4E-9;
% SMOOTHNESS PARAMETER
m = 3.8;
% IOFF ACCOUNTING FOR m
IOFFtotal = ((IOFF^-m)*2)^(-1/m);
% COLORS FOR GRAPHS
black = [0 0 0];
red = [.8 0 0];
blue = [0 0 .5];
% DEFINE i FOR LATER
i=1;

%%%%%%%%%%%%%%%%%%%%%%%%%% FITTINGS %%%%%%%%%%%%%%%%%%%%%%%%%%
%% OUTPUT
if curve == 1
  % LOAD MEASUREMENTS
  DEVICESOUT = xlsread('output.xls',t);
  Vdsmea = DEVICESOUT(1:61,1);
  % SETUP FIGURES
  % MAIN
  app.figure1.Visible = 1;
  title(app.figure1,['W=' num2str(W*1E6) 'um;L=' num2str(L*1E6) 'um - Output
      curves']);
  xlabel(app.figure1,'VDS(V)');
  ylabel(app.figure1,'IDS(A)');
  xlim(app.figure1,[0 3]);
  ylim(app.figure1,[0 inf]);
  % CLOSE UP
```

```
79    app.figure2.Visible = 1;
80    title(app.figure2,['W=' num2str(W*1E6) 'um;L=' num2str(L*1E6) 'um - Output
          curves (ZOOM)']);
81    xlabel(app.figure2,'VDS(V)');
82    ylabel(app.figure2,'IDS(A)');
83    xlim(app.figure2,[0 0.5]);
84    % SET IDS ARRAY
85    ids=zeros(21,5);
86    % 5 CURVES FOR DIFFERENT VG
87    for z = 1:5
88      vgs = [1;2;3;4;5];
89      VGS = vgs(z);
90      Idsmea = DEVICESOUT(1:61,VGS+1);
91      % JUST 21 POINTS FOR FASTER FIGURES
92      for i = 1:21
93        VDS = 0.15*(i-1);
94        vds(i) = VDS;
95        ids(i) = IDStotal(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,GOSAT,KSAT,ASAT
              ,IOFF,VREF,GOSUB,SS,n,Vth,m);
96        % LOADING BAR
97        app.RunningGauge.Value = 20*(z-1)+(i*20)/21;
98        pause(0.00001)
99      end
100     % PLOT MEASURED AND CALCULATED
101     % MAIN FIGURE
102     hold(app.figure1);
103     plot(app.figure1,Vdsmea,Idsmea,'o','color',black);
104     plot(app.figure1,vds,ids,'color',red);
105     hold(app.figure1);
106     legend(app.figure1,'measured','simulated');
107     % CLOSE UP
108     ylim(app.figure2,[0 ids(5)]);
109     hold(app.figure2);
110     plot(app.figure2,Vdsmea,Idsmea,'o','color',black);
111     plot(app.figure2,vds,ids,'color',red);
112     hold(app.figure2);
113     legend(app.figure2,'measured','simulated');
114     pause(0.0001)
115   end
116
117 %% TRANSFER
118 else
119   % LOAD MEASUREMENTS
120   DEVICES = xlsread('transfer.xls',t);
121   Vgsmea = DEVICES(1:61,1);
122   Idsmea = DEVICES(1:61,curve);
123   % DEFINE VDS FOR LINEAR AND SATURATION
124   VDSreg = [0;0.2;1.2];
125   VDS = VDSreg(curve);
126   % ARRAYS
```

```
127   ids=zeros(61,1);
128   vgs=zeros(61,1);
129   % SHOW MAIN FIGURE
130   app.figure1.Visible = 1;
131   app.figure2.Visible = 0;
132   % SETUP FIGURES
133   % X AXIS
134   title(app.figure1,['W=' num2str(W*1E6) 'um;L=' num2str(L*1E6) 'um - IDS(VGS)
          with VDS=' num2str(VDS) 'V']);
135   xlim(app.figure1,[-1 4]);
136   xlabel(app.figure1,'VGS (V)');
137   ylim(app.figure1,[0 inf]);
138   % LEFT AXIS LINEAR SCALE
139   yyaxis (app.figure1,'left')
140   app.figure1.YColor = red;
141   ylabel(app.figure1,'IDS (A)');
142   % RIGHT AXIS LOG SCALE
143   yyaxis (app.figure1,'right')
144   app.figure1.YScale = 'log';
145   app.figure1.YColor = blue;
146   ylabel(app.figure1,'log[IDS] (A)');
147   % PLOT MEASURED
148   % LINEAR SCALE
149   yyaxis (app.figure1,'left')
150   plot(app.figure1,Vgsmea,Idsmea,'o','color',black);
151   % LOG SCALE
152   yyaxis (app.figure1,'right')
153   plot(app.figure1,Vgsmea,Idsmea,'o','color',black);
154   hold(app.figure1)
155   % 61 POINTS (NEEDED FOR ACCURATE ERROR BELOW - IF SELECT)
156   while i<62
157     VGS = -2+0.1*(i-1);
158     vgs(i,1) = VGS;
159     % OFF REGIME
160     if VGS < VON
161       ids(i,1) = IOFFtotal+IDSsub(W,Leff,VGS,VDS,VREF,GOSUB,SS,n,Vth);
162     % LINEAR REGIME
163     elseif curve == 2
164       ids(i,1) = IDStotal(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,GOSAT,KSAT,
              ASAT,IOFF,VREF,GOSUB,SS,n,Vth,m);
165     % SATURATION REGIME
166     elseif curve == 3
167       ids(i,1) = IDStotal(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,GOSAT,KSAT,
              ASAT,IOFF,VREF,GOSUB,SS,n,Vth,m);
168     end
169     % LOADING BAR
170     app.RunningGauge.Value = (i*100)/61;
171     i = i + 1;
172     pause(0.00001)
173   end
```

```
  % PLOT CALCULATED
  % LINEAR SCALE
  yyaxis (app.figure1,'left')
  plot(app.figure1,vgs,ids,'color',red);
  % LOG SCALE
  yyaxis (app.figure1,'right')
  semilogy(app.figure1,vgs,ids,'color',blue);
  % DRAW LEGEND
  legend(app.figure1,'Location','northwest');
  legend(app.figure1,'measured','simulated','log[measured]','log[simulated]');
  % ERROR
  if app.PlotError.Value == 1
    % ARRAY FOR ERROR AND DEFINE e
    error = zeros(61,1);
    e = 1;
    % SETUP FIGURE
    app.figure2.Visible = 1;
    title(app.figure2,['W=' num2str(W*1E6) 'um;L=' num2str(L*1E6) 'um -
        Relative error for IDS(VGS) with VDS=' num2str(VDS) 'V']);
    xlim(app.figure2,[0 4]);
    ylim(app.figure2,[0 100]);
    xlabel(app.figure2,'VGS(V)');
    ylabel(app.figure2,'RELATIVE ERROR (%)');
    % ERROR FOR EVERY POINT (NOTE: SOME NOT SHOWN - CHECK FIGURE SETUP)
    while e < 62
      error(e,1)=abs((Idsmea(e,1)-ids(e,1))/Idsmea(e,1))*100;
      e=e+1;
      % PLOT ERROR
      plot(app.figure2,Vgsmea,error,'color',blue);
      pause(0.00001);
    end
  end
end
```

Listing C.2: I_{DS}^{lin} script

```
function IDSlin = IDSlin(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,IOFF)
syms IDSeqn
eqn = -IDSeqn+GOLIN*(W/Leff)*(exp(KLIN*(VGS-VON)^(ALIN)))*(VDS-RDS*IDSeqn)+
    IOFF==0;
IDSlin = vpasolve(eqn,IDSeqn);
end
```

Listing C.3: I_{DS}^{sat} script

```
function IDSsat = IDSsat(W,Leff,VGS,VON,GOSAT,KSAT,ASAT,IOFF)
syms IDSeqn
eqn = -IDSeqn+GOSAT*(W/Leff)*(exp(KSAT*(VGS-VON)^(ASAT)))*(VGS-VON)+IOFF==0;
IDSsat = vpasolve(eqn,IDSeqn);
end
```

Listing C.4: I_{DS}^{sub} script

```
function IDSsub = IDSsub(W,Leff,VGS,VDS,VREF,GOSUB,SS,n,Vth)
syms IDSeqn
eqn = -IDSeqn+GOSUB*(W/Leff)*(1+tanh(((VGS-VREF)*log(10))/(2*SS)))*(1-exp(-VDS
    /(n*Vth)))==0;
IDSsub = vpasolve(eqn,IDSeqn);
end
```

Listing C.5: I_{DS}^{total} script

```
function IDStotal = IDStotal(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,GOSAT,KSAT
    ,ASAT,IOFF,VREF,GOSUB,SS,n,Vth,m)
syms IDStot
%LIN
IDS_L=IDSlin(W,Leff,VGS,VON,VDS,RDS,GOLIN,KLIN,ALIN,IOFF);
%SAT
IDS_S=IDSsat(W,Leff,VGS,VON,GOSAT,KSAT,ASAT,IOFF);
%SUB
IDS_SUB=IDSsub(W,Leff,VGS,VDS,VREF,GOSUB,SS,n,Vth);
%FINAL
eqn=-IDStot+(((IDS_L)^(-m)+(IDS_S)^(-m))^(-1/m))+IDS_SUB==0;
IDStotal=vpasolve(eqn,IDStot);
end
```

APPENDIX D

Final Model Verilog-A Code

Listing D.1: Verilog-A code

```
// VerilogA for nunolib, test, veriloga

`include "constants.vams"
`include "disciplines.vams"

module nunounifiedmodel(d,g,s);
//
// Node definitions
//
        inout           d,g,s ;   // external nodes
        electrical      d,g,s ;   // external nodes
//
//*** Local variables
//
real Leff, RDS;
real VG, VS, VD;
real IDLIN, IDSAT, IDSUB, alplin, alpsat, linM, satM, Id, I_sign, Qs,
    Qd;
//
//*** model parameter definitions
//
parameter real L      =  100E-6      from[0.0:inf];
parameter real W      =  1000E-6     from[0.0:inf];
parameter real deltaL =  -3.08586E-5;

//***  ON voltage
parameter real VON    =  -0.1;
parameter real IOFF   =  4E-9    from[0.0:inf];

```

```
29 //***  Model parameters
30 parameter real ALPHALIN =  -1.21238;
31 parameter real KLIN     =  -14.47242;
32 parameter real GOLIN    =  1.65605E-4 from[0.0:inf];
33 parameter real ALPHASAT =  -2.13085;
34 parameter real KSAT     =  -16.89114;
35 parameter real GOSAT    =  7.38033e-6 from[0.0:inf];
36 parameter real RDSW     =  0.60955    from[0.0:inf];
37 parameter real M        =  3.8        from[0.0:inf];
38 parameter real GOSUB    =  3.8e-8;
39 parameter real VREF     =  1.15; //vref for subthreshold regime
40 parameter real SS       =  0.5;  // V/dec
41 parameter real vth      =  0.0258;
42 parameter real n        =  1;
43 parameter real Ci       =  5*10^-2; F/m^2
44 parameter real Lov      =  100e-6;
45
46 analog begin
47
48 Qs=-Ci*Lov*W*V(g,s);
49 Qd=-Ci*Lov*W*V(g,d);
50
51 VD = V(d,s);
52 if (VD > 0) begin
53         VG = V(g,s);
54         VD = V(d,s);
55         I_sign=1;
56         //id = ID_func(vg, vd);
57 end
58 else begin
59         VG = V(g,d);
60         VD = V(s,d);
61         I_sign=-1;
62         //id = -ID_func(vg, vd);
63 end
64
65 Leff = L + deltaL;
66 RDS = RDSW/W;
67
68 if (VG-VON>0) begin
69 // LINEAR REGIME
70
71 alplin = pow((VG - VON),ALPHALIN);
72 IDLIN = GOLIN * (W/Leff) * (exp( KLIN * alplin )) * (VD - RDS*IDLIN) +
       IOFF;
73
```

```
74  // SATURATION REGIME
75
76  alpsat = pow((VG - VON),ALPHASAT);
77  IDSAT = GOSAT * (W/Leff) * (exp( KSAT * alpsat )) * (VG - VON) + IOFF;
78
79  end
80  else begin
81
82  IDLIN=IOFF;
83  IDSAT=IOFF;
84
85  end
86
87  //ADDED SUBTHRESHOLD REGIME
88
89  IDSUB = GOSUB * (W/Leff) * (1+tanh((VG-VREF)*ln(10)/2/SS)) * (1-exp(-
        VD/n/vth));
90
91  //ID equation
92  linM = pow(IDLIN, -M);
93  satM = pow(IDSAT, -M);
94  Id = I_sign*(pow((linM + satM),(-1/M))+IDSUB);
95
96  I(d,s) <+ Id;
97  I(g,s) <+ ddt(Qs);
98  I(g,d) <+ ddt(Qd);
99
100 end
101 endmodule
```