Rodrigo da Silva Mendes Fraústo

Licenciado em Ciências da Engenharia Electrotécnica e de Computadores

RF CMOS Transmitter Front-end with Output Power Combiner

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Orientador: Prof. Dr. João Pedro Abreu de Oliveira, Prof. Auxiliar, Universidade Nova de Lisboa

Júri

Presidente:	Prof. Dr. Rodolfo Alexandre Duarte Oliveira
Arguente:	Prof. Dr. Luís Augusto Bica Gomes de Oliveira
Vogal:	Prof. Dr. João Pedro Abreu de Oliveira

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

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"Uma vida a correr atrás do prejuízo"

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Abstract

In this thesis strategies to achieve a high efficiency RF front-end are studied and presented. A high efficiency Power Amplifier is also proposed and simulated.

The applications for this type of designs are vast, but the main ones are in mobile transmission devices where the only power supply source available is a battery.

In order to perform this thesis several topologies of power amplifiers were studied, and the decision fell to those based on a switching behavior. The reason for this decision was the need for high efficiency (it's one of the main objectives).

The Class-D power amplifier with its ideal potential efficiency of 100% has proven the most promising for implementation. The objectives for this thesis in terms of implementation were an efficiency of 20% and an output power of $0dBm$.

Finally, a power-combining technique was used to explore the potential of achieving high output power without affecting the efficiency.

Keywords: Class-D, RF power amplifier, CMOS, drain efficiency, radio-frequency, switching circuits.

Resumo

Esta tese tem por objectivo o design de um RF front-end de alta eficiência. As utilizações deste tipo de sistemas são vastas, mas as principais incidem sobre dispositivos de transmissão móveis onde a única fonte de alimentação disponível é uma bateria.

Para a realização desta tese diversas topologias de amplificadores de potência foram estudadas, sendo que a decisão tomada foi para as que se apresentam como classes comutadas, visto a alta eficiência ser um dos objectivos.

O amplificador de potência Classe-D com a sua ideal eficiência de 100% apresentou-se como o mais promissor para implementação. Os objectivos pretendidos eram de uma eficiência de 20% e uma potência de saída de $0dBm$.

Por fim uma técnica de combinação de potência foi utilizada para explorar as potencialidades de conseguir uma alta potência de saída sem afectar em demasia a eficiência.

Palavras-chave: Classe-D, amplificador de potência RF, CMOS, eficiência de dreno, radiofrequência, circuitos comutados.

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Acronyms

BLE	Bluetooth low energy.
DAC	Digital to analog converter.
PA	Power amplifier.
PAE	Power Added Efficiency.
QPSK	Quadrature Phase-shift keying.

Chapter 1

Introduction

1.1 Background and Motivation

With the evolution of times, communication has become essential in our lives and technologies. Whether in the way we communicate with each other, using increasingly competent mobile devices, or in the way in which the machines and technologies, that are developed, communicate with each other. The need to create a network where multiple devices/machines can communicate with each other, make decisions together or collect data without the need for complex installations has become evident, for example, we can look at the next industrial revolution (industry 4.0) where cybernetic systems create a virtual representation of the real world in order to make decisions in real time and to be totally modular. This allows to look at this type of systems without seeing them as a single unit, but as a set of modules that form an end product.

Another example of the need for wireless communication is in IoT where common everyday devices can communicate and connect to the Internet, making them more productive and effective.

Taking into account these factors, another concept that became essential, due to the reduced dimensions of many devices and the need for autonomy, was the low power consumption without affecting the functionality.

The essential part of a wireless communication is the emission and reception of a signal that contains information. In this thesis the transmission part is addressed. A high efficiency RF front-end propose and design is presented.

The RF front-end is designed to use in an application where low power is supplied but a need for a high output power exists.

Not only power amplifier classes are studied, but also techniques for achieving a high output power maintaining the high efficiency.

1.2 Thesis Organization

The presented thesis is organized in six chapters including the introduction. The thesis organization is as follows:

Chapter 2 - Units of measurement and Strategies to achieve high power output CMOS PAs In this chapter the units of measurement and combining techniques are addressed. The idea behind it is to give a base knowledge to the thesis reader. Watt output power achieving techniques will be also discuss.

Chapter 3 - RF transmission an Overview In chapter 3 many classes of power amplifiers are presented. The classes are distributed between two groups and the distinction is made between them. Each class is briefly described. The main features of the RF amplifiers, as the output power and the efficiency, are described. The most used transmitter topologies are also presented and described.

Chapter 4 - Inverter-Based Class-D Power amplifier In this chapter the inverter base Class-D amplifier will be presented. The starting point is the CMOS transistor as a switch, then a study of the inverter circuit is made, ending with the fully Class-D description and analysis. Gate driving and power combining transformers are also addressed.

Chapter 5 - Inverter-Based Class-D Power amplifier with power combiner, Design and simulation The chapter 5 is the design and simulation of the proposed amplifier. The results are showed not only with the Class-D working in a standalone application but also with a power combiner.

Chapter 6 - Conclusion and Future work In this chapter the conclusions and future work are presented.

Chapter 2

Units of measurement and Strategies to achieve high power output CMOS PAs

This chapter aims at giving some simple context to this thesis in terms of a better understanding of the measuring units. Efficiency is a term that seems to be obvious, it's used in a variety of situations to describe a system behavior in terms of power consumption when in relation to the output power that the system can achieve. When we talk about an RF power amplifier, efficiency has a similar meaning to what we are used to define in other applications. The only thing that changes is the power amplifier overall efficiency where this factor is not only calculated using the power supplied to the PA but also with the input control signal power. This definitions will be discussed in this chapter.

Another important point is the understating of how to achieve high output power. High efficiency doesn't always mean that a system have a low power consumption. In the PA case, we are speaking about an application that in the majority of times is portable (with a battery) so not only the efficiency is important but also the power consumption. This chapter will also introduce some concepts in how to achieve a high power output without affecting in a major way the efficiency and power consumption of the system.

2.1 Amplifier Efficiency

When we talk about the efficiency of a power amplifier the easiest way to measure it is to get the power that is given by the PA to the load and divide this value with the power that is given by the power supply to the PA. This type of measure is called the drain efficiency and it's the most common and easy way to denote the efficiency of the power amplifier. Drain efficiency is defined by the expression 2.1.

$$\eta = \frac{P_{load}}{P_{(DC)}} \tag{2.1}$$

Looking at a PA design from any class or application, we see that this type of measure is not really representing the complete system and could lead to a wrong conclusion about the performance in terms of efficiency. So a better way to perform this measure is to take in count all the parts of the system. The name of this strategy to measure the efficiency of the PA is called the Power Added Efficiency (PAE). This measure consists in taking into consideration all the parts of the power amplifier, or by other words, not only the power drawn by the PA but also the power drawn by the driving stages and the difference between the output power and the input power. The equation that represents the PAE is 2.2.

$$\eta = \frac{P_{load} - P_{in}}{P_{(PA)} + \sum_{n=1}^{\infty} P_{(D_n)}} \tag{2.2}$$

2.2 Output Power

Output Power is an expression that almost characterizes itself in any application where its used. Being this thesis central topic a Power amplifier, the explanation will be centered on what this expression means for RF power amplifiers.

In a simple phrase output power can be defined as the active power delivered by the power amplifier which flows into the antenna [1]. This power is transmitted under the form of a radiated electromagnetic wave. In antenna design, besides the direction and type of waves, the engineer will, in most cases, create the antenna to be resistive at any frequency of interest. That being said, we can easily imagine the antenna as a resistive load (it is common to design antennas with 50ω of impedance, but the reality is that this value is not true in all cases so the calculations will be in a general case). Starting with the basics, we define instant output power as the voltage times current at any given moment, so we can define the total or average output power by equation 2.3.

$$Po = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} p_o(t)dt \tag{2.3}$$

If we define the output voltage as a simple sine wave with the frequency f_c and the period T_c, we get 2.4

$$Po = \frac{1}{T_c} \int_{-T_c/2}^{T_c/2} p_o(t)dt \tag{2.4}$$

And if we assume the antenna as a resistive load, and define <.> as the time average operator, we can calculate the output power as 2.5

$$Po =< v_{out}(t) \cdot i_{out}(t) >= \frac{< v_{out}^2(t) >}{R_L} = \frac{V_{o,rms}^2}{R_L} \tag{2.5}$$

being $V_{o,rms}^2$ defined as 2.6

$$V_{o,rms}^2 = \sqrt{< v_{out}^2(t) >} \tag{2.6}$$

This textbook triviality is not always as useful for a power amplifier as it may look, in reality the power amplifier is not only generating power in the fundamental frequency f_c but also in its harmonics (that's why in most cases a strategy is implemented to filter all the undesired frequency's in order to eliminate the not needed power dissipation). This being said, its more useful to define a fundamental average output power 2.7, where we only take in consideration the fundamental frequency.

$$Po = \frac{V_o^2}{2R_L} \tag{2.7}$$

being V_o the amplitude of the sinusoidal output voltage of the fundamental frequency. This value can be obtained from a Fourier Series expansion of $v_{out}(t)$ [1].

2.3 Strategies to achieve high power output CMOS PAs

When we talk in a high efficiency PA we presume a low power consumption. This affirmation is not always true, because efficiency does not mean that a system will have a low power consumption, it means that regardless of consumption, the system will have a power output with a ratio close to 1 with its input power. We see that, if we need a solution where the system have a low power consumption, but also a high output power need, some kind of strategy has to be implemented. Some strategy's can be used to perform this task, the next ones are a collection of them.

Table 2.1: Comparison between PA classes in terms of peak drain voltage and maximum output power [2]

Class	Peak drain voltage	Fundamental tone peak drain current	Maximum output power
Linear PAs	$2 * Vdd$	$\frac{2*Vdd}{R}$	$\frac{Vdd^2}{2R}$
Class D	Vdd	$\frac{Vdd}{R}$	$\frac{(\frac{2}{\pi}Vdd)^2}{2R}$
Class E	$3.6 * Vdd$	$\frac{1.7*Vdd}{R}$	$\frac{0.577*Vdd^2}{R}$
Class F	$\frac{8*Vdd}{\pi}$	$\frac{8*Vdd}{\pi R}$	$\frac{(\frac{4}{\pi}Vdd)^2}{2R}$

2.3.1 Increase Supply Voltage

This strategy is the easiest to think about, if we need high output power, then we supply more power at the PA entry. If we look at equation 2.7 we see that more voltage supplied will increase the power output capabilities of the device. But we have to remember the technology that we are working with, modern nm-CMOS are limited in the maximum allowed supply voltage [3].

There are two reasons for that, the first one is because of low device breakdown voltages [4] and the second one reliability concerns [5]. As a PA, most classes will generate

peak voltages superior to the supplied voltage, so the device breakdown voltage needs to be (depending on the PA class) two, tree or four times bigger. Also, some margin its needed to prevent a failure in the device in case of voltage output peaks (common in handling or mismatch conditions) [3].

2.3.2 Power combining

Another strategy used to increase the power output without the concerns of a higher supply voltage is to use an old method to solve complex problems, divide and conquer. The idea behind it is, rather than use a "big"PA, why not use low power output, high efficiency PAs combined in order to achieve the watt level power output [6].

2.3.2.1 Differential PA architecture

By increasing the size of the PA output transistor, power will increase also, but the impedance scales equally to lower values turning sometimes impossible to conveniently convert it to 50Ω [3]. We can bypass this issue using a differential architecture. Basically the signal will be split into two antiphase paths using a balun or transformer, where two similar PA (half-size) blocks are used, and the signal is merged at the power amplifier output using the same technique [3].Thus, if the PA is not differential, in that case the signal can be directly fed to and from the power amplifier. There will be losses in the slip-merging process, but we still be able to have a gain of output power.

2.3.2.2 On-Chip Transformers

The real solution for big output CMOS PAs reside in one simple strategy, combine the power of n elements using an on-chip transformer [3]. The transformer combination structures are categorized in two principal categories, series-combining transformers (Voltage-mode) 2.1, that combine the AC voltages on the secondary side resulting in a high output power, or in parallel-combining (current mode) [7].

The big advantage of using the series-combining transformer is that the impedance seen by each amplifier is n times larger than what would be if connected directly to the antenna. This is a very advantageous situation for the driver design.

The advantages of using parallel-combining transformers are less losses on the secondary, and a better signal symmetry (which is also very important in current-mode transformers to avoid a mismatch and consequentially reduction of power output). The problem is that the number of turns with this approach becomes larger on the secondary side, increasing the area and lowering the self-resonance frequency. Two examples can be found in the literature regarding the two strategy's, for current mode transformers we have Aoki *et al.* approach [8] , and for voltage-mode transformers we have the A. Afsahi and L. E. Larson approach [9].

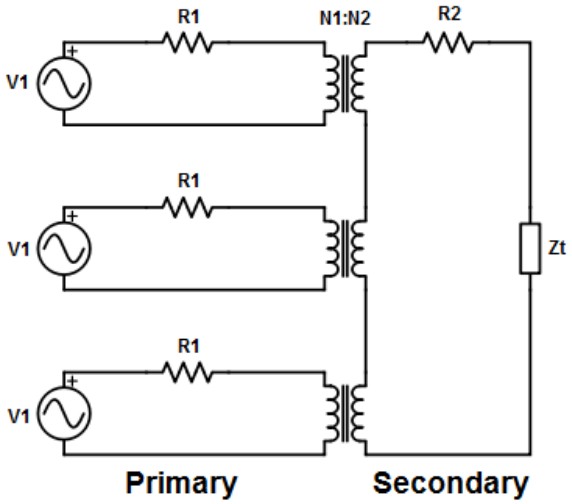


Figure 2.1: Voltage-mode transformer.

Chapter 3

RF transmission an Overview

At its core this thesis is the application of various concepts in the design of an RF transmitter front-end, so it's very important to understand what is at stake in this task. This chapter has the intention of providing to the reader a better understanding of the theory behind this thesis.

In a first approach it is important to understand the architecture of a transmitter and the difference between direct-conversion transmitters and heterodyne transmitters, not only in performance but also in design challenges and inherent problems that each one of them has. Also the concept of digital direct-conversion is introduced to give a theoretical basis about the architecture that will be used in this thesis.

The most critical component of the transmitter is also introduced in this chapter, the power amplifier. The various classes of this device will be studied, and most important the advantages of each one, for a better understanding of the decision to use a Class-D amplifier on this thesis.

Another subject that is introduced are strategies for achieving a High Output Power with integrated CMOS PA, for an understanding of the reason to choose a differential architecture to achieve this specification.

3.1 Transmitter Architectures

The transmission of a wireless signal, although complex in practice, is presented as simple in theory and reasoning. Everything starts with the conversion of a digital signal into an analog signal. This is done by a block called Digital to analog converter (DAC), this block will therefore be the starting point in the transmission chain. This converted signal lies in the baseband or in other words, at an intermediate frequency that depending on the modulation, will be different than desired. Thus, it will be necessary to translate this

wave into another of a different frequency, usually higher. This process can be realized through several techniques, which include analog mixing, direct digital conversion and a combination of the two.

Using analog mixing up-conversion as an example, the block used to perform this translation is called a Mixer, it uses a multiplication operation between a rectangular wave coming from an oscillator at the desired RF frequency and the wave at the baseband from the DAC.

At the end of the transmitting chain is the element responsible for amplifying the signal in terms of power so that it is transmitted by the antenna. The name of this block is descriptive of its function: power amplifier. The RF transmitter has three main tasks: modulation, up-conversion and power amplification.

3.1.1 Heterodyne Transmitter

This type of transmitters (Fig. 3.1) performs the I/Q up-conversion from the baseband to the desired RF band in two stages. The first one consists in the translation of the baseband signal to an intermediate frequency IF which we call ω_1. The second stage consists in the

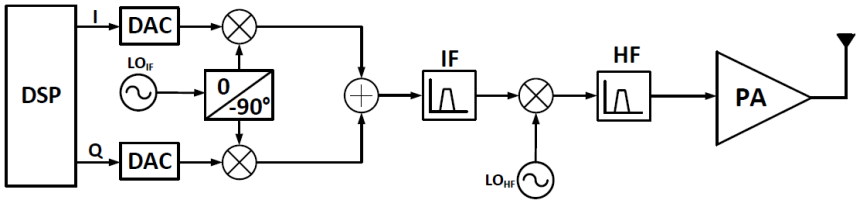


Figure 3.1: Heterodyne transmitter propose architecture.

mixing of ω_1 with the RF desired frequency (ω_2), which will result in two signals, one at $\omega_1 - \omega_2$ and another at $\omega_1 + \omega_2$. Then a bandpass filter will be necessary to eliminate the first one resulting in the output spectrum that consists in the signal around the RF carrier band (Figure 3.2 shows this process). At the end of this transmission chain is a power amplifier that is responsible for the amplification of the output spectrum for transmission at the antenna.

3.1.2 Direct-Conversion Transmitter

Direct-Conversion transmitters are one of the most compact and easy to integrate architectures that can be used. They work by using a quadrature modulator[1] to translate the baseband spectrum to the RF carrier band. This implies that this architecture does the modulation and frequency translation in the same place. This block is preceded by a power amplifier responsible for the signal amplification for transmission. Figure 3.3 shows a schematic propose for this architecture.

[1] Quadrature modulation or Quadrature Phase-shift keying (QPSK)

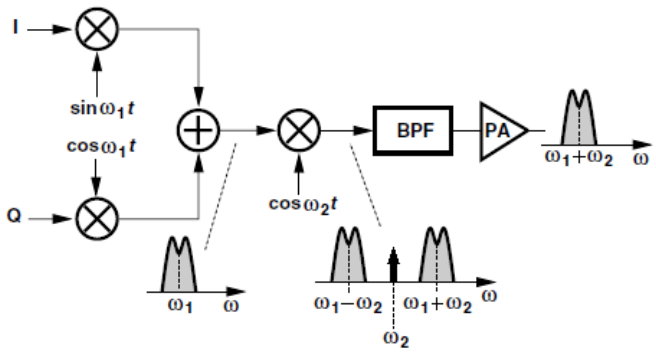


Figure 3.2: Schematic of an exemplification of mixing process with a bypass filter before the PA. [10]

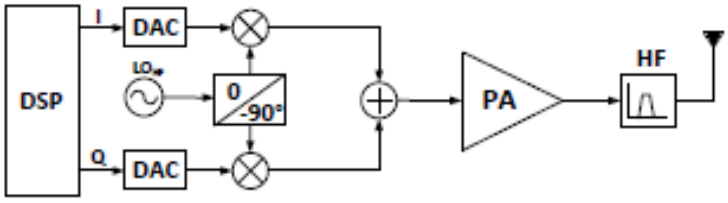


Figure 3.3: Direct-Conversion Transmitter propose architecture.

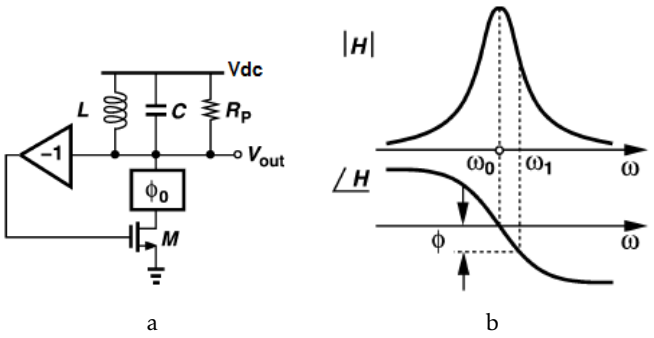
Despite of being capable to transmit a relatively "clean"signal, or by other words the output spectrum obtained only contains the desired signal around the carrier frequency (and its harmonics) without the presence of spurious components, this architecture presents some problems that need to be taken into consideration [10]:

- **I/Q Mismatch** In perfect conditions when quadrature modulation occurs, the I/Q signals should have a difference in amplitude and phase of 90°, but in reality this is extremely difficult to achieve, resulting in a Mismatch between I and Q signals. The result of this little big difference results in ”cross-talk” between the quadrature baseband outputs.

- **Oscillator Pulling** This effect consists in a ”pulling” of the LO frequency which happens when there is a frequency that lies out of, but not very far from the lock range[2] [11]. Figure 3.4(b) shows this effect.

  It’s particularly concerning in this topology because the center frequency of the PA output spectrum is equal to the LO oscillation in direct-conversion transmitters. So taking into account that the PA output can exhibit very large swings, which couple to various parts of the system through the silicon substrate, package parasitics, and traces on the printed-circuit board, it is likely that an appreciable fraction of the PA output couples to the local oscillator [10].

[2]From "Injection locking", that consists in the introducing of a sinusoidal current that forces a phase shift and consequently an oscillation frequency change.



a b

Figure 3.4: (a) Conceptual oscillator with a ϕ_0 phase shift. (b) Open-loop bode diagram, representing the effect of a phase injection. Based on [11].

3.2 Power Amplifiers

A power amplifier is the key component in the design of a transmitter to use in wireless communication systems. They are characterized for being the most power consumption part of the transmitter, making the decision for an architecture and class critical to the fulfillment of the system requirements. Table 3.1 shows the impact of the power amplifier in some of state-of-the-art CMOS transceivers for a variety of communications protocols for a measurable understanding of the importance of this decision.

Table 3.1: PA power consumption impact in state-of-the-art CMOS transceivers in a variety of communications protocols. Adapted from [pg.15] [12]

Standard	**Trans.**	P_T **(mW)**	P_{PA} **(mW)**	**Impact (%)**	**CMOS**
Bluetooth	[13]	19.5	7.5	38.5	0.25μm
IEEE 802.11	[14]	1212	690	56.9	0.18μm
WCDMA	[15]	2114	1700	80.4	0.13μm

Its main purpose is to increase the power level of the signal. Power Amplifiers can be divided in several classes, depending on how the transistor is driven and the harmonic content, or time behavior, of the drain voltage [1]. Another characteristic that defines the various classes of power amplifiers is linear or non-linear working mode. Figure 3.5 show this exact division of categories according linearity of each class. There are two types of linearity that defines the power amplifier: phase linearity and amplitude linearity. This categorization only defines linearity in amplitude, i.e. a non-linear amplifier has phase linearity. Amplitude linearity is defined by when there is a linear correlation between the output magnitude and the input voltage.

The big advantage of using non-linear amplifiers is the inherent high efficiency of them, adding that with the fact that more standards and technologies are created that require a low power consumption justifies the main motivation for their wide usage. Several wireless systems and standards use only phase modulation and the corresponding

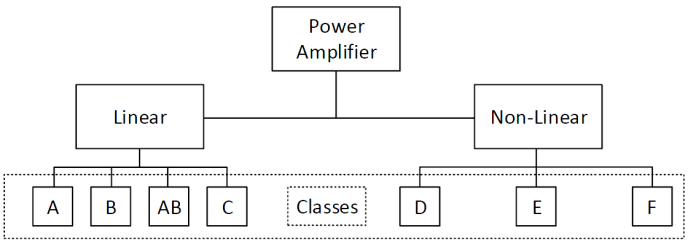


Figure 3.5: Power amplifiers according linearity of each class.

waveforms do not have amplitude variations. As a consequence, the PA only needs to have phase linearity and the amplitude linearity is of no concern. Hence, the non-linear behavior is not considered as a major drawback.

3.2.1 Linear Amplifiers

Looking at figure 3.5 its visible the various classes according to their amplitude linearity. The linear power amplifier classes are A, B, AB and C. As mentioned before, this group of amplifiers is able to amplify signals with non-constant envelope, such as modulated amplitude signals. All these classes share a common topology, that is, all can be implemented using the same base circuit. The main difference between them relates to the bias voltage at the gate that modifies the current conduction angle [12]. Figure 3.6 represents this simplified circuit for linear mode CMOS PAs. The parallel L_f and C_f filter, despite

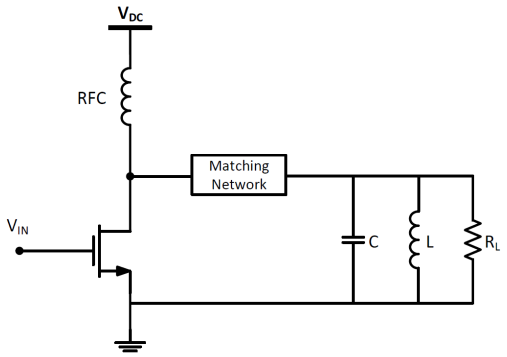


Figure 3.6: Simplified circuit for current source mode CMOS PAs.

not necessary, it's been added in order to filter harmonics outside the fundamental frequency. This will ensure an improvement in the efficiency of the amplifier, because the device only affects the load at the fundamental frequency. At all the other frequencies the filter acts as a short-circuit to the ground. The class of operation of linear amplifiers can easily be identified by observing the drain current waveform. The percentage of the wave cycle in which the transistor is conducting defines the power amplifier operation class, but also has a correlation with is linearity, from the class A, which is the most linear

and has a conduction angle of 360°, through B with a conduction angle of 180°ending in class C which not only has the lowest conduction angle but is also the one that is least linear. It's also important to define that the non-linearity of the PA have a relation with is efficiency, being class C the most efficient. Table 3.2 show the conduction angles of the various linear power amplifier classes[pg.37] [1]. If this amplifier is used with an ampli-

Table 3.2: Conduction angles of the various linear power amplifier class

Class	Conduction Angle (Degrees)
A	360°(100%)
B	180°(50%)
AB	180°(50%) > and < 360°(100%)
C	< 180°(50%)

tude modulated signal, the output voltage V_out will change according to the envelope signal A(t).

3.2.1.1 Class-A Amplifier

The most inefficient of them all, class A PA are characterized by the in active region transistor for the entire input cycle(the drain current waveform has a conduction angle of 360°). This creates a necessity for a continuous current consumption that is practically independent from the output power. Drain efficiency, being 50% at its theoretical maximum, is really poor, especially compared to the other classes. This maximum drain efficiency, assuming that the maximal output swing occurs ($V_{out} = V_{DC}$) and where V_{out} is the output voltage amplitude, can be calculated as 3.1.

$$\eta(\%) = 100 \times \frac{P_{out}}{P_{DC}} = \frac{1}{2} \times \left(\frac{V_{out}}{V_{DC}}\right)^2 = 50\% \tag{3.1}$$

However, if we consider, as an example, the use of a class A amplifier in an amplitude modulated signal we see that the output voltage V_{out} will change according to the envelope signal A(t), so if we consider the probability density function of A(t), the efficiency of the amplifier will fluctuate with it, leading to an average efficiency much lower than the ideal 50%. Also in equation 3.1 we are not taking into account the Knee Voltage[3], which will lead to the maximum amplitude of the output voltage being equal to ($V_{out} - V_{Knee}$), resulting in a maximum ideal efficiency of less than 50%. Figure 3.7 shows the drain current waveform for two periods in this class of amplifiers, showing the 360°conducting angle.

3.2.1.2 Class-B Amplifier

The class-B amplifier like the class-A amplifier is implemented using the same base circuit, but unlike the first one the drain current conduction angle is reduced to 180°,

[3]The voltage limit that separates the saturation from the triodo region of the transistor output [12].

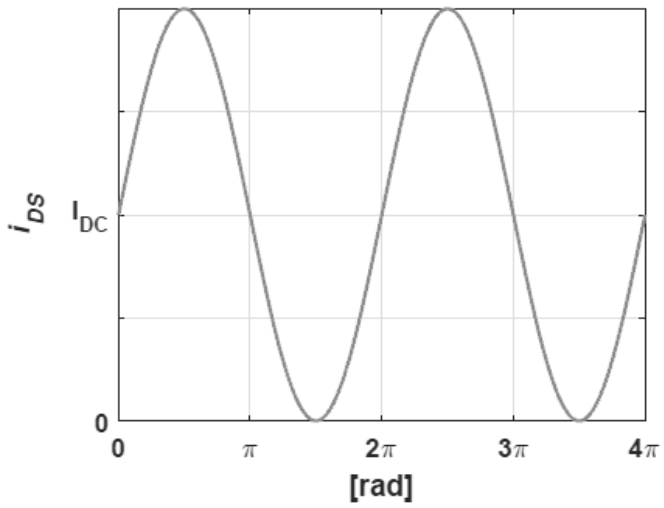


Figure 3.7: Class-A amplifier drain current waveform for two periods.

this is achieved by changing the bias voltage at the gate for this particularly conduction angle. The operation point of the transistor is located exactly at the boundary between the cutoff and the active region [16]. Having half of the conducting angle of the Class-A PA, its efficiency is greater, but consequently the linearity of the amplifier is degraded. Equation 3.2 represents the maximum efficiency theoretical value. If we consider again as an example, the use of a class B amplifier in an amplitude modulated signal we see that the output voltage V_{out} will change according to the envelope signal A(t), so once again if we consider the probability density function of A(t), the efficiency of the amplifier will fluctuate with it.

$$\eta(\%) = \frac{\pi}{4} \times \left(\frac{V_{out}}{V_{DC}}\right)^2 = 78.5\% \tag{3.2}$$

Like in the Class-A amplifier, the maximum efficiency only occurs when V_{out} is equal V_{DC}, which leads to an approximated efficiency of 78.5% (ignoring one more time the Knee Voltage). The drain current waveform is depicted in figure 3.8.

3.2.1.3 Class-AB and C amplifiers

Class-AB Power Amplifiers operates (like the name suggests) between the Class-A and Class-B angle, which settles down between 180 and 360 degrees. This naturally induces that depending on its bias network, this type of amplifier conducts somewhere between 50% and 100% in each cycle [10]. Therefore, the drain efficiency lays somewhere between the 50% maximum of the Class-A amplifier and the 78.5% of the Class-B. The big advantage of this type of power amplifier is that it can achieve a better efficiency than a class-A but remain more linear than a class-B power amplifier [10]. In the end of the linear amplifiers spectrum, we have the Class-C amplifier that has the lowest conduction angle

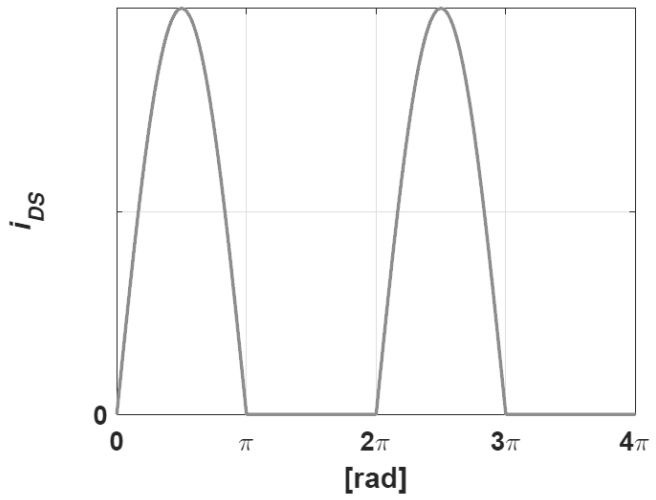


Figure 3.8: Class-B amplifier drain current waveform for two periods.

of all the linear amplifiers. Although the efficiency grows when the conduction angle is lowered, the amplifier becomes less linear because turning off the transistor increases the number of higher harmonics generated [1]. Because of this low linearity some authors do not consider the Class-C as part of the linear amplifiers group. In theory, the amplifier efficiency can be arbitrary increased toward 100% by decreasing the conduction angle until zero. This has the drawback of also reducing the utilization factor of the amplifier toward zero and increasing the drive power to infinite. The drain current waveform is presented in figure 3.9 considering that the LC resonant tank have a high-quality factor, which becomes a short circuit to undesired frequencies besides the fundamental one. The class-AB drain current waveform its not shown because it would be redundant considering the fact that it lies between the Class-A and Class-B waveforms presented before. Figure 3.10 (using the expression 3.3 valid for all classes addressed) shows a comparison between all linear amplifiers considered in this chapter, regarding their drain efficiency (maximum theoretical values) versus the particular conduction angle of each one.

$$\eta(\%) = \frac{1}{2} \times \left(\frac{\alpha - sin(\alpha)}{2sin(\frac{\alpha}{2}) - \alpha cos(\frac{\alpha}{2})} \right) \tag{3.3}$$

Notice that the Class-AB and C amplifiers have a range of possible values that depend on the conduction angle, as previously mentioned.

3.2.2 Non-Linear Amplifiers

Non-Linear amplifiers are the second group of power amplifiers, they are characterized by the lack of amplitude linearity (it is important to note that they maintain phase linearity). The major reason that makes them interesting is its greater efficiency compared to linear amplifiers. They achieve this by having a switching behavior, in fact, this behavior gives them a second widely accepted designation, switch-mode amplifiers. If we ignore the

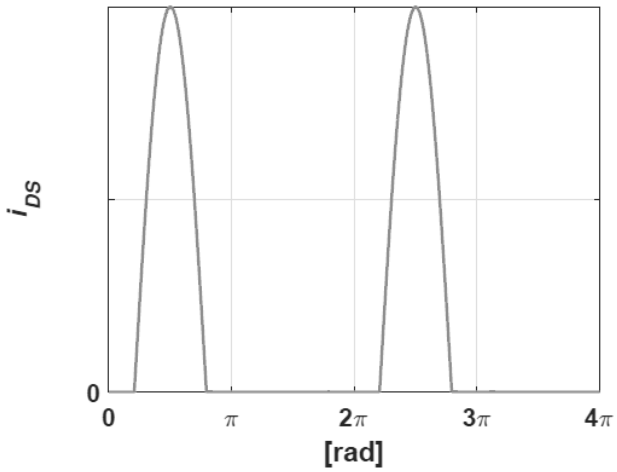


Figure 3.9: Class-C amplifier drain current waveform for two periods.

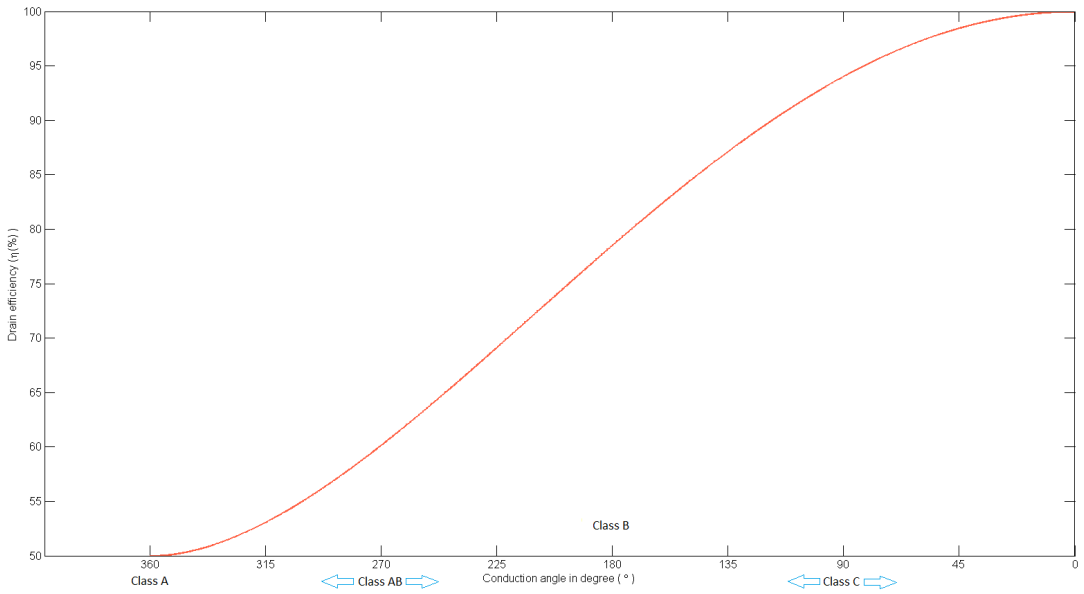


Figure 3.10: Comparison between linear classes drain efficiency.

switching losses, ie the transistor is either conducting or closed, or in other words, we have two states, one where the voltage between its terminals is zero and the current passing through them other than zero ("on"state) or the voltage between their terminals is different from zero and the current passing through them is equal to zero ("off"state), we see that the product of the two, voltage versus current will be always zero, so it's easy to see that if we consider that these amplifiers don't have any other losses the efficiency will be heading towards 100%. Of course in reality the 100 % efficiency value is not real, but in comparison to linear amplifiers and taking into account their ideal efficiency values we easily realize the potentiality of this class of amplifiers in a world where power consumption is such an important factor. The class D amplifier, although it is a non-linear amplifier, will be discussed in Chapter 4.

For example, we can take the image 3.11 circuit that shows a starting point configuration for the understanding of an ideal switching amplifier.

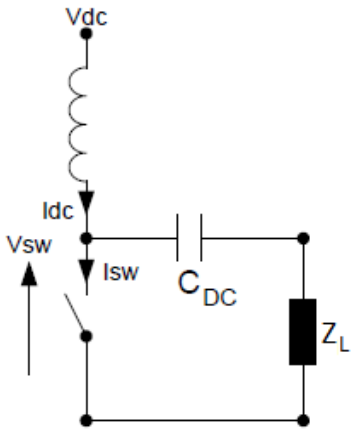


Figure 3.11: Starting point configuration for the understanding of the ideal switching amplifier.

Analyzing this figure we can conclude that the wave produced by this circuit is a square wave with a T period , where the V_{sw} wave and I_{sw} wave are separated by a phase of 180°. This suggests a 100% efficiency in the best case possible and only considering the switching losses, but this is a misconception and it will be demonstrated why.

We know that we are working with square waves so the first step is to calculate the RMS for a square wave with an amplitude of A and a duty cycle of 50%. We do that in

equation 3.4.

$$\begin{aligned} RMS_{square} &= \sqrt{\frac{1}{T} \times \int_{\tau}^{\tau+T} V^2(t)dt} \\ &= \sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} A^2 dt + \frac{1}{T}\int_{\frac{T}{2}}^{T} (-A)^2 dt} \\ &= \sqrt{\frac{2A^2}{T}\int_0^{\frac{T}{2}} 1 dt} \\ &= A \end{aligned} \tag{3.4}$$

Now that we have the RMS for a square wave its time to calculate the output of the amplifier in this case. We consider the Fourier series shown in equation 3.5 with a period of T.

$$f(x) = \frac{4}{\pi} \sum_{n=1,3,5,\ldots}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi x}{T/2}\right) \tag{3.5}$$

Having the two components we can thus calculate the expected maximum efficiency of the switch mechanism for a square wave with a duty cycle of 50 %.

$$\frac{P_{fund}}{P_{square}} = \frac{\frac{\left(\frac{4}{\sqrt{2}\pi}\right)^2}{R}}{\frac{1^2}{R}} = \frac{8}{\pi^2} \approx 81\% \tag{3.6}$$

This mathematical exercise tells us that no matter how efficient the switch is, the efficiency is always limited to 81% (this is not entirely true, because we are considering all the power in a square wave with all the harmonics, if we put a tank circuit in parallel with the load to make a harmonic short, we can reach a theoretical efficiency value of 100%, this will result in a perfect sinusoid at the fundamental frequency being seen by the load), and this is in the most beneficial situation, ie with a duty cycle of 50%, if we reduce the duty cycle we see that this value will be lower. This being said, we will then explore each of the classes in this group of amplifiers.

3.2.2.1 Class-E Amplifier

Class-E amplifiers are the most efficient amplifiers known so far [16]. In figure 3.12 is depicted the basic configuration of this type of amplifiers. Like others in class the transistor operates as a switch, and in perfect conditions should turn on and off abruptly. One of the most attractive feature of this amplifier is that they are designable [17]. The C_S is a grounded capacitor that includes the junction capacitance of the transistor and the parasitic capacitance of the RFC [10], but for high operating frequencies the overall shunt parasitic capacitance is sufficient, making C_S unnecessary [pag.244] [16]. Values of C_s, L_f, C_f and Z_L are chosen in a way that makes the voltage on the source of the transistor (we will denote as V_t) respect 3 conditions [10]:

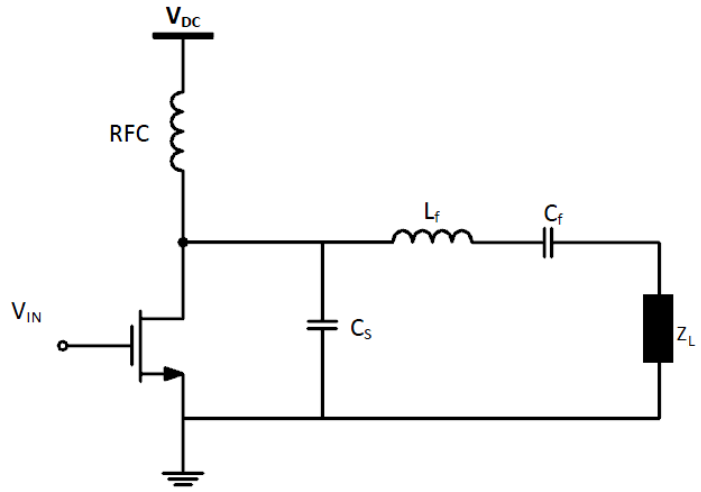


Figure 3.12: Class-E amplifier.

- **1:** When the switch is turning off V_t will remain low long enough making the current drop to zero.

- **2:** V_t will achieve zero just before the on state in the switch.

- **3:** The derivative of V_t with respect to time is also close to zero as the switch is turning on.

The first condition solves the issue of finite fall time at the transistor gate. This condition is guaranteed by C_s. Without this capacitor, V_t would increase at the same rate that V_{in} would drop, allowing the transistor to dissipate power. The second condition exists to ensure the non overlap of V_{DS} and I_D near the turn-on point. This will again minimize the power losses in the transistor even with finite input and output transition times. The third condition serves as a protection for violations of the second condition, or by other words, if there is some overlap between V_{DS} and I_D the efficiency degrades only slightly because when the V_t derivative with respect to time is zero it means that at that point V_t can't have a significant change near the turn-off point [10]. This two last conditions are less straightforward to achieve, but if we look at figure 3.12 we see that when the switch turn off the load network will operate as a damped second-order system being the initial conditions define by C_s, L_f and C_f. The time response of the system depends on the Q of the network. This is shown in figure 3.13, with an under-damped network, an over-damped network and a critically-damped network response. The last one satisfies the second and third condition because if the switch begins to turn on at this time there is zero slope when V_t approaches to zero volt [10].

This conditions are know as the zero-voltage switching conditions (ZCS).

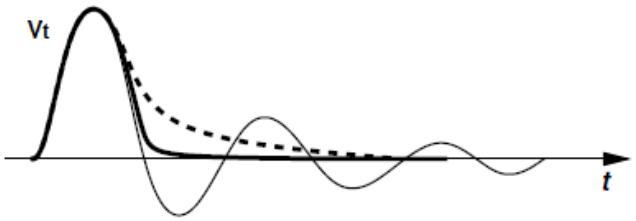


Figure 3.13: Class-E amplifier dumped network time response.

3.2.2.2 Class-F Amplifier

This PA (also called polyharmonic or multiresonant power amplifier) uses one of the oldest methods to improve efficiency [18].

The idea behind it is to let the drain current flow when the drain-to-source voltage is low, and ensure that when the drain-to-source voltage is high the drain current is zero. Therefore, the product of the drain current and the drain-to-source voltage is low, reducing the power dissipation in the transistor and consequently improving the efficiency. In ideal operation the device output will have all even harmonics short circuited (drain current contains only even harmonics), in order to obtain a half sine-wave current waveform, and all odd harmonics open circuited (V_{DS} contains only odd harmonics) to shape the output voltage to a square wave. This is achieved with lumped-element resonant circuits (or Dielectric resonators). This consequentially defines the input impedance of the load network, for each harmonic frequency, as zero or infinite. In a real usage the class F

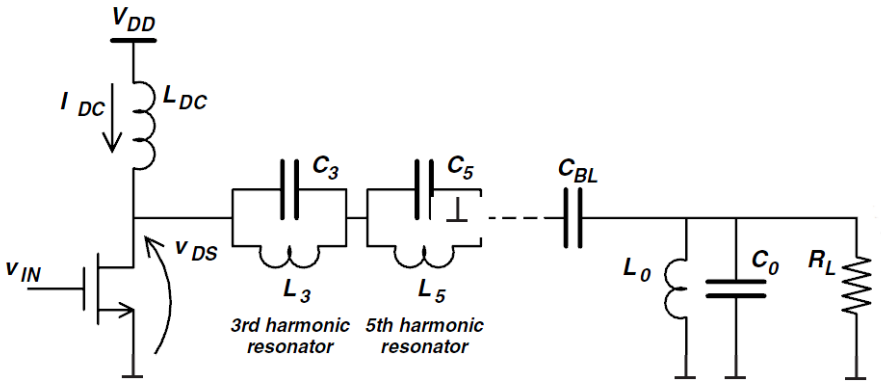


Figure 3.14: Class-F amplifier.

will be tuned to multiples of the fundamental frequency, the image 3.14 shows a class F amplifier tuned to the third and fifth harmonic (this can be expanded to more multiples, increasing consequentially the efficiency). The table 3.3 makes a resume.

This table brings us to the use of a class D amplifier in this thesis, basically what we

Table 3.3: Power amplifier class F performance overview

$Class_{harmonic}$	**Peak efficiency**
F_3	88.4%
F_5	92.0%
F_∞	100.0%

can see is that if we use a resonator for all the harmonics we will have, in a theoretical perspective, an efficiency of 100%. This is exactly the reason for the class D power amplifier selection in this thesis.

Chapter 4

Inverter-Based Class-D Power amplifier

In this chapter the objective is to explore the architecture used to design the power amplifier. As the name suggests the design is based on a simple CMOS inverter. This chapter will not only explore this circuit but also give the reader a better understanding on class-D power amplifiers and some of its architectures. The class-D PA, as mentioned in another chapter is a switched amplifier (non-linear amplifier).

This type of PA was invented in 1959 by Baxandall [19] and at the time gained the name of class D dc-ac resonant power inverter. Applications are extensive, the most common being audio amplification, solid-state electronic ballasts for fluorescent lamps (were they have one of the most simple and smart circuits), soldering and in any application where a power inverter is needed at a low frequency range.

This type of circuit, has been used for low frequency applications for a long time, but for high frequency applications, such as RF, they have been like a *taboo*. The reason for that is the switching losses in MOSFET devices at high frequency applications, but with the introduction of even smaller devices, the technology has evolved to a point where hight speed switching is possible, so this highly promising output power PAs are being study again for this type of applications, where big efficiency is needed as well as high output power.

High output power is extremely difficult to obtain when high efficiency is needed. One way to achieve this is by adopting a strategy that will increase output power without compromising power consumption. This strategy was discussed in a previous chapter, and will be demonstrated in this chapter.

4.1 MOSFET transistor working as a Switch

As explained in the introduction, for the Class-D PA usability in high frequency applications, high speed switches are needed. The function of a switched PA is dependent of this ON-OFF high speed transition. Lets take a NMOS transistor, the drain current in the linear region is given by the expression 4.1.

$$i_D = \mu_{n0} C_{ox} \left(\frac{W}{L}\right)\left[(v_{GS} - V_t) - \frac{v_{DS}}{2}\right] v_{DS} \tag{4.1}$$

This expression is only valid in the ohmic region (or triode region) of the transistor, which is defined by the conditions in 4.2. The $\mu_{n0} C_{ox}$ is the transistor intrinsic transconductance (K_n), μ_{n0} being the low-field electron mobility in the channel and C_{ox} the gate oxide capacitance per unity area.

$$\begin{cases} v_{GS} > V_t, \\ v_{DS} < v_{GS} - V_t. \end{cases} \tag{4.2}$$

The r_{DS}, or the large-signal channel resistance in the same region is given by expression 4.3,

$$rds = \frac{v_{DS}}{i_d} = \frac{1}{K_n \frac{W}{L}\left[v_{GS} - V_t - \frac{v_{DS}}{2}\right]} \tag{4.3}$$

This expression can be simplified for $v_{DS} \ll 2(v_{GS} - V_t)$, gaining the form of 4.4,

$$rds \approx \frac{1}{K_n \frac{W}{L}\left[v_{GS} - V_t\right]} \tag{4.4}$$

We know also that when the transistor is in saturation region (or active region) the drain current is given by 4.5,

$$id = \frac{1}{2} K_n \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 \tag{4.5}$$

Comparing the previous equations, it's simple to conclude that for the MOSFET to work as a switch, we need to be in the triode region, so the drain peak current must be sufficiently lower than the drain saturation current [16]. Image 4.1 shows the relation between drain current versus drain-source voltage for an ideal MOSFET transistor. It's also important to refer that in the cutoff state, when the $v_{GS} < V_t$, the transistor will have a infinite rds and consequentially the drain current will be zero. We see also that the rds in the triode zone 4.3 is inversely proportional to the size of the transistor, so if we want a low power dissipation in the transistor, we need to have a high $\frac{W}{L}$ relation. This will have another effect on the design, if we look to the gate related parasitic capacitances C_{gs} and C_{gd} expressed by 4.6 (equation in triode region [20]), we see that this increase of size will make the transistors very difficult to drive because of the high parasitic capacitances value.

$$C_{gs} = C_{gd} \approx C_{ox}\left(\frac{1}{2} WL + \left(\frac{W}{L_{ov}}\right)\right) \tag{4.6}$$

The drive of these high capacitances will be discussed in the next section, because this subject will be very important to achieve a high efficiency.

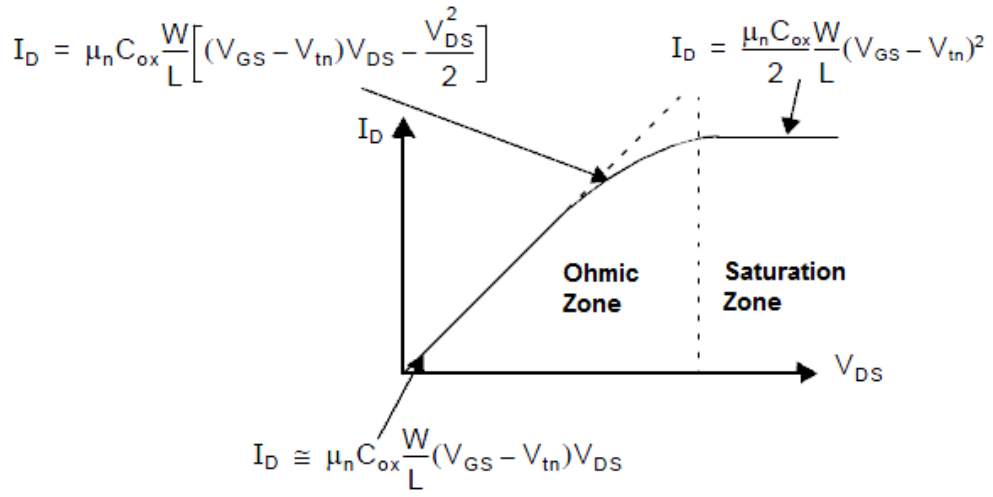


Figure 4.1: Transistor zones regarding i_D versus v_{DS}.

4.2 The CMOS Inverter

The inverter is one of the most used circuits in electronics, for example to transfer DC power to AC power. It's also used as a buffer or a driver in a variety of circuits, or as the name suggests, to invert the signal. In this last application we can see it applied for example in ring oscillators. Another use for the CMOS inverter is for power amplification, in the audio area for example, is a long partner in this usage. This low frequency application as seen the inverter as a good way to make a high efficiency output power stages reducing the heat dissipation and increasing the lifetime of the battery in portable applications [21].

In a simple way the inverter is two switches, one NMOS and another PMOS, with an infinite off resistance (when $v_{GS} < V_t$) and a finite on-resistance when in the linear zone (when $v_{GS} > V_t$) as discussed in the previous section. Image 4.2 shows the static circuit for the CMOS inverter. When we look at this circuit a very intuitive understanding of it can be done. When the input signal is equal to Vdd we will be in the high state of the input. This will cause the NMOS transistor to be "on"creating a direct path between the ground and the V_{out}. For the low state of the input, when the input signal is zero, the PMOS will be active connecting the power supply to V_{out}. The two circuits in 4.3 are representative of this input dependent switching. It's easy to see that in the inverter when the signal input is in the high state the output of the circuit will be in the low state, and when the input signal is at low state the output will be in the high state. This is where the name inverter comes from, the digital "1"is converted to digital "0"and vice versa.

Another important conclusion is that the high and low output levels will be always equal to V_{dd} or GND, this will cause the voltage swing to be equal to the supply voltage. The output voltage in a real world application is described by the 4.4 graphic [22, pg.321].

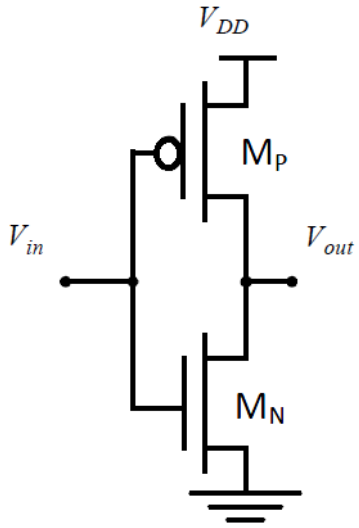


Figure 4.2: The MOSFET inverter circuit.

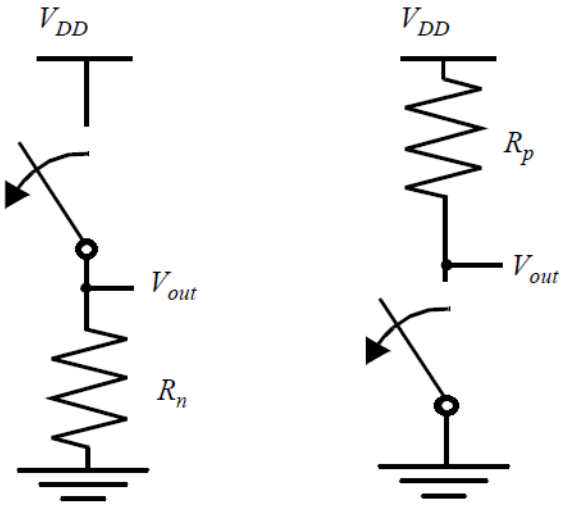


Figure 4.3: The first circuit represents the high side, were the NMOS will be conducting, and the second one the low side were the PMOS will be conducting.

This graphic also shows a zone where both the transistors are saturated, this will cause a direct short from the power supply to ground causing losses and stress on the devices. This type of behavior will be explored in the next chapters.

4.3 The inverter based Class D Voltage-Switching Power Amplifier

There is two types of class-D amplifiers, the voltage-switching(or voltage-source) and the current-switching (or current-source). In the first type they are power supplied by a voltage source and have a series-resonant circuit at the V_{out}. If the resonant circuit quality

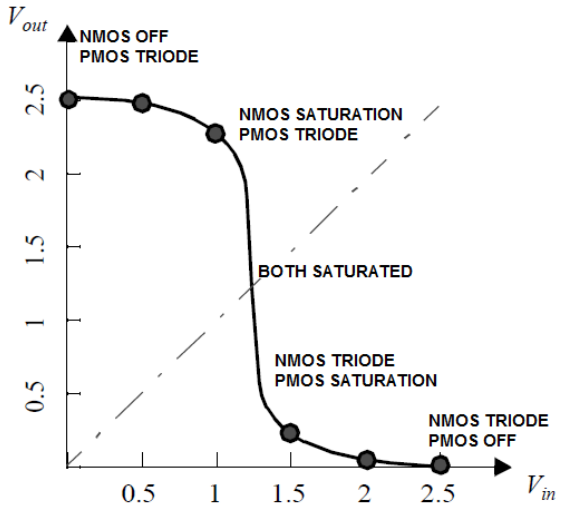


Figure 4.4: The first circuit represents the high side, were the NMOS will be conducting, and the second one the low side were the PMOS will be conducting.

factor is sufficiently high the current passing through the resonant circuit is a sinusoid and in the MOSFET switches a half-sine. The drive made to the switches is a square wave. Image 4.5 shows a voltage-switching inverter based class D power amplifier base circuit. In the current switched case, current will be supplied (V_{dd} with an RFC choke), and a parallel-resonant circuit will be placed before the antenna (the base circuit is showed in image 4.6). The load will see a voltage sinusoidal wave (if again the quality factor is sufficiently high), and the switches half-sinusoid voltage wave [16]. If we look at this

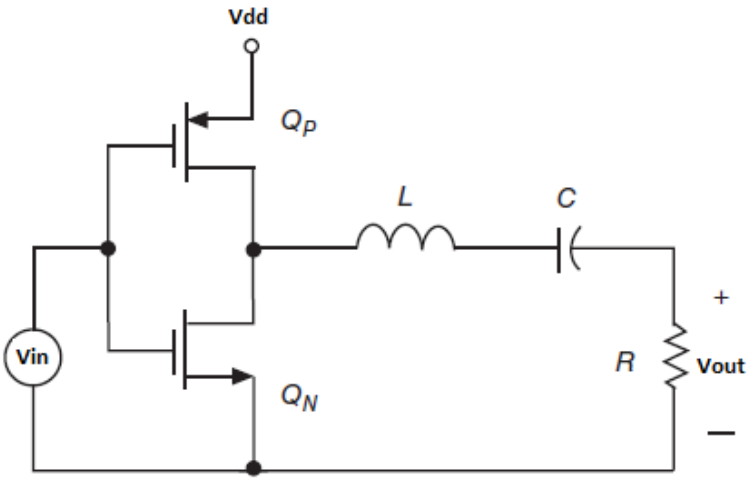


Figure 4.5: Voltage-Switching Inverter based Class-D PA.

topology the base circuit is basically a inverter with a resonant circuit at the end. We can conclude, knowing this, that the behavior of the circuit will be similar to the behavior of the inverter.

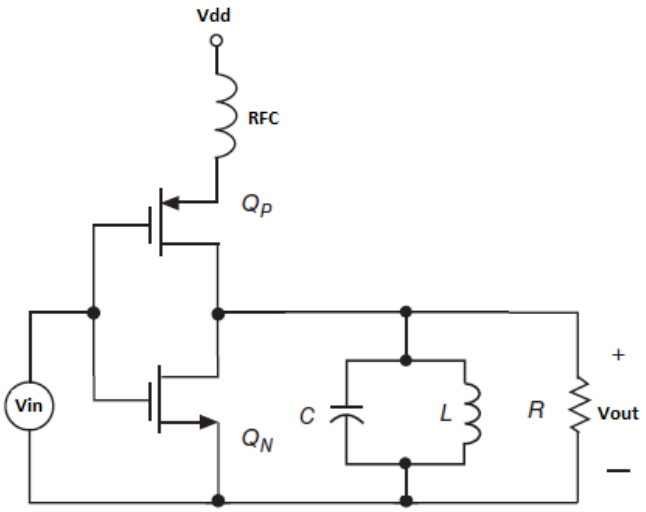


Figure 4.6: Current-Switching Inverter based Class-D PA.

The first important thing to mention is that cross-conduction will occur causing spikes in the drain current, this is justified by the image 4.4 were we can see that during a small period of time both transistors are conducting so we will have a direct short from the power supply to ground, this issue can be minimized if we use non-overlapping gate-to-source voltages to give time for one transistor to be in cutoff zone. In literature we can find some examples like [23] but this method will increase the complexity of the driver circuit.

The next thing that we see is that this circuit can be seen as two switches working from triode to cutoff zone one at a time. If we look at the condition to be in the transistor linear zone (equation 4.1) we see that the drain-to-source voltage needs to be smaller then the gate-to-source voltage. So this means that the power supply voltage needs to be relatively small to avoid voltage breakdown of the gate oxide SiO_2 (one way to avoid this is to use a voltage mirror driver or a voltage level shifter, again this will increase the driver complexity. We can find some literature examples like [24]). This second issue for RF application is not really relevant, because in this type of application the power supplied voltage is low, due to the need of system portability (supplied voltage is usually a battery).

One of the issues with this architecture as already explained, the oxide breakdown, when the gate-to-source voltage swing is to high. Another issue that is also common in this type of architecture is the hot carriers effect. This effect is particularly visible in switched architectures because of the constant switching between the on and off states, cutoff zone and triode zone. The effect consists in carriers traveling at high speeds in the transistor channel and colliding with the edges. Because of this high velocity and energy

collisions, they will create electron-hole pairs by impact ionization. The generated bulk-pair carrier will be collected by the drain or injected into the gate oxide. If the second effect occurs this will lead to hot carrier degradation (like a change of the threshold voltage due to occupied traps in the oxide). The hot carriers can also generate traps at the silicon-oxide interface (fast surface states). The effects caused by this will be sub-threshold swing deterioration and drain leakage [25]. A similar phenomenon that in this case can cause a premature degradation of the transistor is the core principal used for energy generation in photovoltaic cells.

4.3.1 Principle of operation

As the name suggests this topology has a similar working principle as the CMOS inverter with one major difference, at the system output a resonant circuit is present, being in the case of a voltage-switching topology a series-resonant circuit and in the current-switching case a parallel one. The resonant circuit LC is designed to work at a certain frequency (fundamental frequency). If the quality factor is high enough ($Q_L > 2.5$) the current throughout the LC resonant circuit is a sine wave. The quality factor can be calculated by expression 4.7.

$$Q_L = \frac{\sqrt{\frac{L}{C}}}{R} \tag{4.7}$$

The image 4.7, adapted from [16, pg.170], shows the class-D PA operation waveforms. In the original image we can see that there are three operation conditions, one where the output frequency is lower then the fundamental frequency (the resonant circuit will be seen as an high capacitive impedance), one were the output frequency is equal to the fundamental frequency and a last one were the output frequency is above the fundamental frequency (the resonant circuit will be seen as an high inductive impedance). In real systems we will see these three conditions, but for the propose of this explanation we will only concentrate on the "ideal case", which is the output frequency being equal to the resonant frequency.

The circuit V_{in} is a square wave that goes from 1 to 0, this can be seen in image 4.7 as the V_{GS} and V_{SG}.

When the control input square wave is at the low level the PMOS transistor will be conducting and the NMOS will be at cutoff zone. As the PMOS is conducting the output of the circuit will be equal to the supplied voltage. A current will start to flow from the supplied voltage to the resonant circuit plus the load at the end. This will create a positive half-sine wave, since the resonant circuit has a high quality factor. Considering that we have no losses at the transistor and this is an ideal case the source-to-drain voltage in the PMOS transistor will be zero. For the other part, when the control square wave is at the high level the NMOS transistor will conduct and the PMOS will be at the cutoff zone. This will create a direct path between ground and the output of the system, so the series-resonant circuit plus the resistive load will be directly connected to ground. Again

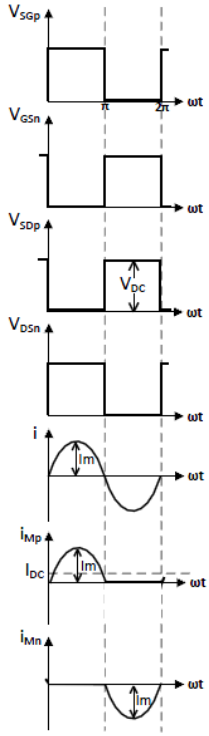


Figure 4.7: Operation waveform for the voltage switching class D PA at fundamental frequency.

as we are considering an ideal case, there will be no losses so the V_{DSn} will be zero. The charged series-resonant circuit will force a current in the opposite direction, creating the negative half-sine wave. The charging process of the resonant circuit is simple to explain, the resonant circuit is composed by an inductor(that stores energy, when a current passes through, in a magnetic field) and a capacitor (that accumulates charge in a electric field). When the PMOS is active, power is flowing from V_{DC} to the LCR circuit, as current is passing through the inductor this will charge the magnetic field. When the PMOS is OFF and the NMOS is ON the charged inductor will dissipate it's energy, creating the negative current. As the resonant circuit is tunned for the fundamental frequency, this will occur with an oscillating frequency equal to the fundamental frequency.

4.3.2 Ideal analysis

As stated before the image 4.7 represents the operation at the fundamental frequency (f_0) without any losses. This will serve as base for the ideal analysis of the circuit. If there is no power being dissipated, and the drain-to-source voltages don't overlap with the current waveforms no power is dissipated. Also when the switching of the transistors occurs the current at their terminals is zero so we can say that the Zero-current-switching (ZCS) condition is achieved. As stated before the transistors are ideal consequentially the switching action is made at the same frequency as the input control square wave. So we

can express the drain-to-source voltage as the trigonometric Fourier series for the square wave knowing that between 0 and π the amplitude will be equal to the supplied voltage and between π and 2π the amplitude will be 0 (assuming the NMOS V_{DS}). Also we ignore the odd harmonics because we are assuming a perfect square wave function.

$$V_{DSn} = Vdd\left[\frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1-(-1)^n}{2n}\sin(nwt)\right] = Vdd\left[\frac{1}{2} + \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{\sin[2k-1]wt}{2k-1}\right] \tag{4.8}$$

We know that the load quality factor needs to be high for the voltage that crosses the load to be a sinusoid with the tunned resonant circuit frequency. In this ideal case we are assuming this factor. So the output voltage is 4.9.

$$v = V_m \sin(wt) \tag{4.9}$$

where the amplitude V_m (first harmonic) is given by,

$$V_m = \frac{2}{\pi}V_{DC} \tag{4.10}$$

and the current i through the load is also a sinusoid,

$$i = I_m \sin(wt) \tag{4.11}$$

The current amplitude is given by,

$$I_m = \frac{V_m}{R_{load}} = \frac{2}{\pi}\frac{V_{DC}}{R_{load}} \tag{4.12}$$

The current given by the power supply to the circuit is equal to the current passing through the PMOS transistor, so we can conclude that is value its different from zero only on half of the control cycle (from 0 to π). Being this period the same that the PMOS is active. In the other half period the PMOS is off and the NMOS is conducting.

Using 4.11 we know that the current that passes in the load is a sinusoid, so we can calculate the DC current,

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(wt)dwt = \frac{I_m}{2\pi}\int_0^{\pi}\sin(wt)dwt = \frac{I_m}{\pi} = \frac{2V_{DC}}{\pi^2 R_{load}} \tag{4.13}$$

Having the DC current consumption, its easy to get the power requested to the power supply,

$$P_{DC} = V_{DC}I_{DC} = \frac{2V_{DC}^2}{\pi^2 R_{load}} \tag{4.14}$$

Now that we have the input power, in order to calculate the efficiency of the amplifier, we need to get the power dissipated on the load. We know that the output current is given by 4.12, so the power output is given by,

$$P_O = I_{m_{rms}}^2 R_{load} \tag{4.15}$$

This will bring us to the reason why the class D amplifier is so promising in terms of high efficiency, the theoretical efficiency is 1(4.16)

$$\eta = \frac{P_O}{P_{DC}} = 1 \tag{4.16}$$

In a real application this analysis is not valid, for example it's impossible achieve no losses in the transistors. Nevertheless this is a promising start for the class D PA, as a great power amplifier for radio frequency portable applications where the efficiency and low consumption are so difficult to achieve. In the next section a more realistic approach will be used for the same calculations.

4.3.3 Non Ideal analysis

The first thing that needs to be taken into account is the on-resistance of each transistor. This resistance is linear and equal for both transistors,

$$r_{DS} = r_{DS_p} = r_{DS_n} \tag{4.17}$$

We are also assuming that the parasitic capacitances of the transistors are linear, and the elements of the series-resonant circuit are passive, linear and time invariant. The inductor internal resistance will be denoted as r_L and the capacitor internal resistance r_C. Looking at the equivalent circuit (4.8) we see that when one of the transistors is "on"and

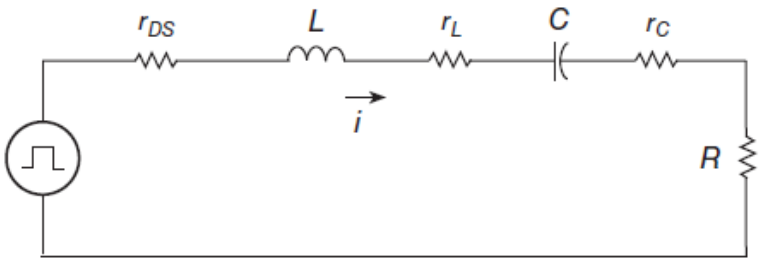


Figure 4.8: Equivalent circuit when on of the transistors is "on".

the other is "off", we can denote the total resistance of the circuit as 4.18.

$$R_{total} = r_{DS} + r_L + r_C + R \tag{4.18}$$

Since there are two transistors, and they conduct in half period each one, we can denote the equivalent resistance in the linear zone as half,

$$r_{DS} = \frac{r_{DS_Q} + r_{DS_N}}{2} \tag{4.19}$$

As stated before the circuit is only draining current from the power supply when the PMOS transistor is on(4.11), so there is a need to calculate the current rms value,

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} (I_m \sin(wt))^2 dwt} = \frac{I_m}{2} \tag{4.20}$$

With this current we can now calculate the conduction power loss in each transistor,

$$P_{loss_{rds}} = r_{DS} I_{rms}^2 = \frac{r_{DS} I_m^2}{4} \tag{4.21}$$

As each transistor only conducts half period, the total power loss needs to be doubled(4.19),

$$P_{lossTotal_{rds}} = 2P_{loss_{rds}} = 2\frac{r_{DS} I_m^2}{4} \tag{4.22}$$

The next part is to calculate the switching losses, they represent the dynamic voltages and currents that the transistor needs to handle during the transition between on and off state [26] (in the ideal case we consider that this transition in time doesn't exist so there is no switching losses). The switching power losses are defined in [16, pg.189],

$$P_{lossSW} = \frac{1}{2} f C_0 V_{DC}^2 \tag{4.23}$$

Since we use two transistors, being one PMOS and another NMOS we need to take into account the switching losses of both,

$$P_{lossSW_p} = \frac{1}{2} f C_{0_p} V_{DC}^2 \tag{4.24}$$

$$P_{lossSW_n} = \frac{1}{2} f C_{0_n} V_{DC}^2 \tag{4.25}$$

Using 4.22, 4.25 and 4.25 we conclude that the total losses in the transistors is given by,

$$P_{lossNP} = \frac{I_m^2}{4}\left(r_{DS} + \frac{\pi^2}{2} f (C_{0_p} + C_{0_n}) R_t^2\right) \tag{4.26}$$

Now that we have the power losses in the transistors, we know the current that passes throughout the system(4.20) and we know the resistive load of the resonant circuit (4.18) it's easy to calculate the total overall efficiency of the circuit,

$$\eta = \frac{P_O}{P_{DC}} = \frac{I_{rms}^2 R}{I_{rms}^2\left(r_L + r_C + R + r_{DS} + \frac{\pi^2}{2} f (C_{0_p} + C_{0_n}) R_t^2\right)} \tag{4.27}$$

That simplifies as,

$$\eta = \frac{R}{\left(r_L + r_C + R + r_{DS} + \frac{\pi^2}{2} f C_0 R_t^2\right)} \tag{4.28}$$

Equation 4.28 shows that an efficiency of 100% is impossible to achieve, there will be always losses in the circuit that cause a reduction of the efficiency. This loss can be reduced with a correct and optimized design.

4.4 Gate driving

One of the most important part of the system is the driver. The efficiency of the class D PA has a great dependency on the transistors size. Looking at equation 4.28 we see that we need a small r_{DS} to achieve a high efficiency design.

This resistance is transistor size dependent, being a bigger transistor the one with the smallest resistance (4.3). This will cause another effect in the design, if we look to the parasitic gate capacitors equation for the transistor 4.6 we see that this necessity for a low on resistance will increase the gate parasitic capacitances.

In this type of PAs the parasitic capacitances are so high that they need to be driven, for that the design of a driver is needed to provide enough current to charge this capacitances without causing a big delay on the topology response.

A lot of strategy's can be used, for example [27] use a pulse transformer to perform this driving, in other cases they use a high efficiency PA class to provide enough current for the driving of this capacitors and last if the objective is not the creation of a full integrated RF front end the driving of the power amplifier can be done outside the chip.

In the case of this thesis the most simplistic approach will be used, a cascade of inverters. The inverter topology has been studied, and is the base of the voltage-switching Class D used in this thesis. A similar approach can be seen in [27].

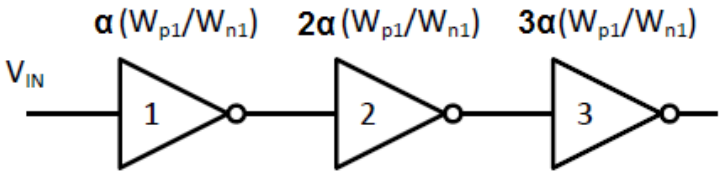


Figure 4.9: Buffer based power amplifier driver.

The inverters will be acting as buffers for the signal guaranteeing a minimum response time of the power amplifier. As the inverter voltage output is directly supplied by the power supply there is enough current to charge the parasitic capacitors. The cascade is composed by N inverters being each one smaller in size by a α factor. The parasitic capacitance will be also smaller by a α factor (4.6). Using the same principle used in [27] the selection of α as 3 is the best option to minimize the propagation delay (the same technique used in device scaling for CMOS output buffers).

4.5 Resonant circuit

The resonant circuit is a simplistic bandpass filters. It acts like a second-order bandpass filter converting the square wave produced by the inverter in a sinusoid. This is achieved by filtering the DC component and all the harmonics of the square wave allowing only the fundamental frequency to pass.

The tunning frequency for the resonant circuit is calculated by 4.29,

$$w_0 = \frac{1}{\sqrt{LC}} \tag{4.29}$$

The load quality factor is given by 4.30,

$$Q_L = \frac{w_0 L}{R_{total}} \tag{4.30}$$

were R_{total} is 4.18. The bandwidth of the series-resonant circuit is 4.31,

$$BW = \frac{f_0}{Q_L} \tag{4.31}$$

Looking at 4.31 it's easy to understand why the load quality factor needs to be high for the circuit to work, because if the bandwidth is to large an ineffective filtering will occur leading to the appearance of harmonics, which will be seen by the antenna load as something different then a perfect sinusoid. Another bandpass filter can be used, for

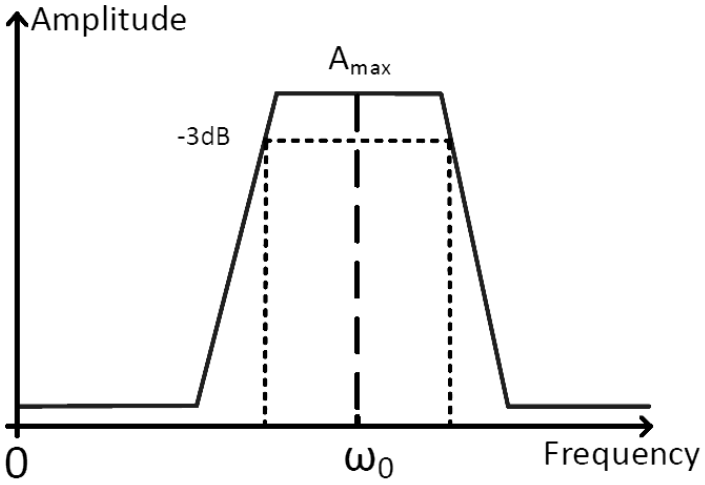


Figure 4.10: Bandpass filter frequency response.

example a butterworth bandpass filter, this strategy is used in [27].

4.6 Integrated transformer

Integrated transformers is something that has been discussed in the first chapter of this thesis. When we refer to power combining the transformer appears as a great solution for the purpose. The on-chip implementation of 1-to-n transformers is very difficult because the primary and/or secondary have to carry large currents, also it's very hard to achieve a turn ratio greater than 2 in this type of topology's [10]. This being said the easiest way to implement a 1-to-1 transformer where the primary is in parallel and the secondary in series (voltage-mode transformer) [28].

The amplification of the transformer will be equivalent to the factor of the number of PAs. If there are two PAs the result will be the sum of the two power outputs.There is a moment where the losses that the transformer has are greater then the power sum of all PAs.

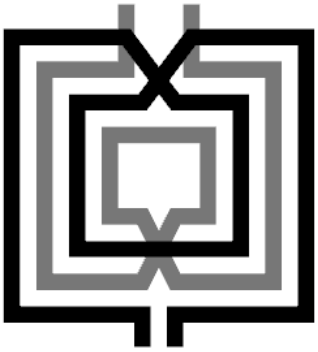


Figure 4.11: 1-to-1 transformer taken from [10, pg.821].

A transformer consists in two inductors with strong magnetic coupling. They need to have between primary and secondary windings a low resistance (to reduce losses) and a low capacitive coupling. Its function is based in the Lenz law, which states that variation in the magnetic flux caused by current flowing in the primary will induce current in the secondary.

With a perfect transformer the induced current will cause a positive voltage across the load connected to the other side. There are two principal parameters in transformer design, the transformer turn ratio 4.32,

$$n = \frac{V_S}{V_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} \tag{4.32}$$

where the V_S and V_P are the voltages in the secondary and primary , the L_S and L_P are the self-inductances of the primary and secondary windings. And the coefficient of magnetic coupling K 4.33,

$$K = \frac{M}{\sqrt{L_P L_S}} \tag{4.33}$$

where M is the mutual inductance between the primary and secondary windings. The coefficient of magnetic coupling K will be zero if there is no coupling and one if the coupling is ideal [29]. The modeling of an integrated transformer is dependent on the existence of accurate models derived from the physical layout and the process technology specifications [30]. The most precise numerical solution is the Maxwell equations in three dimensions. An equivalent model for the transformer exists, the image 4.12 shows this model that takes as a base a simple integrated inductor. Looking at this model we can see the extreme complexity to find all the parameters. Some effort has been made to simplify this task. Transformers are internally connected with the design of integrated inductors so the same principles can be used, only with the addition that there is a necessity for the inductors to be with a strong magnetic coupling.

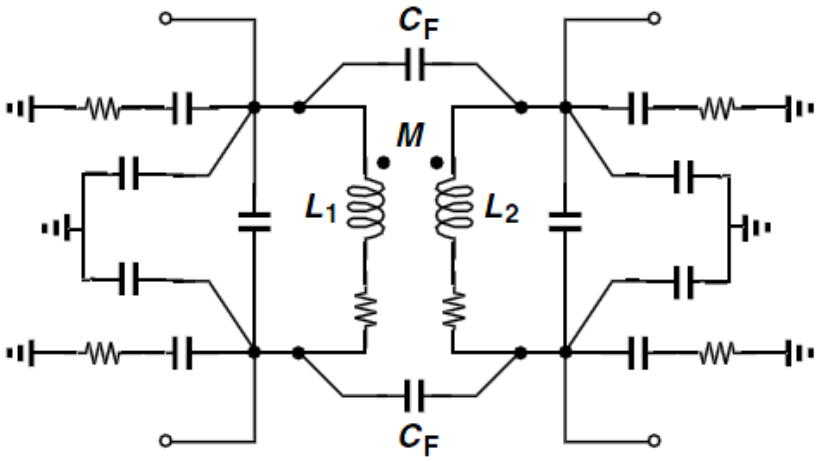


Figure 4.12: Transformer model equivalent adapted from [10].

Chapter 5

Inverter-Based Class-D Power amplifier with power combiner, Design and simulation

This chapter is the conclusion of the study done for the implementation of this thesis. The class D PA was the one selected for the transmitter front end, because of the promising theoretical results that this architecture shows. For higher output power achievement a 1-to-1 voltage-mode transformer was used.

The propose reference values for this thesis were an $130nm$ technology, an efficiency of 20% minimum, a power output of $0dBm$, a working frequency of $2.4Ghz$ and a supplied voltage that could go from $0.5V$ to $1.2V$.

5.1 Inverter based Class D power amplifier - Design

The high level model for this architecture is shown in the image 5.1. This model shows not only the class D architecture, but also the driver stage needed to drive the high gate parasitic capacitances that this architecture have. The starting point of the design was the size of the transistors, for this, and knowing that the power output is not our initial concern, the efficiency was used. From chapter 4 we know all the non-ideal equations that represent the topology. Equation 4.28 show that the efficiency is mostly dependent on the resistive losses, not only in the transistors, with the characteristic r_{DS} and switching losses, but also in the resonant circuit. Before any calculation its important to define the circuit parameters. The r_{DS} is governed by equation 4.3, with this information we can

Table 5.1: Circuit transistors parameters.

V_{DC}	f	K_n	K_p	V_{tn}	V_{tp}	L	C_{ox}
$1.2V$	$2.4Ghz$	$500\mu AV^{-}2$	$100\mu AV^{-}2$	$0.38V$	$0.33V$	$130nm$	$12.3fF/\mu m^2$

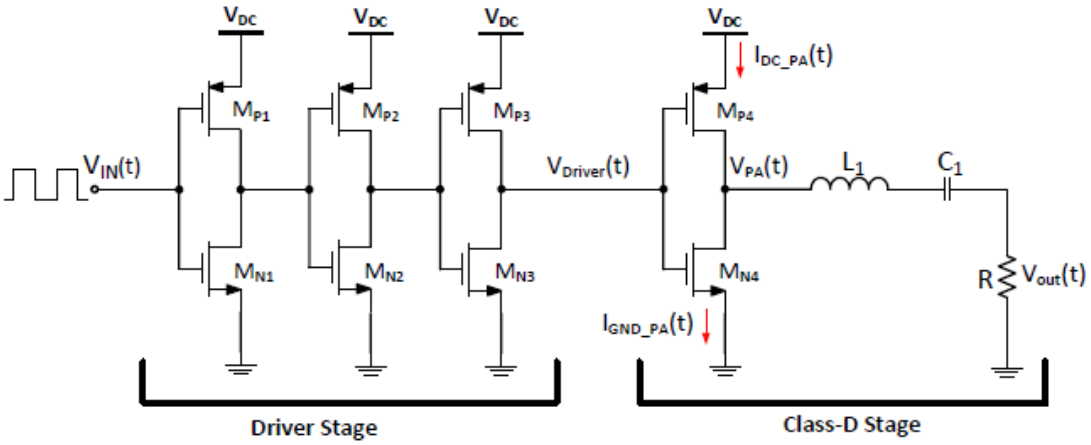


Figure 5.1: High-Level implemented architecture for the inverter based Class D power amplifier.

plot the resistance versus the width of the PMOS transistor, in order to get the minimum value possible (assuming a constant V_GS of 0.8V). Looking at the picture, it's easy to see

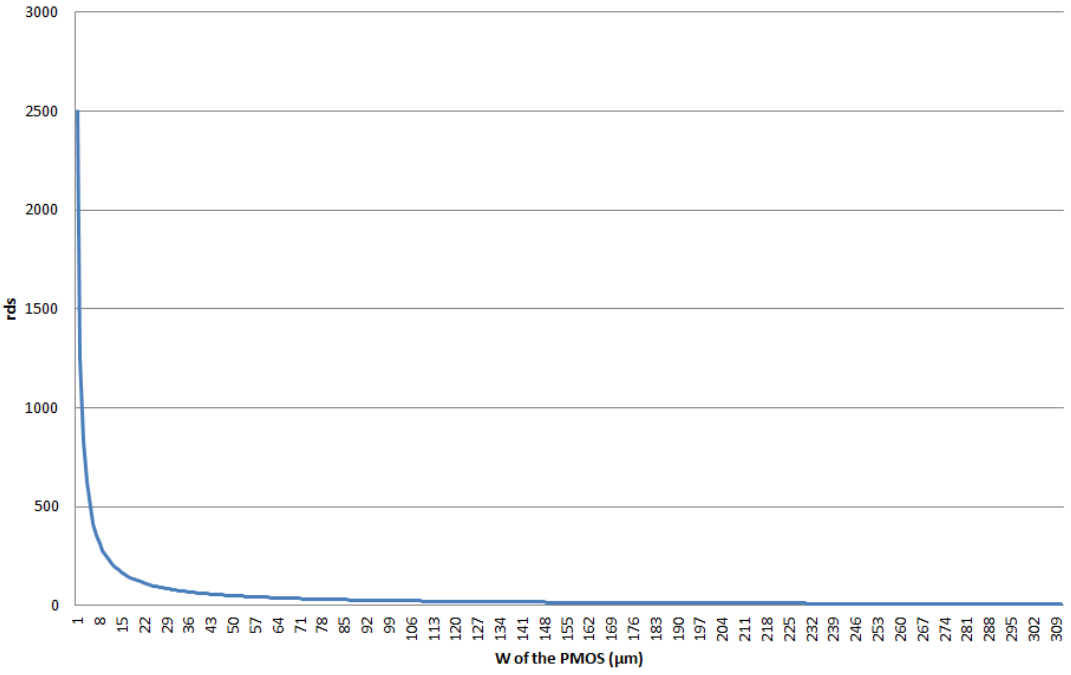


Figure 5.2: Evolution of the PMOS transistor in relation with the channel width (4.3).

that there is a moment where the increase in size of the transistor will not bring a big advantage in terms of resistive losses. This is important also because a bigger transistor will increase the switching losses and therefore reduce the power amplifier efficiency (also will increase the parasitic gate capacitances turning the PA more difficult to drive). This moment its between $130\mu m$ and $170\mu m$ PMOS transistor width size. To maintain

the equilibrium between transistors, the NMOS will be 3 times smaller than the PMOS. So the NMOS size will be between $43\mu m$ and $57\mu m$. Now that we have a range for the transistors size it's time to design the resonant circuit.

Looking at table 5.1 we see that the working frequency is $2.4Ghz$, from 4.29 we get,

$$\sqrt{LC} = \frac{1}{2 * \pi * 2.4 * 10^9} \tag{5.1}$$

With the help of a dedicated software for filter design, and some simulation to see the real rds of the transistors, the values obtain are $17.68nH$ for the inductor and $248.7fF$ for the capacitor. An impedance matching was done, to guarantee less losses in the power transfer. We know by [31] that the quality factor for integrated inductors in silicon substrate is 10 (losses in high frequencies), also that the typical quality factor for an integrated capacitor is 50. With this values in mind we can calculate the resistive part of the inductor and capacitor,

$$r_L = \frac{W_0 L}{Q_L} = 26.66\Omega \tag{5.2}$$

$$r_C = \frac{1}{W_0 C Q_C} = 5.33\Omega \tag{5.3}$$

With all this information we can make a table where all the parameters are compiled 5.2, Now that we have not only a range for the transistors size but also the filter parameters,

Table 5.2: Resonant circuit parameters

L	Q_L	r_L	C	Q_C	r_C
$17.68nH$	10	26.66Ω	$248.7fF$	50	5.33Ω

there is only one thing that lacks in the designing part, the understanding on how to drive the transistors. Various tests were performed by simulation to predict not only the best size for the transistors, being the selected one $153.6\mu m$ for the PMOS and $51.2\mu m$ for the NMOS, but also the selection of the best voltage-swing to drive the transistors to achieve the biggest efficiency possible. The result was a square driving wave with a voltage swing of $0.8V$ where half of the duty cycle the voltage level is $0.4V$ and the other $-0.4V$. Now

Table 5.3: Transistors size and resistance

$PMOS$	r_{DS_p}	$NMOS$	r_{DS_n}
$153.6\mu m$	16.27Ω	$51.2\mu m$	10.81Ω

that all the parameters of the design are available we can predict not only the output power but also the expected efficiency of this system. The difference in internal resistance between transistors is justified by the use of an approximated formula for the calculation.

Having all the parameters the first figure of merit to calculate is the power output of the system 5.4,

$$P_O = \frac{2V_{DC}^2 R}{\pi^2 R_t^2} = \frac{2V_{DC}^2 R}{\pi^2 (R + r_L + r_c + r_{DS})^2} = 1.51mW \tag{5.4}$$

Converting the value to dBm 5.5,

$$10\log_{10}\left(\frac{P(mW)}{1mW}\right) = 1.79dBm \tag{5.5}$$

Now that we have the power output we can calculate another figure of merit for the PA, the efficiency, but for this we need to know the gate parasitic capacitance for both transistors,

$$C_{o_p} = C_{gd,p} \approx C_{ox}\left(\frac{1}{2}W_p L\right) = 17.232fF \tag{5.6}$$

$$C_{o_n} = C_{gd,n} \approx C_{ox}\left(\frac{1}{2}W_n L\right) = 5.744fF \tag{5.7}$$

With all the information we can finally find the efficiency of the proposed power amplifier 5.8,

$$\eta = \frac{R}{\left(r_L + r_C + R + r_{DS} + \frac{\pi^2}{2} f C_0 R_t^2\right)} = 51\% \tag{5.8}$$

This results gives a perfect start for the simulation, the efficiency its inside the expected values, and the power output its sufficient to comply with the propose starting objectives. A more realistic model is expected in simulation, so this results are seen as a maximum value achievement for the PA design, or by other words the maximum in terms of figures of merit to be achieved by the design.

5.2 Inverter based Class D power amplifier - Simulation

The simulation will be the last part of this thesis, where all the work in designing and interpreting the class-D PA will culminate in a result.

The first simulation was done with the PA in a standalone configuration, in this test pre-layout components were used and the PA drive was done with an ideal square wave with a voltage between $-0.4V$ and $0.4V$. The result waves are showed in image 5.3, We can see that the voltage and current seen by the antenna are both sinusoids, as predicted. The output shows a little distortion, which indicates that some harmonics are not being correctly filtered, but this result is good enough to classify the resonant circuit design as correct. In the input current, peaks are present. This peaks are directly related with the transistor switching, and a moment were both transistors are conducting (in an ideal case this wouldn't happen because the transistors are seen has perfect switches). This will cause a direct shunt between the power supply and ground. This effect is the reason for the peaks.

The next simulation was to see the power at the output, image 5.4 shows that simulation, The power amplifier output P_O in this solo architecture achieve an value of $1.78dBm$,

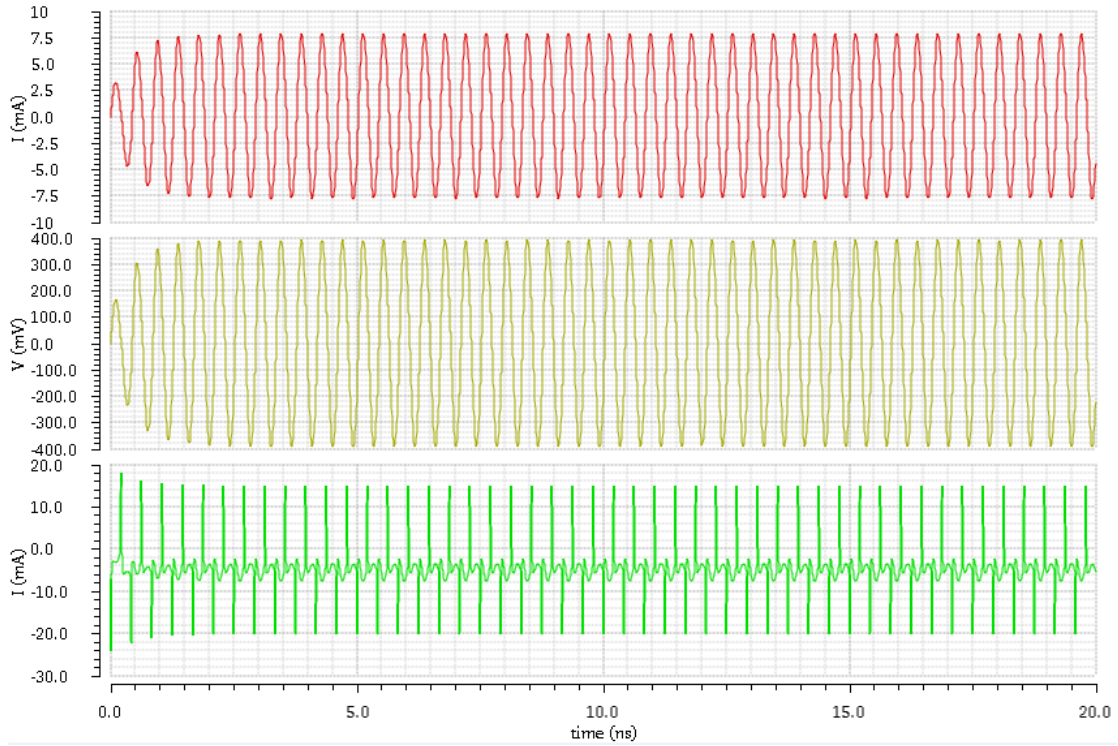


Figure 5.3: The first and second graphic represent the current and voltage at the PA output. The last image is the I_{DC} supplied to the PA.

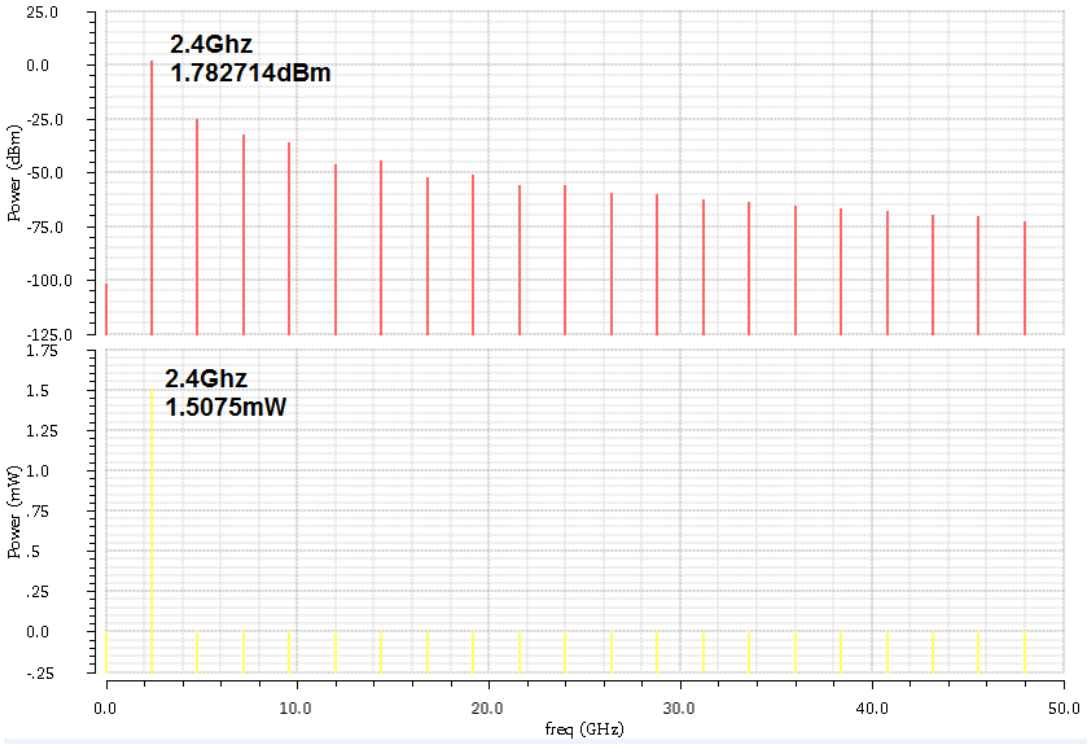


Figure 5.4: PA without driver Output power.

this result plus the current supplied wave allow us to calculate the efficiency of the PA 5.9,

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{I_{rms} * Vdd} = 21\% \tag{5.9}$$

This result is worse than predicted, this indicate that the losses are bigger than expected. Nevertheless, it's important to notice that pre-layout components were used to show the cruelty of real life in terms of IC design.

The next simulation is with the driver implemented. As stated before the technique used to design the driver was the same used in [27]. The size of the transistors were incremented by a factor of 3, and 3 inverters were used to make the drive. The sizes are in table 5.4, The output waves are in image 5.5, In terms of output power, image 5.6

Table 5.4: Transistors size and resistance

Number	*PMOS*	*NMOS*
1	$5.69\mu m$	$1.89\mu m$
2	$17.06\mu m$	$5.69\mu m$
3	$51.20\mu m$	$17.06\mu m$

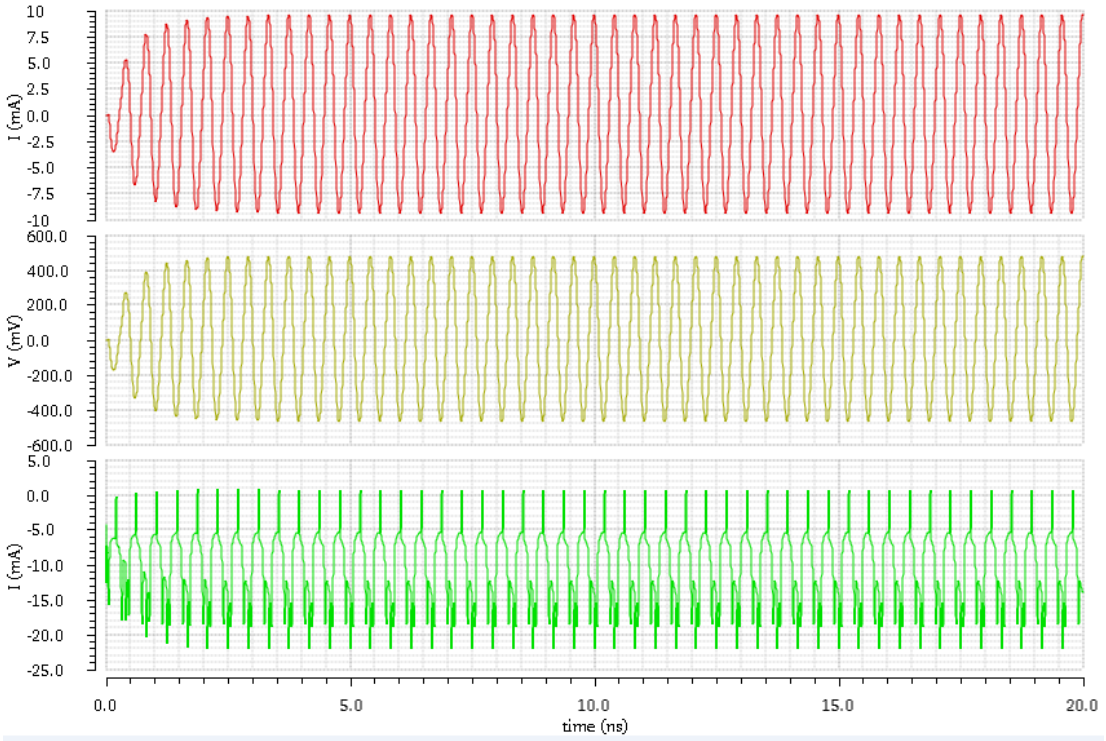


Figure 5.5: The first and second graphic represent the current and voltage at the PA output with the gate driver. The last image is the I_{DC} supplied to the PA and driver.

shows the simulation, The driver as increased the power output, this validate its purpose, driving the parasitic capacitances of the transistors. The power output with the gate

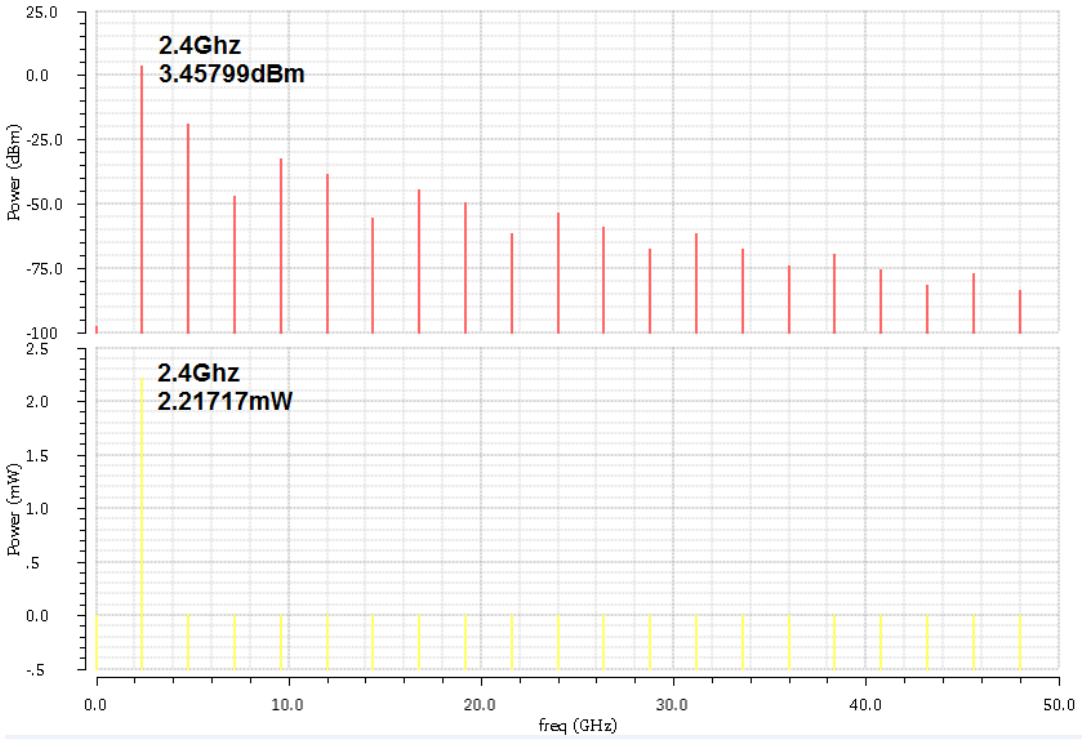


Figure 5.6: PA with driver Output power.

driver is $3.46dBm$. Once again we have all the information to calculate the efficiency of the power amplifier,

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{I_{rms} * Vdd} = 44.5\% \tag{5.10}$$

This result is amazing, with the correct driving of the transistors, not only a power output increase was achieved, but also a major improvement in the efficiency of the Power amplifier.

5.3 Inverter based Class D power amplifier with power combiner - Simulation

Now that the PA is tested and validated was time to use the power combiner to increase the output power without affecting the efficiency. The power combining technique used as mentioned before is series-combining transformer (Voltage-mode).

The first thing was to simulate the system to find the best relation between number of PAs combined versus losses. This tests was performed with the designed PA but with an ideal resonant filter and without a gate driver. The purpose was to avoid losses in the resonant circuit, giving this way a better understanding on the loss mechanism of this power combining technique. The first test was with only two PAs, image 5.7 shows the results, As expected the power output is the double of the power output of only one, power losses are visible but not in a significant matter. The next step is to test the same

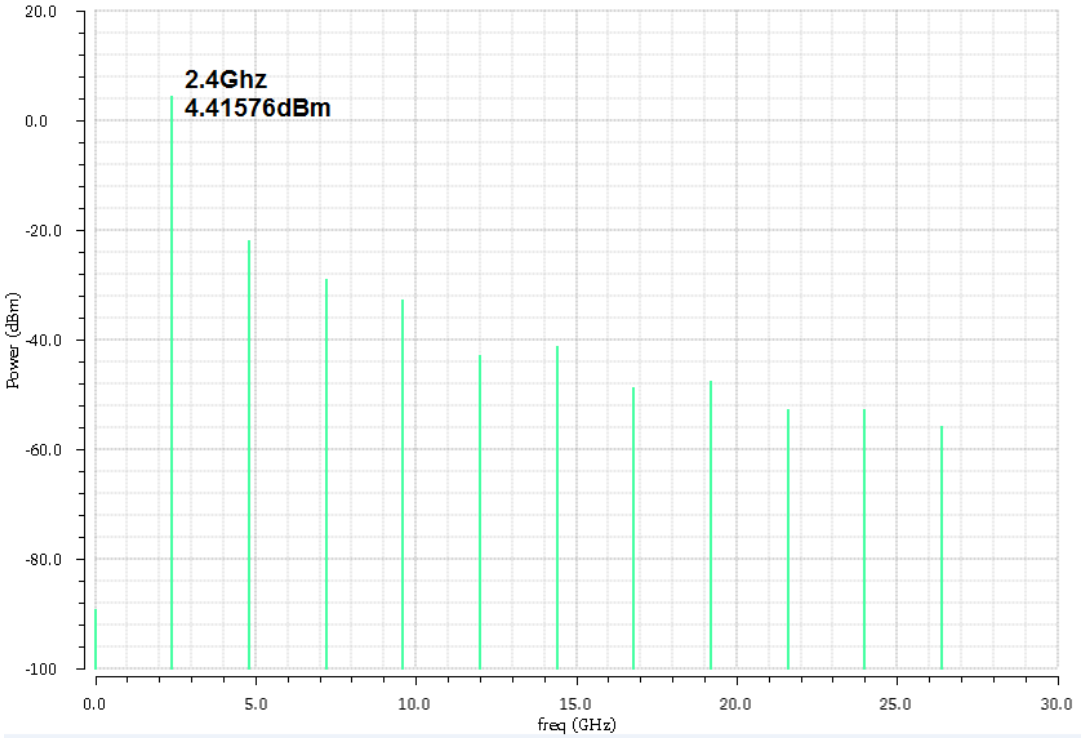


Figure 5.7: Two Class D PAs combined.

architecture but with 4 PAs combined 5.8, We can see that the power output is not two

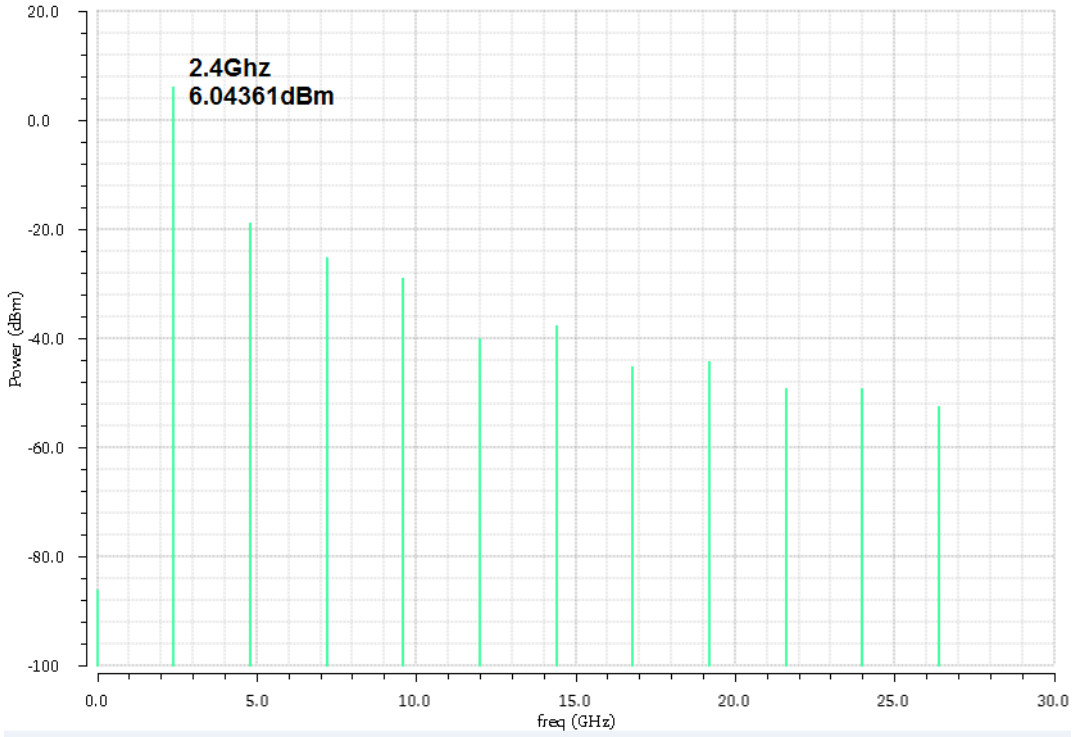


Figure 5.8: Four Class D PAs combined.

times the last results, this is showing the moment where the losses are turning so big that there is no advantage in combining the output of various PAs. The next simulation is with 8 PAs combined, to see if this tendency is true 5.9, We can see that the result is very

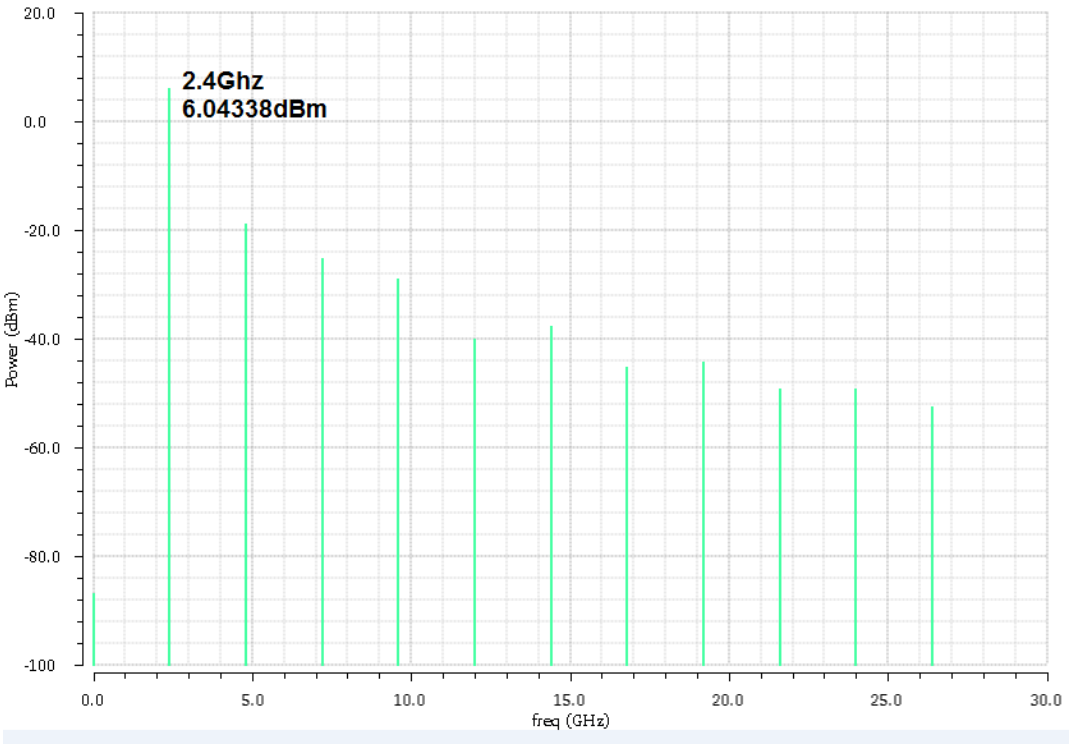


Figure 5.9: Eight Class D PAs combined.

similar to the one with the 4 PAs combined. The reason for that is that we have achieved a point where the losses are so big, that the power output increased obtain is completely lost in the power combiner.

This result was used for the real simulation of the system, as the power output of 0dBm were already achieved with only one PA, there was no need for a great increase of power output. By this reason the power combining architecture is composed for only two PAs. The output voltage wave can be seen in image 5.10, The power output of the system was also simulated 5.11, The efficiency of this system is very low, the reason for that is the big current consumption of all the system plus the losses in the combiner itself. Nevertheless, this type of architecture looks very promising in terms of power control, for example, we can have a situation where in a normal usage only one PA is used but in peaks both are used to increase the output power.

Table 5.5 is a resume of all the results obtained.

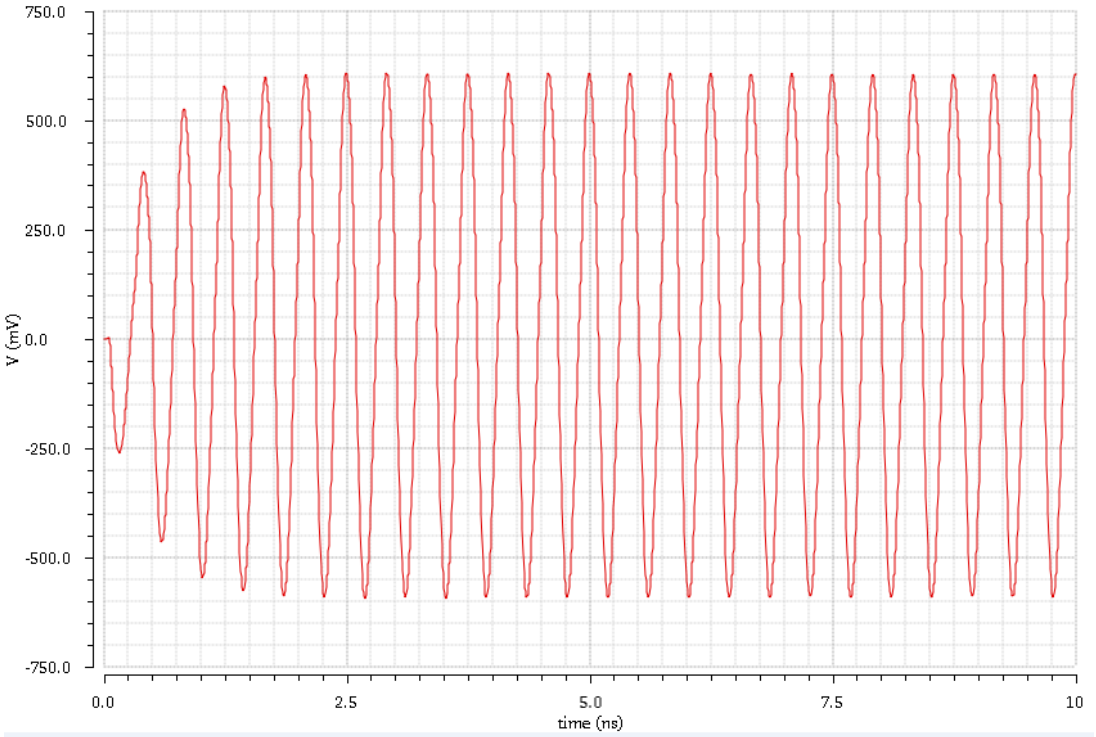


Figure 5.10: Class D PA architecture with power combiner.

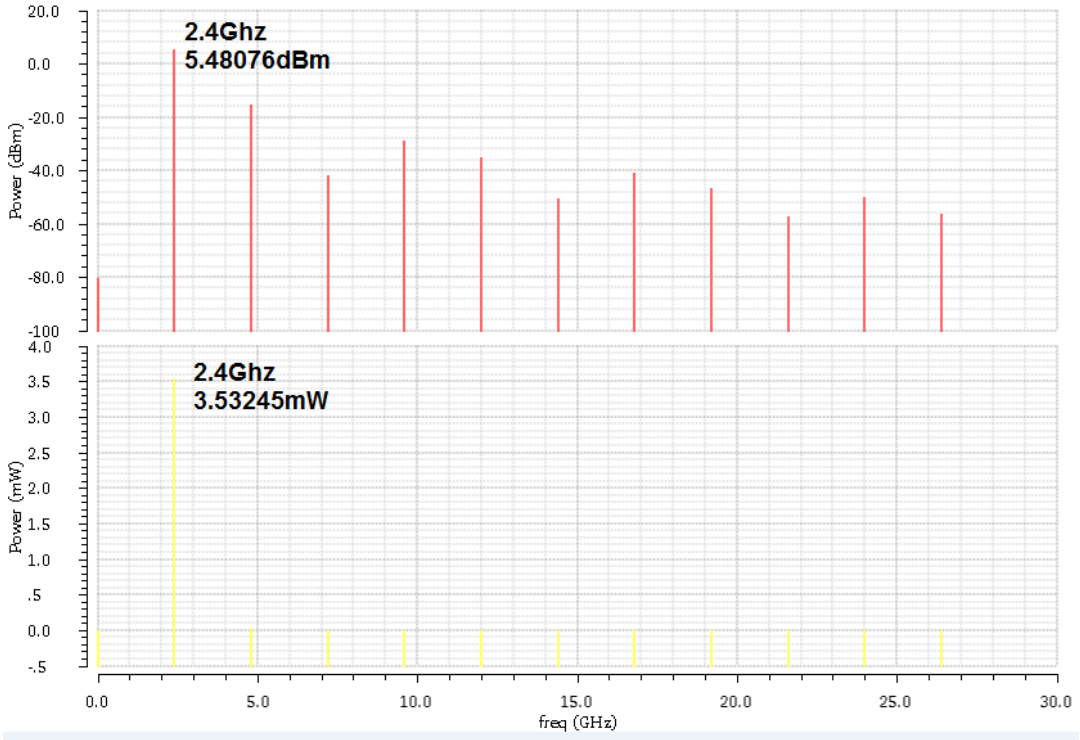


Figure 5.11: Class D PA architecture with power combiner.

Table 5.5: Resume of the inverter based Class D

$ClassD$	η	P_O
Ideal	100%	$7.66dBm$
Non-Ideal	51%	$1.79dBm$
Without Driver	21%	$1.78dBm$
With Driver	44.5%	$3.46dBm$
With Power combiner	–	$5.48dBm$

Chapter 6

Conclusion and Future work

6.1 Conclusion

The objective of this thesis was the design of a high efficiency transmitter front end. In the first part the selection of an appropriated power amplifier was needed. Linear and switched classes were studied in terms of efficiency and output power.

Being the efficiency so important in this RF front end, linear classes were excluded as solutions for the implementation. They have the advantage of amplifying non-constant enveloped signals, but their drain efficiency is not sufficient.

The switched classes have higher efficiency, being in the case of the class D amplifier a theoretical maximum value of 100%. The inverter base class D voltage-switching power amplifier was the architecture selected for implementation.

The high theoretical output power maximum value and an efficiency of 100% were the reasons for that. Looking at the design equations we see that the voltage-switching class-D amplifier have a great dependency of the linear "on"resistance in terms of efficiency. The necessity of a low "on"resistance will force a big size of the transistors. Consequentially the gate parasitic capacitances will increase accordingly. This will force the design of a driver for the correct function of the power amplifier.

The first part of the thesis was the power amplifier design. The simulation of the selected design has given the results of an 44.5% efficiency and a power output of $3.46dBm$. This results are sufficient to comply with the propose specifications. That fact has influenced the second part of the design.

In the second part, the power combiner design was studied to increase the power output of the system without affecting the efficiency. Some tests were performed to see the best relation between power output and power losses in the power combiner architecture. Above 4 power amplifiers the losses were so big that the power output

advantages between, for example, a system with 4 power amplifiers versus the one with 8, will not show a great difference.

The fact that the combination of more power amplifiers will increment the power losses in a big way, and knowing that the base Class-D power amplifier was sufficient to comply with the objectives, only two power amplifiers were combined using the 1-to-1 series-transformer.

The power output of this system was $5.48dBm$ showing an almost multiplication by a factor of 2 in terms of power output related to only one power amplifier. But when the efficiency of the system was calculated the result was a big disappointment. The reason for that was not greatly explored, but some justifications can be found, the first one is the lack of an EM simulation software for the correct design and simulation of the transformer, and the second one a big current consumption caused by both transistors working at the same time, causing a lot of switching losses. Also a bad matching between the load and the power amplifiers with the transformer can be used as reason for the bad efficiency result.

6.2 Future Work

A lot can be done in terms of future work in this thesis, some of these points are addressed:

- Correct design of the power combiner transformer with a correct EM simulation software;
- A study by simulation to have a better understanding of the loss mechanism in the power combiner transformer;
- A frequency study in terms of how a higher frequency will affect the system results. Testing this system for 5G use;
- Testing the system with different modulations to see the differences in terms of performance when a real case usage is applied (like for example in Bluetooth low energy (BLE) modulation techniques);
- Implementation of the RF Class-D amplifier IC layout with the driver and comparison of the simulation results obtained in the layout design with the pre-layout simulation;
- Implementation of the power combiner transformer for an on-chip integrated solution. Simulation of the complete system for results comparison;
- Implementation of the system in a different CMOS technology to compare the advantages and disadvantages of a smaller transistor size technology;
- Fabrication of the IC for testing a comparison with all the simulation results.

We can see that a lot of future work can be done in this thesis, there is a lot of open points that can be explored for not only performance improvement of the power amplifier, but also for the achievement of a final product with a defined usage.

Bibliography

[1] P. M. S. Peynaert. *RF Power Amplifiers for Mobile Communications*. Springer, 2006, p. 257. ISBN: 9781402051166.

[2] T.H.Lee. *The Design of CMOS Radio Frequency Integrated Circuits*. Cambridge University Press, 2004, p. 797. ISBN: 9780521835398.

[3] T. Johansson and J. Fritzin. *A review of Watt-Level CMOS RF power amplifiers*. 2014. DOI: 10.1109/TMTT.2013.2292608. URL: http://ieeexplore.ieee.org/document/6680784/.

[4] J. Scholvin, D. R. Greenberg, and J. A. Del Alamo. "Fundamental power and frequency limits of deeply-scaled CMOS for RF power applications". In: *Technical Digest - International Electron Devices Meeting, IEDM*. IEEE, 2006, pp. 1–4. ISBN: 1424404398. DOI: 10.1109/IEDM.2006.347001. URL: http://ieeexplore.ieee.org/document/4154436/.

[5] U. Gogineni, J. D. Alamo, and C. Putnam. "RF power potential of 45 nm CMOS technology". In: *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2010 Topical Meeting on* (2010), pp. 204–207. DOI: 10.1109/SMIC.2010.5422960. URL: http://ieeexplore.ieee.org/document/5422960/.

[6] B. Razavi. *Design of analog CMOS integrated circuits*. McGraw-Hill, 2000, p. 684. ISBN: 0070529035. URL: http://portal.acm.org/citation.cfm?id=1594009.

[7] K. H. An, O. Lee, H. Kim, D. H. Lee, J. Han, K. S. Yang, Y. Kim, J. J. Chang, W. Woo, C. H. Lee, H. Kim, and J. Laskar. "Power-combining transformer techniques for fully-integrated CMOS power amplifiers". In: *IEEE Journal of Solid-State Circuits*. Vol. 43. 5. 2008, pp. 1064–1074. ISBN: 0018-9200. DOI: 10.1109/JSSC.2008.920349. URL: http://ieeexplore.ieee.org/document/4494643/.

[8] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri. "A 2.4-GHz, 2.2-W, 2-V fully-integrated CMOS circular-geometry\nactive-transformer power amplifier". In: *Proceedings of the IEEE 2001 Custom Integrated Circuits Conference (Cat. No.01CH37169)* (2001), pp. 57–60. ISSN: 08865930. DOI: 10.1109/CICC.2001.929723. URL: http://ieeexplore.ieee.org/document/929723/.

[9] A. Afsahi and L. E. Larson. "An integrated 33.5dBm Linear 2.4GHz power amplifier in 65nm CMOS for WLAN applications". In: *Proceedings of the Custom Integrated Circuits Conference*. IEEE, 2010, pp. 1–4. ISBN: 9781424457588. DOI: 10.1109/CICC.2010.5617401. URL: http://ieeexplore.ieee.org/document/5617401/.

[10] B. Razavi and R Behzad. *RF microelectronics 2nd edition*. Prentice Hall, 1998. ISBN: 9780137134731. DOI: 0137134738978013713473 1. arXiv: 0137134738978013713473 1. URL: ftp://doc.nit.ac.ir/cee/m.zahabi/BOOKS/CommCircuits/RFRazavi/Chapter1.pdf.

[11] B. Razavi. "A study of injection locking and pulling in oscillators". In: *IEEE Journal of Solid-State Circuits* 39.9 (2004), pp. 1415–1424. ISSN: 0018-9200. DOI: 10.1109/JSSC.2004.831608. URL: http://ieeexplore.ieee.org/document/1327738/.

[12] H. Solar Ruiz and R. Berenguer. *Linear CMOS RF power amplifiers : a complete design workflow*, p. 185. ISBN: 9781461486572.

[13] W. Y. Hu, J. W. Lin, K. C. Tien, Y. H. Hsieh, C. L. Chen, H. T. Tso, Y. S. Shih, S. C. Hu, and S. J. Chen. "A 0.18-μm CMOS RF transceiver with self-detection and calibration functions for bluetooth V2.1 + EDR applications". In: *IEEE Transactions on Microwave Theory and Techniques*. Vol. 58. 5 PART 2. 2010, pp. 1367–1374. DOI: 10.1109/TMTT.2010.2042908. URL: http://ieeexplore.ieee.org/document/5438826/.

[14] P. Zhang, L. Der, D. Guo, I. Sever, T. Bourdi, C. Lam, A. Zolfaghari, J. Chen, D. Gambetta, B. Cheng, S. Gowder, S. Hart, L. Huynh, T. Nguyen, and B. Razavi. "A single-chip dual-band direct-conversion IEEE 802.11a/b/g WLAN transceiver in 0.18-μm CMOS". In: *IEEE Journal of Solid-State Circuits*. Vol. 40. 9. 2005, pp. 1932–1937. ISBN: 0018-9200. DOI: 10.1109/JSSC.2005.848182. URL: http://ieeexplore.ieee.org/document/1501993/.

[15] T. Sowlati et al. "Single-chip multiband WCDMA/HSDPA/HSUPA/EGPRS transceiver with diversity receiver and 3G DigRF interface without SAW filters in transmitter / 3G receiver paths". In: *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*. IEEE, 2009, 116–117,117a. ISBN: 978-1-4244-3458-9. DOI: 10.1109/ISSCC.2009.4977335. URL: http://ieeexplore.ieee.org/document/4977335/.

[16] Kazimerczuk Marian. *RF Power Amplifiers*. Vol. 1. 2008, p. 428. ISBN: 9788578110796. DOI: 10.1017/CBO9781107415324.004. arXiv: arXiv:1011.1669v3.

[17] T. Andersson and J. Wahlsten. "\deltaΣ-modulation Applied to Switching RF Power Amplifiers". PhD thesis.

[18] V. J. Tyler. *A new high-efficiency high-power amplifier*. vol. 21, n. Marconi Review, 1958, pp. 96–109.

[19] P. Baxandall. "Transistor sine-wave LC oscillators. Some general considerations and new developments". In: *Proceedings of the IEE - Part B: Electronic and Communication Engineering* 106.16S (1959), pp. 748–758. ISSN: 2054-0418. DOI: 10.1049/pi-b-2.1959.0141. URL: http://digital-library.theiet.org/content/journals/10.1049/pi-b-2.1959.0141.

[20] T. C. Carusone, D. Johns, K. W.K. W. Martin, and D. Johns. *Analog integrated circuit design*. John Wiley & Sons, 2012, p. 794. ISBN: 9780470770108.

[21] B. Cordell. *Designing audio power amplifiers*. McGraw-Hill, 2011, p. 608. ISBN: 007164024X.

[22] J. E. Ayers. *Digital integrated circuits : analysis and design*. CRC Press, 2010, p. 597. ISBN: 142006987X.

[23] K. H. Abed, K. Y. Wong, and M. K. Kazimierczuk. "CMOS zero cross-conduction low-power driver and power MOSFETs for integrated synchronous buck converter". In: *ISCAS 2006: 2006 IEEE International Symposium on Circuits and Systems, May 21, 2006 - May 24, 2006*. IEEE, 2006, pp. 2745–2748. ISBN: 02714310. DOI: 10.1109/ISCAS.2006.1693192. URL: http://ieeexplore.ieee.org/document/1693192/.

[24] M. Kazimierczuk and J. S. Modzelewski. "Drive-Transformerless Class-D Voltage-Switching Tuned Power Amplifier". In: *Proceedings of the IEEE* 68.6 (1980), pp. 740–741. ISSN: 15582256. DOI: 10.1109/PROC.1980.11727. URL: http://ieeexplore.ieee.org/document/1455996/.

[25] T. Wang, L. P. Chiang, N. K. Zous, C. F. Hsu, L. Y. Huang, and T. S. Chao. "A comprehensive study of hot carrier stress-induced drain leakage current degradation in thin-oxide n-MOSFET's". In: *IEEE Transactions on Electron Devices* 46.9 (1999), pp. 1877–1882. ISSN: 00189383. DOI: 10.1109/16.784188. URL: http://ieeexplore.ieee.org/document/784188/.

[26] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. John Shen. "New physical insights on power MOSFET switching losses". In: *IEEE Transactions on Power Electronics* 24.2 (2009), pp. 525–531. ISSN: 08858993. DOI: 10.1109/TPEL.2008.2006567. URL: http://ieeexplore.ieee.org/document/4783535/.

[27] A. J. Frazier and M. K. Kazimierczuk. "DC-AC power inversion using Σ-Δ modulation". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 47.1 (2000), pp. 79–82. ISSN: 10577122. DOI: 10.1109/81.817396. URL: http://ieeexplore.ieee.org/document/817396/.

[28] I. Aoki, S. D. Kee, D. B. Rutledge, and A. Hajimiri. "Fully integrated CMOS power amplifier design using the distributed active-transformer architecture". In: *IEEE Journal of Solid-State Circuits* 37.3 (2002), pp. 371–383. ISSN: 00189200. DOI: 10.1109/4.987090. URL: http://ieeexplore.ieee.org/document/987090/.

[29] J. R. Long. "Monolithic transformers for silicon RF IC design". In: *IEEE Journal of Solid-State Circuits* 35.9 (2000), pp. 1368–1382. ISSN: 00189200. DOI: 10.1109/4.868049. URL: http://ieeexplore.ieee.org/document/868049/.

[30] J. C. Costa. "Analysis of integrated transformers and its application to rfic design". PhD thesis. Universitat de Barcelona, 2002. URL: https://dialnet.unirioja.es/servlet/tesis?codigo=3191.

[31] L. Wanhammar. *Analog filters using MATLAB*. Boston, MA: Springer US, 2009, pp. 1–316. ISBN: 9780387927664. DOI: 10.1007/978-0-387-92767-1. URL: http://link.springer.com/10.1007/978-0-387-92767-1.