João Pedro Castro da Rocha de Meneses Alarcão

Licenciado em Ciências de Engenharia Eletrotécnica
e de Computadores

Design of a Multi-sensor and Re-configurable Smart Node for the IoT

Dissertação para obtenção do Grau de Mestre em

Engenharia Eletrotécnica e de Computadores

Orientador: João Pedro Oliveira, Prof. Doutor, Universidade Nova de Lisboa - Faculdade de Ciências e Tecnologia

Júri

Presidente:	Doutor Luis Filipe Lourenço Bernardo - FCT/UNL
Arguente:	Doutor João Carlos da Palma Goes - FCT/UNL
Vogal:	Doutor João Pedro Abreu de Oliveira - FCT/UNL

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

September, 2017

Design of a Multi-sensor and Re-configurable Smart Node for the IoT

Este documento foi gerado utilizando o processador (pdf)LaTeX, com base no template "novathesis" [1] desenvolvido no Dep. Informática da FCT-NOVA [2].
[1] https://github.com/joaomlourenco/novathesis [2] http://www.di.fct.unl.pt

I would like to dedicate this thesis to my family.

Acknowledgements

I hereby express my deepest thanks, first of all for the sympathy and hard work of Professor João Pedro Oliveira, in the accompaniment and the advice that he gave me along the course of this thesis. I would also like to thank him for the opportunity he gave to me, to have had the pleasure of my thesis being part of the research project taking place in Unicova CTS, headed by the Professor. I am grateful for the opportunity I had to learn from his vast experience and expertise and to have worked with him on the project. I would also like to thank Prof. Rui Tavares, for the help and guidance he offered me, during the work that involved CADIT.

Secondly, I would like to thank my UNINOVA-CTS co-workers, pointing out Nuno Correia, Ricardo Madeira, Hugo Silva, Ivan Bastos for company, support and availability in helping me in my work.

Thirdly, I would like to thank my family for the support they gave me, for the patience they had and for the advice they gave me throughout my academic journey.

And lastly, I would like to thank all my friends, in particular, Tomas Oliveira and Tiago Vieira for their friendships and for the good times we spent that gave me good distractions.

Abstract

The rapid deployment of the Internet of Things (IoT) is much dependent on the capacity of the IoT node to be able to self-adapt to the target application. With the increase of sensor networks and diversity of sensors available and with the increasing integration of multiple sensors in a sensor node, it is necessary to develop systems capable of handling all of these sensors with high level of flexibility. These may have different characteristics that provide quite distinct interface requirements, thus giving rise to the need for systems with re-configurable properties. With the implementation of sensor networks in places where energy supply is limited or non-existent, and in situations where technician intervention is expensive, there is a need to exchange conventional energy sources by methods of storage and harvesting of the energy present in the environment, where the sensor node is used (autonomous and renewable energy sources). This thesis will focus on the study and implementation of a family of re-configurable and multi-sensor IoT nodes with special emphasis on the energy storage and power management. It will also focus on the develop of a CAD tool in order to help in the design of CMOS circuits, for the purpose of integrating all the strategies here presented.

Keywords: Soc, FPGA, IOT, Sensor, Self-adapt, Re-configurability, Super Capacitor, Renewable Energy, Energy Storage, Power Management, CAD.

Resumo

A implantação rápida da Internet das coisas (IoT) depende muito da capacidade do nó do IoT para se adaptar ao aplicativo de destino. Com o aumento das redes de sensores e a diversidade de sensores disponíveis e com a crescente integração de múltiplos sensores em um nó de sensores, é necessário desenvolver sistemas capazes de lidar com todos esses sensores com um nível alto de flexibilidade. Estes podem ter características diferentes que fornecem requisitos de interface bastante distintos, dando origem à necessidade de sistemas com propriedades reconfiguráveis. Com a implementação de redes de sensores em locais onde o fornecimento de energia é limitado ou inexistente, e em situações em que a intervenção do técnico é dispendiosa, é necessário trocar fontes de energia convencionais por métodos de armazenamento e colheita da energia presente no meio ambiente, onde o nó de sensores é usado (fontes de energia autônomas e renováveis). Esta tese incidirá no estudo e implementação de uma família de nós, para a IoT, reconfiguráveis e multisensores com ênfase especial no armazenamento de energia e no seu gerenciamento. Também se concentrará no desenvolvimento de uma ferramenta de CAD para ajudar na concepção dos circuitos CMOS, com a finalidade de integrar todas as estratégias aqui apresentadas.

Palavras-chave: Soc, FPGA, IOT, Sensor, auto-adaptar-se, reconfigurabilidade, Super Condensador, energias renováveis, armazenamento de energia, gerenciamento de energia, CAD.

Contents

List of Figures

List of Tables

Listings

Acronyms

A

AC Alternating Current.

ADC Analog to Digital Converter.

AFE Analog Front End.

ASIC Application Specific IC.

B

BGA Ball Grid Array.

BLE Bluetooth Low Energy.

BSIM Berkeley Short-channel IGFET Model.

C

CAD Computer Aided Design.

CADIT Computer Aided Design Integration Tool.

CG Common Gate.

CM Communication Module.

CMOS Complementary Metal Oxide Semiconductor.

CNT Carbon Nanotube.

CPLD Complex Programmable Logic Device.

CPU Central Processing Unit.

CS Common Source.

D

DAC Digital to Analog Converter.

DC Direct Current.

DPU Digital Processing Unit.

DSP Digital Signal Processor.

E

ESR Equivalent Series Resistance.

F

FPAA Field Programmable Analog Array.

FPGA Field Programmable Gate Array.

G

GUI Graphical User Interface.

I

I2C Inter-Integrated Circuit.

IC Integrated Circuits.

IEEE Institute of Electrical and Electronics Engineers.

IoT Internet of Things.

J

JTAG Joint Test Action Group.

L

LED Light Emitting Diode.

LNA Low Noise Amplifier.

LSB Least Significant Bit.

M

MEMS Micro-Electro-Mechanical System.

MIXDES Mixed Design of Integrated Circuits and Systems.

MOSFET Metal Oxide Semiconductor Field Effect Transistor.

MSB Most Significant Bit.

MUX Multiplexer.

N

NF Noise Figure.

O

OP Operating Point.

P

PCB Printed Circuit Board.

PMU Power Management Unit.

Q

QFN Quad Flat No leads.

R

RF Radio Frequency.

S

SAR Successive Approximation Register.

Si2 Silicon Integration Initiative.

SiP System in a Single Package.

SoC System in a Single Chip.

SPI Serial Peripheral Interface.

T

TF Transfer Function.

U

UART Universal Asynchronous Receiver/Transmitter.

UNB Ultra Narrow Band.

UWB Ultra Wide Band.

V

VLSI Very-Large-Scale Integration.

W

WSN Wireless Sensor Network.

Z

Zin Input Impedance.

CHAPTER 1

INTRODUCTION

1.1 Motivation and Background

The Internet of Things (IoT) is pulling the physical and virtual objects into an ecosystem of global information combining advanced wireless connectivity, advances in micro and nanotechnologies, energy harvesting and storage, and more data storage and signal processing capacity. This is forcing significant changes in traditional sensor monitoring micro-systems, namely in terms of cost and flexibility. This flexibility requires the use of multiple sensor nodes capable of interact within a mesh communication network and their operation is required to be easily re-configurable. Another aspect is the management of energy and power inside the IoT, which must be designed in order to allow the operation of the node with reduced maintenance cost (for example, for battery replacement).

The IoT paradigm is being introduced in many types of applications. For example, in the field of water quality monitoring, strong developments efforts are targeting its widespread use over public water networks, supported on compact and energy autonomous multi-sensor node probes based on low-cost sensor technologies, e.g. Micro-Electro-Mechanical System (MEMS) and Carbon Nanotube (CNT), co-integrated with a System in a Single Chip (SoC) designed in a low-cost standard Complementary Metal Oxide Semiconductor (CMOS) technology[1].

The typical architecture of the IoT node consists of four main subsystems, which are the Analog Front End (AFE) module, the Digital Processing Unit (DPU), the Communication Module (CM) and Power Management Unit (PMU). Figure 1.1 shows a simplified block diagram of an IoT node.

The AFE subsystem is responsible for the acquisition and conditioning of the analog

[1] PROTEUS project which is an European Union's H2020 Programmed for research, technological development and demonstration under grant agreement No 644852 http://www.proteus-sensor.eu/

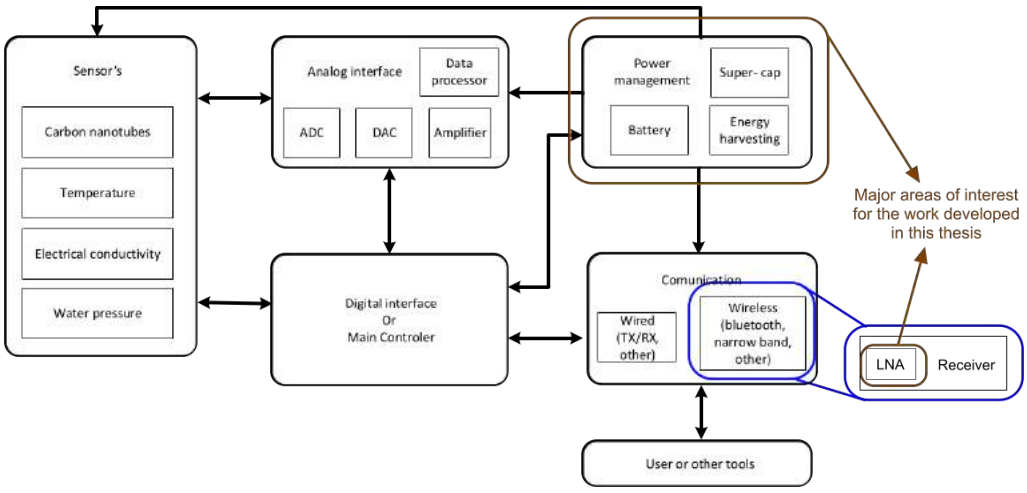


Figure 1.1: Diagram of the project system proposed architecture.

signals delivered by the sensors. Besides these tasks, the AFE also incorporates a high resolution Analog to Digital Converter (ADC) whose output is further processed by the digital subsystem. The latter is also responsible for the operation of the complete node. Another important block is the CM which deals with the exchange of information between the node and the Cloud based application. For the case of wireless communications, the trend now is that this module can support multiple standards and multiple radio bands, meaning that the Radio Frequency (RF) front-end must be designed accordingly. The Low Noise Amplifier (LNA), which is part of the RF front-end, plays an important role since it must have a wideband characteristic in order to support multiple radio bands. This is one of the topics covered in this dissertation, in the context of full integration either by using a SoC or System in a Single Package (SiP) approaches, in order to reduce the device size.

Another topic is the PMU which is responsible for the harvesting, storage and supply of energy to the IoT node. To improve flexibility, multi-source energy harvesting sources is a trend in the modern IoT node design. Additionally, the PMU has to be able to recognize the power requirements needed by each node subsystem and correctly manage the balance and flux of energy between the harvesters, the energy storage elements and the circuits.

1.2 Overview and Contributions

Focusing on the design aspects of the IoT node, the contributions of this thesis are divided in three areas, including circuit design optimization software, PMU and multi-sensor IoT node implementation, as briefly described in the following list:

- For the SoC integration design using standard CMOS technology, is developed an automated software design tool for the optimization and sizing of a wideband LNA

with noise canceling, which is the first stage of a receiver in the communication block. Optimization circuit design algorithms were implemented and grouped in a single software package with a Graphical User Interface (GUI). The software allows the extraction of the transfer functions regarding the single ended and differential gain of the LNA as well as the Input Impedance (Zin) and the Noise Figure (NF), considering device noise sources and parasitics. A symbolic extraction tool and modified node analysis is used to achieve the desired outputs. This work has originated a publication in Institute of Electrical and Electronics Engineers (IEEE) Mixed Design of Integrated Circuits and Systems (MIXDES) conference, entitled "Analysis of a Noise Canceling LNA using a Si2 OpenAccess based Tool - CADIT" [3].

- Design, implementation and testing of a PMU prototype capable of managing and monitoring the flow of energy between multiple energy harvesting sources (both Alternating Current (AC) and Direct Current (DC) type), multiple energy storage elements (including super-capacitors and lithium battery) and the modules of IoT node that requires energy to operate.

- Implementation and testing of a multi-sensor IoT node, designed using a modular approach for increasing the reconfigurability. The resulting implementation, designated by "Rolling Probe" has received the second prize in the 2016 International Contest of Innovation ICAN'16[2], Paris-France.

The output of the work was partially included in the research project PROTEUS[3]. The existance of PROTEUS is due to the fact that "water is a vital to all forms of life (human, animal and plant) and its quality is essential to people health. It is also an unavoidable component in a wide range of industrial process, from energy production to construction activities or food production. (...) Therefore, the production of water quatity and quality is among the cornerstones of environmental protection schemes worldwide" [2]. This being said the overall objective of the project is to have an autonomous, highly multi-functional node sensor capable of monitoring drink and waste water quality in an adaptive and cognitive way, enabling a single device to support different application goals related to water monitoring networks. The final goal of Proteus is to give the roots for a full integration of all systems and sub-systems in a single SoC/SiP device.

[2]International Contest of innovation, shorted as iCAN. It's globally co-organized by the iCAN Association, ESIEE, ENS, Peking University, VDE, IEEE NTC, ANF, MEMS Park Consortium, Nano-Tera and Chinese International NEMS Society.

[3]This project has received funding from the European Union's H2020 Programme for research, technological development and demonstration under grant agreement No 644852. http://www.proteus-sensor.eu/

1.3 Thesis Organization

This dissertation is divided into six chapters and several appendixes. The first chapter introduces the objectives and gives an overview of the main contributions. In the context of the IoT, the second chapter addresses the design considerations and principles of the IoT node. It illustrates the general ideas behind the work developed under the project in which this dissertation was included. Chapter three deals with the design, implementation and testing of a power and energy management prototype for the IoT node. Still in the scope of the IoT node design, the fourth chapter presents the implementation of a software tool used for the circuit design optimization using nano-scale CMOS technologies. Chapter five presents the implementation of a IoT node for multi-sensor applications, as is the case of the quality monitoring systems. The last chapter presents the conclusions and future work topics. To support the main content of this document, several appendixes are included with additional information.

1.4 Software Used in this Thesis

For the development of the work done in this thesis it is necessary the use of different types of software, from simulators to editors for programming code.

In relation to the work carried out in chapter 3, that refers to the study done in the area of power management and in chapter 5, the design of a smart node, the following software's were used:

- EAGLE from AUTODESK, it was used to design the Printed Circuit Board (PCB) of both prototypes (physical implementation of the systems);
- LTSPICE from Linear technology and TINA from Texas Instruments, they were used to simulate the behavior of several components;
- Code Composer from Texas Instruments, was used for programming C code to be loaded in the MSP430 microcontroller;
- LabVIEW from National Instruments, was used to implement a graphical interface to display data from the prototype (PMU).

For chapter 4, the development of a Computer Aided Design (CAD) tool to help in the designed of circuits, the following software's were used:

- MATLAB and MATLAB engine from MathWorks, was used for graphical representation of data (graphics) and calculation of the node equations (modified node analysis);
- Virtuoso and Specter from Cadence, was used for simulating CMOS circuits;

- Microsoft Visual Studio from Microsoft, was used to designed, in C++, a graphical interface for control;
- OpenAccess from Silicon Integration Initiative (Si2), was used for storing circuit data (netlist).

Chapter 2

Design Considerations for the Multi-sensor IoT Node

2.1 Introduction

This chapter presents the main aspects to take into account when designing a multi-sensor IoT node. This chapter begins by introducing the concept of IoT, and then centers the discussion around the IoT node. A module-based architecture is advocated with special emphasis on the PMU. Finally, system integration in SoC & SiP is referred, highlighting the need for tools dedicated to circuit design optimization.

2.2 Internet of Things (IoT)

The first step into what is known today as the IoT was the concept of the Wireless Sensor Network (WSN) which is defined as "A Wireless Sensor Network can generally be described as a network of nodes that cooperatively sense and may control the environment, enabling interaction between persons or computers and the surrounding environment", [26]. The WSN are constituted by "node sensors and actuators", which may include a gateway to bridge to a different network or to connect to a user/client, as demonstrated in figure 2.1. Usually the network contains multiple nodes with a random distribution within an area in which it is desired to monitor. Advanced techniques of self-adaptation and self-organization were proposed in the past to improve not only the interconnectivity and interoperability between nodes but also to optimize the overall energy consumption of the entire system, [34, 48].

However, to cope with the interoperability between WSN and other Internet system applications, the IoT concept has emerged. One of the definitions of IoT is the ability an object has to connect to a communication network and to exchange information, i.e., any

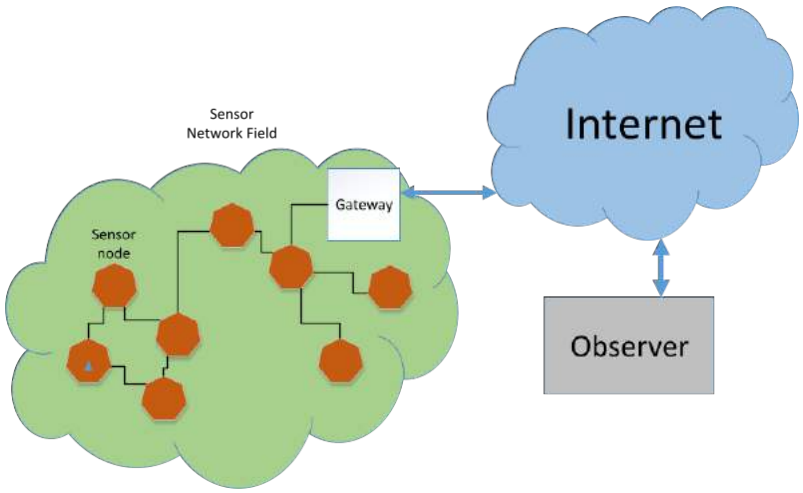


Figure 2.1: Wireless sensor networks.

object can connect to the Internet and share information with other devices, similar or not, to supply and access all of real-world information. With the increased use of various types of sensors and the potential massive information data, there is now a need to connect all of these IoT nodes to Cloud scaled technologies (processing, storing data) using the services provided by the Internet. This is now possible due to advances in wireless communications, distributed computation process and fast speed Internet, [38]. In fact, objects with sensors, actuators and controllers can now be connected to the Internet and controlled remotely, linking the physical world to cyberspace through the smart device. Everyday object can now be an extension of the Internet into the real world,[4], [20]. The potential of IoT spreads in a large variety of applications, namely ([4, 8, 20, 32]):

- Smart Home/Smart Building, to improve energy efficiency and smarter home environments;
- Health-care and Wearables, as for example in the case of elderly care;
- Smart Environment Monitoring/Smart Cities, namely for monitoring and control traffic flows, city logistics, water quality monitoring and rational use of water resources;
- Security and Safety.

2.3 The IoT Node

The IoT node is the most important element in a sensor/actuator network. It has the capability to acquire data from sensors, processing them and sending them to other entities. It is usually made up of a power management module, a multiple-sensor and AFE module, a microcontroller, and a wireless transceiver [9, 23, 52]:

- The power management module is responsible for provide a reliable power supply to the node;
- The sensor allows the node to acquire information about environmental and equipment status. It is responsible for collecting and conditioning the signals, such as light, vibration and chemical signals, into electrical signals;
- The micro-controller processes the digital/analog signals coming from the sensors units;
- The wireless transceiver (RF module) provides the bidirectional connectivity with the Cloud application.

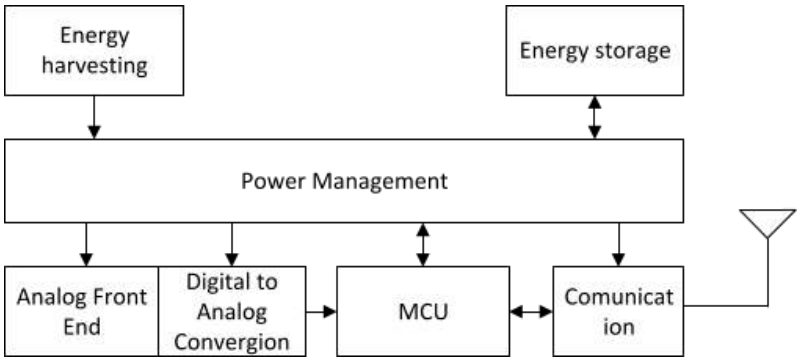


Figure 2.2: Node sensor architecture.

It is necessary to take into account the importance of node features of tiny size and limited power in the design of all components of the sensor network [10, 23, 26]. As reported in [27], it's possible to identify slightly differences in the way the sensor architecture is built:

- based only on a Micro-controller,
- based on Digital Signal Processor (DSP),
- based on Application Specific IC (ASIC),
- based on programmable hardware devices (Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD)),
- using Field Programmable Analog Array (FPAA),
- based on SiP or SoC,
- based on mix combination of the above architectures.

2.3.1 Sensors

The most common type of sensors are fabricated in discrete packages being some of them inexpensive and easy to use. However, with the need of small form factors nodes, it is necessary to co-integrate the sensors along with the SiP or SoC. With the miniaturization technology based on MEMS, it is now possible to combine microelectronics with micro-machining technology in 2D or 3D micro-packaging structures. Integrating these structures with power harvesting supply and signal conditioning circuits we obtained miniature MEMS based node sensors. At present, there are already many types of miniature MEMS sensors in the market which can be used to measure a variety of physical, chemical and biomass signals, including displacement, velocity, acceleration, pressure, stress, strain, sound, light, electricity, magnetism, heat, pH value [11, 14–16, 25, 26].

2.3.2 Connectivity

The IoT node can now select a variety of communication standards, with some of the most used highlighted below:

- Bluetooth Low Energy (BLE),[12],
- ZigBee, [17],
- Ultra Narrow Band (UNB),
- Ultra Wide Band (UWB),[7].

One of the criteria for the choice of a transceiver is the coverage range for a given transmission type attending to the energy available at the node.

2.3.3 Energy and Power Management

Power management is the most important aspect of sensor node. It is responsible for supplying the energy to the entire node. The energy problem in a sensor node is that there is not always enough energy available, especially if the system uses only the energy supply via batteries. Therefore, to be autonomous the node energy paradigm has to change in the sense that it needs to harvest and store locally energy form the environment. As a consequence, the IoT node must be able to manage its energy consumption by applying a smart energy-saving mechanism to become efficient and prolong the life operation of the node, [19]. A sensor node can benefit from using techniques like scheduling their operations in time, when there is not sufficient energy to maintain the continuous operation of all subsystems, [36].

One of the modules with potential to consume a significant amount of energy is the wireless communication module. Techniques related with the operational state machine like putting the wireless communication module in send, receive, idle or sleep states can reduce the average power consumption. For example, an idle state can be used to monitor

the wireless radio channel, but not to send or receive any sensor data, while a sending state is only activated when there is useful data to be transmitted. Outside of these states, the module is in sleep mode (ultra-low power consumption). Also, to reduce the node energy consumption we can reduce the communication time, reduce the traffic (through data compression to reduce redundant data sent) and reduce the transmitted power of the sending node, [13].

2.3.3.1 Energy Harvesting

The use of energy harvesting gives the ability to node sensor to extend their operating live, [28]. As reported in [7, 26] "Ambient energy harvesting cannot only be realized by conventional optical cell power generation, but also through miniature piezoelectric crystals, micro-oscillators, thermoelectric power generation elements, or electromagnetic wave reception devices". Two types of energy harvesters, [13] are:

- Vibration energy is obtained by the use of piezoelectric materials. By applying a force, the material deforms which produce a polarization charge that can be used to extract energy;
- Solar energy through the use of advanced photoelectric technology can operate both indoor or outdoor and they are lightweight and easy to install.

There are two major approaches in how a system may collect and use the energy of the environment in which it will be inserted [39]:

- Harvest-Use Architecture: the energy harvested is directly used by the the sensor, this means that it can only operate if there is available power continuously over a level that allows their operation, otherwise the node crashes due to insufficient power.
- Harvest-Store-Use Architecture: energy is stored before being used which allows the node operation when the harvester is not available to to provide power.

2.3.3.2 Energy Storage

The combination of energy harvesters with energy storage elements is a key principle to obtain an autonomous IoT node, [39]. Sensor nodes can benefit from two main types of storage elements: battery and super-capacitors.

Batteries are expensive and have a limited useful life (limited number of recharge cycles), has however high output voltage, high energy density, and moderately low self-discharge rate. They may also need special charging circuits which increases the complexity of the system design. Two storage technologies, NiMH and Lithium based, emerge as good choices.

The supercapacitors can be an alternative to the battery, since they require no special charging circuitry, and can be directly connected to a DC power source. In case of an AC

power source, a rectifier is needed. One disadvantage is the fact that the supercapacitor self-discharges at a much higher rate than battery, [49]. The advantage that have influenced the use of supercapacitors is its much higher power density and low Equivalent Series Resistance (ESR). Also, a typical supercapacitor supports a much higher number of charging cycles, [37].

2.4 Design considerations

Due to the increasing integration of IoT systems into an enormous diversity of applications, each with different characteristics but requiring the same electronic platform (sensor node), it is necessary to look for systems capable of following the requirements that IoT requires.

For this, each sensor node must have three main characteristics:

- Processing capacity, that allows the control of all aspects of the system and implementation of algorithms for signal processing;
- Ability to read the physical world (using sensors);
- Autonomy, being active and function properly for long periods of time without any intervention needed.

2.4.1 Analog Front End (AFE)

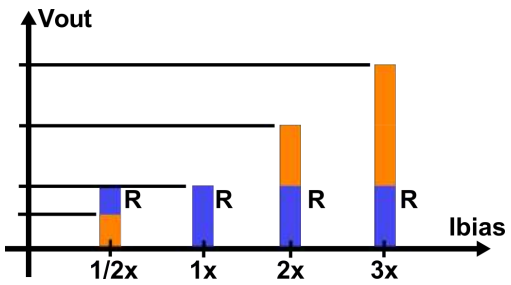
The AFE establish the interface between the sensor and the digital part. It comprises sensor biasing, sensor signal readout and conditioning and an ADC.

2.4.1.1 Sensor Biasing

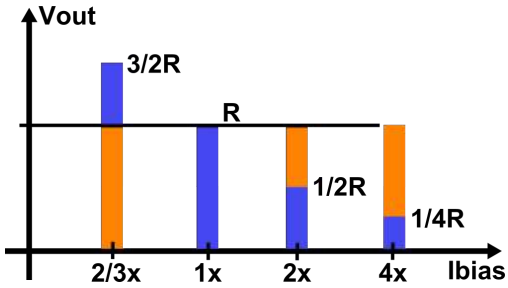
The analogue interface for sensing the physical environment needs to adapt to the diverse characteristics of the sensors. Most analog sensors need to employ some method of biasing (for establishing proper operating conditions), and this varies from sensor to sensor. In order to have some control over that parameter a biasing interface (polarization circuit) is needed that can generate variable voltages or currents. For this, the use of Digital to Analog Converter (DAC) is employed.

In most sensors the biasing can be used to define the range of values to be read. If the value is greater than the limits of the ADC it is possible to adjust the biasing, as demonstrated in figure 2.3. This method provides the use of a single biasing circuit for multiple sensors through multiplexing.

Otherwise applying a constant biasing for each sensor means an increase of the number of required circuits, resulting in an increase in power consumption and the loss of re-configurability.

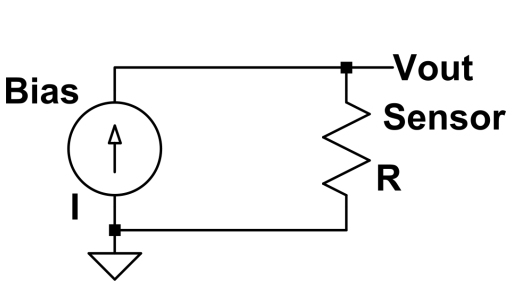


(a) Different biasing for the same resistance. By applying different biasing current to the same resistor, the output voltage can be increased or decreased.

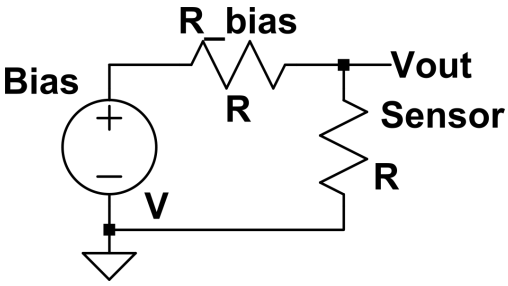


(b) Different biasing for the different resistance. By applying different biasing current to different resistors, the output voltage is the same for all.

Figure 2.3: Biasing graphics (sensor output amplification).



(a) Current biasing method.



(b) Voltage biasing method.

Figure 2.4: Polarization circuit for resistive sensors.

It's possible to use two types of biasing circuits, either using current or voltage, as shown in the figure 2.4. The current biasing is preferred because it requires less components and is independent of parasitic resistances between the biasing source and the sensor. In other words, there is more freedom in circuit layout design (there is a relaxation of the interface layout restrictions with PCB sensors, connector type, track size and track spacing).

The method of voltage biasing requires, for sensors with very different internal resistance characteristics, the need to re-size the biasing resistance if the ranges of variation are either very small or very large, as demonstrated by the equations 2.1a for the extreme cases,

$$V_{Out} = \left(\frac{R_{Sensor}}{R_{Sensor} + R_{Bias}} \right) \cdot V_{Bias} \tag{2.1a}$$

$$\begin{cases} V_{Out} \approx \left(\dfrac{R_{Sensor}}{R_{Sensor}} \right) \cdot V_{Bias} \approx V_{Bias} & , R_{Sensor} \ll R_{Bias} \\ V_{Out} \approx 0 \cdot V_{Bias} \approx 0 & , R_{Sensor} \gg R_{Bias} \end{cases} \tag{2.1b}$$

Even if the biasing voltage is controlled (voltage source in figure 2.4b), it will be necessary to use voltages values, either very low or very high, depending on the sensor resistance (internal resistance of the sensor), to obtain a range of values acceptable for

all sensors. This may involve excessive energy consumption in extreme cases. Another option is to keep the value of the voltage variable, but to introduce a biasing resistance for each sensor in which its sizing will be according to the characteristics of the sensor in question. However, this option implies N resistors for N sensors (using a analog multiplexer between the biasing circuit and the sensor), resulting in a larger implementation area and layout complexity.

Using the current biasing method shown in the figure 2.4a, it is possible to reduce the layout area, the complexity of designed and the energy consumption. The extreme cases where there are large differences between sensors, is now simpler to deal with, only a current DAC capable of generating the necessary interval of biasing values is essential.

$$V_{Out_{sensor}} = R_{sensor} \cdot I_{Bias} \tag{2.2}$$

For a given range of variation of the internal resistance value of a sensor, it is possible with increasing or decreasing, through the equation 2.2 (linear equation where I_{Bias} determines the scale of the range of values to be read), to increase or decrease the value range (if the range of values is small by increasing the biasing these values will be amplified by a factor of I_{Bias}, as shown in the figure 2.3).

2.4.1.2 Sensor Multiplexing

As previously described with the implementation of a variable biasing circuit, it is possible to excite several sensors through a single biasing circuit. For this, the integration of an analogue Multiplexer (MUX) (implemented with analog switches) is employed. Thus, allowing a reduction of layout area and low consumption, since the MUX consumes less than N biasing circuits. The number of sensors is now limited to the size of the MUX, allowing the implementation of a single sensor node capable of measuring all the sensors required for a particular application.

However, the use of MUX presents some disadvantages, being, the excitation and measurement of one sensor at a time, the intrusion of parasitic effects such as the internal resistance of the MUX switches, for high frequencies the maximum bandwidth in the signal can be reduced and also a noise source can be introduced.

2.4.2 Processor Unit

A node sensor needs to have a processing unit in order to implement communication and control protocols on all the re-configurable aspects of the system. It is necessary to implement smart controls, such as power management, and to implement, if necessary, some signal pre-processing, in order to reduce the amount of information to be shared.

In order to obtain processing capacity in a node sensor, two types of processing systems can be implemented, such as micro-controllers and FPGA. The implementation of micro-controllers provides a quicker and easier solution since it has the analog and digital

part of the whole system implemented and integrated in a single chip, thus reducing the number of components in the implementation. This solution does not require any development in the integration and analog and digital subsystems. Some micro-controllers are used for low power applications in which they exhibit low power consumption modes. The development of applications in this type of system, is all the basis of configuration of the registry of its peripherals (through programming).

The use of FPGA in the designed sensor node as the processing unit requires additional steps, being a more difficult solution and time consuming to implement. Unlike the micro-controllers in which the system is implemented, in FPGA it is necessary to implement the logic of the processor. FPGA thus allows greater re-configurability in the digital part, since the processing unit can now be customized according to the needs of the applications. It also implies the opportunity to develop hardware accelerators where a Central Processing Unit (CPU) intervention is not necessary. FPGA also has the advantage of being able to implement multiple controllers independent of each other.

Unfortunately, in applications where it is necessary to use sensors, the FPGA can only be used for the digital part of the system as it does not offer integrated analog blocks, these blocks will have to be added externally if necessary.

2.4.3 Power Management

Consumption and storage of energy is one of the main problems in autonomous sensor nodes. The amount of energy is limited and there are no continuous sources of energy for high power consumption, what implies that there must be strategies to lower consumption. This must be well managed according to the needs and requirements of the application and systems that minimize energy waste, such as the use/implementation of circuits optimized for low power applications.

The use of alternative energy sources should be used to supply energy storage tanks whenever possible using methods that allow the collection of energy from the environment to the system (e.g. solar energy collection), i.e. the use of renewable energy sources should be used to maximize the collection of energy from all possible sources of energy present in the environment in which the system is inserted (ex. solar energy together with energy from vibration through a piezo).

Because of the rapid use and storage/harvesting of energy, i.e. charging and discharging, of conventional energy storage media (batteries), they are no longer able to deal with this type of operation, their wear is very high, they have limited number of charging cycles. It is necessary to think about new strategies.

The battery has more limitations in the number of charges and discharges, which causes a faster wear if it is used in these conditions (regular charges and discharges of the battery whenever there is energy and storage space, even if it is small, whenever there is energy to store the charge starts). So, the use of super-capacitor is a solution. They present a larger number of (almost infinite) charging cycles. This implies that they can

handle the stress of multiple loads whenever there is energy to harvesting and space for store it.

However super-capacitors have a very high self-discharge, much higher than a battery. The ideal would be to use a combination of the two. Fast consumption (small charges and discharges) can be carried out on the super-capacitors (the capacitor is always being charged and discharged) and when prolonged consumption is required, which means longer charges, the batteries are used because they can have a higher energy stored than a capacitor. Thus, the stress of rapidly charging and discharging is mainly in the super-capacitor, that can handle this effect better.

It is also possible to use more than one super-capacitor. This allows a longer duration in the power supply for a certain task, resulting in a lower use of the energy of the batteries, consequently reducing the number of charges to it. It also implies that while one capacitor is supplying power, the others may be charging whenever it's possible the energy storage (there is still storage space and energy available to store). And it allows several tasks to occur at the same time within the limits of energy stored in each super-capacitor.

2.4.3.1 Super Capacitor Charging

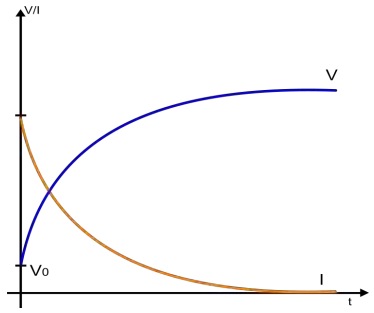
The use of super-capacitors is useful for storing small amounts of energy to be used quickly. For this purpose, it is necessary to use some method to charge the capacitor with energy, which is fast and efficient. Two ways to charge a capacitor were considered, through a voltage source or a current source.

Charging using a voltage source

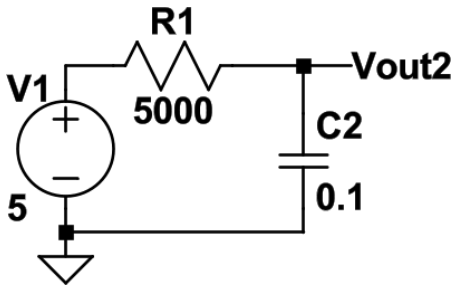
With the charging voltage source, it is necessary to introduce a resistor in series with the capacitor as shown in figure 2.5b. This is because, if the connection of the voltage source is made directly to the capacitor, there is no control over the maximum current occurring in the same (maximum current theoretically will be infinite [1]).

In reality there is always a resistance between the voltage source and the capacitor (internal resistance of the source and capacitor terminals and the resistance of the conductors between the two), but this can present very low values which is nonetheless problematic, because the current is of very high values due to the fact that the capacitor has a high capacity. Whit high values of current this can mean the destruction of the super-capacitor, the power supply and the connections between the two (e.g. connection lines of a PCB).

[1] The capacitor behaves as a short circuit at the beginning of charging. That is, at the terminals of the capacitor at time $t = 0$ (when charging starts) there is a discontinuity in the voltage at its terminals, going from zero Volts to the voltage of $V1$. Using the current equation in a capacitor, the derivative of the voltage at that instant causes an infinite current.



(a) Charging behavior. Blue line represents the voltage across the capacitor terminals and the orange line represents the current entering the capacitor.



(b) Charging circuit. Consists of a voltage source in series with a resistor and a capacitor.

Figure 2.5: Circuit and graphic behavior for voltage charge method.

The capacitor voltage and current equations of the circuit in figure 2.5b were taken from [31]. It is possible to verify both by the figure 2.5a and by the voltage equation 2.3 and current equations 2.4 [2] that the charging behavior of the capacitor is not linear (have exponential components),

$$V_{Capacitor} = V_1 - (V_1 - V_0) \cdot \exp\left(\frac{-t}{R \cdot C}\right) \tag{2.3}$$

$$I_{Capacitor} = \frac{V_1 - V_0}{R} \cdot \exp\left(\frac{-t}{R \cdot C}\right) \tag{2.4}$$

This means that as the capacitor is being charged, the charging process of transferring energy will lose force, i.e. the current decreases as the voltage increases. The voltage across the capacitor when the charging time approaches infinity, tends to a value equal to that of the power source.

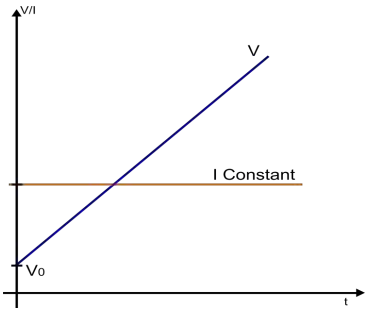
The charge time of the capacitor is given by equation 2.5 (from equation 2.3),

$$t = \ln\left(\frac{V_1 - V_0}{V_1 - V_{Capacitor}}\right) \cdot R \cdot C \tag{2.5}$$

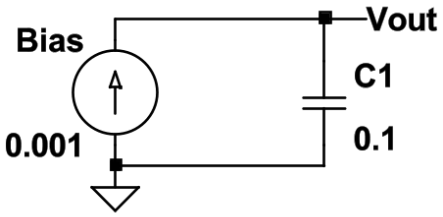
Charge using a current source

The current charging method involves applying a current source in parallel with the capacitor, as shown in the circuit present in figure 2.6b.

[2] These equations are drawn from the circuit analysis using the Kirchhoff law method and rearranging them in order to obtain a first-order differential equation with constant coefficients to be able to apply the mathematical theorems that allow us to calculate this type of equations



(a) Charging behavior. Blue line represents the voltage across the capacitor terminals and the orange line represents the current entering the capacitor.



(b) Charging circuit. Consists of a current source in parallel with a capacitor.

Figure 2.6: Circuit and graphic behavior for current charge method.

Using the equation that defines the current in a capacitor and imposing a constant current, we obtain an equation of the current where the derivative becomes a difference between two values of voltage in a certain time interval[3] as shown in equation 2.6,

$$I_{Capacitor} = C \cdot \frac{dV}{dt} \underset{I \rightarrow .Constant}{\Leftrightarrow} I_{Capacitor} = C \cdot \frac{\Delta V}{\Delta t} \tag{2.6}$$

Through the use of equation 2.6 and rearranging the variables and assuming that the time interval is between the initial instant $t_0 = 0$ up until t, the voltage equation 2.7 is obtained , where V_0 Is the value present in the capacitor at the initial time (start of charging),

$$I_{Capacitor} = C \cdot \frac{\Delta V}{\Delta t} \Leftrightarrow I_{Capacitor} = C \cdot \frac{V_0 - V}{t} \Leftrightarrow V = V_0 + \left(\frac{I_{Capacitor}}{C} \right) \cdot t \tag{2.7}$$

It is possible to verify in the figure 2.6a and in the equation 2.7 that the voltage in the capacitor (the charging of the capacitor) now has a linear behavior. The voltage equation now shows the shape of an equation of a line in which the slope of this is given by the relationship between the current and the capacity of the capacitor ($\frac{I_{Capacitor}}{C}$).

The time that the capacitor takes to be charged to the desired value is given by equation 2.8 (from equation 2.7),

$$I_{Capacitor} = C \cdot \frac{\delta V}{\delta t} \Leftrightarrow I_{Capacitor} = C \cdot \frac{V_0 - V}{t} \Leftrightarrow t = C \cdot \frac{V_0 - V}{I_{Capacitor}} \tag{2.8}$$

Theoretically the charging method by current causes, if the charging time is infinite, the voltage in the capacitor to be infinite. But in practice, because a current source is

[3] If the current $I_{Capacitor}$ is constant, the integral of the current in the capacitor has as an equation, that of a straight line,

$$I_{Capacitor} = C \cdot \frac{dV}{dt} \Leftrightarrow V = \int \frac{1}{C} \cdot I_{Capacitor}\, dt \Leftrightarrow V = \Delta t \cdot I_{Capacitor} \cdot \frac{1}{C} + V_0 \Leftrightarrow \Delta V = \frac{I_{Capacitor}}{C} \cdot \Delta t$$

normally constituted by active elements such as transistors, if the voltage in the capacitor causes voltages of vds (transistor Metal Oxide Semiconductor Field Effect Transistor (MOSFET), drain to source voltage) smaller than $vdsat$ (transistor MOSFET, drain to source saturation voltage), they are no longer able to generate current, thus limiting the voltage in the capacitor.

Comparison

It's demonstrated in figure 2.7 the simulations of the two charging types of circuits present in figures 2.6b and 2.5b. In the two types of circuits here demonstrated the size of the capacitance in them is the same and the size of the resistance is obtained in order to maintain the initial current equal for both circuits.

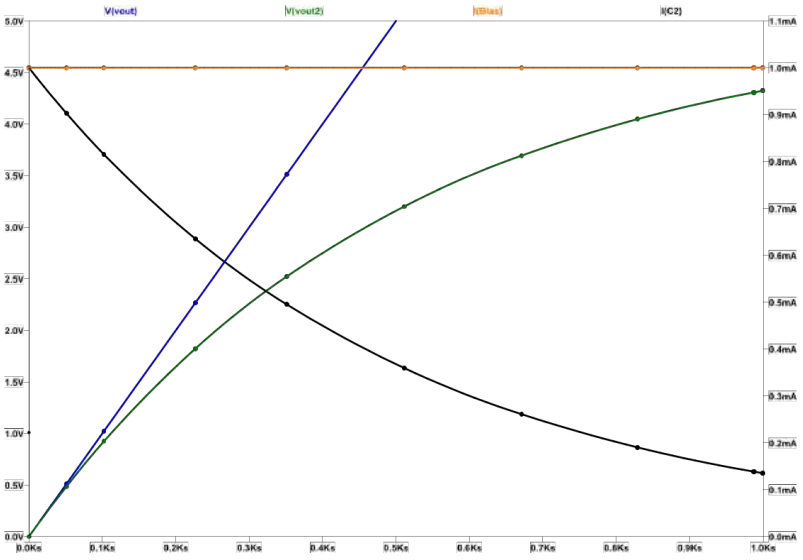


Figure 2.7: Electrical simulation of current and voltage charging schemes for the comparison of the behavior of the circuits in Figures 2.6b and 2.5b.

For a charging with the same characteristics as the initial current and maximum voltage on the capacitor, using the current method becomes faster, because the current with the passage of time does not decrease as the capacitor voltage increases, as expected in the charging voltage method, i.e. does not lose the charging force, remaining constant. For the same characteristics, the current charging method reaches the maximum voltage value when the voltage charging method is still only $63,2\%$ [4].

The use of constant current to charge the capacitor also has an impact on is control, as the equations are linear (equation 2.6) it's less expensive, in energy and time, to calculate in processing units (CPU, micro-controllers). Thus resulting in faster and more efficient

[4]The time constant $\tau = R \cdot C$ represents the time the capacitor takes to charge if the current remains constant. Replacing τ in the equation 2.3 and assuming that the initial value is zero, we obtain $V_{Capacitor} = V_1 \cdot 0,632$, [31].

controllers (fewer operations are required than to calculate the exponential equations 2.4 e 2.5).

2.4.3.2 Programming Techniques

The storage of energy may not be enough for a given application to keep all its functionality active, such as communication and sensor reading, among others. But it has to be at least enough to keep at least one at a time for a limited period of time. It is thus important to apply some scheduling of the various tasks present on a node sensor, that is, only one thing is done at a time. In a sensor node with many peripherals only those whose scheduled task is required to perform their functions are connected.

If the processing unit has features that allow the energy consumption to be reduced, they should be used whenever possible. Some functionalities are:

- the use of several types of operating modes, where it is possible to put the CPU and its peripherals when they are not being used in standby (the peripherals are powered off until needed),
- the use of interrupts to generate events that wake the CPU when something important happens (as some kind of stimulation at the terminals of a micro-controller).

In a controller program design, it must be implemented to operate at base events (interrupts, which can be triggered by internal or external peripherals), where the CPU and peripherals are only active when needed. If some kind of delay is needed this should be done with timers, as they allow the CPU to be off while waiting (only the timer is on), i.e. the CPU will not be blocked counting the delay time.

In programming micro-controllers, events are triggered by interrupts, but as some events may share multiple interrupts [5] these should be kept as simple as possible so as not to block the CPU for a given interrupt stimulus. It should be noted that the use of calculations in events should be used as little as possible, especially if they are complex calculations. These types of calculations can take a long time to be calculated causing some triggered interrupts to not be taken care of (the event is lost). It is good practice to keep the calculations and complex functions inside the main function of the program (main function, in C code), this allows to release the subroutine for new interrupts, because calculations or functions can be interrupted.

2.4.4 Software Tools for IoT node circuit design

With the tremendous demand for increasingly faster wireless communication, the level of specifications in terms of noise and bandwidth are increasingly difficult to achieve because it's necessary for greatest debit of bits, greater robustness between signal and

[5] Event is a subroutine that is called whenever an interrupt is triggered, the combination of multiple interrupts for a subroutine is specific to the architecture of the micro-controller in use

noise and higher bandwidth, thus originated receptors (Front End) increasingly difficult to implement.

One of the main blocks of a Front End, probably the one with the most important and difficult design constraints to achieve, is the LNA. The restrictions of a LNA are due primarily to noise introduced in this system. The noise of this block, as is the first in the signal path (directly coupled to the antenna), is what has the greatest impact on the final Front End noise. The gain of this block is also important because the noise of all the blocks after the LNA are divided by this gain, thereby reducing the effect that these have on the Front End. Another constraint is that the Zin of the LNA must have specific value in order to have an adapted antenna,

As these days the use of different carriers for different types of communication in one device requires that the equipment is capable of receiving signals over a wide bandwidth. The use of a wide band LNA allows the receiver to have only one LNA for all carriers thereby reducing the chip size and power of the same.

Due to the high cost of making the layout masks of the circuits, it's necessary to know before production the circuit performance, so if there is something wrong (specifications not achieved), it can be possible to correct the error in time before it's construction thus saving money and time. To be possible to predict the circuit operation is necessary to obtain the equations that model the circuit characteristics (gain, Zin, NF). Making the extraction of this equations by hand, is not trivial and can be time consuming. So, in order to obtain these complex equations, with some precision, we turn to CAD software to simplify this process. This types of software's can be simulators, like Cadence Virtuoso and Ngspice, among others.

The use of CAD software makes possible a complete and accurate (depending on the modulation of the instances) theoretical analysis of the circuit, reducing the time and cost of circuit design.

2.4.5 Conclusion

The design of a system, to be integrated in IoT, propose a serious growth in complexity, to maintain is operation across several applications without the need to redraw the system. It is necessary to increase the operating time in which the system is active and the ability to self-adapt its functionalities to various applications.

For the power management of a system a good strategy can be the use of supercapacitors as alternative energy storage units, using the constant current method for energy transference, due to the fact that this one is faster. However, to improve power consumption, methods such as using interrupts in software, allowing the CPU to be turned off when it is not needed, can improve the energy consumption, allowing to extend the time in which it is active. Using energy harvesting from the environment when possible can also extend the time of operation.

For the ability to self-adapt to several applications were different functionalities are

required, it's necessary the used of components like FPGA and microcontrollers that have the ability to be reconfigurable, like for example the used of an ADC form a microcontroller that requires the application to measuring signals from sensors. Also, to increase reconfigurability to measure several types of sensors the use of a MUX and current biasing are beneficial. Current biasing allows for the AFE to adapt is range, to the requirements of the sensors.

With the aim of integrating all the functionalities of the system into a single chip (passing the various modules to SoC or SiP) and taking into account the complexity that these functionalities present in integrated circuits. The use of CAD tools can speed up the design process.

Chapter 3

Power Management Unit

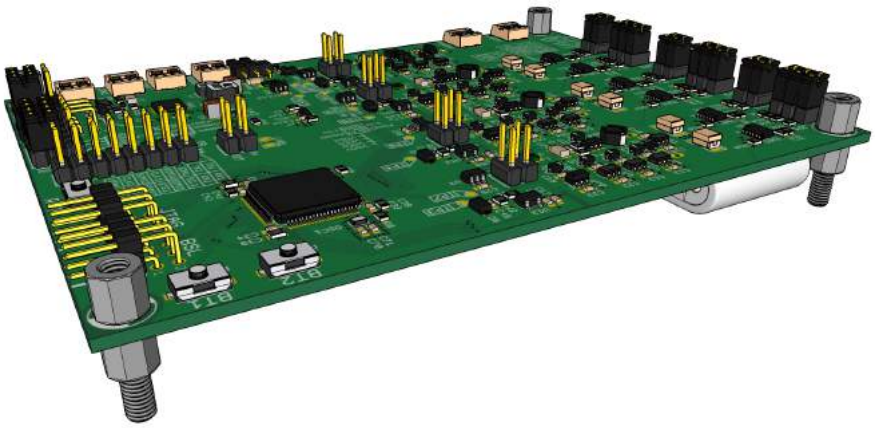


Figure 3.1: PMU Board (theoretical representation).

3.1 Introduction

Power distribution, low power consumption and energy storage are topics that nowadays require lots of attention due to the high demand of systems that require longer operating time intervals with limited energy. Many of these systems are being applied to the vast area of the IoT that require to be self-powered, to have long lasting energy storage, for applications that are applied in remote locations and require long periods without maintenance, and power management capability for improving energy consumption efficiency, by redirecting power to where is needed and power off anything that is not needed.

The ability to connect and disconnect parts of the system circuits (and also to choose its power source) allow to decrease unnecessary energy consumption, do with the fact that, these circuits are completely disconnected and do not have any current consumption, as would be, if they were in standby (always have a small amount of current being used). In order to be able to connect and disconnect sub circuits efficiently, same processing capability is necessary to implement power management algorithms.

Having the capacity to gather energy from its environment gives the system autonomous operation capability, meaning that the system has the ability to operate in remote locations for long periods of time. Increasing the amount of energy sources from which the system can collect energy, increasing its operational time interval. A lot of this energy sources are not constant and have periods of time where they don't give enough energy to maintain the system operation, so the use of energy storage devices is necessary. The more storage devices the system has, the more energy it can collect, taking the maximum advantage of the periods of time in which the power sources have the energy to be collected.

The normal way to implement storage elements is using batteries, but a problem is presented using this strategist. The batteries have few charging and discharge cycles, meaning that, when they are used in energy harvester, they will be in a constant process of charging and discharging (energy source is not constant) this translates in a faster battery degradation. A possible solution is to implement the energy storage elements with the use of supercapacitors, these elements have a much higher number of charging and discharging cycles. Unfortunately, supercapacitors have lower energy storage capabilities, in comparison with batteries, so implementing an array of capacitors is necessary to increase storage limits. If we also maintain each of the elements of the array independent of each other, we can charge some of them while using the others to supply energy when and where is needed.

In this chapter it's presented the design and implementation of a system, for evaluating the use of a supercapacitors array, energy harvester, power distribution and overall control (power management control algorithms). A PCB prototype is developed to test all these characteristics in combination with which other in a real environment. The structure of this chapter consists of five sections. The first section is a brief introduction to the topic, the second section describes the system structure and its main blocks, the third section demonstrates the implementation of the system and the prototype, the fourth section presents the test results obtained with the prototype and finally the fifth section contains a small conclusion of the work done in this chapter.

3.2 System Structure

In a typical system the power distribution tends to be fixed, everything is always connected to the power rails and normally only exists one power source. In order for this system to have an efficient power management capability, it requires the ability to sense

its parameters, to a controller and understand them. Which means that the system must have additional and sufficient specific hardware to manage power consumption, distribution, harvesting, storing and system efficiency.

The design starts by defining the structure of the system capable of having multiple energy storage units, multiple output power rails, that can be activated or deactivated in real time and a configurable power distribution path (power MUX) between energy harvesting, energy storage and the output. This path is also controlled in real time, meaning that a processor unit is required.

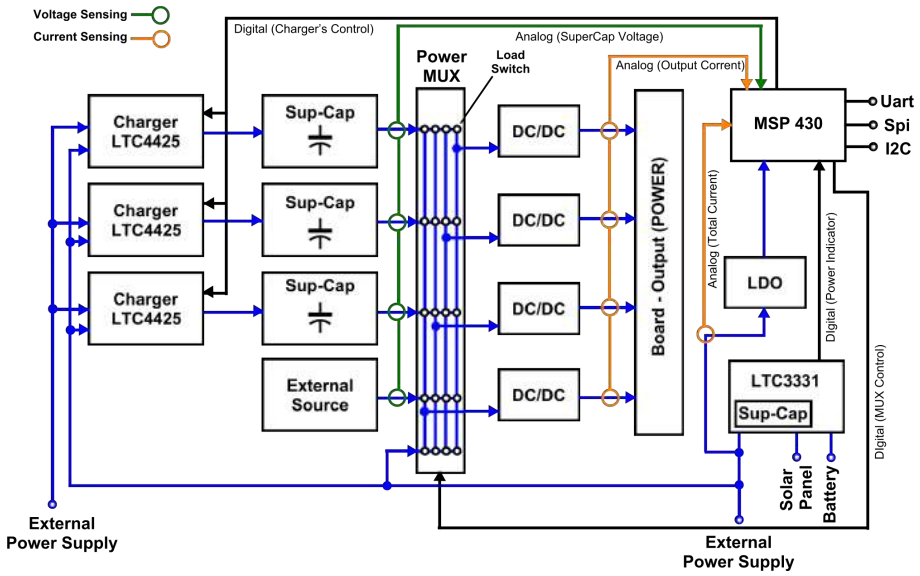


Figure 3.2: PMU board block diagram (representation for power, digital and analog sensing signals).

The system structure main blocks consist of Energy Harvesting, Power Multiplexer, Super-capacitor, super-capacitor Charger, DC/DC Voltage Regulator and a controller. The structure of the system is presented in Figure 3.2.

The energy harvester block is responsible for collecting all the energy available from various energy sources, such as a solar panel. The management of internal power in this block is left to the LTC3331 chip from Linear Technology company [33]. This block is what provides all the energy that will be used within the total system.

Supercapacitors are the energy storage elements of this system. The energy supplied by the energy harvester is stored in these through the super-capacitor charger block implemented using the chip LTC4425 from Linear Technology [30]. The use of the charger blocks in the energy storage of the supercapacitors, allows to control the charging of the same ones efficiently. The charger works basically as a constant current source, thus allowing a linear behavior, easily predictable and a faster charging, as described in the Chapter 2 (Section 2.4.3.1).

Because the harvester has a reduced current limit, the possibility of storing energy in the super-capacitor through an external source with a higher current limit would

allow it to be charged more quickly, this is especially useful when the super-capacitor is completely discharged, which originates long charging periods.

In order to be able to transfer energy between the supercapacitors and the outputs it is necessary to implement a block capable of receiving energy from several sources and directing them to various output. Using a MUX capable of dealing with high power levels we get a fully configurable block in which you can choose which input connects to an output, allowing each output to receive power from one source or several and the reverse is also possible.

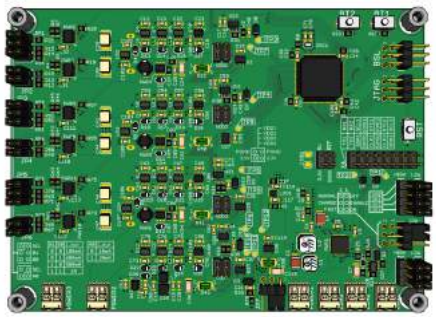
Using supercapacitors to supply power directly into the output presents a problem because the output voltage needs to be stable (always having the same value), this does not happen in the voltage to the terminals of the super-capacitor, which decreases depending on the energy that the super-capacitor provides (supplying power to the capacitor is discharging). In order to counteract this effect, it is necessary to add a DC/DC converter that allows the voltage to be maintained stable in the output, regardless of the input voltage. So, the DC/DC block functions as a buffer that stabilizes the voltage between the super-capacitor and whatever circuits are connected to the output.

The final block is the controller. This one allows the system to be autonomous, and to have the possibility of employing intelligent control algorithms for the control of energy distribution and storage. To implement this block, it is necessary to use processing units for signal control (enable signal of the power switches, enable signal of the charger, etc.) and analogue measuring units, where the measured analog signals represent the state of the system (voltage in the supercapacitors, output current and charger output current). The best option to implement the controller block is to use a micro-controller with the ability to measure analog signals, thus being a compact and easy implementation solution. The controller will be implemented using a low power micro-controller chip called MSP430FR5994 of the MSP430 family from Texas Instruments [40]. The controller will also allow for the integration of the PMU in the complete system, meaning it can interact with higher level systems throw serial communication.

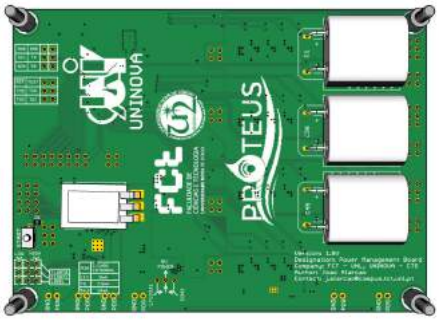
3.3 System Implementations

The implementation of the system is done in two parts, the first part is hardware and the second part is software (control algorithm). The first part, within the scope of this document, is the most relevant for the study of the improvement of power management in a given generic system. Emphasis is given to the circuit design of each block discussed in section 3.2. The second part being not only to demonstrate that the circuit allows to implement an algorithm, but serves to control the control signals in each block for testing purposes.

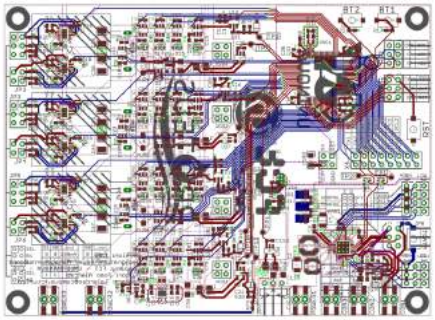
As the system to be implemented only focuses on the power management area, by itself, is not a complete system to be used in a given application in which other functionality outside the energy management area are needed. Which means that this system must



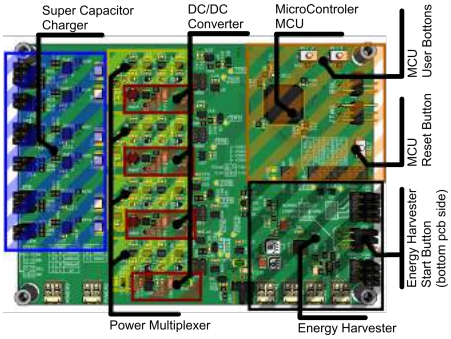
(a) Top view.



(b) Bottom view.



(c) PCB layout, 4 layers.



(d) Organization and position of diagram main blocks (Figure 3.2) main blocks.

Figure 3.3: Theoretical implementation, expected final result of the complete system (PMU Board - PCB Version V1).

be interconnected with other systems capable of performing those additional functions, this system is only concerned with dealing with power. This means that it will also be necessary for this system to have an interface which enables the ability to communicate with other systems, so that the system can be integrated into a generic application.

The expected final result of the physical implementation of the system (prototype) is presented in Figure 3.3. The physical implementation of the system involves the design of a PCB that contains the implementation of the circuits of the main blocks shown in the Figure 3.2. The physical position of the blocks in the PCB can be seen in Figure 3.3d.

3.3.1 User Interface Description

There are two types of interface, the hardware and software interfaces. The software interface is responsible for the communication between systems, from which it sends the measured values, and instructions, commands to activate certain system functionality (such as switching on and off the outputs) and is defined through communication protocols. The hardware interface covers the configurations that each block requires, which are not automatically controlled, and the energy inputs and outputs.

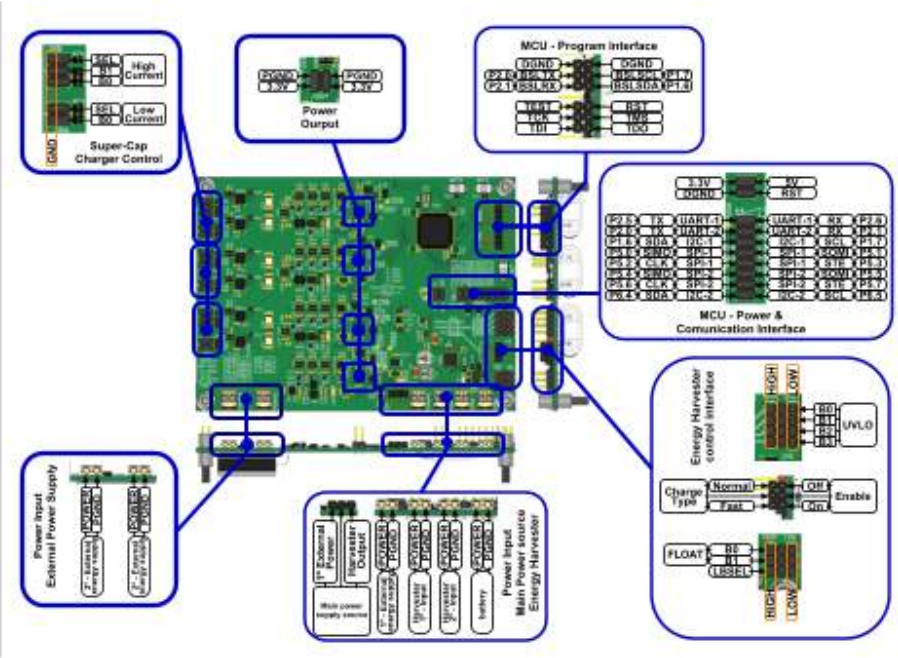


Figure 3.4: PMU board pin-out description and configuration.

3.3.1.1 Pinout Description

Each circuit of each block that has been implemented requires that the user imposes certain configuration signals to obtain different performances from the blocks, for better fitting the power constraints. To do so, the user needs to have access to such signals. The chosen way to control these signals (configuration) is the use of strips pins connector with shunts.

The Figure 3.4 shows the entire physical interface available to the user. It is possible to see the configuration connectors ("Super-Cap Charger Control" box and "Energy Harvester Control Interface" box), the connectors for communication interface ("MCU - Program Interface" box and "MCU - Power & Communication Interface" box) and the connectors for input and output power ("Power Output" box, "Power Input External Power Supply" box and "Power Input Main Power Source Energy Harvester" box).

Super-Capacitor Charger

In the blue box designated by the name "Super-Cap Charger Control", of the Figure 3.4, these connectors serve the purpose of configuring the two current values of the charger block whose function is the charging of the super-capacitor (high Current and low current). In low current charging the connector B0 pin, if connected to GND will set the charger to supply $20mA$ current, otherwise it will be configured to $10mA$. In high Current charging, the connections of the pins B0 and B1 will allow to configure the charging currents for the levels expressed in Table 3.1. The configuration is done by

connecting the pins to GND or to leave it disconnected [1].

Table 3.1: High Current Charger Configuration Bits

B1	B0	Charge Current
0	0	100mA
1	0	500mA
0	1	600mA
1	1	1000mA

In case the power source is not able to supply the amount of current that the charger is configured to, the actual value will be dictated by the power source if its maximum current is inferior to the values programmed. If this situation occur, were the poser source it's not sufficient, will result in a breakdown of the power source used.

Energy Harvester

In order to configure the energy harvester block the connectors in the blue box called "Energy Harvester control interface" are used. These are responsible for defining the type of charging of the battery (charging type) that can be fast or slow, to turn on or off the harvester (enable) thus saving the battery when the device is not in use, to set limits in which the battery is switched on or off (FLOAT and LBSEL) and to set the input value range where the harvester will operate to collect energy (UVLO)[2]. The values for the FLOAT, LBSEL and UVLO are represented in the Tables 3.3 and 3.2 [3] [33].

Table 3.2: FLOAT Configuration Bits

LBSEL	FLOAT1	FLOAT0	FLOAT	Conect	Disconect
0	0	0	3.45V	2.35V	2.04V
0	0	1	4.0V	3.03V	2.7V
0	1	0	4.1V	3.03V	2.7V
0	1	1	4.2V	3.03V	2.7V
1	0	0	3.45V	2.85V	2.51V
1	0	1	4.0V	3.53V	3.20V
1	1	0	4.1V	3.53V	3.20V
1	1	1	4.2V	3.53V	3.20V

[1] In the table 3.1 one corresponds connecting the pin to GND, the zero corresponding leaving it disconnected.

[2] The range of values should be centered at the point of greatest power supply of the generator. This implies studying the V/I of the generator [18, 21] to choose the best configuration.

[3] In the Table 3.3 and 3.2 one corresponds connecting the pin to HIGH pins, the zero corresponds connecting to LOW pins.

Table 3.3: UVLO Configuration Bits

UV3	UV2	UV1	UV0	Rising	Falling
0	0	0	0	4V	3V
0	0	0	1	5V	4V
0	0	1	0	6V	5V
0	0	1	1	7V	6V
0	1	0	0	8V	7V
0	1	0	1	8V	5V
0	1	1	0	10V	9V
0	1	1	1	10V	5V
1	0	0	0	12V	11V
1	0	0	1	12V	5V
1	0	1	0	14V	13V
1	0	1	1	14V	5V
1	1	0	0	16V	15V
1	1	0	1	16V	5V
1	1	1	0	18V	17V
1	1	1	1	18V	5V

Power Outputs

There are four "Power Output" blue boxes, all of them have the same pin-out, two pins for supplying $3.3V$ and tow pins for GND. The first three outputs (output 1, 2 and 3 counting from the top of the PCB) in Figure 3.4, have a maximum current of $100mA$, this value is software limited, the last power output has a higher current capability, also software limited to $800mA$, in Section 3.3.2 this subject will be explained in more detail. Any load that requires the output to supply higher current, will result in the permanent shutdown of that output, meaning that to activate the output again, a new request needs to be done to the controller.

Power Inputs

There are six power inputs and they are represented in Figure 3.4, highlighted with a blue box with the names "Power Input External power supply" and "Power input main power source energy harvester".

The harvester has three power inputs, one for the battery and the other for harvesting energy from solar panel or piezoelectric transducers (their names are "Harvester 1st input" and "Harvester 2nd input"). The two harvester inputs have a direct connection to the pins of the harvester chip (LTC3331), this can be verified in Figure 3.6 from Section 3.3.2

and A.1 from Attachment A, where the pins in question are AC1 and AC2.

The "1º external energy supply" pins are to be used as second energy input to supply more power (higher current levels) to the board if the user decides not to use the harvester. In the power pin is required that the power supply has $5V$ and a minimum of $60mA$ drive capability [4].

The "main power supply source" pins are configuration pins, by shorting this pin from the side to the middle, it's possible to choose to connect the harvester to supply energy to the board or to use the power supply input named "1st external energy supply". The rest of the power input is used for the charger (named "3º external power supply"), to charge the supercapacitors with higher currents and used as another external energy source to supply power directly to the outputs (named "2º external power supply").

The "3rd external power supply" is required to have a value of $5V$ to charge the capacitors. A lower voltage can be used, but the charger will only be able to charge the super-capacitor to that level of voltage (modifications are required to be done in the autonomous algorithm to use lower voltages).

The requirements for the second external power supply are the same as for the supercapacitors, it requires a voltage value higher than the minimum limit for the DC/DC operation which is $2.16V$[5].

Main Controller

The controller requires communication interfaces to pass data and commands with other systems and for that purpose, we can use the pins in blue box named "MCU - Power & Communication Interface". They allow three types of communication, Universal Asynchronous Receiver/Transmitter (UART), Inter-Integrated Circuit (I2C) and Serial Peripheral Interface (SPI), this pin can be chosen by the user[6].

In order to be able to be able to modify the code and to reload it into the controller (micro-controller MSP430 chip) he can use the pins in the blue box named "MCU - Program interface". The pins TEST, RST is for programming the chip using the Texas Instruments programmer (launch pads), this pin can also be used in conjunction with the pins TCR, TDI2, TMS and TDO for Joint Test Action Group (JTAG) interface. The rest of the pins in the blue box are duplicated.

3.3.1.2 software description and restrition

In order for the user to have control and to obtain the state of the system (measured signals and switch status) it requires a communication interface with the main controller.

[4]This value is limited by software to protect the harvester, by modifying the controller code this value can be increased using the full capacity of the "1º external power supply".

[5]This value is limited by the software to ensure that there is sufficient voltage for the DC/DC converter to operate properly. Also, the minimum current depends on the type of the converter and its output current.

[6]The choice of the type of communication requires modification to the code in the controller, for the purpose of this test only UART communication was implemented.

The communication interface is implemented using UART communication protocol. It is necessary to create a communication protocol between the Power Management system and any other that is connected to the interface and that wants to communicate, so that the data to be transmitted are interpreted correctly, that is, both systems interpret the data in the same way.

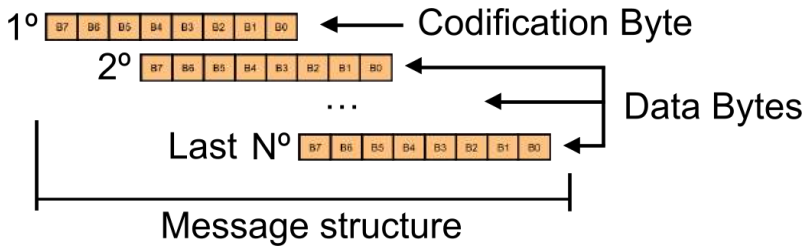


Figure 3.5: UART communication protocol. Message structure.

The protocol consists of defining the structure of the messages containing the data to be sent through the UART interface. The UART communication works by sending one byte at a time and there is a need to send more than one byte, each group of bytes sent corresponds to a message in which its data has a certain interpretation. To differentiate each message, it's structure begins with a byte of codification that allows to differentiate the interpretation that is given to the following bytes, it also allows to know how many bytes for each type of message will be transmitted or received. The Figure 3.5 demonstrates the concept of message encoding.

Table 3.4: Communication codes for UART interface send by the PMU Board.

OpCode	**Descripton**	**Bytes**	**Parameters**
11	Sending data from all the sensors	21	1º- OpCode; 2º to 21º - Signal values
50	Sending data of the system status	5	1º- OpCode; 2º to 5º - Values of the switches and of the supercapacitor chargers

In the Tables 3.5 and 3.4 it is possible to check the types of messages that the system receives and sends, respectively. Most of the messages that the system receives from the Table 3.5 are control data and can be divided into five main groups:

- The first group consists of a message with the functionality of asking the system to reset.

- The second group consists of the messages that allow the control of the sending of measured data and the state of the system (opcode 3, 4 and 50).

Table 3.5: Communication codes for UART interface received by the PMU Board.

OpCode	Descripton	Bytes	Parameters
0	Full system reset	1	1º- OpCode;
3	Continuous send data from all sensors at the same time	1	1º- OpCode;
4	Stop sending data from sensors	1	1º- OpCode;
50	Request data from: type of charge, output source and harvester signals	1	1º- OpCode;
174	Stop autonomous mode (power management)	1	1º- OpCode;
175	Start autonomous mode (power management)	1	1º- OpCode;
176	Power on output (power management)	2	1º- OpCode; 2º- Output
177	Power off output (power management)	2	1º- OpCode; 2º- Output
200	Connect a charger without disconnecting the other (start charging, high or low current, to full)	2	1º- opcode ; 2º- Charging and super-cap
201	Connect a charger without disconnecting the other (start charging, high or low current, to value then disconnect all charger)	4	1º- opcode ; 2º- Charging and super-cap ; 3º- Value; 4º- Value
202	Disconnect a charging without disconnecting the other (stop charging, high or low current)	2	1º- opcode ; 2º- Charging and super-cap
203	Disconnect a charger control (stop charging and stop the control)	2	1º- opcode ; 2º- Super-cap
204	Connect a source to Output,and not disconnect the others	2	1º- opcode ; 2º- Source and output
205	Disconnect a source to Output,and not disconnect the others	2	1º- opcode ; 2º- Source and output

- The third message group refers to the control of the automatic power management mode (opcode 174, 175, 176 and 177). This mode is responsible for controlling the entire system (charging, switching supercapacitors, activate output) automatically.
- The fourth group of messages consists of messages that allow the control of the state of the super-capacitor chargers (opcode 200, 201, 202 and 203).
- The last group refers to the control of outputs (opcode 204 and 205).

All the messages that the system sends, Table 3.4, have the objective to send the measured data and the state of the system (as an example of data about the state of the system we have the condition of the chargers and the state of the power MUX, that is, of the switches that which the MUX is constituted).

A more detailed explanation on the codification of the messages is provided in the Appendix A.

3.3.2 Hardware Designed

The hardware design is implemented by using proprietary chips, to allow for a rapid development of the prototype. The implementation follows the design of Figure 3.2, in which each block is implemented through the circuits present in the Figures 3.6,3.8, 3.10, 3.11 and 3.14, this image presents only the circuits simplified and necessary for its operation without interoperability between blocks. A more detailed circuit of all the PCB implementation, designed and connections between blocks is presented in Figures A.1, A.2, A.3, A.4, A.5, A.6 and A.7 from Appendix A.

The designed in the Figure 3.2 requires specialized chips for the implementation of its blocks, and requires a block capable of collecting energy that will be implemented through the chip LTC3331, a block capable of storing energy, built on supercapacitors and specialized charger to charge super-capacitor, one block with the ability to redirect energy to where it is needed, the implementation is done using load switches that result in a five inputs to four output power MUX.

In order to design the system, some considerations need be taken into account[7]. The system requires at least one input for energy harvesting, it needs to be sufficient to power the charger of at least one super-capacitor, so the super capacitor charger should allow for current charging configuration, for fast charging the super-capacitor the charger block also needs to have an external power supply.

It also should have the capacity to power the outputs through the energy in the super-capacitor, so the capacitance should be enough to drive an output with the maximum current of $800mA$ and it requires a power MUX capable of driving these types of currents, it also needs to be fully programmable for allowing the connection of multiple sources

[7] One of the main reasons for the choice made about the chips is its packaging (footprint in PCB layout). The type of packaging needs to be able to be soldered by hand.

to multiple outputs. All of these blocks have analog and digital signals that require to be read and controlled, so the main controller needs to have the necessary pins and peripheral to connect all these signals, the controller should also have low power features for power saving purposes.

Energy Harvesting

The harvester block is implemented using the chip LTC3331 from linear technology, that is a "Nanopower Buck-Boost DC/DC with Energy Harvesting and Battery Charger" [33]. It has the ability to retrieve energy from two different energy harvesting power supply, like solar panel or the piezoelectric transducer. The internal management of the LTC3331 allows a continuous supply of energy between the sources and the battery for when there is no energy to collect. It has also the possibility to configure a hysteresis window to maximize the power of the solar panel and also allow for charging the battery when there is available energy (from the solar panel) but the output of the harvester does not require it. Figure 3.6 shows the necessary circuit for the LTC3331 to operate.

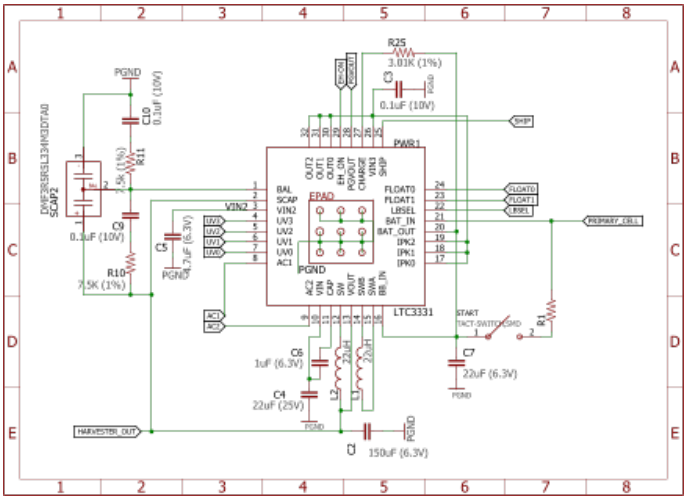


Figure 3.6: Simplified circuit of energy harvester block, implemented with LTC3331, supercapacitor, additional passive components and a capacitor to simulate the discharge of a battery.

The energy harvester has the ability to harvest $50mA$ at each power input (pins AC1 and AC2) from a wide range of voltages (up to $19V$). It's possible to achieve the maximum current supplied by the harvester of $100mA$, this of course requires that the harvester power source can produce that amount of energy. It can supply a higher current, to a maximum rated $250mA$, but at the cost of depleting the energy available in the battery, because the maximum harvested energy that the harvester can acquire is not enough to supply this amount of current for the output. This level is expressed in the chip datasheet [33].

In Figure 3.7 we can observe the behavior of the LTC3331 chip independent of the rest of the system. The chip uses the energy available in the input to power the output, but when this energy goes away the battery is responsible for supplying energy, even in the consumption of $50mA$ in the output. If the input does not have enough power the chip will fetch power from the battery, if it goes down quickly, there will be a failure in the voltage levels of the output, for high currents this can be even more problematic because the harvester only supplies at maximum $100mA$. If we have a higher current it's the battery that will support that supply of energy. Ideally the expected operation is, to use the harvester supply power, but this one depends quite of the type of energy source. A good choice needs to be done to ensure that energy supply can accommodate the system consumption.

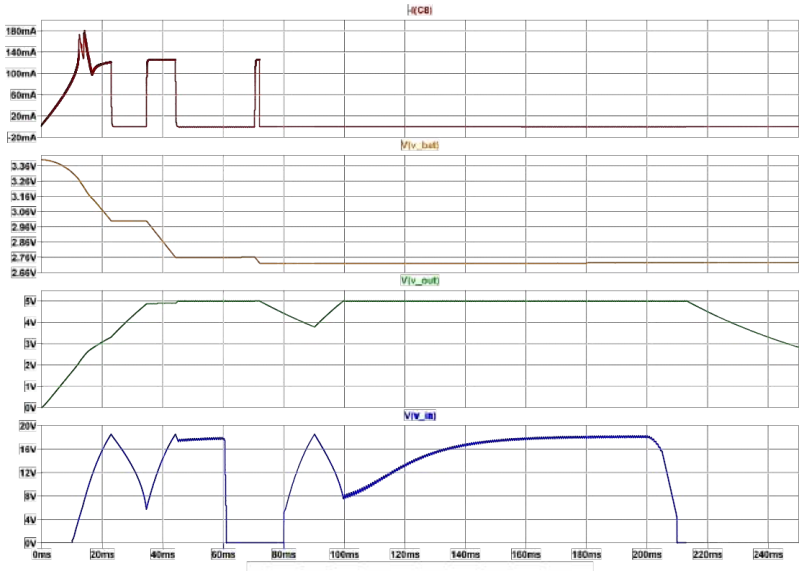


Figure 3.7: Simulation of the chip LTC3331, the circuit to simulate is present in Figure A.18.

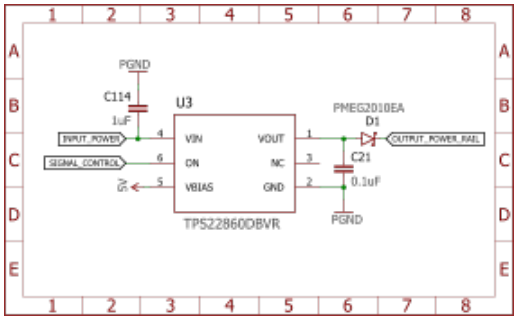
Power Multiplexer

The power MUX is responsible for delivering power from point A to point B, is the one that connects the super-capacitor to the output. It has five inputs and four outputs, it will be consisted of power switches. Since one of the outputs has higher current capability than the others, some of the switches will have more tolerances to higher levels of currents.

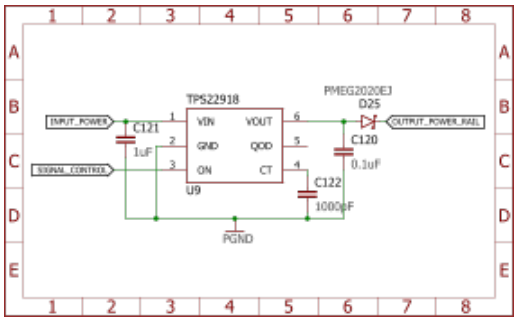
The configuration of the MUX switches is shown in Figure 3.8c. The highlighted switch are the ones that are conducting higher levels of currents, with this structure is necessary for two types of switches. For high currents is used the TPS22918 chip [42], from Texas Instruments and for lower currents is used the TPS22860 chip [41], also from Texas Instruments. The circuits to use both types of load switches are present in the Figures 3.8a and 3.8b.

The purpose of the choice of this two chip was its package size, its ability to operate at lower voltages (down to $1.8V$ minimum), it also has a very low resistance [8] and the fact that it does not have the quick output discharge functionality or that allows the possibility to not use it [9] allowing the connection of multiple sources to a node, since no one is pulling the voltage to zero.

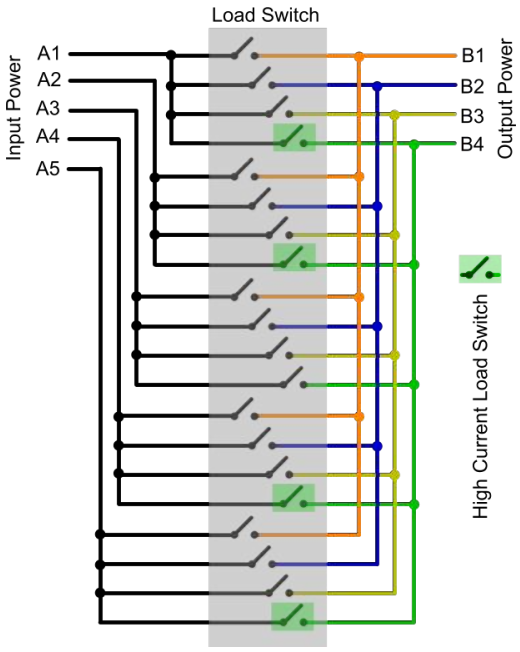
Unfortunately, the switches do not have protection against inverse current so it is necessary to integrate a Schottky diode, in series with the switch output to prevent current from flowing backwards. Two sources can supply power to the same output, but whit the use of a diode they cannot supply between them.



(a) Simplified circuits for low current power switches (TPS22860).



(b) Simplified circuits for high current power switches (TPS22918).



(c) Power MUX configuration, five inputs to four outputs.

Figure 3.8: Power MUX configuration and simplified circuits for the power MUX switches.

As we want no interruption in the power supply when we are switching between two power sources and the commutation in practice is not instantaneous, it is necessary to implement a strategy "make before break", meaning the two switches to be used to make the exchange will be at some point in time in the same ON state together for a brief period of time. This ensures that when the old switch is turned off the new one has already had time to make is transition, allowing for a non-interrupt supply of energy. The simulation

[8] On resistance is the resistance that the switch has when it is allowed to pass through it, meaning when it is in the on state.

[9] Quick output discharge, is the ability that the switches have to disconnect and power down all circuits connected to it, meaning when he is in its open state (off), still has some energy in the output node of the switch, so there will be a path to ground to discharge the energy, powering the circuit faster (the voltage drops to zero.

of the TPS22918 chip, Figure 3.9, done with the circuit in Figure A.19 from Appendix A, demonstrates the effect of turning the switch one, it is this value of time that must be taken into account in the controller wen doing switching in power in mid operation.

The high current chip, TPS22918 allows to set the rise time through a capacitor on the pin designated CT, this capacitor was chosen with a value of $1nF$, it allows for a fast enough transition as demonstrated in the datasheet [10][42]. The choice of the value of this capacitor also determines the inrush current[11], allowing it to be within acceptable values. With these values of the high current switch and with the equations of the datasheet [42] we obtain the following values of inrush current, expressed by the calculations 3.1,

$$\begin{aligned} I_{InRush} &= 22uF \times \frac{4V}{2540us} \\ I_{InRush} &= 0.034647 = 34.647mA \end{aligned} \tag{3.1}$$

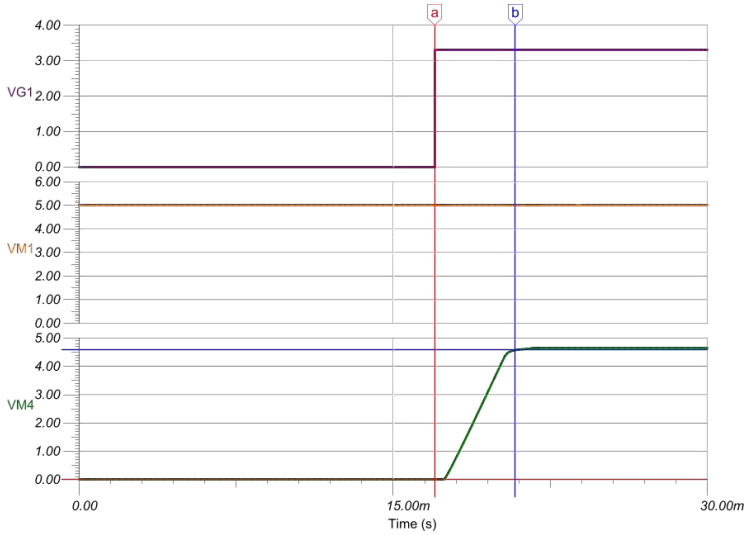


Figure 3.9: Transition time simulation for the high current power switch, from circuit in Figure A.19.

Using the datasheet for the switches and the simulation, a value of $20ms$ was used in the code to ensure that, with any possible delays in the control signal and in other places, like unforeseen delay caused by the board layout, that are not counted for, there is no interruption in the supply of energy. The expected transition time, for the high current switch-over, gather from the datasheat [42] is $2,540ms$ but this only takes into account 10% to 90% of the output voltage, so using the simulation in Figure 3.9 for the full transition time it's expected a stable output after four to five milliseconds as passed, from the moment the control signal is turned on.

[10]This value allows the two switches to have similar transition times, thus making code implementation simpler.

[11]Is the maximum, instantaneous input current drawn by an electrical device when first turned on.

Super Capacitor Charger

Energy needs to be stored in the super-capacitor from the harvester, since this energy is limited, it is necessary to have control of the charging process, for such purpose it's used the charger LTC4425, from Linear Technology [30]. This charger has the ability to control the current, allowing to have a constant rate of charge being delivered to the super capacitor, meaning the current can be maintained constant during the all charging process. The level of current can also be controllable.

The charger has two charging methods, one that allows you to use two levels of currents, for when the capacitor is discharged (low voltage) and for when it is close to being fully charged, this method has a profile that can be seen in the datasheet [30], that the lowest current is one tenth of the highest current. Another method, is simply using the same current value for the entire energy transfer process.

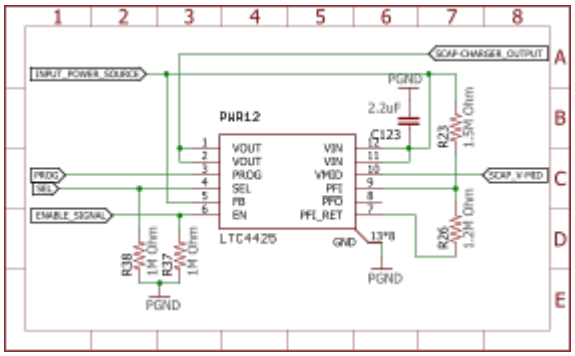


Figure 3.10: Simplified circuit for super-capacitor charger block, implemented with LTC4425 and additional passive components.

In Figure 3.10, the circuit of the LTC4425 chip is demonstrated. The programming of the current is made through the PROG pin with a resistance connected to ground, where its value is given by equation 3.2,

$$R_{PROG} = 1000 \times \frac{1}{I_{CHRG}} \tag{3.2}$$

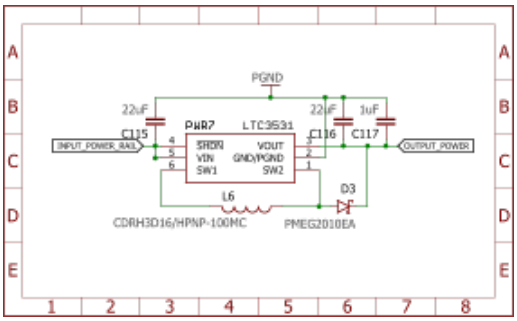
In order to be able to choose between the two methods, the FB pin of the chip needs to be connected to the input voltage (INPUT_POWER_SOURCE) to select the two-level current profile, or connected to ground to select the constant current method. In Figure A.4, A.5 and A.4 from Attachment A it's possible to see that the charger in the PROG pin has a multiple resistor for manual configure the correct level. The configuration of the value of the current charger is defined in Section 3.3.1.1.

DC/DC Voltage Regulator

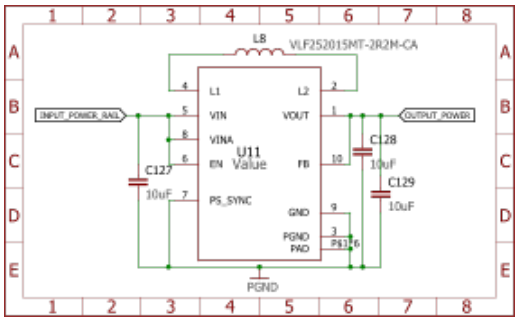
In order to be able to use a wide range of the super-capacitor voltage, it's necessary to have a DC/DC converter with buck boost architecture to stabilize the output voltage level

using a wide range of input voltage. The converter will allow the use of input voltages below the output voltage, thus extending the operating time using the maximum possible power of the super-capacitor. The buck boost architecture means that when the voltage is higher than the output, converting simple reduces the voltage, but when it passes the output, the converter increases the voltage through the current-to-voltage conversion.

As the system is designed to have an output with a high current, the converter to be employed in this output must be capable of supplying this current. So, it is chosen for high current output the chip TPS63001 [43], from Texas Instruments and for the low-voltage output the LTC3531 chip [29] from Linear Technology. The Figures 3.11 presents the necessary circuit for the convert to operate.



(a) Low current DC/DC converter circuit, implemented with LTC3531.



(b) High current DC/DC converter circuit, implemented with TPS63001.

Figure 3.11: Simplified circuits for high and low current DC/DC converters.

The current consumption from the converter is not linear, meaning that with voltages lower than the output voltage the beaver of the super-capacitor discharge is no longer linear. Both chargers increase the current in order to be able to maintain the output voltage for a given output current, this can be seen in Figure 3.13, for the circuit in Figure A.24 from Attachment A and for the Figure 3.13, for the circuit in Figure A.22 from Attachment A. Both converters have a limit of $1.8V$ of voltage at the input, any voltage below this value results in the power off of the converter. This means that the voltage range in which the super capacitor will operate is between $5V$ to $1.8V$.

Is possible to see in the Figures A.23 and A.25 from the Attachment A, that the converters cannot sustain the output for all output currents with input voltage below the output voltage. The output voltage starts to decay the moment that the input voltage drops below the expected output voltage. So, in order to guarantee the stability of the output voltage, a software limit value was impose, and any current higher than that value will result in output shutdown.

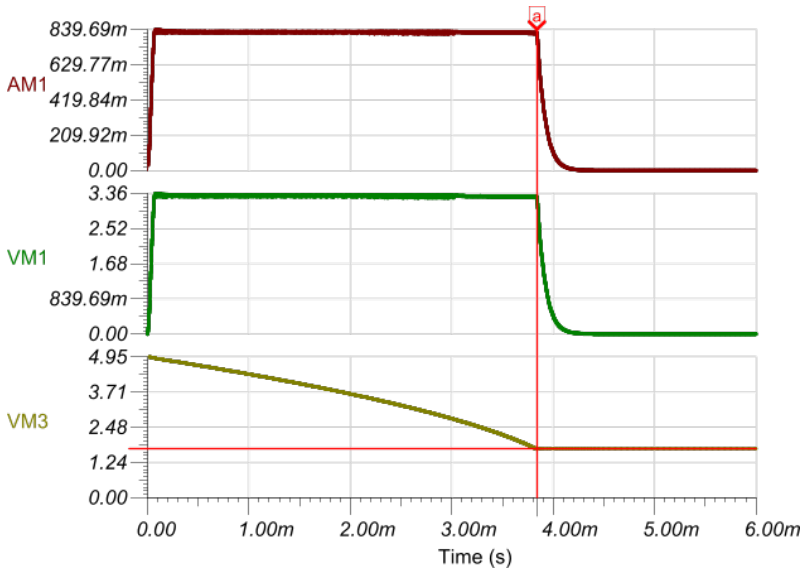


Figure 3.12: Simulation of TPS63001 circuit, presented in Figure A.22. For input source uses a capacitor with $1mF$ and initial voltage of $5V$. The output is $3,3V$ and the load is model whit a resistance of $4Ohms$, resulting in a current of approximately $800mA$.

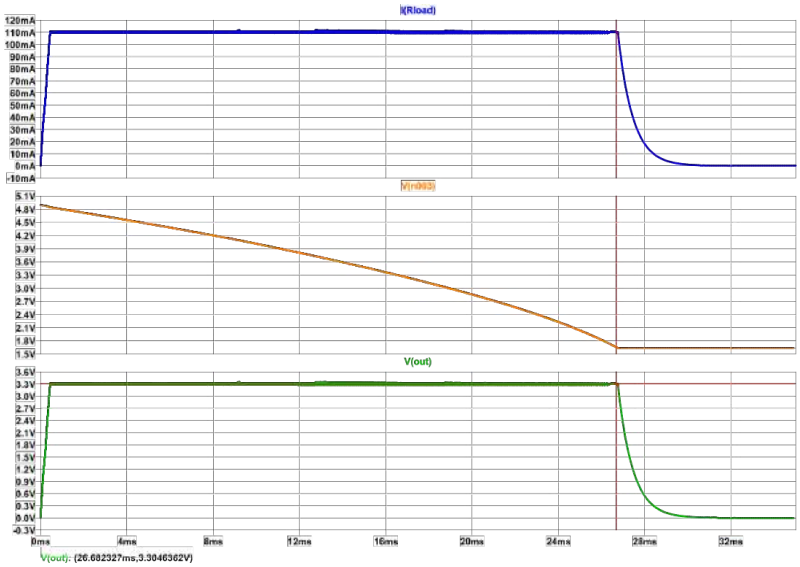


Figure 3.13: Simulation of LTC3531 circuit, presented in Figure A.24. For input source uses a capacitor with $1mF$ and initial voltage of $5V$. The output is $3,3V$ and the load is model whit a resistance of $30Ohms$, resulting in a current of approximately $100mA$.

Low Power Micro-controller

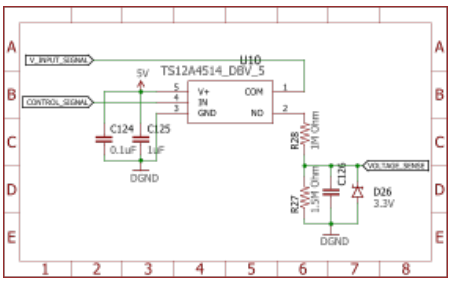
The choice for a micro-controller was the MSP430FR5994 [40]. This chip belongs to the MSP430 micro-controller family that has low power capacities. It can activate several types the low power modes, meaning that in the same cases is able to enter into a state where the CPU can be turned off and waiting for something to do and have the possibility

to use the low power crystal oscillator, to generate the clock signal.

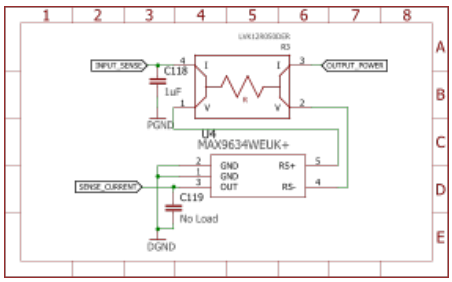
In order to have control of the system, some analog signal is required for the autonomous controller algorithm. So, for the micro-controller to be able to take readings, there's the need to implement the analog interface. The signals that are required to measure are the current for the outputs, the current supplied by the harvester, the voltages from the supercapacitors and the voltages for the external supplies. Since the ADC from the MSP430 micro-controller only can read voltages below $3.3V$ and all the voltages that it needs to measures can reach $5V$, it is necessary to implement the circuit present in the Figure 3.14a, this circuit is a simple voltage divider.

For current measurement it is necessary to use the circuit of Figure 3.14b. The circuit consists of a resistor in series with the DC/DC converter output and an amplifier that measures the voltage difference to the terminals of that resistance. Given by Ohm's law, it is possible in the controller to calculate the current, using the voltage at the terminals of the resistor being measured by the micro-controller ADC.

In the circuit for sensing the voltage in the super-capacitor there is present the chip called TS12A4514 that is an analog, switch [44]. Its purpose is to prevent the discharge of the super-capacitor through the voltage divider when no measurement is being made.



(a) Circuit for sensing super-capacitor and external voltages.



(b) Circuit for sensing DC/CD and harvester output currents.

Figure 3.14: Simplify circuits for analog signal sensing (voltage and current).

For the system to be able to interpret the real meaning of the signals, the equations 3.4 and 3.3 are used to convert the voltage signal from the circuit in Figure 3.14b and to convert the voltage from the circuit in Figure 3.14a to the true value of the voltage in the super-capacitor, respectively,

$$SENSE\_CURRENT = Gain \times (V_{INPUT\_POWER} - V_{OUTPUT\_POWER}) \tag{3.3a}$$

$$I_{R_3} = \frac{(V_{INPUT\_POWER} - V_{OUTPUT\_POWER})}{R_3} = \frac{\frac{SENSE\_CURRENT}{Gain}}{R_3} \tag{3.3b}$$

$$VOLTAGE\_SENSE = \frac{R_{28}}{R_{28} + R_{27}} \times V\_INPUT\_SIGNAL \tag{3.4}$$

3.3.3 Software Implementation

The software implementation of the controller was done on the MSP430 family chip platform. This controller allows for manual and automatic control of the system parameters, like enabling the super-capacitor charges and the outputs. The automatic controller is the Power Management algorithm, which has as main responsibility, the choice and the control of the energy allocation, to feed the outputs (energy supply done by supercapacitors).

For the purpose of this thesis and to test the implementation of an autonomous controller, for power capabilities management, using a micro-controller, a simple algorithm was created, with the capability of choosing which super-capacitor will be connected to which output to supply energy. It also controls the charging of the super-capacitor taking into account the maximum limits of current supplied by the harvester.

3.3.3.1 Super Capacitor Control Algorithms

The software structure is divided into three parts. Being the communication the first which is responsible for receiving, sending and interpreting the messages between the PMU and the higher-level systems. The measurement of values is the second part, it has the responsibility to read the voltage from the supercapacitors and the current from the outputs. the final part is the algorithm for autonomous power management operation, which has the function of controlling everything automatically.

The autonomous algorithm is working in three steps, starting with the monitoring of the energy values of supercapacitors (Figure 3.15), according with the interpretation of these values, in which it has been verified that one must see if there is a super-capacitor with better capacitance to supply power, then follow the choice of a new capacitor if it exists. This choice can however be made in two ways depending on the energy value of the super capacitors (Figures 3.17 and 3.16). The last step is the charging of the supercapacitors (Figure 3.18), if any super-capacitor that is not being used and still have the capacity to receive more energy it will be charged, checking the status of capacitors for charging is independent of the first stage.

Each super-capacitor has implemented one copy of the autonomous algorithm, in which its operation is independent of the algorithms of the other super capacitors and all work in parallel.

The first step of the automation algorithm serves the purpose of verifying the voltages levels of the supercapacitors. The values of the supercapacitors are divided in 4 intervals when these values go outside one interval and enter in another of the define intervals (only once for each interval) the second step is activated. This means that the algorithm is not always asking to see if there is a capacitor with more energy. As will be seen in more detail below, the choice of the best super-capacitor is made with the voltage value of the capacitor as a priority. If the algorithm is always checking, it will always be switching between capacitors, thus preventing them from being charged.

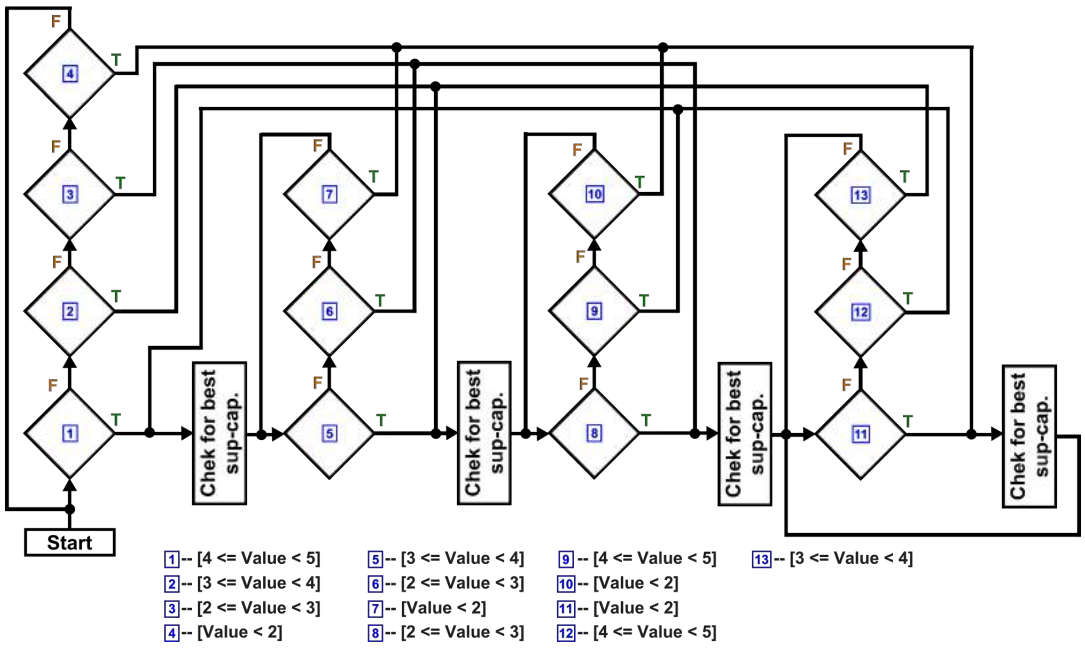


Figure 3.15: Control algorithms for evaluating the super-capacitor condition.

What happens in the first step, in more detail and as Figure 3.15 shows, begins with the choice of the interval where the algorithm begins to check if the values are exiting an interval, this is the first time that the super capacitor as entered that interval. If it is the first one, it is activated the choice for the best capacitor, if after choosing the same or another capacitor, this one is still being used, the algorithm waits until it enters another interval and then triggers again the choice for the best capacitor.

The comparisons 1, 2, 3 and 4 are the initial steps, when the algorithm starts, that define the initial interval where the value of the supercapacitor is located. In the beginning, it is assumed that it is the first time the capacitor enters this range and a check is made to choose witch interval the value belongs to. after that, if the capacitor stays active in that interval, the algorithm is waiting in that loop until the value of the capacitor belongs to another interval and activate the second algorithm for calculating the best supercapacitor. As an example, assuming that the interval of comparison 1 is chosen, the algorithm remains in that loop composed of comparisons 5, 6 and 7 until the value is between those intervals activating another check for calculating the best supercapacitor and repeats the process again with another loop correspondent to another interval. It is to denote in the Figure 3.15 that in the loop 5, 6 and 7 there is no comparison equal to the comparison 1, thus ignoring any value within that interval, since the verification corresponding to that interval has already been made and we only want it to be done once.

The loops done in this algorithm are time control. Since we are using ADC to measure the necessary values and these ones are periodically triggered, there's now need to be always comparing the same ADC value between periods since the value is the same. So only one loop is done in each period.

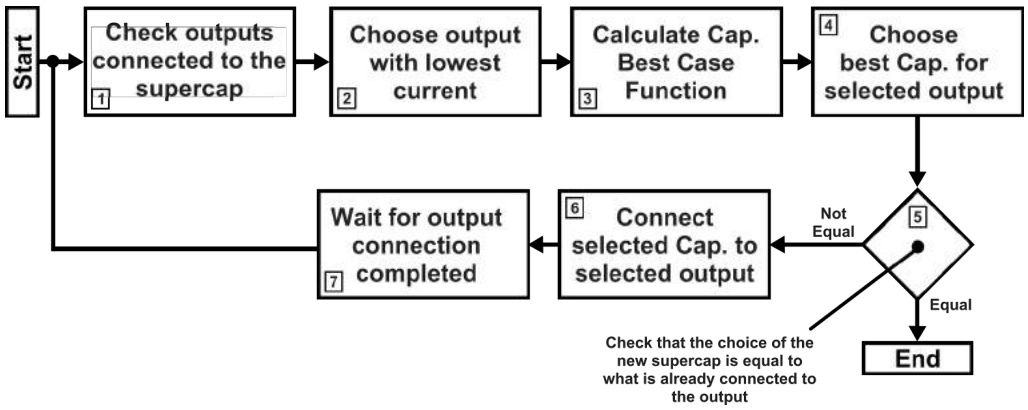


Figure 3.16: A second control algorithm for choosing the best super-capacitor for the output.

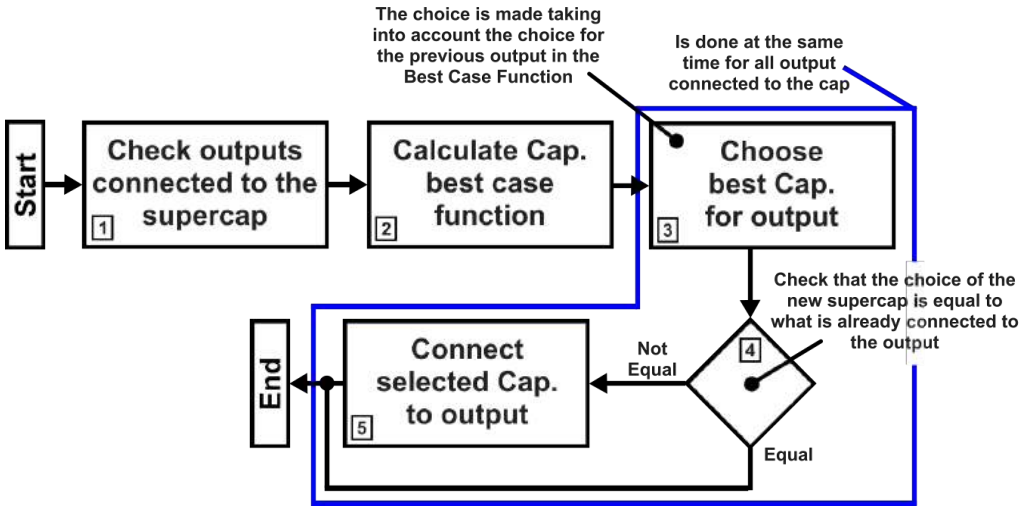


Figure 3.17: First Control algorithm, for choosing the best super-capacitor for the output.

The second stage of the algorithm corresponds to the process of calculating and choosing the best supercapacitor to be connected to an active output. This process involves computing the equation 3.5 to obtain a value that describes the performance of the supercapacitor. The higher the value obtained by the function for each capacitor, the better the capacitor is to be connect to an output.

$$f_{BestCap} = \begin{cases} V_{SupCap} - \sum I_{output_{SupCap}} - I_{output} & \text{if } I_{output} \text{ not conected to SupCap} \\ V_{SupCap} - \sum I_{output_{SupCap}} & \text{if } I_{output} \text{ conected to SupCap} \end{cases} \quad (3.5)$$

The purpose of the implementation of the equation 3.5 is to allow the quantification of the supercapacitors performance related to wits voltage and the current we will need to supply or is already supplying. Also the propose of the current being subtracted, is justified by the fact that the more current withdrawn from the capacitor the faster it will discharge. In the equation 3.5 the higher the total amount of current of the outputs connected to the supercapacitor the smaller will be the value of the equation. There for,

indicating that the capacitor may not be the best to connect to an output. For the voltage effect, it's required the opposite, because the higher the voltage the supercapacitor has, the longer it remains active and thus avoiding unnecessary switching.

In order to know which supercapacitor is best to provide power to an output, it is necessary to calculate the equation 3.5 for each supercapacitor, taking into account the effect that the output in question can have on the supercapacitors that have the possibility to be connected to it, as that choice is made for the one with the highest value. The effect of the output on the supercapacitor is given by the parameter I_{output} of the equation 3.5. this parameter is obtain by the ADC on the microcontroller. The parameter $\sum I_{output_{SupCap}}$ (equation 3.5) is the sum of all the currents of the outputs connected to the capacitor for which the equation is being calculated.

The effect of the output on the supercapacitor is obtain withe the current I_{output} being add to the total current of the supercapacitor, in case this one is not connected to it, this allows for understanding the effect that a output will have in the supercapacitor. other way if the output is already connected to the supercapacitor we already now its effect, this is already used in the parameter $\sum I_{output_{SupCap}}$ from equation3.5.

This second step has two methods of calculating the choice of the super-capacitor, demonstrated in the Figures 3.17 and 3.16. The first method, Fig. 3.17 differs from the second in the way it calculates the best capacitor for each output connected to a capacitor. That is, this method calculates for all outputs at the same time, [12] the best capacitor taking into account the choice of the previous output [13]. The effect of the previous choice is made in the parameter $\sum I_{output_{SupCap}}$, both for the capacitor where the output was previously connected, and for the super-capacitor where the output will be connected before calculations, again to the new output. The effect is shown in equation 3.6, where the equation 3.6a is used in the old capacitor and the equation 3.6b is used for the new super-capacitor,

$$\sum I_{new_{output_{SupCap}}} = \sum I_{old_{output_{SupCap}}} + I_{output} \tag{3.6a}$$

$$\sum I_{new_{output_{SupCap}}} = \sum I_{old_{output_{SupCap}}} - I_{output} \tag{3.6b}$$

In the second method, the only difference to the first one is that it now only makes the choice of the new super-capacitor for one output at a time. The next choice is made when the super-capacitor of the old choice has terminated the connection process with the output.

Both the same methods follow the same structure. They start by checking which outputs are connected and calculate for each output the equation 3.5 which indicates

[12] The calculation for all the outputs connected to a capacitor is made in the same period of one sample of the measured signals, it means that the values are all equal for the calculation of each output. In fact the calculation is not done at the same time, because in C-language the whole code is executed sequentially.

[13] The calculation for each output makes one after the other, means that the calculation for the next output will be done taking into account the effect of the previous output on the chosen super-capacitor.

which is the best capacitor. Then the choice of the best value is made, it is here that the methods differ. If the capacitor that was chosen is not equal to the capacitor the output is already connected, proceed to connect the supercapacitors to the outputs. This connection in both methods is "make before break", which means that the new capacitor is turned on but the old one is only disconnected after a while. This waiting time is imposed by timers. At the end of the connection in the case of method one ends the method and in the case of method two returns to the beginning to calculate the remaining outputs.

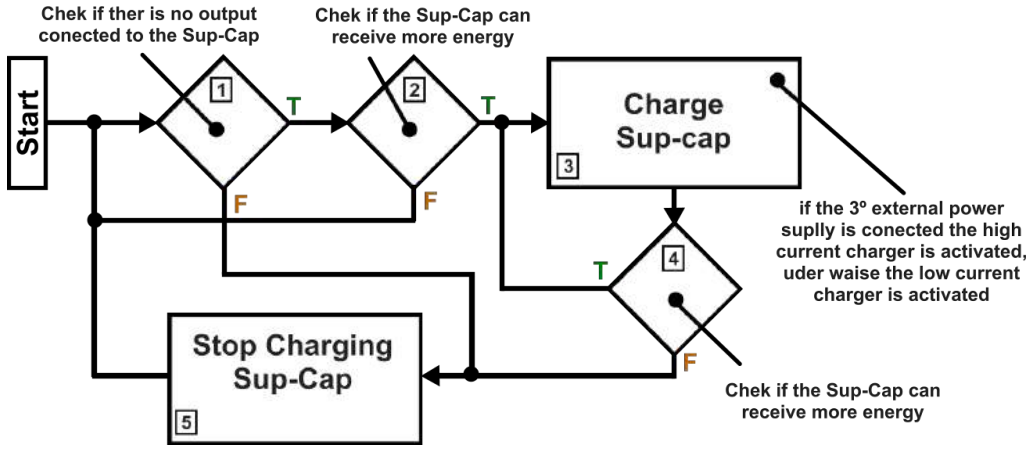


Figure 3.18: Control algorithm for charging the super-capacitor to full capacity.

The last step of the autonomous algorithm corresponds to the charging of the supercapacitors, it's process is shown in the Figure 3.18. The charging process starts by checking if there is any connected output, if it is not, then it is checked if the super capacitor still has room to receive more energy, if this happens the charger of the super-capacitor is activated and will remain activated until it is verified that there is no more space. Once charging is completed, the process is repeated. The value of the current to charge the capacitor depends if the third external power supply is connected, by default the charging process with high current is always selected if an external source is connected.

3.3.3.2 Micro-controller Peripherals Configurations

As previously stated the algorithms were developed to be implemented in a micro-controller of the MSP430 family, so it is possible to use them and it is necessary that it has the capacity for the collection of analog data, waiting times and UART communication interface. It is necessary to use the peripherals of the chip to be implemented as board controller. In order to use these peripherals, it's necessary a prior, its configuration. This will be done in software through the memory register of the chip. The peripherals to be used for the development of the system controller are the clock of the chip, the 12-bit Successive Approximation Register (SAR) ADC, the timers and lastly the primary UART communication. All this configuration can be seen in [45] for more detailed explanation.

Clock

The clock peripherals are configured to use the low power oscillator that generates at $32,768KHz$ frequency. In order to use the specifically physical pins in the microcontroller for this oscillator need to be configured for the specific function of low power clock input. this is done by using the line two of the code in Listing 3.1. The rest of the code is used to configure the various clock signals needed to power the chip. In this case of the auxiliary clock is chosen as the source the oscillator for low power, for the master clock and subsystem clock uses an internal oscillator configured to generate $8MHz$ of frequency, this will be the frequency of the CPU since the master clock is responsible for supplying the clock signal to the CPU. The rest of the peripherals as it will be verified later can choose where they will get the clock signal.

Listing 3.1: Code to configure the clock

```
1  // clock crystal input LF
2  PJSEL0 |= BIT4 | BIT5; // For XT1
3
4  // Configure one FRAM waitstate as required by the device datasheet for MCLK
5  // operation beyond 8MHz before configuring the clock system.
6  // Change the NACCESS_x value to add the right amount of wait-states
7  FRCTL0 = FRCTLPW | NWAITS_1;
8
9  // XT1 Startup clock system with max DCO setting ~8MHz
10 CSCTL0_H = CSKEY_H;                     // Unlock CS registers
11 CSCTL1 = DCOFSEL_3 | DCORSEL;           // Set DCO to 8MHz
12 CSCTL2 = SELA__LFXTCLK  | SELS__DCOCLK | SELM__DCOCLK;
13 CSCTL3 = DIVA__1 | DIVS__1 | DIVM__1;   // Set all dividers
14 CSCTL4 &= ~LFXTOFF;
15 do{
16   CSCTL5 &= ~LFXTOFFG;                // Clear XT1 fault flag
17     SFRIFG1 &= ~OFIFG;
18 } while (SFRIFG1 & OFIFG);             // Test oscillator fault flag
19 CSCTL0_H = 0;                          // Lock CS registers
```

Comunication UART

The first thing to do, to use UART is to configure the physical pins of the chip. As each pin of the chip has several features, we will have to choose the ones that allow the use of the UART interface through the registration P2SELo and P1SEL1 as shown in Listing 3.2. The remaining code is used to represent the UART communication parameters such as baud rate, number of bytes to send (7 or 8 bits), which is the first bit to be sent (Least Significant Bit (LSB)-first or Most Significant Bit (MSB)-first data transmit and receive), etc.

The settings in the Listing 3.2 set a baud rate of 9600 baud and an $8MHZ$ clock, generated by the subsystem clock. No parity bits will be used and in the receiving method, over sampling will be used. However, for the configuration of the baud rate some calculations are necessary to configure the registers. this calculation can be seen in the equations 3.7, 3.8 and 3.9,

$$N = \frac{f_{BRCLK}}{baudrate} \tag{3.7}$$

$$UCBRx = INT(N/16) \tag{3.8}$$

$$UCBRFx = INT([(N/16)\check{}INT(N/16)]16) \tag{3.9}$$

UCBRSx can be found by looking up the fractional part of N (= $N - INT(N)$) in Table 24-4 from [45].

Listing 3.2: Code for configure the UART peripheral

```
P2SEL0 &= ~(BIT0 | BIT1);
P2SEL1 |= (BIT0 | BIT1); // USCI_A3 UART operation

UCA0CTLW0 = UCSWRST;                    // Put eUSCI in reset
UCA0CTLW0 |= UCSSEL__SMCLK;             // CLK = SMCLK
UCA0BRW = 52;                           // 8000000/16/9600
UCA0MCTLW |= UCOS16 | UCBRF_1 | 0x4900;
UCA0CTLW0 &= ~UCSWRST;                  // Initialize eUSCI
UCA0IE |= UCRXIE;                       // Enable USCI_A3 RX interrupt
```

Timer for ADC sampling

The timer is configured for continuous operation, and generating an output signal of a pulse, to activate the start of the sampling process in ADC, at a frequency given the equation 3.10, the code for configuring the timer is present in Listing 3.3. The clock source for this peripheral is the auxiliary clock, meaning that the frequency is $32,768KHz$.

$$TIMER_{frequecy} = \frac{TIMER_{CLOCK_{frequecy}}}{SamplingTime - 1} \tag{3.10}$$

The sampling timer parameter of the equation 3.10 is the number of clock cycles, meaning that the sampling time in seconds is given by equation 3.11,

$$SamplingTime = \frac{1}{TIMER_{CLOK_{frequecy}}} \times (SamplingTime - 1) \tag{3.11}$$

Listing 3.3: Code to configure the Timer for ADC sampling

```
// Configure Timer0_A0 to periodically trigger the ADC12
TA0CCR0 = SamplingTime-1; // PWM Period -> (1/32.768KHz)*(SamplingTime-1)
TA0CCTL1 = OUTMOD_3;      // TACCR1 set/reset
```

```
4 TA0CCR1 = SamplingTime-1; // TACCR1 PWM Duty Cycle
5 TA0CTL = TASSEL__ACLK;    // ACLK
```

SAR ADC

The ADC requires clock input for the signal sampling & hold time and for conversion time, so the peripheral internal clock source is used. The ADC is configured to sample, single ended signals in a continuous and sequential way from 10 analog channels (ADC12CONSEQx bits from ADC12CTL1 register).

The start of the sampling and conversion of a channel sequence is controlled by a pulse (ADC12SHP bits of the ADC12CTL1 register). After the sampling and conversion of the first channel terminates, automatically begins the sampling time for the second channel. This process is done until it arrives in the last channel, after this one is done the ADC is powered down and it waits until another pulse starts the sequence (ADC12MSC bits from ADC12CTL0 register).

The ADC is configured to receive the pulse form Timer A0 (ADC12SHSx bits of ADC12CTL1 register). The configuration of the ADC can be seen in listing 3.4. The time for the sampling period needs to be configured, this is done through the ADC12CTL0 register in the ADC12SHT0 field (4 bits). The choice for the number the cycles that the sampling time takes depends on the physical characteristics of the signal path to the pins of the chip. Normally this can be modeled with a low pass filter, but to calculate the value of the capacitance and the resistance is complicated, due to the complexity of the PCB layout, so the configuration value was done by trial and error, which resulted in the choice of 16 cycles of the clock. It's also important to point out, that the tolerance of the components can influence the sampling time, but likely the ADC has sufficient degree of reconfigurability to address this case, by trial and error. This ADC is also configured for 12 bit resolution (ADC12RES bits of ADC12CTL2 register).

For the 10 channels it is necessary to configure the physical pins and also the ADC memory registers which stores which channels to use for the sampling sequence (registers ADC12MCTLx, $x = [0;9]$).

Listing 3.4: Code to configure the SAR ADC

```
1  P1SEL1 |= ( BIT0 | BIT1 | BIT2 | BIT3 | BIT4 | BIT5 );
2  P1SEL0 |= ( BIT0 | BIT1 | BIT2 | BIT3 | BIT4 | BIT5 ); // ADC operation
3  P3SEL1 |= ( BIT0 | BIT1 | BIT2 | BIT3 );
4  P3SEL0 |= ( BIT0 | BIT1 | BIT2 | BIT3 ); // ADC operation
5
6  ADC12CTL0 &= !ADC12ENC & !ADC12ON & !ADC12SC;
7  ADC12CTL0 |= ADC12SHT0_2 | ADC12MSC;
8  ADC12CTL1 |= ADC12SHP | ADC12CONSEQ_3 | ADC12SHS_1;
9  ADC12CTL2 = ADC12RES_2;
10 ADC12CTL3 = ADC12CSTARTADD_0;
11 ADC12MCTL0  |= ADC12INCH_0;            // A0 ADC input select  (V C1)
```

```
12 ADC12MCTL1  |= ADC12INCH_1;             // A1 ADC input select  (I Vdd1)
13 ADC12MCTL2  |= ADC12INCH_2;             // A2 ADC input select  (V C2)
14 ADC12MCTL3  |= ADC12INCH_12;            // A12 ADC input select (I Vdd2)
15 ADC12MCTL4  |= ADC12INCH_13;            // A13 ADC input select (V C3)
16 ADC12MCTL5  |= ADC12INCH_14;            // A14 ADC input select (I Vdd3)
17 ADC12MCTL6  |= ADC12INCH_15;            // A4 ADC input select  (V C4)
18 ADC12MCTL7  |= ADC12INCH_3;             // A3 ADC input select  (I Vdd4)
19 ADC12MCTL8  |= ADC12INCH_4;             // A15 ADC input select (V external))
20 ADC12MCTL9  |= ADC12INCH_5 | ADC12EOS; // A5 ADC input select  (I total)
```

Timer for switching the supercapacitors

The configurations for the timers, responsible for count the time that the switch must be connected, only needs the count number of clocks. So the amount of time that the switches will be also given by equation 3.11. The clock signal for all timers is sourced by the auxiliary clock with a frequency of $32,768KHz$. The code for configuring the timers can be seen in the Listing 3.5.

Listing 3.5: Code to configure the Swiches Timers

```
1  // timer A1, A2, A3 and A4 configuration
2  // time -> (1/32,768KHz)*Switche_Time_Constante
3  // Configure Timer0_A1
4  TA1CCR0 = Switche_Time_Constante;
5  TA1CTL = TASSEL__ACLK;
6  // Configure Timer0_A2
7  TA2CCR0 = Switche_Time_Constante;
8  TA2CTL = TASSEL__ACLK;
9  // Configure Timer0_A3
10 TA3CCR0 = Switche_Time_Constante;
11 TA3CTL = TASSEL__ACLK;
12 // Configure Timer0_A4
13 TA4CCR0 = Switche_Time_Constante;
14 TA4CTL = TASSEL__ACLK;
```

3.4 System Test Results

The system to be tested, was implemented on a printed circuit board with discrete components, the layout was made to allow the integration of all blocks in the same platform. In order to test the prototype, the test setup will be performed, requiring an interface capable of controlling the same, this interface will be deployed in the computer. Figure 3.19 demonstrates the graphical interface that will allow to control all aspects of the board. The interface will be able to control the outputs and the power MUX by making the connection between the supercapacitors and converters. It will also allow to control the charging for high or low current. Since it is also required to test the autonomous

algorithm the interface makes the control of the same. All the data measured by the controller, will also be available in the interface, thus allowing to validate the state of the system.

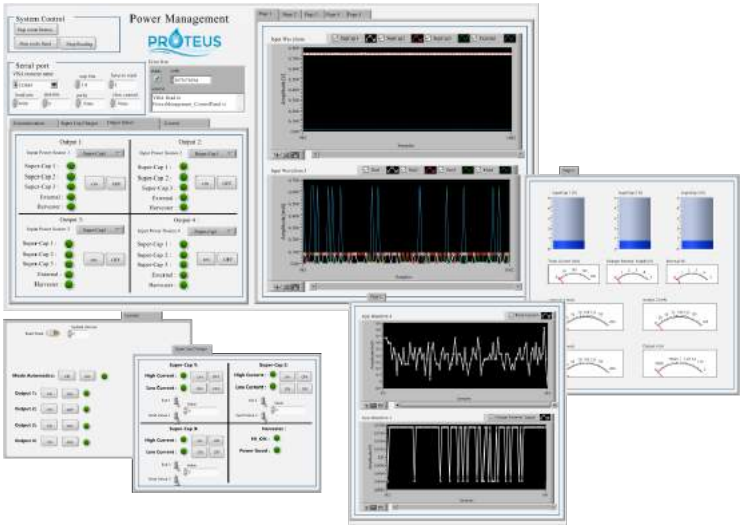


Figure 3.19: Computer graphical interface to visualize and control the PMU Board signals (Super-capacitor voltage, output current, switch control signals, etc.).

3.4.1 Test Setup

The test setup consists of connecting the board to the Texas Instruments launch pad, this serves as a communication interface to the computer and connects to a simple circuit to serve as a load on the output.

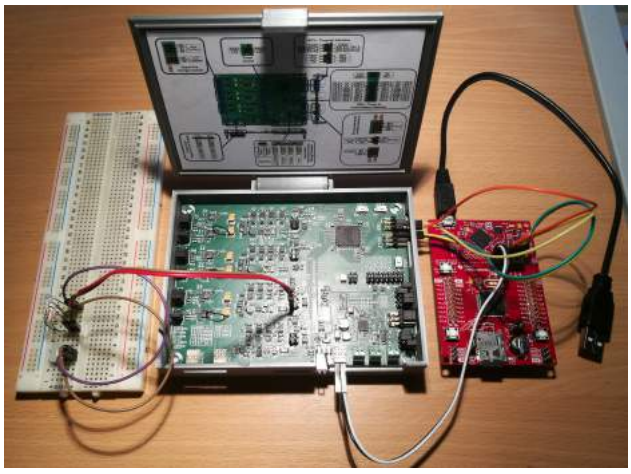


Figure 3.20: PMU board test setup. Consist of a load circuit to test the power output and launch pad to serve as a communication interface (UART to USB) with the computer.

Figure 3.20 demonstrates the setup test configuration and connections. The board will be operating in automatic mode operation, to test the algorithm and by applying

the load into the output, it will be possible to see the supercapacitors commutations and charges on the graphical interface. In order to start the test setup is necessary to give the command to start the autonomous mode and them to power on the output where the load is applied.

The load circuit is implemented with a Light Emitting Diode (LED) with a resistance in series, for a visual way to see if the output is connected and a trimer in parallel for controlling the output current. For the test, it will be applied to the output a current near the maximum limit allowed for the low power output. Also for the test of the board, the harvester block will be bypassed with an external power supply, this allows to test the board without the concern of energy availability and the test can be easy to set up in the laboratory.

3.4.2 Results

In the tests made to the board, there were some unexpected results. These were respectively related to the power-off of the board due to the load switch for low currents. These switches require a bias pin, when it is no longer polarized and if there is still power in the supercapacitors, there is a transfer of power through this pin to the board's general power, which is connected to the harvester.

Also, some of the limit values for the supercapacitors minimum voltage to power the converters had to be made by trial and error, due to the fact that have to do with (it was expected, but not considered in calculations) voltages drops in the path of the power to be delivery to the output (power MUX). Meaning that the minimum value of the DC/DC converter operation add to be increased, this can be seen in the code for the constant related to the super capacitor limits in Listing 3.6.

Listing 3.6: Code for Super Capacitor constantes

```
1  // 2.3V  -> 2,3 / 0,0013427734375 = 1712,872727272727272727272727272727 [LSB]
2  #define SupCapVoltage_TypeConect_Threshold 1713
3   // 2.34V -> 2,34 / 0,0013427734375 = 1742,661818181818181818181818181818 [LSB]
4  #define SupCapVoltage_Conect_ThresholdLimit 1742
5  // 2.18V -> 2,18 / 0,0013427734375 = 1623,505454545454545454545454545455 [LSB]
6  #define SupCapVoltage_ContinuousConect_ThresholdLimit 1624
7  // 2.16V -> 2,16 / 0,0013427734375 = 1608,610909090909090909090909090909 [LSB]
8  #define SupCap_MinLimit_Voltage 1609
9  // 4.8V -> 4,8 / 0,0013427734375 = 3574,690909090909090909090909090909 [LSB]
10 #define VoltThreshold_5V 3575
11 // 4V -> 4 / 0,0013427734375 = 2978,909090909090909090909090909091 [LSB]
12 #define VoltThreshold_4V 2979
13 // 3V -> 3 / 0,0013427734375 = 2234,181818181818181818181818181818 [LSB]
14 #define VoltThreshold_3V 2234
15 // 2V -> 2 / 0,0013427734375 = 1489,454545454545454545454545454545 [LSB]
16 #define VoltThreshold_2V 1489
```

The first parameter in Listing 3.6 is related to the level of super-capacitor voltage in which will be making the choice for the type of method to find the best super-capacitor. The second and third constants are related to the last value where the algorithm in Figure 3.15 does a new verification of the output connected in the super-capacitor. The last value is the voltage limit that allows the converter to operate.

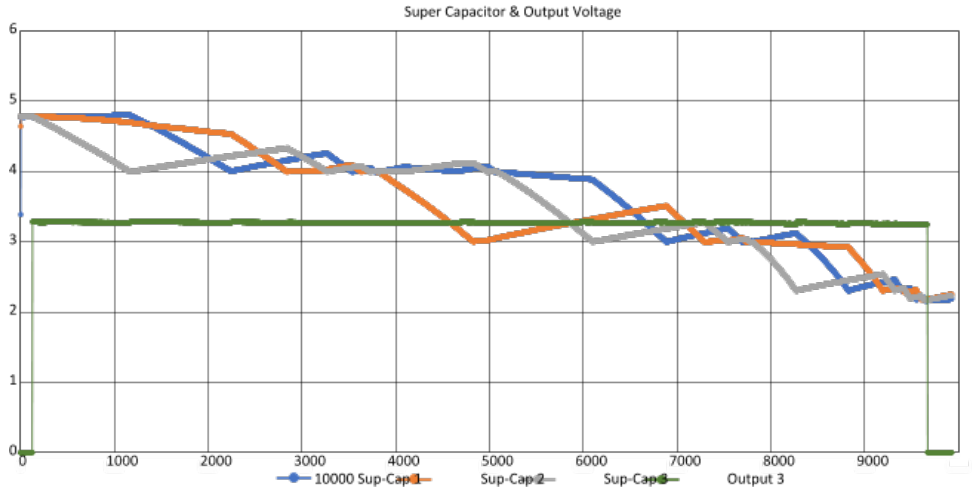


Figure 3.21: Experimental data retrieved from the test setup in Figure 3.20. The data represent the commutations between supercapacitors to supply power to output 3 that has an output current of approximately $100mA$.

Experimental data retrieved from the test setup in Figure 3.20. The data represent the commutations between supercapacitors to supply power to output 3 that has an output current of approximately $100mA$. In Figure 3.21 it's possible to see the algorithm working as expected, when the command for powering the output is given the algorithm connects the super capacitor. When its voltage starts to go down and reaches the first stage to check the state of the capacitors ($4V$), a new capacitor is chosen and switched with the previous capacitor. It is possible to verify that the algorithm in each step performs a check of the capacitors and usually switches to another one with a higher voltage. It is also found that when the capacitor is not in use, it is immediately charged if the total current does not exceed the possibilities of the harvester, in which case an external source is being used, but that the limits are maintained.

In Figure 3.22 we have presented a more detail view of the signals from the moment where the output is turned off, from insufficient input voltage. It demonstrates that the system, when the minimum voltage is reached, powered down the output, until that moment the output is maintained stable. When the minimum input voltage of the DC/DC converter is lowered, we obtain a non-stable output voltage near the event where the power is finally turned off. This can be verified in Figure 3.23 where the test was made with different constant level presented in the Listings 3.6.

The charge of the super-capacitor is only done when no output is connected to it and it is current, in addition to the current supply being provided by the harvester, does not

exceed the maximum value. Figure 3.24 shows the total current that is being delivered to the system and we can see that in some instances there is an increase in the current value, this corresponds to the current that the charger is charging the capacitor. It is possible to see that the current does not exceed the maximum limit.

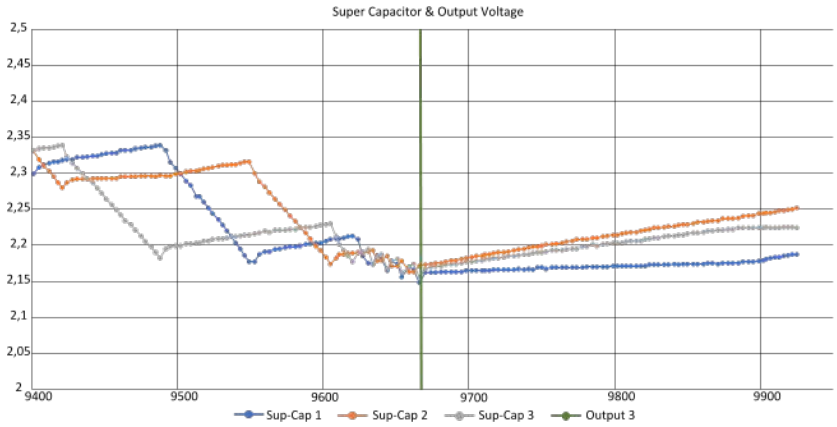


Figure 3.22: A more detailed view of the final moments of the experimental data results. The graph demonstrates the moment where the output is disconnected due to insufficient energy in the supercapacitors.

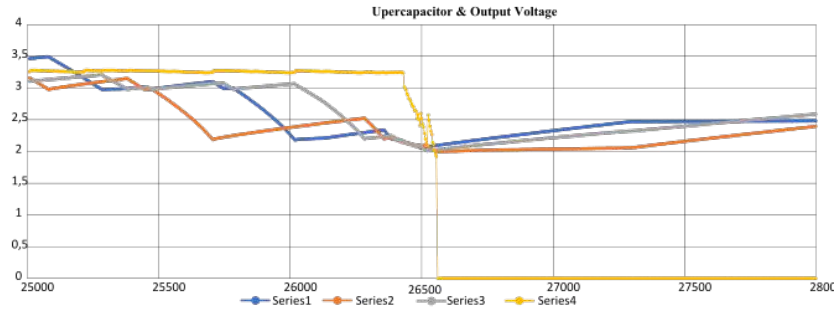


Figure 3.23: A more detailed view of the final moments of the experimental data results with lower configuration values than those used to obtained Figure 3.22.

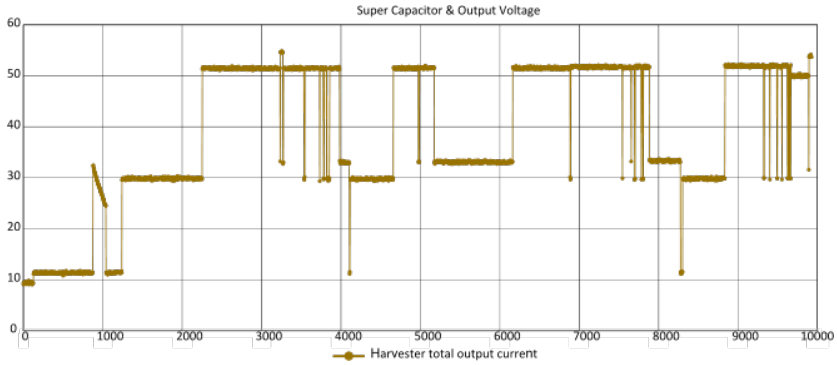


Figure 3.24: Experimental data retrieved from the test setup in Figure 3.20. The data represents the total current being supplied to the board. A percentage of this current is used by the super-capacitor chargers.

3.5 Conclusion

By using super capacitors as temporary energy sources we can use a low power source to operate a high-power circuit for a limited period of time. Meaning that a given system can operate, in higher current consumption, functions for a limited period of time. The use of the DC/DC converter on the output expands the time of operation, by using a wide range of super capacitor voltages. The charger allows for efficient control of the energy to be stored in the capacitor without compromising the limitation of the source. It also allows for a rapid charging period of time compared to an RC type of charging circuit. In general, the system allows for a good power control by giving the possibility to implement intelligent algorithms to control the distribution of energy, energy only goes to where its need, reducing the waste of energy to circuits that do not need to be powered.

CHAPTER 4

CADIT

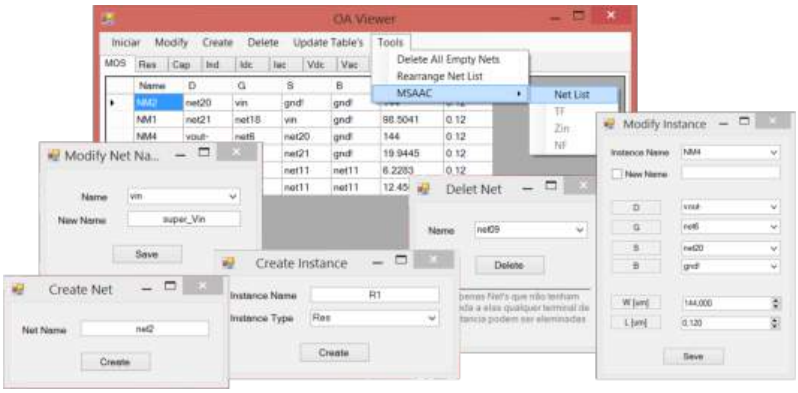


Figure 4.1: Graphical interface of the CAD software available to the user.

4.1 Introduction

Due to the high cost of making the layout Integrated Circuits (IC) masks, it is necessary to reduce the risk of circuit performance issues. To be possible to predict the circuit operation is necessary to obtain the equations that model the circuit characteristics (e.g., gain, Zin, NF). Making the extraction of this equations by hand, is not trivial and may even be impossible, or take a long time. In order to obtain complex precise circuit equations, we turn to CAD to simplify this process, [46, 47, 50, 51].

The CAD software makes possible a complete and accurate (depending on the modulation quality) theoretical analysis of the circuit, reducing the time and cost of circuit design. In this chapter a Si2 OpenAccess Database based toll for circuit analysis (Figure 4.2) is presented that combines a symbolic equation extractor with circuit parameters (transistors, resistors, capacitor's, etc), computed using precise models.

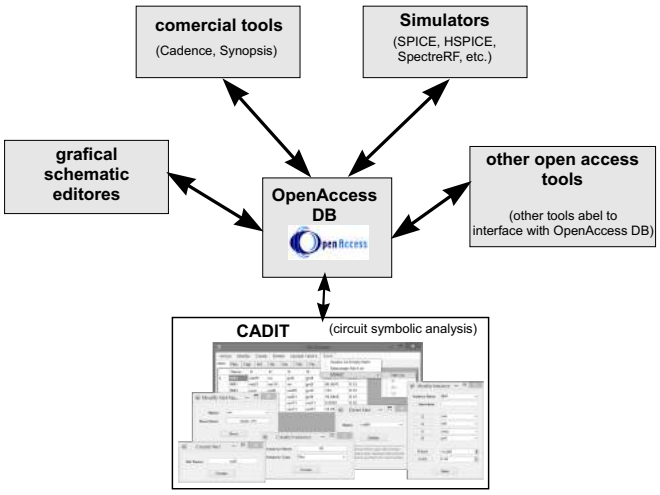


Figure 4.2: Main blocks of CADIT tool.

Figure 4.1 shows the Computer Aided Design Integration Tool (CADIT) graphical user interface. As can be seen, the software has available a variety of functions to use the database, open access, such as delete, create and modify instance and nets, and offers the tools to calculate the circuit equations.

As previously referred the tool is used to design an wideband LNA (for an RF front end) that uses a noise canceling technique in order to minimize the NF along the input bandwidth.

4.2 Software Structure and Implementation

The developed software uses the tool [35], which allows the software to find the equations that characterize the circuit (Gain, Zin, NF), and also uses the OpenAccess database for storing the circuit (connections and instance).

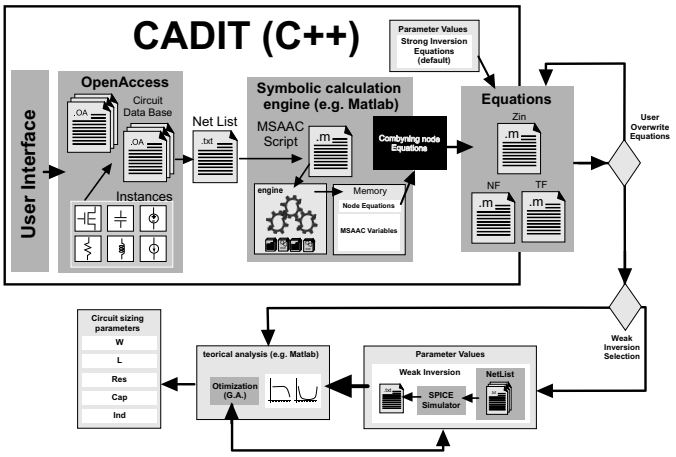


Figure 4.3: The CAD software diagram of the process to calculate the circuit equations and it simulations for circuit sizing.

The tool [35] derives the circuit equations by means of the modified nodal analysis method [24], and then solves the equations symbolically. After the equations are obtained from each node through the [35], the software calculates the gain, Zin and the NF, giving the user the choice of small signal model type (transistors parameters: gm, gmb, gds, Cgs, Cgd, Csb and Cdb) for the transistors. The equations that model those parameters are expressed in Appendix C. It is also possible to choose for the NF equation the introduction of the effect of flicker noise. Figure 4.3 represents this process.

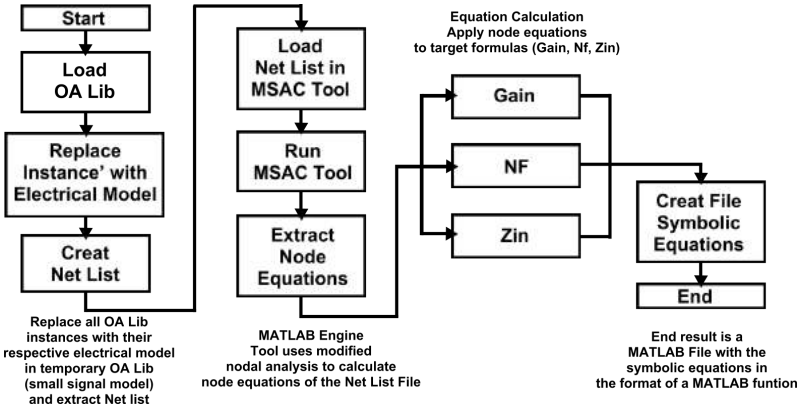


Figure 4.4: The CAD software process work-flow to obtain the symbolic equations files of the circuit functions.

The process of obtaining the equations starts by creating the necessary instances (transistors, resistances, capacitors, inductors, DC voltage and current sources) and their connections (net list). After the circuit is complete the net list is created in `.txt` file. Depending on what type of equation (Gain, NF and Zin) the user wants to calculate the software passes the net list file to the MSAAC tool [35] to obtain the circuit node equations, after that the software is responsible for combining the node equation to obtained the desire equation, the final equation is then passed to a `.m` file to allow the user to used it in Matlab to simulate its behavior. Depending on the type of equation requested the software differs slightly in the way that it calculates but still maintains principal fundamental described above. Figure 4.4 represents the calculation flow.

4.2.1 Equations automatically generated by CADIT

The tool CADIT is able to compute the Transfer Function (TF) (gain) equation $\left(\frac{Vout}{Vin}\right)$, the Zin equation $\left(\frac{Vac1}{I_{Vac1}}\right)$ and the NF equation(4.1) for a given circuit. Each expression of Zin and TF are computed on a single interaction with the MSAAC module. On the other hand, the final expression of the NF is obtained by several interactions with the MSAAC module, one interaction per each noise source included in the circuit, applying the superposition theorem, shown in the Figure 4.5. In equation 4.2 the number of loops will be $N+K$, being N the number of transistors plus resistors, thermal noise sources and K the number of transistors flicker noise sources.

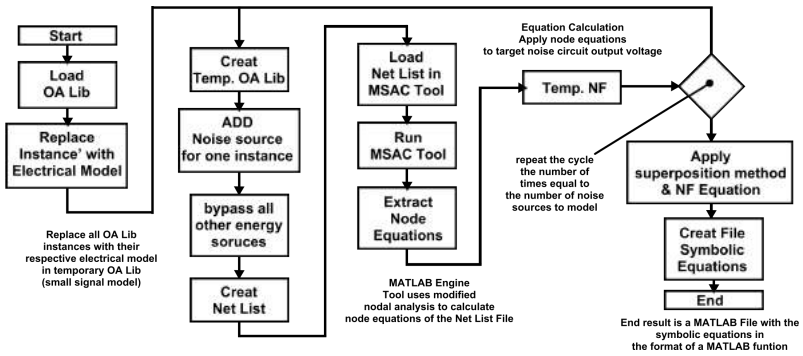


Figure 4.5: The CAD software process work-flow to obtain the NF symbolic equations files of the circuit.

Also the parameters $\overline{Vout_{Thermal,j}}^2$ and $\overline{Vout_{Flicker,j}}^2$ of the equation 4.2a represent the effects of thermal and flicker noise of a single transistor, eliminating all other noise sources. Considering the TF expression, in terms of input and output, it can be computed differential or single ended. In case of differential, the tool replaces $Vout$ and Vin by $(Vout = vout_+ - vout_-)$ and $(vin = vin_+ - vin_-)$,

$$NF = 10log_{10}\left(1 + \frac{\overline{Vout_{noise}}^2}{\overline{Vout_{RS1noise}}^2}\right) \tag{4.1}$$

Equation 4.2 represents the superposition method,

$$\overline{Vout_{noise}}^2 = \sum_{j=1}^{N}\left(\overline{Vout_{Thermal,j}}^2\right) + \sum_{j=1}^{K}\left(\overline{Vout_{Flicker,j}}^2\right) \tag{4.2a}$$

$$N = n.\ of\ MOST\ plus\ resistors, K = n.\ of\ MOST \tag{4.2b}$$

4.2.2 Small signal models

The Table 4.1 presents the implemented models for the transistors small signal circuit.

Table 4.1: All, small signal, models available to the user

Model Name	gm	gmb	gds	Cgs	Cgd	Cdb	Csb
md11	✓						
md12	✓		✓				
md13	✓	✓	✓				
md14	✓		✓	✓			
md15	✓		✓	✓	✓		
md16	✓	✓	✓	✓	✓	✓	✓
md17	✓	✓	✓	✓		✓	✓

The tool [35] that calculates the node voltages of the equivalent small signal circuit of the main circuit does not take into account the operating point of it. This means that is

left to the user to choose the necessary equations to model the parameters of the small signal models.

In the equation files the software assumes that all instances of type transistor are in saturation region, meaning that the equations for all transistor parameters are from saturation region (Appendix C). This model parameters equations can be overwritten by the user for Other operating regions (weak and moderate inversion), is only necessary, to change the function header in the equation file and implement these functions in `.m` file. In order for the Matlab to call those function, all files must be in the same directory or it's necessary to add the path to the Matlab environment.

Computation resources can limit the use of the most complete version of the model of the transistor, i.e. (`md16`). The parasitic capacitance, cgd, of the transistor NM2 in the circuit depicted in Figure 4.6 originates an expression with multiple terms that consumes a considerable amount of resources.

4.2.3 Software Prerequisite for Normal Operation

In order to be possible to the software to calculate the equations some prerequisites have to be met. In case of single input, a AC source supply must be present with the name `Vac1` and the input net name must be `vin`. For the case of differential input the net names must be `vin+` for positive input and `vin-` for negative input. In case of single output, the net name has to be `vout`. For the case of differential output, the net names must be `vout+` for positive output and `vout-` for negative output. For instance, for the type transistor, their names must have a `N` or a `P` to differentiate from Nmos or Pmos. If there first letter it's not one of them, the software assumes it's a Nmos type.

The TF equation is the relation off the output to the input voltage. This means that this is a voltage gain, as shown in the equation 4.3,

$$Gain = \frac{vout}{vin} \tag{4.3}$$

4.3 Software Test Results

As the tool allows to calculate the equations of a circuit, for the purpose of testing the tool, the equations of a low noise amplifier for Very-Large-Scale Integration (VLSI) implementation will be extracted (Figure 4.6). After equation extraction a comparison between theoretical data, retrieve from the simulation of the equations, is done with proprietary simulation software (CADENCE, Spectre).

4.3.1 Circuit Analysis

The circuit presented in the Figure 4.6 has two stages of amplification, which are a Common Gate (CG) and Common Source (CS), in which its signal inputs are the same, or are

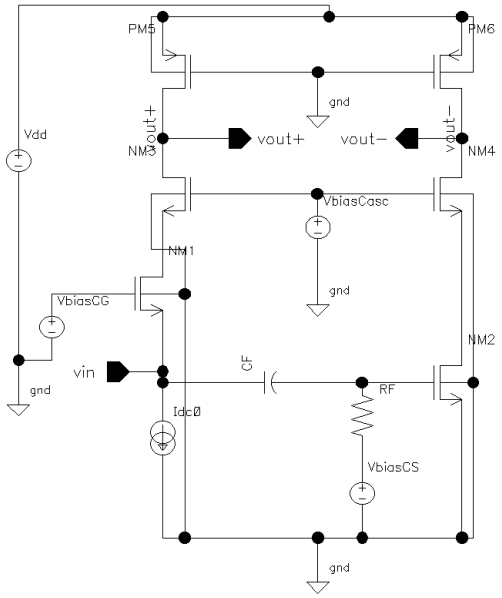


Figure 4.6: LNA circuit.

both the same input signal. This allows for a differential output voltage and an attenuation of the noise introduced by theCG stage. This two-stage configuration means that there is a greater noise contribution from the CS.

The operation principle of this circuit is similar to the circuit used in [6] and [5] with minor enhancements (cascade transistor, active loads in the triode region of the transistor). The equations expressed in [6] can be used here just to have a rough idea of the circuit operation (TF, Zin, NF), for a more precise use [5].

The main diferences between [5] and this are the use of cascade amplification stages instead of just a simpler (one transistor) amplification level and the use of a high pass filter. The loads of the two stages are implemented with P-type MOS transistor in the triode area. The use of transistors instead of resistors leads to an increase of the gain, because they have a higher AC impedance to the same DC current and voltage applied to a resistor, namely for the same Operating Point (OP). The transistors in cascade configuration also impacts the gain, allowing its increase. It is important to note that by introducing more transistors we are introducing more noise sources, which may increase the NF, however if the effect that these additional transistors have in the gain is greater than the effect on the NF this will be diminished.

Between the input signal from the LNA and the CS a high pass filter (RC filter) is added. This filter function is to eliminate the effect of the DC component imposed by the CG. This filter will allow also slightly improve the bandwidth at lower frequencies providing an attenuation of the NF at frequencies above its cutoff frequency. However, there are limitations to filter sizing as this for very low frequencies is no longer able to attenuate the NF because this is very high, due to noise Flicker.

4.3.2 Circuit Equations

The equations in[5] do not demonstrate the effect that the transistors in cascade configuration have in the NF, the TF and in Zin. So, all the equations necessary to analyze the circuit were obtain using CAD software (CADIT). A more detailed but still simplified expression will be presented for the gain and the Zin. these expressions do not take into consideration the effects of higher frequencies (RF-model) and the body effect, among other effects.

Gain

One of the restrictions of an LNA is that it cannot introduce distortion. If the gains of the CG and CS stages are not equal, the LNA will cause distortion in the signal, so in the design of the special circuit, it is necessary to keep the gains equal but with phase opposition to obtain a differential signal. A differential signal is obtained by making the difference between two points of the circuit, in this circuit will be the two outputs, as one of the output is in phase opposition with the other, differential output is obtained. This is due to the fact that the gain of the CS stage is negative (signal inversion, phase with 180 degrees with respect to the input signal) and the gain of the CG stage is positive. Equations 4.4, 4.5a and 4.5b demonstrate this effect,

$$A_{V_{diferencial}} = A_{V_{CG}} - A_{V_{CS}} = |A_{V_{CG}}| - (-1)|A_{V_{CS}}| = A_{V_{CG}} + A_{V_{CS}} \tag{4.4}$$

$$A_{V+} = \frac{(gm_1 + gds_1)(gm_3 + gds_3)}{gds_5(gm_3 + gds_3) + gds_1(gds_5 + gds_3)} \tag{4.5a}$$

$$A_{V-} = -\frac{gm_2(gm_4 + gds_4)}{gds_6(gm_4 + gds_4) + gds_3(gds_6 + gds_4)} \tag{4.5b}$$

Input Impedance

$$Z_{in} = \frac{gds_5(gm_3 + gds_3) + gds_1(gds_5 + gds_3)}{gds_5(gm_1 + gds_1)(gm_3 + gds_3)} \tag{4.6}$$

Noise Figure

The implementation of the NF equation can be seen below. This equation does not take into account the flicker noise and noise from the filter. The $GS1$ is the admittance of the characteristic impedance ($\frac{1}{RS1}$) of the antenna ($RS1 = 50\Omega$ is the typical value).

The NF equation is the result of the contribution of every single noise source provenience from the resistors and the transistors in the output voltage of the circuit. For simplicity in expressing graphically the NF, only transistors thermal noise sources were taken into account. The following equations demonstrate the calculation of NF.

$$NF = 10log_{10}(F) \tag{4.7}$$

$$F = 1 + \frac{\overline{Vout_{noise}}^2}{\overline{Vout_{RS1noise}}^2} \tag{4.8}$$

$$\begin{aligned}\overline{Vout_{noise}}^2 = \quad & \overline{Vout_{noise,1}}^2 + \overline{Vout_{noise,2}}^2 + \\ & + \overline{Vout_{noise,3}}^2 + \overline{Vout_{noise,4}}^2 + \\ & + \overline{Vout_{noise,5}}^2 + \overline{Vout_{noise,6}}^2\end{aligned} \tag{4.9}$$

$$\begin{aligned}\overline{\boldsymbol{Vout_{noise,1}}}^2 &= \overline{I_{Termal,1}}^2 \times (gm3 + gds3)^2 \times \\ &\times \left(\frac{GS1\, temp_1 - gds5\, gm2\, (gm4 + gds4)}{temp_2\, temp_1} \right)^2\end{aligned} \tag{4.10}$$

$$\overline{\boldsymbol{Vout_{noise,2}}}^2 = \overline{I_{Termal,2}}^2 \times \left(\frac{gm4 + gds4}{temp_1} \right)^2 \tag{4.11}$$

$$\begin{aligned}\overline{\boldsymbol{Vout_{noise,3}}}^2 &= \overline{I_{Termal,3}}^2 \times gds1^2 \times \\ &\times \left(\frac{GS1\, temp_1 - gds5\, gm2\, (gm4 + gds4)}{temp_2\, temp_1} \right)^2\end{aligned} \tag{4.12}$$

$$\overline{\boldsymbol{Vout_{noise,4}}}^2 = \overline{I_{Termal,4}}^2 \times \left(\frac{gds2}{temp_1} \right)^2 \tag{4.13}$$

$$\begin{aligned}\overline{\boldsymbol{Vout_{noise,5}}}^2 &= \overline{I_{Termal,5}}^2 \times \\ &\times \left(\frac{temp_3}{temp_2} + \frac{gm2\, gds1\, gds3\, (gm4 + gds4)}{temp_1\, temp_2} \right)^2\end{aligned} \tag{4.14}$$

$$\overline{\boldsymbol{Vout_{noise,6}}}^2 = \overline{I_{Termal,6}}^2 \times \left(\frac{gm4 + gds4 + gds2}{temp_1} \right)^2 \tag{4.15}$$

$$\begin{aligned}\overline{\boldsymbol{Vout_{RS1noise}}}^2 &= \overline{I_{Termal,RS1}}^2 \times \\ &\times \left(\frac{temp_4}{temp_2} + \frac{gm2\, (gm4 + gds4)\, temp_5}{temp_1\, temp_2} \right)^2\end{aligned} \tag{4.16}$$

$$temp_1 = gds6\,(gm4 + gds4 + gds2) + gds2\,gds4 \tag{4.17a}$$
$$temp_2 = gds5\,temp_3 + gds1\,gds3\,GS1 \tag{4.17b}$$
$$temp_3 = temp_4 + GS1\,(gm3 + gds1 + gds3) \tag{4.17c}$$
$$temp_4 = (gm1 + gds1)\,(gm3 + gds3) \tag{4.17d}$$
$$temp_5 = gds5\,(gm3 + gds3 + gds1) + gds1\,gds3 \tag{4.17e}$$

Band Pass Filter Cutoff frequency(fc)

$$TF_{filter} = \frac{C_{Filter} \times s}{\frac{1}{R_{filter}} + C_{filter} \times s} \tag{4.18a}$$
$$f_{Cutoff} = \frac{1}{R_{fiter} \times C_{filter}} \times \frac{1}{2 \times \pi} \tag{4.18b}$$

4.3.3 Theoretical & Cadence Simulations

The theoretical data will be compared with two types of simulation data, one set of data is obtained from the normal Berkeley Short-channel IGFET Model (BSIM) model (used for low and medium frequencies) and the other will use an extended version of BSIM model, it will be obtained from an RF model (used for high frequencies). We will also show other way of analyzing the circuit, using the theoretical equations, by simulating the response of the circuit (equations that describe him) to the variations of is scaling parameters.

4.3.3.1 Circuit Theoretical Parametric Analysis

With the Figures 4.7, 4.8, 4.9, 4.12 and 4.10 we have a good way to understand the circuit operation and what to expect for given scaling. These figures were obtained for $L = Lmin$, this is the best design as we will be able to verified later in this document.

Gain Analysis

In order to size the single-ended gains, so as to be equal in amplitude, one must vary either the voltages *VDsat* of the transistors or the current that travels each stage. In the Figure 4.7, it is verified that with the increase of these tensions the gains of each floor decrease. As the intended gain is to have the best possible gain, ideally the *VDsat* should

be very small, but to keep the transistors in the conduction zone would require a very large value of W, which would increase the area of the circuit considerably and the voltage $VDsat$ cannot be very low because as it will be analyzed then the Zin would influence.

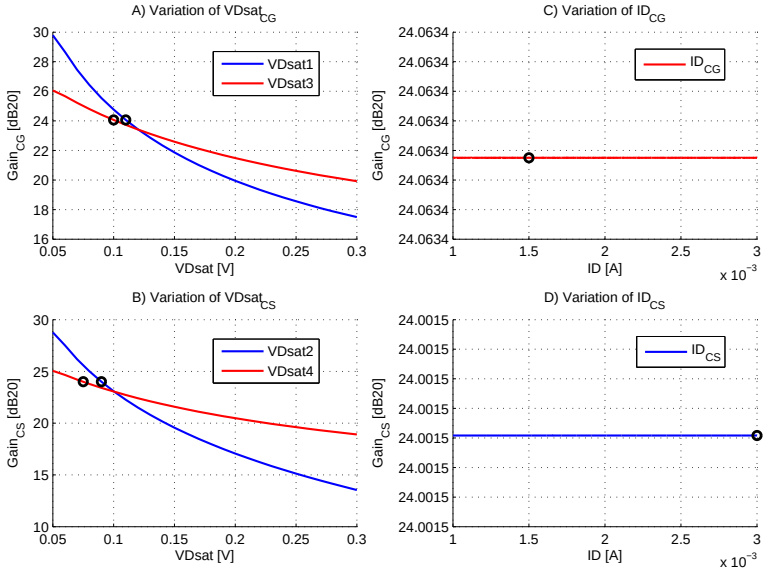


Figure 4.7: Theoretical parametric simulation of the single ended Gain equations for $Lmin$ sizing. Variation of $VDsat$ and ID from CG and CS.

It is possible to analyze that the CS stage requires smaller $VDsat$ to achieve an equal gain in amplitude to the CG stage, this phenomenon is due to the fact that transistor NM1 (figure 4.6) of the CG stage has the component gmb contributing to the increase of its gain, i.e. the voltage between the source terminal and the bulk terminal (Vsb) of the transistor which is equal to vin and the voltage between the gate terminal and the source terminal (Vgs) which is the negative signal causes the sum between the gm and the gmb, which does not happen in the transistor NM2 of the CS stage. The transistors that most influence the gain variation are NM1 for the CG floor gain and NM2 for the CS gain.

Figure 4.7 shows the response of the gain to the variation of the $VDsat$ and the CG and CS current. As mentioned in [6] both single ended CG and CS gains must be equal, analyzing Figure 4.7 is possible to find $VDsat$ values that validate $Av_{CG} = Av_{CS}$. It's interesting to see that varying the current the gain stays the same.

Using the simplified gain equation in [6] and the equations gm and gds in Appendix C, equations C.1a and C.2a, we obtained the equation 4.19 ,

$$Av = gm\frac{1}{gds} = \frac{2ID}{VDsat} \times \frac{\mathrm{Cte}L}{ID} = \frac{2 \times \mathrm{Cte}L}{VDsat}. \tag{4.19}$$

This means that the gain it isn't dependent of the current.

The variation of the current in the CG and CS stages does not have a significant influence on the gain variation. This happens because when the current varies the transistors

in the triode zone compensate for the variation of the transistors below in the cascade configuration, keeping the gain approximately constant, as can be Checked in Figure 4.7.

Since the gain of the circuit doesn't vary with the current of the CG and CS, it is only necessary to dimension the values of *VDsat*. The fact that the current produces no change in the gain, doesn't mean that it can be any value, as will be seen next, the Zin and the NF depend on the current variation.

Zin Analysis

For the LNA to have its input adapted this must be equal to the characteristic impedance of the antenna, because this block is the first of the Front End in the signal path, so the LNA is connected directly to the antenna. It is possible between the LNA and the antenna to be present a filter, this is to attenuate everything outside the band where the Front End will operate. In the analysis of the Zin, the effect of the RC filter isn't considered.

The CG stage is responsible for adapting the input impedance. With the variation of the *VDsat* of the transistor NM1 and NM3 and with the current passing through this stage it is possible to size the input impedance. This is only valid for the low frequency model, because at high frequencies the parasitic capacities of both the CG floor and the CS floor have implications for the LNA input impedance.

By varying the *VDsat* of the transistors NM1 and NM3 it's possible to increase or decrease as necessary the value ofZin of the LNA, as shown in the Figure 4.8. The transistors that most influence the increase in Zin is NM1.

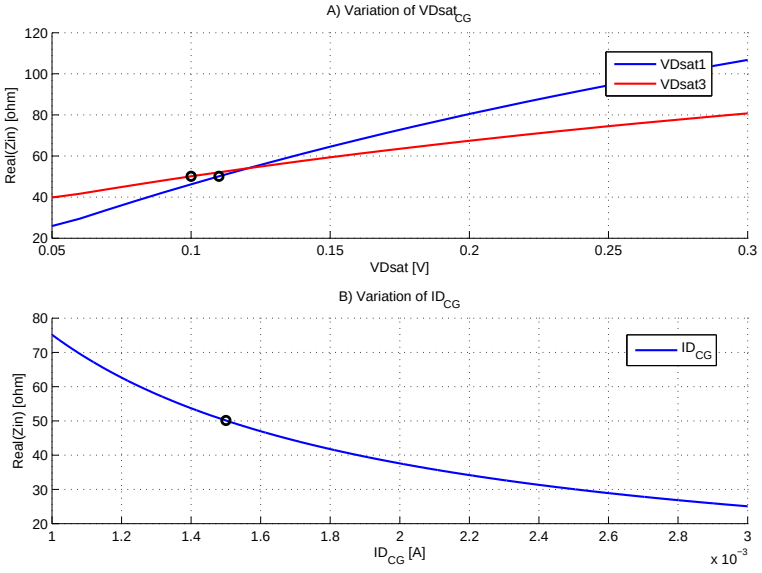


Figure 4.8: Theoretical parametric simulation of the Zin equation for *Lmin* sizing. Variation of $VDsat$ and ID from CG.

Figure 4.8 shows the response of the Zin to the variation of the *VDsat* and the CG current. In this figure the variation of the current exercises influence in the Zin. It's

possible use this figure for scaling the transistors to obtained a Zin equal to 50ω, in order to have a good adaptation in the input port of the LNA.

In the sizing of Zin it is necessary to take into account the effect that the *VDsat* of the transistors NM1 and NM3 provoke in the gain, whatever the value it must be equalized by the gain of the CS.

The current has the inverse effect on the Zin, as the current increases the impedance decreases. This variation can be seen in the Figure 4.8.

A tradeoff between the current and the *VDsat* voltages must be done because if the current is too high the circuit will waste more energy which can be problematic for mobile communication systems but if the current Is low, it is necessary to compensate with the increase of *VDsat*. The problem of having large *VDsat* means that the value of the gain will be lower which can mean an increase in the NF, as will be discussed below. Another problem in the OP of the circuit, with very large *VDsat*, is that in order to have the transistors in the active zone, in moderate or strong inversion, the voltage at the terminals of the drain and of the source (*Vds*) is greater than *VDsat*, which may not be enough voltage, collapsing the circuit.

NF Analysis

Figure 4.9 shows the response of the Zin to the variation of the *VDsat* and the CG and CS current. As is described in [6] for different relationship ($n > 1$) between the CG and CS current the NF decreases, this can be observed in the Figure 4.10 that demonstrate the NF for a relationship of $n = 1$ and $n = 2$ between CG and CS current and it's possible to see a decrease in the value of the NF.

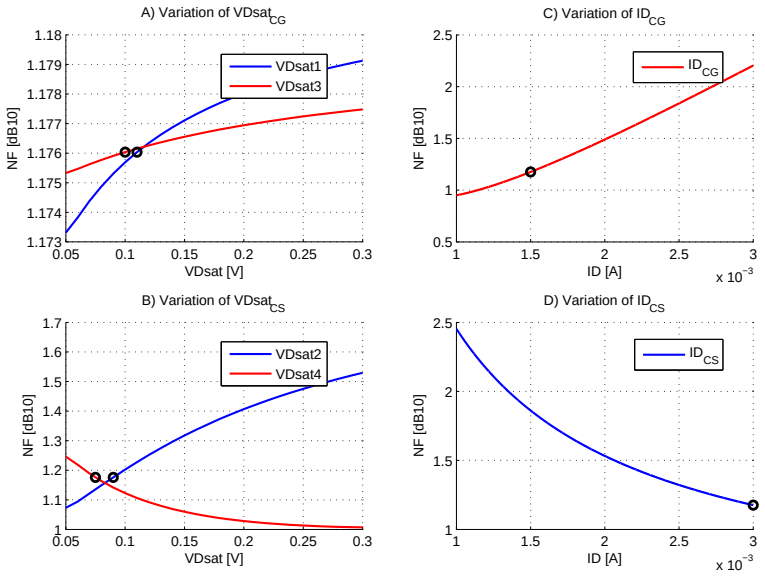


Figure 4.9: Theoretical parametric simulation of the NF equations for *Lmin* sizing. Variation of $VDsat$ and ID from CG and CS.

The lower the NF of a circuit, the smaller the noise introduced by him and the better the LNA is. The components of the circuit that introduce noise are the resistors and transistors. The transistors have associated more than one type of noise, the most important are thermal and flicker noise.

In the Figure 4.9 it will be seen that with the increase of the *VDsat* of the transistors NM1, NM2 and NM3 that the NF value increases but with the *VDsat* of the transistor NM4 is Possible to decrease the NF value. It is also verified that with the increase of the current of the CG, that the value of the NF increases, but with the increase of the current of the CS it is possible to decrease the value of the NF. This implies that if a current relationship used between the CG and the CS greater than 1 (e.g. 2, 3 or 4), as the gain and the Zin do not change with the current from the CS it is possible to have a greater current in the CS ($2\times I_{CG}$) to reduce NF. The CG stage for the same current as the CS stage has a smaller value in the NF, thus implying that the noise of the CG when propagating through the CS in the differential output is attenuated.

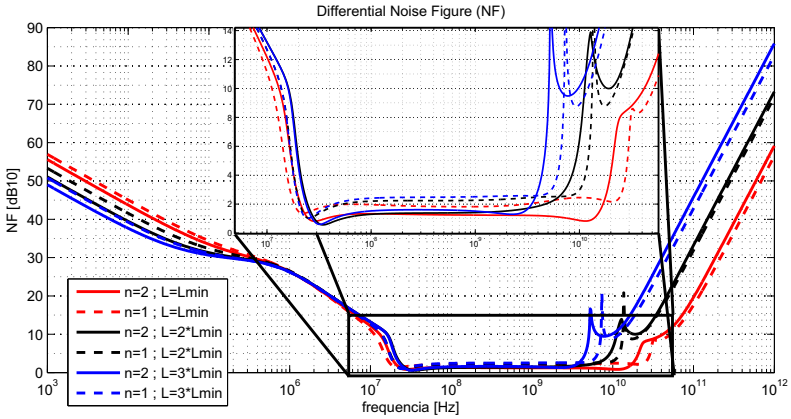


Figure 4.10: Theoretical parametric simulation of the current (relationship between the current of the CG and CS stage, $n = \frac{ID_{CS}}{ID_{CG}}$) influence in the NF equation for various sizing.

As can be seen in the Section 4.3.3.2 and reinforced with the Figure 4.11, the noise of the CG is attenuated by the CS stage (it has the smaller value/influence on the differential output), leaving to the CS, the greatest influence on NF.

It's possible to see in Figure 4.12 that the introduction of a high pass RC filter does not only eliminate the DC component imposed by theCG in theCS, but also, with a well-chosen cut-off frequency (CF capacitor and resistance RF sizing) the lower the NF will be, slightly increasing the operating threshold of the LNA at lower frequencies.

It's also possible to use the software to calculate various combinations of noise sources in order to understand with transistors or configurations introduce more noise. As we can see in Figure 4.11 that the CG configuration as a lower value of NF than the CS, thus proving what it's said in [6].

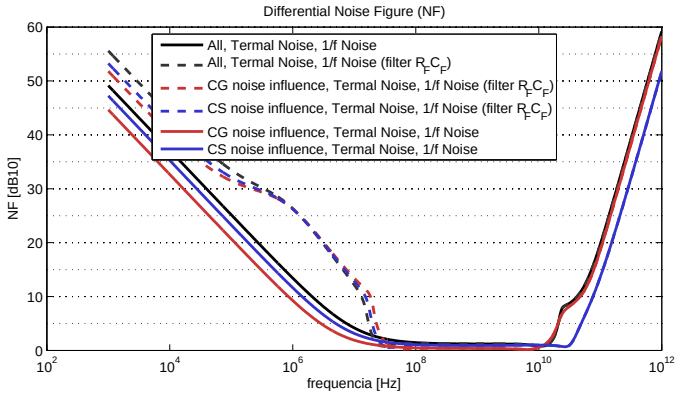


Figure 4.11: CG and CS influence in the NF for *Lmin* and $n = 2$ sizing.

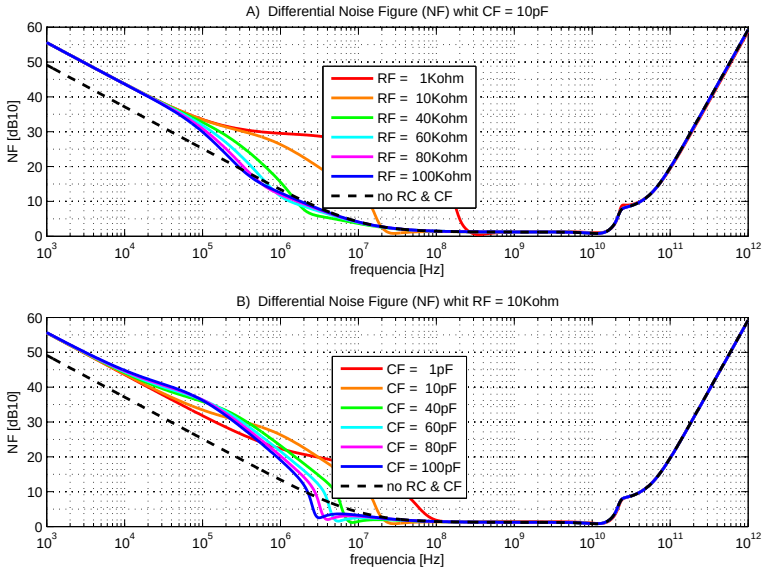


Figure 4.12: Theoretical parametric simulation of the filter influence in the NF equation for *Lmin* sizing.

4.3.3.2 Circuit Frequency Analysis

In this sub section is presented the simulations obtained from Cadence, Spectre(RF) simulator, with UMC CMOS 130nm BSIM models and the simulations of the equations obtained by the use of CAD software, in total there are four theoretical simulations, each represents a scaling of the circuit, and their respective Cadence simulations (BSIM model). A comparison between the equations extracted by the CADIT tool and the simulations made in Cadence simulator will be made, showing the error that they present between each other (Figures 4.13, 4.14 and 4.15).

The theoretical equations used were obtained with the models `md16` and `md17`. The `md17` is used in the NF, because the `md16` requires a lot of computational resources. Also, some parameters necessary for the theoretical equations were derived from the same BSIM models.

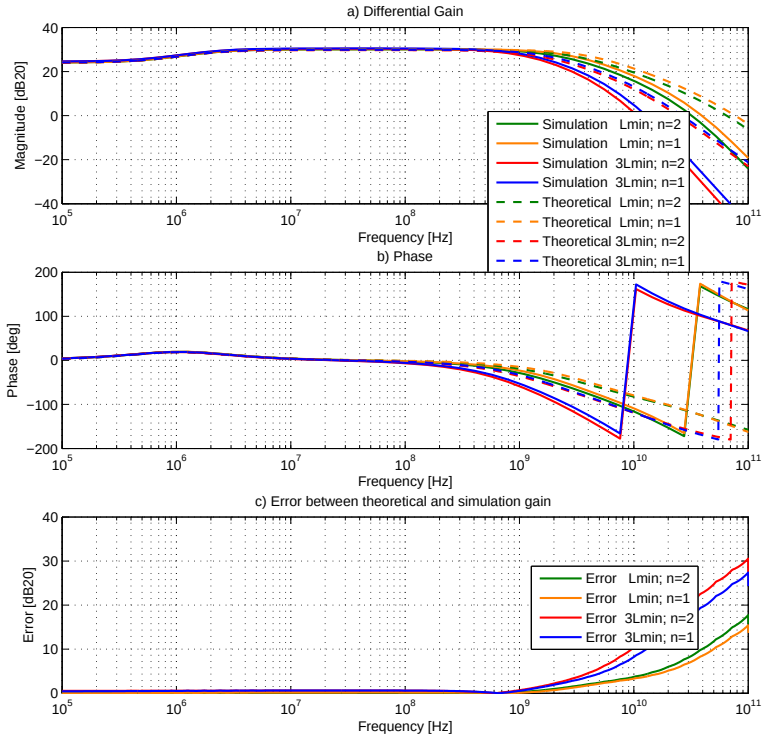


Figure 4.13: Theoretical and Cadence Gain simulations and the error between them for $Lmin$ and $3\,Lmin$ sizing

In Figures 4.13, 4.14 and 4.15 are represented the theoretical and Cadence simulations for sizing with $3\,Lmin$ and $Lmin$ and relations $n = 1$ and $n = 2$ between the CG and CS currents.

In these figures is expressed (TF, Zin and NF) the error that exists between the theoretical data obtained using the equations obtained by the tool and the simulations obtained using Cadence simulator. It is also possible to check (compare) the main parameters that define the transistor (gm, gds, W, ID e $VDsat$).

The equation used to calculate the error (Gain and NF differences) is as follows:

$$Erro = Teorico_{dB} - Simulation_{dB} \tag{4.20}$$

It can be seen in Figure 4.13 that the largest error is located at frequencies above $1\,GHz$, for any sizing of the elements in LNA. This occurs because the BSIM model used provides a more complete and accurate modeling of the parasitic effects that are noticeable at higher frequencies. In these Cadence simulations it appears that the gain tends to suffer a greater attenuation from the frequency of the dominant pole ($\approx 1\,GHz$).

The fact that the error of sizing with $Lmin$ to be shorter than the $3\,Lmin$, which is not expected (should be greater due to short channel effect) can have to do with adjusting the sizes of the transistors so that the Zin value is equal to $50 ohm$, to have a good adaptation

(it was considered the most important feature to be achieved in the design), coinciding the value of the simulated gain with the theoretical value. But is possible to see in the Tables 4.2 and 4.3 that the values of the transistors parameters has greater error in the case of sizing with Lmin.

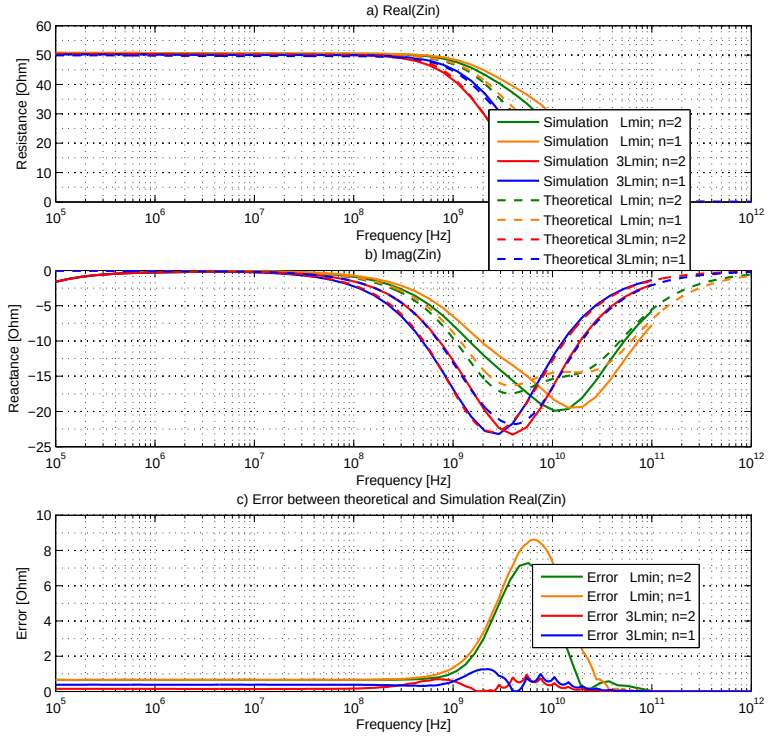


Figure 4.14: Theoretical and Cadence Zin simulations and the error between them for $Lmin$ and $3\,Lmin$ sizing

In Figure 4.14 is verified that noise of scaling transistors with $Lmin$ is greater for high frequencies ($\approx 1GHz$), since the sizing with $3\,Lmin$ remain reduced throughout the frequency spectrum. This is due to the fact that not only already explained above but also because the of the use of the minimum technology value of L, we have the presence of the short channel effect, which is not modeled with the equations present in the Appendix C. The Zin error here is calculated as follows:

$$Erro = Teorico_{linear} - Simulation_{linear} \tag{4.21}$$

Figure 4.15 demonstrates that for a sizing with current relationship between CS and CG larger than one ($n > 1$), which shows that the NF has is lowest values among the frequencies $100MHZ$ and $1GHZ$.

It can be seen that using minimal L it's possible to obtain a higher bandwidth in noise (up to $\approx 3GHz$) and also in gain and in Zin (up to $\approx 2GHz$) as shown in the Figures 4.13 and 4.14, because reducing the size of L results in faster transistors as shown in the following equation,

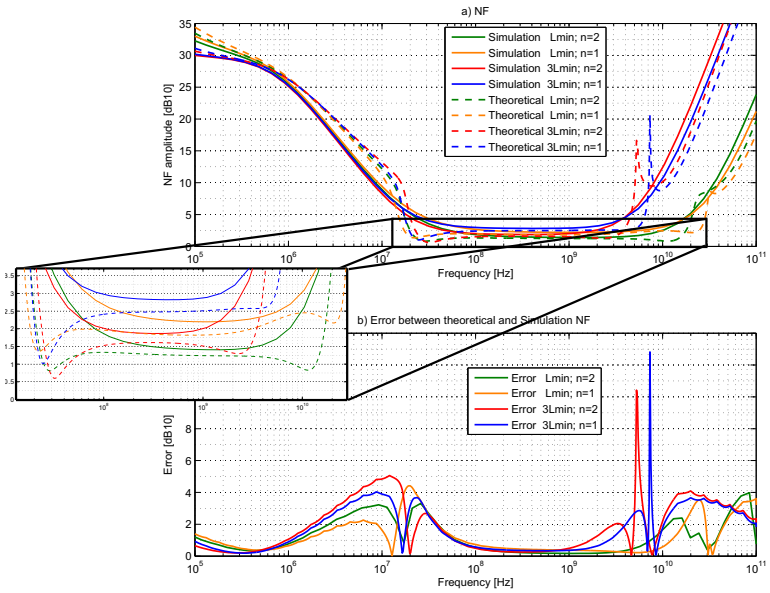


Figure 4.15: Theoretical and Cadence NF simulations and the error between them for $Lmin$ and $3\,Lmin$ sizing

$$f_T = \frac{gm}{2\,\pi\,C_g} = \frac{C_i\,V_{eff}}{C_g\,2\,\pi\,L} \tag{4.22}$$

Below $100MHz$ due to the modeling of flicker noise (difficult effect to model), this shows a high error, also above $2GHz$ for sizing with $Lmin$ and above $1GHz$ for sizing with $3\,Lmin$ the error is high. Note that the effect of the filter near $100MHz$ is not as pronounced as it was expected theoretically this can happen because once again the parasitic capacity and resistance have influence (parasitic resistances other than the $rds = \frac{1}{gds}$ are not being modulated). If the equations of these capacities are not well modeled and the effect of parasitic resistances are not considered, they can introduce a significant error in the filter effect as seen in figure 4.15. The effect of parasitic effects seems similar to the changing of the frequency of the pole shown in Figure 4.12.

Tables 4.2 and 4.3 present the values that characterize the transistors for sizing with $3\,Lmin$ and $Lmin$. It is noticeable that for L values close to minimum L that this difference increases, because the smaller the L, the more noticeable the effect of the short channel. Another effect is the field effect (GMB) where the bulk of the transistor is at a different potential from that of the source. Despite being considered in the equations, their modeling is very weak, the equation C.3 shows this modulation.

4.3.3.3 Simulation Data Obtained with RF Module

In this subsection, the simulations obtained by Cadence with the RF model and the errors with the respective theoretical values are presented.

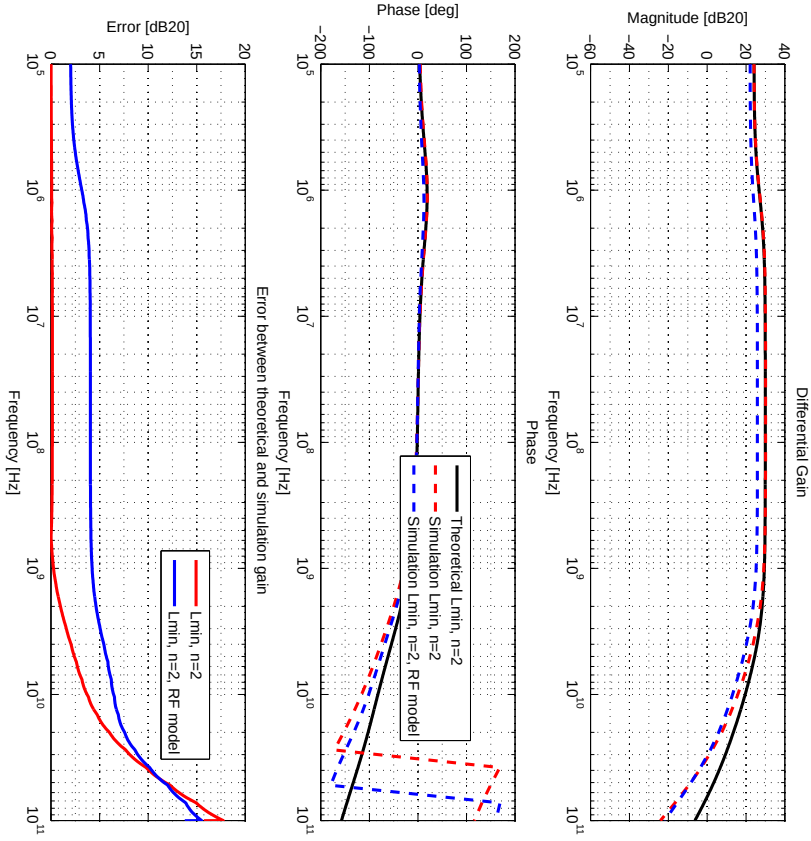


Figure 4.16: Theoretical and simulated with and without RF model Gain simulations for *Lmin* and $n = 2$ sizing

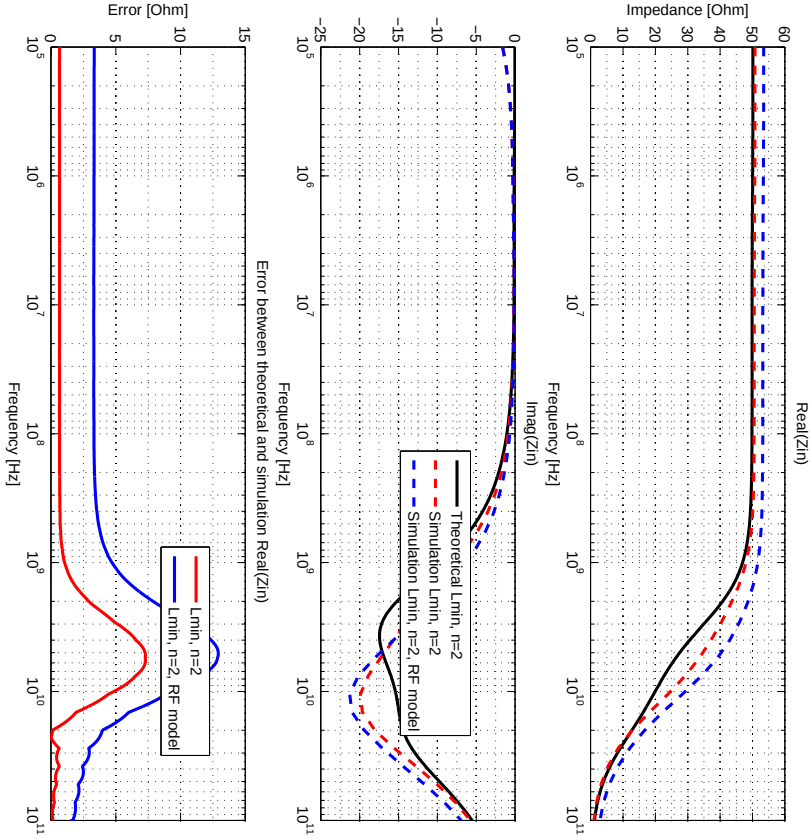


Figure 4.17: Theoretical and simulated with and without RF model Zin simulations for *Lmin* and $n = 2$ sizing

Table 4.2: Theoretical and Cadence transistor parameters for $3\,Lmin$ and $n = 2$

parameter	NM1	NM2	NM3	NM4	NM5	NM6
Theoretical						
gm $[mS]$	19,35	47,62	18,75	50	2,5	5
gds $[mS]$	2,02	4,05	2,02	4,05	1,25	2,5
W $[\mu m]$	89,91	272,11	84,38	300	15	30
ID $[mA]$	1,5	3	1,5	3	1,5	3
VDsat $[mV]$	155	126	160	120	900	900
Simulated						
gm $[mS]$	18,34	40,48	17,87	39,31	2,05	4,28
gds $[mS]$	0,81	0,93	1,02	3,17	1,18	2,18
W $[\mu m]$	120,7	272,01	117,7	300	20,9	41,8
ID $[mA]$	1,5	3,06	1,5	3,06	1,5	3,06
VDsat $[mV]$	137,39	126,55	141,55	130,66	859,19	859,73

Table 4.3: Theoretical and Simulated with and without RF model transistor parameters for $Lmin$ and $n = 2$

parameter	NM1	NM2	NM3	NM4	NM5	NM5
Theoretical						
gm $[mS]$	27,28	66,67	30	80	2,5	5
gds $[mS]$	6,07	12,14	6,07	12,14	1,25	2,5
W $[\mu m]$	59,5	177,78	72	256	5	10
ID $[mA]$	1,5	3	1,5	3	1,5	3
VDsat $[mV]$	110	90	100	75	900	900
Simulated						
gm $[mS]$	20,8	48,96	22,26	52,98	1,91	3,84
gds $[mS]$	2,24	3,8	2,49	5,97	1,24	2,5
W $[\mu m]$	59,5	177,76	72	256	7,2	14,4
ID $[mA]$	1,5	3,03	1,5	3,03	1,5	3,03
VDsat $[mV]$	97,96	81,17	92,99	78,07	754,16	756,92
Simulated RF model						
gm $[mS]$	18,44	35,8	20,1	38,65	1,83	2,36
gds $[mS]$	2,12	2,62	1,94	3,06	1,54	4,77
W* $[\mu m]$	59,52	177,92	72	256	7,2	14,4
ID $[mA]$	1,5	2,26	1,5	2,26	1.5	2,26
VDsat $[mV]$	118,06	92,25	109,32	82,78	721,12	711,38

In Figures 4.16, 4.17 and 4.18 it is possible to see the differences that the theoretical simulations have for sizing with $Lmin$ and ratio $n = 2$ have regarding the Cadence simulations(this is the best sizing obtained, it has smaller NF and greater bandwidth). It appears with the RF model that errors in TF and Zin are higher, already in NF this is approximate to the normal model error.

These increases in the error are due to the RF model adding to normal BSIM model,

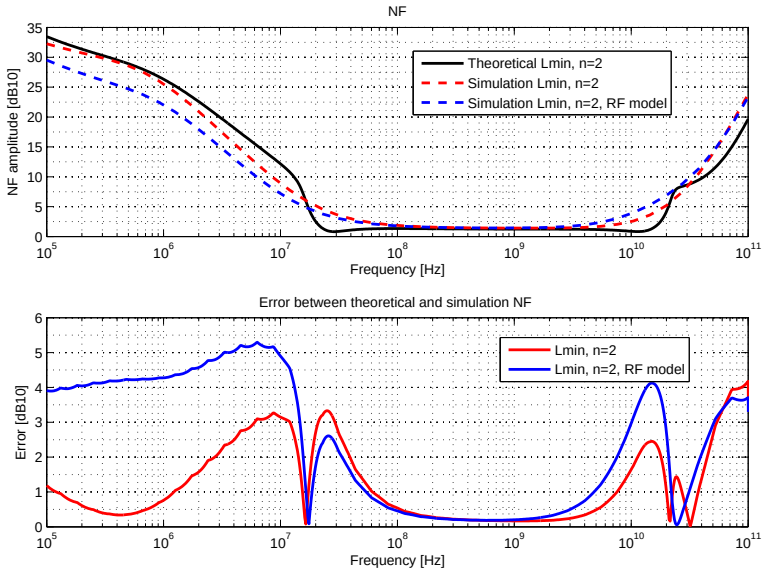


Figure 4.18: Theoretical and simulated with and without RF model NF simulations for $Lmin$ and $n = 2$ sizing

the effects of the wells that isolate the transistors, among others. These results introduce further parasitic capacity and resistances due to the junctions of the P-type or N-type barrier have whit the transistor, and also the diode effect that they introduce due to PN or NP junctions resulting from the binding of a P-type barrier with an N-type area.

In figure 4.16 the RF model has a generally gain reduction in amplitude resulting in increased error with the theoretical simulation, is also lower than the normal model.

In figure 4.17 the RF model also has an generally increase in Zin regarding to the theoretical and simulated values with normal model.

Using table 4.3 it's also possible to compare the theoretical parameters that characterize the transistors whit the simulation ones, whit and whit out RF model.

4.3.3.4 Simulation Data Obtained with RF Model in Weak Inversion

Figures 4.21, 4.20 and 4.19 demonstrated a theoretical analysis and its comparison with simulated data for circuit operating in weak inversion ($Vdd = 0.5V$). The transistors used in this simulation are special RF transistors with triple well. Table 4.4 presents the transistor DC operating point values used in the theoretical analysis.

Table 4.5 shows the bias voltage of each transistor. The table 4.6 shows the DC operating point values for the *Theoretical* and *Theoretical with DC simulation*. Table 4.7 presents the vales of the parameters: gm; gds; w; id; and $vdsat$; of each transistor: NM1; NM2; NM3; NM4; NM5; and NM6; for the curves previously described: *Theoretical*; *Theoretical with DC simulation*; and *Simulation*. Some sizing adjustments were made between the *Theoretical* and the *Simulation* results to achieve similar results. This is mainly due to the fact there were used the simplified version of the transistor model, `md13`.

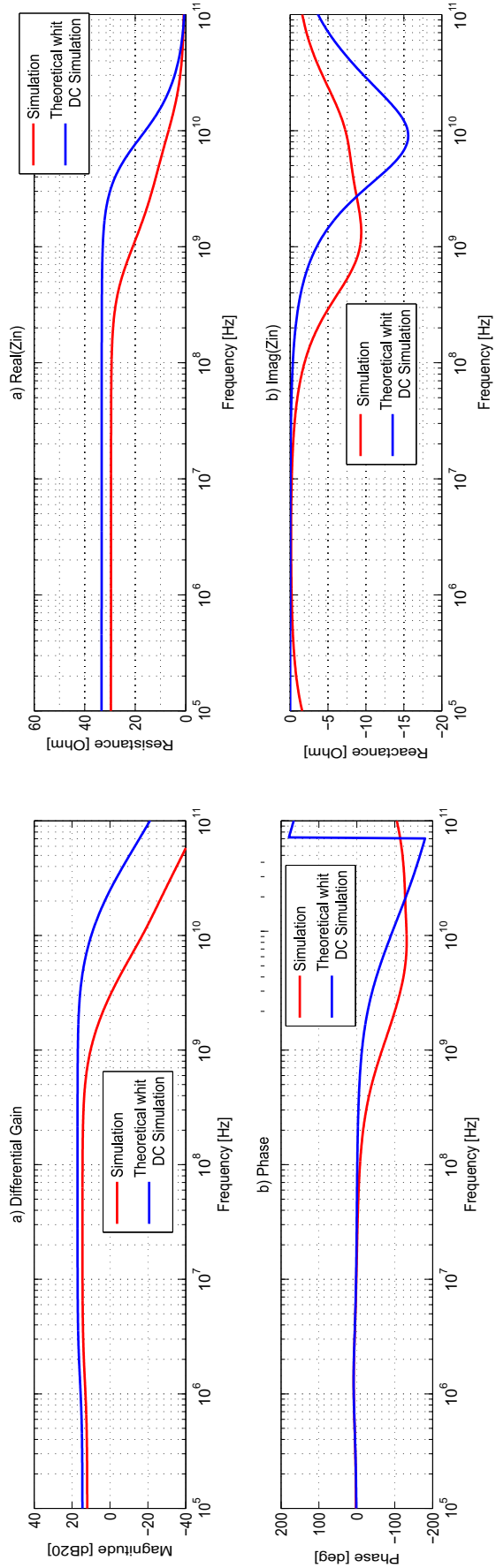


Figure 4.19: Comparing the theoretical data (with DC simulation parameters) and simulated TF, of the circuit presented in Figure 4.6, in Cadence software, for weak inversion. The TF represents the gain in the differential output.

Figure 4.20: Comparing the theoretical data (with DC simulation parameters) and simulated Zin, of the circuit presented in Figure 4.6, in Cadence software, for weak inversion.

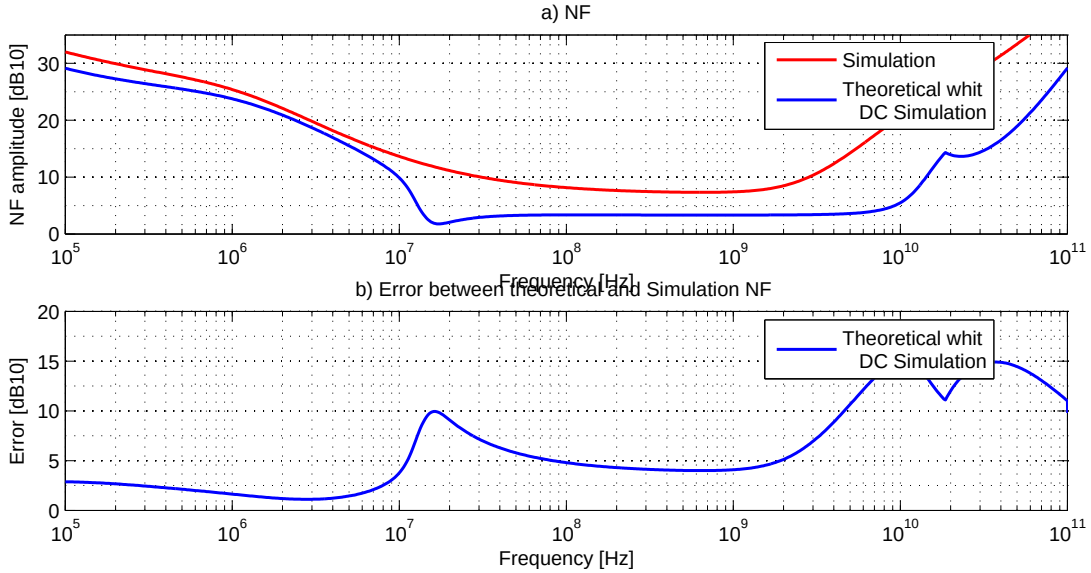


Figure 4.21: Comparing the theoretical data (whit DC simulation parameters) and simulated NF function, of the circuit presented in Figure 4.6, in Cadence software, for weak inversion. The NF represents the noise in the differential output.

Table 4.4: Simulated circuit and CMOS DC operating point for *Lmin* in weak inversion.

parameter	**NM1**	**NM2**	**NM3**	**NM4**	**PM5**	**PM6**
Vdsat	62.028m	75.673m	64.268m	60.211m	-196.846m	-191.737m
Ids	1.564m	1.083m	1.564m	1.083m	-1.564m	-1.083m
W	921.6u	194.6u	604.8u	604.8u	123u	123u
gds	11.346m	1.678m	2.977m	1.861m	5.631m	9.617m
gm	31.165m	19.791m	31.515m	22.815m	13.155m	7.974m
gmb	1.777m	805.934u	1.991m	1.489m	2.262m	1.39m
Cdb	1.32f	380.155a	1.1f	845.493a	3.487f	3.958f
Cgs	329.972f	85.281f	226.432f	212.748f	80.121f	78.098f
Csb	1.826f	562.801a	1.621f	1.253f	4.95f	5.099f
Cgd	232.816f	47.832f	150.295f	149.688f	17.686f	20.904f

It is possible to infer in this example that for higher frequency the small signal model used in the CADIT tool, do not modulate properly the effects of a RF transistor. Moreover, it is clear that in the frequency range of the LNA operation it presents a significant difference compared to simulation data. Therefore, one can conclude that a more precise model should be used, with RF characteristics, as described in [22] and [1].

Table 4.5: Transistors theoretical and Cadence simulated bias voltages

Vbias $[mV]$	**Theoretical**	**Theoretical DC Simulated**	**Simulated**
NM1	670	608,26	630
NM2	470	426,55	413
NM3 & NM4	880	872,62	860

Table 4.6: Transistors theoretical and Cadence simulated DC node voltages

parameter	NM1	NM2	NM3	NM4	NM5	NM6
Theoretical						
Vds $[mV]$	200	300	200	300	600	600
Vbs $[mV]$	200	0	300	400	0	0
Vdb $[mV]$	300	300	600	600	600	600
gm/gmb	0,15	0	0,15	0,15	0	0
Simulated						
Vds $[mV]$	224,8	415,23	209,91	178,68	604,11	606,1
Vbs $[mV]$	161,184	0	385,98	415,23	0	0
Vdb $[mV]$	385,98	415,23	595,9	593,9	604,11	606,1
gmb/gm	0,08	0	0,07	0.07	0	0

Table 4.7: Theoretical and simulated transistor parameters for *Lmin*

parameter	NM1	NM2	NM3	NM4	NM5	NM6
Theoretical						
gm $[mS]$	27,28	66,67	30	80	2,5	5
gds $[mS]$	6,07	12,14	6,07	12,14	1,25	2,5
W $[\mu m]$	59,5	177,78	72	256	5	10
ID $[mA]$	1,5	3	1,5	3	1,5	3
VDsat $[mV]$	110	90	100	75	900	900
Theoretical whit simulated DC voltages						
gm $[mS]$	30,62	74,72	32,26	77,58	3,32	6,67
gds $[mS]$	6,07	12,25	6,07	12,25	0,82	1,66
W* $[\mu m]$	75,03	220.65	83,26	238,5	6,59	13,21
ID $[mA]$	1,5	3,03	1,5	3,03	1.5	3,03
VDsat $[mV]$	97,96	81,17	93	78,07	754.16	756,92
Simulated						
gm $[mS]$	20,8	48,96	22,26	52,98	1,91	3,84
gds $[mS]$	2,24	3,8	2,49	5,97	1,24	2,5
W $[\mu m]$	59,5	177,76	72	256	7,2	14,4
ID $[mA]$	1,5	3,03	1,5	3,03	1,5	3,03
VDsat $[mV]$	97,96	81,17	92,99	78,07	754,16	756,92

4.4 Conclusion

The use of computational tools provides a more detailed analysis of the behavior of the different characteristics of a circuit. It is advantageous to analyze its performance in frequency, where it is possible to infer the operating zones and their possible characteristics of the circuit in this zone, such as NF, gain and Zin, among many others.

Chapter 5

System Design of an IoT Sensor Node

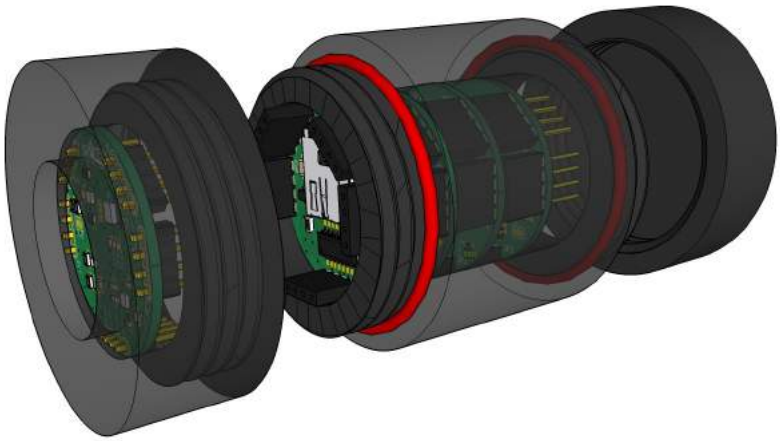


Figure 5.1: Final expected result, the system is incorporated in a cylindrical container with a small opening for the sensors.

5.1 Introduction

In this chapter a new approach is given to the implementation of multi-sensor node. The node system is to be implemented in the IoT world and needs to be able to measure data, process them and transmit them, also maintaining the possibility of the system being used in several applications, originating the need for re-configurability. The concept and prototype behind the rolling probe was used to compete in an international competition called ICAN and the competition consisted of a presentation and a live demo. In recognition for the merit of the work done in the rolling probe project, it was awarded to it the second place in the ICAN competition (certificate of second place presented in Figure B.15 in Appendix B). Present in Appendix B it's possible to see the presentation done in

the competition, the certificate, the prize given to the development team and also the live demo for the jury of the competition to evaluate.

The chapter will be divided in tow section. the first will demonstrate the system design and the in the second the demonstration for the competition will be described.

5.2 Rolling Probe

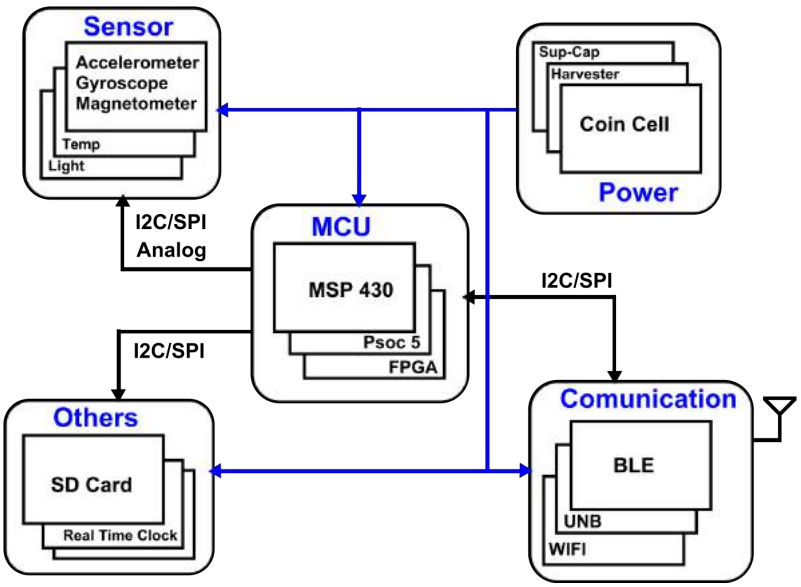


Figure 5.2: Rolling Probe structure.

In order to maintain the possibility of reconfigurability, the system will be designed so that parts of its hardware can be quickly replaced by different circuits, or simply add more circuits to the existing ones in order to increase the functionality of the system. This gives rise to the possibility that certain blocks may be be replaced with better performance versions, without having to redo the entire implementation of the system. Some of the blocks may even be designed in such a way that they contain some reconfigurability. For example, by using a programmable SoC (PSOC 5 from cypress) that has the ability to internally multiplex all its pins, he has now the possibility to read multiple different sensor. The architecture present in the figure 5.2 allows the possibility to increase and decrease the number of blocks depending on the needs of the application where the system will be used.

The system will be implemented using discrete components. Also, it comprises two processing units, both capable of processing, analog signals (PSOC5 and MSP430), two communication units, via wireless data transfer (BLE and UNB), a data storage unit using an SD card, a power unit, and finally a multi-sensor unit, where a light sensor, a temperature sensor, a gyroscope, accelerometer and magnetometer are present. The expected physical implementation of the different blocks can be seen in figure 5.3.

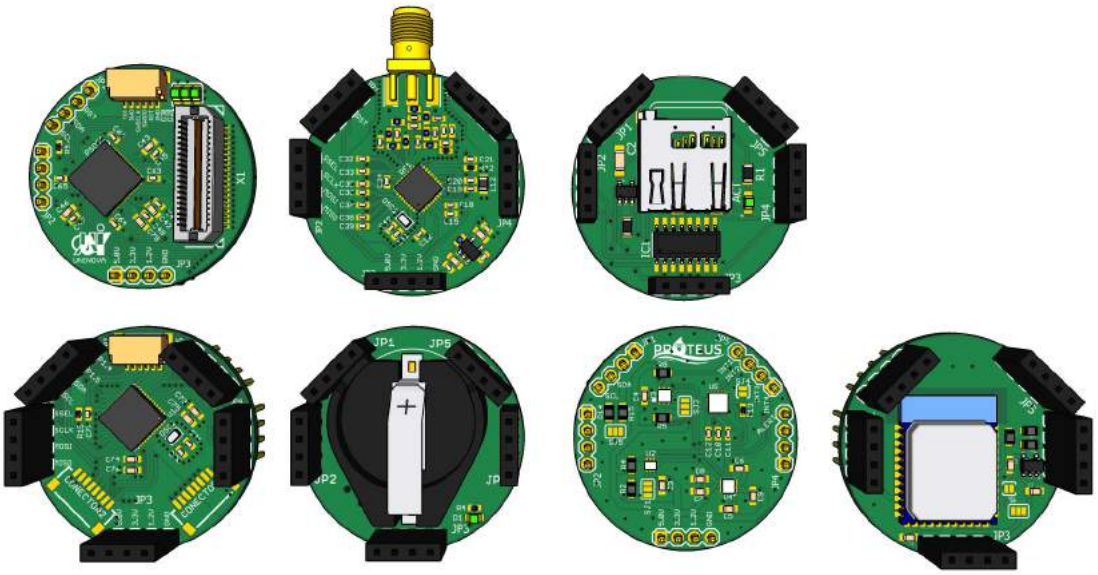


Figure 5.3: ICAN prototype boards, expected result.

The idea is to physically implement each block on a different board and through a bus of connectors make all the necessary interconnections, for communications between blocks. It is possible to replace several blocks, the communication bus between them has to be defined generically so that all the blocks can communicate without interfering with each other.

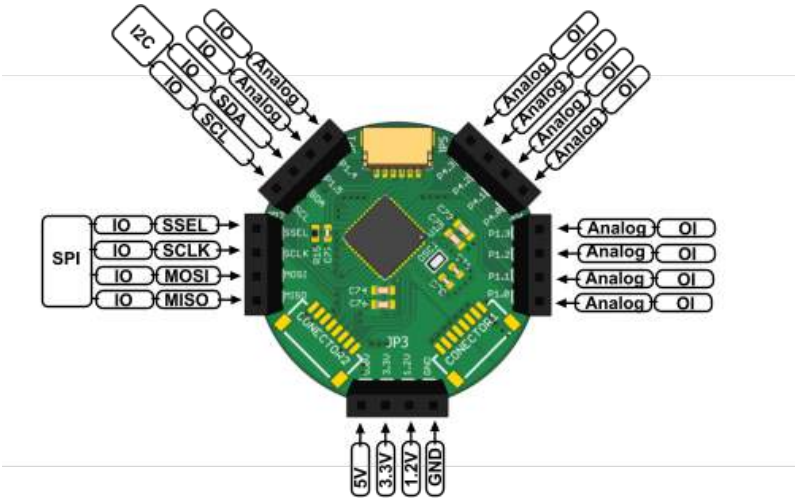


Figure 5.4: Rolling probe defined connections between boards (pin functionality).

The signals for all pins in the communications are defined according to the MSP430 controller, making this block the main one. Figure 5.4 demonstrates the type of connections between boards and its pin functionality.

All the other board need to use the configuration present in Figure 5.4. However, this

is the possibility that two board need to use the same pins. This can happen for example, when two systems need to use the UART pins, but only one UART communication interface is available. In case of conflicts between tow modules there are two options:

- redesign that part of the system, for one of the blocks;
- only one can be used at a time.

The use of UART communication is discouraging, best solution to transfer data is using I2C interface since this type of communication allows for multiple ICs to communicate using the same interface.

Another communication is the SPI bus, it's also a master slave configuration, the only difference in the SPI is that, to use it for more than one slave it requires that the amount of enable pins to be equal to the number of slaves, to prevent data collision. In the I2C this does not happen because the I2C protocol uses addresses to define each slave you want to talk to.

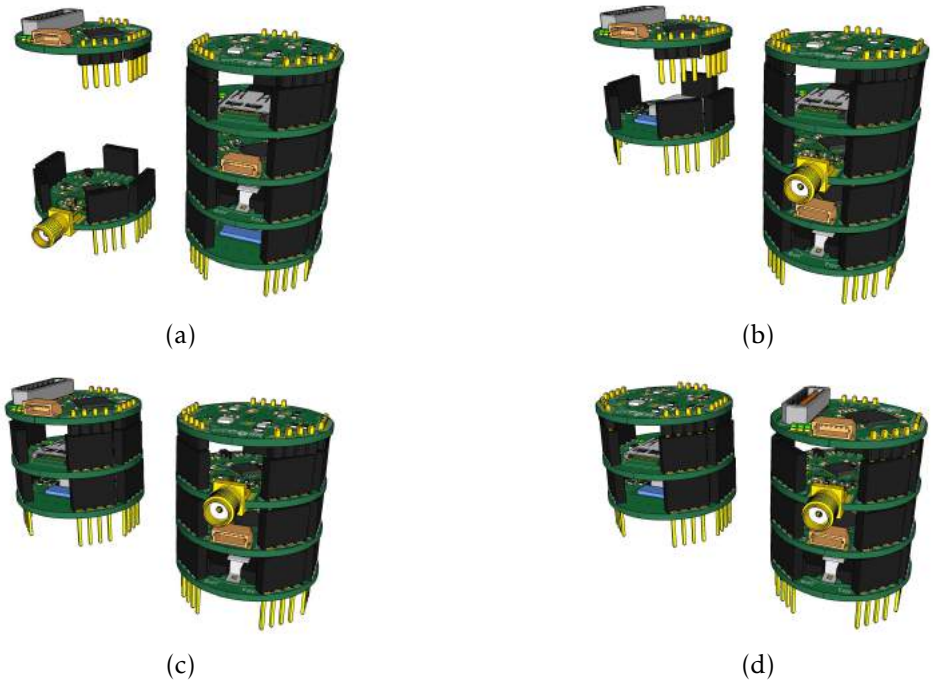


Figure 5.5: Theoretical implementation (expected final result) of the complete system, ICAN Node Sensor, PCB's stack version $1V$. It's presented four types of configurations.

The Figure 5.5 demonstrates the idea behind the new method of implementing the system, where a modular approach is used. It's possible to see several possible node configurations. This idea allows for the removal of hardware that is not necessary for the application, where the system is applied. Different combinations can produce better efficiency in power.

The boards are connected through a pin connector, resulting in flexible stack structure. The round appearance of the boards, is due to the physical restrictions of the node sensor

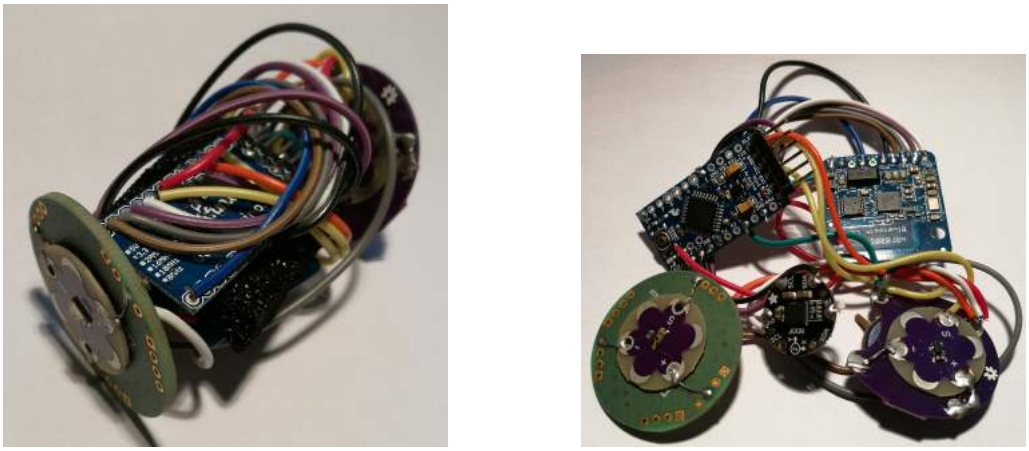
housing. For this purpose, it was attempted to maintain the same requirement, resulting in a round plate, to be introduced in a round capsule. In attachment B it is possible to see the final format of the set of plates that constitute the system and its encapsulation.

5.3 Node Sensors Test Results

In order to be able to enter into the competitions, another simpler prototype was made, with boards already commercially available and made by different companies, like Adafruit and Sparkfun, among others. The system will keep the same approach by using the same blocks presented in Figure 5.3, but implemented with different components. The Figure 5.6 demonstrates the assembling of the first version of the system.

The first prototype consists of the following components:

- Arduino Pro Mini 328 - 3.3V/8MHz.
- Bluefruit LE - Bluetooth Low Energy (BLE 4.0) - nRF8001 Breakout - v1.0.
- FLORA 9-DOF Accelerometer/Gyroscope/Magnetometer - LSM9DS0 - v1.0.
- LilyPad Coin Cell Battery Holder - Switched - 20mm.
- LilyPad Temperature Sensor.
- LilyPad Light Sensor.



(a) (b)

Figure 5.6: Rolling probe first version prototype assembly.

For implementing the processing unit it's used the Arduino pro mini. This module will be responsible for acquiring the data from the sensors and transmit it through BLE communication module, using the nRF8001 breakout board. The communication between the transmitter and the processor is done using an SPI interface. In order for Arduino pro mini to be able to gather the data from the sensor it used the I2C interface

for the LSM9DS0 board, and an analog interface for the light and temperature sensor. The only thing left is to power the prototype. This is done by using a simple coin cell direct connected to the power rail for all the boards.

For the live presentation in ICAN booth and for test purposes, a simple test setup was used, consisting of a tube with several magnets along its length, there will be parts where there will be no light (it will be of very reduced values), will be done through a coating on the tube with adhesive tape and finally at the end of the tube will be present a lamp which will be used to raise the temperature at that place. The Figure 5.7 demonstrates the configuration of the setup for testing.

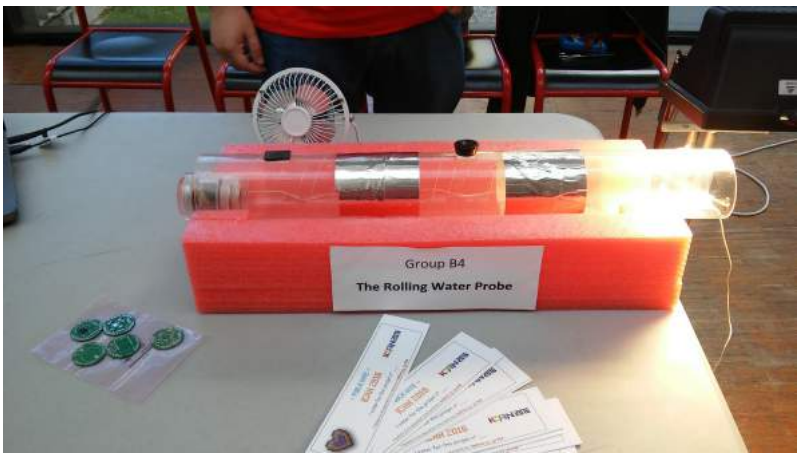


Figure 5.7: Test setup for the rolling air probe.

Figure 5.8: Data gathering, from the capsule into a computer, displayed in a graphical interface.

The test its done by pulling the system capsule to the acrylic pipe and display the sensor data in the graphical interface. During the capsule movement, through the magnets and the low light zones, variations in the levels of the values of each respective sensor are verified. At the end of the of its displacement by turning on the light, the heat that lamp transmits will be caught by the temperature sensor. This sensor value (also found in

the graphical interface) will enter the prototype gets closer to the heat source. Image 5.8 show the graphical interface displaying the data obtained from the sensors as it passes through the pipe.

The objective of this setup is to simulate a possible real application for the rolling probe system, being this one the air conditioning conduct monitoring probe. Were the capsule would be used to send the temperature of the air and if there are any existing breaches along the air conduits that could provoke air leakage resulting in a loss of efficiency. For this purpose, the most important sensors are the light sensor used to detect cracks in the pipes, this result in a small amount of light entering the pipe and the magnetometer to detect its position along the path.

In recognition for the merit of the work done in the rolling probe, it was awarded to it the second place in the ICAN competition (certificate of second place presented in image B.15 in attachment B). Present in attachment B it's possible to see the presentation done in the competition, the certificate and prize given to the development team and also the live demo setup for the jury to evaluate.

5.4 Conclusion

By using a modular approach, we gain the ability to change easily the circuits that are no longer necessary. We also gain the advantage that the system is very adaptable to a wide range of application.

Chapter 6

Conclusions

The purpose for this thesis is to implement ideas and validate them, so that later on they can be integrated in integrated circuits, were there designed can be done with the assistance of CAD tools like the one developed also here (CADIT).

Two research areas were covered in the design of systems for IoT. The first area is related to the design off the power module of a given system, by its self and in the scope of this thesis, this module is the whole system that later on can be integrated with other system. The second area covers the ability of a system to adapt to various applications.

Techniques were also studied to implement tools in the domain of CAD, so that it is possible to integrate in integrated circuits some of the characteristics of the systems developed here.

With the results obtained from the work developed and tested in this thesis, it is verified that the design of an IoT system, not as simple as it seems, presents a challenge in reconciling issues of energy efficiency and adaptability to diverse environments. It is also important the use of CAD tools, they present the possibility of accelerating the design and implementation of circuits.

Power Management

In the development of the prototype for the Power Management system, one restriction had to be defined at the start. The footprint of the components must be solder by hand, this means that at the beginning the choice of components has been limited. This is due to the fact that using components with very small footprints implies the use of specialized equipment, which presents a very high cost. Soldering the components by hand lowers the cost but also lowers the success rate of the board. during the assembly process of the board some components had to be replaced due to unexpected operations

resulting from the possibility of having burned during the welding process.

The power management system did have some unexpected results, does are mainly concern when the board is power off. the system enters in an uncontrolled state. These results are due to the fact that some of the load switch chosen for the power MUX, require to be always power on wen they have energy in the input, and start to leaking that energy into the main power rail that is used to receive energy form the harvester, this presents a problem because the harvester its complete exposed to a reverse current. So not all load switches can be used in this system, there is also some other functionality that so load switches have that can't be used like quick output discharge.

All the main ideas implemented did help in understanding and improve the power management capabilities of the prototype.

The use of super capacitors allows to increase the energy storage capacity, it also gives the possibility to use a small power source (small current) to supply power to a high current consumption circuit, for a limited time period, it is possible to storage in the super-capacitors significant amounts of energy to supply power to maintain circuits working. Meaning that, in a sensor node, if the system requires to use a high current functionality, it can through the super-capacitor storage energy. And after the operation is done, it just stores enough energy, to make another high current operation.

Unfortunately, the use of super capacitors, has a high waste of energy compared to both the battery due to its self-discharge is significant, requiring always maintain the capacitor charging when not in use.

the fact that there is an amount of energy that is not used in the capacitor, due to the minimum input voltage of the converters, requires that it never discharge beyond this value, otherwise it is necessary to always charge the capacitor with energy that does not will be used, thus further increasing the waste of energy. If the capacitor is maintained with energy above this amount, the wasteful misuse of energy only occurs at the beginning when the system is turned on for the first time or when it has been too long without power to charge the capacitors.

The application of a power MUX to make distribution of energy allows to reduce the consumption of the circuits that are not being used, causing that the energy of the super-capacitor is saved. The fact that you can also choose the type of power source allows you to choose which is the most efficient to keep the circuit running. However, when using load switch, they present a voltage drop in their terminals, which will further reduce the useful power of the super capacitor, because of the converters minimum levels for operation. The use of MUX allows to extend the number of capacitors used, thus allowing not only to store more energy, but also to extend the operation time of the outputs. By allowing each output to be individually controlled, it implies that it is possible to keep a super capacitor supplying energy while others are harnessing the harvester's energy (they are being charged).

The use of DC/DC converters allows a greater range of capacitor energy to be used, keeping the output voltage stable, otherwise this would not happen, because the capacitor

voltage as it decreases with the discharge would go from the required voltage value to the circuit, stop being able to keep this above that level.

By using a constant current charger, we obtained a more rapid charging period, since the current does not decrease with the increase of voltage, as would be expected in a RC circuit. The fact that we can control the discharge allows for choosing wen to storage energy, because not always will be possible, due to the limitations of the harvester, to have energy available for that purpose, thus, protecting the harvester, and keeping the critical blocs like the controller in continuous operations.

With the implementation of a digital controller like the MSP430 we have the ability to implement smart algorithms to efficiently control the power distribution, and consumption. The MSP430 is also low power, it decreases the consumption of the board allowing for more power to be used to charge the super-capacitors and other subsystems. A good aspect to choose the micro-controller, to serve the brains of the board is the fact that it has the ability to enter in low power modes to save power wen it's not necessary to do any action. Also, the use of interrupts is a good way of programming because controller wen waiting for something to happen can be put in one of the low power modes, until the interrupts are triggered. Without the use of the interrupts the CPU needs to constantly check for all the actions, meaning that the CPU is always active and consuming power.

CADIT Tool

The implementation of the tool developed here, trough the work done in this thesis, is integrated in the initial steps for the automation of the design process of a integrated circuits.

The tool with the use of the OpenAccess database allows easy integration with tools like Cadence. Interoperability between tools is easily achievable because both interpret the data in the same way. Is also a good way to store circuit data, allowing for quick and simple access. It is not necessary to be processing text files such as NetList, all these links are already configured in the database.

However, it has the disadvantage of not being able to calculate the OP of a non-linear circuit (circuit with active components as transistors), thus limiting its performance, but using the small signal model it is possible to use the algorithms to calculate the equations of nodes. However, it is necessary to model the parameters of the small signal models using a OP assumed or obtained by simulator, external to the tool.

With the increase of the complexity of the small signal models, increases the requirements of quantity of memory for the calculation of the simulated equations. However, this calculation is only necessary once, as long as the circuit remains unchanged at the net list level.

The Matlab engine although to be a tool easily integrate in CADIT, presents memory problems for complex circuits, in the tests made with LNA for the most complete small-sized model, Matlab is no longer able to calculate the symbolic equations, it is necessary

to circuits use less accurate models.

By using the symbolic equations provided by CADIT it is possible to understand the effect that some parameters of the transistors have on them. This allows for a rapid understanding of the starting point of the system, and by applying this starting point in a simulator and knowing the effect of the parameters variations, it possible to now the necessary modifications to the starting point on the simulator, in order to obtain a good size capable of validating all restrictions imposed.

Node Sensor

The use of re-configurability on the analog front end of the node sensor allows for multiples sensors integration. meaning that the system can be used for multiple applications, without the necessary to redesign the node sensor, reducing manufacture costs. Having the control to configure the signal processing path, allows for better measurements, the analog circuits are configured to better fit the needs of the sensor signals. Since many of the analog signals require polarization, a good way to keep re-configurability is to have the possibility to control the polarization value. By using a current DAC for the polarization, the range of the signal can be changed to better fit the restrictions of analog circuits.

In order for the system to be independent, some power management capability it must have. It is also important to reinforce its independence, the capability to generate its own power through the use on energy harvesting. This allow for longer periods of operation hideout the intervention of a third party.

By designed the system through a modular approach, it's possible to increase the re-configurability of the system by being possible to switch different parts of the hardware to better fit an application. What this means, is that by dividing the system hardware in different platforms and connected in a stack configuration, it's possible to switch some circuits that are not needed for other that better fit the application. For different applications is only needed to design the hardware that is specific to that application, the rest of the system remains the same.

6.1 Future Work

All the work developed here leads to a possible integration of multiple systems in a single chip (platform) for that purpose and the fact that the work done here were the initial steps, there is still the necessity to continue working in the subject of this dissertation in order to make a complete system in integrated circuits to be applied in the field as a multi-re-configurable node sensor withe power management and optimization capabilities.

6.1.1 Power Management

In the intuit to increase the optimization of power management board, producing better control algorithms, the following ideas could be applied and analyzed:

- Use smaller discrete components in order to reduce the area of the PCB. examples of footprints can be Ball Grid Array (BGA), Quad Flat No leads (QFN), etc..
- Change the load switch. use switch with the capability of not requiring polarization pins and reverse current protection. Also, the switch must have the lowest resistance possible and minimum input voltage.
- Measure the input current of the converters to know the actual current consumed by the them. This current is the one actually being supplied by the capacitor. Also measure the output voltage to check if the drive has failed to operate properly. This maximizes the output current for an input voltage. By measuring these two signals, it is possible to characterize all the operating zones of the converter.
- Introducing more configurability in the chargers, by implementing switches to configure the current value, you can optimize the current needed to charge the capacitors, thus allowing a faster load. The current value is set according to the availability of the harvester.
- Increase the number of capacitors and the value of their capacity, allowing more energy to be stored, further lengthening the periods of operation of the outputs.
- Try different control algorithms. Possibility of implementing a genetic algorithm to find the best MUX settings (the best link between super-capacitors and outputs).
- Measure the outputs of the switch to optimize the time it is switched on when exchanging power sources for an output.

6.1.2 Node Sensor and Rolling probe

For increasing the capability of the node sensor some improvements need to be design and tested:

- Increase the power management of the board, by using switch to disconnected parts of the board.
- Increase the analog front-end capability. Switching the PSOC 4 to the PSOC 5 and also adding a FPAA, like the Anadigm chip, could increase the capability of handling analog signals.
- Increase the digital processing capability. This can be done with better micro controller or with adding a FPGA, for hardware specific controllers like state machines.

- Use more types of communications like Wifi, Lora, etc.

In the new modular approach for the node sensor some improvements can also be made:

- Test the whole set.
- Reduce gap between levels.
- Increasing pin capability for signal transfer.
- Implement more types of sensors.
- Use more types of communications, Wifi, Lora, etc.
- Increase the processing capacity, through different micro-controllers or with the use of a FPGA.

6.1.3 CADIT

In order to achieve a complete tool to help in the design of integrated circuits some ideas for improvements could be applied:

- remove the Matlab engine and implement the MSAAC toll in c ++ code. implement libraries for symbolic calculation processing in c ++.
- Integrating a simulator with the CADIT tool, thus allowing the integration of the OP calculation, or even making the complete simulation automatically, without having to configure anything. A possible simulator to be integrated could be the NGSIPCE.
- Automate the process of design of integrated circuits, in which the optimization of the sizing could be done through genetic algorithms.
- Using better models of the components for the calculation of equations
- Expand the tool to be possible to employ it to other types of circuits as mixers.

Bibliography

[1] E. Abou-Allam and T. Manku. "A small-signal MOSFET model for radio frequency IC applications." In: *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 16.5 (1997), pp. 437–447. ISSN: 0278-0070. DOI: 10.1109/43.631207.

[2] *AdaPtive micROfluuidic- and nano-enabled smart systms for waTEr qUality Sensing*. Document of Work (DoW) at E.C. EH2020. PROTEUS, 2015.

[3] J. P. Alarcão, L. B. Oliveira, J. P. Oliveira, and R. Santos-Tavares. "Analysis of a noise canceling LNA using a Si2 OpenAccess based tool - CADIT." In: *2015 22nd International Conference Mixed Design of Integrated Circuits Systems (MIXDES)*. 2015, pp. 464–469. DOI: 10.1109/MIXDES.2015.7208564.

[4] M. H. Asghar, A. Negi, and N. Mohammadzadeh. "Principle application and vision in Internet of Things (IoT)." In: *International Conference on Computing, Communication Automation*. 2015, pp. 427–431. DOI: 10.1109/CCAA.2015.7148413.

[5] I. Bastos, L. B. Oliveira, J. Goes, and M. Silva. "A low power balun LNA with active loads for gain and noise figure optimization." In: *Analog Integrated Circuits and Signal Processing* 81.3 (2014), pp. 693–702. ISSN: 1573-1979. DOI: 10.1007/s10470-014-0426-6. URL: https://doi.org/10.1007/s10470-014-0426-6.

[6] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta. "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling." In: *Solid-State Circuits, IEEE Journal of* 43.6 (2008), pp. 1341–1350. ISSN: 0018-9200. DOI: 10.1109/JSSC.2008.922736.

[7] C. Botteron, D. Briand, B. Mishra, G. Tasselli, P. Janphuang, F.-J. Haug, A. Skrivervik, R. Lockhart, C. Robert, N. de Rooij, and P.-A. Farine. "A low-cost UWB sensor node powered by a piezoelectric harvester or solar cells." In: *Sensors and Actuators A: Physical* 239.Supplement C (2016), pp. 127 –136. ISSN: 0924-4247. DOI: https://doi.org/10.1016/j.sna.2016.01.011. URL: http://www.sciencedirect.com/science/article/pii/S0924424716300115.

[8] A. W. Burange and H. D. Misalkar. "Review of Internet of Things in development of smart cities with data management amp; privacy." In: *2015 International Conference on Advances in Computer Engineering and Applications*. 2015, pp. 189–195. DOI: 10.1109/ICACEA.2015.7164693.

[9] R. B. Caldas, F. L. Correa, J. A. Nacif, T. R. Roque, L. B. Ruiz, A. O. Fernandas, J. M. da Mata, and C. Coelho. "Low power/high performance self-adapting sensor node architecture." In: *2005 IEEE Conference on Emerging Technologies and Factory Automation*. Vol. 2. 2005, 4 pp.–976. DOI: 10.1109/ETFA.2005.1612777.

[10] B. H. Calhoun, D. C. Daly, N. Verma, D. F. Finchelstein, D. D. Wentzloff, A. Wang, S.-H. Cho, and A. P. Chandrakasan. "Design considerations for ultra-low energy wireless microsensor nodes." In: *IEEE Transactions on Computers* 54.6 (2005), pp. 727–740. ISSN: 0018-9340. DOI: 10.1109/TC.2005.98.

[11] J. Calusdian, X. Yun, J. Li, Y. Lu, and M. Meyyappan. "Design and Testing of a Wireless Portable Carbon Nanotube-Based Chemical Sensor System." In: *2006 Sixth IEEE Conference on Nanotechnology*. Vol. 2. 2006, pp. 794–797. DOI: 10.1109/NANO.2006.247778.

[12] A. Chen, A. G. de Castro, E. J. Palacios-García, J. M. Flores-Arias, and F. J. Bellido-Outeiriño. "In-home data acquisition and control system based on BLE." In: *2015 International Symposium on Consumer Electronics (ISCE)*. 2015, pp. 1–2. DOI: 10.1109/ISCE.2015.7177780.

[13] F. Chen, L. Guo, and C. Chen. "A Survey on Energy Management in the Wireless Sensor Networks." In: *IERI Procedia* 3.Supplement C (2012). 2012 International Conference on Mechanical and Electronics Engineering, September 27-28, 2012 Bangkok, Thailand, pp. 60 –66. ISSN: 2212-6678. DOI: https://doi.org/10.1016/j.ieri.2012.09.011. URL: http://www.sciencedirect.com/science/article/pii/S2212667812002201.

[14] T. S. Cho, K. J. Lee, J. Kong, and A. P. Chandrakasan. "A Low Power Carbon Nanotube Chemical Sensor System." In: *2007 IEEE Custom Integrated Circuits Conference*. 2007, pp. 181–184. DOI: 10.1109/CICC.2007.4405708.

[15] T. S. Cho, K. J. Lee, J. Kong, and A. P. Chandrakasan. "A 32-*mu* W 1.83-kS/s Carbon Nanotube Chemical Sensor System." In: *IEEE Journal of Solid-State Circuits* 44.2 (2009), pp. 659–669. ISSN: 0018-9200. DOI: 10.1109/JSSC.2008.2010805.

[16] T. S. Cho, K. jae Lee, J. Kong, and A. P. Chandrakasan. "The design of a low power carbon nanotube chemical sensor system." In: *2008 45th ACM/IEEE Design Automation Conference*. 2008, pp. 84–89.

[17] S. Choi, H. Cha, and S. Cho. "A SoC-based Sensor Node: Evaluation of RETOS-enabled CC2430." In: *2007 4th Annual IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks*. IEEE, 2007, pp. 132–141. ISBN: 1-4244-1268-4. DOI: 10.1109/SAHCN.2007.4292825. URL: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4292825.

[18] A. Chouder, S. Silvestre, N. Sadaoui, and L. Rahmani. "Modeling and simulation of a grid connected PV system based on the evaluation of main PV module parameters." In: *Simulation Modelling Practice and Theory* 20.1 (2012), pp. 46–58. ISSN: 1569190X. DOI: 10.1016/j.simpat.2011.08.011. URL: http://linkinghub.elsevier.com/retrieve/pii/S1569190X11001456.

[19] J. F. Christmann, E. Beigné, C. Condemine, J. Willemin, and C. Piguet. "Energy Harvesting and Power Management for Autonomous Sensor Nodes." In: *Proceedings of the 49th Annual Design Automation Conference*. DAC '12. San Francisco, California: ACM, 2012, pp. 1049–1054. ISBN: 978-1-4503-1199-1. DOI: 10.1145/2228360.2228550. URL: http://doi.acm.org/10.1145/2228360.2228550.

[20] L. Coetzee and J. Eksteen. "The Internet of Things - promise for the future? An introduction." In: *2011 IST-Africa Conference Proceedings*. 2011, pp. 1–9.

[21] J. Cubas, S. Pindado, and C. De Manuel. *New Method for Analytical Photovoltaic Parameters Identification: Meeting Manufacturer's Datasheet for Different Ambient Conditions*. URL: http://oa.upm.es/30687/1/2014enef.pdf.

[22] C. Enz. "MOS transistor modeling for RF integrated circuit design." In: *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*. 2000, pp. 189–196. DOI: 10.1109/CICC.2000.852646.

[23] S. Esmaeili and M. F. Ain. "Design and Implementation of Self-Reconfigurable Wireless Sensor Node Based on Wireless Sensor Network." In: *2013 1st International Conference on Artificial Intelligence, Modelling and Simulation*. 2013, pp. 409–412. DOI: 10.1109/AIMS.2013.74.

[24] C.-W. Ho, A. E. Ruehli, and P. A. Brennan. "The modified nodal approach to network analysis." In: *Circuits and Systems, IEEE Transactions on* 22.6 (1975), pp. 504–509. ISSN: 0098-4094. DOI: 10.1109/TCS.1975.1084079.

[25] A. Hyldgård, D. Mortensen, K. Birkelund, O. Hansen, and E. Thomsen. "Autonomous multi-sensor micro-system for measurement of ocean water salinity." In: *Sensors and Actuators A: Physical* 147.2 (2008), pp. 474 –484. ISSN: 0924-4247. DOI: https://doi.org/10.1016/j.sna.2008.06.004. URL: http://www.sciencedirect.com/science/article/pii/S0924424708003208.

[40] T. Instruments. "MSP430FR599x, MSP430FR596x Mixed-Signal Microcontrollers." In: (). URL: http://www.ti.com/lit/ds/symlink/msp430fr5994.pdf.

[26] International Electrotechnical Commission. "Internet of Things: Wireless Sensor Networks." In: *White Paper* December (2014). URL: http://www.iec.ch/whitepaper/pdf/iecWP-internetofthings-LR-en.pdf.

[27] F. Karray, M. W. Jmal, M. Abid, M. S. BenSaleh, and A. M. Obeid. "A review on wireless sensor node architectures." In: *2014 9th International Symposium on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC)*. 2014, pp. 1–8. DOI: 10.1109/ReCoSoC.2014.6861346.

[28] H. G. Lee and N. Chang. "Powering the IoT: Storage-less and converter-less energy harvesting." In: *The 20th Asia and South Pacific Design Automation Conference*. 2015, pp. 124–129. DOI: 10.1109/ASPDAC.2015.7058992.

[29] Linear Technology Corporation. *LTC3531/ LTC3531-3.3/LTC3531-3 200mA Buck-Boost Synchronous DC/DC Converters*. URL: http://cds.linear.com/docs/en/datasheet/3531fb.pdf.

[30] Linear Technology Corporation. *LTC4425 - Linear SuperCap Charger with Current-Limited Ideal Diode and V/I Monitor*. URL: http://cds.linear.com/docs/en/datasheet/4425fa.pdf.

[31] V. C. Meireles. *Circuitos Eéctricos*. LIDEL, 2009. ISBN: 9789727575862.

[32] D. Miorandi, S. Sicari, F. D. Pellegrini, and I. Chlamtac. "Internet of things: Vision, applications and research challenges." In: *Ad Hoc Networks* 10.7 (2012), pp. 1497 –1516. ISSN: 1570-8705. DOI: https://doi.org/10.1016/j.adhoc.2012.02.016. URL: http://www.sciencedirect.com/science/article/pii/S1570870512000674.

[33] *Nanopower Buck-Boost DC DC with Energy Harvesting Battery Charger*. LTC3331. Rev. C. Linear Technology. 2014. URL: http://www.linear.com/product/LTC3331.

[34] M. A. Rajan, P. Balamuralidhar, K. P. Chethan, and M. Swarnahpriyaah. "A Self-Reconfigurable Sensor Network Management System for Internet of Things Paradigm." In: *2011 International Conference on Devices and Communications (ICDeCom)*. 2011, pp. 1–5. DOI: 10.1109/ICDECOM.2011.5738550.

[35] E. Santin and F. Gil. "MATLAB Tool for Symbolic Analysis of Analog Circuits - MSAAC." In: (2012).

[36] M. Severini, S. Squartini, F. Piazza, and M. Conti. "Energy-Aware task scheduler for self-powered sensor nodes: From model to firmware." In: *Ad Hoc Networks* 24.Part A (2015), pp. 73 –91. ISSN: 1570-8705. DOI: https://doi.org/10.1016/j.adhoc.2014.06.009. URL: http://www.sciencedirect.com/science/article/pii/S1570870514001644.

[37] F. Simjee and P. H. Chou. "Everlast: Long-life, Supercapacitor-operated Wireless Sensor Node." In: *ISLPED'06 Proceedings of the 2006 International Symposium on Low Power Electronics and Design*. 2006, pp. 197–202. DOI: 10.1145/1165573.1165619.

[38] D. Singh, G. Tripathi, and A. J. Jara. "A survey of Internet-of-Things: Future vision, architecture, challenges and services." In: *2014 IEEE World Forum on Internet of Things (WF-IoT)*. 2014, pp. 287–292. DOI: 10.1109/WF-IoT.2014.6803174.

[39] S. Sudevalayam and P. Kulkarni. "Energy Harvesting Sensor Nodes: Survey and Implications." In: *IEEE Communications Surveys Tutorials* 13.3 (2011), pp. 443–461. ISSN: 1553-877X. DOI: 10.1109/SURV.2011.060710.00094.

[41] Texas Instruments. *TPS22860 Ultra-Low Leakage Load Switch 1 Features 3 Description*. URL: http://www.ti.com/lit/ds/symlink/tps22860.pdf.

[42] Texas Instruments. *TPS22918 5.5-V, 2-A, 52-mΩ On-Resistance Load Switch*. URL: http://www.ti.com/lit/ds/symlink/tps22918.pdf.

[43] Texas Instruments. *TPS6300x High-Efficient Single Inductor Buck-Boost Converter With 1.8-A Switches*. URL: http://www.ti.com/lit/ds/symlink/tps63001.pdf.

[44] Texas Instruments. "TS12A4514, TS12A4515 SPST CMOS ANALOG SWITCHES." In: (). URL: http://www.ti.com/lit/ds/symlink/ts12a4514.pdf.

[45] Texas Instruments. "MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx Family User's Guide." In: (2012). URL: http://www.ti.com/lit/ug/slau367n/slau367n.pdf.

[46] T. Tuma and Á Buermen. *Circuit simulation with SPICE OPUS: theory and practice*. 2009, p. 399. ISBN: 9780817648664. DOI: 10.1007/978-0-8176-4867-1. arXiv: arXiv:1011.1669v3.

[47] U. V. Wali, R. N. Pal, and B. Chatterjee. "On the modified nodal approach to network analysis." In: *Proceedings of the IEEE* 73.3 (1985), pp. 485–487. ISSN: 0018-9219. DOI: 10.1109/PROC.1985.13168.

[48] Z. Xinhua and L. Hong. "A Self-Reconfigurable Sensor Network Constructon Reaseach in the Paradigm of Internet of Things." In: *2012 International Conference on Computer Science and Service System*. 2012, pp. 311–314. DOI: 10.1109/CSSS.2012.85.

[49] H. Yang and Y. Zhang. "Analysis of Supercapacitor Energy Loss for Power Management in Environmentally Powered Wireless Sensor Nodes." In: *IEEE Transactions on Power Electronics* 28.11 (2013), pp. 5391–5403. ISSN: 0885-8993. DOI: 10.1109/TPEL.2013.2238683.

[50] A. B. Yildiz. "Modified Nodal Analysis-Based Determination of Transfer Functions for Multi-Inputs Multi-Outputs Linear Circuits." In: *Automatika* 51.4 (2010), pp. 353–360.

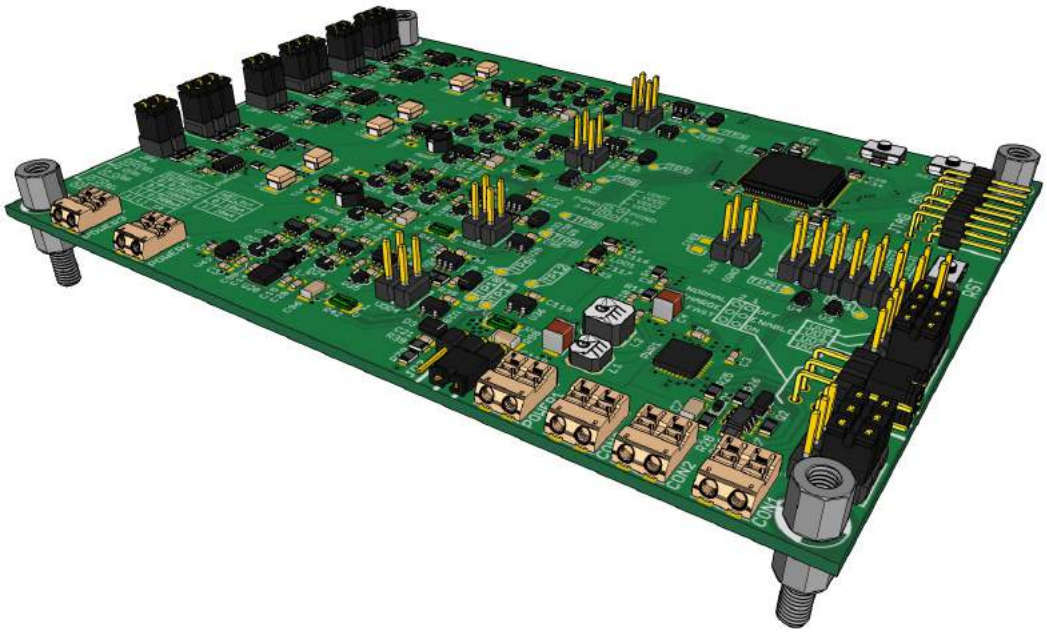
[51] H. Yu, Y. Inoue, Y. Matsuya, and Z. Huang. "An effective pseudo-transient algorithm for finding DC operating points of nonlinear circuits." In: *2006 IEEE International Symposium on Circuits and Systems*. 2006, 4 pp.–1775. DOI: 10.1109/ISCAS.2006.1692949.

[52] Z. Zhu and S. H. Yang. "A Possible Hardware Architecture of Wireless Sensor Nodes." In: *2006 IEEE International Conference on Systems, Man and Cybernetics*. Vol. 4. 2006, pp. 3377–3381. DOI: 10.1109/ICSMC.2006.384640.

Appendix A

Power Management

A.1 PCB Circuitt & Layout



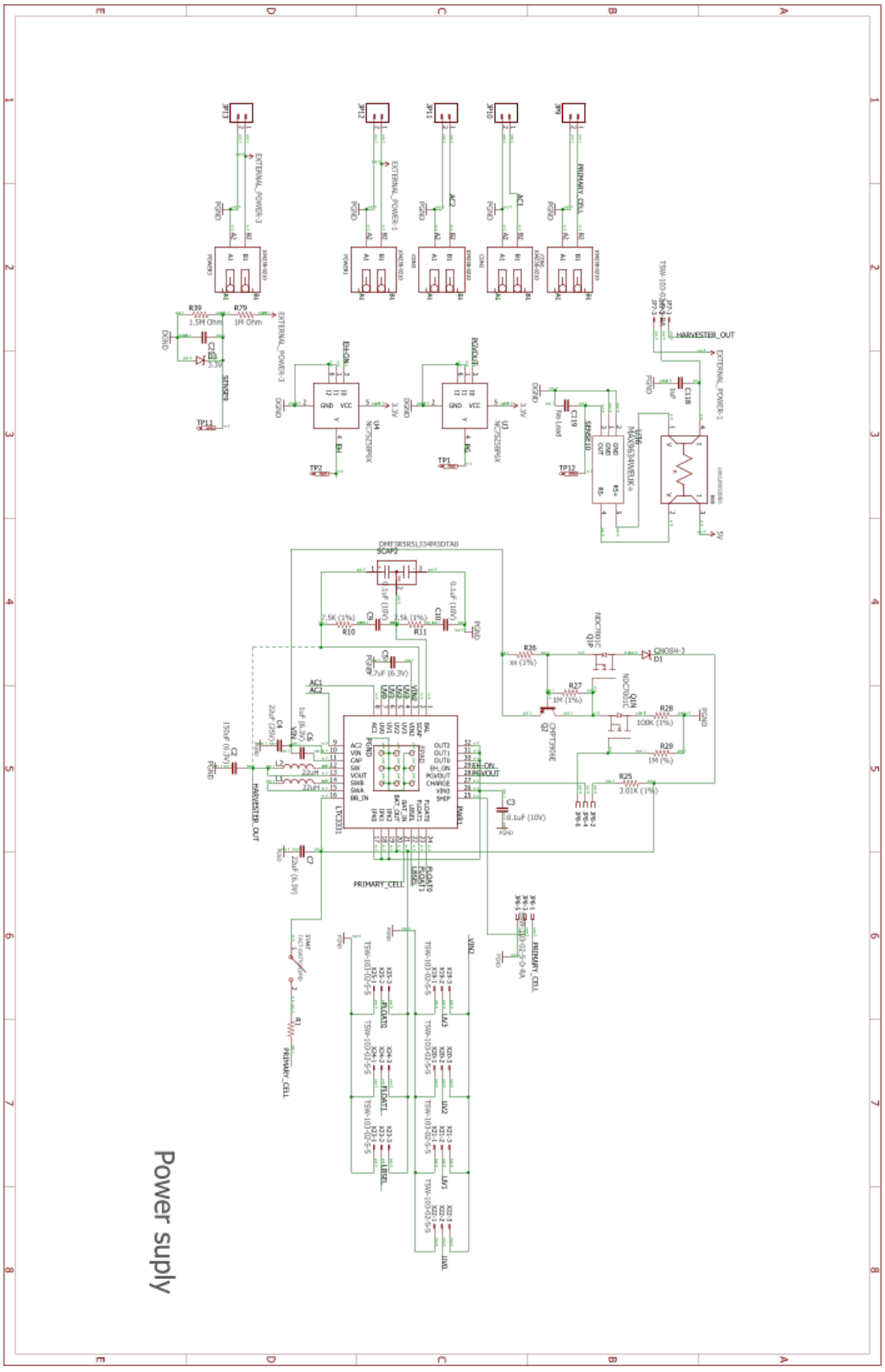


Figure A.1: Input power connections and harvester circuit.

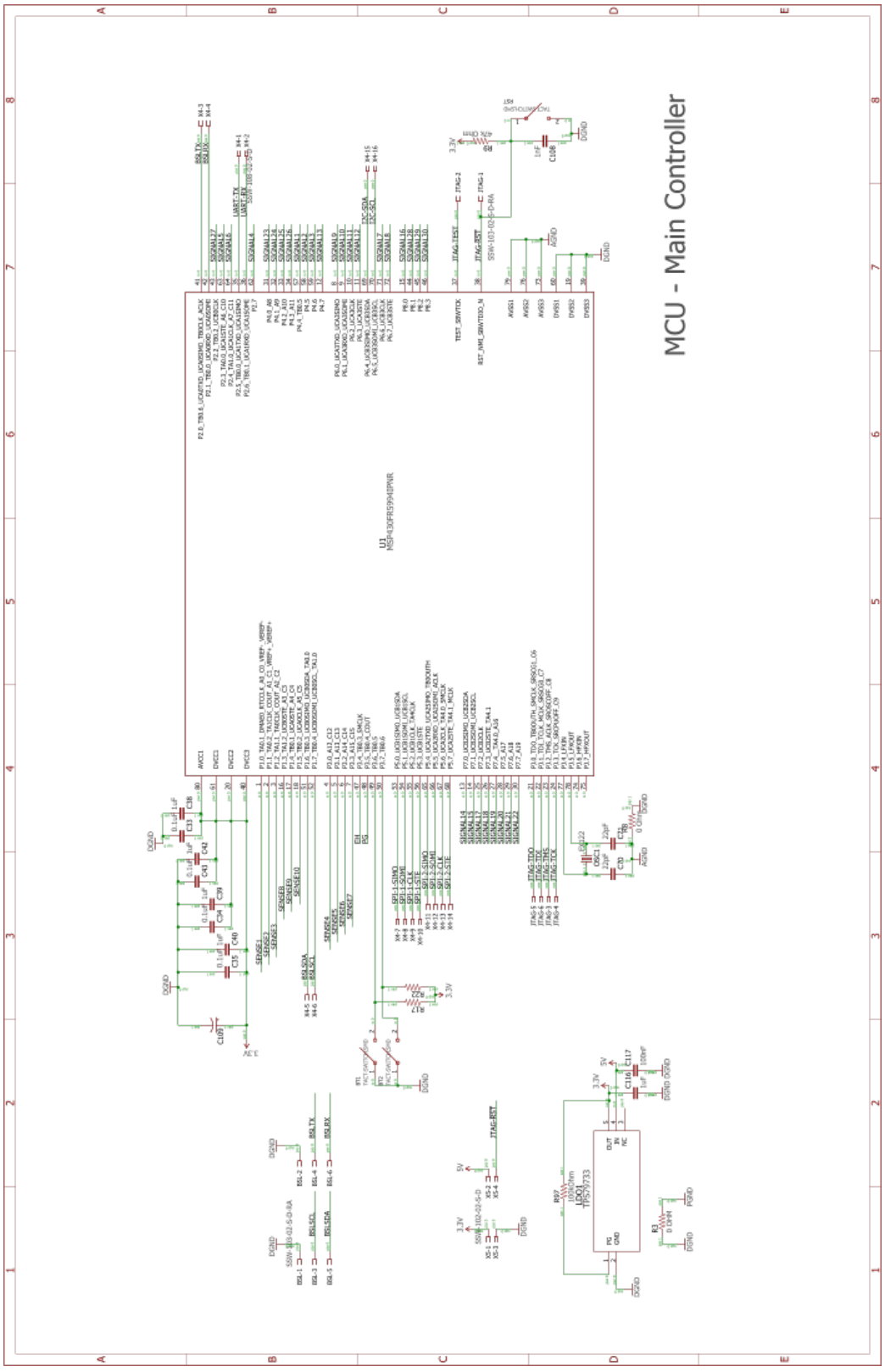


Figure A.2: MSP430 circuit and analog and digital signal connections.

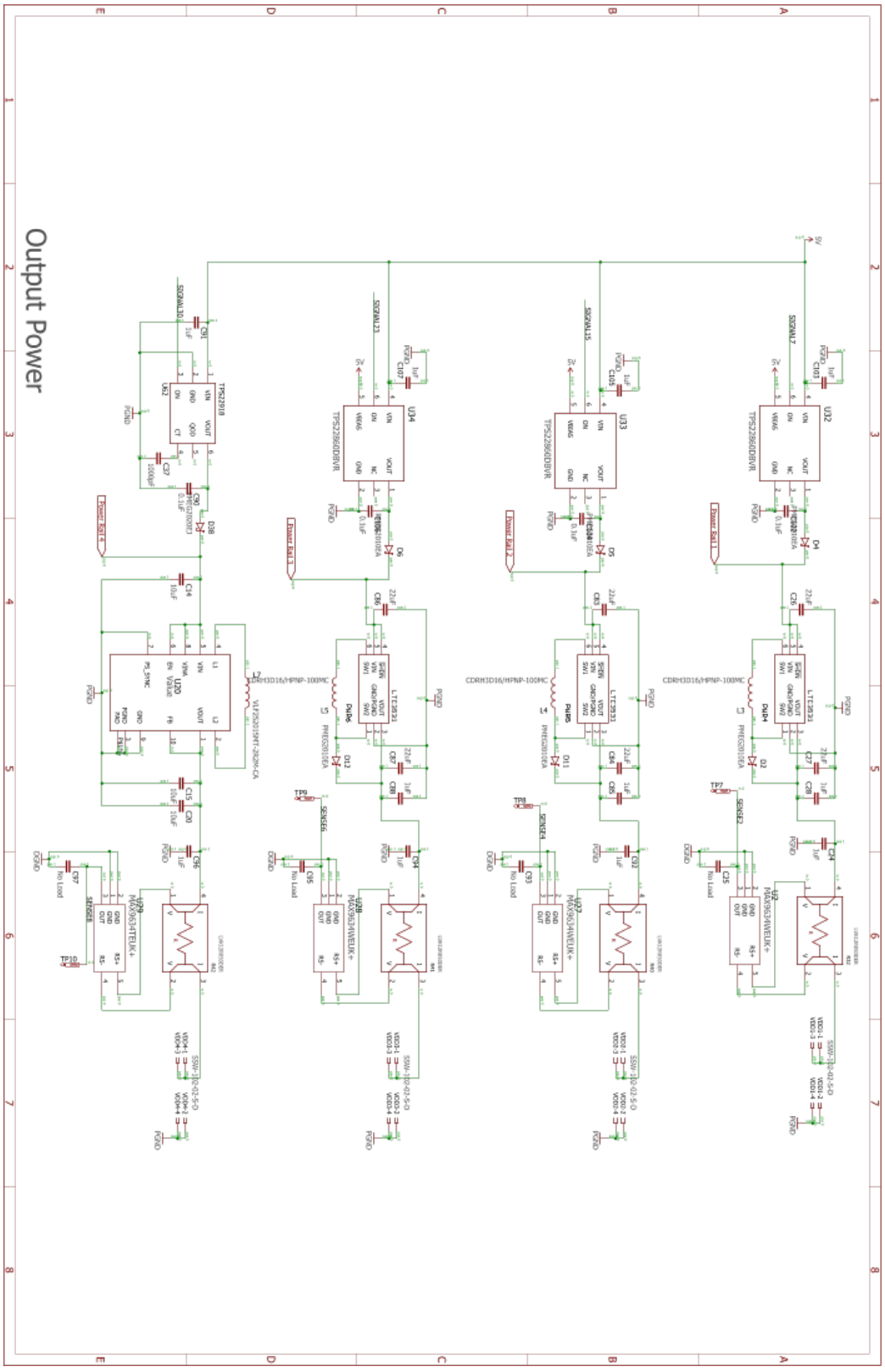


Figure A.3: Four output power connections and there respective DC/DC Converters. There is also present the current sensing circuits.

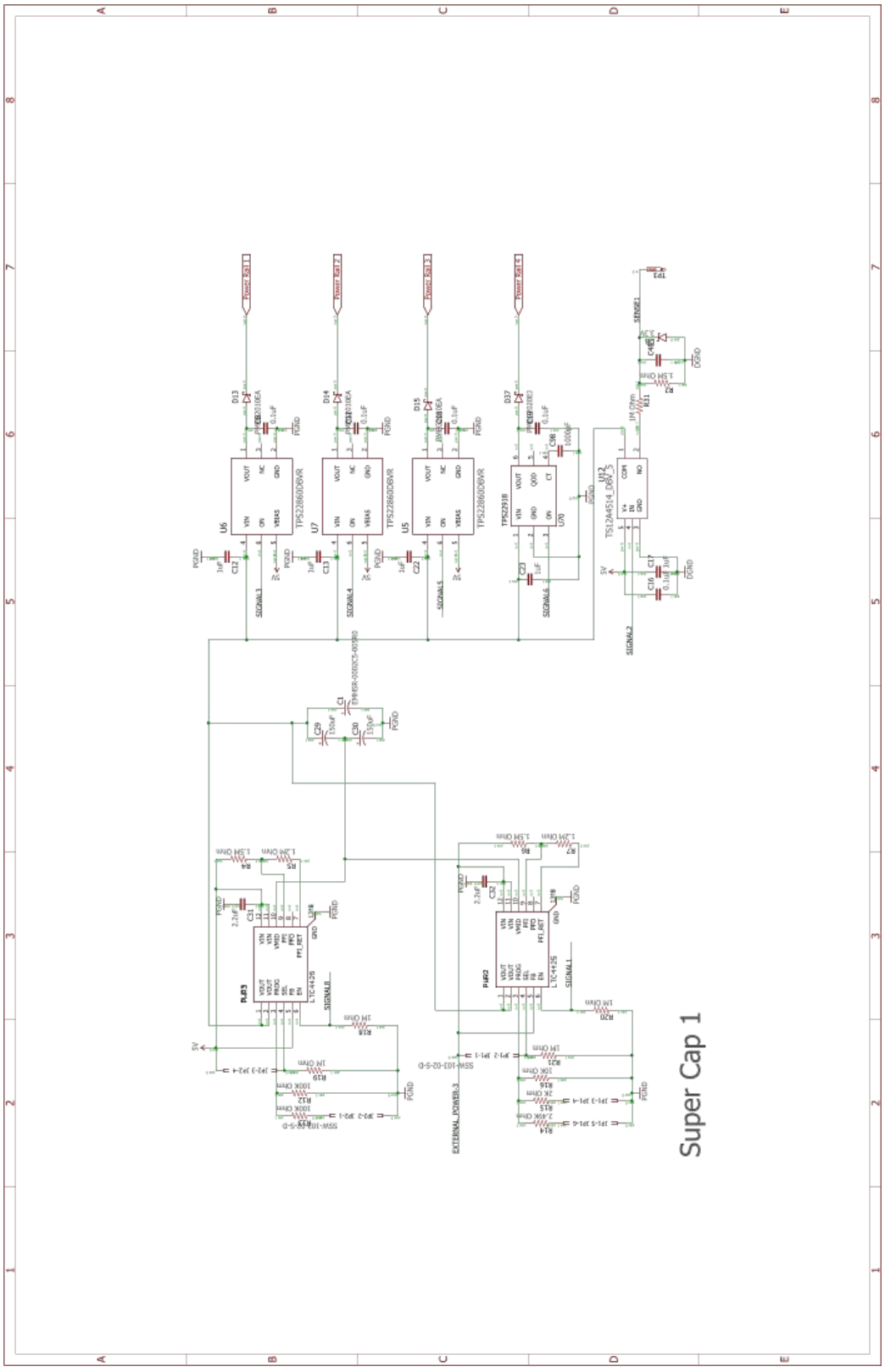


Figure A.4: First super-capacitor and its chargers, its also present the voltage sensing circuit.

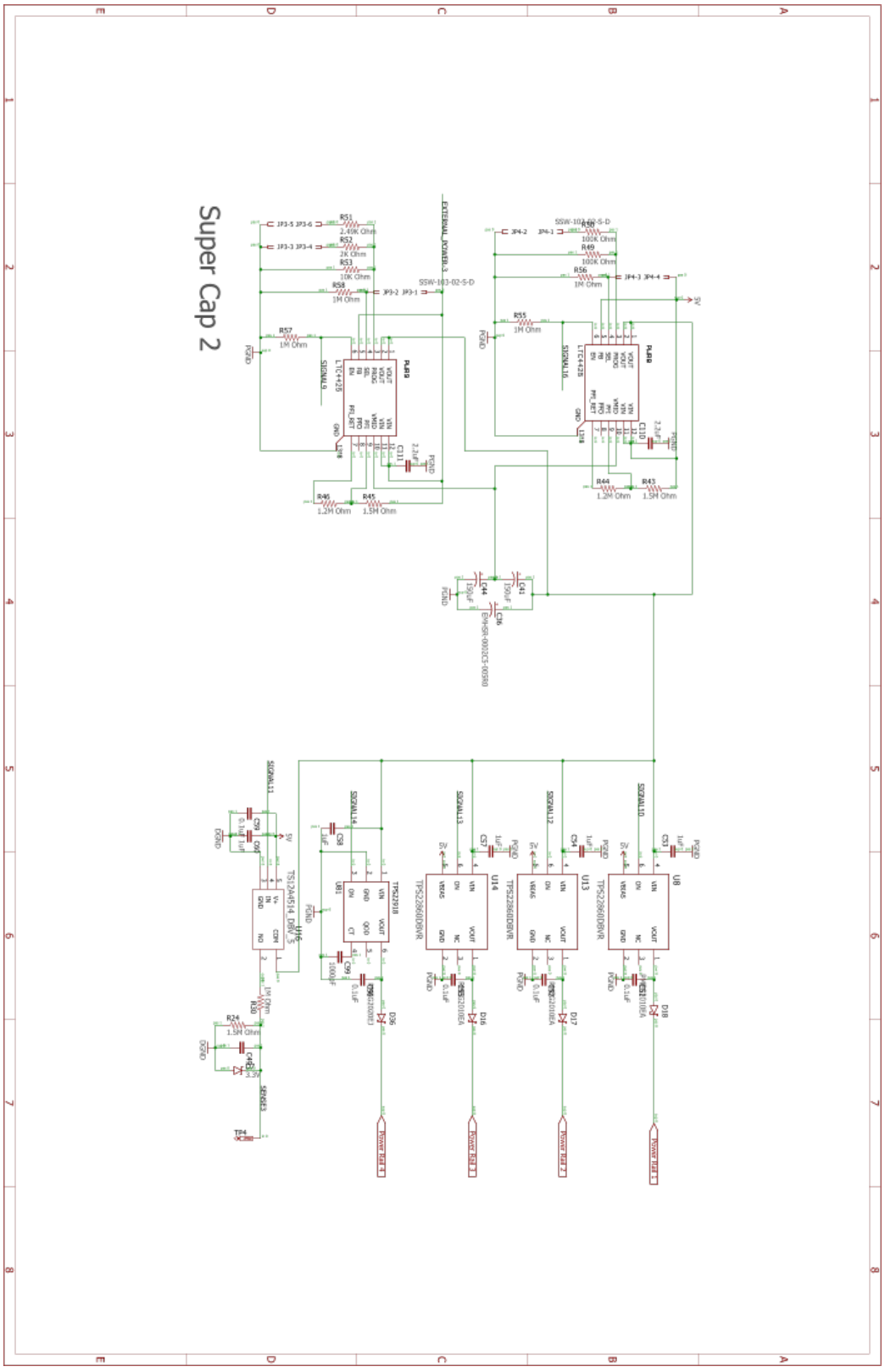


Figure A.5: Second super-capacitor and its chargers, its also present the voltage sensing circuit.

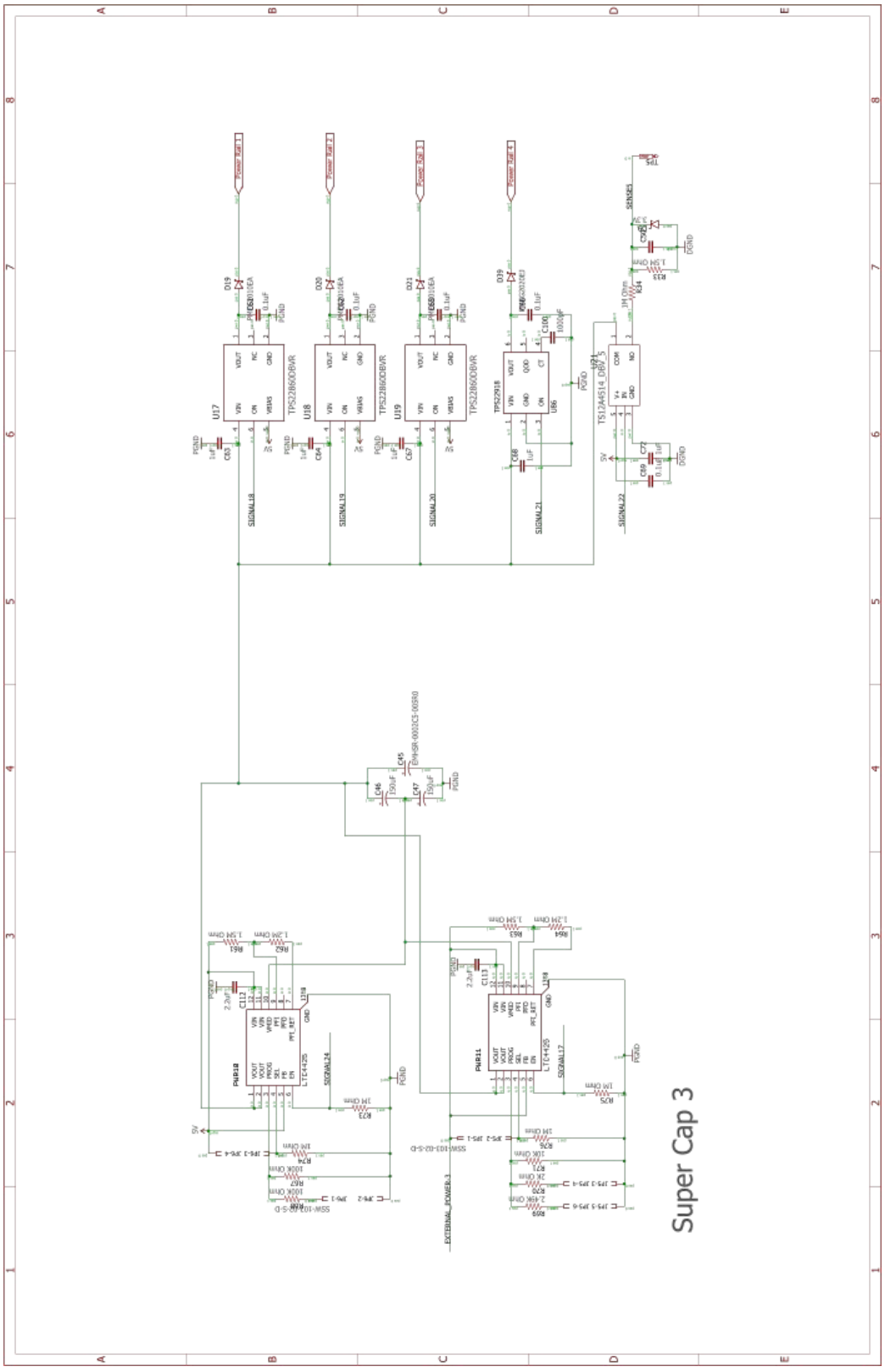


Figure A.6: Third super-capacitor and its chargers, its also present the voltage sensing circuit.

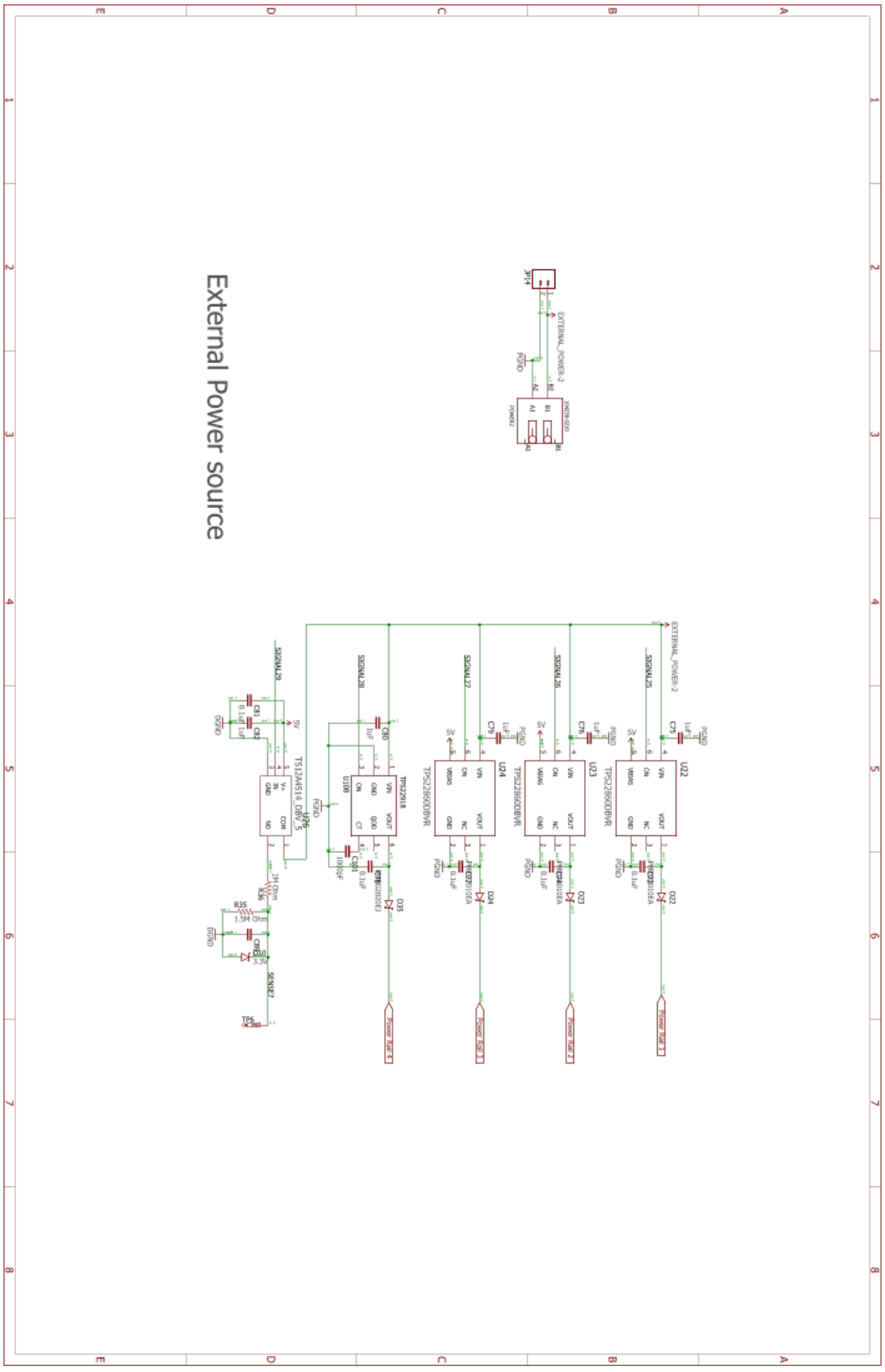
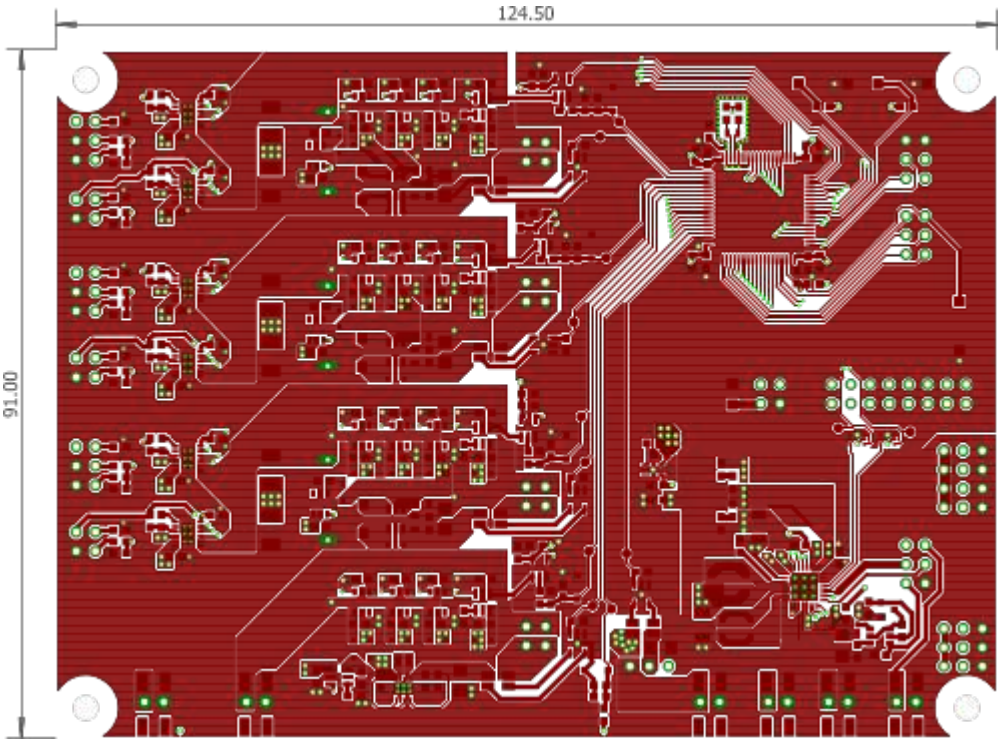
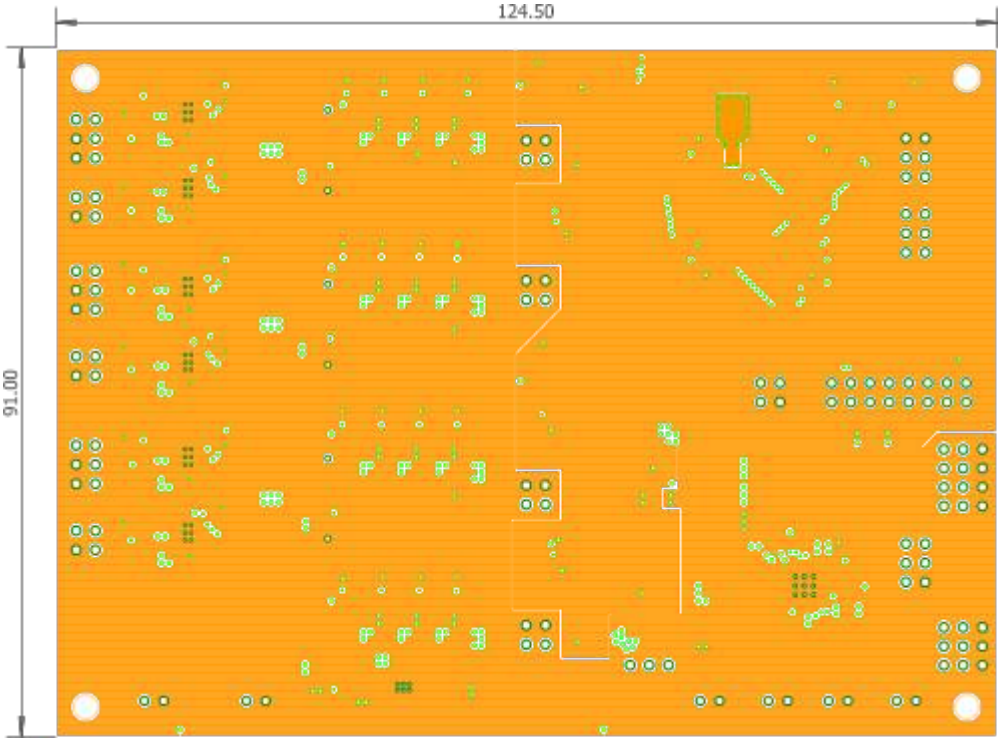


Figure A.7: External power input to supply directly to the outputs.

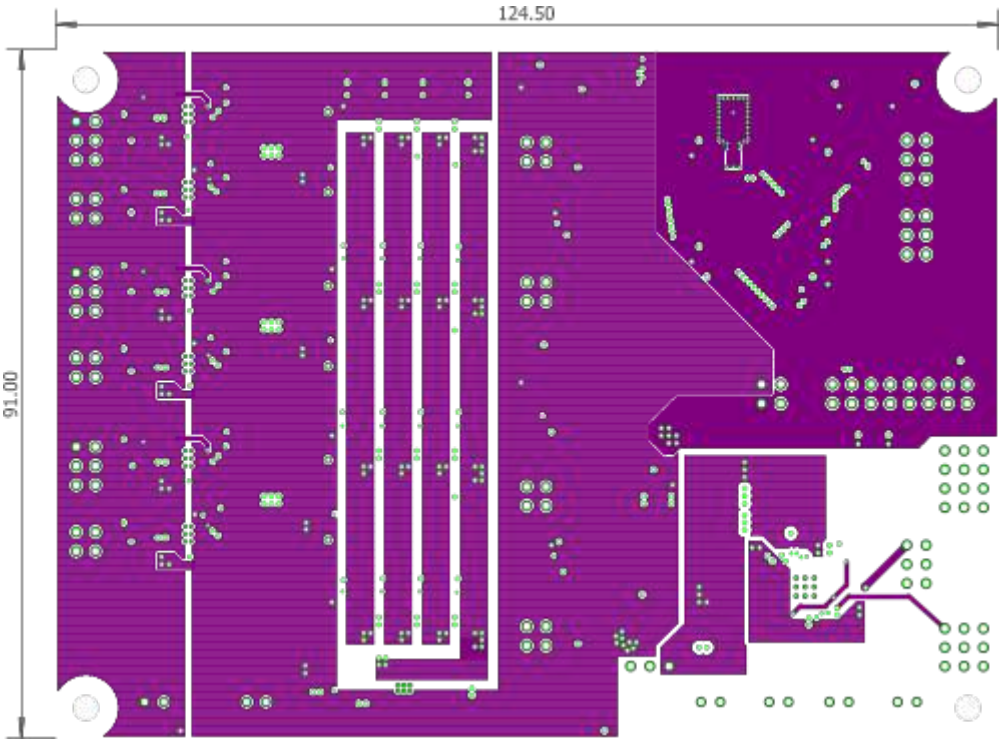


(a) First layer of the PCB layout implementation. This the signal routing plane.

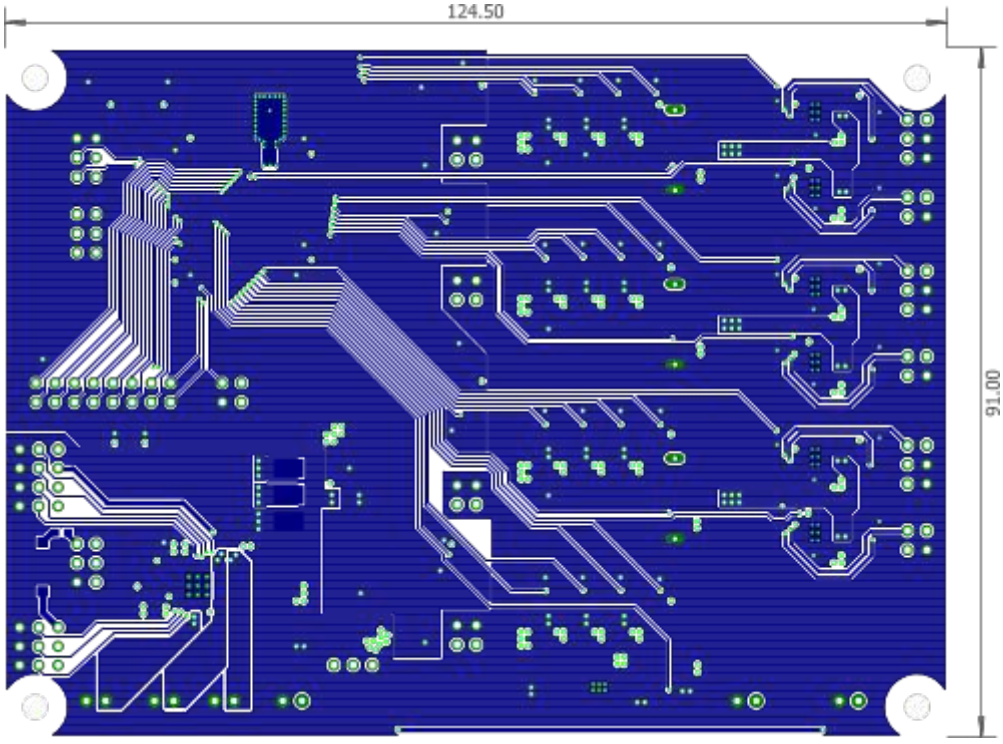


(b) Second layer of the PCB layout implementation. This is the ground plane.

Figure A.8: PMU PCB layout, first tow layers.

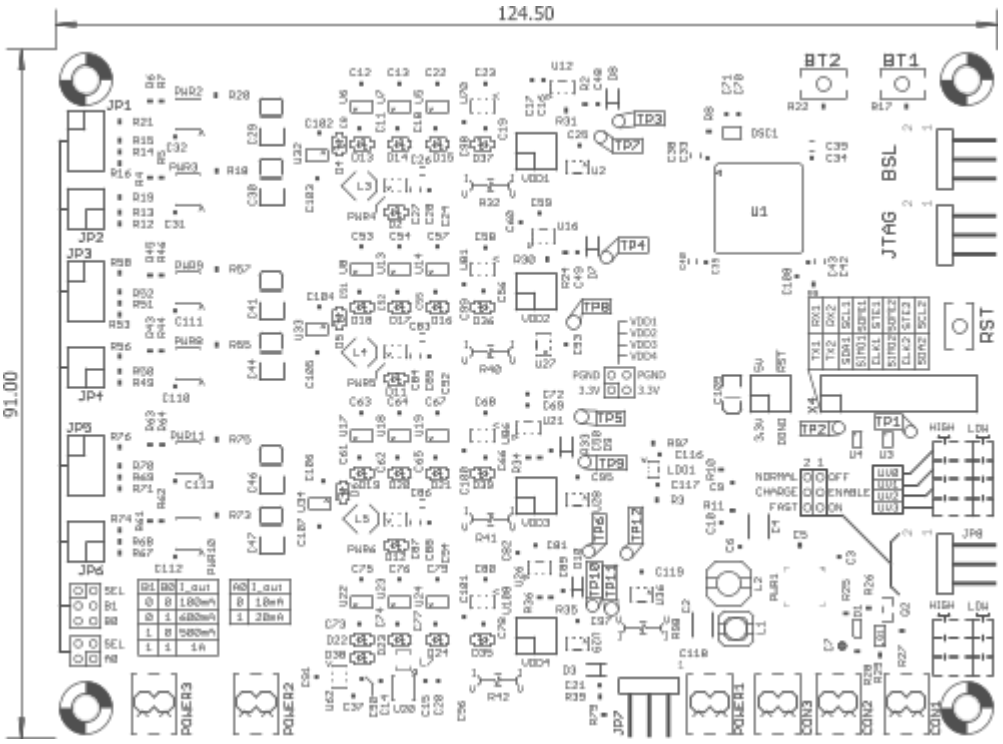


(a) Third layer of the PCB layout implementation. This is the power plane.

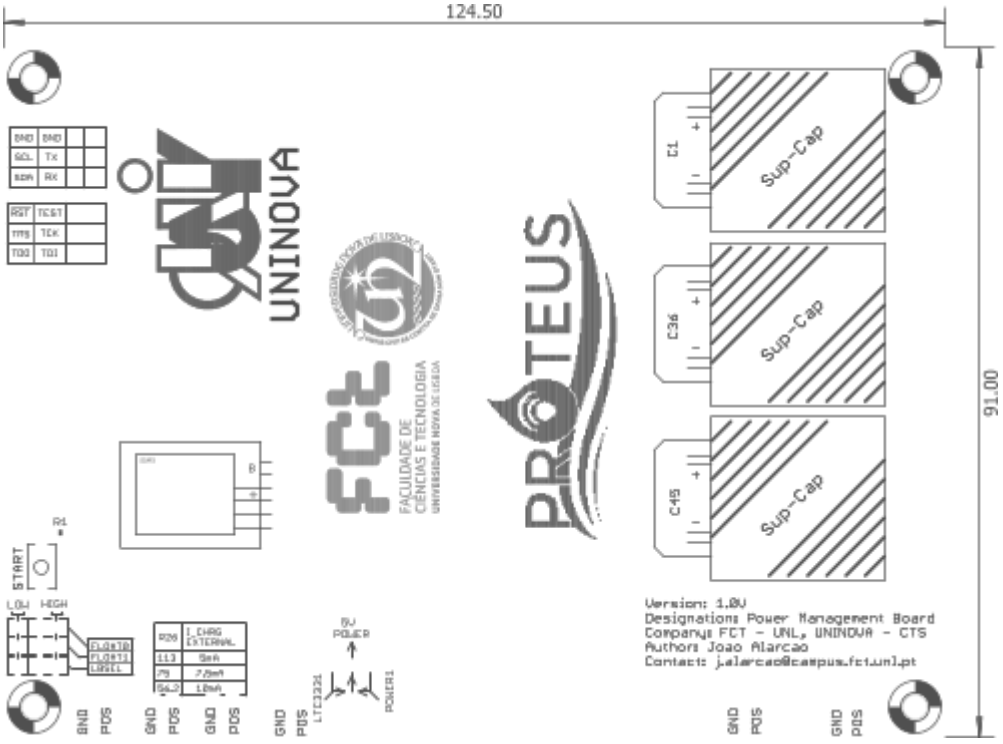


(b) Fourth layer of the PCB layout implementation. This is second signal routing plane.

Figure A.9: PMU PCB layout, last tow layers.



(a) Top label layer.



(b) Bottom label layer.

Figure A.10: PMU PCB silk-screen layer, top and bottom.

A.2 Prototype Communication Interface

A.2.1 Messages received by the Power Management Board

A.2.1.1 OpCode 176 and 177

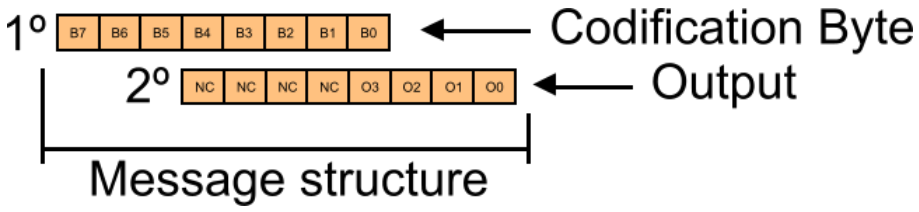


Figure A.11: Message structure for OpCode 176 and 177.

Messages for OpCode 176 and 177 are to bytes long.

- 1º byte codification:
  - OpCode 176 : Binary representation [B0:B7] = 10110000.
  - OpCode 177 : Binary representation [B0:B7] = 10110001.
- 2º byte codification:
  - Bits [O0:O3] : Output number, from one to four. Represented as decimal value.
  - Bits NC : Not used.

A.2.1.2 OpCode 200 and 202

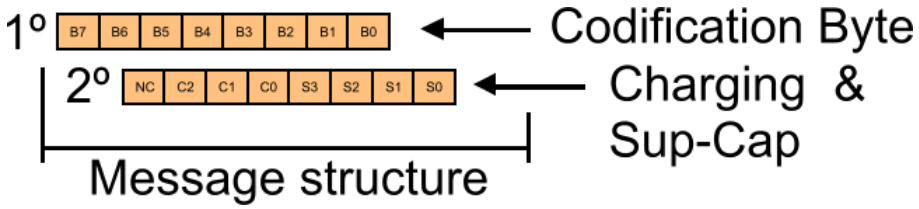


Figure A.12: Message structure for OpCode 200 and 202.

Messages for OpCode 200 and 202 are to bytes long.

- 1º byte codification:
  - OpCode 200 : Binary representation [B0:B7] = 11001000.
  - OpCode 202 : Binary representation [B0:B7] = 11001010.
- 2º byte codification:
  - Bits [S0:S3] : Super-capacitor number, from one to three. Represented as decimal value.

- Bits C0 : Low current charger enable.
- Bits C1 : High current charger enable.
- Bits NC : Not used.

A.2.1.3 OpCode 201

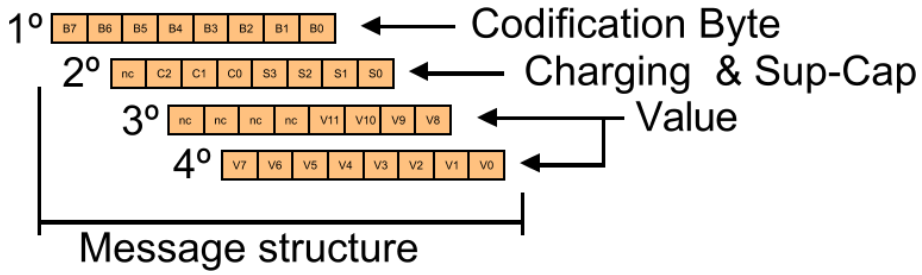


Figure A.13: Message structure for OpCode 201.

Messages for OpCode 201 is four bytes long.

- 1º byte codification:
  - OpCode 201: Binary representation [B0:B7] = 110010001.
- 2º byte codification:
  - Bits [S0:S3] : Super-capacitor number, from one to three. Represented as decimal value.
  - Bits C0 : Low current charger enable.
  - Bits C1 : High current charger enable.
  - Bits C1 : Stop chargers controller if value reached.
  - Bits NC : Not used.
- 3º and 4º bytes codification:
  - Bits [V8:V11] : This are the most significant bits of a 12 bit value.
  - Bits [V0:V8] : This are the less significant bits of a 12 bit value.

A.2.1.4 OpCode 203

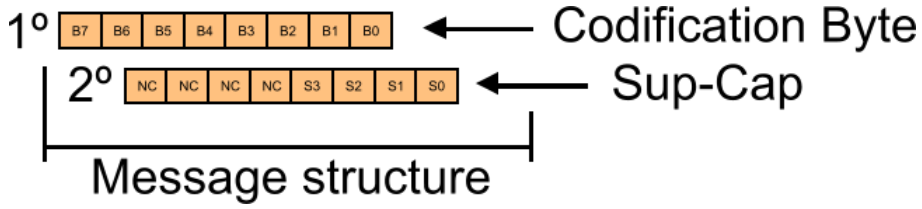


Figure A.14: Message structure for OpCode 203.

Messages for OpCode 203 is to bytes long.

- 1º byte codification:
  - OpCode 203 : Binary representation [B0:B7] = 11001011.
- 2º byte codification:
  - Bits [S0:S3] : Super-capacitor number, from one to three. Represented as decimal value.
  - Bits NC : Not used.

A.2.1.5 OpCode 204 and 205

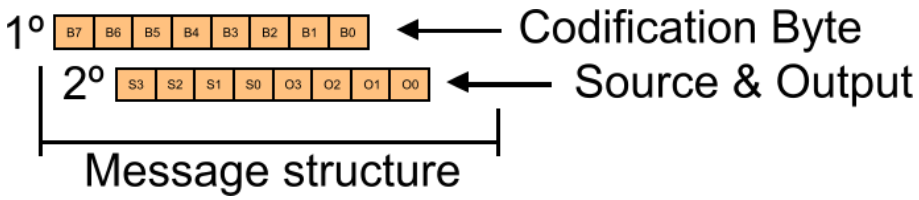


Figure A.15: Message structure for OpCode 204 and 205.

Messages for OpCode 204 and 205 is to bytes long.

- 1º byte codification:
  - OpCode 204 : Binary representation [B0:B7] = 11001100.
  - OpCode 205 : Binary representation [B0:B7] = 11001101.
- 2º byte codification:
  - Bits [O0:O3] : Output number, from one to four. Represented as decimal value.
  - Bits [S0:S3] : Super-capacitor number, from one to three and external power supply represented with a four. Represented as decimal values.
  - Bits NC : Not used.

A.2.2 Messages send by the Power Management Board

A.2.2.1 OpCode 11

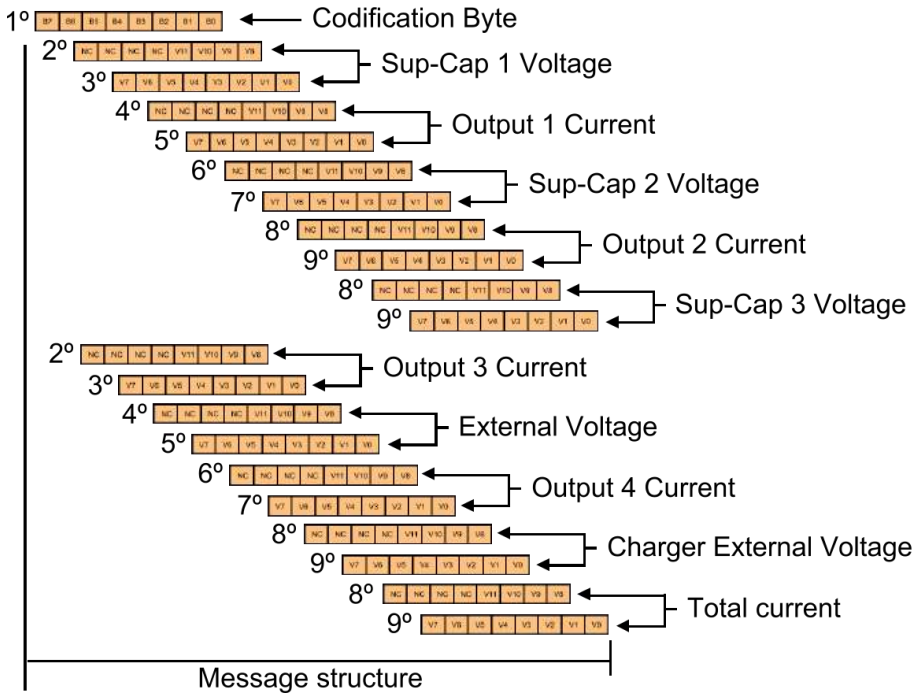


Figure A.16: Message structure for OpCode 11.

Messages for OpCode 11 is twenty one bytes long.

- 1º byte codification:
  - OpCode 11 : Binary representation [B0:B7] = 00001011.
- All the rest of byte codification in pares:
  - Bits [V8:V11] : This are the most significant bits of a 12 bit value.
  - Bits [V0:V8] : This are the less significant bits of a 12 bit value.
  - Bits NC : Not used.

A.2.2.2 OpCode 50

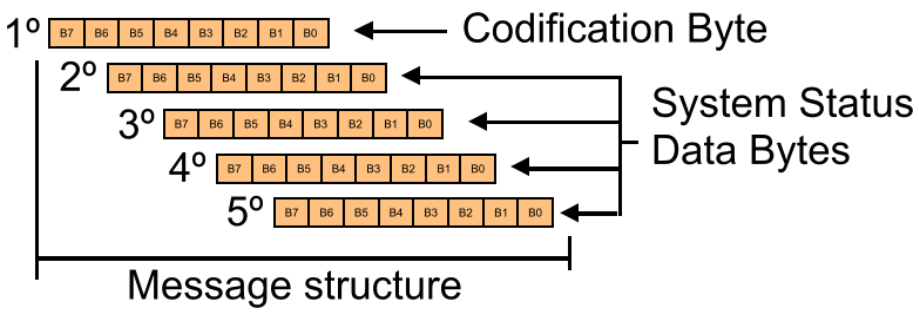


Figure A.17: Message structure for OpCode 50.

Messages for OpCode 50 is five bytes long.

- 1º byte codification:
  - OpCode 50 : Binary representation [B0:B7] = 00110010.
- 2º byte codification:
  - Bits B0 : Output1 conected to supercap1.
  - Bits B1 : Output1 conected to supercap2.
  - Bits B2 : Output1 conected to supercap3.
  - Bits B3 : Output1 conected to external.
  - Bits B4 : Output1 conected to harvester.
  - Bits B5 : Output2 conected to supercap1.
  - Bits B6 : Output2 conected to supercap2.
  - Bits B7 : Output2 conected to supercap3.
- 3º byte codification:
  - Bits B0 : Output2 conected to external.
  - Bits B1 : Output2 conected to harvester.
  - Bits B2 : Output3 conected to supercap1.
  - Bits B3 : Output3 conected to supercap2.
  - Bits B4 : Output3 conected to supercap3.
  - Bits B5 : Output3 conected to external.
  - Bits B6 : Output3 conected to harvester.
  - Bits B7 : Output4 conected to supercap1.
- 4º byte codification:

  - Bits B0 : Output4 conected to supercap2.
  - Bits B1 : Output4 conected to supercap3.
  - Bits B2 : Output4 conected to external.
  - Bits B3 : Output4 conected to harvester.
  - Bits [B4:B7] : Not used.

- 5º byte codification:
  - Bits B0 : Supercap1 charger high current active.
  - Bits B1 : Supercap1 charger low current active.
  - Bits B2 : Supercap2 charger high current active.
  - Bits B3 : Supercap2 charger low current active.
  - Bits B4 : Supercap3 charger high current active.
  - Bits B5 : Supercap3 charger low current active.
  - Bits B6 : EH_ON active.
  - Bits B7 : PGVOUT active.

A.3 Circuitt's Simulations

A.3.1 Harvester - LTC3331

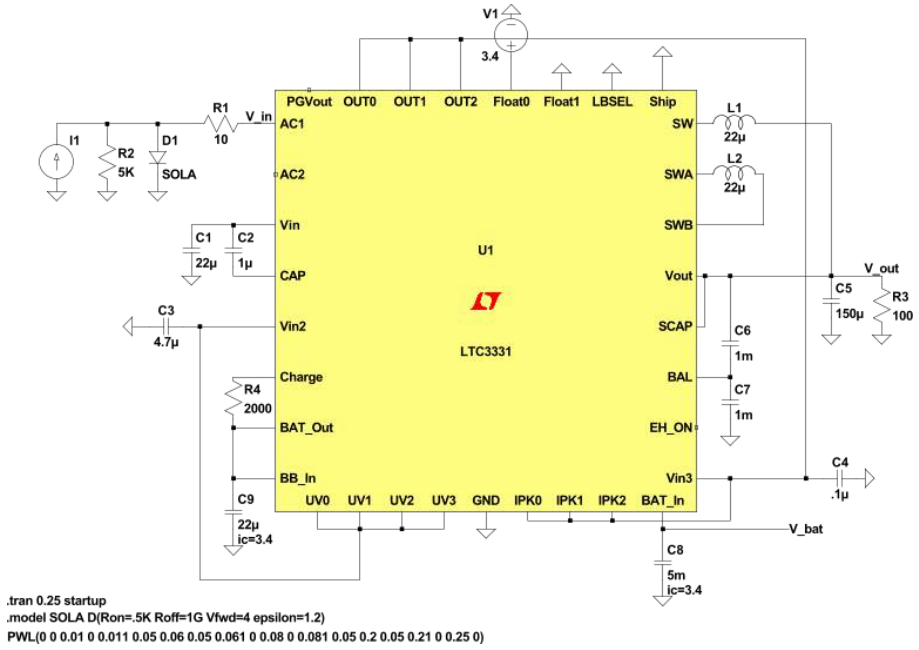


Figure A.18: Circuit for simulating the harvester (LTC3331) performance.

A.3.2 Load Switch - TPS22918

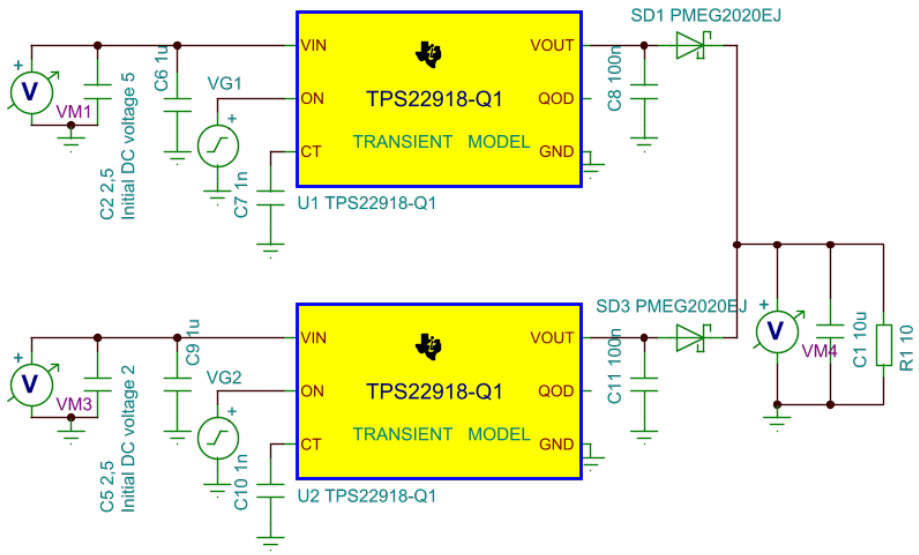


Figure A.19: Circuit for simulating the high current power switch (TPS22918) performance.

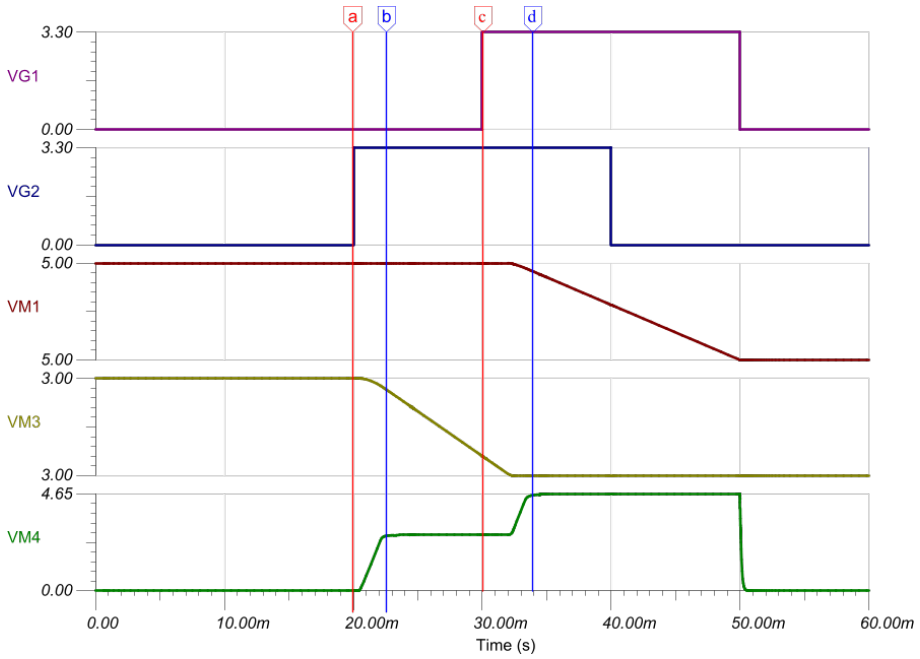


Figure A.20: Simulation for the load switch TPS22918. Its was tested withe a $10Ohm$ load, ans it switch from a $3.3V$ to a $5V$ power supply. The enable signal from the tow switches are overlaps. There is no drop in the output voltage, it increases form $3V$ to $5V$.

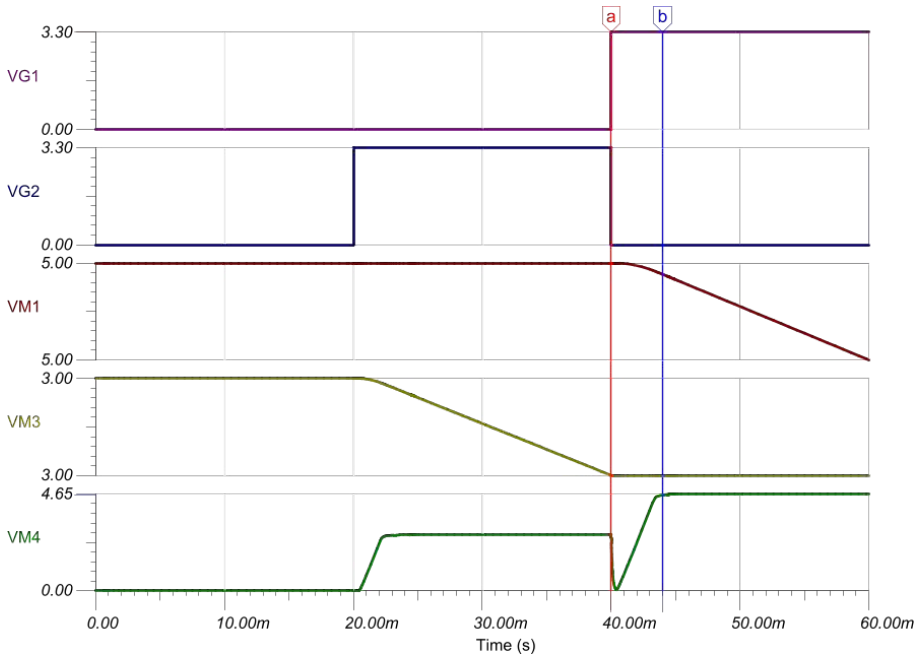


Figure A.21: Simulation for the load switch TPS22918. Its was tested withe a $10Ohm$ load, and it switches from a $3.3V$ to a $5V$ power supply. The enable signal from the tow switches do not overlaps. There is a drop in the output voltage, switch fails to make a smooth transition.

A.3.3 DC/DC Converter - TPS63001

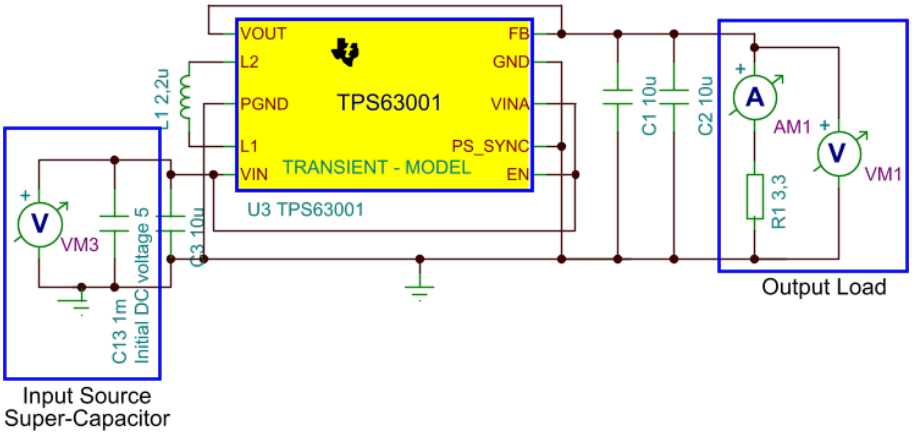


Figure A.22: Circuit for simulating high current DC/DC converter (TPS63001) performance.

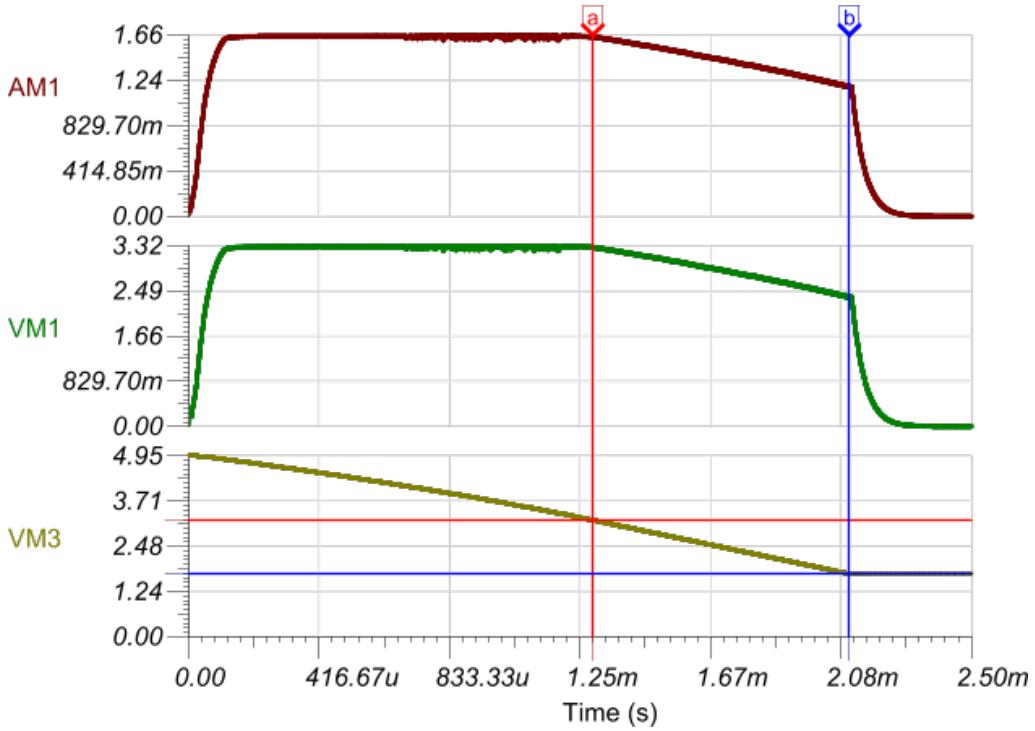


Figure A.23: Simulation for the dc/dc converter TPS6001. The test was done withe $2Ohm$ load, and a supercapacitor withe a $5V$ initial voltage and $1mF$ capacity. The output voltage is $3.3V$. The converter fails to keep the voltage stable for input voltages lower than about $3.3V$.

A.3.4 DC/DC Converter - LTC3531

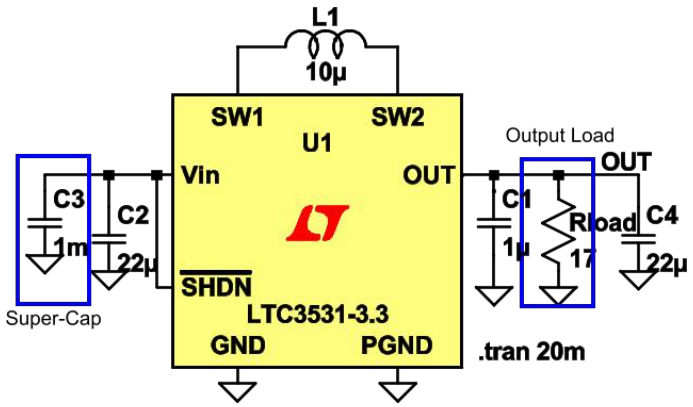


Figure A.24: Circuit for simulating the low current DC/DC converter (LTC3531) performance.

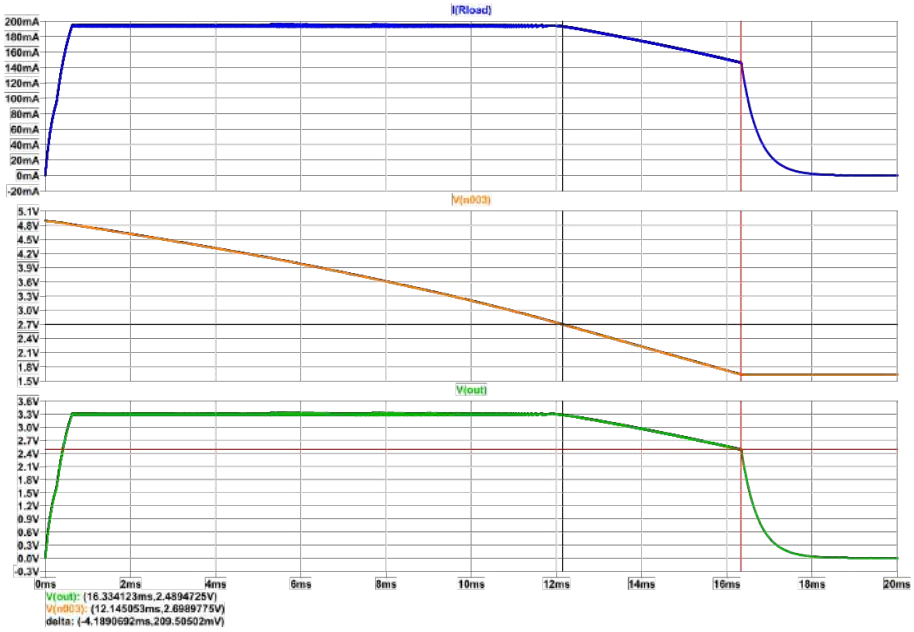


Figure A.25: Simulation for the dc/dc converter LTC3531. The test was done withe $17Ohm$ load, and a supercapacitor withe a $5V$ initial voltage and $1mF$ capacity. The output voltage is $3,3V$. the converter fails to keep the voltage stable for input voltages lower than about $2.8V$.

Appendix B

Rolling Probe

B.1 PCB Circuit & Layout

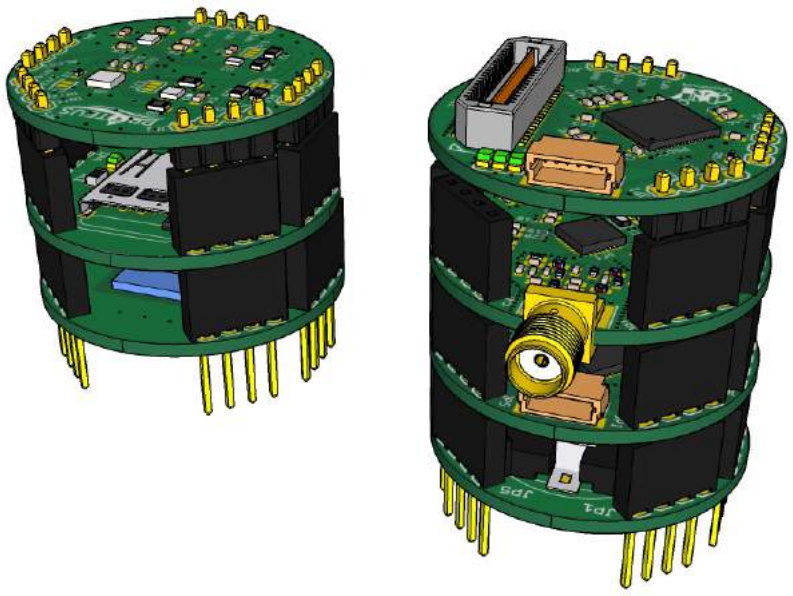
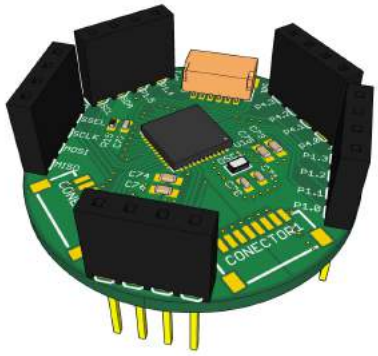
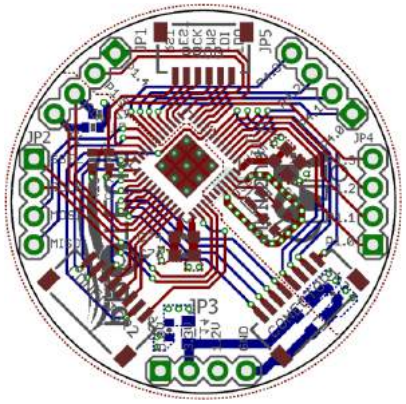


Figure B.1: Final expected result



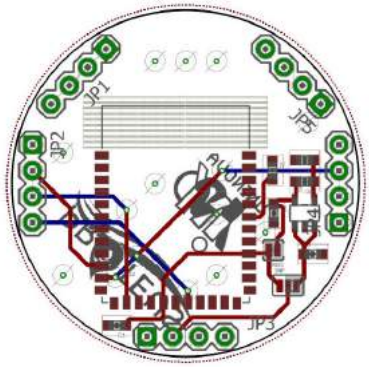
(a) 3D rendering of the board.



(b) Eagle layout implementation of the block.

Figure B.2: Processing unit block, implemented using an MSP430 family device.

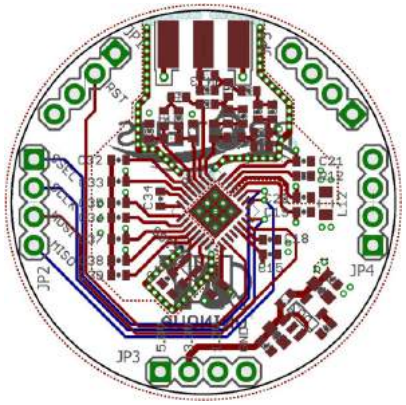
(a) 3D rendering of the board.



(b) Eagle layout implementation of the block.

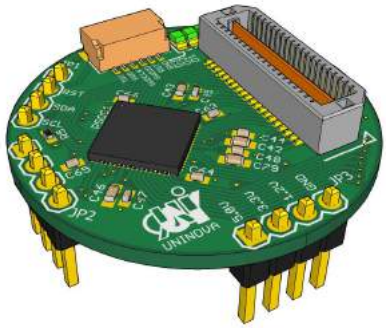
Figure B.3: Communication block, implemented withe a BLE device.

(a) 3D rendering of the board.

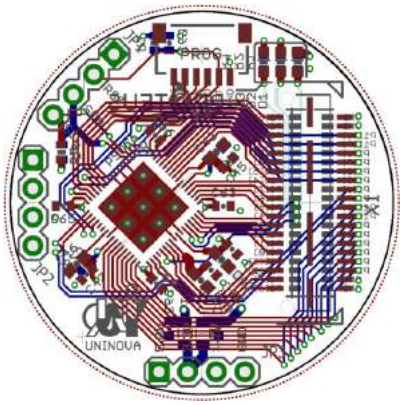


(b) Eagle layout implementation of the block.

Figure B.4: Communication block, implemented withe a UNB device.

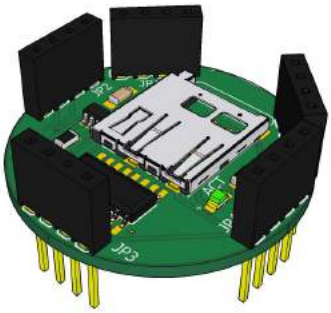


(a) 3D rendering of the board.

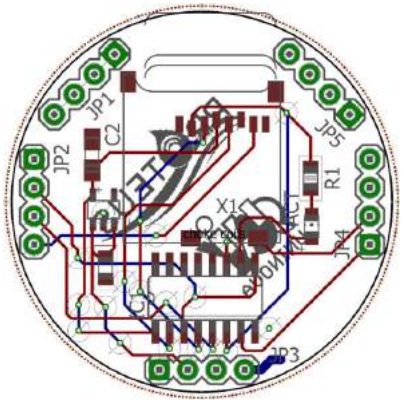


(b) Eagle layout implementation of the block.

Figure B.5: Processing and AFE unit, implemented with PSOC 5.



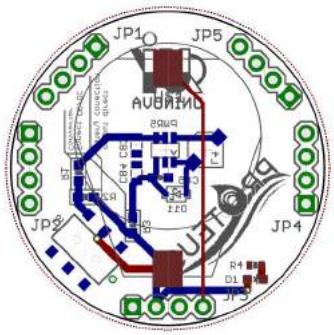
(a) 3D rendering of the board.



(b) Eagle layout implementation of the block.

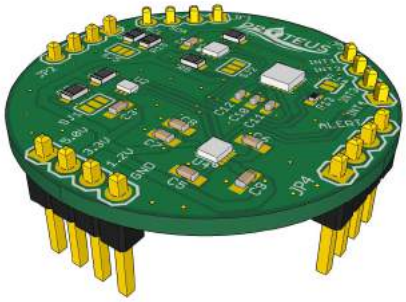
Figure B.6: Data storage unit, implemented withe the use of a SD card.

(a) 3D rendering of the board

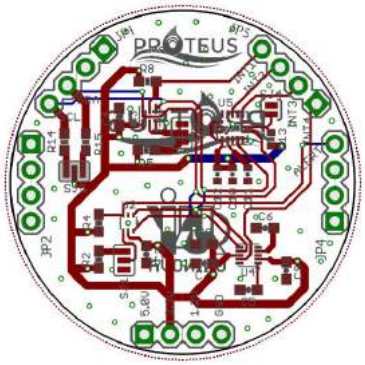


(b) Eagle layout implementation of the block.

Figure B.7: Power unit, implemented using a coin cell and a dc/dc converter.



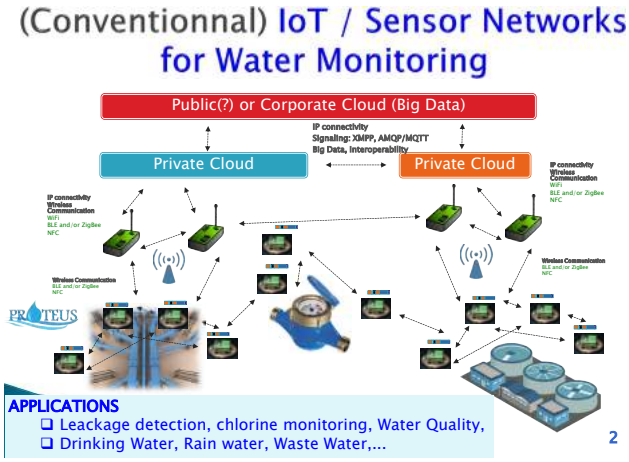
(a) 3D rendering of the board

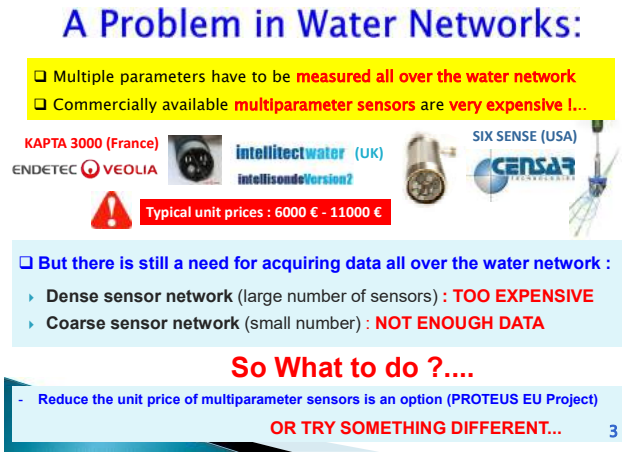


(b) Eagle layout implementation of the block.

Figure B.8: Sensor unit, implemented with a gyroscope, accelerometer, magnetometer temperature, and light sensor.

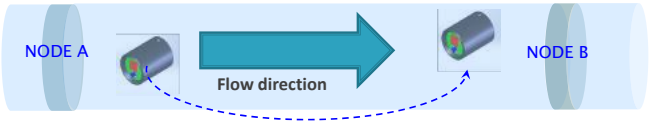
B.2 ICAN Competition





Our solution : The Rolling Water Probe

It can acquire data while surfing over the water network
It can cover the missing regions between 2 nodes of the network

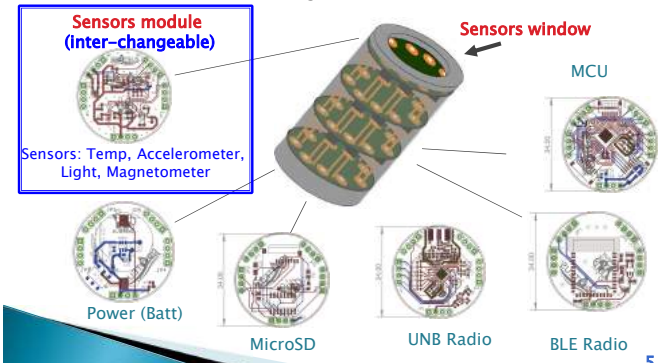


- A Rolling Water Probe travels through the water pipeline network and it measures multiple parameters inside the pipe.
- This is a moving multi parameter sensor that can be used either between fixed locations with sensor nodes or even in a pipe which has no sensors at all
- Data can be either wirelessly transmitted in real time or stored in memory for later analysis

4

First Prototype: The Air Rolling Probe

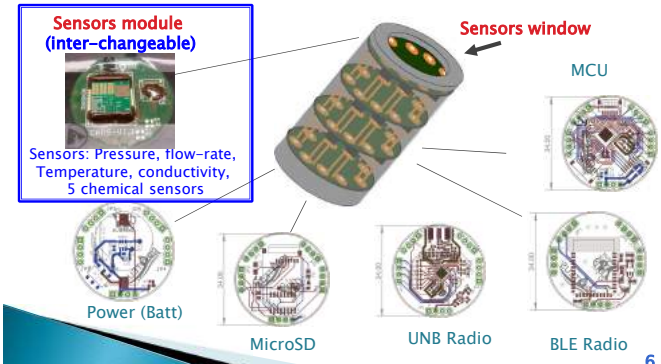
- **Modular structure**, which allows to easy add or remove different , e.g. sensors, communication, storage



5

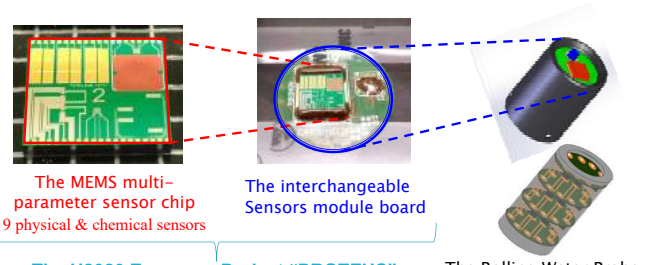
The Rolling Water Probe: Architecture

- **Modular structure**, which allows to easy add or remove different , e.g. sensors, communication, storage



6

The Rolling Water Probe: Content



7

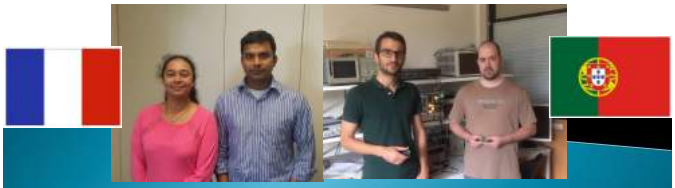
OUR FIRST PROOF OF CONCEPT in AIR PIPES

- Same concept of Rolling Probe can be used in other pipe networks such as the air conditioning networkS
- In this case, our multi-parameter sensor can measure : TEMPERATURE, MAGNETIC FIELD (for acquiring the position), ACCELERATION and LIGHT

8

Come visit Booth B4 and see the Demo !

Thank You !



9

Figure B.9: ICAN Booth for the rolling probe prototype.

Figure B.10: Test setup, for demonstrate the prototype at work. The capsule will pass to an acrylic pipe to simulate the application environment.

Figure B.11: ICAN poster for the rolling probe concept.

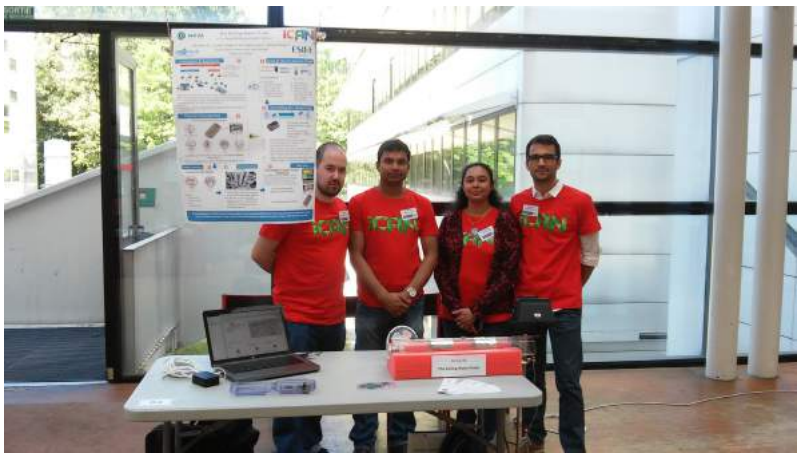


Figure B.12: The rolling probe developer team.

Figure B.13: The rolling probe team withe one of its adviser (Prof. João Oliveira).

Figure B.14: Receiving the prize for second place.

Figure B.15: Second prize award certificate.

APPENDIX C

CADIT - Software Relevant information

C.1 Model Equations Used to Simulate the Transistores

The constantes necessary to implement the model equations were obtained from UMC for the 130nm CMOS technology.

C.1.1 AC Equations

$$gm = \frac{2 \times ID}{VDsat} \tag{C.1a}$$

$$gm_{Triode} = \frac{ID}{(VDsat \times Vds) - \frac{Vds^2}{2}} \times Vds \tag{C.1b}$$

$$gds = \frac{ID}{\mathtt{Cte} \times L} \tag{C.2a}$$

$$gds_{Triode} = \frac{ID}{(VDsat \times Vds) - \frac{Vds^2}{2}} \times (VDsat - Vds) \tag{C.2b}$$

$$gmb = \mathtt{X} \times gm \tag{C.3}$$

C.1.2 Noise Equations

$$\text{Res: } \overline{I_{Termal}}^2 = 4 \times \mathtt{K} \times T \times \frac{1}{R} \tag{C.4}$$

$$\text{MOSfet: } \overline{I_{Termal}}^2 = 4 \times \frac{2}{3} \times \mathtt{K} \times T \times gm \tag{C.5a}$$

$$\overline{I_{Flicker}}^2 = \frac{\mathtt{Kf}}{\mathtt{Cox} \times W \times L \times f^{\mathtt{af}}} \tag{C.5b}$$

C.1.3 Parasitic Equations

$$Cgd = W \times \texttt{CGSD0} \tag{C.6}$$

$$Cgs = \frac{2}{3} \times W^2 \times \texttt{CGOX} \tag{C.7}$$

$$Csb = \frac{W \times (\texttt{Sd}_\texttt{s} + L) \times \texttt{CJN}}{\left(1 - \frac{Vsb}{\texttt{PBN}}\right)^{\texttt{MJN}}} + \frac{(W + \texttt{Sd}_\texttt{s}) \times 2 \times \texttt{CJSWN}}{\left(1 - \frac{Vsb}{\texttt{PBN}}\right)^{\texttt{MJSWN}}} + \frac{2 \times W \times L \times \texttt{CJN}}{3 \times \left(1 - \frac{Vsb}{\texttt{PBN}}\right)^{\texttt{MJN}}} \tag{C.8}$$

$$Cdb = \frac{(W + \texttt{Sd}_\texttt{s}) \times 2 \times \texttt{CJSWN}}{\left(1 + \frac{Vdb}{\texttt{PBN}}\right)^{\texttt{MJSWN}}} + W \times \texttt{Sd}_\texttt{s} \times \frac{\texttt{CJN}}{\left(1 + \frac{Vdb}{\texttt{PBN}}\right)^{\texttt{MJN}}} \tag{C.9}$$

Appendix

Relevant Articles Made by the Author of this Thesis

Analysis of a Noise Canceling LNA Using a Si2 OpenAccess Based Tool - CADIT

João P. Alarcão, Luis B. Oliveira, João P. Oliveira, Rui Santos-Tavares
Centre for Technologies and Systems (CTS) - UNINOVA
Department of Electrical Engineering (DEE), Universidade Nova de Lisboa (UNL)
Caparica, 2829-516, Portugal,
Email: j.alarcao@campus.fct.unl.pt, {l.oliveira, jpao, rmt}@fct.unl.pt

***Abstract*—Noise canceling techniques have been successfully applied to the design of modern multi-band RF-CMOS inductorless receivers. However, low voltage supply requirements are imposing new design challenges which are pushing the operation of the MOS transistor into moderate or weak inversion, making the setup of closed sizing expressions a difficult task. This paper presents a Si2 OpenAccess based circuit analysis tool that can combines a symbolic equation extractor with the transistor parameters obtained from precise models, reinforcing the performance estimation while reducing the design time. The tool is applied for a wide-band Low Noise Amplifier (LNA). The results are validated by comparing them with values obtained from SpectreRF eletrical simulations using a 130 nm CMOS technology.**

***Index Terms*—RF-CMOS, Si2 OpenAccess, CAD, EDA Tool, Weak Inversion, Modified Nodal Analysis.**

I. Introduction

The growing demand for high data rate wireless digital communication and the corresponding level of specifications in terms of noise and bandwidth are increasingly difficult to achieve by modern fully integrated RF transceivers, in standard CMOS technology. It is, therefore, important to develop and reinforce new tools to assist the designers in this task. Previously developed CAD tools are based in electrical simulation, which are precise but require significant processing resources. On the other hand, symbolic circuit analysis has received less attention but it can be employed in early stages of the design process, speeding it up.

In this paper, a Si2 OpenAccess based circuit analysis tool, CAD Interface Tool (CADIT), is presented that combines a symbolic equation extractor with the transistor parameters computed using precise models. By choosing an OpenAccess database format, which is standardized by the Si2 organization [1], CADIT is able to easily interface with other CAD tools.

The paper is structured as follows. In Section II the architecture of the proposed tool CADIT is presented. A design example is presented in Section III, consisting in a noise canceling LNA. In Section IV a comparison between SpectreRF simulations and CADIT is presented. Finally, some conclusions are draw in Section V.

This work was supported by national funds through FCT - Portuguese Foundation for Science and Technology under projects DISRUPTIVE (EXCL/EEI-ELC/0261/2012).

II. CAD Interface Tool Description

CAD Interface Tool (CADIT) automates the process of extraction and evaluation of complex equations for analog circuits: the transfer function (TF); the impedance level (Zin); and the noise figure (NF). The diagram in Fig. 1 presents the architecture of the tool which includes the Si2 OpenAccess (OA) interface to circuit database, the equation extraction module and the user interface. The OA interface provides a standard mechanism to interact with other CAD tools, either commercial or open source tools.

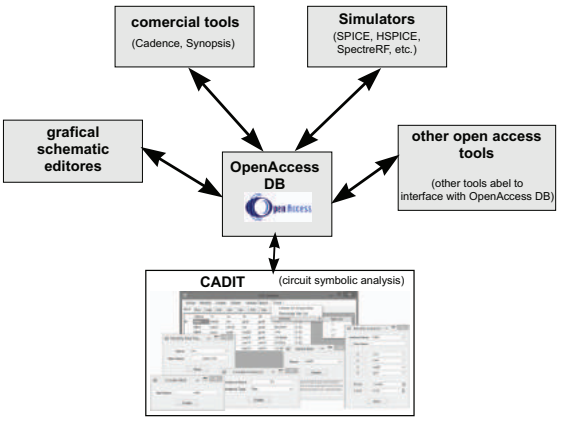


Fig. 1. Main blocks of CADIT tool.

For the equation extraction, CADIT integrates the MSAAC [2] module. This module computes the symbolic node equations using the Modified Nodal Analysis method [3]. In order to obtain the final expressions CADIT combines these nodal equations and the expression required for the transfer function (TF), input impedance (Zin) and noise figure (NF). The resulting equations are then exported to a MATLAB. Figure 2 demonstrates the process of exporting the required expressions, for a circuit stored in the OA database.

A. Equation extraction

CADIT is able to compute the TF, $\frac{v_{out}}{v_{in}}$, the Zin, $\frac{v_{in}}{i_{in}}$, and the NF, (1), for a given circuit. Each expression of Zin and TF are computed on a single interaction with the MSAAC module. On the other hand, the final expression of the NF is

 ISBN 978-83-63578-06-0

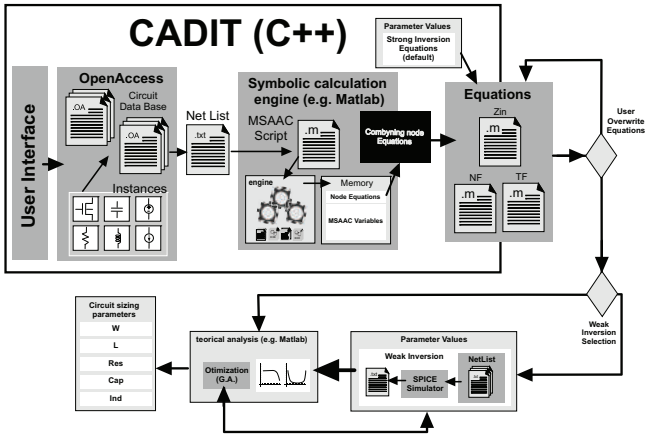


Fig. 2. Computational flow used in circuit analysis.

obtained running the MSAAC module for each noise source by applying the superposition theorem. In (2) the number of loops is given by $K+N$, being N the total number of thermal noise sources (including MOS transistors and resistors) and K the total number of flicker noise sources. Regarding the TF expression, it can be computed both single ended or in differential mode, just by replacing v_{out} and v_{in} by ($v_{out} = vout_+ - vout_-$) and ($v_{in} = vin_+ - vin_-$).

$$NF = 10\,log_{10}\left(1 + \frac{\overline{Vout_{noise}}^2}{\overline{Vout_{RS1noise}}^2}\right) \tag{1}$$

$$\overline{Vout_{noise}}^2 = \sum_{j=1}^{N}\left(\overline{Vout_{Thermal,j}}^2\right) + \sum_{j=1}^{K}\left(\overline{Vout_{Flicker,j}}^2\right) \tag{2a}$$

$N =$ num of MOST + num of resistors, $K =$ num of MOST (2b)

B. Component models

For passive components, the tool integrates ideal models for resistance, capacitors and inductors. However, is it straightforward to extend the MSAAC module to include RF models by using, for example, the model described in [4] in case of inductors and [5] in case of capacitors.

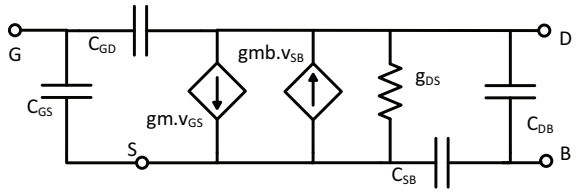


Fig. 3. Transistor small signal model circuit used in CADIT.

Figure 3 shows the equivalent small signal model of a transistor included in CADIT. Table I describes the different model switches available, where md11 represents the simplest version. The most complete version of the model is the md17, depicted in Fig. 3.

TABLE I
ALL, SMALL SIGNAL, MODELS AVAILABLE TO THE USER.

Model Name	gm	gmb	gds	Cgs	Cgd	Cdb	Csb
mdl1	✓						
mdl2	✓		✓				
mdl3	✓	✓	✓				
mdl4	✓		✓	✓			
mdl5	✓		✓	✓	✓		
mdl6	✓	✓	✓	✓	✓	✓	✓
mdl7	✓	✓	✓	✓		✓	✓

Initially, all the expressions (TF, Zin and NF) are computed assuming saturation region in strong inversion (SI) for all the devices. Weak and moderate inversions can be implemented by changing the respective function source code.

Computation resources can limit the use of the most complete version of the model of the transistor, i.e. (`mdl6`). The parasitic capacitance, cgd, of the transistor M2 in the circuit depicted in Fig. 4 originates an expression with multiple terms that consumes a considerable amount of resources.

III. LNA ANALYSIS WITH CADIT

A. LNA description

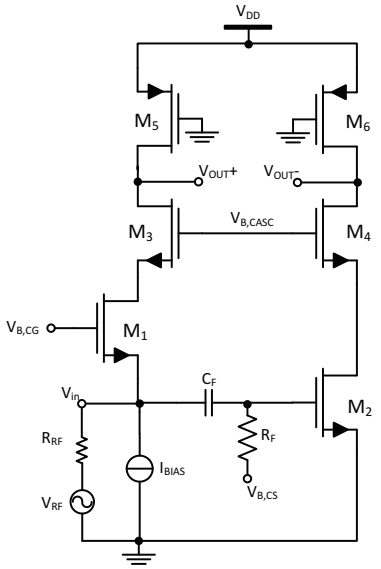


Fig. 4. Noise canceling LNA circuit used to test the tool.

In the LNA circuit shown in Fig. 4 the input signal is applied, simultaneously, to a common gate (CG) and a common source (CS) stages. Using these two transistor configurations, both differential output voltage and cancellation of the noise introduced by CG stage, are achieved. The major noise contribution is from the CS stage.

The operation principle of this circuit is similar to the circuit used in [6] and [7] with an additional cascode transistor. The equations expressed in [6] are used here for a first approach

calculation (gain, Zin, NF), while more precise ones can be obtained from [7].

The main difference between [7] and this work is the cascode transistor and the use of a high-pass filter. The I/V converter is a P-type MOS transistor operating in the triode region. Using transistors instead of resistors as an I/V converter, increases the gain for similar DC biasing. Transistors have a higher AC impedance for the same DC operating point. The transistors in cascode configuration also contributes to increase the overall gain. It is important to note that by introducing more transistors we are introducing more noise sources. However, when their input referred noise contribution are reduced do to the increased gain. A high pass filter (RC filter) is added between the LNA input and the CS configuration transistor, M2, for DC component isolation.

B. CADIT parametric analysis

Parametric analysis is an useful technique to verify the effects of a particular transistor parameter in circuit gain, TF, Zin or NF. Moreover, it provides an intuitive way to understand which parameters impact most the final result.

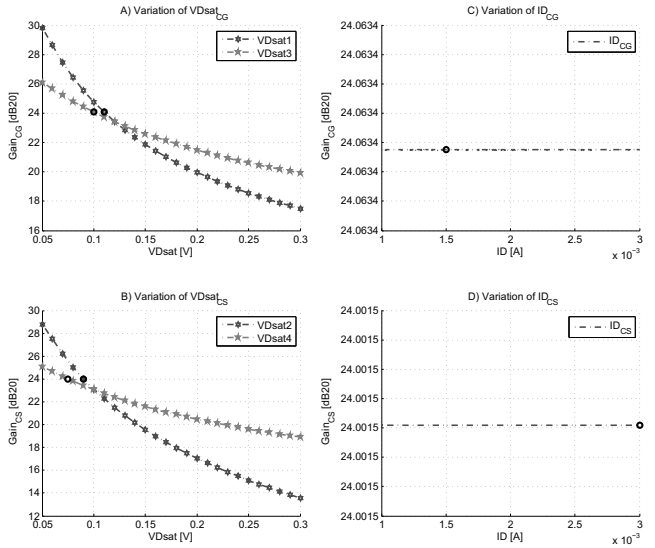


Fig. 5. Gain analysis with respect to design parameters vds_{sat} and ID.

Figures 5, 7 and 6 show the theoretical data of parametric simulations. All circuit parameter variations are done considering the same DC operating point.

The theoretical data presented in this section was obtained using the model `mdl3`, neglecting the effect of the high pass filter in the input CS stage. This means that the expressions do not contain frequency dependent terms. So, for the LNA operating at 1 GHz, one use these simplified model based expressions to estimate the values and variation of the values of TF, Zin and NF.

Figure 7 shows the variation of the NF value in function of vds_{sat} and ID. Similar variation can be found in [6]. Particularly, Fig. 7 show that decreasing the drain current ratio between CG and CS transistors, the NF also decreases.

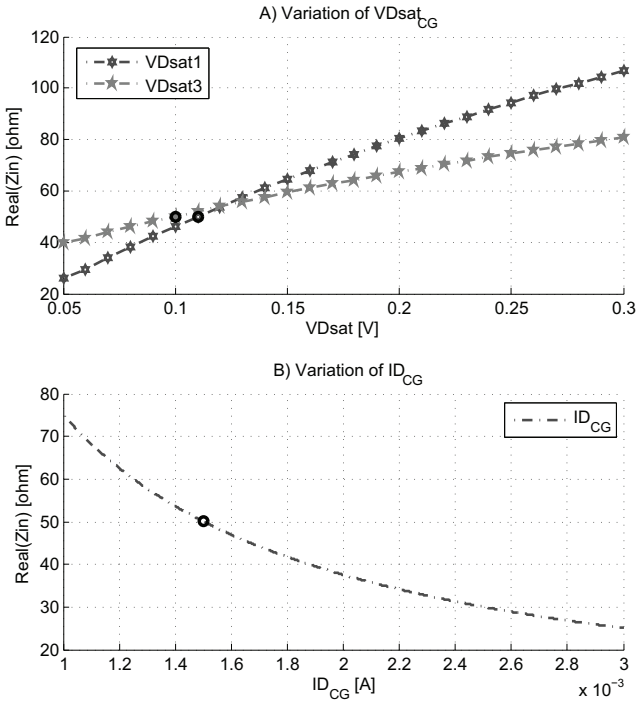


Fig. 6. Zin analysis with respect to design parameters vds_{sat} and ID.

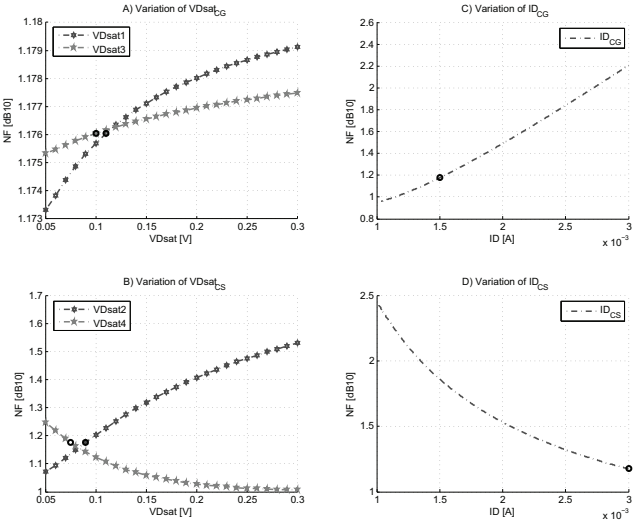


Fig. 7. NF analysis with respect to design parameters vds_{sat} and ID.

IV. CADIT vs SpectreRF Simulations

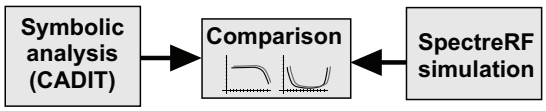


Fig. 8. Setup used for data validation.

In this section, the simulations obtained directly from the equations extracted by CADIT are compared with those results

obtained by SpectreRF simulator using BSIM 3v3 models, using a 130 nm CMOS tecnology.

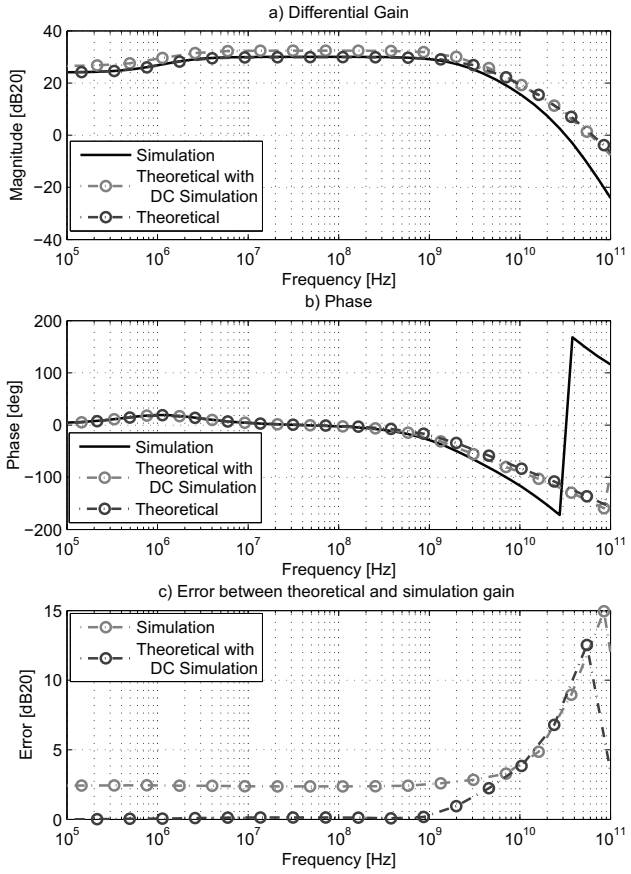


Fig. 9. Theoretical and SpectreRF simulated TF of the LNA shown in Fig. 4, considering a differential output.

Three different curves are displayed: $Theoretical$, $Theoretical\ with\ DC\ simulation$, and $Simulation$. Both type of $Theoretical$ curve values are calculated using the expressions extracted from CADIT. For the first type, an hand calculated DC operating point estimation is used. For the second type, the DC operating is gathered from DC SpectreRF simulation. The third curve, $Simulation$, is obtained from a full SpectreRF simulation. Table II details the bias voltage of each transistor, while Table III shows the DC operating point values for $Theoretical$ and $Theoretical\ with\ DC\ Simulation$ cases. Finally, in Table IV the AC parameters for all transistors as well as their widths are presented for all cases.

TABLE II
THEORETICAL AND SPECTRERF SIMULATED BIAS VOLTAGES

Vbias $[mV]$	**Theoretical**	**Theoretical DC Simulated**	**Simulated**
M1	670	608,26	630
M2	470	426,55	413
M3 & M4	880	872,62	860

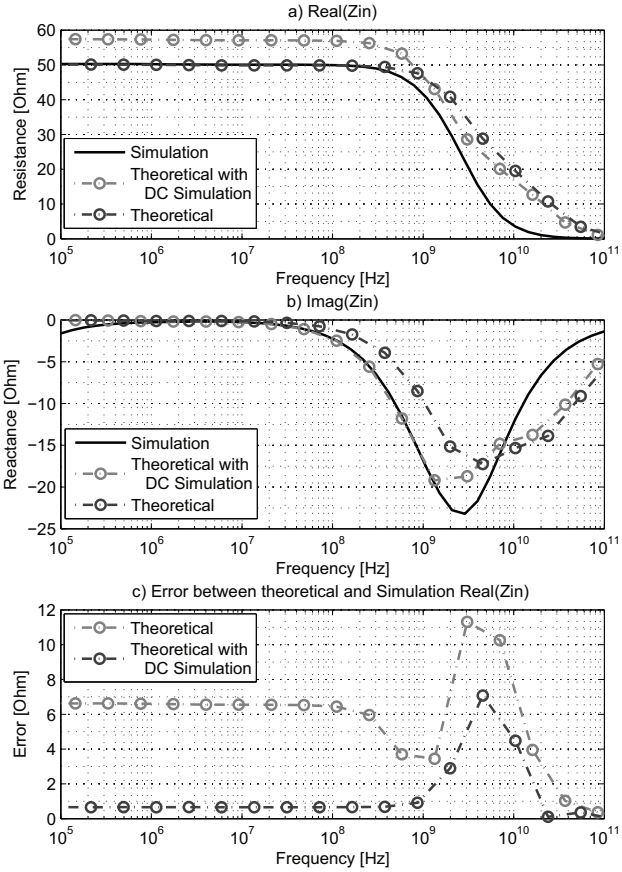


Fig. 10. Theoretical and SpectreRF simulated Zin of the LNA shown in Fig. 4.

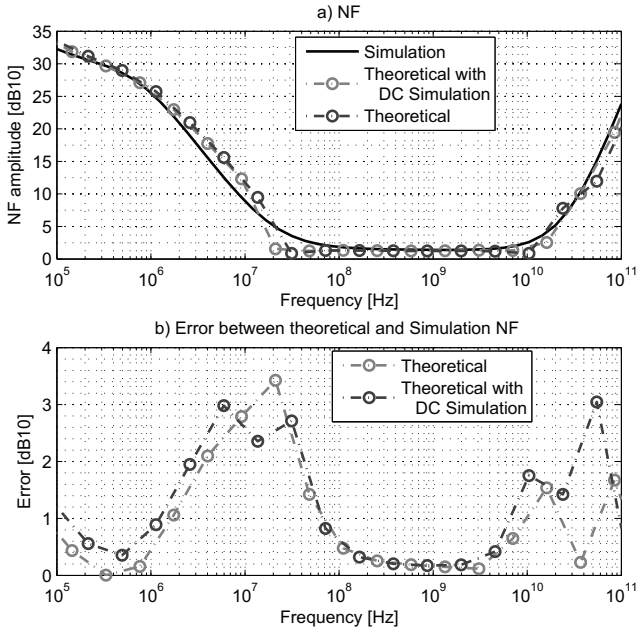


Fig. 11. Theoretical and SpectreRF simulated NF of the LNA shown in Fig. 4.

TABLE III
THEORETICAL AND CADENCE SIMULATED DC NODE VOLTAGES

parameter	M1	M2	M3	M4	M5	M6
Theoretical						
Vds $[mV]$	200	300	200	300	600	600
Vbs $[mV]$	200	0	300	400	0	0
Vdb $[mV]$	300	300	600	600	600	600
gm/gmb	0,15	0	0,15	0,15	0	0
Simulated						
Vds $[mV]$	224,8	415,23	209,91	178,68	604,11	606,1
Vbs $[mV]$	161,184	0	385,98	415,23	0	0
Vdb $[mV]$	385,98	415,23	595,9	593,9	604,11	606,1
gmb/gm	0,08	0	0,07	0.07	0	0

TABLE IV
THEORETICAL AND SIMULATED TRANSISTOR PARAMETERS FOR $Lmin$

parameter	M1	M2	M3	M4	M5	M6
Theoretical						
gm $[mS]$	27,28	66,67	30	80	2,5	5
gds $[mS]$	6,07	12,14	6,07	12,14	1,25	2,5
W $[\mu m]$	59,5	177,78	72	256	5	10
ID $[mA]$	1,5	3	1,5	3	1,5	3
VDsat $[mV]$	110	90	100	75	900	900
Theoretical with simulated DC voltages						
gm $[mS]$	30,62	74,72	32,26	77,58	3,32	6,67
gds $[mS]$	6,07	12,25	6,07	12,25	0,82	1,66
W* $[\mu m]$	75,03	220.65	83,26	238,5	6,59	13,21
ID $[mA]$	1,5	3,03	1,5	3,03	1.5	3,03
VDsat $[mV]$	97,96	81,17	93	78,07	754.16	756,92
Simulated						
gm $[mS]$	20,8	48,96	22,26	52,98	1,91	3,84
gds $[mS]$	2,24	3,8	2,49	5,97	1,24	2,5
W $[\mu m]$	59,5	177,76	72	256	7,2	14,4
ID $[mA]$	1,5	3,03	1,5	3,03	1,5	3,03
VDsat $[mV]$	97,96	81,17	92,99	78,07	754,16	756,92

Figures 9, 10 and 11 show the comparison between the three cases of simulations. For frequencies below 1 GHz, the differences between the Theoretical and the SpectreRF simulation results are small, thus validating the theoretical extracted circuit expressions.

Regarding noise figure performance, the flicker noise dominates at lower frequencies as shown in the results obtained from the $Theoretical$ and $Simulation$ curves. Note that around the operating frequency of the LNA, 1 GHz, the differences are negligible.

TABLE V
SIMULATED CIRCUIT AND MOS DC OPERATING POINT FOR L_{min} IN WEAK INVERSION.

parameter	M1	M2	M3	M4	M5	M6
Vdsat	62.028m	75.673m	64.268m	60.211m	-196.846m	-191.737m
Ids	1.564m	1.083m	1.564m	1.083m	-1.564m	-1.083m
W	921.6u	194.6u	604.8u	604.8u	123u	123u
gds	11.346m	1.678m	2.977m	1.861m	5.631m	9.617m
gm	31.165m	19.791m	31.515m	22.815m	13.155m	7.974m
gmb	1.777m	805.934u	1.991m	1.489m	2.262m	1.39m
Cdb	1.32f	380.155a	1.1f	845.493a	3.487f	3.958f
Cgs	329.972f	85.281f	226.432f	212.748f	80.121f	78.098f
Csb	1.826f	562.801a	1.621f	1.253f	4.95f	5.099f
Cgd	232.816f	47.832f	150.295f	149.688f	17.686f	20.904f

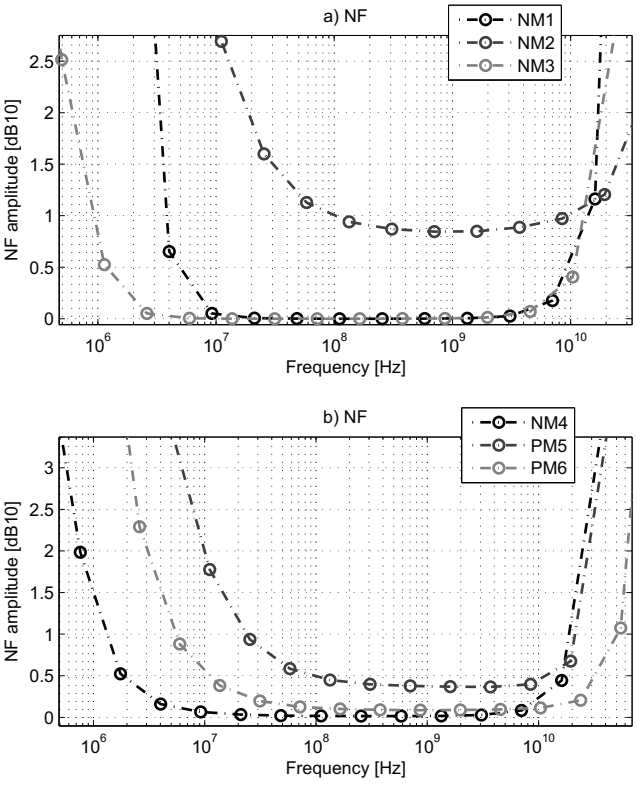


Fig. 12. Influence of each transistor in the NF.

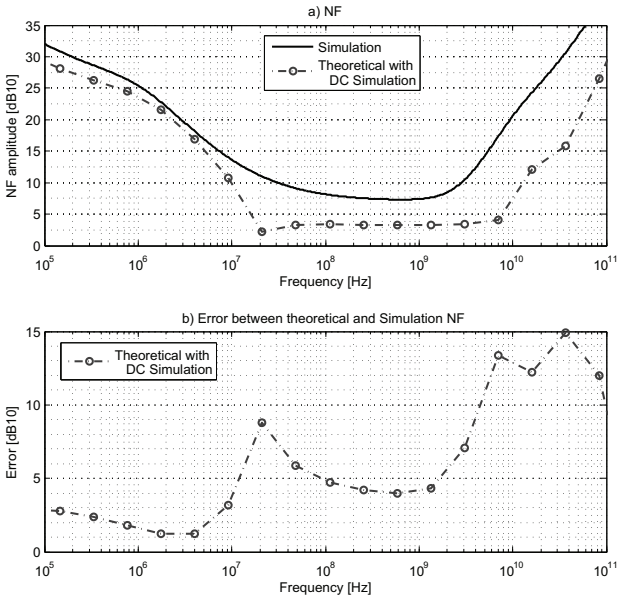


Fig. 13. Noise figure theoretical analysis versus SpectreRF, considering the differential output.

Figure 12 shows the effect of each noise sources. This allows the designer to better understand which transistors have more influence in the NF. For example, it can be observed the significant contribution of transistor M2 on the overall performance, thus validating the initial prediction.

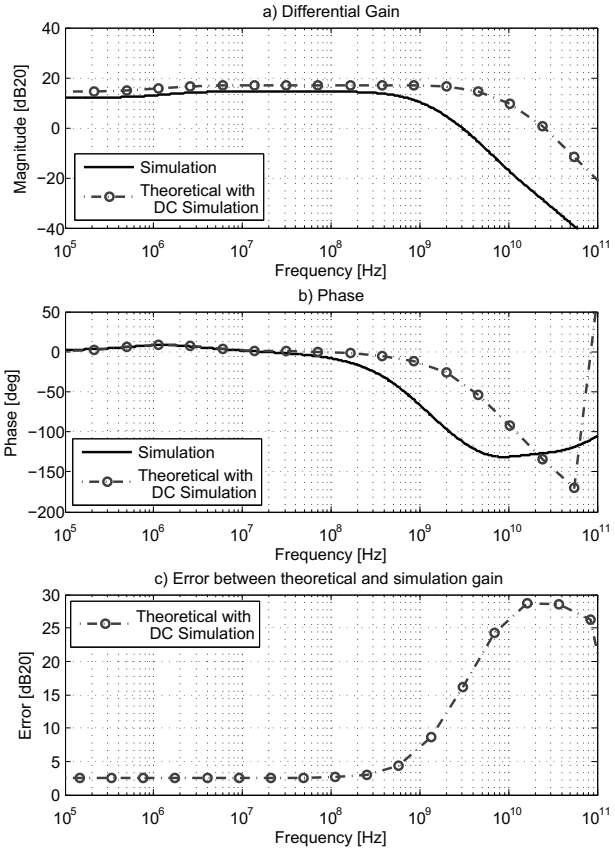


Fig. 14. Transfer function analysis obtained from the theoretical analysis and SpectreRF, considering the differential output.

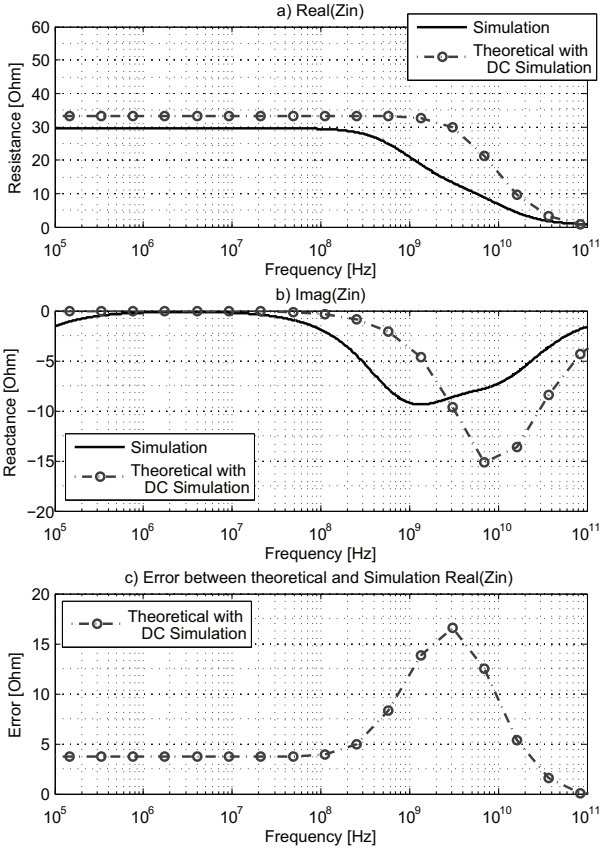


Fig. 15. Input impedance obtained from theoretical analysis and SpectreRF.

Figures 13, 15 and 14 show a theoretical analysis and its comparison with simulated data when the transistors are operating in weak inversion. The transistors used in this simulation are special RF transistors with triple well. Table V presents the transistor DC operating point values used in the theoretical analysis.

It is possible to infer in this example that for higher frequency the small signal model used do not modulate properly the RF transistors. Moreover, it is clear that in the frequency range of the LNA operation it presents a significant difference compared to simulation data. Therefore, one can conclude that a more precise model should be used, as described in [8] and [9].

V. Conclusion

Parametric simulations provide a way to the designer to have a good estimation of the influence of each device in the circuit operation, in terms of NF, Zin, and TF. Moreover, it is independent of the operating region (strong, moderate or weak inversion) of the devices. A circuit analysis software tool was developed to extract the circuit expressions using a standard interface, Si2 OpenAccess. An application example of an LNA was presented. The comparison with SpectreRF simulations using an 130 standard CMOS technology validates the results obtained from the tool.

References

[1] S. S. I. Initiative. Openaccess coalition. [Online]. Available: http://www.si2.org/oac_index.php

[2] E. Santin and F. Gil, "Matlab tool for symbolic analysis of analog circuits - msaac," April 2012. [Online]. Available: https://sites.google.com/site/edineisantin/software-tools

[3] C.-W. Ho, A. E. Ruehli, and P. A. Brennan, "The modified nodal approach to network analysis," *Circuits and Systems, IEEE Transactions on*, vol. 22, no. 6, pp. 504–509, Jun 1975.

[4] J. Long and M. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon rf ic's," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 3, pp. 357–369, Mar 1997.

[5] K. Subramaniam, A. Kordesch, and M. Esa, "Design and modeling of metal finger capacitors for rf applications," in *Applied Electromagnetics, 2005. APACE 2005. Asia-Pacific Conference on*, Dec 2005, pp. 4 pp.–.

[6] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband balun-lna with simultaneous output balancing, noise-canceling and distortion-canceling," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 6, pp. 1341–1350, June 2008.

[7] I. Bastos, L. Oliveira, J. Goes, and M. Silva, "A low power balun lna with active loads for gain and noise figure optimization," *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 3, pp. 693–702, 2014. [Online]. Available: http://dx.doi.org/10.1007/s10470-014-0426-6

[8] C. Enz, "Mos transistor modeling for rf integrated circuit design," in *Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000*, 2000, pp. 189–196.

[9] E. Abou-Allam and T. Manku, "A small-signal mosfet model for radio frequency ic applications," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 16, no. 5, pp. 437–447, May 1997.