Parasitic Effect on Reduced Latency of SoC-Based Big Data

Seyi Stephen Olokede and Babu Sena Paul
Department of Electrical and Electronic Engineering Technology
University of Johannesburg, South Africa
solokede@gmail.com; bspaul@uj.ac.za

Abstract Big data technology sustainability is contingent on the availability of interconnections of large scale, ultra-high-speed, densely integrated big data heterogeneous server platforms. For highly densified servers to be attainable, semiconductors technologies upon which these servers are predicated must further be miniaturized. It is recently not uncommon to implement bandgap reduction engineering of SiGe HBT in a bid to attain highly densified integrated circuit for large scale servers. Unfortunately, the parasitic effects become significant, in particular as these integrated circuits are targeted for high frequency of operations due to the interconnections links between the chip and the transceivers. Insertion loss $|S_{21}|$ becomes considerable, and both the signal level as well as noise figure depreciate substantially as a result. In this work therefore, we investigate the effect of parasitic effect on the roundtrip latency of system-on-chip (SoC).

Keywords: Big data, insertion loss, integrated circuit, latency, parasitic effect, system-on-chip

1 Introduction

The system requirements for big data communication in particular with regards to hardware demands are very stringent. The interconnections of highly densified chips to meet the resources requirements of massive data communications create more rooms for densified fine wire lines with serious challenges between the chip/transceivers, signal traces, and, interconnections. Unfortunately, the side effect of compromising these requirements could result to substantial performance degradation, signal distortion, low speed, and, inability to recover clock-signal components correctly. Transmission losses along the signal traces as well as interconnections are considerable due to discontinuities as a result of bends and junctions along the transmission lines. The parasitic effects of these interconnections cause significant propagation delay as the length and frequency increases with attendant impedance bandwidth degradation. The increase effect of mutual coupling, initiate and propagate surface waves, and thus limit the system efficiency in particular the low speed, signal distortion and inability to recover clock-signal correctly.

This challenge is becoming exacerbated due to increasing need for more highly integrated SoC. The reduced chip size to meet systemic integration capability requirements put more stringent constraints on other ancillary associated circuits. For instance, the bond wire or flip chip needed to interconnect the chip to AoC/AiP is expected to be longer to be effective. Interestingly, longer length of interconnect - in order to accommodate more increasingly densified heterogeneous circuits in a chip - leads to more interconnect delay [1]-[4]. Unfortunately, the present deep submicron is

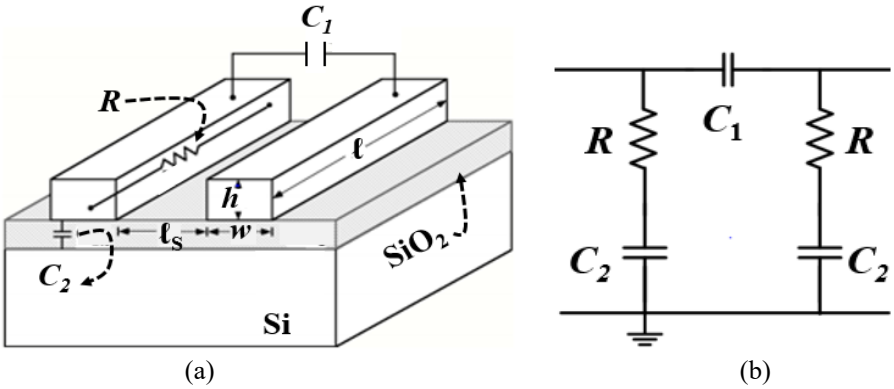
dominated by increasing die size with decreasing wire pitch. The pressure for highly integrated single chip become more sever as the need for interconnections of heterogeneous integration of various technologies into one single chip increases. Research efforts has been ongoing in order to mitigate the SoC delay latency. In 1990, copper-low dielectric interconnects was propounded. However, the overtly longer interconnect delay with attendant systemic performance degradation of the SoC disqualifies the technology. The interconnects scaling is subsequently proposed. The intent of this work however, is in first instance to empirically confirm that delay do exists in SoC due to interconnections, and the delay could cause signal distortion and inability to recover the clock signal. Secondly is to assess the extent of this delay, and specifically, we intend to characterize a typical SoC in order to proffer an approximate estimate for the delay latency.

2 Proposed Interconnect Configuration

In Figure 1, a typical schematic diagram of interconnect of two wires are depicted. In Figure 1(a) is the cross-sectional schematic diagram and Figure 1(b) is the equivalent circuit diagram. The interconnects are photoetched on ungrounded Silicon substrate with dielectric constant of 11.7. Though interconnect wires could be assessed based on being local, global, or semi-local. In this work, we intend to focus our work on the intermediate to global interconnects interconnections.

2.1 Equivalent Circuit Representation and Analysis

Figure 1(b) is the equivalent circuit representation of Figure 1(a). Equations (1) through to (4) are the formulae to determine the various equivalent circuit components of the proposed equivalent circuit, where R is the line resistance of one of the interconnect wire, C_{ox} is the substrate to line capacitance, C_1 is the capacitance between the two interconnect wires, C is the total wire capacitance, k_1, k_2 are the fringing fields to the substrate, and to the air respectively, ε_r is the dielectric constant, and ℓ_s is the feature size, or lithographic resolutions (in $k\lambda$), X_{ox} = oxide



(a) (b)

Figure 1: Interconnect of two wires. (a) Cross-section schematic, (b) Equivalent circuit

$$R = \frac{\ell}{\sigma w h} \tag{1}$$

$$C_1 = \varepsilon_0 \varepsilon_r \frac{\ell h}{\ell_s} \tag{2}$$

$$C_2 = \varepsilon_0 \varepsilon_r \frac{w\ell}{X_{0x}} \tag{3}$$

$$C = k_1 \left(C_1 + C_2 \right) \tag{4}$$

thickness. The total line capacitance is determined by using equation (4). The delay function is as stated in equations (5) and (6) below [5]-[6].

$$\tau_L = 2\rho\varepsilon_0\varepsilon_r \frac{w}{wh}\left(\frac{w}{X_{0x}} + \frac{h}{\ell_s} \right) \tag{5}$$

$$\tau_L = 2R\left(C_1 + C_2 \right) \tag{6}$$

3 Experimental Results

The circuit parameters of Figure 1(b) are extracted using Matlab code. Wire interconnections made of copper and Aluminum with restivities (ρ) of 1.7×10^{-8} Ω.m and 2.82×10^{-8} Ω.m were both examined, with a constant aspect ratio (*h*/*w*). The effect of line to substrate capacitance with respect to delay time (τ_L), the effect of the line width on the resistance of the interconnect wire, and finally, the effect of lithographic resolution on interconnect wire line were examined. Figure 1 depict the dependency of interconnection resistance on the line width. It is evident that the interconnection resistance depreciated with the line width. When this occurs, the feature size (ℓ_s) becomes wider. The capacitance between the two interconnected wires appreciates until there comes a time when the spacing between the two lines becomes too (ℓ_s >>) big with little charges. The capacitance then nosedived. Consequently, the interconnect line thus affect the delay response, as supported by equations (1) and (6). Interestingly, Aluminum interconnection wires respond more abrupt to line width compared with the copper wire. In both, the responses become very steep at an average line width of about 0.9 to 1 μm. Alternatively, the interconnection resistance becomes very high at low line width. The effect of this also impacted on the delay time. In Figure 3, the graph of interconnection length against the lithographic resolution is demonstrated. Findings indicate that the longer the interconnection length the better to use bigger cross sectional area with lower resistivity materials in order to achieve a reduced resistance. Conversely, it may be expedient and beneficial to place smaller length of interconnections in a layer of smaller cross sectional area of higher resistivity materials.

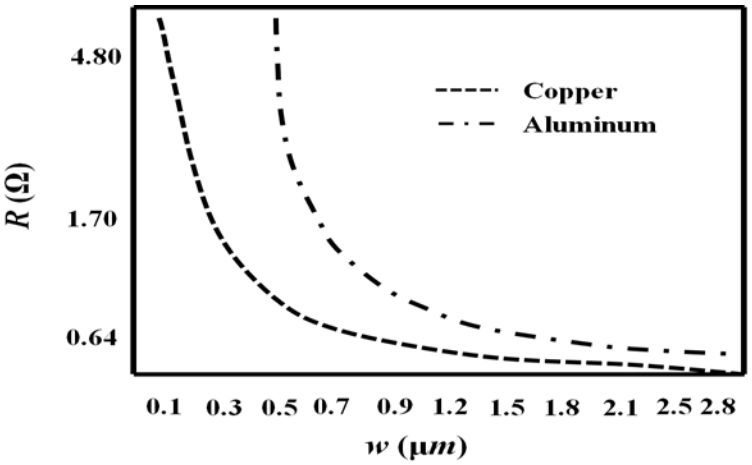


Figure 2: Effect of line width on the resistance of interconnect wire

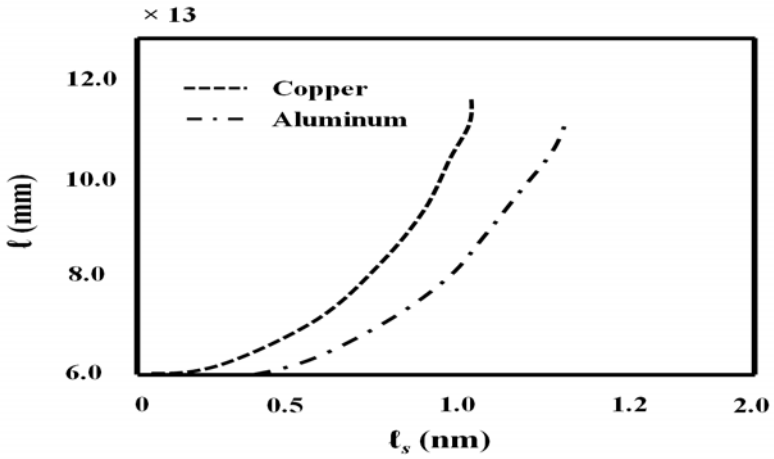


Figure 3: Interconnect length of versus lithographic resolution

In Figure 4, we demonstrate the effect of line to substrate with respect to delay time. Ironically, delay time is directly proportional to line-to-substrate capacitance. The higher the line-to-substrate capacitance the more the delay time. However, abnormality was observed somewhere between 0 - 4 pF where the delay time depreciate before it appreciate again and then steadily. While we do not specifically investigate what could be responsible to this due to exigency, we envisage that this may not be unconnected to the effect of line resistance as the line width becomes too large.

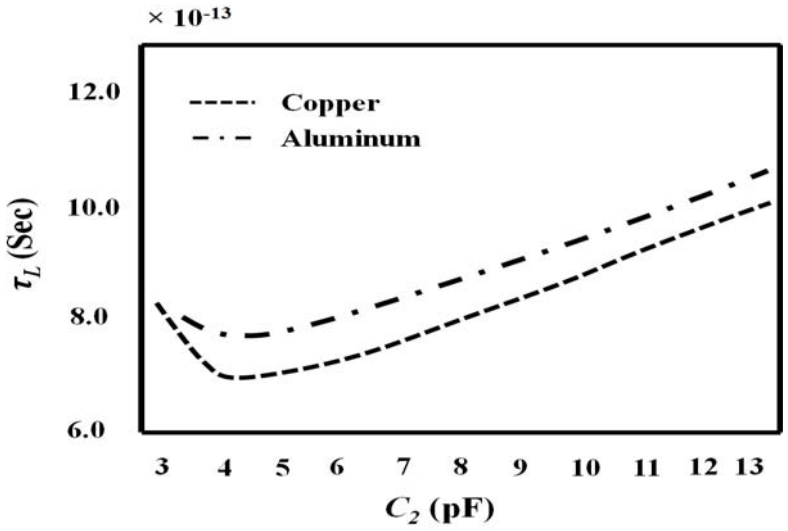


Figure 4: Delay time vs. line to substrate capacitance

Though Figure 5 depicts the effect of chip area with respect to delay time, we specifically draw our observation on both Figure 4 and 5 to underscore our objective of this work. Obviously, the delay time respond to chip area [7]-[8]. Alternatively, the interconnect delay increases with increase of interconnection lengths. By implication, the delay through interconnection length is a larger percentage of the entire model delay time. Therefore, our assertion is that if the interconnect line constitute very significant part of the entire circuit delay as demonstrated by this model which only

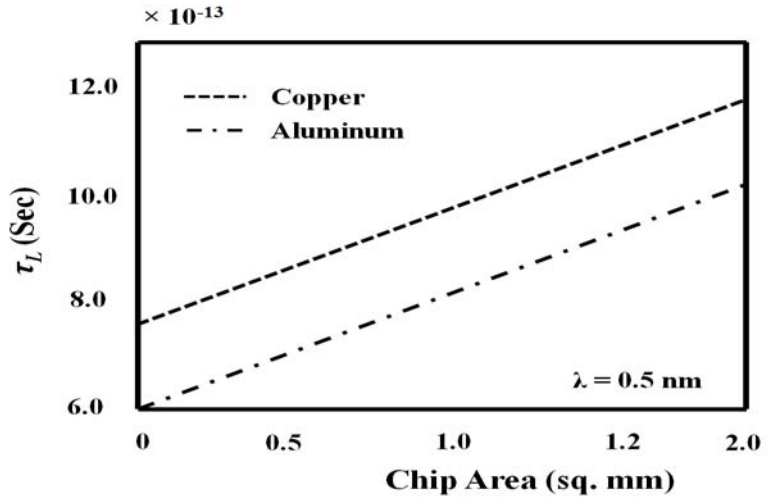


Figure 5: Delay time vs. chip area

focus on two wire interconnect lines, it won't be wrong therefore to infer the magnitude of delay that will be experienced in a highly densified integrated circuit for large-scale servers to provide robust platform for big data [9]. Thus if the delay time is that substantial, signal distortion, transmission losses, surface wave propagation, will depreciate the circuit performance. In turn, there would be no certainty that the transmitted data will be correctly recover due to signal degradation and distortion.

Conclusion

In this paper, we have theoretically investigated the parasitic effect of reduced latency of SoC-based big data. We investigates interconnect of two wires on silicon substrate analytically by drawing the equivalent circuit representation. We extracted the equivalent circuit parasitics and examine its influence on the delay time. The effect of interconnect resistance, line-to-substrate capacitance, and that of capacitance between the two interconnect lines on the delay time were all examined. We conclude that the interconnect wires contribute more than 50% of the delay. By implication therefore, is that if this is to be robust for big data communication, tremendous effort must be put in place to reduce the delay due to interconnection lines. The obvious reason is that, big data will require interconnections of highly densified networks of heterogeneous large scale integrated circuits. It then means this delay will multiply exponentially and the result is that the efficiency will depreciate. The roundtrip latency will severely be affected, and data communication will not be able to be recovered due to signal distortion, the effect of which will worsen as diverse of massive of data is communicated by big data technology.

References

1. Eduardo Abreu, Michael Lightstone, Sanjit K Mitra, and Kaoru Arakawa. (1996). "A new efficient approach for the removal of impulse noise from highly corrupted images," *IEEE Transactions on Image Processing*, 5(6):1012-1025.
2. Oistamo K., Urban J., and Heintz C., (1995). "A highly integrated processor for improved quality television," IEEE Trans. Consumer Electron., 41, 421–428.
3. Hoeneisen B. and Mead C. A., (1972). "Fundamental limitations in microelctronics -I. MOS technology," Solid State Electron., 15, 819-829.
4. Chung J. E., Jeng M. C., Moon J. E., KO P. K., and Hu C., (1990). "Low-voltage hot-electron currents and degradation in deep submicron MOSFET's," IEEE Trans. Electron Devices, 37, 1651-1657.
5. Davari B., Dennard R. H., and Shahidi G. G., (1995). "CMOS scaling for high performance and low power-The next ten years," *Proc. of the IEEE*, 83(4), 595-606
6. Sai-Halasz G. A., (1995). "Performance trends in high-end processors," *Proc. of the IEEE*, 83(1), 20-36.
7. Saraswat K. C., and Mohammadi F., (1982) "Effect of interconnection scaling on time delay of VLSI circuits," *IEEE Trans. Electron Devices*, ED-29, 645-650
8. Rahman A., and Reif R. (2000). "System-level performance evaluation of three-dimensional integrated circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems 8(6), 671 – 678
9. Saraswat K.C., and Mohammadi F. (2005) "Effect of scaling of interconnections on the time delay of VLSI circuits," IEEE Transactions on Electron Devices 29(4), 645 – 650