

CMOS technology for increasing efficiency of clock gating techniques using tri-state buffer

ABSTRACT

Clock gating is an effective technique of decreasing dynamic power dissipation in synchronous design. One of the methods used to realize this goal is to mask the clock which goes to the unnecessary to use in specific time. This paper will present a comparative analysis of this clock gating technique in an 8-bit Arithmetic Logic Unit (ALU). The new clock gating method provides a solution to the problems in the existing techniques. The new proposed clock gating technique generating circuit uses tri-state buffer in a negative latch design, instead of OR gate logic. With the same function being performed, this circuit saves more power and reduces area used, irrespective of design performance. The minimum power gain realized 6.4 % percentage in total power consumption by executing 20 MHz frequency. It also used a 0.9 % occupation area. The proposed method was implemented by using ASIC design methodology, and 130 nm standard cell technology libraries were used for ASIC implementation. Furthermore, the architecture of the ALU was created using Verilog HDL language (32-Bit Quartus II 11.1 Web Edition). The simulation was carried out by using the Model Sim-Altera 10.0c (Quartus II 11.1 Starter Edition). Finally, the design will reduce complexity in hardware and similar clock power.

Keyword: Clock gating; Power dissipation; Dynamic power; Low power; Tri-state techniques; ALU