Influence of Pixel Design on Charge Transfer Performances in CMOS Image Sensors

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Abstract— The influence of pixel design on image lag is investigated by focusing on two different aspects which impact the charge transfer. First, it is confirmed that the transfer gate (TG) channel doping profile strongly affects image lag. Introducing a step under the TG in the potential diagram, due to the doping implant differences in the channel, enables very good transfer performances by limiting spillback of the charge to the photodiode. On the other hand, it is demonstrated that the overlap between the two implants used to create the step can produce a potential barrier under the TG which extension increases the image lag. Then, the influence of pixel layout geometrical parameters (e.g., the photodiode size, the TG length, and the floating diffusion area) on the charge transfer efficiency is clarified. The whole study conclusions allow identifying the design parameter limiting the transfer efficiency in a given design and the possible design-based solutions to improve it.

Index Terms— Charge transfer, CMOS image sensors (CIS), image lag, pinned photodiode (PPD).

I. Introduction

PINNED photodiode (PPD) CMOS image sensors (CIS) are today the main solid-state image sensor technology for commercial cameras and imaging systems, such as digital single-lens reflex and smartphone cameras, as well as for scientific applications, due to their high performances, high integration capabilities, and low power consumption [1]. The charge transfer process is a key performance parameter of PPD CIS. In an ideal situation, all the electrons accumulated in the PPD should be transferred and readout. However, this is not the real situation. PPDs were originally invented for charge-coupled device image sensors [2] and since about two decades they have also been implemented in CIS [3]. Their structure (presented in Fig. 1) allows the transfer of the photogenerated electrons from the PPD to the floating diffusion (FD) node thanks to a transfer gate (TG). An incomplete charge transfer in the pixel leads to image lag, which is a nonideal effect in solid-state image sensors. The charge left in the PPD also

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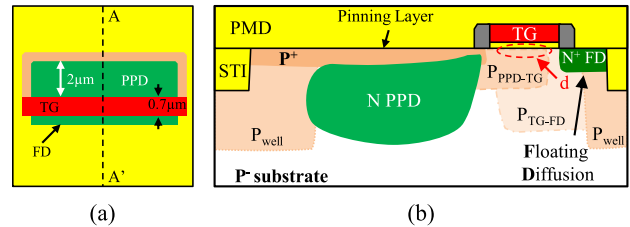
Fig. 1. (a) Layout and (b) schematic cross-sectional ($A - A'$) views of a 4T-PPD-pixel. STI = shallow trench isolation; PMD = premetal dielectric; P_{PPD-TG} = PPD-TG P-doped region; P_{TG-FD} = TG-FD P-doped region; and d = overlap between P_{PPD-TG} and P_{TG-FD}.

causes deterioration in the readout information, in particular, in the cases of bright-to-dark or dark-to-bright transition situations. Finding and mitigating design and fabrication lag sources are a key research access to improve PPD CIS performances [4], especially for dynamic scenes or high-speed imaging.

The understanding of image lag causes and optimization of CIS pixel designs have been widely treated in the literature. Furthermore, diverse papers have been devoted to the evaluation of the PPD, TG, and FD impacts on charge transfer. It has been pointed out several times that the PPD shape has a strong impact on the charge transfer performances [5] since the PPD potential can be engineered to accelerate the electron transfer time in the photodiode. The TG shape and position influence the electron transfer by reducing the electron diffusion path in the PPD [6], whereas the TG doping profile can enhance the electron flux during the transfer [7]. A method to distinguish the image lag cause, between potential barrier, potential pocket, and TG traps, has been developed in [8]. As regards the potential nonidealities, their measurements [9] and the understanding of their location in the transfer path [10] has been a tricky point in the optimization process of lag-free and high-speed sensors. Despite the fact that charge transfer in CIS has been widely investigated, many aspects in the charge transfer limiting mechanisms still remain to clarify, such as the role of the TG doping profile and its correlation with the spill-back phenomenon, or the relative roles of the PPD, TG, and FD designs in the overall transfer performance.

The purpose of this paper is then to further determine the design parameter influence on charge transfer efficiency (CTE) in order to improve the understanding of electron

transfer limiting mechanisms in CIS. The correlation between charge transfer and pinning voltage characteristic measurements enables an in-depth analysis on the influence of several key pixel design parameters, mostly unexplored in the literature, such as the TG channel doping variation and the dimension and position of different TG doping regions. Thanks to the large number of tested structures the TG width and length influence on the electron transfer as well as the existence of charge trapping under the TG are clarified. Moreover, the spill-back and charge partition phenomena are investigated and related to the design variations.

II. Pixel Details and Experimental Procedure

The investigated CIS, constituted of $256 \times 256-$ 7 μm-pitch 4T-PPD pixels [see cross section in Fig. 1(b)], has been designed and manufactured by using a mature 0.18-μm CIS technology. The sensor is divided in different subarrays, with about 2500 identical pixels each. Each pixel is composed by three main components illustrated in Fig. 1: the PPD where the charges are collected, the TG transistor, which allows the electron transfer, and the FD node, the $N+$ doped region where the electrons are transferred by the TG and, then, readout. Three other transistors are also present in each pixel to reset the FD, amplify the signal, and select the pixel [11].

The studied subarrays are divided into two main categories. The first contains pixel variants which differ from each other by the doping profile under the TG, i.e., the presence and the dimensions of a PPD-TG P-doped region (P_{PPD-TG}) and of a TG-FD P-doped region (P_{TG-FD}). The second is composed by pixels which have different design layouts, i.e., with different TG lengths, TG widths, PPD sizes, or FD areas.

Image lag measurements were performed at 22 °C using a LED source at 540 nm to obtain the bright-to-dark transition conditions. For our measurements, the nominal high- and low-TG bias conditions are $V_{HITG} = 3.3$ V and $V_{LOTG} = -0.5$ V, with a transfer time, i.e., the time where TG is in its ON state, of 125 ns. The reset supply voltage, V_{DDRST}, was nominally set at 3.3 V. The image lag is usually [4] determined in terms of CTE or charge transfer inefficiency (CTI = 1-CTE) defined as

$$CTI = 1 - \frac{Q_{OUT}}{Q_{PPD}} \quad (1)$$

where Q_{OUT} is the charge transferred from the PPD to the FD and Q_{PPD} is the charge initially stored in the PPD.

In order to understand the charge transfer mechanism limits and optimization in the studied pixel, the high TG bias levels and the transfer time were varied from 3.5 to 2.1 V and from 40 to 2500 ns, respectively.

Pinning voltage characteristics, which will give useful information about the potential diagram of the PPD-TG-FD structure, were obtained by using the procedure implemented in [12] at the nominal bias conditions (e.g., $V_{HITG} = 3.3$ V, $V_{LOTG} = -0.5$ V, and $V_{DDRST} = 3.3$ V) as well as by varying V_{HITG} from 3.3 to 2.7 V. The following parameters are extracted from the characteristic [12]: the pinning voltage (V_{PIN}, i.e., the maximum PPD channel potential) and the

	P_{PPD-TG}	P_{TG-FD}	OVERLAP d (μm)	CVF[1] (μV/e-)
A	Yes	Yes	0.1	
B	No	Yes	-	
C	Yes	No	-	14
D	No	No	-	

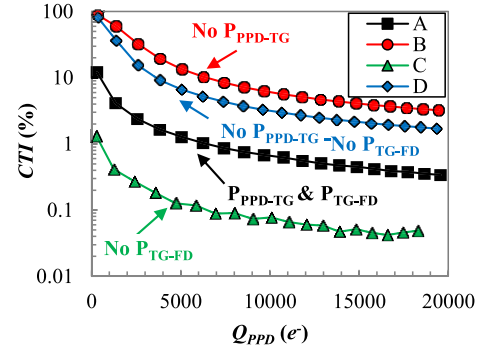[1]Charge to voltage conversion gain, measured

Fig. 2. CTI as a function of the photodiode charge level for pixels A to D.

TG channel potential at which the strong inversion condition occurs, noted $\phi_{TG|inv}$.

III. Transfer Gate Channel Doping Influence on the Charge Transfer

A. Effect of P_{PPD-TG} and P_{TG-FD} on CTI

This section is dedicated to the influence of the TG channel doping on the charge transfer. The examined pixels, the characteristics of which are reported in Table I, have a rectangular PPD area of 2 μm $\times$ 5.7 μm, a TG area of 0.7 μm $\times$ 5.7 μm, and an FD area of 0.3 μm $\times$ 5.7 μm [see Fig. 1(a)]. The pixels from B to D are variants of the pixel A where, the P_{PPD-TG}, the P_{TG-FD}, or both were eliminated.

Fig. 2 reports CTI for pixels from A to D. It can be seen that the transfer performances are strongly dependent on channel doping. The degradation is enhanced when the P_{PPD-TG} (pixels B) or both implants (pixel D) are removed, whereas CTI decreases of one order of magnitude when P_{TG-FD} is eliminated (pixel C).

In order to clarify the P_{PPD-TG} and P_{TG-FD} role in the potential diagram modification and hence its role on lag response, the V_{PIN} characteristics were measured by varying V_{HITG} from its nominal value, 3.3 to 2.7 V. The results are reported in Fig. 3(a), whereas Fig. 3(b) shows the zoomed-in-view of the characteristics highlighting the TG channel inversion condition for the four pixels. It can be observed that, as in the case of lag performances, the shape of the V_{PIN} characteristics is affected by the TG doping profile. Looking at the curves at $V_{HITG} = 3.3$ V (i.e., the dotted lines in Fig. 3) it can be seen that pixels A and C exhibit V_{PIN} characteristics allowing an estimation, as explained in [12], of the maximum PPD channel potential, $V_{PIN} \approx 0.76$ V for both pixels, and of the TG channel potential at which the strong inversion condition is noted, $\phi_{TG|inv} \approx 2.10$ V in
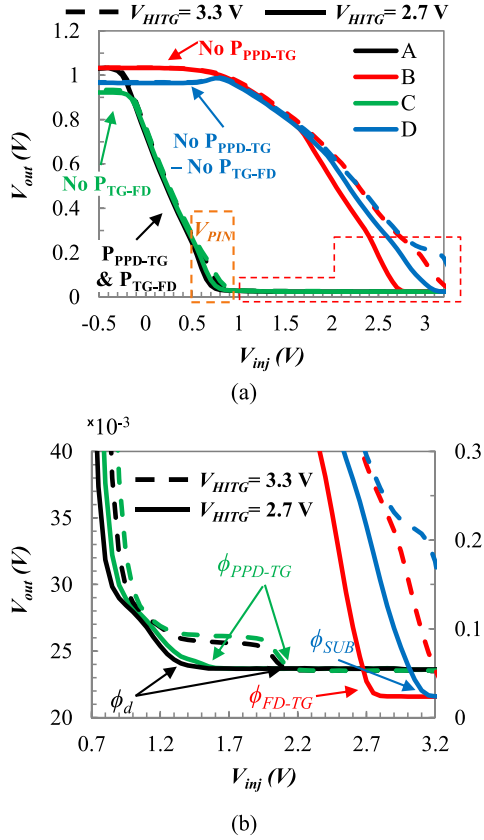
Fig. 3. (a) V_{PIN} characteristic is reported for different TG doping profiles (pixels A–D) at V_{HITG} = 3.3 V (dotted lines) and V_{HITG} = 2.7 V (solid lines). (b) Zoomed-in view of the red rectangle region is reported in order to highlight the inversion condition.

pixel A and $\phi_{TG|inv} \approx 2.15$ V in pixel C. For pixels B and D, the output signal increases with the decreasing of V_{inj}, due to the modifications of the implants under the TG which induce high charge partition at each injection condition.

At $V_{HITG} = 2.7$ V (see solid curves in Fig. 3), there is no noticeable change in the V_{PIN} characteristic for pixels A and C being $V_{PIN} \approx 0.74$ V and the charge partition plateau still present (even if reduced with respect to $V_{HITG} = 3.3$ V). It can be noted that the inversion potential is shifted to lower value due to the decrease of $V_{HITG}(\phi_{TG|inv} \approx 1.60$ V in pixel A and $\phi_{TG|inv} \approx 1.65$ V in pixel C). As regards pixels B and D, at $V_{HITG} = 2.7$ V, it is possible to evaluate the injection condition at which the charges start going into the PPD: 2.8 V in pixel B and 3.2 V in pixel D. This result is very important because it allows the clarification of the potential diagram modifications induced by different TG doping configurations.

First of all, it is possible to conclude that the $\phi_{TG|inv}$ found for pixels A and C is the potential associated with P_{PPD-TG} implant rather than that of P_{TG-FD}. Indeed, it is shown that no modification of the V_{PIN} characteristics are induced from the removing of P_{TG-FD} implant, but that the elimination of P_{PPD-TG} implant leads to the disappearance of the charge partition plateau. Moreover, the slight difference of $\phi_{TG|inv}$ obtained from the curves in Fig. 3 informs that a small potential barrier appears in the middle of the TG due to the overlap of the two implants.
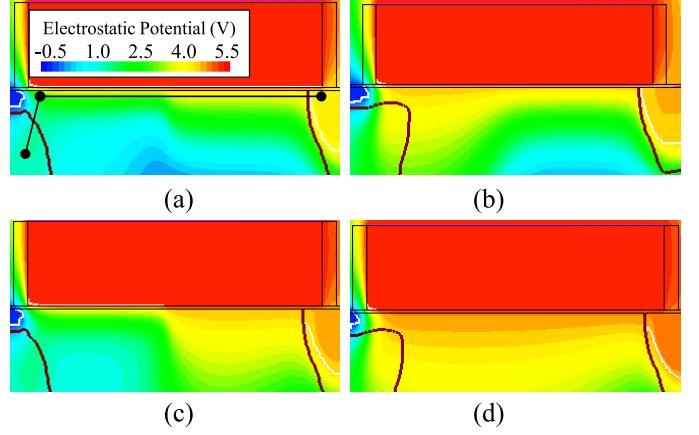

Fig. 4. 2-D TCAD electrostatic potential simulations to illustrate the charge transfer (TG on) limiting or improving mechanisms for pixels (a) with PPPD-TG and PTG-FD, (b) without PPPD-TG, (c) without PTG-FD, and (d) pixel D without PPPD-TG and PTG-FD.
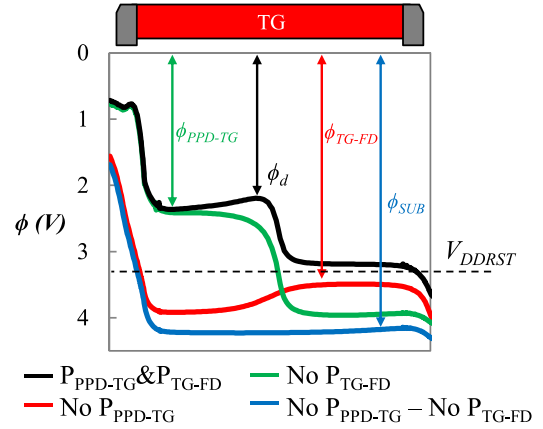

Fig. 5. 1-D TCAD simulation cuts under the TG allowing it to extract ϕ_{PPD-TG}, ϕ_d, and ϕ_{TG-FD}.

Pinning voltage characteristics measured at different V_{HITG} have permitted to estimate the doping concentration of the two implants [12]. TCAD simulations were performed in order to extract the potential diagram of the pixel variants. Fig. 4 reports the 2-D potential in the four pixels. Introducing the P_{PPD-TG} under the TG generates a potential step in the potential diagram, as illustrated in Fig. 4(a) and (c), due to the differences in the doping concentration under the TG [7], [13]. When the PPD-TG implant is removed the step under the TG disappears leading to the creation of a potential pocket [Fig. 4(b)], and to a uniform potential when P_{TG-FD} is also eliminated [Fig. 4(d)]. The relative 1-D potential cuts are reported in Fig. 5. Coupling pinning voltage measurements and TCAD simulations the potential of the PPD-TG implant, $\phi_{PPD-TG} \sim 2.2$ V, and of the $P_{PPD-TG}-P_{TG-FD}$ overlap, $\phi_d \sim 2.1$ V, are estimated.

The differences in CTI observed from Fig. 2 can be explained by the potential diagram modifications induced by the doping profile change (see Figs. 4 and 5). In the case of pixel A, i.e., P_{PPD-TG} and P_{TG-FD}, the presence of the potential step under the TG allows high transfer performances since it prevents the spillback of transferred electrons
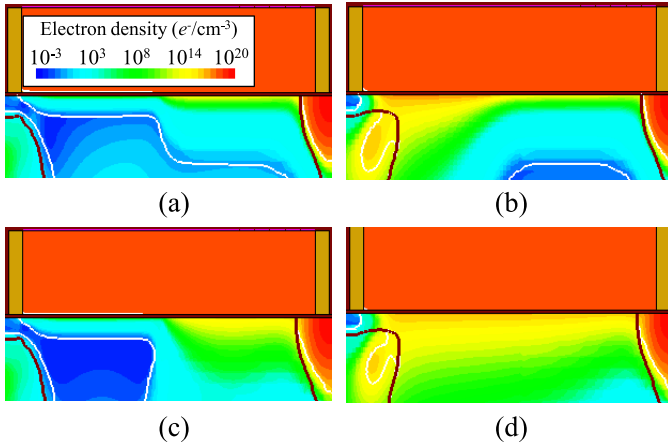
Fig. 6. 2-D TCAD electron density simulations during the TG off switch for pixels (a) with PPPD-TG and PTG-FD, (b) without PPPD-TG, (c) without PTG-FD, and (d) pixel D without PPPD-TG and PTG-FD.
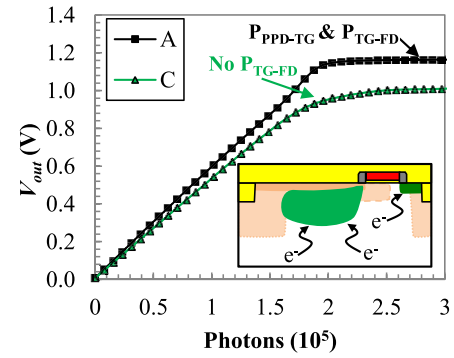

Fig. 7. (a) Optoelectrical transfer function comparison between pixels A and C. (b) Cross-sectional view of pixel C which illustrates that due to the absence of the PTG-FD implant, the electrons can be collected by the sense node directly.
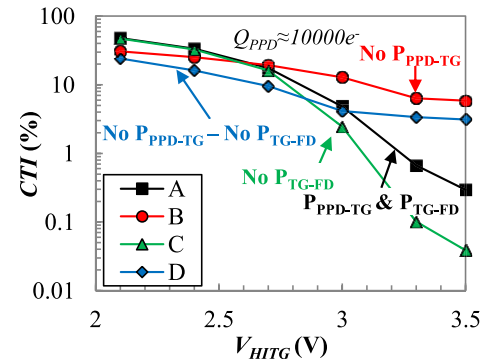

Fig. 8. CTI as a function of V_{HITG} at a fixed $Q_{PPD} \approx 10\,000$ e− for pixels A–D.

(back to the PPD). Indeed, during the charge transfer from PPD to FD, most of signal electrons—the small barrier induced by the overlap may retain a few carriers—do not remain in the first half of the TG channel since a higher electrostatic potential exist in the second half of the TG (near the FD). Then, when the TG is switched in its OFF state, the potential difference between $P_{\mathrm{PPD-TG}}$ and $P_{\mathrm{TG-FD}}$ levels direct the electrons that are in the right half of the TG channel toward the FD and prevent them returning back to the PPD. The antispill-back function of the potential step under the TG is highlighted by TCAD simulation of Fig. 6 where 2-D electron density maps are reported during the switching OFF of the TG MOSFET. It can be observed from Fig. 6(a) that once TG is turning OFF the remaining electrons under the TG are located in the second part of the TG thus preventing the spillback.

Removing the $P_{\mathrm{PPD-TG}}$ [Fig. 4(b)] creates a potential pocket due to the difference of the doping level between the P^{-} substrate and the $P_{\mathrm{TG-FD}}(N_{P-} < N_{\mathrm{PTG-FD}})$. Then, during the transfer (TG ON) a part of the electrons that go toward the FD are trapped in the potential pocket and are sent back to the PPD when the TG is switched OFF as shown in Fig. 6(b).

On the other hand, the absence of the $P_{\mathrm{TG-FD}}$, Fig. 4(c), brings to a situation similar to that of Fig. 4(a): a step in the potential under the gate transfer. In this case, since the $P_{\mathrm{TG-FD}}$ is removed, the potential of the second part of the step is higher than in pixel A, improving the efficiency of the anti-spill-back step, but at the same time the potential barrier due to the overlap is removed, thus enhancing the transfer performances [see Fig. 6(c)]. It is worth noting that the absence of the $P_{\mathrm{TG-FD}}$ leads to a reduction of the quantum efficiency of about 5%, as observed from the optoelectrical transfer function comparison of Fig. 7. (The two pixels have the same charge to voltage conversion gain). Indeed, the absence of the $P_{\mathrm{TG-FD}}$ enhances the collection of the electrons by the FD, thus reducing the quantum efficiency of the PPD (see cross section in Fig. 7). Moreover, it can be noted that the pixels without $P_{\mathrm{TG-FD}}$ have lower saturation voltage. Indeed, the purpose of this implant is to prevent from punchthrough. Consequently,

eliminating $P_{\mathrm{TG-FD}}$ reduces the full well capacity (FWC) of the PPD because of the punchthrough leakage current between PPD and FD when the photodiode is full.

Finally, when both implants are removed [situation of Fig. 4(d)] the step in the potential diagram disappears being the doping profile under the TG uniform. In this case, the electrons that during the transfer are under the gate will go back to the PPD when the TG is switched OFF, thus leading to the deterioration of the charge transfer observed in Fig. 2.

This last result clearly shows that an antispill-back barrier is much more efficient at reducing image lag than having a high potential difference between the PPD and the TG region. Indeed, as highlighted by Fig. 6(d) high spillback occur due to the elimination of the step under the TG.

Fig. 8 displays the measured CTI at a fixed PPD charge level (about $10\,000$ e^{-}) as a function of V_{HITG}. It is observed that for all the pixels the CTI decreases with the increase of V_{HITG}. In the case of pixels without $P_{\mathrm{PPD-TG}}$ or without both implants the charge transfer remains poor due to the spillback mechanisms discussed above. For pixels A and C, it is found again that charge transfer performances are enhanced by removing $P_{\mathrm{TG-FD}}$ implant for $V_{\mathrm{HITG}} > 2.7$ V due to the elimination of the $P_{\mathrm{PPD-TG}} - P_{\mathrm{TG-FD}}$ barrier, whereas the two pixels have the same response for lower high TG bias levels.

Indeed, when V_{HITG} decreases the potential difference between the PPD and $P_{\mathrm{PPD-TG}}$ in the potential diagram

	$P_{\text{PPD-TG}}$	$P_{\text{TG-FD}}$	OVERLAP d (μm)	CVF (μV/e-)
E	Yes	Yes	0.1	14
F	Yes	Yes	0.8	
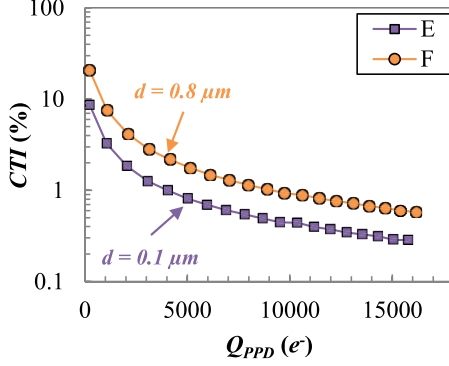
Fig. 9. CTI as a function of the photodiode charge level for pixels E and F.

Fig. 10. Potential diagrams for (a) pixel E with a reduced overlap between $P_{\text{PPD-TG}}$ and $P_{\text{TG-FD}}$ implants and (b) pixel F where the overlap region is increased.

	PPD LENGTH L_{PPD} (μm)	CVF (μV/e-)
A	2	14
G	0.3	13
H	4	14

of Fig. 4(a) and (c) is reduced, thus leading to a reduced efficiency of the antispill-back step. The reduction of PPD-$P_{\text{PPD}-\text{TG}}$ step also brings to the increase of the PPD-TG barrier [14], smoothed for $V_{\text{HITG}} > 2.7$ V, which contribute to the CTI increase displayed in Fig. 8.

B. Effect of the Overlap Between $P_{\text{PPD}-\text{TG}}$ and $P_{\text{TG}-\text{FD}}$

This section is devoted to the influence of the overlap between $P_{\text{PPD}-\text{TG}}$ and $P_{\text{TG}-\text{FD}}$ implants. It has been shown that the presence of these implants under the TG channel is very important for the charge transfer performances since they induce a step in the potential diagram which prevents spillback so improving the transfer efficiency without impacting the others CIS parameters (this is not true if the $P_{\text{TG}-\text{FD}}$ implant is remove as shown above). However, the overlap between these two implants leads to a potential barrier which can play an important role in the charge transfer mechanisms as already mentioned in this paper. In order to clarify the role of the overlap two different pixel variants, the characteristics of which are reported in Table II, has been examined. They have a rectangular PPD area of 2 μm × 5.7 μm, a TG area of 2.1 μm × 5.7 μm, and an FD area of 0.3 μm × 5.7 μm, thus permitting to vary the overlap between $P_{\text{PPD}-\text{TG}}$ and $P_{\text{TG}-\text{FD}}$ under the TG from 0.1 to 0.8 μm.

The CTI as a function of the PPD charge for pixels E and F is reported in Fig. 9. It shows that increasing the overlap region from 0.1 to 0.8 μm degrades the charge transfer performances 8. Extending the overlap between $P_{\text{PPD}-\text{TG}}$ and $P_{\text{TG}-\text{FD}}$ modifies the potential diagram, as illustrated in Fig. 10(a) and (b). Indeed, by doing so, the length and height of the potential barrier are extended, thus leading to a higher amount of charges which could not pass the barrier and that are sent back to the PPD once the TG is switched OFF.

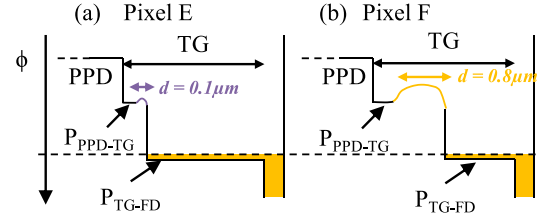As a conclusion for this part, it appears that using two P-doped region to create the antispill-back step is required to achieve high transfer performances and these two P-doping profiles shall overlap to avoid the creation of a potential pocket. Indeed, using only one may reduce the quantum efficiency and the FWC as discussed previously. On the other hand, the overlap region shall stay reasonably small to avoid the retention of signal carriers in the first part of the TG.

IV. INFLUENCE OF THE PIXEL LAYOUT ON THE CHARGE TRANSFER PERFORMANCES

This section is devoted to investigate how different parts of the pixel layout (PPD, TG, and FD) influence the charge transfer. It is divided in three sections which will, respectively, analyze the effect of the PPD size, the TG length, and the FD area.

A. Photodiode Size

At first, the influence of the PPD size on the charge transfer performances has been investigated in order to discriminate between the lag causes in the pixels under study. Indeed, it is known that PPD dimensions are considered as key parameters [6], influencing the PPD-to-FD charge transfer. This is engaged by different mechanisms as the thermal diffusion, which depends on the PPD size, and self-induced drift, which is linked to the PPD electron density [15]–[18]. Thanks to pixels A, G, and H, (see details in Table III) the presence and the impact of these mechanisms have been clarified in order to identify the charge transfer limiting factors in the sensors under study. The pixels have a rectangular PPD which length varies from 0.3 to 4 μm The TG and FD design are the same in the three pixels ($L_{\text{TG}} = 0.7$ μm, $W_{\text{TG}} = 5.7$ μm, $L_{\text{FD}} = 0.3$ μm, and $W_{\text{FD}} = 5.7$ μm).

The comparison of the charge transfer performance as a function of the transfer time in Fig. 11. It can be observed that the image lag is the highest when the PPD is the longest for all the transfer times considered. However, it can be noted from Fig. 11 that, even if the transfer time is not optimized, the CTI decreases with the increasing of transfer time for the
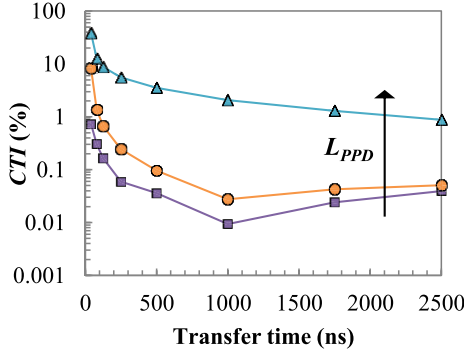
Fig. 11. CTI as a function of the transfer time at a fixed $Q_{PPD} \approx 10\,000\ e^-$.

TABLE IV
LIST OF THE PIXELS' CHARACTERISTICS

	TG LENGTH $L_{TG}\,(\mu m)$	CVF $(\mu V/e\text{-})$
A	0.7	
I	1.4	
J	2.1	14
K	2.7	

longest PPD whereas at time $> 1\ \mu s$ the performances of pixels A and H stabilize. The thermal diffusion inside the photodiode is considered as the limiting mechanism for long PPD: since the diffusion path is longer for longer PPD, the time needed for the photoelectrons to reach the TG is increased. On the other hand, in medium and short PPD transfer performance becomes limited by the other factors discussed previously (i.e., spill-back and potential barriers).

B. Effect of the Transfer Gate Length

The influence of the TG length, L_{TG}, has been studied, thanks to the pixels A, I, J, and K. These pixels have a rectangular PPD ($2\ \mu m \times 5.7\mu m$); the TG is designed to have the same width than PPD and FD (which length is $0.3\ \mu m$); the TG length varies from $0.7\ \mu m$ up to the maximum allowed, $2.7\ \mu m$ (different L_{TG} are reported in Table IV). Fig. 12 displays the results of CTI as a function of the PPD charge. It is observed that the charge transfer decreases with increasing charge in the PPD. Moreover, for the whole range of investigated Q_{PPD}, CTI decreases with increasing L_{TG}. This result can be explained by the fact that, for a given Q_{PPD} amount that is transferred, the longer the L_{TG} the higher the potential difference between PPD and TG (when the TG is ON), thus leading to a better charge transfer, as illustrated in Fig. 13. Moreover, it excludes the phenomenon of charge trapping under the gate due to interface states (mentioned in [4] and [8]) since its presence should lead to a deterioration of the charge transfer which increases with the L_{TG}.

From the V_{PIN} characteristics it was found that the four pixel types have the same $V_{PIN} \approx 0.76$ V and the same $\phi_{TG|inv} \approx 2.10$ V. In between these two potentials (see the inset in Fig. 12), the plateau due to the charge partition regime and the increase due to thermionic emission decrease with
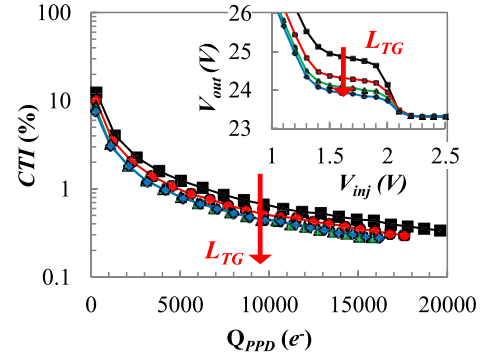

Fig. 12. CTI as a function of the photodiode charge level for pixels A (black squares), I (red circles), J (green triangles), and K (blue diamonds).. Inset: Magnification of the V_{PIN} characteristics to highlight the charge partition and thermionic emission regimes.
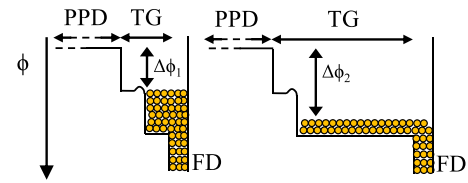

Fig. 13. Potential diagrams to illustrate the influence of the L_{TG} on the charge transfer process.
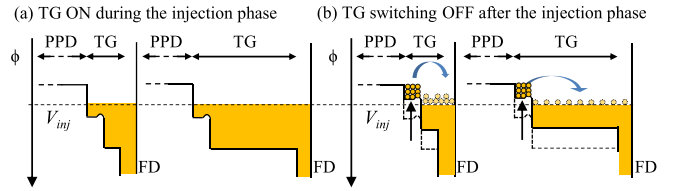

Fig. 14. Potential diagrams for the V_{PIN} measurement during (a) injection phase [12] for pixel A (left) and pixel K (right) and (b) switching off of TG after the injection and before the readout phase, which illustrate the charge partition augmentation with L_{TG}.

the increasing of L_{TG}. This fact can be explained by looking at the potential diagrams represented in Fig. 14. The V_{PIN} measurement consists of one phase, called injection phase, where the V_{DDRST} is lowered to the injection potential, V_{inj}. During this phase, the TG is ON and, as shown in Fig. 14(a), the potential level is not depending on the pixel design since it is set to V_{inj}. For $V_{inj} > \phi_{TG|inv}$, when the injection phase is ended and before the readout phase, the TG is switched OFF and the FD is emptied [12]. In an ideal case, while the TG is rising to its OFF state [see Fig. 14(b)], all the charges go into the FD rather than into the PPD, thus inducing an increase potential level in the P_{TG-FD}-FD region.

This increase is more important for shorter P_{TG-FD}-FD region (this means, in our designs, for shorter TG), thus leading an increase of the charge partition phenomena with L_{TG}, as highlighted from V_{PIN} characteristics.

The charge transfer performances in this pixel family were also investigated by varying the transfer time for a fixed Q_{PPD} charge of about $10\,000$ e−. The results (Fig. 15) show that the CTI decreases with increasing time transfer. Moreover, for transfer time longer than ~100 ns, the longer is the L_{TG}, better
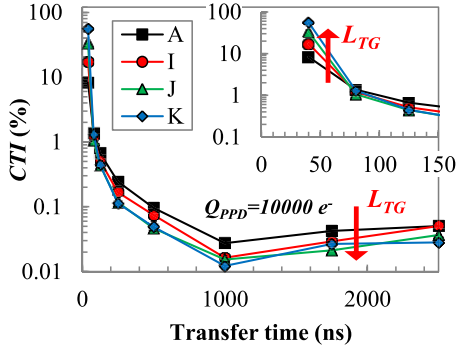
Fig. 15. CTI as a function of the transfer time at a fixed $Q_{PPD} \approx 10\,000$ e−; Inset: Zoomed-in view for transfer times <150 ns to highlight the influence of this parameter on the charge transfer.

are the transfer performances of the pixels. It is observed, however, that this tendency is changed for times shorter than ∼100 ns (see inset in Fig. 15). When the transfer time is decreased, the electrons have not anymore the time to cross the TG and the CTI for the pixel A (the one with the shortest L_{TG}) is the lowest at 40 ns. This result clearly shows that for this particular technology, the transit time in the TG channel is not the limiting factor for transfer time higher than 100 ns. This agrees well with the fact that for the transfer time used in Section III, the limiting mechanism is the spill-back effect and not the transfer time.

C. Transfer Gate Width and Sense Node Area

Finally, this last section is dedicated to the study of the influence of the FD dimensions on charge transfer performances. Four pixel types, which layouts are reported in Fig. 16, are used. These pixels have a rectangular PPD (area = 2 μm × 5.7 μm); the width of the TG and of FD is 2.7 μm for pixels L and M and 1.1 μm for pixels N and O. For each TG (or FD) width two different FD lengths were implemented, or in order to maintain the FD area of about 2 μm^2, for pixels L and N, and to reduce it as in the case of pixels M and O, where the area was 0.9 and 0.3 μm^2, respectively. A summary of these characteristics is reported in Table V.

The results on the charge transfer performances are displayed in Fig. 17 for different levels of charges in the PPD. It can be noted that when the FD area is of about 2 μm^2, the CTI curve has the same behavior for both TG widths. Moreover, the pixels having the smallest W_{TG} exhibit higher image lag for the same PPD charge level. When the FD area is reduced, the spill-back phenomenon appears occurring at a lower charge level for the lower FD area. Indeed, as reported in [14], when the FD is not sized correctly the phenomenon of charge partition may occur thus explaining the higher CTI values obtained at reduced FD areas.

The zoomed-in-view of V_{PIN} characteristics, displayed in the inset of Fig. 17, show that although the pixels have the same $V_{PIN} = 0.76$ V and the same $\phi_{TG|inv} = 2.10$ V the charge partition plateau increases with the decreasing of the FD area due to the decreasing of the P_{TG-FD}-FD region dimensions.
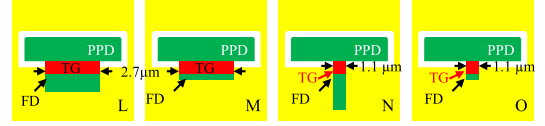

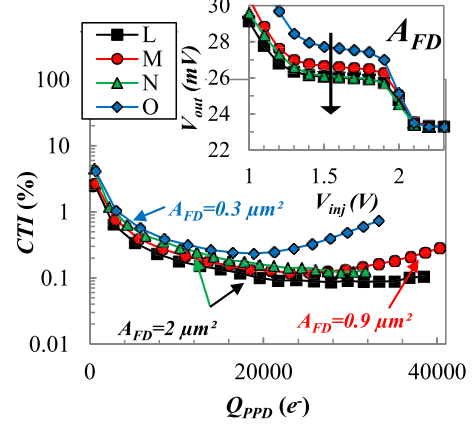Fig. 16. Pixel layouts for the investigation of FD area.

Fig. 17. CTI as a function of the photodiode charge level for pixels L to O.

TABLE V
LIST OF THE PIXELS' CHARACTERISTICS

	TG WIDTH W_{TG} (μm)	FD AREA A_{FD} (μm^2)	CVF ($\mu V/e$-)
L	2.7	1.8	18
M	2.7	0.9	21
N	1.1	2.1	19
O	1.1	0.3	29

V. CONCLUSION

The influence of pixel design on the image lag has been investigated in this paper. Two different aspects have been mainly treated: the TG channel doping profile effect and the influence of TG, photodiode, and FD layout on the charge performances.

Concerning the doping profile influence on image lag, this paper confirmed that introducing a step in the TG channel potential by using two different P implants under the TG improves dramatically the transfer efficiency. This paper clarifies that the main effect of this potential step is to prevent spillback. Moreover, it appears that several possibilities are offered to the designer to build this potential step. Using only one TG implant instead of two leads to the best transfer performances, but it reduces the quantum efficiency by allowing the collection of photogenerated charge by the FD. The overlap between the two TG P-doping profiles used for creating the step is an important parameter because it induces an additional potential barrier under the TG which may enhance image lag. V_{PIN} measurement on this set of pixels has allowed the association of $\phi_{TG|inv}$ potential to the P_{PPD-TG} one.

As regards the different parts of the pixels layout, it has been shown that each of the three main parameters can influence the charge transfer performances.

1) It has been shown that CTI decreases with increasing L_{TG}, thus excluding the phenomenon of charge trapping under the gate as a limiting factor for this technology.

2) It has been confirmed that CTI increases with increasing PPD size because the thermal diffusion in the photodiode becomes the limiting factor in a PPD longer than 4 μm.

3) When the FD area is reduced, the influence of spillback on CTE is enhanced since the FD potential is lowered compared to larger FD (with the same amount of transferred charge).

4) The charge partition phenomena are decreased when the $P_{\text{TG}-\text{FD}}$-FD region dimensions are increased by the modification of at least one between L_{TG} and A_{FD}.

As a conclusion, this paper provides valuable information and clarifications to help PPD CIS designers achieving the best transfer performances or to assess the impact of their design choices on the imager transfer performances.

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