DESIGN OF POWER MANAGEMENT INTEGRATED CIRCUITS AND HIGH-PERFORMANCE ADCS

A Dissertation

by

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ABSTRACT

A battery-powered system has widely expanded its applications to implantable medical devices (IMDs) and portable electronic devices. Since portable devices or IMDs operate in the energy-constrained environment, their low-power operations in combination with efficiently sourcing energy to them are key problems to extend device life. This research proposes novel circuit techniques for two essential functions of a power receiving unit (PRU) in the energy-constrained environment, which are power management and signal processing.

The first part of this dissertation discusses power management integrated circuits for a PRU. From a power management perspective, the most critical two circuit blocks are a front-end rectifier and a battery charger. The front-end CMOS active rectifier converts transmitted AC power into DC power. High power conversion efficiency (PCE) is required to reduce power loss during the power transfer, and high voltage conversion ratio (VCR) is required for the rectifier to enable low-voltage operations. The proposed 13.56-MHz CMOS active rectifier presents low-power circuit techniques for comparators and controllers to reduce increasing power loss of an active diode with offset/delay calibration. It is implemented with 5-V devices of a 0.35 μm CMOS process to support high voltage. A peak PCE of 89.0%, a peak VCR of 90.1%, and a maximum output power of 126.7 mW are measured for 200Ω loading.

The linear battery charger stores the converted DC power into a battery. Since even small power saving can be enough to run the low-power PRU, a battery charger with low I_{Q} is desirable. The presented battery charger is based on a single amplifier for regulation and the charging phase transition from the constant-current (CC) phase to the constant-voltage (CV) phase. The proposed unified amplifier is based on stacked differential pairs which share the bias current. Its current-steering property removes multiple amplifiers for regulation and the CC-CV transition, and achieves high unity-gain loop bandwidth for fast regulation. The charger with the maximum charging current of 25 mA is implemented in 0.35 μm CMOS. A peak charger efficiency of 94% and average charger efficiency of 88% are achieved with an 80-mAh Li-ion polymer battery.

The second part of this dissertation focuses on analog-to-digital converters (ADCs). From a signal processing perspective, an ADC is one of the most important circuit blocks in the PRU. Hence, an energy-efficient ADC is essential in the energy-constrained environment. A pipelined-successive approximation register (SAR) ADC has good energy efficiency in a design space of moderate-to-high speeds and resolutions. Process-Voltage-Temperature variations of a dynamic amplifier in the pipelined-SAR ADC is a key design issue. This research presents two dynamic amplifier architectures for temperature compensation. One is based on a voltage-to-time converter (VTC) and a time-to-voltage converter (TVC), and the other is based on a temperature-dependent common-mode detector. The former amplifier is adopted in a 13-bit 10-50 MS/s subranging pipelined-SAR ADC fabricated in 0.13-μm CMOS. The ADC can operate under the power supply voltage of 0.8-1.2 V. Figure-of-Merits (FoMs) of 4-11.3 fJ/conversion-step are achieved. The latter amplifier is also implemented in 0.13-μm CMOS, consuming 0.11 mW at 50 MS/s. Its measured gain variation is 2.1% across the temperature range of -20 °C to 85 °C.

DEDICATION

Be strong and courageous.

Do not be afraid; do not be discouraged,

for the Lord your God will be with you wherever you go.

Joshua 1:9

To God, who enables me to finish a long journey.

To my parents, who always love and pray for me.

To my wife, Inhye Ahn, who endures a long journey with me.

To my son, Philip Jaeho Noh, who gives me great joy.

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Chapter 2 is based on a published paper co-authored with Judy Amanor-Boadu and Minglei Zhang of the Department of Electrical and Computer Engineering. Chapter 3 is based on a published paper co-authored with Minglei Zhang of the Department of Electrical and Computer Engineering. Chapter 4 and Chapter 5 are based on published papers co-authored with Minglei Zhang of the Department of Electrical and Computer Engineering and Xiaohua Fan of the Univerisity of Chinese Academy of Sciences.

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NOMENCLATURE

ADC	Analog-to-Digital Converter
CC	Constant Current
CDAC	Capacitor DAC
CM	Current Mode or Common Mode
CV	Constant Voltage
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
ENOB	Effective Number of Bit
FFT	Fast Fourier Transform
FoM	Figure of Merit
IC	Integrated Circuit
IMD	Implantable Medical Device
INL	Integral Non-Linearity
ISSCC	International Solid-State Circuits Conference
LSB	Least Significant Bit
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PCE	Power Conversion Efficiency
PMIC	Power Management Integrated Circuit
PRU	Power Receiving Unit
PSD	Power Spectral Density
PTU	Power Transmitting Unit

PVT	Process Voltage Temperature
RX	Receiver
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise+Distortion Ratio
SOC	State of Charge
SOVC	Symposium On VLSI Circuits
TC	Trickle Current
THD	Total Harmonic Distortion
TVC	Time-to-Voltage Converter
TX	Transmitter
VCR	Voltage Conversion Ratio
VM	Voltage Mode
VTC	Voltage-to-Time Converter
WPT	Wireless Power Transfer
ZCD	Zero-Crossing Detector

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1. INTRODUCTION

1.1 Motivation

A battery-powered system has widely expanded its applications to implantable medical devices (IMDs) and portable electronic devices. Recently, it has been studied together with an energy harvesting system to harness ambient energy [1]. The first IMD with an implantable battery was a battery-powered pacemaker inserted into a patient in Sweden in 1958 [2]. Since then, several types of IMDs have entered the clinic—including pacemakers, cochlear implants, and deep brain stimulators—improving the quality and longevity of human lives. Likewise, advancement of portable electronic devices like laptops and smart phones have facilitated ubiquitous computing and user-friendly interfaces, aided by high-resolution displays used in these devices. Fig. 1.1 shows an example of a neural recording and stimulation system [3, 4]. From a probe array, weak neural signals are sensed, amplified, and digitized in an analog front-end block. Also, electrical or optical stimulation signals are generated by a digital-to-analog converter (DAC). Since the system is located in the isolated environment, power management of the system is critical. Energy can be sourced by wireless power transfer [5] or energy harvesting [1]. A battery charger stores redundant energy in a battery [6]. Wireless data communication block can be embedded, too.

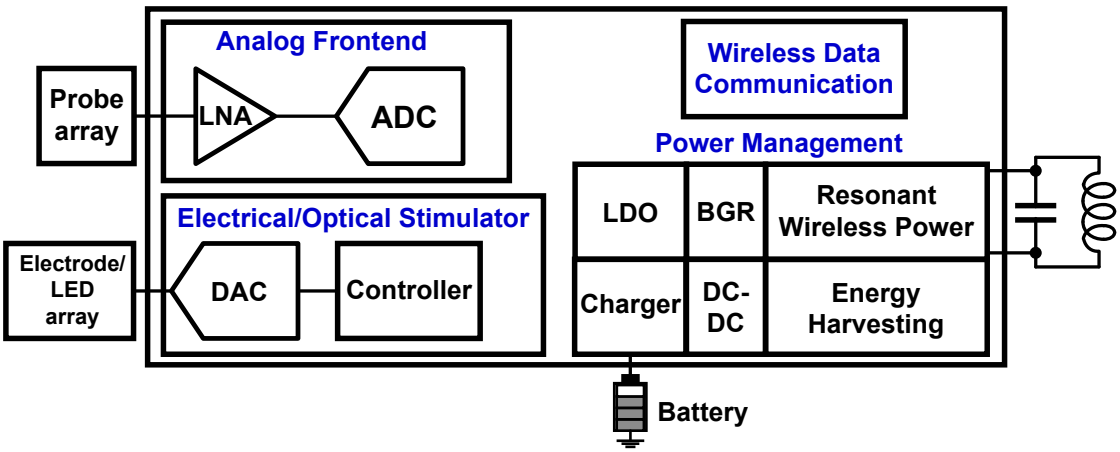
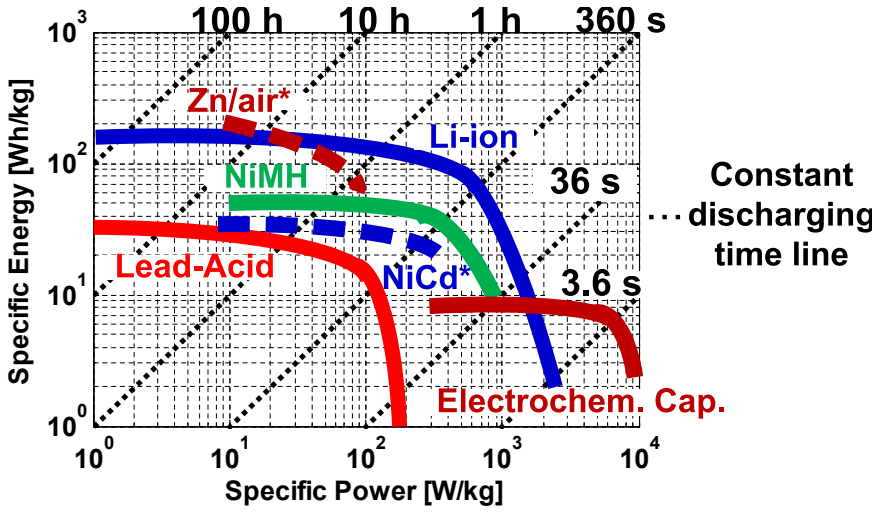


Figure 1.1: An example of a neural recording and stimulation system.



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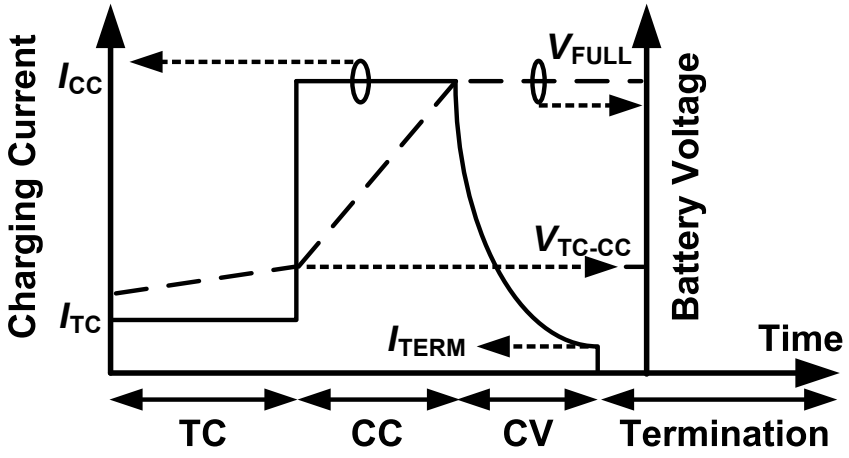


(b)

Figure 1.2: Li-ion battery's (a) Ragone plot and (b) CC-CV charging profile.

While specific requirements for batteries vary according to applications, an ideal battery for any of the applications should have high energy density and high specific energy to reduce volume and weight. The size constraint of IMDs, however, limits the use of batteries with high energy capacity; hence, conventional IMDs require frequent battery replacements. Portable electronic devices confront a similar challenge due to device portability limiting the battery size and making it difficult to meet the high-power demand of high-resolution displays. In this regard, a lithium-ion (Li-ion) battery is a good fit for these applications due to its high energy density and high specific energy. Fig. 1.2(a) shows a Ragone plot [7] for various energy storage devices. Based on data

collected from [8] and [9], the plot shows that a Li-ion battery is superior to competitors over a wide range of discharging time in terms of specific energy, whereas a capacitor is superior for short-time discharging.

As a fast and stable charging technique for a Li-ion battery, constant current (CC) - constant voltage (CV) charging is popular [10]. Fig. 1.2(b) shows a typical charging profile of a CC-CV battery charging algorithm. Initially, trickle-current (TC) charging is necessary for a deeply discharged battery. This is because equivalent series resistance (ESR) of the discharged battery is large, and high current through large ESR can generate excessive heat leading to a loss of capacity. Charging current in the TC phase, I_{TC}, is typically no more than 0.1 C [11]. Once the battery voltage is larger than threshold voltage $V_{\text{TC-CC}}$ ranging from 2.5 V to 3 V [11, 12], the TC phase is switched to the CC phase to speed up the charging process. Charging current in the CC phase, I_{CC}, is typically 0.2 C to 1 C [10, 11]. As the battery voltage approximates the maximum charging voltage V_{FULL} (4.1 V-4.2 V), the CC phase is switched to the CV phase for precise regulation of battery voltage. Note that CV regulation for the CV phase requires high precision for battery safety and health, whereas CC regulation for the TC/CC phases does not [10]. The whole charging process is terminated when the charging current is less than I_{TERM} which is 0.025 C-0.05 C [13, 14] or 10% of the maximum charging current [15].

In summary, a Li-ion battery can be the optimal energy storage device for a battery-powered system, and the CC-CV charging algorithm is popular for fast charging. However, we have not answered a critical question: how do we get and process the energy to charge the battery? Conventionally, a battery-powered system is charged through a battery power cord. To cut the last cord, wireless power transfer (WPT) techniques were actively investigated recently along with the emerging applications such as neural recording and stimulating systems [16], an intraocular pressure sensor [17], and a non-contact memory card [18]. A key design issue in WPT is how efficiently the energy is transferred, and a solution to the design problem lies in rectifier design with high power conversion efficiency (PCE) and high voltage conversion ration (VCR), which are

defined as

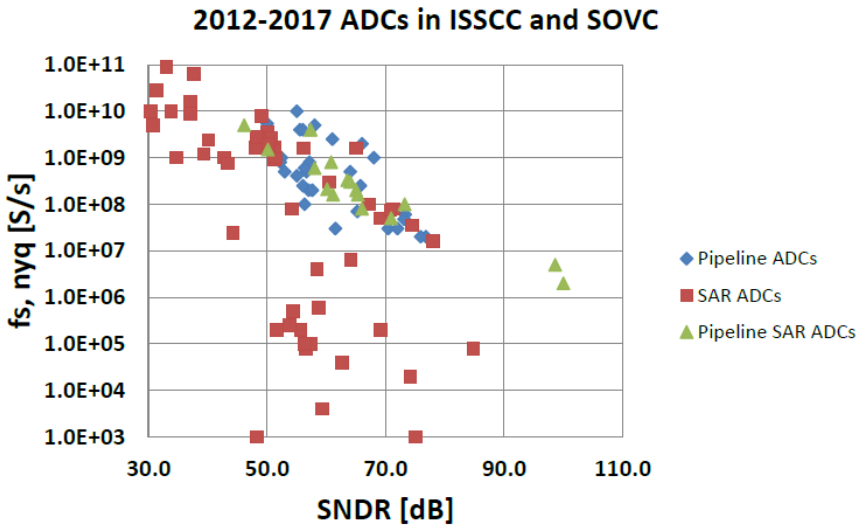
$$\text{PCE} = \frac{P_{\text{LOAD}}}{P_{\text{IN}}} \tag{1.1}$$

$$\text{VCR} = \frac{V_{\text{DC}}}{V_{\text{AC}}} \tag{1.2}$$

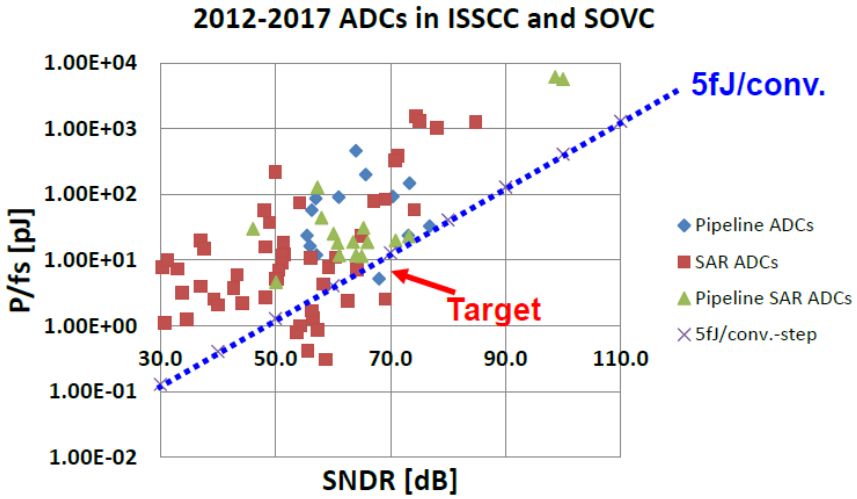
where P_{LOAD}, P_{IN}, V_{DC}, and V_{AC} are rectifier output load power, rectifier input power, rectifier output DC voltage, and a rectifier input AC voltage amplitude.

To store the received energy, energy-efficient battery charger design is also essential. Since the aforementioned emerging applications usually consume mW or sub-mW power, even small power saving in the battery charger contributes to prolonged device operations. Therefore, it is necessary to design a battery charger with low quiescent current (I_{Q}) in the energy-constrained environment. Therefore, .

While a high-performance rectifier and a energy-efficient battery charger are important in terms of power management of the power receiving unit (PRU), a low-power high-performance analog-to-digital converter (ADC) is important in terms of signal processing in the PRU. Currently three types of ADC architectures compete in a design space with moderate-to-high resolution and speed: a pipelined ADC, a successive approximation register (SAR) ADC, and a pipelined-SAR ADC. Fig. 1.3 shows ADC trends published in International Solid-State Circuits Conference (ISSCC) and Symposium on VLSI Circuits (SOVC) from 2012 to 2017 [19]. A pipelined ADC has been a dominant architecture for moderate-to-high resolution and speed applications. However, a SAR ADC emerged due to its simple architecture and low power operations about 10-15 years ago. Fig. 1.3(a) shows a Nyquist sampling frequency ($f_{s,nyq}$) versus SNDR. In Fig. 1.3(a), they compete in the design space of 50-to-70 dB SNDR, and a pipelined ADC is better than a SAR ADC in high speed applications. However, energy efficiency of a pipelined ADC is low, so a pipelined-SAR ADC was proposed for better energy efficiency as a hybrid architecture. Fig. 1.3(b) clearly shows that a pipelined ADC has higher energy consumption (P/f_s) than a SAR ADC does. A pipelined-



(a)



(b)

Figure 1.3: ADC trends published in ISSCC and Symp. VLSI Circuits from 2012 to 2017. (a) Speed vs. SNDR and (b) Energy vs. SNDR [19].

SAR ADC takes strength of both a pipelined ADC and a SAR ADC. Therefore, a pipelined-SAR ADC can be targeted for the PRU under the consideration of scaling of power supply voltage and CMOS technology.

1.2 Research Contribution

This research investigates design of both power management integrated circuits (ICs) and ADCs for the PRU. For the power management ICs, a high-performance rectifier and a low I_Q

linear battery charger are considered. In the rectifier design, we proposed novel low-power comparator circuits for active diodes along with a dynamic logic-based feedback controller to achieve higher PCE and VCR. In battery charger design, we proposed a single amplifier as known as the unified amplifier to perform CC and CV regulation with lower I_{Q}. Both are good for power management ICs in the energy-constrained environments. In ADC research, we proposed a subranging pipelined-SAR ADC with a temperature-insensitive time-based amplifier. This work tries to solve the PVT variation of a high-gain dynamic residue amplifier in the pipelined ADC at the cost of design complexity. Moreover, a temperature compensation technique for a moderate-gain dynamic amplifier is investigated with the benefit of lower design complexity.

1.3 Dissertation Organization

Chapter 2 presents a CMOS active rectifier with a voltage mode switched-offset comparator in TSMC 0.35μm CMOS for wireless power transfer [5]. Novel switched-offset comparators and dynamic logic-based feedback controllers reduce power for active diode operations which are robust to PVT variations.

Chapter 3 describes a linear battery charger for energy-constrained low-power applications [6]. With a proposed low I_{Q} technique, the battery charger achieves low-power operations, maintaining fast regulation. A prototype is implemented in TSMC 0.35μm CMOS.

Chapter 4 discusses a subranging pipelined-SAR ADC using a temperature-insensitive time-based amplifier in IBM 0.13μm CMOS [20]. By using both voltage-to-time conversion and time-to-voltage conversion, temperature-insensitive inter-stage gain is achieved.

Chapter 5 presents a simpler temperature compensation technique for inter-stage gain, which is implemented in in IBM 0.13μm CMOS [21]. A temperature-dependent common mode detector contributes to temperature-insensitiveness of the inter-stage gain amplifier.

This dissertation is concluded in Chapter 6. Chapter 6 summarizes this research and discusses the future work.

2. DESIGN OF A CMOS ACTIVE RECTIFIER FOR WIRELESS POWER TRANSFER*

2.1 Rectifiers

A rectifier is a circuit block that converts the input AC voltage to the output DC voltage. Recent research on energy harvesting and wireless power transfer makes rectifier design gain interest, again. Fig. 2.1 shows many applications adopting rectifiers. Wireless power transfer for portable devices such as tablet PCs and smart phones, electric vehicles (EVs), and bio-implantable devices like neural stimulators are representative examples.

Figure 2.1: Examples of wireless power transfer applications.

Rectifiers can be categorized into passive rectifiers and active rectifiers [22, 23]. Passive rectifiers have the simplest architecture using passive diodes, diode-connected transistors, or gate cross-coupled transistors. A forward voltage-drop problem with passive diodes and diode-connected transistors is mitigated by using Schottky didoes [24], low threshold voltage devices, or gate cross-coupled transistors. However, the Schottky diodes are not always available in CMOS [23], so circuit techniques like threshold voltage cancellation are proposed [23, 25, 26]. Moreover, a passive rectifier with gate cross-coupled transistors still suffers from reverse current.

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Table 2.1: CMOS Passive Rectifier Performances

	TBCAS, 2012 [23]	JSSC, 2010 [26]	ISSCC, 2009 [27]	JSSC, 2006 [25]
Technology (nm)	180	180	130	300
Frequency (MHz)	10	402-405	915 or 1000	900
PCE_{peak} (%)	80	45.2	65	11
P_{OUT} (mW)	2	-	0.24	0.028

In contrast, active rectifiers use active diodes to reduce conduction loss. An active diode is comprised of a comparator and a pass transistor. Since high-speed comparator design is critical to the overall rectifier performance, many comparator designs have been proposed, and they are reviewed in Section 2.3. Although active rectifiers have high power conversion efficiency, they are not attractive solutions to very low power applications or high-frequency applications. This is because static power consumption from control circuits challenges start-up operations, and high-frequency switching consumes considerable switching power from large pass transistors and drivers [23]. Therefore, low-power rectifiers like RF energy harvesters or rectifiers operating at hundreds MHz are usually based on passive rectifiers. Table 2.1 shows passive rectifier performances.

2.2 Wireless Power Transfer for IMDs

Owing to energy constraints, implantable medical devices (IMDs) require efficient AC-DC conversion with high power conversion efficiency (PCE) and high voltage conversion ratio (VCR) in conjunction with efficient DC-DC conversion. IMDs typically use piezoelectric energy harvesting or wireless power transfer (WPT) for power telemetry [1, 28]. Depending on types of IMDs, voltage and power requirements are diverse. For example, lithium-ion batteries popular to IMDs require a full charging voltage of 4.2 V [2, 11]. Moreover, general therapeutic stimulation parameters for deep brain stimulation (DBS) are 1-5 V stimulus amplitude, 60-200 μs stimulus pulse duration, and 120-180 Hz stimulus frequency [29]. Power level of 100 mW can support a wide range of IMDs such as neural recorder/stimulators, retinal implants, and cochlear processors [28]. Fig. 2.2 shows how wireless charging works in cochlear implants and retinal implants.

Recently, resonance-based WPT has been actively investigated to enhance spatial flexibility

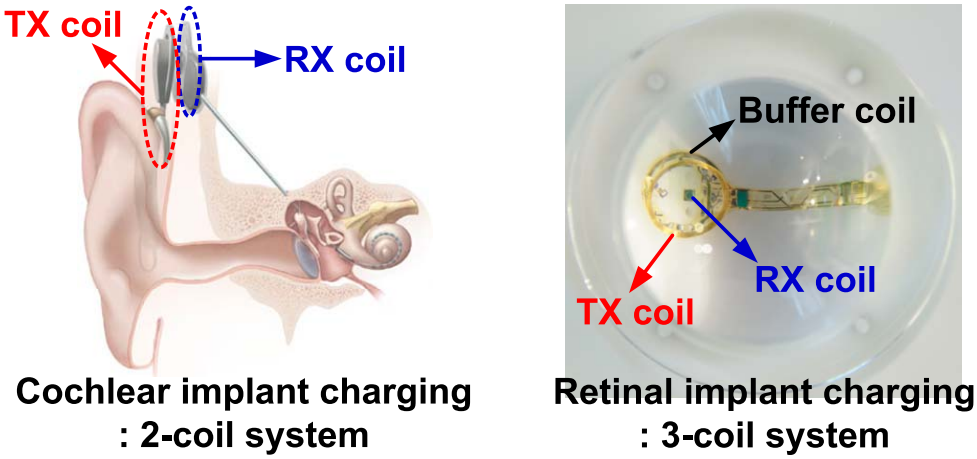


Figure 2.2: 2 or 3-coil wireless power transfer system examples for IMD applications. The photo of retinal implant charging is credited to Robertba, 2011 under Creative Commons license [30].

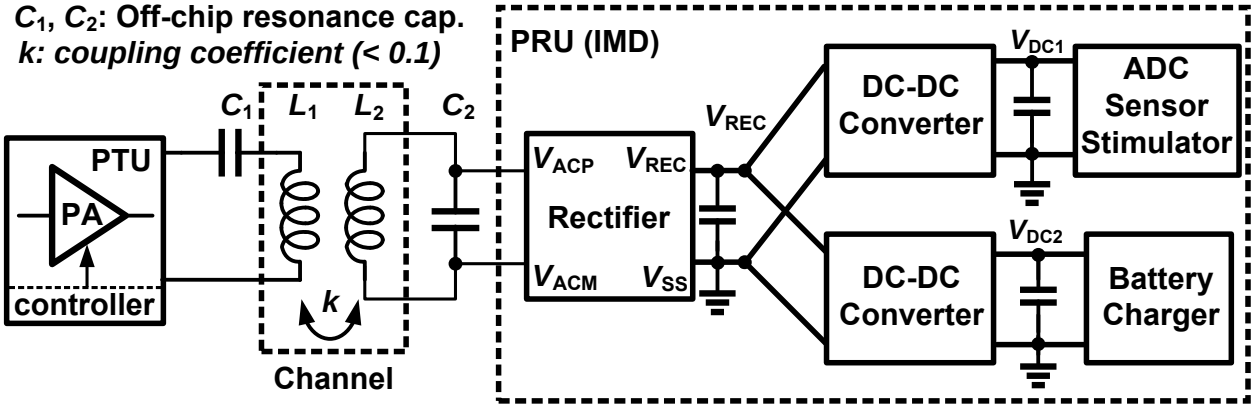


Figure 2.3: General resonance-based WPT system for IMDs with secondary parallel LC resonance.

in loosely coupled systems whose coupling coefficient, k, is typically less than 0.1 [31]. Fig. 2.3 shows a general resonance-based WPT system comprised of a power transmitting unit (PTU), an inductive channel, and a power receiving unit (PRU). A PTU consists of a coil driver and a controller. Both class-D and class-E power amplifiers (PAs) are popular coil drivers. While the class-E PA has higher efficiency, the class-D PA has strengths over the class-E PA regarding its lower design complexity and robustness against load impedance variation [32]. PTU/PRU coils for an inductive channel are made of Litz wire or a PCB trace. Coil resonance configuration of the PRU depends on how a high-Q LC tank is made. For example, a low power system in the mW

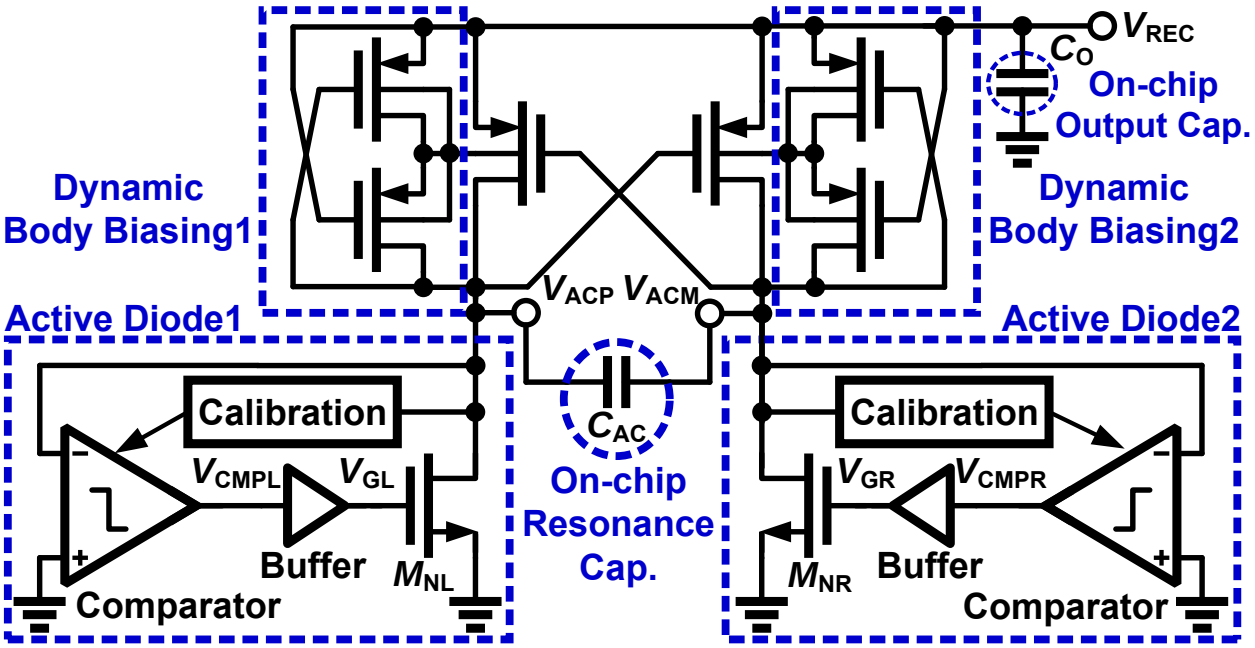


Figure 2.4: Active rectifier with NMOS active diodes and offset calibration.

range employs parallel LC resonance in the PRU, whereas a medium-to-high power system in the W range uses series LC resonance. A PRU can include a rectifier, power management blocks, and load circuits.

To achieve high end-to-end efficiency of the WPT system, rectifier power loss should be minimized. Switching loss and conduction loss are major loss components, and their optimization has been studied well. Appendix A shows the detailed analysis. To minimize these power losses, an active rectifier with NMOS active diodes shown in Fig. 2.4 is preferred to a passive rectifier and an active rectifier with PMOS active diodes because it avoids the forward voltage-drop of a passive diode and the large switching loss of a PMOS power transistor [33]. The rectifier converts input differential AC voltage, $V_{\mathrm{ACP}} - V_{\mathrm{ACM}}$, to the output DC voltage, V_{REC}. On-chip capacitors, C_{O} and C_{AC}, help to reduce the number of off-chip capacitors and the effect of bonding wire inductance. Dynamic body biasing for PMOS power transistors prevents latch-up [34]. Moreover, circuit techniques like a buffer with a starving resistor inserted for short-circuit current suppression [35] and adaptive power transistor sizing [36] further reduce the power loss. However, these techniques do

not solve the issues related to power transistor switching timing: reverse current and maximum conduction time.

Recent comparator offset/delay calibration techniques for accurate power transistor switching [33, 36–42] minimize reverse current, and maximize conduction time, thereby enhancing PCE. While conduction loss is reduced significantly, however, the power loss of comparators and offset calibration circuits becomes one of the major power loss components [37, 42]. For example, under the rectifier output voltage of 3.29 V and 500 Ω loading, comparators and offset calibration circuits occupy 36% of the total power loss in a well-designed rectifier [37]. Their loss along with switching loss is detrimental to PCE particularly in light-load systems. Therefore, low-power circuit techniques for comparators and offset calibration circuits are necessary.

This chapter presents low-power comparators and offset calibration circuits for a 13.56 MHz CMOS active rectifier shown in Fig. 2.4. The proposed voltage mode switched-offset comparator achieves low-power switched-offset operations, while the proposed low-power dynamic logic-based offset calibration circuits generate control signals for the switched-offset operations. The rest of this chapter is organized as follows. Section 2.3 reviews prior art common-gate comparators for active diodes. Section 2.4 presents the voltage mode switched-offset comparator with the offset calibration circuits, and discusses comparisons with the current mode counterpart. Section 2.5 discusses technology scaling effects on power loss. Section 2.6 reports the measurement results. Conclusions are drawn in Section 2.7.

2.3 Review of Common-Gate Comparators for Active Diodes

A basic NMOS active diode consists of an NMOS power transistor, a comparator, and a buffer. Since the comparator compares the input voltage with 0 V, a common-gate comparator has been widely employed in rectifiers [35–39, 43–45]. Fig. 2.5 shows different kinds of common-gate comparators for the active diode1 shown in Fig. 2.4. Accurate on/off-switching of the active diode is crucial to secure the maximum conduction time and prevent reverse current. However, delay of the comparator and the buffer makes the on/off-switching inaccurate.

To compensate for the delay, two approaches have been proposed in comparator design. One

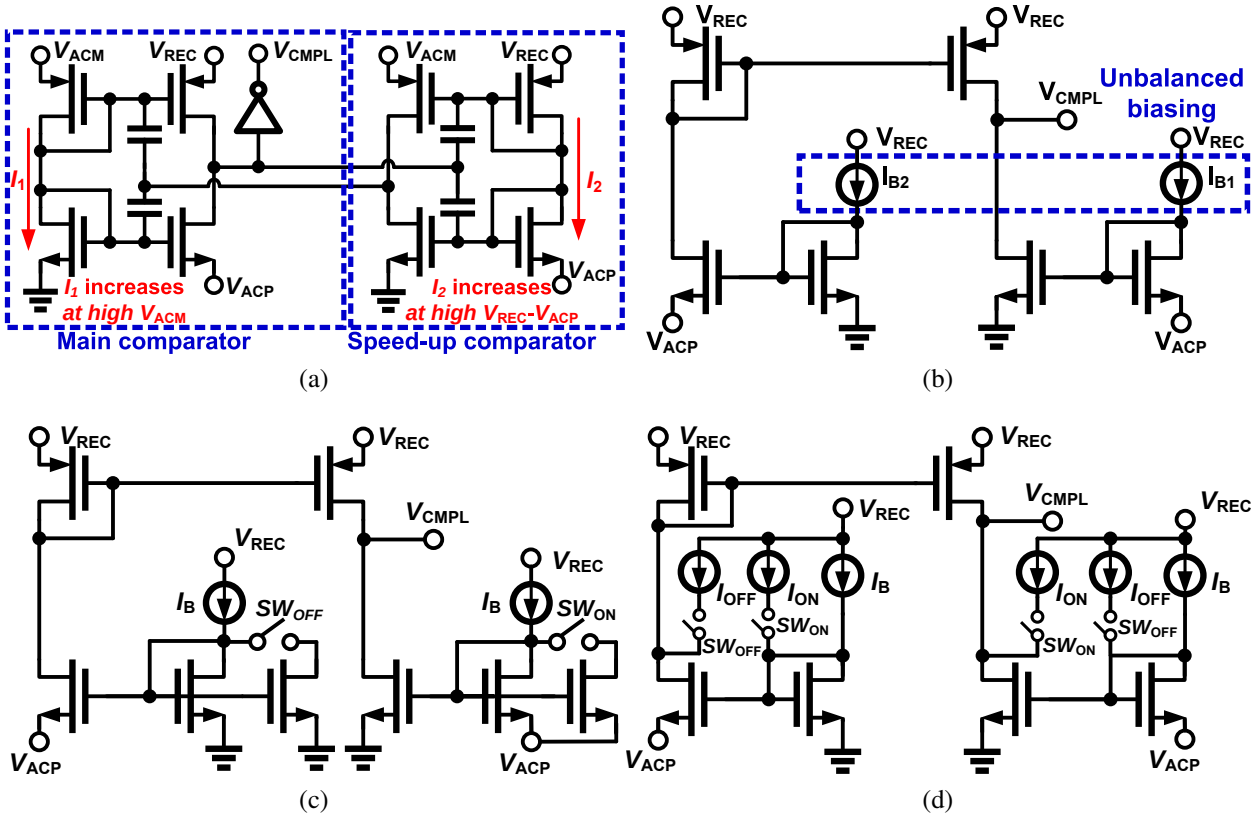


Figure 2.5: Simplified comparators for the active diode1 of Fig. 2.4: (a) positive feedback [43], (b) unbalanced biasing [44], (c) unbalanced sizing [45], and (d) offset current injection [36, 37].

is to enhance the comparator speed with the help of positive feedback. The comparator shown in Fig. 2.5(a) [43] utilizes latching operation through capacitive cross-coupling between the main comparator and a speed-up comparator, enhancing the transient response of the output V_{CMPL}. However, high voltage can induce large current through the stack of diode-connected transistors, which worsens PCE.

The other approach is to inject artificial offset into the comparator. Fig. 2.5(b)-Fig. 2.5(d) show various offset injection methods such as unbalanced biasing [44], unbalanced sizing [45], and offset current injection [36, 37], respectively. The unbalanced biasing of Fig. 2.5(b) is simple, but has proven effective only for off-switching compensation by making I_{B1} larger than I_{B2}. In case of unbalanced sizing in Fig. 2.5(c), both on- and off-switching compensations are done. SW_{ON} is closed and SW_{OFF} is open for the on-switching, and vice versa for the off-switching. However, the

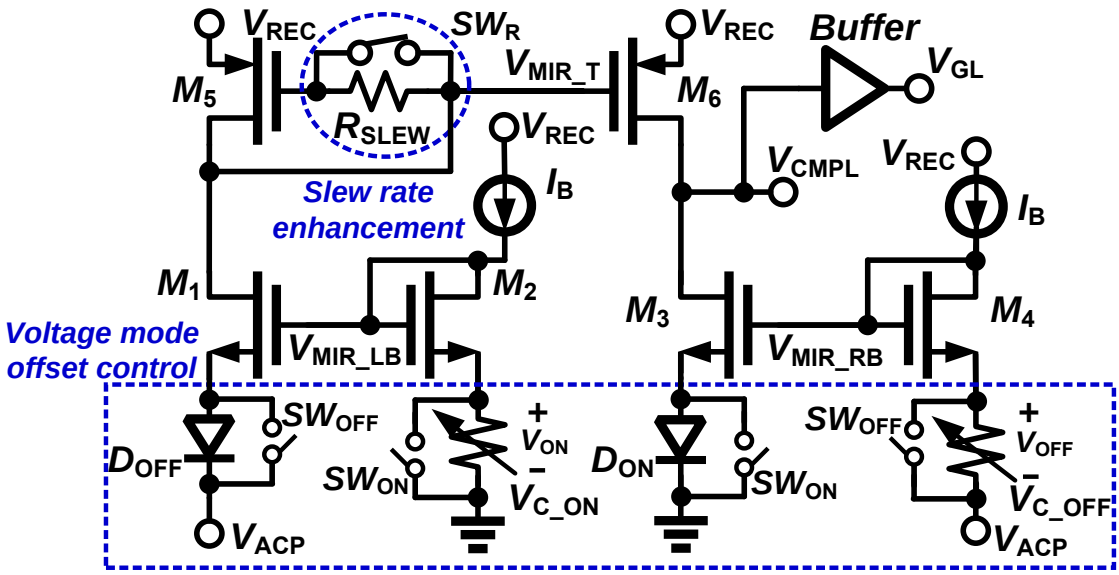


Figure 2.6: Concept of the voltage mode switched-offset comparator.

amount of offset is fixed by transistor sizing in the design phase, so compensation is not robust to process, voltage, and temperature (PVT) variation and loading conditions. Offset current injection of Fig. 2.5(d) compensates for on/off-switching in a way similar to the operations of SW_{ON} and SW_{OFF} for the unbalanced sizing. The amounts of the offset currents, I_{ON} and I_{OFF}, can be either fixed in the design phase [38, 39] or adjusted adaptively [36, 37]. However, offset current injection accompanies extra power consumption to implement artificial input-referred offset voltages. In case of the adaptive offset currents, comparator power loss increases when large input-referred offset voltage is required, or the rectified output voltage, V_{REC}, is high.

2.4 Voltage Mode Switched-Offset Comparator With Offset Calibration Circuits

2.4.1 Voltage Mode Switched-Offset Comparator

We will refer to a comparator shown in Fig. 2.5(d) as a current mode switched-offset comparator. In this section, we propose a voltage mode switched-offset comparator to reduce power loss.

Fig. 2.6 illustrates the concept of the proposed voltage mode switched-offset comparator. In contrast to the current mode offset control shown in Fig. 2.5(d), the offset control circuit in Fig. 2.6

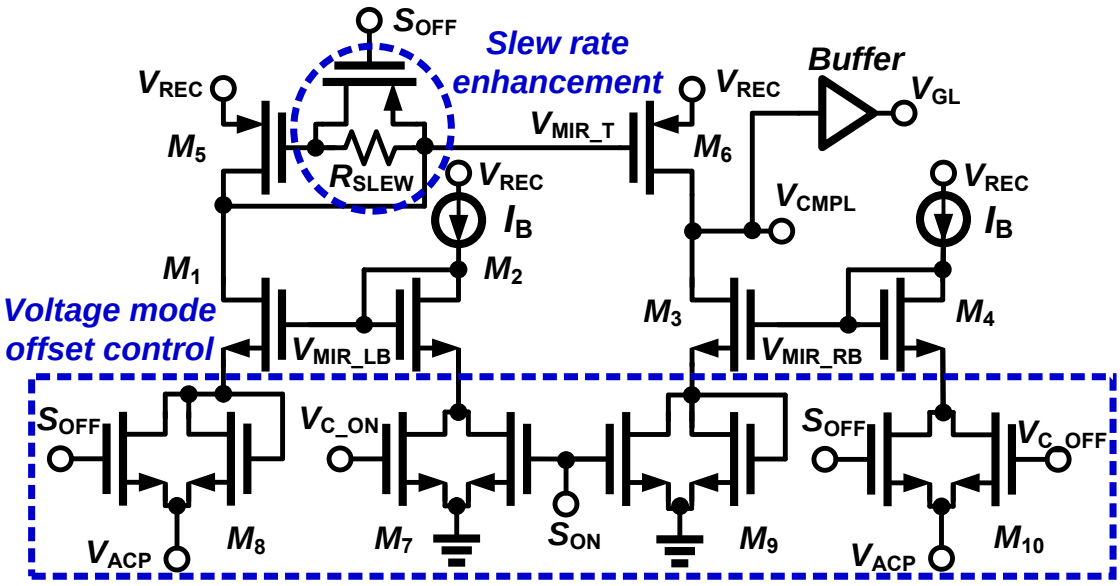


Figure 2.7: Proposed voltage mode switched-offset comparator.

directly injects the offset voltage into the comparator without using extra current. Switches, SW_{ON} and SW_{OFF}, are initially closed, and are open to inject the required offset voltages when the active diode is turned on or off, respectively. The on-chip offset calibration feedback adjusts the magnitude of offset voltages, V_{ON} and V_{OFF}, by calibrating their control voltages, $V_{\text{C\_ON}}$ and $V_{\text{C\_OFF}}$, respectively [36,37]. Diodes, D_{ON} and D_{OFF}, are current limiting diodes to suppress shoot-through current. A switched resistor, R_{SLEW}, enhances a comparator slew rate during the on-switching by suppressing M_5 gate capacitor charging. M_5 and M_6 are used as a current folder in the proposed comparator, whereas they are used as a current mirror in conventional comparators. While an accurate mirror ratio is not design interest, it is design intent to amplify small incremental current through M_1 by switching R_{SLEW} for fast on-switching. For proper R_{SLEW} control, a required switch, SW_{R}, should be open before the on-switching, and be closed right after the on-switching. SW_{ON}, SW_{OFF}, and SW_{R} are controlled by the on-chip offset calibration circuits.

Fig. 2.7 shows the proposed comparator circuit. M_7 and M_{10} implement the required offset voltages, V_{ON} and V_{OFF}, controlled by their gate voltages, $V_{\text{C\_ON}}$ and $V_{\text{C\_OFF}}$. M_8 and M_9 are the current limiting diodes. S_{ON} and S_{OFF} are control signals for switched-offset operations. The

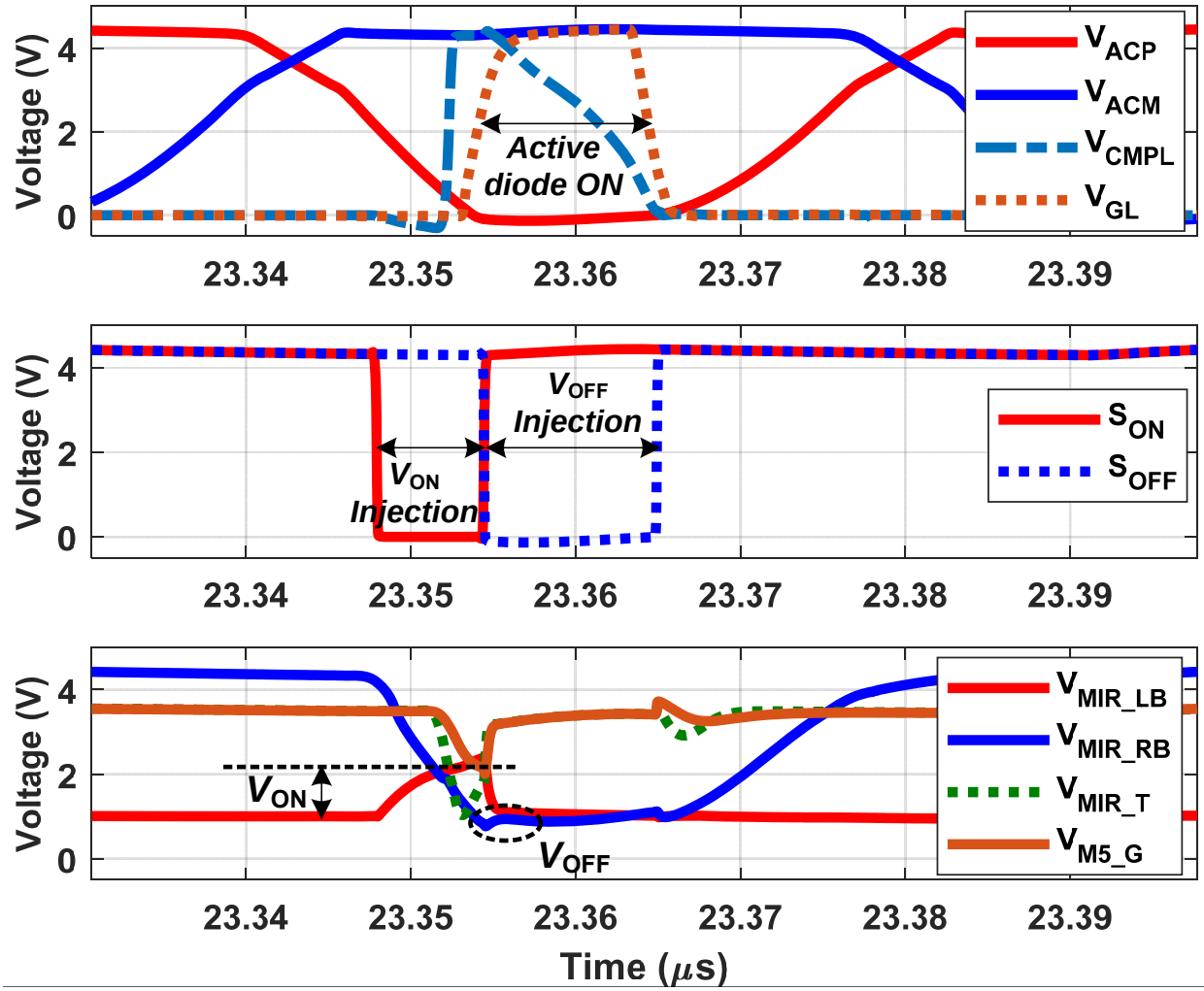


Figure 2.8: Simulated waveforms of the proposed comparator.

resistor R_{SLEW} is an N-well diffusion resistor with high sheet resistance. Resistance variation is acceptable as long as the resistance is large enough to suppress charging to the gate capacitor of M_5 during the on-switching.

Fig. 2.8 shows simulated transient waveforms of the input, output, and internal nodes of the proposed comparator. For accurate on-switching, S_{ON} becomes low to inject the offset voltage before V_{ACP} crosses 0 V. $V_{\text{MIR\_LB}}$ controlled by M_7 starts to increase, while the current limiting diode M_9 suppresses shoot-through current through M_3. At this point, R_{SLEW} further helps a fast comparator decision by enhancing the slew rate of V_{CMPL}. As shown in Fig. 2.8, $V_{\text{MIR\_T}}$ drops quickly in comparison with M_5 gate node voltage, $V_{\text{M5\_G}}$. When the gate signal, V_{GL},

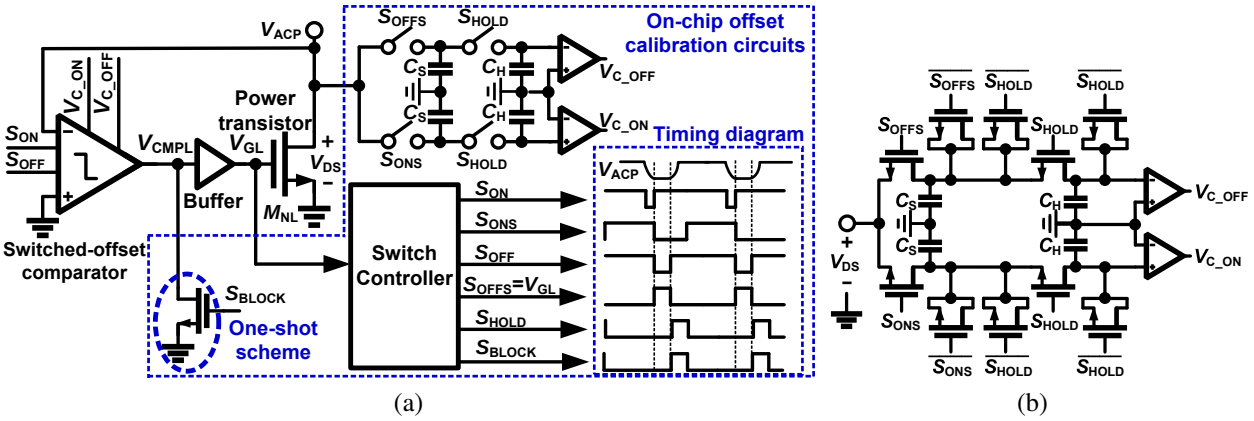


Figure 2.9: (a) Simplified NMOS active diode with on-chip offset calibration feedback and its timing diagram [37] and (b) its detailed V_{DS} sampling network.

of the NMOS power transistor, M_{NL}, in Fig. 2.4 transits from low to high, S_{ON} and S_{OFF} are inverted as shown in Fig. 2.8, and the offset voltage for the off-switching is injected. $V_{\mathrm{MIR\_RB}}$ controlled by M_{10} starts to increase, while the current limiting diode M_8 suppresses shoot-through current through M_1. Short-circuiting R_{SLEW} rapidly increases $V_{\mathrm{MIR\_T}}$, thereby reducing the current through M_6. When V_{GL} transits from high to low, S_{OFF} becomes high, and the offset voltage for the off-switching is reset.

2.4.2 Low-power Dynamic Logic-based Switch Controller

Fig. 2.9(a) shows an NMOS active diode with on-chip offset calibration circuits. Sampling-based offset/delay calibration circuits [36, 37, 41] sample V_{DS} of the power transistor, M_{NL}, at the transition of V_{GL}, and negative feedback forces the sampled V_{DS} to be 0 V. Therefore, reverse current is minimized, and conduction time is maximized. Here, we adopted operational transconductance amplifier (OTA)-based feedback [36, 37]. Since there is no specific constraints on calibration feedback loop bandwidth, low-power low-speed two-stage Miller-compensated amplifiers are used for stability [36, 37]. The one-shot scheme [37] prevents multiple pulsing [33]. A switch controller in Fig. 2.9(a) generates control signals for sampling (S_{ONS}, S_{OFFS}, and S_{HOLD}), switched-offset (S_{ON} and S_{OFF}), and the one-shot scheme (S_{BLOCK}), occupying most power loss of the whole offset calibration circuits. This is because analog power consumption of the OTAs and

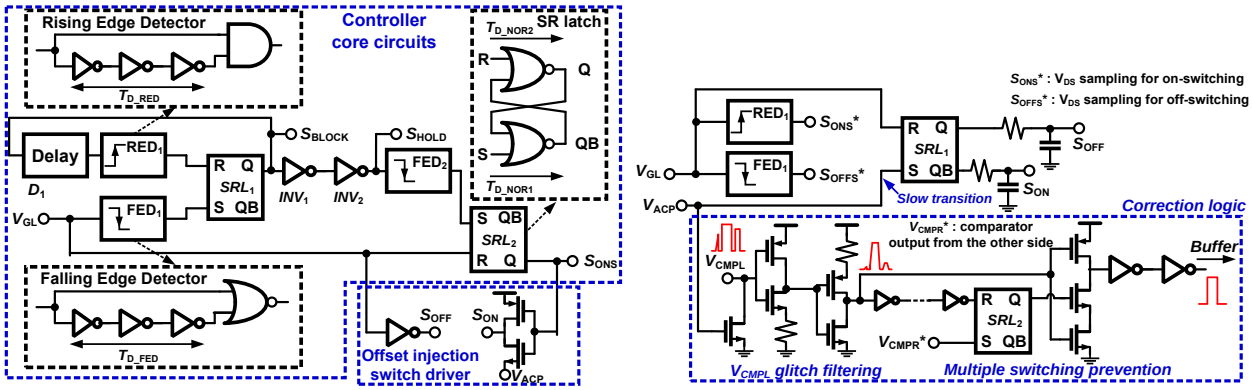
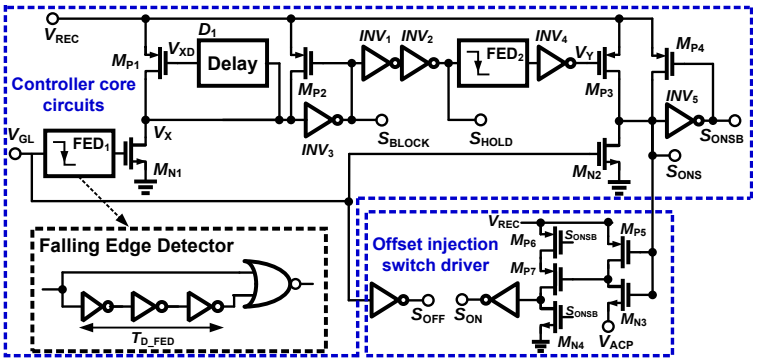


Figure 2.10: Conventional switch controller examples from (a) [37] and (b) [36].

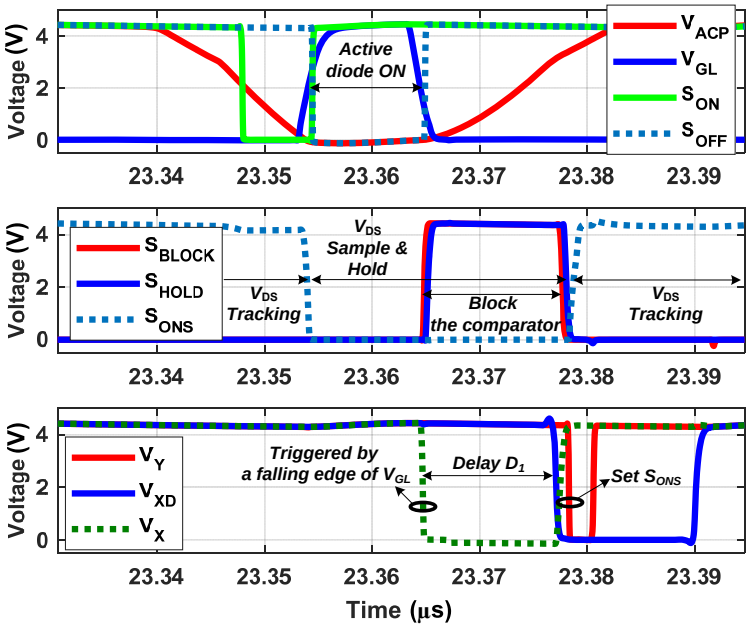
sampling/holding capacitors, C_{S} and C_{H}, can be minimized as mentioned above. Both C_{S} and C_{H} are 108 fF in this design, and dummy switches are used for sampling to minimize charge injection and clock feed-through as shown in Fig. 2.9(b). Offset voltage of the amplifiers are minimized by common-centroid layout with large transistors.

NOR gate-based SR latches and rising/falling edge detectors are key blocks to conventional switch controllers. The inputs of the SR latches are connected to the edge detector output signals [37] or the rectifier input signals [36]. Fig. 2.10 shows conventional switch controller examples [36, 37]. The SR latches significantly affect power loss of the switch controller in Fig. 2.10(a). A NOR gate has larger input capacitance than a simple inverter gate, which increases power loss. Moreover, for proper latching operation, the input signal of the NOR gate-based SR latch should be stable for the duration longer than propagation delay through two cross-coupled NOR gates, $T_{\mathrm{D\_NOR1}} + T_{\mathrm{D\_NOR2}}$. This constraint requires the output pulse signal duration of the edge detector, $T_{\mathrm{D\_FED}}$ or $T_{\mathrm{D\_RED}}$, to be longer than $T_{\mathrm{D\_NOR1}} + T_{\mathrm{D\_NOR2}}$, thereby increasing power consumption of the edge detector.

In Fig. 2.10(b), the SR latch input is connected to the rectifier input AC voltage, V_{ACP} [36], and a slow transition of V_{ACP} increases short-circuit power of the SR latch. As shown in Fig. 2.8, rail-to-rail transitions of V_{ACP} take longer than 10 ns. Therefore, it is necessary that the input of the SR latch avoid the output pulse signal of the edge detector or the rectifier input AC voltage



(a)



(b)

Figure 2.11: (a) Proposed dynamic logic-based switch controller for the offset calibration circuits and (b) its simulated waveforms

for low-power operation. Note that control signals generated by Fig. 2.10(b) do not exactly match those in Fig. 2.9(a) because on-chip offset calibration feedback circuits in [36] are slightly different from Fig. 2.9(a). We adopted offset calibration shown in Fig. 2.9(a) for our proposed controller to avoid delay from correction logic circuits in Fig. 2.10(b) which are inserted between a comparator and a buffer.

Fig. 2.11 illustrates the proposed low-power dynamic logic-based switch controller and its simulated waveforms. Eliminating NOR-based SR latches solves the aforementioned problems.

M_{N1}, M_{P1}, M_{P2}, and INV_3 in Fig. 2.11(a) are functionally equivalent to RED_1 and SRL_1 in Fig. 2.10. At the falling transition of V_{GL} in Fig. 2.11(b), an NMOS power transistor, M_{NL}, is turned off. At this point, a falling edge detector, FED_1, generates a short pulse, and triggers the following self-resetting domino buffer with a small keeper, M_{P2}. The generated pulse duration should be long enough to discharge the internal node of V_X, but shorter than propagation delay of the delay line block, D_1. Propagation delay of D_1 should be long enough to prevent multiple pulsing. Since small capacitance at the node of V_X enables rapid discharging, FED_1 can reduce power consumption. A pulse signal for the one-shot scheme, S_{BLOCK}, makes the comparator output voltage, V_{CMPL}, grounded to prevent multiple switching of the comparator. S_{HOLD} is a control signal for holding capacitors, C_H, and is a non-overlapped signal with S_{ONS} and S_{OFFS}. The other falling edge detector, FED_2, generates a pulse signal at the falling transition of S_{HOLD}. M_{N2} and M_{P3} implement a dynamic SR latch triggered by pulse signals at V_{GL} and V_Y. The node of S_{ONS} is also buffered by a static inverter with a small keeper, M_{P4}, to avoid a high impedance node. S_{ONSB} is a complementary signal to S_{ONS} for sampling switches. S_{ON} and S_{OFF} are generated to control offset injection switches. In contrast to Fig. 2.10, we use a domino buffer consisting of M_{P6}, M_{P7}, M_{N4}, and an inverter to generate S_{ON}. By doing this, voltage mode switched-offset injection for on-switching, V_{ON}, starts earlier, which increases range of V_{ON}. The dynamic inverter is used to reduce short-circuit current induced by a slow transition of V_{ACP}.

Fig. 2.12 shows power consumption of controller core circuits in Fig. 2.10(a) and Fig. 2.11(a), respectively. The same falling edge detectors, FED_1 and FED_2, and delay line block, D_1, are used to assess the proposed low-power techniques for the worst case simulation. If we reduce T_{D_FED} in Fig. 2.11(a), power consumption is reduced more. Power consumption is reduced by 22-24%. In summary, as compared with the example shown in Fig. 2.10(a), the proposed switch controller has less number of edge detectors and less internal capacitive loading by eliminating NOR gate-based SR latches, which leads to lower power consumption.

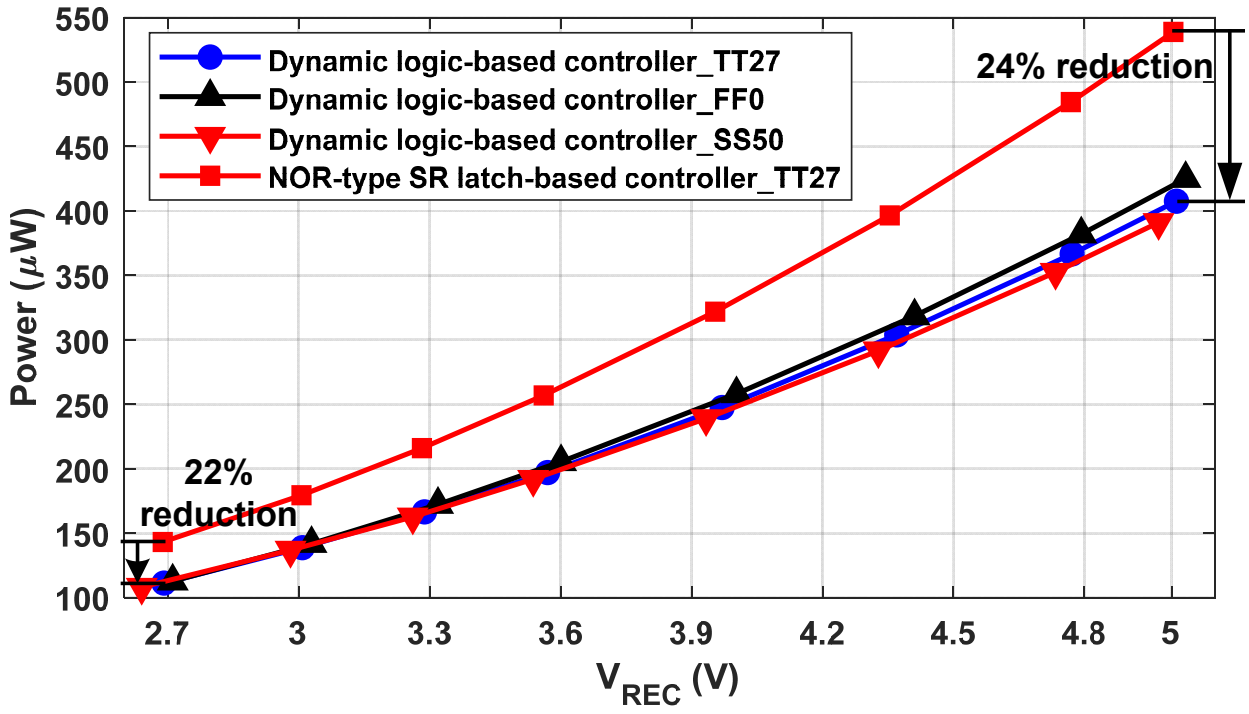


Figure 2.12: Power consumption of controller core circuits in Fig. 2.10(a) and Fig. 2.11(a).

2.4.3 Transient simulations

Fig. 2.13 shows the simulated waveforms during start-up of a rectifier with the proposed comparators and controllers. I_{NMOS} shows the current through the NMOS power transistor, M_{NL}. The calibration feedback loop makes offset control voltage, $V_{\mathrm{C\_ON}}$ and $V_{\mathrm{C\_OFF}}$, converge to proper voltage for accurate on/off-switching, respectively, eliminating reverse current.

2.4.4 Comparison with a Current Mode Switched-Offset Comparator

We use an active diode of Fig. 2.9(a) to compare the proposed comparator with the current mode counterpart. For fair comparisons, each simulation uses the same circuits except the switched-offset comparator in Fig. 2.9(a). The proposed switch controller is used in the simulations. For the switched-offset comparator, two different comparators of Fig. 2.7 and Fig. 2.5(d) are used. They have the same push-pull core transistors, M_1-M_6, and the same bias current, I_{B}.

Fig. 2.14 shows simulated power consumptions of two comparators and two offset calibration

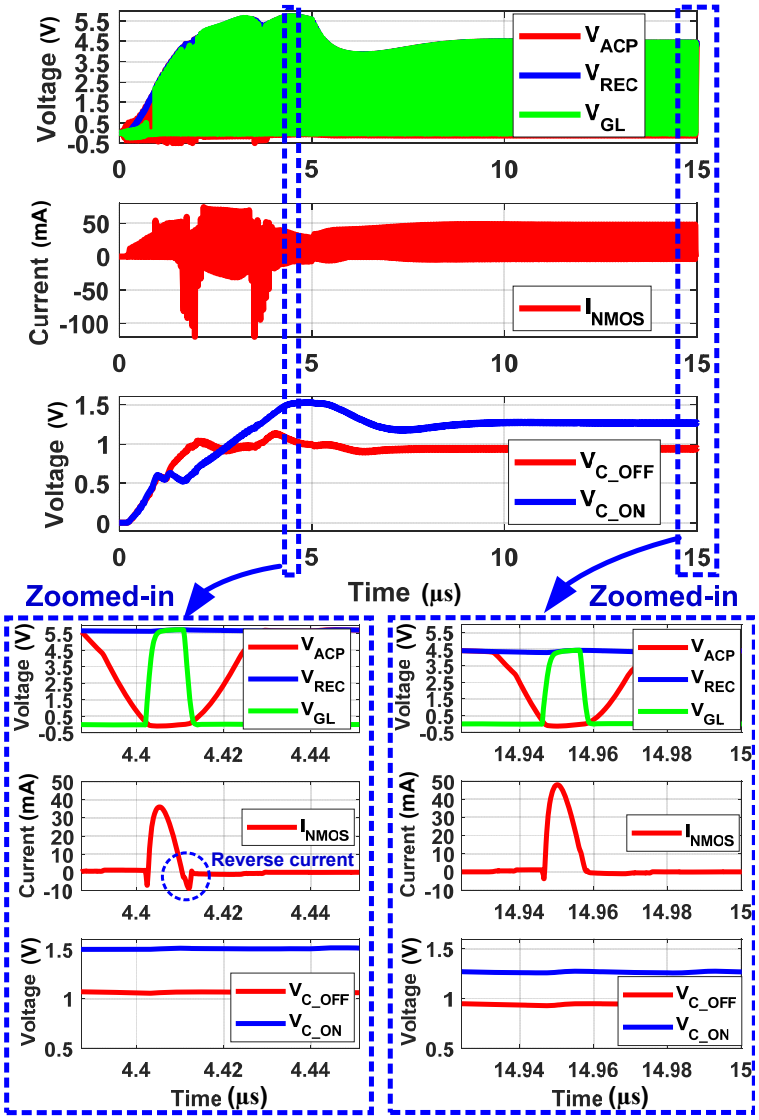


Figure 2.13: Simulation waveforms during start-up with R_{L} = 500 Ω

circuits, $P_{CMP+CAL\_2X}$, power consumptions of two comparators, P_{CMP_2X}, PCEs, and VCRs of the rectifiers with different loading R_{L}, which is implemented with 5-V devices of 0.35 μm CMOS process. To avoid exaggerated comparisons, it is necessary to assess if the simulated rectifier with current mode comparators is reasonably designed. The simulated rectifier with current mode comparators consumes $P_{CMP+CAL\_2X}$ of 1.16 mW at V_{REC} = 3.3 V and 500 Ω loading. A similar rectifier [37] designed with 3.3-V devices of 0.35 μm CMOS process has $P_{CMP+CAL\_2X}$ of 0.77 mW at V_{REC} = 3.29 V and 500 Ω loading. Since $P_{CMP+CAL\_2X}$ is mainly dissipated by digital logic

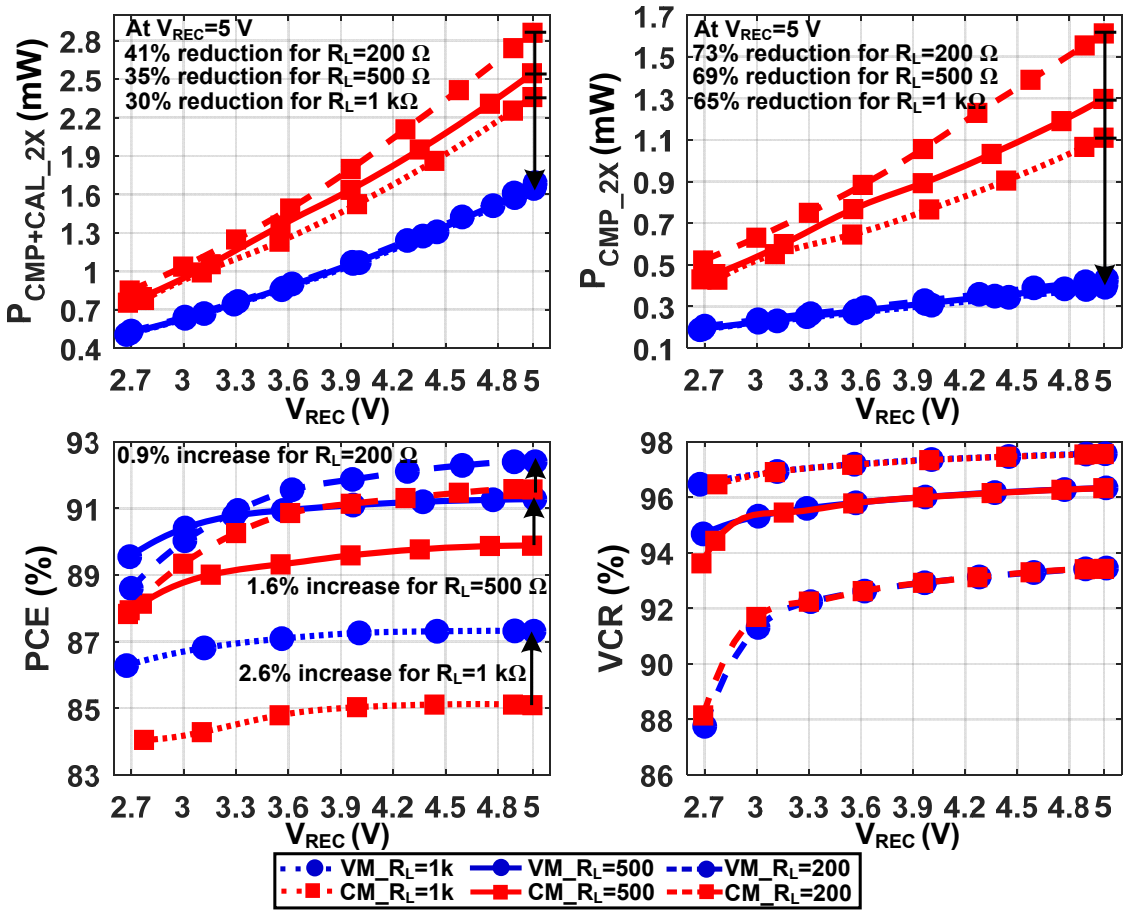


Figure 2.14: Simulated $P_{CMP+CAL\_2X}$, P_{CMP_2X}, PCE, and VCR of the rectifiers with voltage/current mode (VM/CM) switched-offset comparators.

circuits and comparators, the CMOS scaling theory [46] is used to account for the technology difference. 30% shrinking from 0.5 μm to 0.35 μm reduces power consumption of digital circuits under the same supply voltage by 30%. Based on this, $P_{CMP+CAL\_2X}$ of 0.77 mW is scaled to 1.1 mW, which approximates 1.16 mW of the simulation. Therefore, the above design comparisons are not exaggerated.

At V_{REC} = 5 V, P_{CMP_2X} reductions of 65%, 69%, and 73%, equivalent to $P_{CMP+CAL\_2X}$ reductions of 30%, 35%, and 41%, improve PCEs by 2.6%, 1.6%, and 0.9% for R_L = 1 $k\Omega$, 500 Ω, and 200 Ω, respectively. P_{CMP_2X} of the proposed comparator increases 2.1-fold for 500 Ω loading and V_{REC} = 2.7-5 V, whereas that of the current mode counterpart increases 3.0-fold. VCR of the rectifier using the proposed comparator decreases for R_L = 200 Ω and $V_{REC} \leq$ 3 V because the total

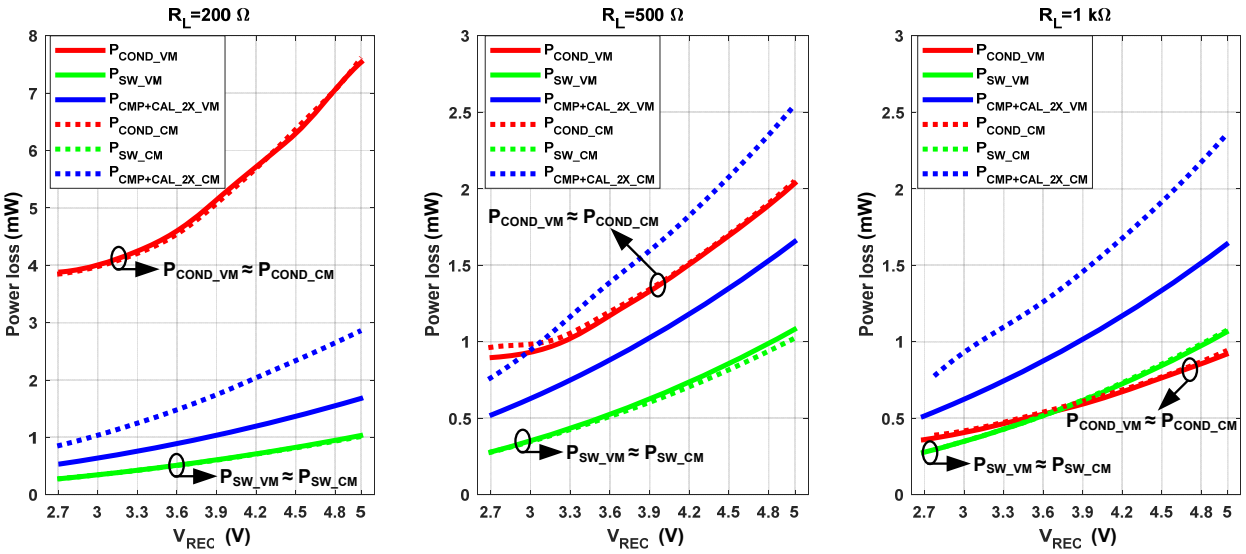


Figure 2.15: Simulated power loss distribution under different V_{REC} and loading conditions

capacitance at the drain of M_9 in Fig. 2.7 limits the offset voltage injection speed, delaying the on-switching. Increasing the comparator bias current enhances VCR, but lowers light-load PCE. Advanced CMOS process can relax this design trade-off thanks to reduced drain capacitance.

Fig. 2.15 shows power loss breakdown of the active rectifier under different V_{REC} and loading conditions. Regardless of loading conditions, the rectifiers with the voltage mode switched-offset comparators and the current mode switched-offset comparators have similar conduction loss, $\mathrm{P_{COND\_VM}}$ and $\mathrm{P_{COND\_CM}}$, and switching loss, $\mathrm{P_{SW\_VM}}$ and $\mathrm{P_{SW\_CM}}$. While $\mathrm{P_{COND\_VM}}$ and $\mathrm{P_{COND\_CM}}$ are dominant for R_{L} = 200 Ω, $\mathrm{P_{CMP+CAL\_2X\_VM}}$ and $\mathrm{P_{CMP+CAL\_2X\_CM}}$ are dominant for R_{L} = 1 kΩ. For R_{L} = 500 Ω, $\mathrm{P_{CMP+CAL\_2X\_CM}}$ becomes dominant power loss in the rectifier with the current mode comparators, whereas $\mathrm{P_{CMP+CAL\_2X\_VM}}$ is still smaller than $\mathrm{P_{COND\_VM}}$. Therefore, reduction of $\mathrm{P_{CMP+CAL\_2X}}$ is critical to light-load efficiency enhancement.

2.4.5 PVT variations

Fig. 2.16 shows simulated PCEs and VCRs of the rectifier with the proposed comparator and 500 Ω loading under different PVT corners. Since human body temperature does not change much, large temperature variation is not a great concern to IMDs. The simulated temperature range is well

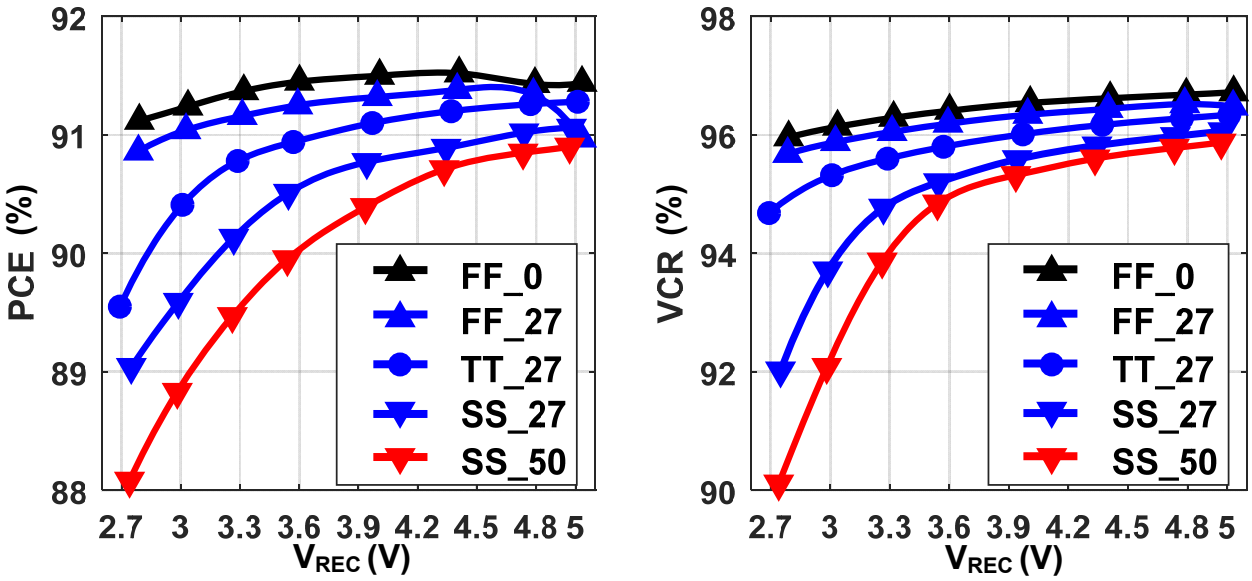


Figure 2.16: PVT variation simulations with R_{L} = 500 Ω

beyond the typical temperature range of IMDs [11].

2.5 Effects of Technology Scaling on Power Loss

It is necessary to understand how technology scaling affects power loss not to compare rectifier performances without considering technology. While advanced CMOS technology potentially provides low on-resistance, low switching loss, and high-density on-chip capacitors, device reliability becomes an issue in high-voltage applications like IMDs. Since all the advanced CMOS technology does not provide high-voltage device options to designers, high-voltage rectifier design implemented with standard low-voltage devices has been investigated to overcome this hurdle [36, 47]. Stacking low-voltage devices is a well-known solution to high-voltage rectifiers as well as high-voltage DC-DC converters. However, design/layout complexity significantly increases, whereas PCE even decreases in consideration of efficiency of a necessary DC-DC converter [36]. Therefore, high-voltage applications prefer implementation with high-voltage devices in finer CMOS technology.

Conduction loss and VCR are closely related with on-resistance of the power transistors, which

is given by

$$R_{\text{on}} = \frac{1}{\beta_{\text{n}} \cdot (V_{\text{REC}} - V_{\text{th,n}})} + \frac{1}{\beta_{\text{p}} \cdot (V_{\text{REC}} - |V_{\text{th,p}}|)} \tag{2.1}$$

where $\beta_{\text{n/p}} = \mu_{\text{n/p}} C_{\text{ox,n/p}} (W/L)_{\text{n/p}}$. $\mu_{\text{n/p}}$, $C_{\text{ox,n/p}}$, and $V_{\text{th,n/p}}$ are the electron/hole mobility, gate oxide capacitance per unit area, and threshold voltage of the NMOS/PMOS power transistor with the aspect ratio of $(W/L)_{\text{n/p}}$, respectively. For simplicity, we assume $C_{\text{ox,n}} = C_{\text{ox,p}} = C_{\text{ox}}$ and $L_{\text{n}} = L_{\text{p}} = L_{\text{min}}$. L_{min} is the minimum channel length. Since the optimal size ratio of the PMOS and NMOS transistors [48] for the minimum area is given by

$$(\frac{W_{\text{p}}}{W_{\text{n}}})_{\text{opt}} = \sqrt{\frac{\mu_{\text{n}} \cdot (V_{\text{REC}} - V_{\text{th,n}})}{\mu_{\text{p}} \cdot (V_{\text{REC}} - |V_{\text{th,p}}|)}} = \gamma, \tag{2.2}$$

the optimal on-resistance is rewritten as

$$R_{\text{on,opt}} = \frac{1+\gamma}{\beta_{\text{n}} \cdot (V_{\text{REC}} - V_{\text{th,n}})}. \tag{2.3}$$

For the same conduction loss, switching loss of one NMOS power transistor is given by

$$\begin{aligned} P_{\text{sw,n}} &= f_{\text{o}} C_{\text{ox,n}} W_{\text{n}} L_{\text{n}} {V_{\text{REC}}}^2 \\ &= \frac{f_{\text{o}}}{\mu_{\text{n}} R_{\text{on,opt}}} \cdot \frac{{L_{\text{min}}}^2 V_{\text{REC}} (1+\gamma)}{1 - V_{\text{th,n}}/V_{\text{REC}}} = \frac{f_{\text{o}}}{\mu_{\text{n}} R_{\text{on,opt}}} \cdot S_{\text{scaling}} \end{aligned} \tag{2.4}$$

where f_o is the operating frequency. Using technology parameters [46], Fig. 2.17 shows that technology scaling significantly reduces switching loss. For example, in 0.35 μm process, switching loss of 5-V device implementation is 2.12-fold higher than that of 3.3-V device implementation for the same on-resistance and V_{REC}.

Technology scaling also reduces $P_{\text{CMP+CAL\_2X}}$. Analog power loss of feedback amplifiers and sampling networks occupies only about 9% of $P_{\text{CMP+CAL\_2X}}$ on average in this design under V_{REC} = 2.7-5 V and R_{L} = 500 Ω because low feedback loop bandwidth for stability allows for a low-power amplifier [37]. Digital logic circuits for switch control occupy about 60% of $P_{\text{CMP+CAL\_2X}}$ on aver-

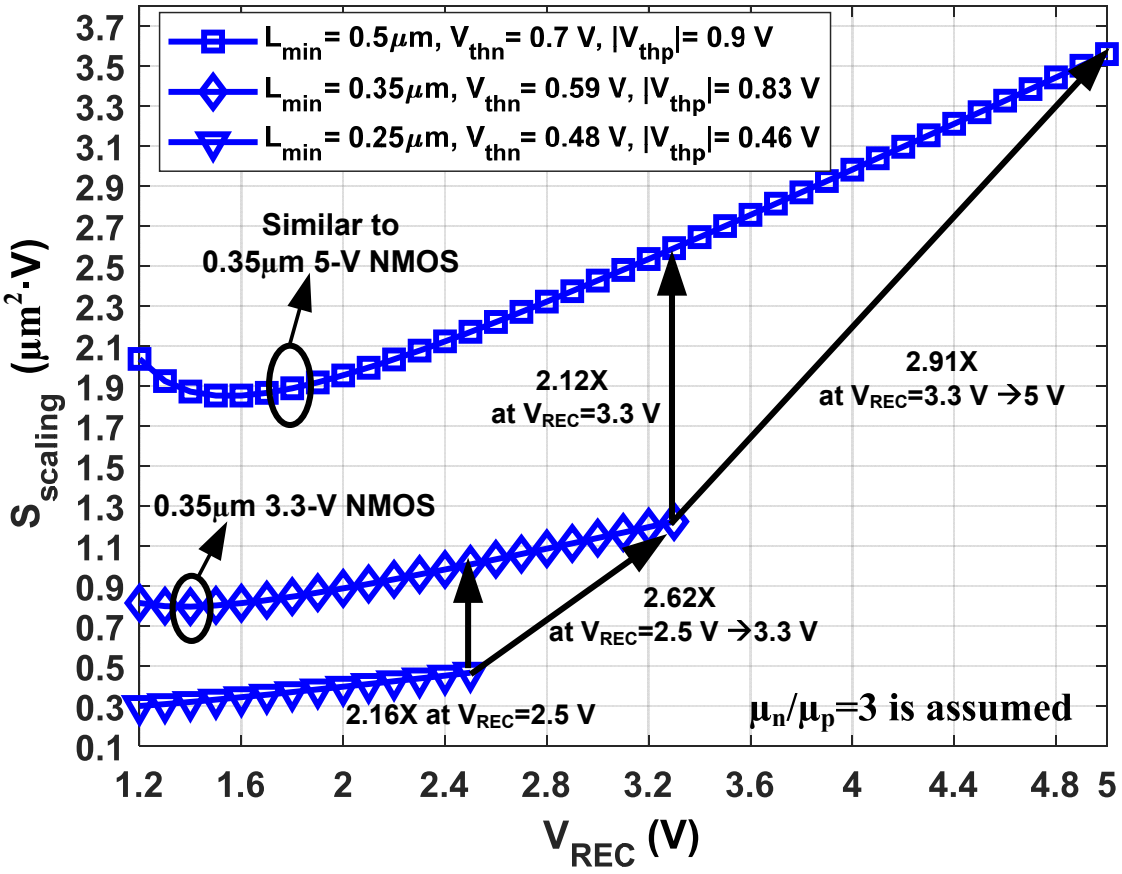


Figure 2.17: Scaling effect of technology and voltage on switching loss

age under the same conditions. According to the scaling theory [46], 30% shrinking from 0.5 μm to 0.35 μm reduces power consumption of digital circuits under the same supply voltage by 30%. Advanced CMOS technology further reduces comparator power loss which is 31% of $P_{CMP+CAL\_2X}$ on average under the same conditions. First, comparator output loads less capacitance due to reduced drain capacitance and buffer input capacitance. Second, comparator/buffer delay reduction as well as rapid offset injection speed reduces the required amount of the offset voltage/current in finer CMOS process. Therefore, a switched-offset comparator in advanced CMOS process can work with lower power consumption over a wide range of V_{REC}.

Fig. 2.18 shows power loss ratios normalized to switching loss, P_{COND}/P_{SW} and $P_{CMP+CAL\_2X}/P_{SW}$, in the proposed rectifier under different output voltage and loading conditions. Regardless of loading conditions, $P_{CMP+CAL\_2X}/P_{SW}$ does not change much over a wide range of

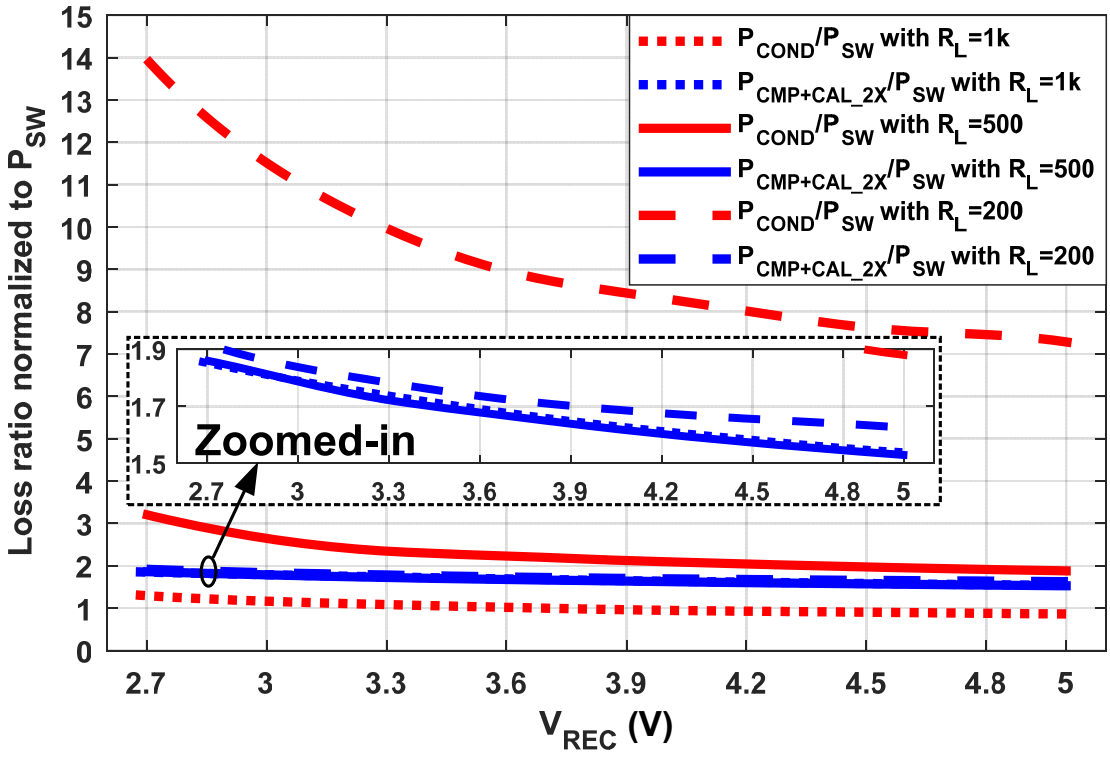


Figure 2.18: Power loss ratios normalized to switching loss

V_{REC}. This implies that digital power consumption dominates $P_{\text{CMP+CAL\_2X}}$ like P_{SW}. Therefore, the scaling theory can be used to compare power consumptions of comparators and control circuits among the rectifier designs implemented with different CMOS technology.

2.6 Measurement Results

The proposed rectifier was fabricated with 5-V devices (L_{min} = 0.5 μm) of TSMC 2P4M 0.35 μm CMOS process to support high voltage, and packaged in QFN48. A chip micrograph is shown in Fig. 2.19. The active area of the rectifier is 1.87 mm^2 (2.10 mm $\times$ 0.89 mm), or 0.38 mm^2 (0.89 mm $\times$ 0.43 mm) if the on-chip output capacitor C_{O} (= 1.7 nF) is excluded. C_{O} is made of MOM and MOS capacitors, which are stacked to maximize capacitance density. C_{AC} is the on-chip input capacitance of 25 pF.

Fig. 2.20 shows the measurement setup, which is similar to [33]. A Tektronix TDS3054 oscilloscope and active differential probes are used for measurements. A class-D PA is implemented

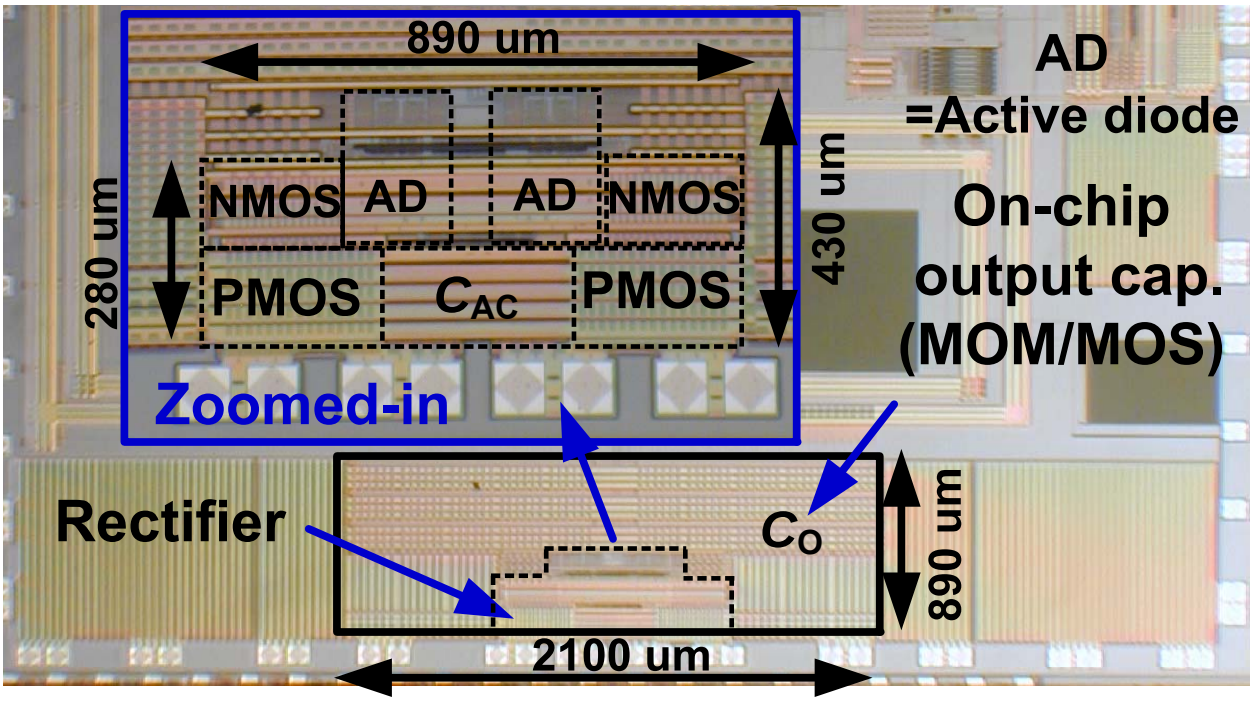


Figure 2.19: Chip micrograph of the implemented rectifier.

for a PTU with discrete components.

Fig. 2.21(a) shows PCB spiral coils for a PTU and a PRU. The primary coil is a 10-turn coil with the outer diameter of 3 cm. Measured inductance and quality factor at 13.56 MHz are 2.19 μH and 90, respectively. The secondary coil is a 4-turn coil with the outer diameter of 1.5 cm. Its inductance and quality factor at 13.56 MHz are 0.48 μH and 55, respectively. Fig. 2.21(b) shows the measured AC input and rectified output waveforms of the proposed rectifier with 500 Ω loading. It is known that suboptimal active diode switching makes the input AC voltage rugged due to Ldi/dt noise [37] in combination with the inductance of bonding wires and package pins. The input AC voltage in this work is not rugged thanks to accurate on/off-switching by offset calibration. However, ringing of the input voltage is observed due to parasitic inductance of bonding wires and interconnect [39], which deteriorates PCE and VCR. The segment with increased V_{REC} confirms on/off-switching moments of the active diode.

Fig. 2.22 shows measured and simulated PCEs and VCRs. For measurements with R_{L} = 200 Ω, 500 Ω, and 1 $k\Omega$, peak (PCE, VCR) are (89.0%, 90.1%), (86.1%, 92.7%), and (79.6%, 96.1%),

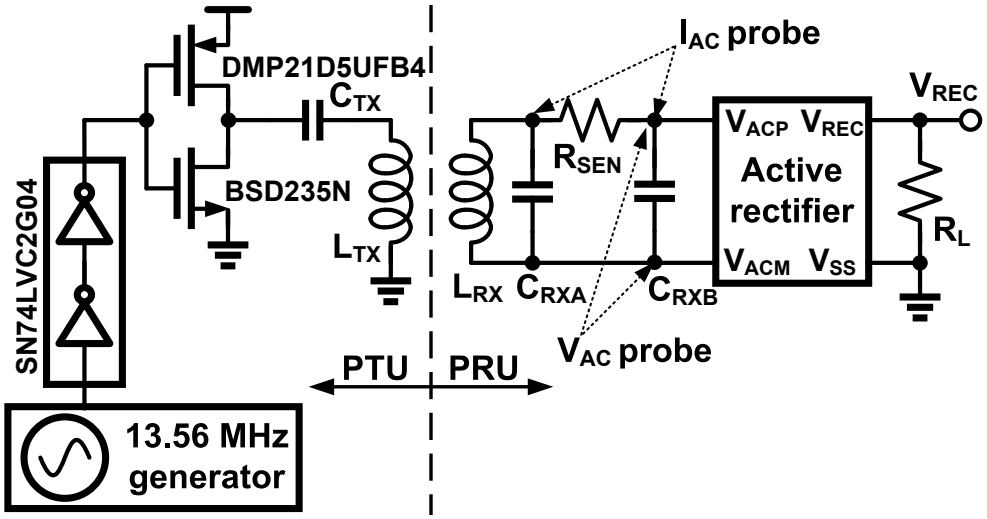
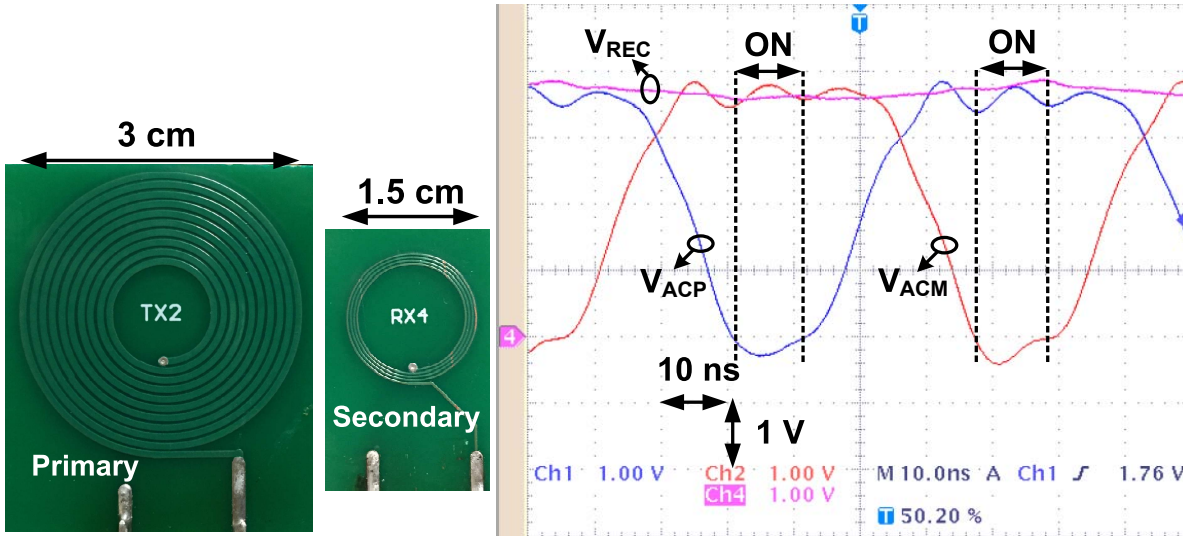


Figure 2.20: Measurement setup [33].



(a) (b)

Figure 2.21: (a) Coils and (b) measured rectifier waveforms with V_{REC} = 3.75 V and R_{L} = 500 Ω .

respectively. For simulations with R_{L} = 200 Ω, 500 Ω, and 1 $k\Omega$, peak (PCE, VCR) are (92.4%, 93.4%), (91.3%, 96.3%), and (87.3%, 97.6%), respectively.

Table 2.2 compares the proposed rectifier with prior works in similar technology whose maximum output powers, $\mathrm{P_{OUT\_MAX}}$, are larger than 30 mW. As discussed in Section. 2.5, low-voltage

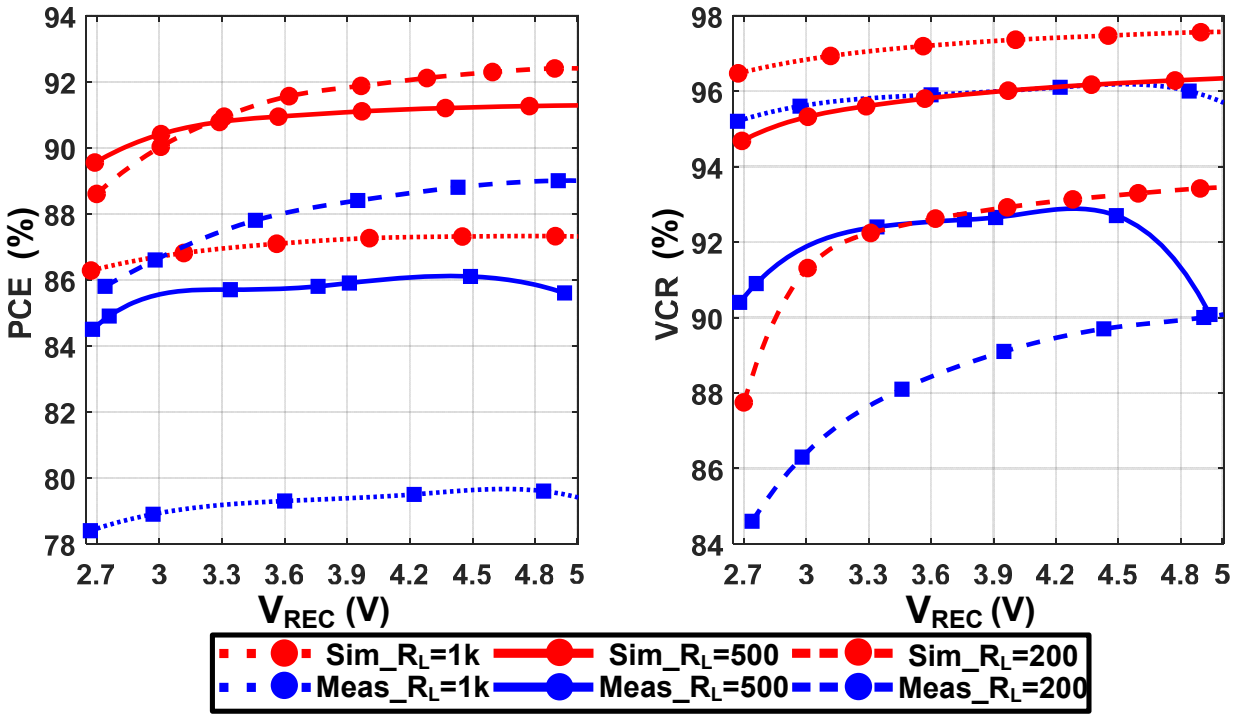


Figure 2.22: Measured and simulated PCEs and VCRs.

devices with short feature length have lower switching loss for the same on-resistance. For example, 5-V NMOS in 0.35μm CMOS technology has 2-fold and 4-fold switching loss in comparison with 3.3-V NMOS in 0.35μm CMOS and 2.5-V NMOS in 0.25μm CMOS, respectively. In addition, power loss from comparators and control circuits is scaled down in advanced CMOS technology. However, low-voltage devices are inadequate for high-voltage applications because of device reliability, additional design complexity, and lower PCE. Therefore, blind PCE comparison without technology consideration is misleading.

This work uses 5-V devices only to support high voltage, and outperforms rectifiers with similar input ranges and feature length (0.5μm). Thanks to comparator power reduction shown in Fig. 2.14, $P_{CMP+CAL\_2X}$ in this work is 3.9% lower than that of [37] for V_{REC} = 3.3 V and R_L = 500 Ω, despite the fact that this work uses 5-V devices. $P_{CMP+CAL\_2X\_SCALED}$ for 30% shrinking from 0.5μm to 0.35μm under the same V_{REC} is 32.7% lower than that of [37]. In comparison with comparators in similar technology [39], P_{CMP_2X} is reduced by about 34% and 60% for V_{REC} = 3.3 V and 3.9

Table 2.2: 13.56 MHz Acitve Rectifier Comparison

		This Work	[40] ISSCC, 2012	[39] TCAS1, 2011	[37] JSSC, 2016	[38] ISSCC, 2013
Technology		0.35 µm 5-V Devices[a.]	0.5 µm	0.5 µm	0.35 µm	0.35 µm
Offset compensation		On/Off	On/Off	On/Off	On/Off	Off
Switched-offset comparator type		VM[b.]	CM[c.]	CM[c.]	CM[c.]	CM[c.]
Input range		2.9-5.4 V	3.2-5 V	3.3-5 V	1.8-3.6 V	1.5-4 V
Output V_{REC} range		2.7-5 V (R_L=500 Ω)	2.5-4.3 V (R_L=500 Ω)	2.5-3.9 V (R_L=500 Ω)	1.45-3.33 V (R_L=500 Ω)	1.27-3.6 V (R_L=500 Ω)
Output cap.		1.7 nF On-chip	2 µF Off-chip	10 µF Off-chip	2 nF On-chip	4 nF On-chip
P_{OUT_MAX}		126.7 mW	37 mW	30.42 mW	64.8 mW	32 mW
VCR at R_L=500 Ω		90.1-92.7 %	77-86 %	76-81 %	90.4-92.4 %	85-90 %
PCE	R_L=200 Ω	85.8-89.0 %	N/A	N/A	88.6-90.5 %	N/A
	R_L=500 Ω	84.6-86.1 %	73-77[d.] %	68-80.2 %	89.1-91.4 %	81-84.2[d.] %
Simulated P_{CMP_2X}[e.]	V_{REC}=3.3 V	0.25 mW	N/A	0.38 mW	N/A	N/A
	V_{REC}=3.9 V	0.31 mW	N/A	0.77 mW	N/A	N/A
Simulated $P_{CMP+CAL\_2X}$[f.]		0.74 mW	N/A	N/A[h.]	0.77 mW	N/A
$P_{CMP+CAL\_2X\_SCALED}$[g.]		0.52 mW	N/A	N/A[h.]	0.77 mW	N/A

Note: Shaded cells denote high voltage application.

[a.] Minimum channel length (L_{min})=0.5 µm. [b.] VM=Voltage mode. [c.] CM=Current mode.
[d.] Compared with a full wave rectifier structure. [e.] R_L=500 Ω. [f.] V_{REC}=3.3 V, R_L=500 Ω.
[g.] $P_{CMP+CAL\_2X\_SCALED}$=$P_{CMP+CAL\_2X}$×S. S=0.7 for 0.5µm-to-0.35µm scaling under the same V_{REC}.
[h.] Off-chip offset control.

V, respectively. Regarding PCE, this work targets the peak PCE at the maximum output power, whereas the rectifier in [37] targets it at 500 ohm loading. The measured peak PCE of this work is 2.4% less than that of [37]. This is because high-voltage devices have larger switching loss, and parasitic inductance of bonding wires and interconnect further deteriorates PCE in this work.

2.7 Conclusion

This chapter presents a voltage mode switched-offset comparator and a dynamic logic-based switch controller for a 13.56 MHz CMOS active rectifier. The proposed low-power circuit techniques reduce power loss of switched-offset comparators and offset/delay calibration circuits which emerges as one of the major power loss components in advanced CMOS active rectifiers. To gener-

ate continuously adjustable input-referred offset voltage, the proposed comparator reuses the bias current instead of injecting extra offset current into the common-gate push-pull comparator core circuit, thereby reducing comparator power loss. The proposed switch controller reduces power overhead that NOR-based SR latches and edge detectors cause due to large capacitance of digital logic gates and short-circuit power by a slow transition of the rectifier input voltage. Moreover, effects of technology scaling on power loss are studied. The presented rectifier is implemented with 5-V devices in 0.35 μm CMOS to support high voltage for low-power applications such as IMDs. It achieves a peak PCE of 89.0%, a peak VCR of 90.1%, and a maximum output power of 126.7 mW for R_{L} = 200 Ω.

3. DESIGN OF A CC-CV LINEAR CHARGER FOR ENERGY-CONSTRAINED LOW-POWER APPLICATIONS*

3.1 Battery Chargers

As discussed in Chapter 1, charging a Li-ion battery needs precise regulation for battery health and safety. There are two popular types of battery chargers: a switching charger and a linear charger. Although a switching charger is highly power-efficient, it tends to be bulky and expensive due to an external inductor, causing electromagnetic interference (EMI) issues [49,50]. In contrast, a linear charger has the advantage of ripple-free, compact, on-chip implementation [11, 15]. Its efficiency is affected by V_{DS} drop of a power transistor and quiescent current (I_{Q}). The V_{DS} drop can be compensated by adaptive supply control schemes [12, 51, 52]. However, even though low I_{Q} design becomes increasingly important in the energy-constrained low-power applications, fast battery charging with low I_{Q} is still challenging due to multiple amplifiers for feedback regulation loops. The following section discusses a fast linear battery charger for low-power applications.

3.2 CC-CV Linear Charger for Energy-Constrained Low-Power Applications

A battery-powered system has widely expanded its applications to implantable medical devices (IMDs) and energy harvesting systems [1]. A constant current (CC)-constant voltage (CV) linear charger is popular for fast, stable, and ripple-free charging as well as compact implementation in the applications [11, 15], whereas a switching charger tends to be bulky and expensive due to an inductor, causing electromagnetic interference issues [10]. These energy-constrained low-power applications raise new challenges to linear charger design because even sub-mW power saving can be useful.

The CC-CV linear charger has three charging phases, i.e., a trickle-current (TC) phase, a CC phase, and a CV phase. Since CC regulation inherently conflicts with CV regulation, a seamless

*

CC-CV transition has long been a research goal in linear charger design. One of the solutions to the seamless CC-CV transition is a comparator-based transition, which selectively turns on a constant current source for the TC/CC phases or a variable current source for the CV phase [12, 14]. This transition requires multiple amplifiers for current source implementation and regulation. Moreover, oscillatory battery voltage [13] and spike battery charging current [14] are well-known design issues during the CC-CV transition.

To resolve these design issues, studies have preferentially used an analog transition method rather than digital. A diode-based transition [51], a smooth control circuit (SCC)-based transition [13, 53], and a subthreshold operational transconductance amplifier (OTA)-based transition [11] are reported. However, diode/SCC-based transitions require multiple amplifiers for regulation and additional bias current for the diodes and SCC. The subthreshold OTA-based transition suffers from low-speed linear settling for the CV phase, consuming extra current of cascaded current mirrors for large current gain.

This chapter proposes a unified amplifier-based linear lithium-ion (Li-ion) battery charger to achieve the seamless CC-CV transition, quiescent current (I_{Q}) reduction by sharing the bias current, and high unity-gain loop bandwidth (f_{unity}) for fast regulation. The rest of this paper is organized as follows. Section 3.3 presents circuit implementation of the proposed battery charger. Section 3.4 analyzes the stability of the charger. Measurement results are presented in Section 3.5, and the conclusions are drawn in Section 3.6.

3.3 Unified Amplifier-Based Linear Charger

Fig. 3.1 presents the simplified architecture of the proposed charger. The proposed unified amplifier merges amplifiers for CC/CV regulation, and removes the diodes or the SCC. It has three differential input ports, which individually handle CC regulation (CA), CV regulation (VA), and the seamless transition (SA). I_{SET} is reference current, and I_{BAT} is battery charging current. A hysteresis comparator, $\mathrm{CMP_{TC}}$, changes a current mirror ratio to generate charging current, I_{TC}

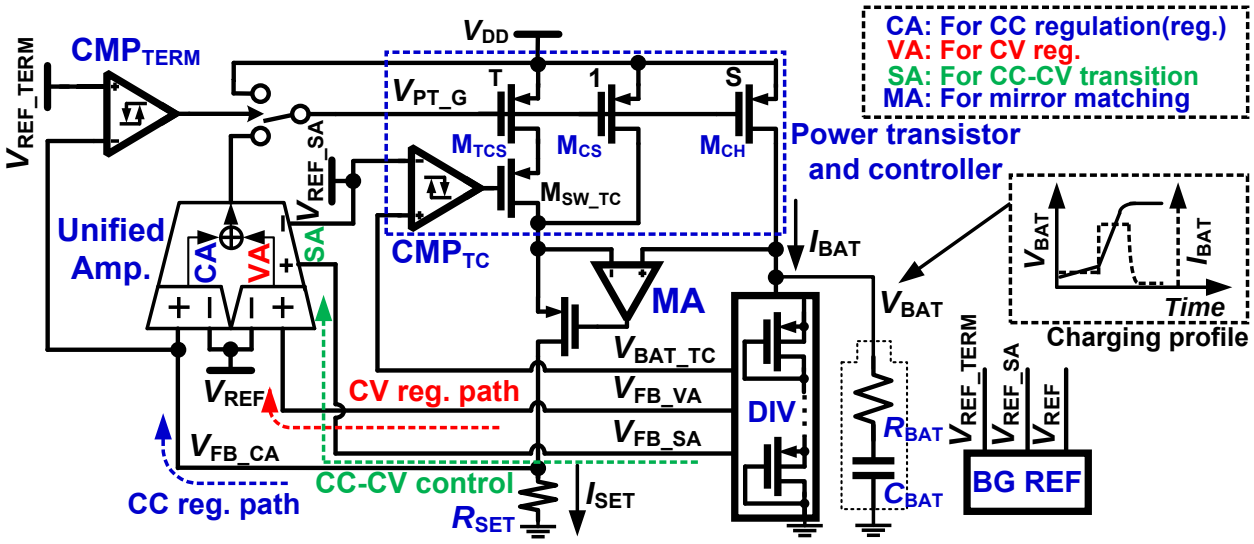


Figure 3.1: Simplified architecture of the unified amplifier-based charger.

and I_{CC}, during the TC/CC phase. Depending on $V_{\mathrm{BAT\_TC}}$ ($= \frac{5}{14} \cdot V_{\mathrm{BAT}}$), I_{BAT} is given by

$$I_{\mathrm{BAT}} = \begin{cases} S/(1+T) \cdot V_{\mathrm{FB\_CA}}/R_{\mathrm{SET}} & \text{in the TC phase,} \\ S \cdot V_{\mathrm{FB\_CA}}/R_{\mathrm{SET}} & \text{in the CC phase.} \end{cases} \tag{3.1}$$

where S and T are the sizing ratios of $\mathrm{M_{CH}}$ and $\mathrm{M_{TCS}}$ to $\mathrm{M_{CS}}$, respectively. Here, S and T are set to 1000 and 10, respectively.

The voltage divider, DIV, uses a string of 14 diode-connected PMOS devices to reduce static power consumption and the area. In the CV phase, the whole charging process is terminated by a hysteresis comparator, $\mathrm{CMP_{TERM}}$, when I_{BAT} is less than 7.5% of I_{CC} [15]. A bandgap reference [54] with 5-bit trimmable resistors generates voltages for each regulation and termination on-chip, which are 1.2 V for V_{REF}, 0.9 V for $V_{\mathrm{REF\_SA}}$, and 0.12 V for $V_{\mathrm{REF\_TERM}}$.

Fig. 3.2 shows the unified amplifier and its operations in the whole charging process. CA, VA, and SA share I_{BIAS}, and current-steering at SA makes a smooth CC-CV transition. The unified amplifier has a balanced differential pair (CA) and two unbalanced differential pairs (VA and SA). The unbalanced pairs are critical to implement tail current sharing and accurate CV regulation. We define the deep CC phase to distinguish it from the CC phase due to their different transistor oper-

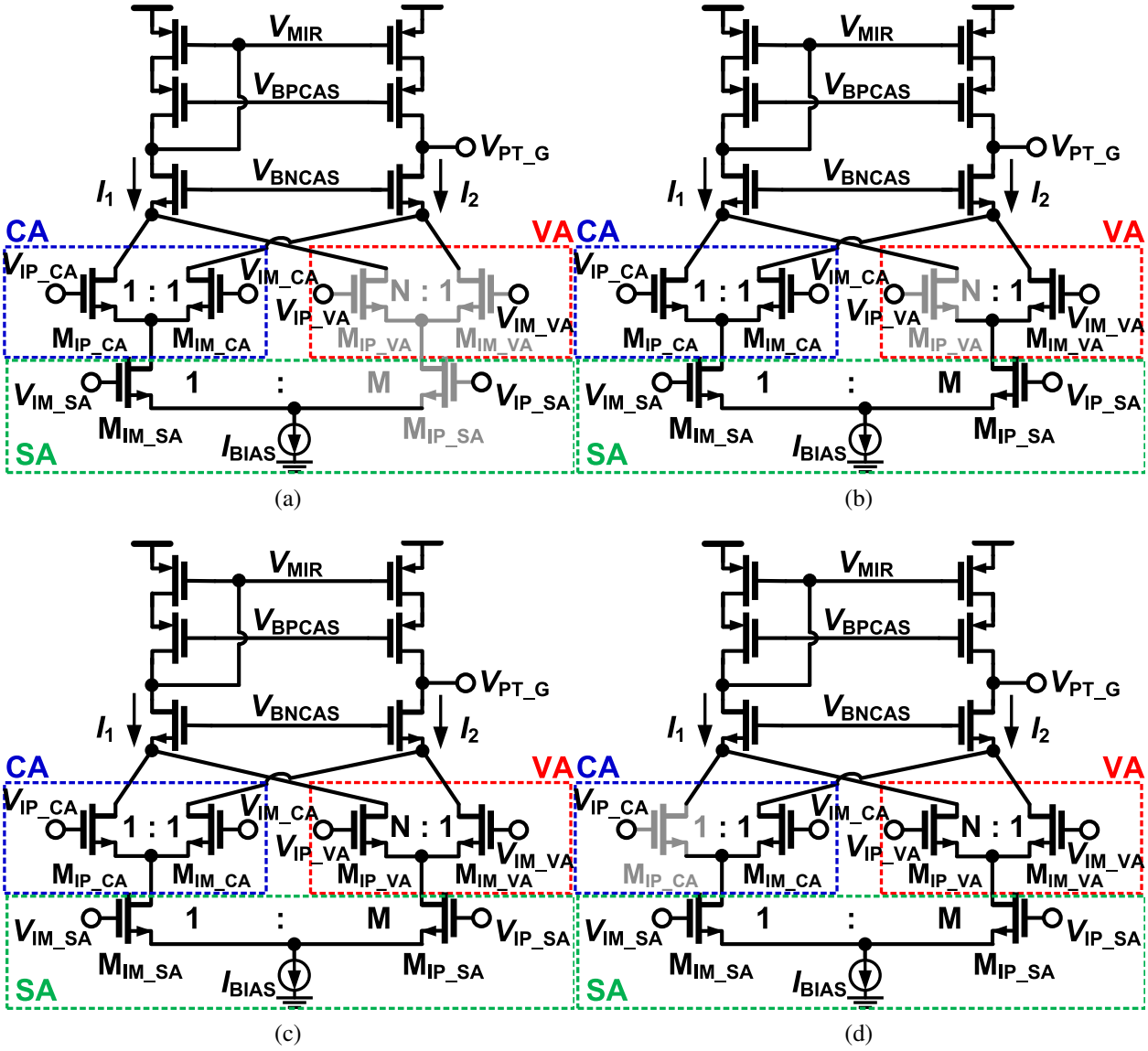


Figure 3.2: Unified amplifier and its operations in (a) the TC/deep CC phase, (b) the CC phase, (c) the CC-CV transition phase, and (d) the CV phase.

ations. Greyed transistors denote cut-off transistors. To understand transistor operations, it should be noted that $V_{\text{IM\_CA}}$ and $V_{\text{IM\_VA}}$ are connected to V_{REF}, and $V_{\text{IM\_SA}}$ is connected to $V_{\text{REF\_SA}}$. As shown in Fig. 3.1, $V_{\text{IP\_CA}}$, $V_{\text{IP\_VA}}$, and $V_{\text{IP\_SA}}$ are connected to $V_{\text{FB\_CA}}$, $V_{\text{FB\_VA}}$ ($= \frac{2}{7} \cdot V_{\text{BAT}}$), and $V_{\text{FB\_SA}}$ ($= \frac{3}{14} \cdot V_{\text{BAT}}$), respectively. In the TC phase and the deep CC phase, low V_{BAT} makes transistors for VA turn off, as shown in Fig. 3.2(a). Increasing V_{BAT} starts to make a portion of

the I_{BIAS} flow into $M_{\text{IP\_SA}}$, as shown in Fig. 3.2(b). However, V_{BAT} is not high enough to turn on $M_{\text{IP\_VA}}$ in this phase. Hence, the equivalent input-referred offset voltage of CA due to the output offset current from VA increases slowly as V_{BAT} increases. This offset voltage is acceptable because I_{CC} does not require high accuracy [10]. As V_{BAT} becomes high enough to turn on $M_{\text{IP\_VA}}$ like Fig. 3.2(c), both CA and VA are in the linear operation region. Increasing V_{BAT} reduces the equivalent input offset voltage of CA, and finally changes its polarity. As a result, the CC regulation loop forces $V_{\text{IP\_CA}}$ ($= V_{\text{FB\_CA}}$) to decrease. In Fig. 3.2(d), $M_{\text{IP\_CA}}$ is finally turned off, which disables CC regulation and enables CV regulation. The current through $M_{\text{IM\_CA}}$ offsets the unbalanced differential pair of VA, making voltages at $V_{\text{IP\_VA}}$ and $V_{\text{IM\_VA}}$ almost the same in the CV phase.

To determine the size ratios of the unbalanced differential pairs, M and N, we assume that $V_{\text{IP\_SA}} = V_{\text{IM\_SA}}$ and $V_{\text{IP\_VA}} = V_{\text{IM\_VA}}$ in Fig. 3.2(d) at the battery's fully charged voltage. Normalized output currents, I_1/I_{BIAS} and I_2/I_{BIAS}, in Fig. 3.2(d) are calculated as

$$\begin{aligned} I_1/I_{\text{BIAS}} &= M/(M+1) \cdot N/(N+1), \\ I_2/I_{\text{BIAS}} &= 1/(M+1) + M/(M+1)/(N+1). \end{aligned} \tag{3.2}$$

Therefore, the following condition from $(I_1 - I_2)/I_{\text{BIAS}} = 0$ should be satisfied to prevent unified amplifier saturation.

$$(M-1) \cdot (N-1) = 2. \tag{3.3}$$

Fig. 3.3 shows a contour plot of $(I_1 - I_2)/I_{\text{BIAS}}$ with respect to M and N and layouts of SA and VA at the design point. W(M_X) denotes the width of the MOSFET M_X. While a small fractional part of N increases layout complexity, small M makes $(I_1 - I_2)/I_{\text{BIAS}}$ sensitive to M's variation. Therefore, we set M and N to 4 and 5/3, respectively. SA and VA are laid out with large devices in a common centroid way. Device variation affects the input-referred offset voltage of the unified amplifier, which deteriorates accuracy of fully charged battery voltage. Reference voltage

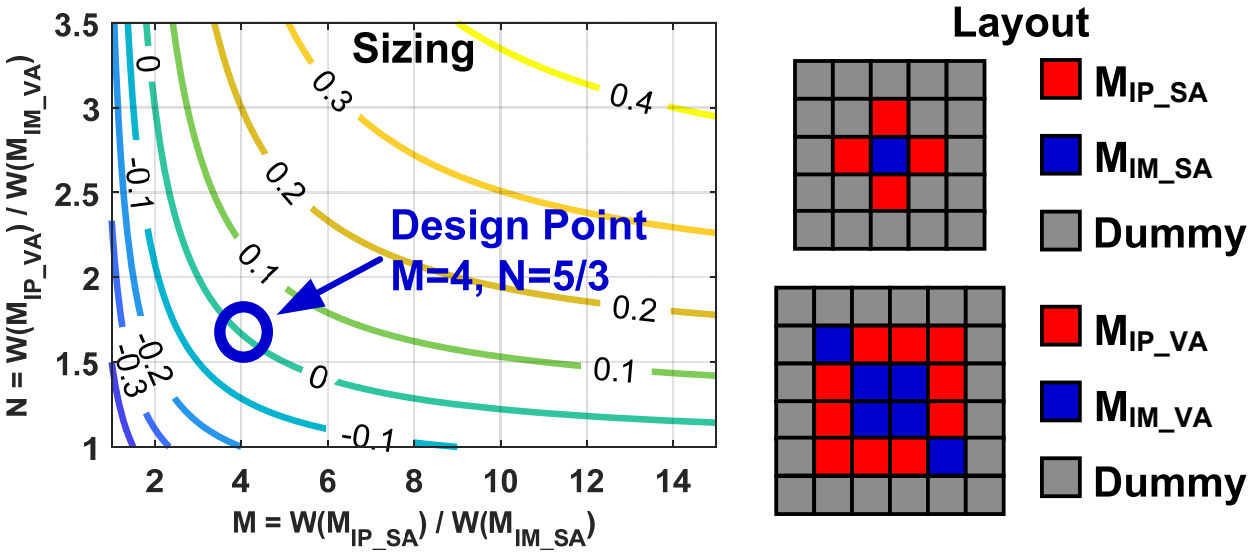


Figure 3.3: Contour plot of $(I_1 - I_2)/I_{\text{BIAS}}$ in the CV phase and layouts of SA and VA at the design point.

trimming can compensate for it.

Fig. 3.4 shows transient simulation waveforms of the proposed charger with $I_{\text{BIAS}} = 20\ \mu$A and $R_{\text{SET}} = 48\,k\Omega$. Battery capacitance, C_{BAT}, and the internal resistance, R_{BAT}, depend on battery capacity. For example, an 80-mAh battery has the maximum R_{BAT} of 460 mΩ at 50% state-of-charge (SOC) [55]. Moreover, an 8-mAh battery is reported with C_{BAT} and R_{BAT} of 26 F and 1 Ω, respectively [11]. We assume $R_{\text{BAT}} = 1\,\Omega$ and $C_{\text{BAT}} = 10$ mF to capture waveforms in the oscilloscope measurement [13]. For small R_{BAT} like 200 mΩ, charging waveforms are similar. Normalized currents (I_{NORM}) describe behavior of CA, VA, and SA. The normalized tail currents of CA and VA are defined as

$$I_{\text{T\_CA\_NORM}} = I_{\text{T\_CA}}/I_{\text{BIAS}},\ \ I_{\text{T\_VA\_NORM}} = I_{\text{T\_VA}}/I_{\text{BIAS}}. \tag{3.4}$$

Here, $I_{\text{T\_CA}}$ and $I_{\text{T\_VA}}$ are the raw tail currents of CA and VA, respectively. Also, the normalized

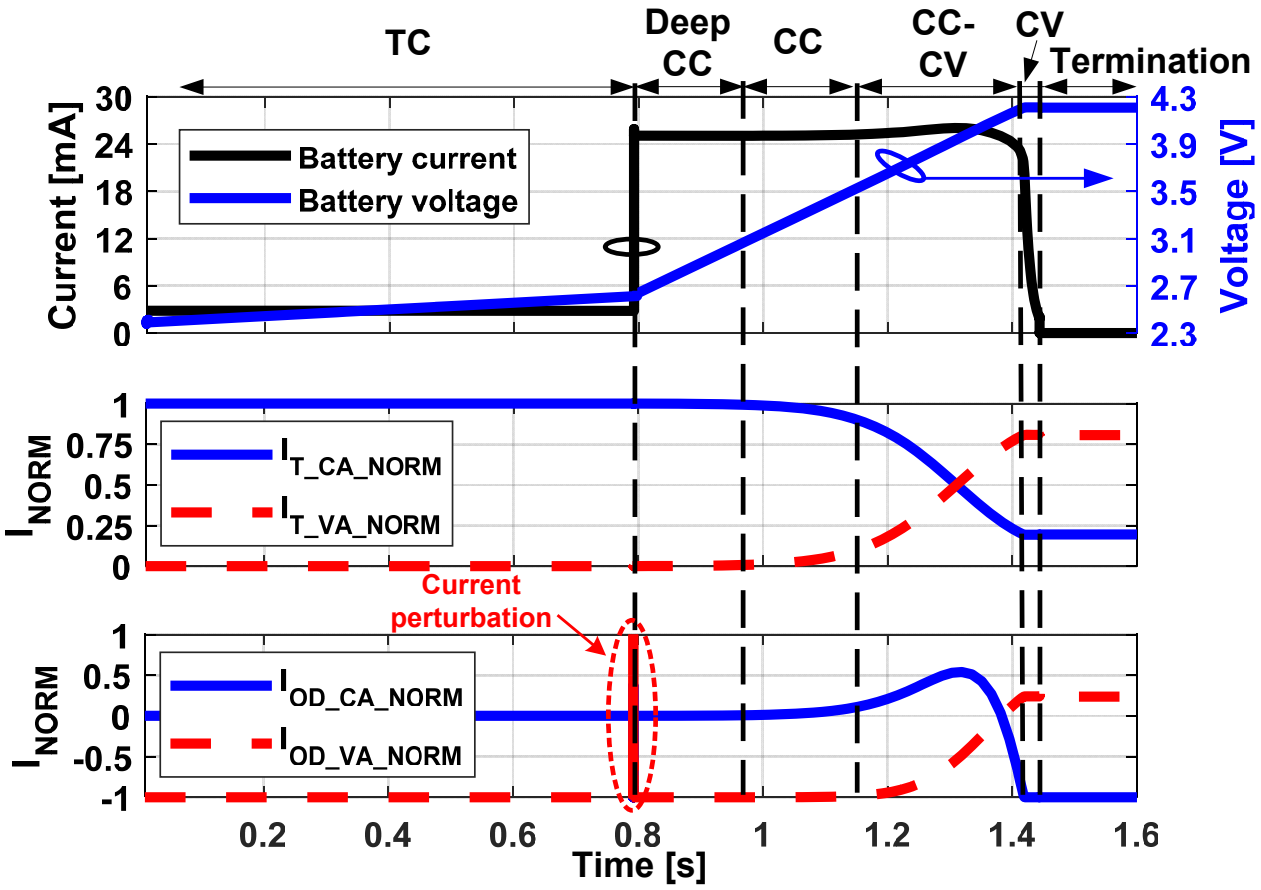


Figure 3.4: Transient charging waveforms with $C_{\mathrm{BAT}} = 10\,\mathrm{mF}$ and $R_{\mathrm{BAT}} = 1\,\Omega$.

output differential currents of CA and VA are defined as

$$I_{\mathrm{OD\_CA\_NORM}} = (I_{\mathrm{D\_M_{IP\_CA}}} - I_{\mathrm{D\_M_{IM\_CA}}})/I_{\mathrm{T\_CA}},$$
$$I_{\mathrm{OD\_VA\_NORM}} = (I_{\mathrm{D\_M_{IP\_VA}}} - I_{\mathrm{D\_M_{IM\_VA}}})/I_{\mathrm{T\_VA}}. \tag{3.5}$$

Here, $I_{\mathrm{D\_M_X}}$ denotes the drain current of the MOSFET $\mathrm{M_X}$. Waveforms in Fig. 3.4 agree well with the operations shown in Fig. 3.2. $I_{\mathrm{OD\_CA\_NORM}}$ and $I_{\mathrm{OD\_VA\_NORM}}$ are perturbed during the TC-deep CC transition because turning off $\mathrm{M_{SW\_TC}}$ in Fig. 3.1 drops $V_{\mathrm{FB\_CA}}$. However, fast regulation stabilizes it quickly.

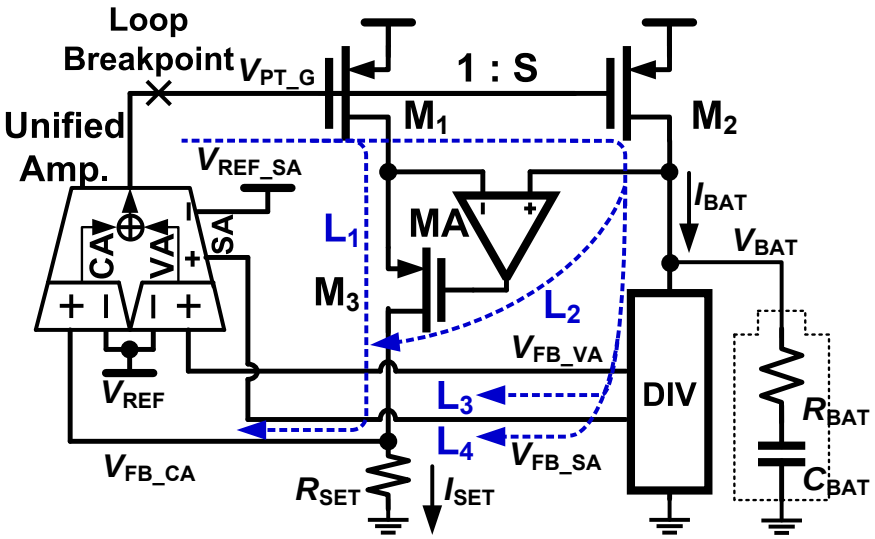


Figure 3.5: Simplified circuit diagram for the stability analysis.

3.4 Stability

Fig. 3.5 shows a simplified circuit diagram for the following stability analysis. Transconductance and output resistance of the MOSFET M_k are defined as g_{mk} and r_{ok}. $A_{CA}(s)$, $A_{VA}(s)$, $A_{SA}(s)$, and $A_{MA}(s)$ denote gain of CA, VA, SA, and MA, respectively. CA, VA, and SA have the same output pole at $-1/C_{out}r_{out}$ due to the gate capacitance of the power transistor and the output resistance of the unified amplifier. This pole forms the first non-dominant pole of the loop gain. MA's high-frequency pole is ignored.

Loop gain $T_k(s)$ corresponding to a loop L_k is given by

$$
\begin{aligned}
T_1(s) &\approx -A_0 \cdot (R_{SET}/r_{o1}) \cdot A_{CA}(s), \\
T_2(s) &\approx -T_1(s) \cdot \alpha \cdot (1 + s/z_{bat})/(1 + s/p_d), \\
T_3(s) &\approx -A_0\beta_{SA}A_{SA}(s) \cdot \delta \cdot (1 + s/z_{bat})/(1 + s/p_d), \\
T_4(s) &\approx A_0\beta_{SA}A_{SA}(s) \cdot (1 + s/z_{bat})/(1 + s/p_d),
\end{aligned}
\tag{3.6}
$$

where $A_0 = g_{m1}r_{o1} = g_{m2}r_{o2}$, $\alpha = 1 - 1/A_{MA}(s)$, $z_{bat} = 1/(C_{BAT}R_{BAT})$, $p_d = 1/(C_{BAT}r_{o2})$, and $\beta_{SA} = V_{FB\_SA}/V_{BAT}\,(= 3/14)$. Moreover, δ is defined as $\beta_{VA}A_{VA}(s)/(\beta_{SA}A_{SA}(s))$ where

$\beta_{\mathrm{VA}} = V_{\mathrm{FB\_VA}}/V_{\mathrm{BAT}}(= 2/7)$. δ is bias-dependent and larger than one. Note that the input polarity notation of SA in Fig. 3.5 is for tail current steering, not for SA's small signal gain. As shown in Fig. 3.2, SA has a negative gain.

In the TC phase and the deep CC phase, L_1 and L_2 are effective. Therefore, the combined loop gain is calculated as

$$T_{\mathrm{TC}}(s) \approx -A_0 \cdot (R_{\mathrm{SET}}/r_{\mathrm{o1}}) \cdot \frac{A_{\mathrm{CA}}(s)}{A_{\mathrm{MA}}(s)} \cdot \frac{1 + sA_{\mathrm{MA}}(s)/p_{\mathrm{d}}}{1 + s/p_{\mathrm{d}}}. \tag{3.7}$$

In the CC phase, L_1, L_2, and L_4 are effective. The combined loop gain in this phase is calculated as

$$T_{\mathrm{CC}}(s) \approx A_0\beta_{\mathrm{SA}}A_{\mathrm{SA}}(s) \cdot \frac{1 - s(R_{\mathrm{SET}}/r_{\mathrm{o1}}) \cdot \gamma/p_{\mathrm{d}}}{1 + s/p_{\mathrm{d}}}. \tag{3.8}$$

where $\gamma = A_{\mathrm{CA}}(s)/(\beta_{\mathrm{SA}}A_{\mathrm{SA}}(s)) \gg 1$. γ is bias-dependent but first-order frequency-independent because CA and SA have the same output pole. γ decreases in the CC phase due to tail current steering. Moreover, β_{SA} and SA's low transconductance make γ larger than one. The effect of high-gain positive feedback at low frequencies is discussed later.

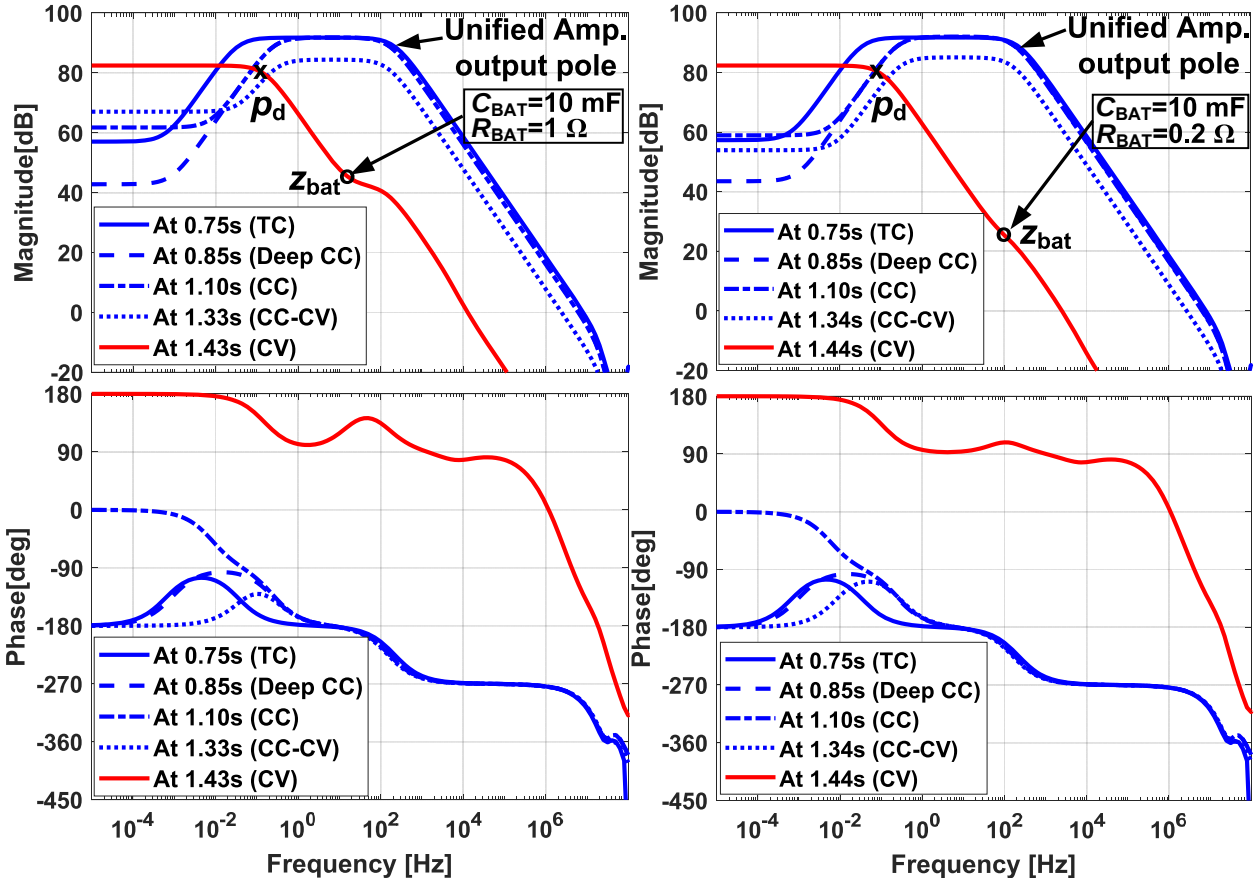
All the feedback loops are active in the CC-CV phase. The combined loop gain is given by

$$\begin{aligned} T_{\mathrm{CC\text{-}CV}}(s) \approx & -A_0\beta_{\mathrm{SA}}A_{\mathrm{SA}}(s) \cdot (\delta - 1) \\ & \cdot \frac{1 + s(R_{\mathrm{SET}}/r_{\mathrm{o1}}) \cdot \gamma/(\delta - 1)/p_{\mathrm{d}}}{1 + s/p_{\mathrm{d}}}. \end{aligned} \tag{3.9}$$

The zero frequency in the CC-CV phase increases in comparison with that in the CC phase as does the DC gain. δ increases in this phase because A_{VA} increases due to tail current steering.

L_3 and L_4 are active in the CV phase. The combined loop gain is calculated as

$$T_{\mathrm{CV}}(s) \approx -A_0\beta_{\mathrm{SA}}A_{\mathrm{SA}}(s) \cdot (\delta - 1) \cdot \frac{1 + s/z_{\mathrm{bat}}}{1 + s/p_{\mathrm{d}}}. \tag{3.10}$$



(a) (b)

Figure 3.6: Loop gain simulations (a) with $C_{\text{BAT}} = 10\,\text{mF}$ and $R_{\text{BAT}} = 1\,\Omega$, and (b) with $C_{\text{BAT}} = 10\,\text{mF}$ and $R_{\text{BAT}} = 0.2\,\Omega$.

As compared with the CC-CV phase, the DC gain is maintained in the CV phase, whereas the zero frequency increases.

Fig. 3.6 presents a loop gain simulation with different R_{BAT} for each charging phase, which agrees well with the above analysis. In an experiment with a real battery, larger C_{BAT} lowers both p_{d} and z_{bat}, which does not affect f_{unity} much.

High-gain positive feedback at low frequencies in the CC phase gives a low-frequency RHP pole and a high-frequency LHP pole to the closed-loop system. From (3.8), the closed-loop RHP

pole location can be approximated to

$$p_{\text{closed,RHP}} \approx p_{\text{d}}/\{(R_{\text{SET}}/r_{\text{o1}}) \cdot \gamma\}, \tag{3.11}$$

which is the same as the RHP zero location of $T_{\text{CC}}(s)$ because high-gain feedback makes the closed-loop pole move from the open-loop pole location to the open-loop zero location in the root locus analysis.

Bounded CC phase duration limits the effect of the above RHP pole. A pessimistic estimate for the CC phase duration can be calculated as

$$t_{\text{CC}} \approx C_{\text{BAT}} \Delta V_{\text{CC}}/(S \cdot V_{\text{REF}}/R_{\text{SET}}). \tag{3.12}$$

Here, the ΔV_{CC} is a battery voltage change in the CC phase, and S is the size ratio of the power transistor. Therefore, the effect of the RHP pole is given by

$$e^{p_{\text{closed,RHP}} \cdot t_{\text{CC}}}\big|_{\text{pessimistic}} \approx e^{\frac{\Delta V_{\text{CC}}}{V_{\text{REF}} \cdot \gamma}} \approx 1. \tag{3.13}$$

Here, the worst case ΔV_{CC} is about 0.5 V from Fig. 3.4, and the other parameter values are $V_{\text{REF}} = 1.2\,\text{V}$, $R_{\text{SET}} = 48\,k\Omega$, and $r_{o1} = S \cdot r_{o2} = 55\,k\Omega$. The factor γ varies. However, it is much larger than one. This can be confirmed from the simulations in Fig. 3.6(a), where a ratio of the dominant pole frequency to the zero frequency is much larger than one in the CC phase. Therefore, the effect of the RHP pole in the CC phase is negligible.

The closed-loop dominant pole locus in Fig. 3.7 is found by using the loop gain simulation data in MATLAB. Fig. 3.7 verifies that the bounded CC phase duration limits the effect of the closed-loop RHP pole. As predicted by the root locus analysis, high loop gain makes the closed-loop dominant pole close to the open-loop zero location which moves across the $j\omega$ axis of the s-plane twice during the whole charging process.

To test the stability, Fig. 3.8 compares battery voltage and current (V_{BAT} and I_{BAT}) under

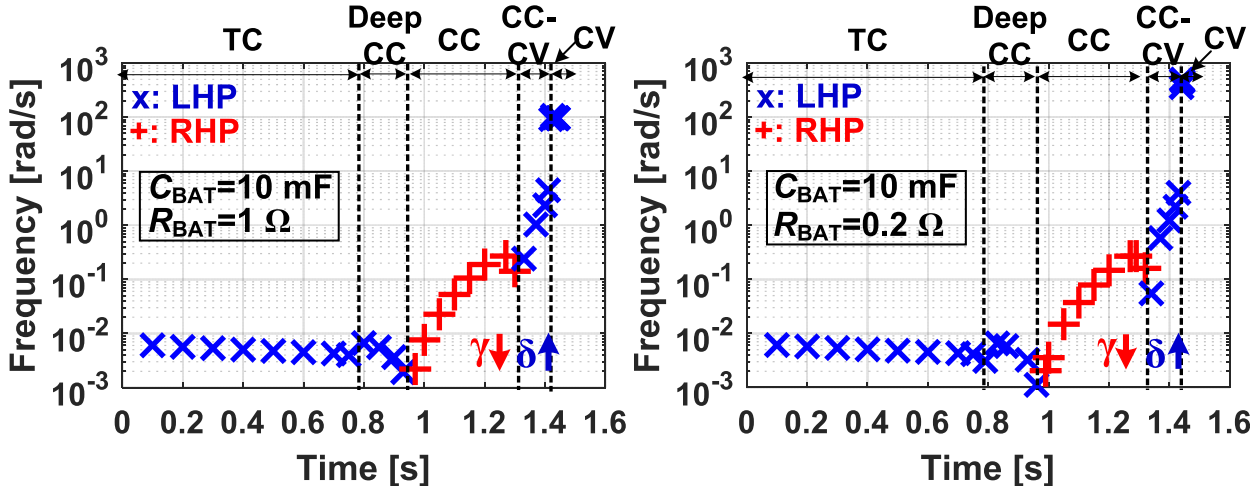


Figure 3.7: Closed-loop dominant pole locus (a) with $C_{\text{BAT}} = 10\,\text{mF}$ and $R_{\text{BAT}} = 1\,\Omega$, and (b) with $C_{\text{BAT}} = 10\,\text{mF}$ and $R_{\text{BAT}} = 0.2\,\Omega$.

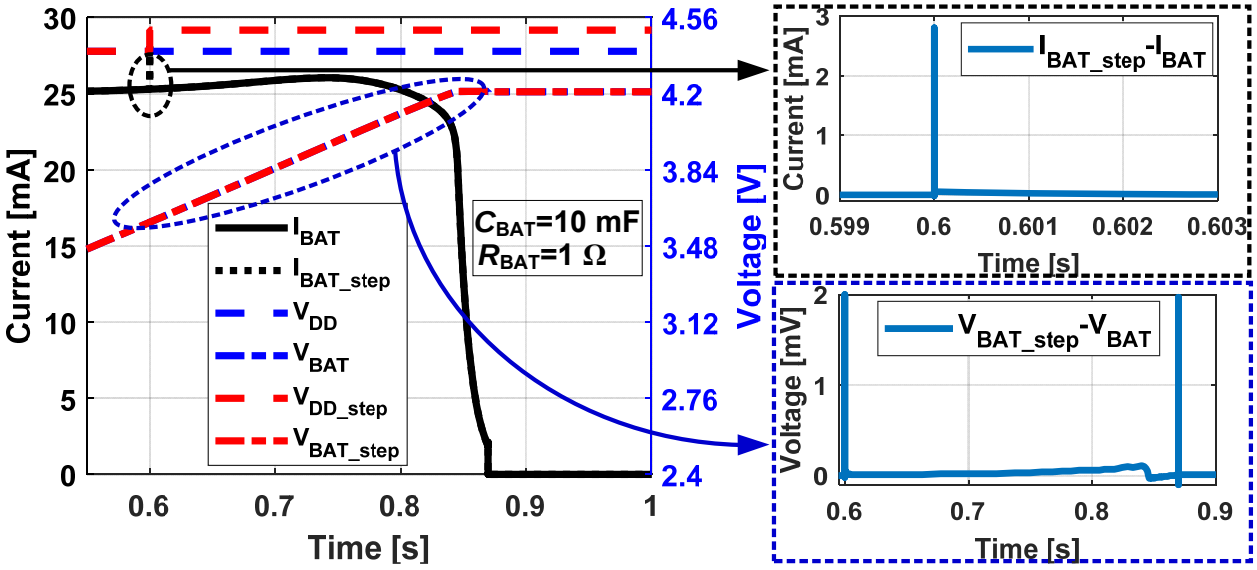


Figure 3.8: Power supply step response simulation with $C_{\text{BAT}} = 10\,\text{mF}$ and $R_{\text{BAT}} = 1\,\Omega$.

nominal supply voltage V_{DD} with those ($V_{\text{BAT\_step}}$ and $I_{\text{BAT\_step}}$) when the supply voltage steps up by 100 mV ($V_{\text{DD\_step}}$). A spiked current occurs when the supply voltage steps up. However, fast regulation recovers it quickly. Spiky battery voltage differences are also observed temporarily when the supply voltage steps up, or the charging process ends. Battery voltage difference starts

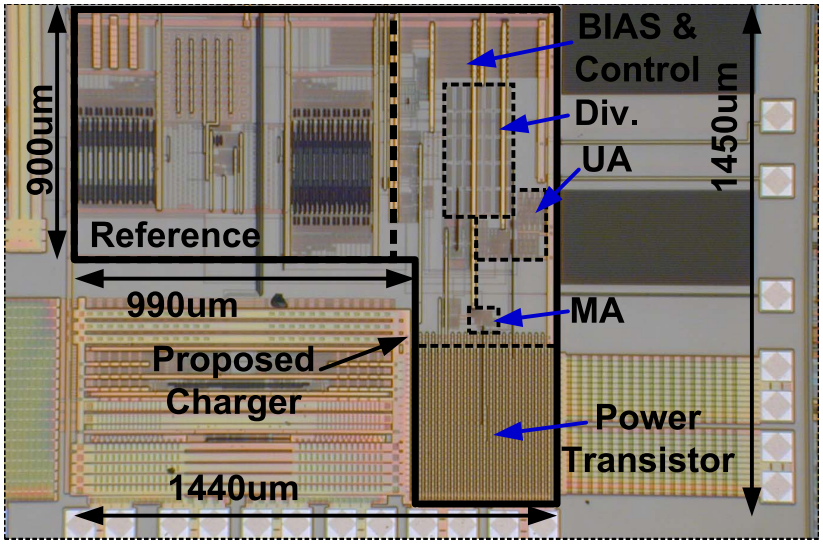


Figure 3.9: Chip micrograph of the battery charger circuit.

to increase slightly after the step disturbance in the CC phase. However, it is negligible, and there is virtually no difference between final voltages.

3.5 Measurement Results

The proposed charger is fabricated in TSMC 2P4M 0.35 μm CMOS process. A die micrograph is shown in Fig. 3.9. The active area of the battery charger is 2.09 mm^2 (1.44 mm $\times$ 1.45 mm). However, the core blocks occupy a small portion of the total area. The power transistor, the unified amplifier, the MA, and the divider occupy 0.189 mm^2 (0.43 mm $\times$ 0.44 mm), 0.04 mm^2 (0.20 mm $\times$ 0.20 mm), 0.0054 mm^2 (0.09 mm $\times$ 0.06 mm), and 0.076 mm^2 (0.20 mm $\times$ 0.38 mm), respectively. Since the area for reference, bias, and control was not optimized due to an irrelevant design at the bottom left corner of Fig. 3.9, there is room for improvement. Also, a state-of-the-art voltage reference circuit can reduce its area down to 0.0025 mm^2 [56]. Therefore, the total area can be enhanced significantly without the irrelevant design.

The supply voltage and the fully charged battery voltage are set to 4.4 V and 4.2 V, respectively. Moreover, threshold voltage for the TC-CC transition, $V_{\text{TC-CC}}$, is set to 2.66 V. To observe the whole charging process within a short space of time, we use C_{BAT} of 10 mF and R_{BAT} of 1 Ω to emulate a Li-ion battery [11, 13]. Charging currents, I_{TC} and I_{CC}, are set to 2.273 mA and 25

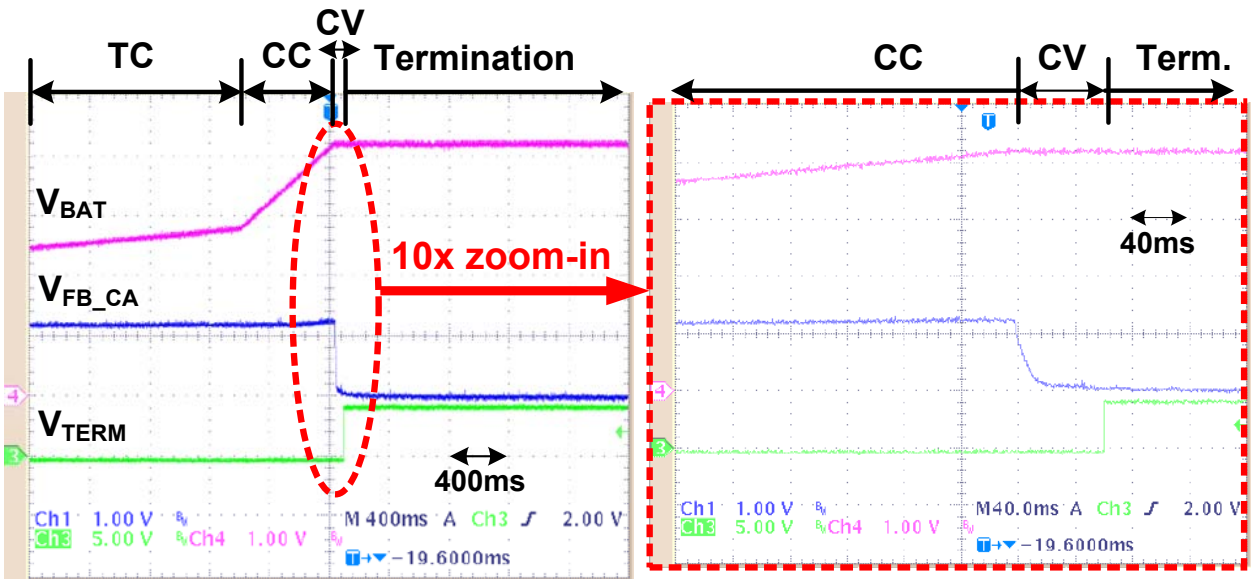


Figure 3.10: Charging waveforms with C_{BAT} = 10 mF and R_{BAT} = 1 Ω.

mA. Fig. 3.10 shows one shot capture of the charging waveforms by Tektronix TDS3054. A top waveform and a middle waveform displays V_{BAT} and $V_{\mathrm{FB\_CA}}$ in Fig. 3.1, respectively. V_{TERM} is a termination flag signal, which is set when I_{BAT} is less than $0.075 \cdot I_{\mathrm{CC}}$. Since I_{TC} and I_{CC} are set by the current mirror ratio according to (3.1), $V_{\mathrm{FB\_CA}}$ maintains its level when the charger enters the CC phase from the TC phase. However, $V_{\mathrm{FB\_CA}}$ decays exponentially in the CV phase, which means I_{BAT} also decays in the same fashion. The measured waveforms show a smooth CC-CV transition.

Fig. 3.11 shows the measured results of battery current, battery voltage, and charger efficiency with a commercial battery, Renata rechargeable 80-mAh Li-ion polymer battery. Its fully charged voltage, nominal voltage, and cut-off voltage are 4.2 V, 3.7 V, and 3 V, respectively [55]. Although this battery has a 3-V cut-off voltage, there is no problem with verifying a smooth CC-CV transition of the proposed charger. The maximum charging current error was 5.5% of 25 mA, and the final battery voltage was 4.208 V, which is about 0.2% error of 4.2 V. Regarding charger efficiency defined as $V_{\mathrm{BAT}} \cdot I_{\mathrm{BAT}} / \{V_{\mathrm{DD}} \cdot (I_{\mathrm{Q}} + I_{\mathrm{BAT}})\}$, peak/average charger efficiencies were 94% and 88%, respectively.

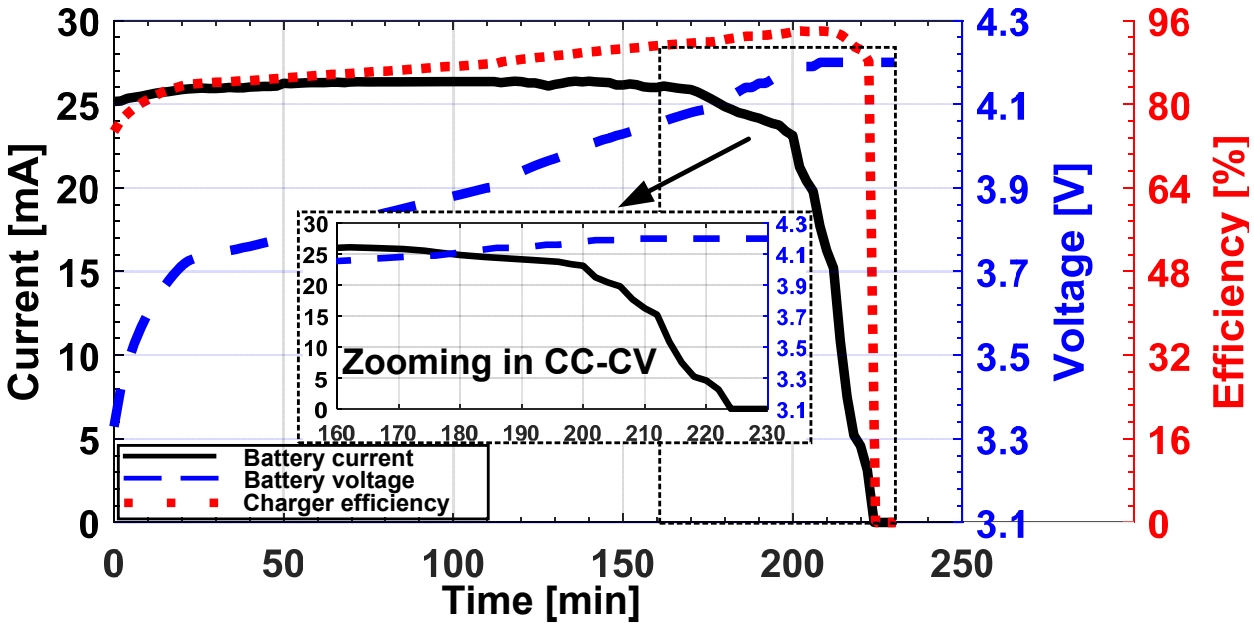


Figure 3.11: Measured battery current, battery voltage, and charger efficiency with an 80-mAh Li-ion polymer battery.

Table 3.1 compares the proposed charger with chargers described in previous works. Direct comparisons among them are not easy because I_{CC} depends on applications, and different chargers reported different charging rates or no charging rates in their experiments. Although the charger proposed in [11] achieves good average efficiency, its low f_{unity} of the feedback loop gain makes linear settling of the OTA slow in the CV phase, which is not adequate for fast charging. In contrast, f_{unity}s of [53] and this work in the CC-CV/CV phases are high because they are relatively independent of battery capacitance. However, this work uses a single amplifier for CC-CV control, while [53] uses multiple amplifiers. Consequently, our work achieves high peak/average charger efficiencies with reduced I_Q under fixed power supply voltage.

3.6 Conclusion

We presented and experimentally verified the unified amplifier-based CC-CV linear charger for energy-constrained low-power applications. The proposed charger achieves the seamless CC-CV transition with lower I_Q because its unique structure using current steering shares one tail current source among stacked differential pairs for regulation and the transition unlike conventional

Table 3.1: Linear Li-Ion Battery Charger Comparison

	This Work	[52] TPEL, 2017	[53][A.] TCAS2, 2017	[12] TIE, 2015	[11] TBCAS, 2011
Technology	0.35um CMOS	0.35um CMOS	0.13um BCD 6V	0.18um CMOS	0.5um CMOS
Supply Voltage [V]	4.4	Max 5.7 Adaptive[B.]	5	4.7	4.3
Charging Modes	TC-CC-CV	TC-CC-CV	TC-CC-CV	TC-CC-CV	TC-CC-CV
CC-CV control circuits	Unified amplifier	CA+VA +diode	CA+VA +SCC[C.]	Comparators +Variable current source	1 OTA + current gain
I_{CC} [mA]	25	500	495	450	2.8
Charging rate [C]	0.31	N/A	0.66	N/A	0.35
Peak efficiency [%]	94	88.3	83.9	83	N/A
Avg. efficiency [%]	88	N/A	N/A	79	89.7
f_{unity} of the loop gain [Hz]	2M(CC-CV) 14k[D.]/10k[E.](CV)	N/A	0.3M[F.](CC-CV) N/A(CV)	N/A	N/A(CC-CV) 175u[E.](CV)
Max I_Q for CC-CV control [uA]	58[G.]	N/A	N/A	N/A	102[H.]

[A.] With built-in resistance compensation [B.] Integrated buck converter [C.] SCC: Smooth Control Circuit

[D.] C_{BAT}=10 mF, R_{BAT}=1 Ω [E.] C_{BAT}=26 F, R_{BAT}=1 Ω [F.] C_{BAT}=infinity, R_{BAT}=N/A

[G.] I_{SET}(25 uA) + Unified amp. I_{BIAS}(20 uA) + Unified amp. bias circuits (13 uA)

[H.] OTA bias current (0.25 uA) + 3-stage current gain block (101.625 uA). Assume each stage's current gain is the same ($22400^{1/3}\approx 28$)

linear chargers. High f_{unity} of the feedback loop gain enables fast regulation, and avoids slow linear settling for the CC-CV/CV phases. A peak charger efficiency of 94% and average charger efficiency of 88% are achieved with an 80-mAh Li-ion polymer battery.

4. DESIGN OF A SUBRANGING PIPELINED-SAR ADC USING A TEMPERATURE-INSENSITIVE TIME-BASED AMPLIFIER*

4.1 SAR ADC and Pipelined ADC

For low-to-moderate resolution data conversion, a successive approximation register (SAR) analog-to-digital converter (ADC) [57–59] benefits from dynamic operation and no need for high-gain amplifiers as the feature size of CMOS technology scales down, thereby resulting in the best energy efficiency. However, the energy efficiency of a SAR ADC is degraded in high resolution and high speed [60–63] design because of a strict noise requirement for comparator design and an inherent serial conversion process.

To overcome the problem, a pipeline technique [64, 65] can play a continuing role for high speed and high resolution conversion. In the design space of moderate-to-high speed and resolution, a pipelined ADC has been a dominant ADC architecture. Each pipeline stage is conventionally based on a capacitor array multiplying DAC (MDAC) [66]. However, the MDAC requires a high-gain high-speed OTA for accuracy and speed, which is power-consuming and difficult to design in advanced CMOS technology. Increasing the stage resolution relaxes the MDAC accuracy requirement, but this strategy leads to increase in power consumption of a conventional flash sub-ADC.

4.2 A Hybrid Architecture: Pipelined SAR

For high speed and high resolution applications, a pipelined SAR ADC [67–75] is a promising architecture which combines two moderate resolution SAR ADCs with an inter-stage residue amplifier. Compared with a conventional pipeline ADC, this architecture allows a higher first-stage resolution to improve linearity while it avoids a front-end sample-and-hold amplifier. This is because signal sampling, SAR operations, and residue holding are made on the same CDAC array.

*

Compared with a conventional high resolution SAR ADC, a stage redundancy of the pipelined-SAR ADC significantly relaxes a comparator noise requirement and the pipelined operation breaks the speed bottleneck of a conventional SAR ADC. Furthermore, noise and linearity requirements of the second stage can be mitigated dramatically as well because of inter-stage gain.

While the pipelined-SAR architecture features the aforementioned benefits, it encounters a few design challenges. First, it still requires a high-gain high-speed amplifier to enable precise large inter-stage gain after a large number of bits are resolved in the first stage. A conventional telescopic OTA-based switched-capacitor (SC) residue amplifier [67–69] is power hungry and technology scaling-unfriendly with limited output swing and long settling time. As an alternative, a ring amplifier-based SC residue amplifier [72] has the advantage of energy-efficient slew-based charging as well as a nearly rail-to-rail output swing. However, it has an inherent stability issue due to its ring operation and requires high threshold voltage devices additionally to accomplish high gain. A dynamic amplifier [73–77] is also attractive to a pipelined-SAR ADC because it operates as a time-domain integrator with the benefit of noise filtering [73] and an inherent dynamic feature. However, its open loop nature makes it sensitive to process, supply voltage, and temperature (PVT). Therefore, background calibration [73, 75] is essential to achieve accurate inter-stage gain. Second, the linearity requirement of the first-stage CDAC must satisfy that of the whole ADC regardless of the resolution of the first-stage SAR ADC because DAC errors are reflected into residual voltage and cannot be corrected by digital error correction. Digital calibration [70, 73] can be used to eliminate a mismatch error but increases design complexity. In this regard, high linearity switching algorithms [72, 78] are attractive because they usually accomplish both low switching energy and high linearity simultaneously.

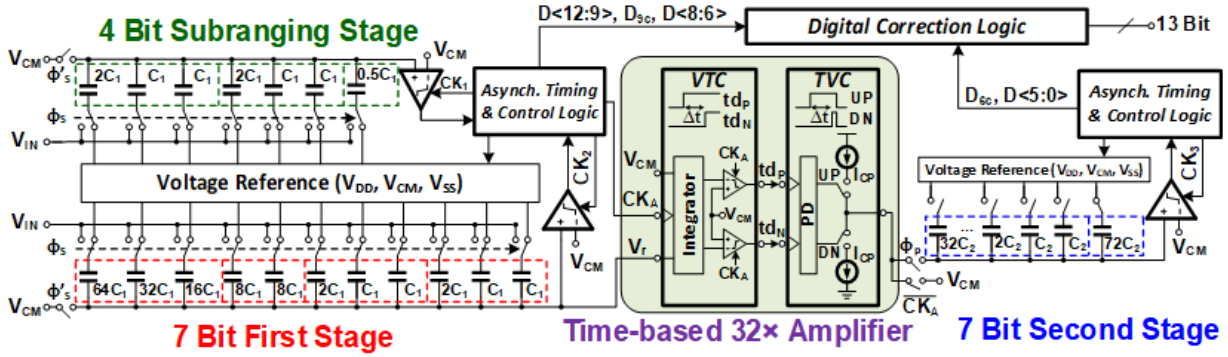
In this chapter, we explore a 13-bit subranging pipelined-SAR ADC with a temperature-insensitive time-based residue amplifier. First, this work improves the accuracy and energy efficiency of the CDAC in the first-stage SAR ADC through the SAR-assisted subranging floating capacitor switching algorithm. Second, a 32$\times$ technology scaling-friendly time-based residue amplifier is presented to overcome the issues of PVT variation and small inter-stage gain in conventional dy-

namic amplifier through time information. Third, this work also presents a pre-window technique adopted by the asynchronous SAR control logic to accelerate SAR logic operation. With the techniques presented above, the prototype ADC achieves Walden FoMs of 4.0-11.3 fJ/conversion-step with a Nyquist frequency input at 10-to-50 MS/s in a scalable power supply voltage range of 0.8-to-1.2 V.

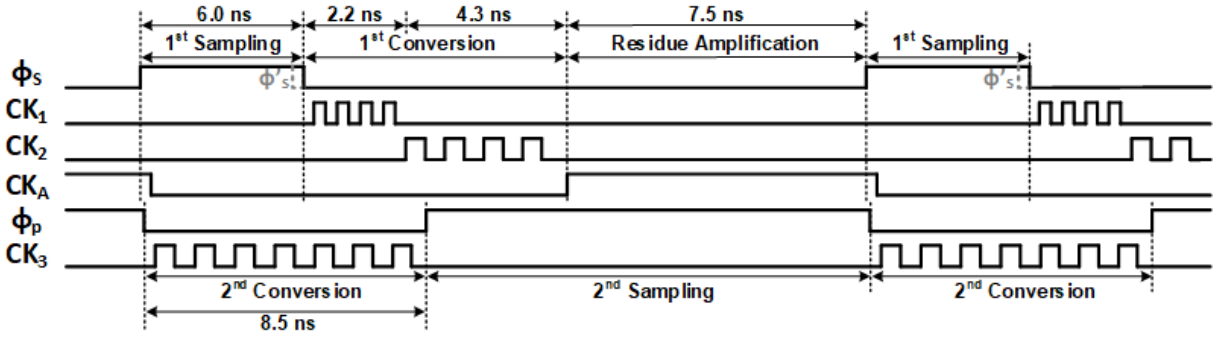
This chapter is organized as follows. Section 4.3 presents the architecture of the prototype ADC. Section 4.4 shows how the SAR-assisted subranging floating capacitor switching improves both linearity and switching energy. Section 4.5 describes the principle and implementation of the temperature-insensitive time-based residue amplifier. Section 4.6 discusses the pre-window-based asynchronous SAR logic. Section 4.7 presents the measurement results. Finally, conclusions are drawn in Section 4.8.

4.3 ADC Architecture

The overall ADC architecture is described in Fig. 4.1(a). Each 7-bit first stage and second stage SAR ADC is connected by a 32$\times$ time-based residue amplifier with one inter-stage redundancy bit. In the 7-bit first-stage SAR ADC, the first four most significant bits (MSBs) are resolved by a subranging stage [57], which is a 4-bit SAR ADC. One redundancy bit is inserted between the subranging stage and the first stage to cover the mismatch between them. The subranging architecture in [57] sets the capacitors in the first stage after the subranging stage completely finishes bit decisions, which slows down the comparison cycling loop of the total SAR ADC. However, the subranging floating capacitor architecture in our work (detailed in the Section 4.4.3) sets the partial floating capacitors in the first-stage SAR ADC immediately after the corresponding decision bit from the subranging stage is acquired. Moreover, compared with the big and small DAC architecture [71–73], the subranging operation in our work has lower comparator energy consumption because the first four bits are acquired by a low resolution comparator while maintaining the benefits of high energy efficiency, high linearity, and a fast SAR bit cycling loop. Bottom plate input sampling is adopted in the subranging stage and the first stage to avoid the gain error caused by parasitic capacitance on the top plate of CDAC and comparator input, and at the same time, it



(a)



(b)

Figure 4.1: (a) Block diagram and (b) timing diagram of the subranging pipelined-SAR ADC at 50MS/s.(Actual implementation is fully differential)

enhances the accuracy of sampling process.

The 32× time-based residue amplifier shown in Fig. 4.1(a) consists of a dynamic integrator-based voltage-to-time converter (VTC) and a charge pump-based time-to-voltage converter (TVC). The residue voltage stored in the first-stage CDAC is converted to time difference Δt by a dynamic integrator [76] and a zero-crossing detector. The time difference is restored to voltage information by a phase detector (PD) and a charge pump [79]. The gain sensitivity to temperature and supply voltage variations is compensated by a time-based two-step conversion, which will be discussed in Section 4.5. The output current of the charge pump is integrated on the top plate of the 7-bit second-stage SAR ADC's CDAC to minimize parasitic capacitor charging. Half-full scale range design [70] is adopted in the second-stage SAR ADC to relax the gain of the residue amplifier from 64× to 32× for linearity considerations.

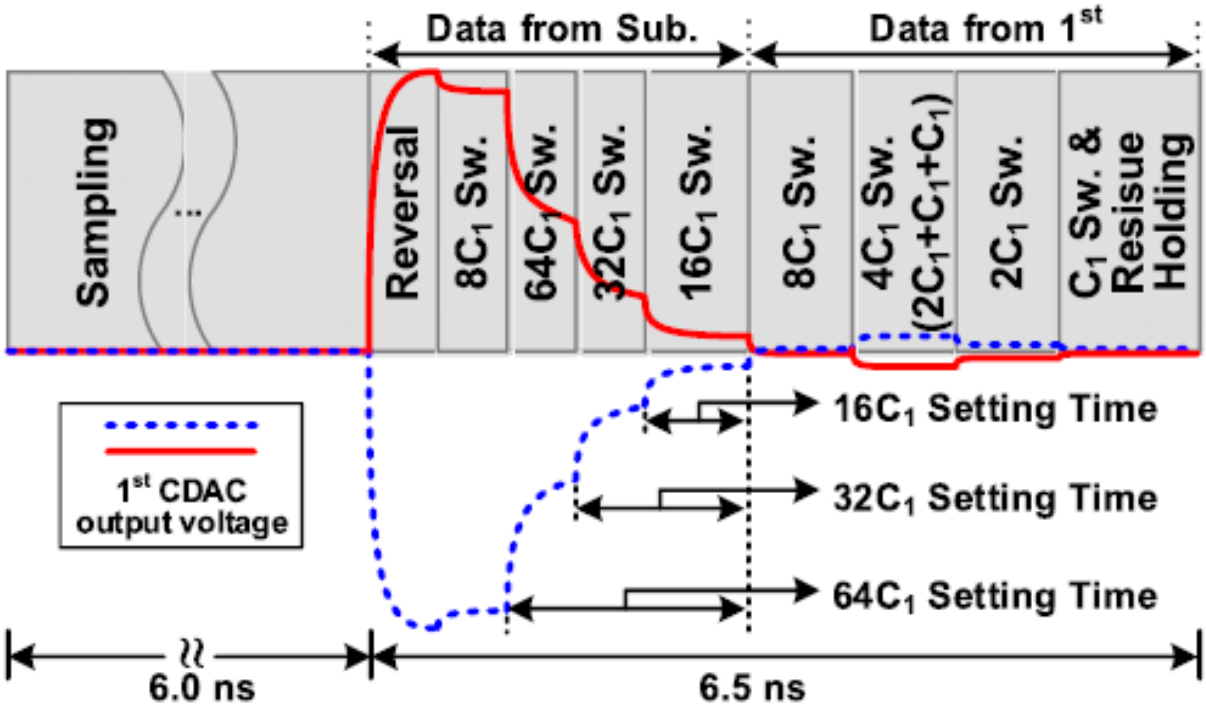
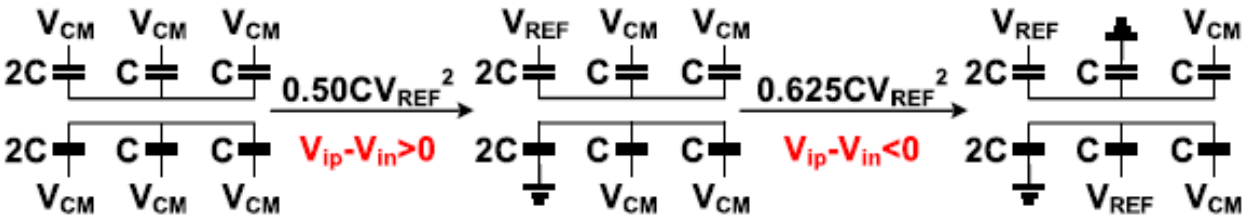


Figure 4.2: First-stage CDAC output voltage during sampling, subranging, and first-stage conversion at 50 MS/s.

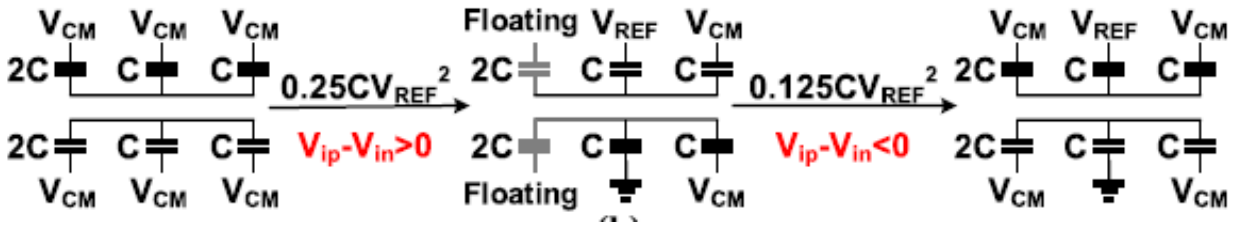
Fig. 4.1(b) shows the timing diagram of the overall ADC. The ADC requires a 30% duty cycle external clock ϕ_S for sampling, and all the other comparison clocks and control signals are asynchronously generated on chip. For example, when the pipelined-SAR ADC works at 50 MS/s with a 1.2 V power supply, the first-stage SAR ADC spends 6.0 ns for input sampling and 6.5 ns for the subranging-stage operation (2.2 ns) and first-stage CDAC setup. The remaining 7.5 ns is used for residual amplification and the system margin. The second-stage SAR ADC spends 8.5 ns for data conversion. Fig. 4.2 shows the differential output voltage of CDAC in the first stage. The settling time of the first three capacitors in the first stage is significantly relaxed because of the subranging operation. The detailed switching procedure is addressed in the Section 4.4.3.

4.4 SAR-Assisted Subranging Floating Capacitor Switching Technique in the First Stage

An energy-efficient and highly linear CDAC is essential in high resolution and low power pipelined-SAR ADC design. This section explains how the subranging floating capacitor switch-



(a)



(b)

Figure 4.3: (a) V_{CM}-based switching and (b) partial floating capacitor switching energy consumption for a 3-bit CDAC ($V_{\text{REF}} = 2V_{\text{CM}}$). ($V_{\text{ip}}$ and V_{in} are the output voltages of CDAC.)

ing technique improves linearity and reduces switching energy in the first-stage SAR ADC.

4.4.1 Review of energy saving of the partial floating capacitor switching technique

The partial floating capacitor switching technique in [80] reduces switching energy consumption by interchanging the switching order of the largest capacitor with the second largest one. Fig. 4.3 shows an example of a 3-bit CDAC switching energy consumption of the VCM-based switching technique [81, 82] and the partial floating capacitor switching technique. To illustrate an energy saving at each decision step, the decision steps of the first two bits "10" are considered here. In comparison with the V_{CM}-based switching technique, the partial floating capacitor switching technique can save switching energy through two approaches. First, the largest capacitor is made floating when the second bit is determined. This avoids additional charging to the largest capacitor and leads to a 50% energy savings in comparison with the V_{CM}-based switching technique (from $0.50\text{CV}_{\text{REF}}^2$ to $0.25\text{CV}_{\text{REF}}^2$ in Fig. 4.3). Second, when the first bit decision is different from the second bit decision, the floating capacitors are reconnected to V_{CM}, and this results in an 80% reduction of switching energy in comparison with the V_{CM}-based switching (from $0.625\text{CV}_{\text{REF}}^2$ to $0.125\text{CV}_{\text{REF}}^2$ in Fig. 4.3).

4.4.2 Linearity Analysis of the partial floating capacitor switching technique

In this section, we address the INL characteristic of the partial floating technique and the effect of parasitic capacitors on the linearity of the CDAC. The partial floating technique reduces INL error (not mentioned in [80]) because V_{CM} is utilized as a reconstruction reference to the MSB capacitor between 1/4 V_{FS} and 3/4 V_{FS}. As explained in [81, 82], the worst case INL for an N-bit V_{CM}-based switching CDAC is expected to occur at the mid-scale code, and its value is

$$\sigma[INL_{\text{max}}]_{\text{V}_{\text{CM}}\text{-based}} = \sqrt{2^{N-2}} \cdot \frac{\sigma_0}{C_0}[LSB] \tag{4.1}$$

where σ_0 is the standard deviation of the unit capacitor C_0. For the partial floating capacitor array, the worst case INL occurs at 1/4 V_{FS} and 3/4 V_{FS}, which is

$$\sigma[INL_{\text{max}}]_{\text{partial floating-based}} = \frac{\sqrt{3}}{2} \cdot \sqrt{2^{N-2}} \cdot \frac{\sigma_0}{C_0}[LSB] \tag{4.2}$$

This value is the same as the INL error at 1/4 V_{FS} and 3/4 V_{FS} of the V_{CM}-based switching because they have the same switching sequence from 0 to 1/4 V_{FS} and from 3/4 V_{FS} to V_{FS}. So, the partial floating technique relaxes the matching requirement between the unit capacitors by a factor of $2/\sqrt{3}$ in comparison with the V_{CM}-based switching.

However, the top and bottom plate parasitic capacitance deteriorates the performance of the partial floating-based SAR ADC. Depending on whether the largest capacitor is floating or not, the weight of parasitic capacitance to the CDAC varies, and this generates a non-binary scaled voltage step during bit cycling. Fig. 4.4 models how large the top and bottom plate parasitic capacitance affects the SNDR of a 13-bit pipelined-SAR ADC with a 7-bit partial floating-based first-stage SAR ADC. Through MATLAB modeling, 2% top and bottom plate parasitic capacitance decreases the ENOB of the 13-bit ADC to around 10 bit. Therefore, the partial floating capacitor switching technique is not suitable for high-resolution ADCs, and the SAR-assisted subranging floating capacitor switching technique is presented in our work to solve the aforementioned issues.

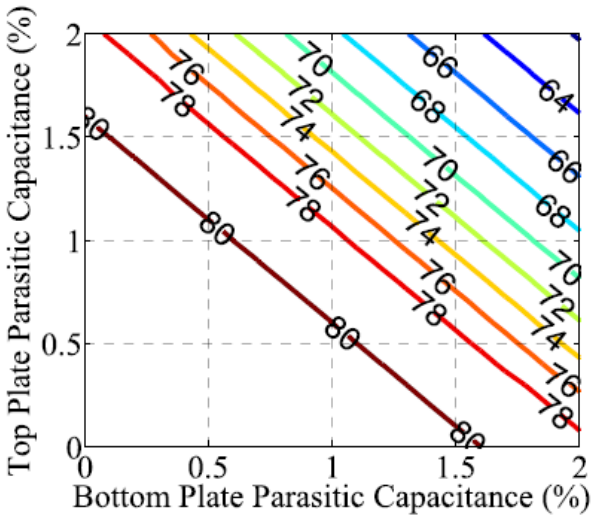


Figure 4.4: SNDR degradation of a 13-bit pipelined-SAR ADC with a 7-bit partial floating-based first-stage SAR ADC, owing to capacitor array's top and bottom parasitic capacitance.

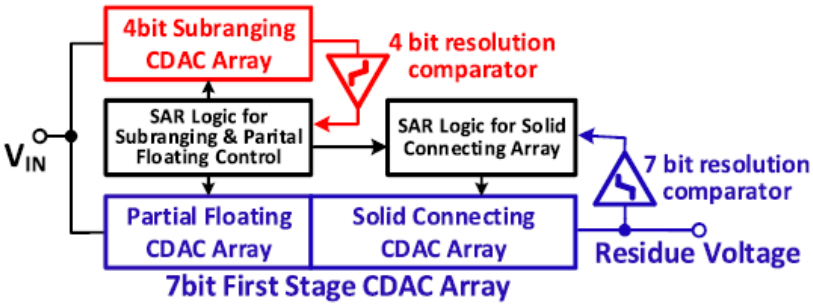
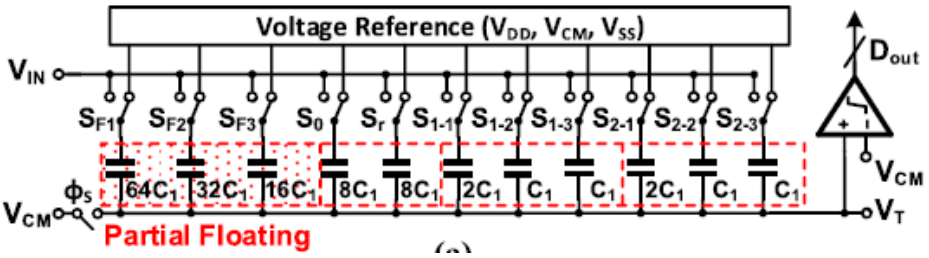


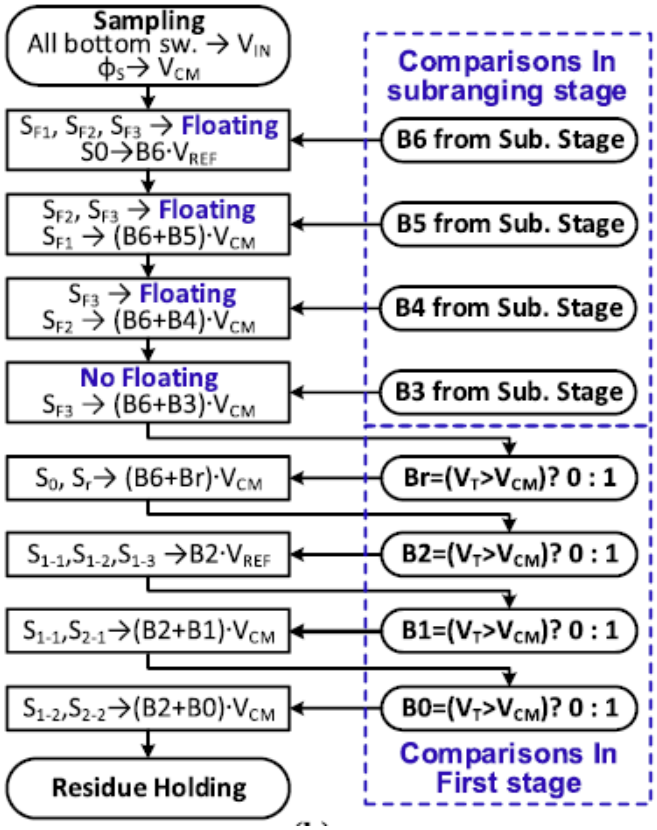
Figure 4.5: SAR-assisted subranging floating operation in the 7-bit first-stage SAR ADC.

4.4.3 SAR-assisted subranging floating capacitor switching technique

From the energy saving approaches in Section 4.4.1, more switching energy can be saved when more capacitors are used by the partial floating technique. However, this results in more decision errors because more non-binary scaled voltage steps appear. In Fig. 4.5, in order to skip the decision errors from the floating capacitors, a 4-bit subranging CDAC, which samples the input signal simultaneously with the first-stage CDAC, is employed to resolve the first four bits. With the help of these 4 bits, the first-stage CDAC array resolves the remaining 4 bits (one redundancy bit is included) and generates residue voltage to be transferred to a residue amplifier. Fig. 4.6(a)



(a)



(b)

Figure 4.6: (a) Capacitor array of the first-stage 7-bit SAR ADC with SAR-assisted subranging floating technique. (b) Its switching algorithm. (Actual implementation is fully differential.)

shows the capacitor array details of the first-stage 7-bit SAR ADC with the subranging floating technique. The first three largest capacitors ($64C_1$, $32C_1$, $16C_1$) use the partial floating technique to save switching energy and reduce INL error. Fig. 4.6(a) shows the switching algorithm of the first-stage CDAC. After sampling, the first three capacitors are made floating, and are set by the data stream from the subranging stage one by one. After all the capacitors are solidly connected,

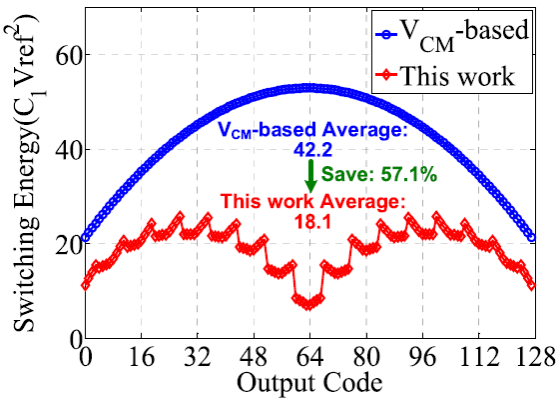


Figure 4.7: Seven-bit first-stage switching energy comparison versus output code.

the comparator in the first stage reaches the redundancy bit to set $8C_1$. Then, $4C_1$ is split into $2C_1$, C_1 and C_1 like a split capacitor array in [83] to further improve CDAC linearity. Splitting capacitors like this enables to employ the same control logic structure that the partial floating and redundancy capacitors employ.

Fig. 4.7 shows theoretical 7-bit CDAC switching energy of the SAR-assisted subranging floating capacitor switching. This switching energy includes energy consumption of both the first-stage CDAC and the subranging CDAC with a same unit capacitance. As compared with the VCM-based switching, the subranging floating technique consumes 57.1% less switching energy on average. Since the three largest capacitors are partially floating in the subranging floating technique, smaller INL error can be achieved when VCM is used as the reconstruction reference voltage. Fig. 4.8 shows behavioral 5000 Monte Carlo RMS INL simulation results under the assumption of 0.3% one sigma unit capacitor mismatch in the subranging and the first-stage CDAC. The simulation shows that the maximum RMS INL of the subranging floating technique is 41% lower than that of the VCM-based switching technique. In Fig. 4.9, 5000 Monte Carlo simulations in MATLAB show ENOB improvement as a result of the subranging floating technique. Here, the other blocks are assumed to be ideal. The horizontal axis denotes a standard deviation of the unit capacitor percent mismatch in the subranging stage and the first stage. For a 1% mismatch, the subranging floating capacitor switching technique improves the mean value of ENOB by 0.8 bit in comparison

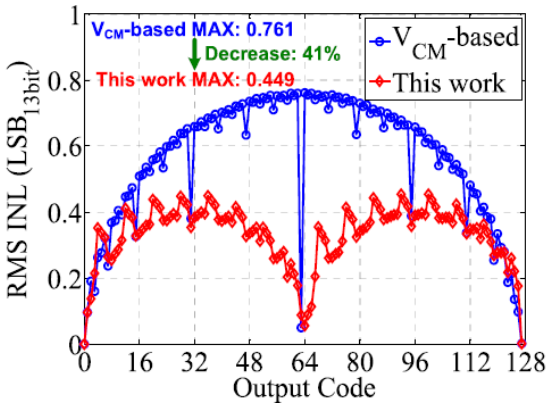


Figure 4.8: Seven-bit first-stage linearity comparison due to CDAC mismatch.

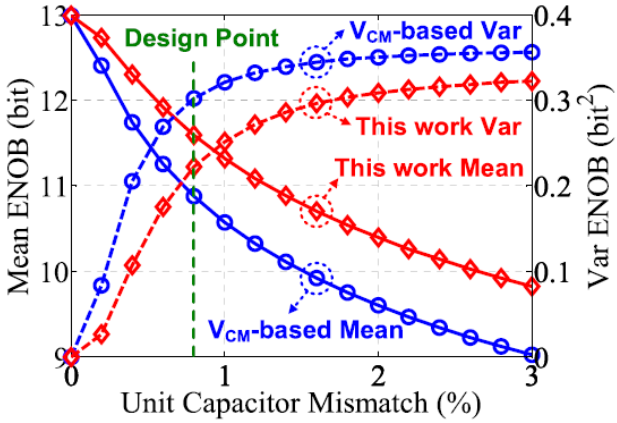


Figure 4.9: ENOB improvement by SAR-assisted subranging floating capacitor switching technique.

with the V_{CM}-based switching scheme.

4.5 Temperature-Insensitive Time-Based Residue Amplifier

4.5.1 Review of Conventional Inter-Stage Residue Amplifiers

In a pipelined-SAR ADC with an M-bit first-stage, the inter-stage residue amplifier needs a gain of 2^{M-1} to finish the residual amplification while there is no extra input swing attenuation in the second-stage SAR ADC [67]. An OTA-based feedback amplifier [67–69] achieves an accurate inter-stage gain through the ratio of capacitance. However, it is not friendly to technology scaling due to low intrinsic gain. Moreover, with certain settling time, a smaller feedback factor β ($\approx 2^{1-M}$)

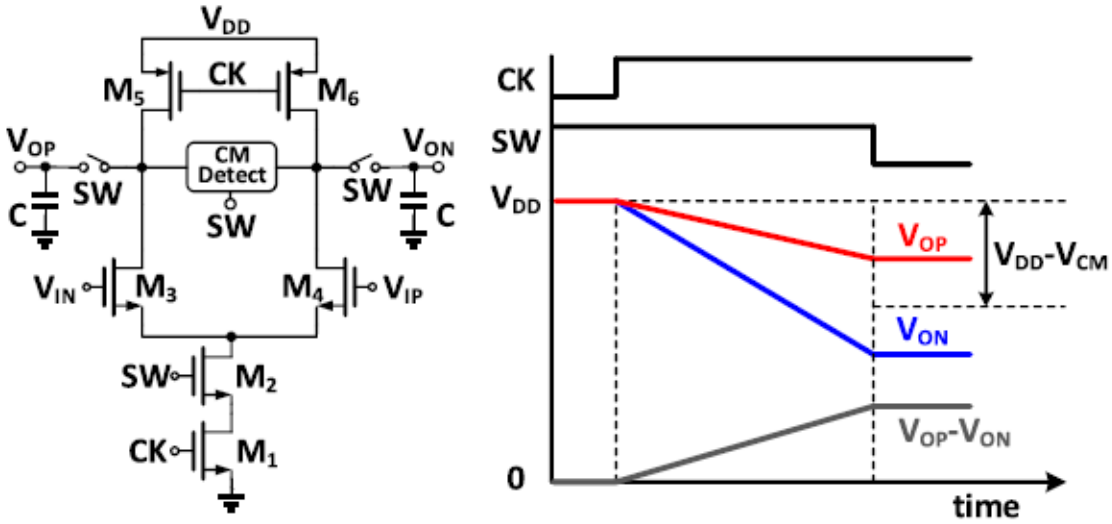


Figure 4.10: Circuit diagram and timing diagram of a conventional dynamic amplifier.

for a higher inter-stage gain requires the OTA to have larger transconductance for the same settling error, which translates to increase in static power consumption [67]. On the other hand, an inter-stage gain less than 2^{M-1} increases the total sampling capacitance of the second-stage SAR ADC due to the extra capacitors for the input swing attenuation, and in turn increases the load capacitance of the OTA [69].

A dynamic amplifier is attractive to a pipelined-SAR ADC because of its zero static power and noise filtering features [73–77]. Fig. 4.10 shows the circuit and timing diagram of a single-stage dynamic amplifier [76]. The voltage amplification is done by the clock-controlled charging and discharging operations to the load capacitors. The dynamic amplifier exhibits a transfer function of an integrator, and provides the best separation of a sampled-data input signal and thermal noise [73]. The gain of the single-stage dynamic amplifier is given by [76]

$$\text{Gain}_{\text{Dynamic Amplifier}} = \frac{g_{\text{m}}}{I_{\text{d}}} \cdot (V_{\text{DD}} - V_{\text{CM}}) \tag{4.3}$$

where g_m/I_d is the ratio of the transconductance and drain current of the input transistors (M_3 and M_4). From (4.3), the dynamic amplifier faces two critical challenges when it is used as a residue

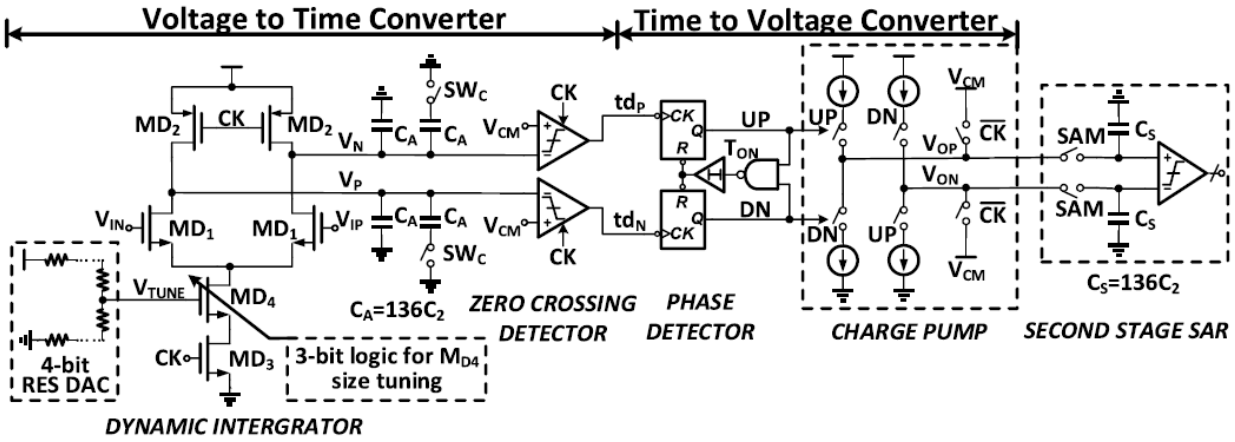


Figure 4.11: Temperature-insensitive time-based residue amplifier.

amplifier: One is that its gain is sensitive to PVT variations, and another is that the gain is limited to a small value inherently due to the limitations of supply voltage and g_m/I_d. A temperature-insensitive time-based residue amplifier is introduced in the following to solve the above challenges, while maintaining the merits of the conventional dynamic amplifier.

4.5.2 Operating principle of the time-based residue amplifier

The presented residue amplifier finishes its residue transfer through time-domain information as shown in Fig. 4.11. The residue voltage stored in the first-stage SAR ADC is converted to time difference by a VTC which consists of a dynamic integrator for noise filtering [73] and a zero crossing detector (ZCD) for time delay generation. The time difference is converted to the output voltage of the residue amplifier by a TVC which consists of a PD and a charge pump [79]. The ZCD in Fig. 4.11 contains a dynamic pre-amplifier and a dynamic inverter for power efficient full dynamic operation. The load capacitors of the dynamic amplifier use capacitor arrays which have the same capacitance and structure as those of the sampling capacitor arrays in the second-stage SAR ADC to eliminate the inter-stage gain's dependence on the capacitance (C_A and C_S). The 4-bit resistor DAC for V_{TUNE}, the 3-bit logic for MD_4 transistor size tuning, and the SW_C switches at the output of the dynamic integrator are used for initial settings for different power supply modes and process corner correction. Fig. 4.12 shows the timing diagram of the time-based residue amplifier.

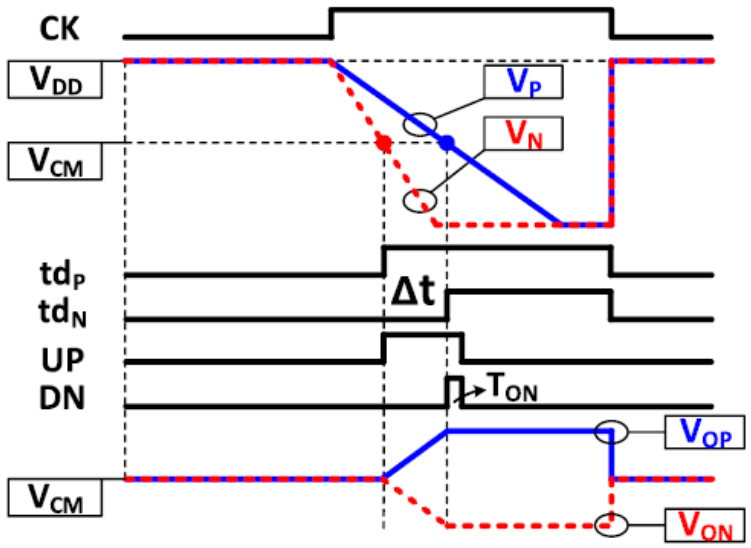


Figure 4.12: Timing diagram of the time-based residue amplifier.

When CK is low, the output node voltage (V_{N} and V_{P}) of the dynamic integrator is reset to V_{DD} and the output node voltage (V_{ON} and V_{OP}) of the charge pump is reset to common mode voltage V_{CM}. At the rising edge of CK, V_{N} and V_{P} start to be discharged at different rates based on the input residue voltage and the output of the ZCD ($\mathrm{td_P}$ and $\mathrm{td_N}$), which becomes high after V_{N} and V_{P} cross V_{CM}, respectively. Control signals of the charge pump (UP and DN) are generated by the PD, and T_{ON} is used for dead zone elimination. According to UP and DN signals, the charge pump injects current into the CDAC in the second-stage SAR ADC, and it develops the output voltage of the residue amplifier. The residue amplification is done through the above discharging and charging operation, which is reminiscent of a dual-slope ADC [84]. The ZCD's offset voltage and the input transistor's (MD1) offset voltage in Fig. 4.11 can be translated to the equivalent input offset voltage of the residue amplifier. If the total input offset voltage of the residue amplifier is less than the inter-stage redundancy voltage range (8.82 mV), the performance of the ADC is not affected. The offset voltage of the ZCD in this work is attenuated by the dynamic integrator gain, whereas that of the ZCD in a ZCD-based ADC [85] is not. The effect of signal-dependent delay of the ZCD is also minimized because of a similar discharging slope across the small input range of

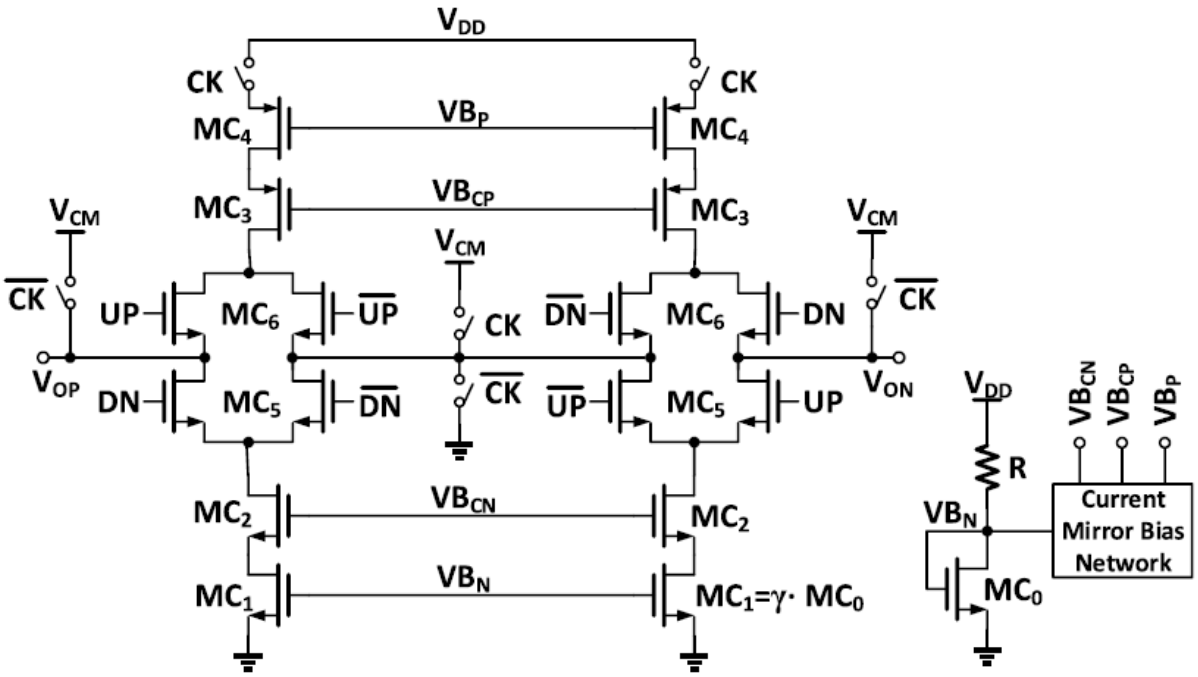


Figure 4.13: Schematic of the charge pump in the residue amplifier.

the dynamic integrator in Fig. 4.11.

Fig. 4.13 shows the schematic of the charge pump in the residue amplifier [79]. Replica branches (UP and DN switches) are used for current stabilization when both UP and DN are low. A mismatch between PMOS and NMOS current will cause the output common mode voltage of the charge pump to change. However, this is not critical because the V_{CM}-based switching is adopted in the second-stage SAR ADC. Furthermore, the mismatch between UP current sources (two transistors of MC4 in Fig. 4.13) brings different voltage gains when the input voltage polarity of the residue amplifier is different. According to our simulations, the ENOB of the ADC is higher than 11.5 bit with a mismatch of 30% between the UP current sources, which is easy to satisfy.

The gain of the time-based residue amplifier is determined by the gain of VTC and TVC, which are controlled by V_{TUNE} in Fig. 4.11 and the resistor R in Fig. 4.13, respectively. The gain of the

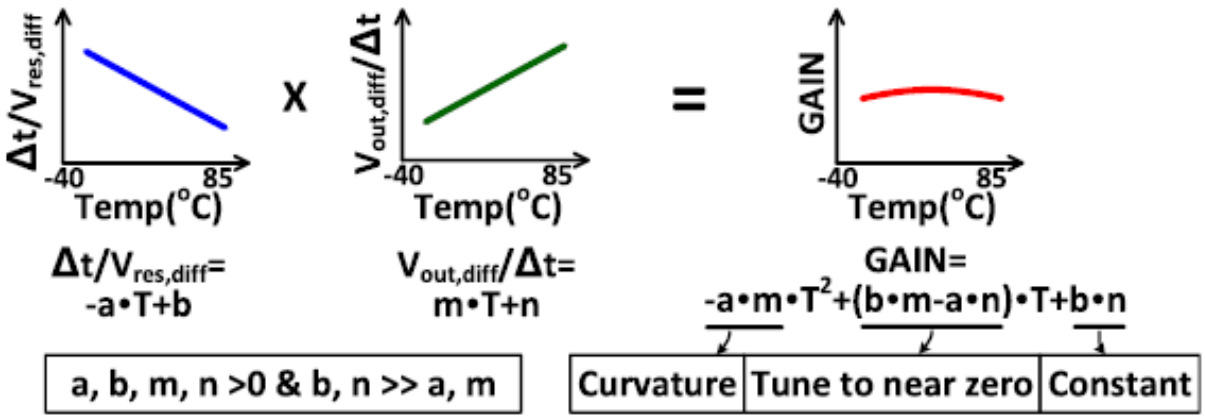


Figure 4.14: Temperature compensation concept.

time-based residue amplifier is given by

$$\text{Gain}_{\text{Time-based amp}} = 2 \cdot I_{\text{CP}} \cdot \frac{g_{\text{m, MD1}}}{{I_{\text{d, MD1}}}^2} \cdot (V_{\text{DD}} - V_{\text{CM}}) \tag{4.4}$$

where $g_{\text{m, MD1}}$ and I_{MD1} are the transconductance and drain current of MD1 in Fig. 4.11, respectively, I_{CP} is the drain current of MC1 in Fig. 4.13. Compared with (4.3) and (4.4), the time-based residue amplifier is easy to achieve 32× gain. Furthermore, the total transfer time of the time-based residue amplifier has a relation with the sampling capacitance C_S in the second stage. Hence, the time-based residue amplifier is technology scaling-friendly in terms of speed because the metal-oxide-metal (MOM) capacitor C_S is also technology scaling-friendly.

4.5.3 Temperature compensation in the time-based residue amplifier

The temperature compensation is done by a VTC with a negative temperature coefficient (TC) and a TVC with a positive TC. For simplicity, we model the negative TC and positive TC with a linear equation in Fig. 4.14. The detailed derivation procedure of the TC of the VTC and TVC is given in the Appendix B.1. Through equations (B.1), (B.5), (B.6) and (B.8) in the Appendix B.1, all the coefficients in Fig. 4.14 can be obtained. From (B.5), the negative TC of VTC increases as V_{TUNE} increases (because $V_{\text{OV, MD1}}$ increases) in Fig. 4.11. From (B.8), the positive TC of TVC

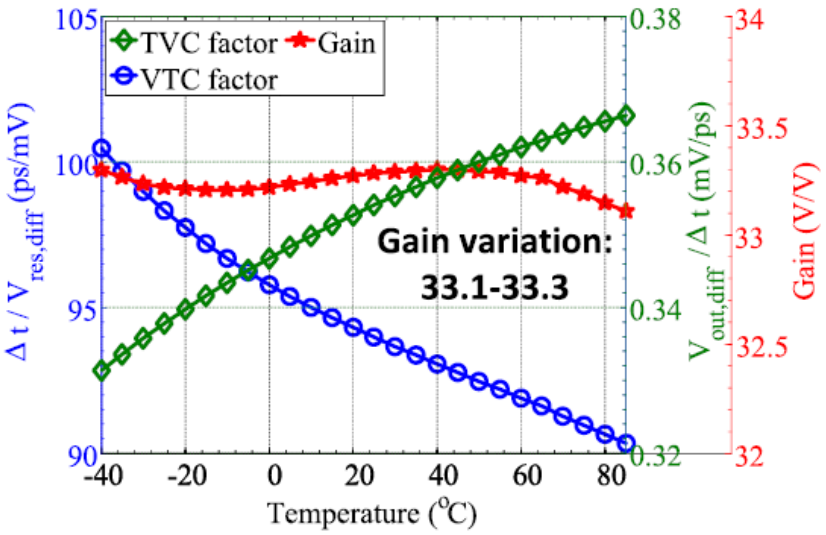


Figure 4.15: Simulation result of the temperature compensation process.

decreases as R increases in Fig. 4.13. Therefore, the temperature compensation can be done by tuning V_{TUNE} in Fig. 4.11 and R in Fig. 4.13. Fig. 4.15 shows the simulation results of the conversion factors of the VTC and the TVC at a 1.2 V power supply and the TT corner. When the temperature varies from -40 °C to 85 °C, the gain of the residue amplifier changes only 0.6% from 33.1× to 33.3× (bigger than 32× to compensate the top plate parasitic capacitance in the first-stage CDAC). From equations (B.9) and (B.10) in the Appendix B.1, the time-based residue amplifier can also tolerate some degree of supply voltage variation in the same principle shown in Fig. 4.14 through a negative voltage coefficient (VC) in (B.9) and a positive VC in (B.10). Fig. 4.16 shows the simulation result of the residue amplifier gain versus power supply voltage variation (1.2 V is nominal supply voltage) at the TT corner. With ±10% power supply voltage variation, gain of the residue amplifier changes 4.2% from 31.9× to 33.3×.

The equations (B.5), (B.8), (B.9), and (B.10) in the Appendix B.1 show that TC and VC of the VTC have the same trends as those of the TVC, respectively. Moreover, they are governed by the same design variables, and can be tuned by V_{TUNE} and R. The design point of the residue amplifier in this work is determined mainly by temperature compensation, while power supply sensitivity is reasonably minimized. Table 4.1 summarizes the simulation results of the gain variations of the

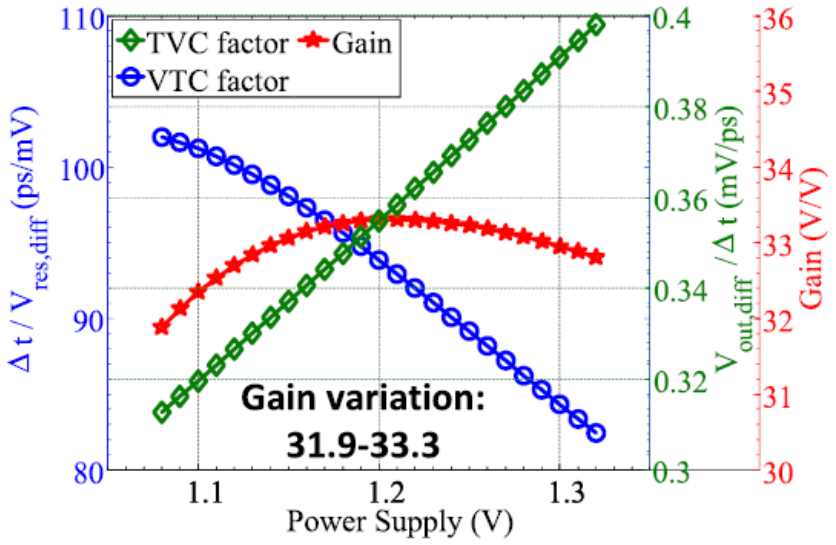


Figure 4.16: Simulation result of the residue amplifier gain versus power supply voltage variation.

Table 4.1: Residue Amplifier Gain Variations With PVT Variations (-40°C to 85°C)

Corners	SS	SF	TT	FS	FF
1.32 V Supply	31.7-32.9	31.7-33.0	32.0-33.1	32.5-33.6	32.5-33.5
1.20 V Supply	33.1-33.3	33.1-33.3	33.1-33.3	33.1-33.3	33.1-33.3
1.08 V Supply	32.1-32.7	32.2-32.7	31.7-31.9	31.5-31.7	31.5-31.7

residue amplifier at different process corners and different power supplies when the temperature varies from -40 °C to 85 °C. Different trimming block settings are used for different process corners to cover the process variations

4.5.4 Noise and linearity of the time-based residue amplifier

According to the analysis in the Appendix B.2, the input-referred noise of the presented time-based residue amplifier in Fig. 4.11 is given by

$$\overline{v_{i,noise}^2} = \frac{4kT\gamma}{C_{\mathrm{A}}} \cdot \frac{I_{\mathrm{MD1}}}{g_{\mathrm{m,MD1}}(V_{\mathrm{DD}} - V_{\mathrm{CM}})}. \tag{4.5}$$

Table 4.2: Noise Breakdown of the Pipelined-SAR ADC

Total Noise [V^2]	Quantization Noise [V^2]	Sampling Noise [V^2]	Residue Amp. Noise [V^2]	2nd Comparator Noise [V^2]
1.11e-8	6.35e-9	2.60e-9	2.03e-9	0.12e-9

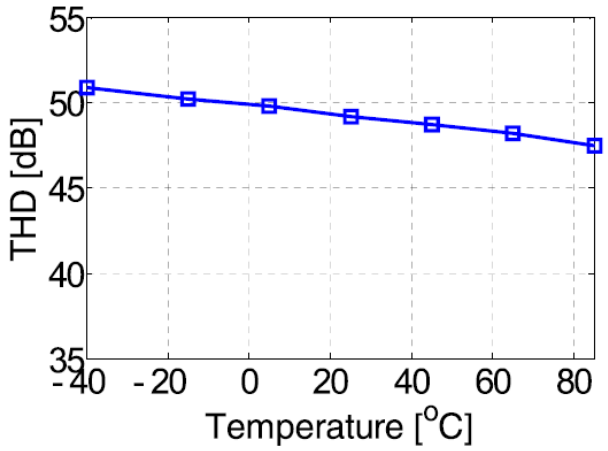
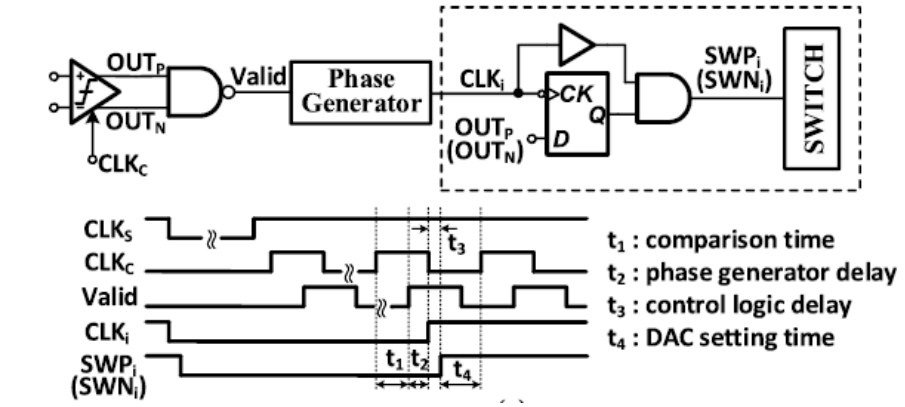


Figure 4.17: Simulated THD of the residue amplifier versus temperature.

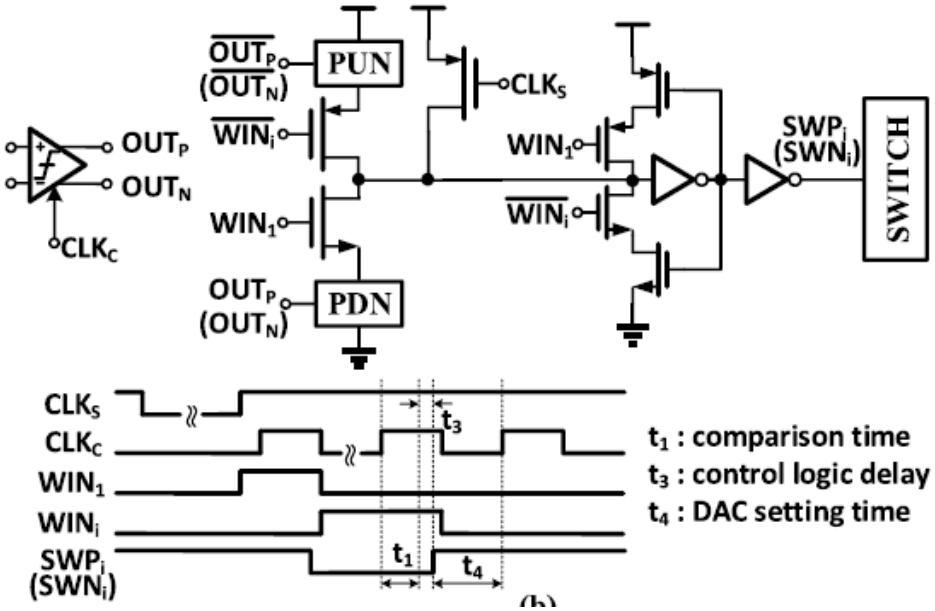
The noise in (4.5) is same with the noise of a conventional dynamic amplifier [73], so the presented time-based residue amplifier is also a low-noise solution due to the noise filtering feature. Table 4.2 shows the simulated noise breakdown of the pipeline-SAR ADC. Our time-based residue amplifier occupies only 18% of the total noise power of the ADC. Fig. 4.17 shows the simulated THD of the residue amplifier versus temperature under 1.2 V power supply and TT corner. The input signal of the residue amplifier is an 11 MHz stair-case sinusoidal signal with a voltage swing of 17.65 $mV_{pp,diff}$ (maximum residue voltage swing) and it is generated by an ideal DAC clocked at 50 MHz. From Fig. 4.17, the linearity of the time-based residue amplifier is sufficient to resolve the 7 bits in the second stage.

4.6 Pre-window Asynchronous Control Logic

In high resolution SAR ADC design, a large CDAC for a strict matching requirement makes a DAC settling time longer. Moreover, the comparison results always suffer further delays in order to set the control logic for a CDAC as shown in Fig. 4.18(a) [86]. Therefore, a DAC settling time



(a)



(b)

Figure 4.18: (a) Conventional SAR logic. (b) Subranging stage's pre-window SAR logic.

requirement is getting harder to achieve in high-speed high-resolution SAR ADC design. Fig. 4.18 shows the comparison between conventional SAR logic [86] and the presented pre-window-based SAR logic. Fig. 4.18(b) shows an example of the pre-window technique used in the subranging stage. In a similar way, it can apply to the first stage and the second stage as well. In the pre-window-based SAR logic, a window (WIN_i) is enabled for the comparator output before it is clocked. With assistance from WIN_i, comparison results are used by the corresponding switched control blocks without extra delay. In Fig. 4.18 the pre-window-based SAR logic saves the delay

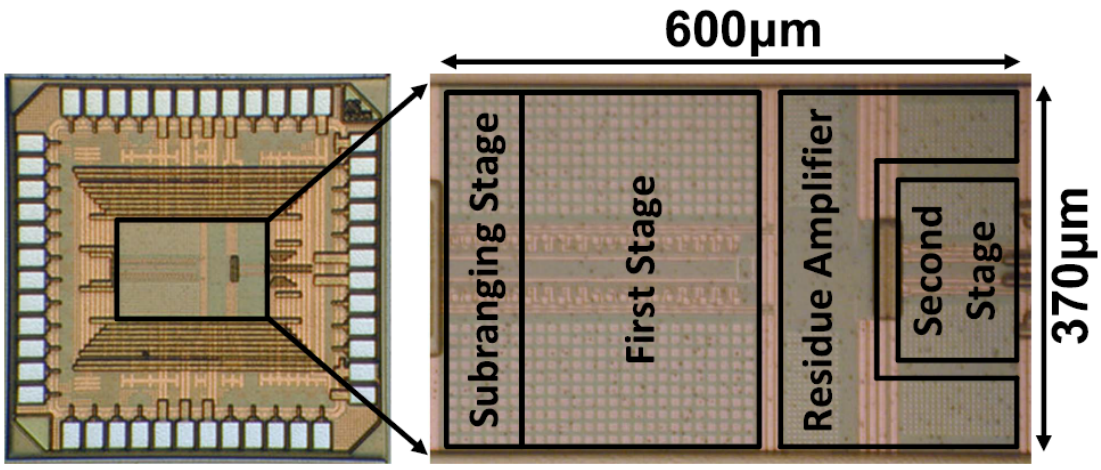


Figure 4.19: Die microphotograph of pipelined-SAR ADC.

time of the phase generator t_2, which is usually considerable in high resolution SAR ADC because the delay cells are always inserted into the asynchronous loop in order to relax the CDAC set up time. The pre-window signal, WIN_i is generated through a TSPC DFF-based shift register chain.

4.7 Measurement Results

The prototype pipelined-SAR ADC was fabricated in an 1P8M 130 nm CMOS process. A die photo is shown in Fig. 19. The active area of the ADC is 0.22 mm^2, and most of the active area is occupied by the CDAC in both the first stage and second stage. The unit capacitance of the first-stage SAR ADC is 22 fF. Moreover, both the CDAC of the second-stage SAR ADC and the load capacitor of the dynamic integrator in the residue amplifier use the same unit capacitance, 1.8 fF. All of the unit capacitor is a custom-designed encapsulated MOM capacitor [86]. The designed pipelined-SAR ADC has three operation modes supporting different power supply voltages (1.2 V, 1.0 V and 0.8 V) with different maximum conversion speeds (50 MS/s, 30 MS/s and 10 MS/s, respectively). As there is no integrated reference buffer on chip, V_{DD} and GND are used as the high reference and low reference voltage, respectively to simplify the measurement. Large on-chip bypass capacitors are used to stabilize the reference voltages. Foreground calibration is used for the temperature compensation configuration of the open-loop residue amplifier at in different operation modes with a DC input signal of V_{CM}. The calibration flow is as follows: First, configuring the

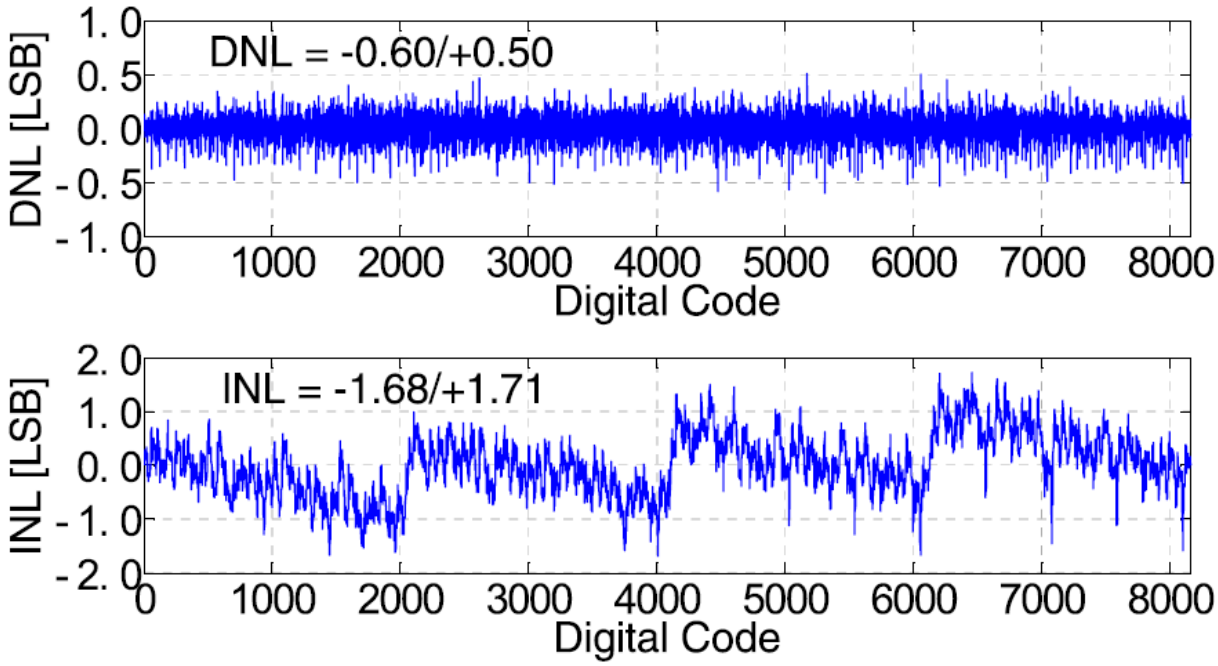


Figure 4.20: Measured DNL and INL errors.

residue amplifier in Fig. 11 with the default settings which are from simulations; then changing the current of the charge pump by changing adjusting the resistor R in Fig. 13 to make the output code of the ADC 4096 (mid-scale code of a 13-bit ADC) under 25 oC. Second, putting the measured ADC under -40 °C and 85 °C, and capturing its output code simultaneously; if the output code is within a range of [4094 to 4098], the calibration is done; if not, changing V_{TUNE} in Fig. 4.11 and R in Fig. 4.13 according to the temperature compensation analysis in Section 4.5.3 to make the output code of the ADC in the range of [4094 to 4098] under -40 °C and 85 °C.

Fig. 4.20 shows the measured DNL and INL errors under 50 MS/s conversion rate. The DNL is within -0.60/ +0.50 LSB and the INL is within -1.68/ +1.71 LSB with assistance from the highly linear SAR-assisted subranging floating capacitor switching scheme and a large CDAC array used in the first-stage SAR ADC. Fig. 4.21 shows the measured FFT spectrums at different modes with Nyquist frequency input signals. The ADC achieves 69.1 dB SNDR and 80.7 dB SFDR at 50 MS/s under 1.2 V power supply, 71.0 dB SNDR and 80.0 dB SFDR at 30 MS/s under 1.0 V power supply, and 71.2 dB SNDR and 81.5 dB SFDR at 10 MS/s under 0.8 V power supply.

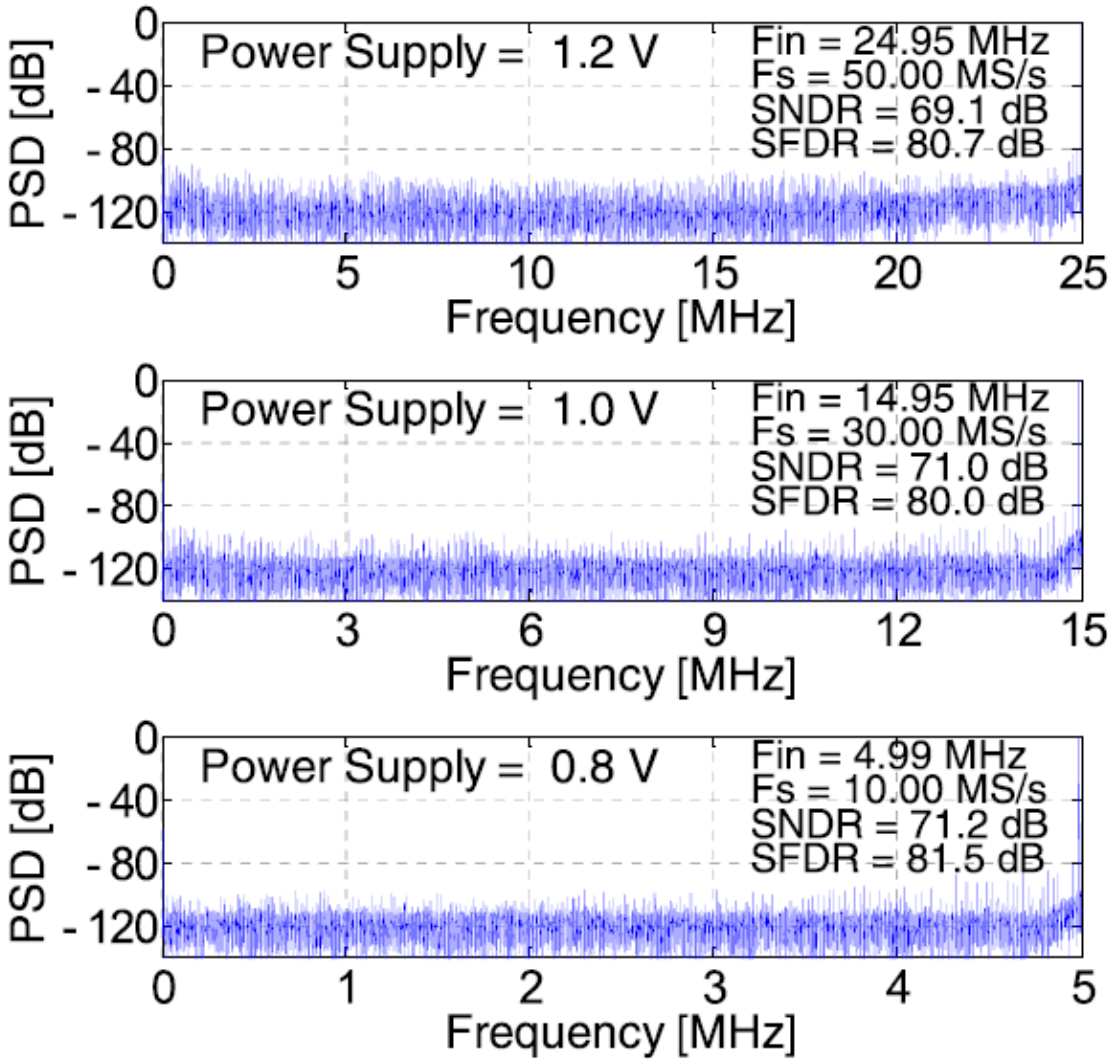


Figure 4.21: Measured FFT from 66536 data output with Nyquist input signals at 1.2-, 1-, and 0.8-V power supplies.

The designed pipelined-SAR ADC has a very low noise floor thanks to the noise filtering benefit from the residue amplifier. Fig. 4.22 summarizes the measured SNDR and SFDR versus input frequencies at different operation modes. The performance drops in the high input frequencies due to sampling bandwidth limitation by the resistance in ADC test input paths, including the sampling switches, the ESD protection resistors and the routing resistors.

The robustness of the presented pipelined-SAR ADC against temperature and power supply variation is also measured in Fig. 4.23 and Fig. 4.24. Since the sampling performance of ADC is

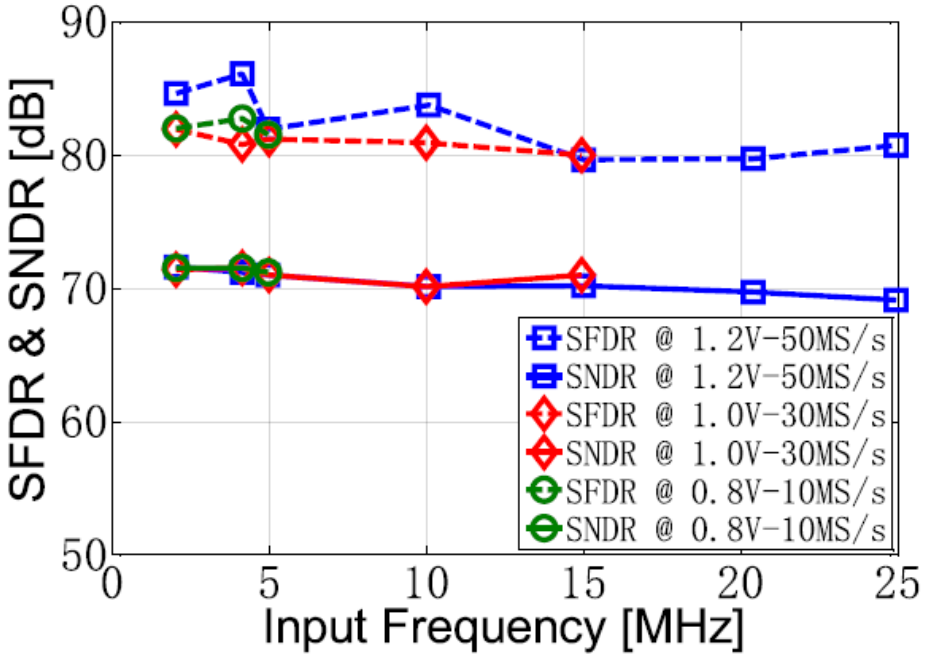


Figure 4.22: Measured SFDR and SNDR versus input frequency at different power supply voltages and sampling rates.

strongly related with its ambient temperature and power supply voltage, the measurements in Fig. 4.23 and Fig. 4.24 were performed at low conversion rates to evaluate the residue amplifier gain variation versus ambient temperature and power supply voltage by minimizing the performance deterioration from sampling. The ADC has a higher than 68.5 dB measured SNDR and a higher than 76.5 dB measured SFDR over a -40 °C to 85 °C temperature range at all operating modes in Fig. 23. If temperature ranges from -25 °C to 65 °C, SNDR is higher than 70.1 dB, and SFDR is higher than 78.2 dB at all operating modes. This verifies that the temperature compensation presented in Section 4.5 is valid. More than 66.0 dB measured SNDR and more than 80.9 dB measured SFDR can be obtained within $\pm 10\%$ power supply variation of the whole pipelined-SAR ADC at all operating modes in Fig. 4.24. If measured within $\pm 5\%$ power supply variation, SNDR is higher than 68.9 dB, and SFDR is higher than 81.4 dB at all operating modes. Fig. 4.25 shows the power consumption breakdown of the presented pipelined-SAR ADC at 1.2 V power supply and 50 MS/s conversion rate with a Nyquist frequency input. The total measured power

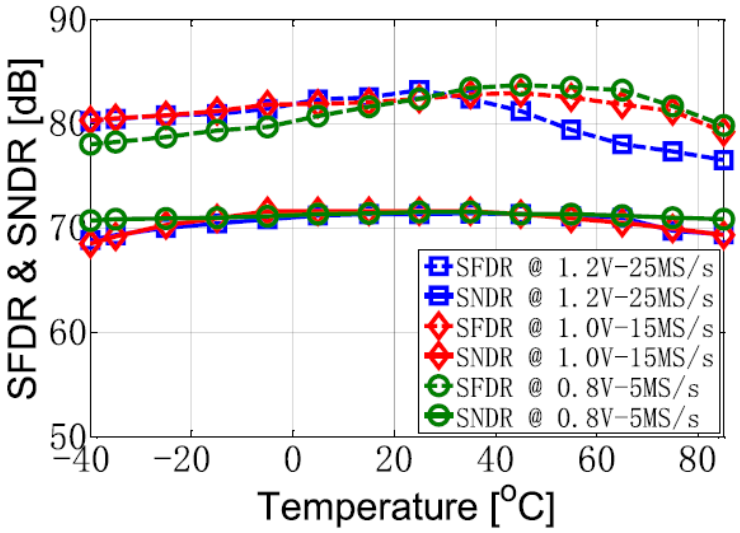


Figure 4.23: Measured SFDR and SNDR versus temperature of ADC with 2.05-MHz input signals.

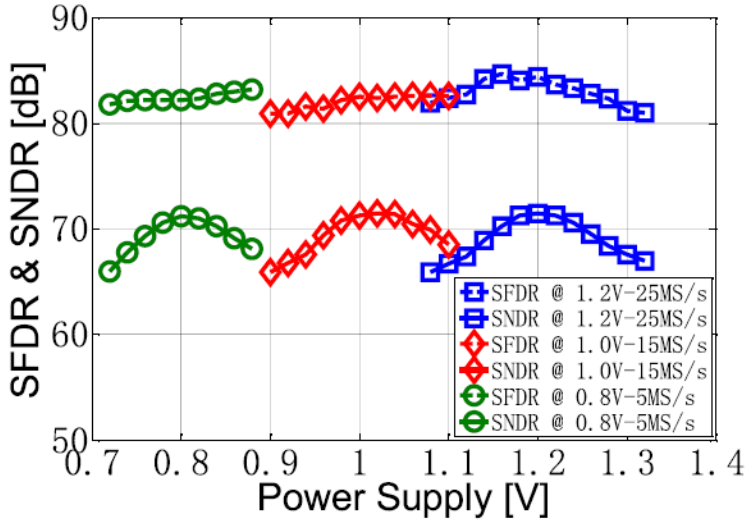


Figure 4.24: Measured SFDR and SNDR versus $\pm 10\%$ power supply variation of ADC with 2.05-MHz input signals.

is 1.32 mW. Only 26.1% of the total power is consumed by the time-based residue amplifier, and this is much smaller than that of a closed-loop residue amplifier design [67–69]. The other power consumption percentages include 46.1% for the subranging and first stage, 19.2% for the second stage, and 8.6% for the clock generator.

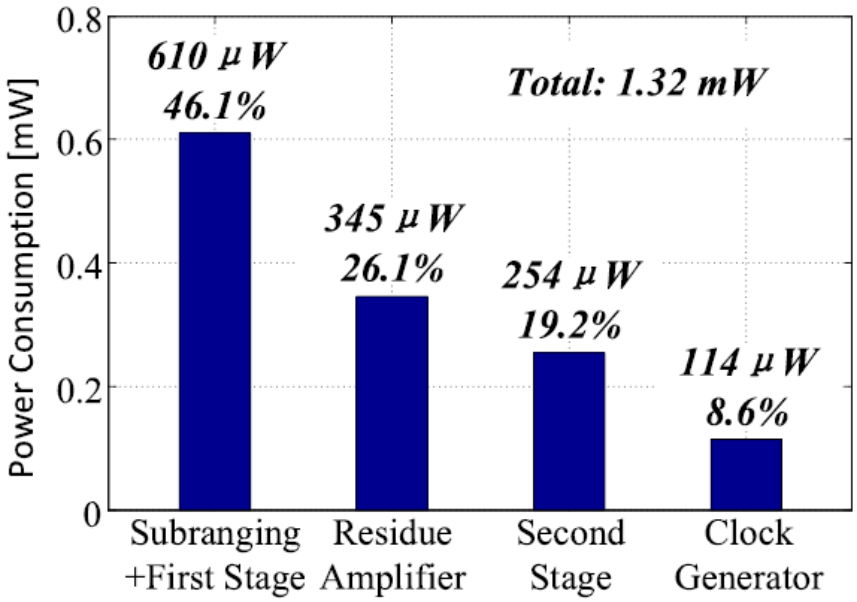


Figure 4.25: Pipelined-SAR ADC power consumption breakdown (1.2-V power supply and 50 MS/s).

Table 4.3 summarizes the performance of the pipelined-SAR ADC at different operating modes. The full-scale differential input signal range is 16/17 of $2\times V_{\mathrm{DD}}$ due to the redundancy capacitor in the first stage. The performance of the pipelined-SAR ADC keeps similar at down-scaled power supply voltages, even leading to better FoMs at 0.8 V and 1.0 V power supply. The Walden FoM with 2.05 MHz input signal is from 3.9 to 8.5 fJ/conversion-step, and 4.0 to 11.3 fJ/conversion-step with a Nyquist frequency input. Table 4.4 shows a comparison between the prototype ADC and other pipelined-SAR ADCs. To our best knowledge, among the pipelined-SAR ADC with an open-loop residue amplifier, this work is the only one that achieves high gain and background calibration-free operation simultaneously under ambient temperature and power supply variation. This work also shows an attractive power supply scaling feature with competitive energy efficiency, even though it is implemented in a relatively old technology. With a 0.8 V power supply and a 10 MS/s conversion rate, the 4.0 fJ/conversion-step is the best reported FoM to date for an ADC with more than 70 dB measured SNDR and more than 10 MS/s conversion rate.

Table 4.3: Pipelined-SAR ADC Performance Summary

Resolution	13 bits		
Technology	130 nm 1P8M CMOS		
Active Area	0.22 mm^2		
DNL	-0.60/+0.50 LSB		
INL	-1.68/+1.71 LSB		
Power Supply	1.2 V	1.0 V	0.8 V
Sampling Rate	50 MS/s	30 MS/s	10 MS/s
Input Range	2.26 $V_{p\text{-}p,diff}$	1.88 $V_{p\text{-}p,diff}$	1.51 $V_{p\text{-}p,diff}$
SNDR @ 2.05 MHz input	71.6 dB	71.4 dB	71.5 dB
SFDR @ 2.05 MHz input	84.6 dB	81.9 dB	82.0 dB
SNDR @ Nyquist input	69.1 dB	71.0 dB	71.2 dB
SFDR @ Nyquist input	80.7 dB	80.0 dB	81.5 dB
Total Power	1.32 mW	0.56 mW	0.12 mW
FoM @ 2.05 MHz input	8.5 fJ/conv. step	6.1 fJ/conv. step	3.9 fJ/conv. step
FoM @ Nyquist input	11.3 fJ/conv. step	6.4 fJ/conv. step	4.0 fJ/conv. step

4.8 Conclusion

This chapter introduces a subranging pipelined-SAR ADC employing a new CDAC switching algorithm and a new residue amplifier. The presented SAR-assisted subranging floating capacitor switching algorithm reduces the CDAC switching energy and improves its linearity by utilizing a subranging stage which also breaks the speed bottleneck in the first-stage SAR ADC. The presented temperature-insensitive time-based residue amplifier solves the PVT variation issue in the

Table 4.4: Comparison with State-of-art Pipelined-SAR ADC Designs

	This Work			[67] SOVC 2010	[68] ISSCC 2012	[73] ISSCC 2014	[75] SOVC 2014	[72] ISSCC 2015	[87] ISSCC 2017
Technology	130 nm			65 nm	130 nm	28 nm	28 nm	65 nm	65 nm
Resolution [bits]	13			12	14	14	14	13	12
Active Area [mm^2]	0.22			0.16	0.24	0.137	0.35	0.054	0.08
Interleaving	No			No	No	2X	2X	No	No
DNL [LSB]	0.60			0.75	0.89	-	-	0.58	0.67
INL [LSB]	1.71			1.50	3.52	-	-	0.96	0.8
Residue Amplifier Structure	Open-loop Time-based			Closed-loop Telescopic		Open-loop Dynamic		Closed-loop Ring	Open-loop Dynamic
Residue Amplifier PVT-Stabilized	Yes			Yes		Digital Calibration		Yes	Yes
Power Supply [V]	1.2	1.0	0.8	1.3	1.2	1.0	0.9	1.2	1.3
ADC FS [$V_{p\text{-}p,diff}$]	2.26	1.88	1.51	2.0	2.0	1.4	-	2.4	-
Sampling Rate [MS/s]	50	30	10	50	30	80	200	50	330
SNDR @ Nyq. [dB]	69.1	71.0	71.2	64.4	70.4	66.0	65.0	70.9	63.5
SFDR @ Nyq. [dB]	80.7	80.0	81.5	75.0	79.6	74.0	-	84.6	76.5
Total Power [mW]	1.32	0.56	0.12	3.5	2.54	1.5	2.3	1.0	6.23
FoM @ Nyq. [fJ/conv.step]	11.3	6.4	4.0	51.8	31.3	11.5	7.9	6.9	15.4

open-loop residue amplifier. This time-based residue amplifier also shows power supply voltage scalability. The pre-window asynchronous control logic is used to extend the settling time of the CDAC array. With the aforementioned three techniques, the prototype ADC achieves 69.1 dB SNDR and 80.7 dB SFDR for a Nyquist frequency input sampled at 50 MS/s and consumes 1.32 mW. With a power supply range of 0.8-to-1.2 V and 10-to-50 MS/s conversion rate, this ADC achieves Walden FoMs from 4.0 to 11.3 fJ/conversion-step.

5. A TEMPERATURE COMPENSATION TECHNIQUE FOR A DYNAMIC AMPLIFIER IN PIPELINED-SAR ADCS*

5.1 Dynamic Amplifiers

In electronic circuit design, the word "dynamic" implies storing charges in a capacitor. For example, a memory cell of a dynamic random access memory (DRAM) stores charges into the cell capacitor, thereby storing digital bit information, whereas a static random access memory (SRAM) stores digital information into a latch. Moreover, dynamic logic circuits utilize pre-charging or post-charging to capacitors to enhance speed and remove static power consumption [46]. In applications to analog circuits, a dynamic current mirror [88] is used to mirror the current without static bias current consumption. On the same line, a dynamic amplifier uses pre-charging to amplify the input signal without static bias current consumption.

A dynamic amplifier uses pre-charging to set the bias condition of the amplifier without static bias current consumption. Elimination of the static bias current makes a dynamic amplifier a good candidate for a low-power amplifier. Moreover, a dynamic amplifier is inherently fit into discrete time applications because dynamic circuit operation requires a pre-charging or post-charging phase. However, there are some caveats for dynamic amplifier design. First of all, designers should take care of capacitive coupling from other noisy signals because all the analog information of a dynamic amplifier is stored in capacitors. Moreover, gate leakage current of transistors in advanced CMOS technology can destroy the stored information, or requires to use large storage capacitors, which leads to low speed and increase in power and area.

Fig. 5.1 shows an example of a dynamic amplifier [89]. Operating points of the amplifier are set when ϕ is high, and the input signal is amplified when ϕ is low. Dynamic biasing makes the amplifier less sensitive to threshold and power supply variations.

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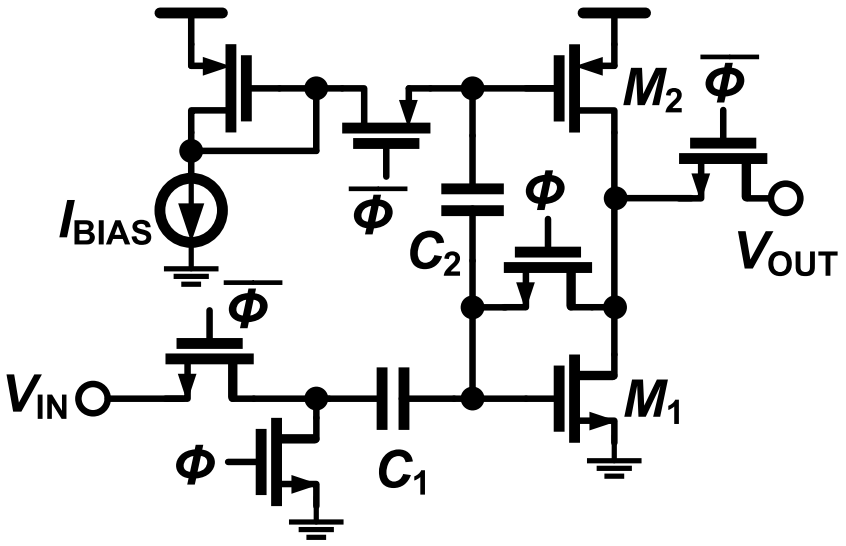


Figure 5.1: An example of a dynamic amplifier.

5.2 Dynamic Amplifiers in Pipelined-SAR ADCs

For high-speed and high-resolution applications, a pipelined-successive approximation register (SAR) analog-to-digital converter (ADC) [20, 67, 68, 72, 73, 75, 87] shows better energy efficiency than conventional pipeline and SAR ADCs [60, 64]. While the pipelined-SAR ADC can have a high first-stage resolution to enhance linearity, design of a precise high-gain residue amplifier is still challenging. A conventional operational transconductance amplifier-based closed-loop residue amplifier [67, 68] is not only power-hungry due to stringent requirements of settling speed and accuracy, but also adverse to technology scaling due to low intrinsic transistor gain in nanometer CMOS. A ring amplifier-based residue amplifier [72] benefits from slew-based charging and near rail-to-rail output swing. However, its ring operation brings an inherent stability issue, and the multi-stage structure limits its maximum conversion speed.

Recently, a dynamic amplifiers [73,75,76,87,90] has become an attractive approach to energy-efficient residue amplification in the pipelined-SAR ADC because it benefits from noise filtering and dynamic power features [73]. However, gain of the dynamic amplifier is sensitive to process, supply voltage, and temperature (PVT) variations due to its open-loop operation. One way

to compensate for the PVT-sensitive gain is digital background calibration [73, 75] which usually suffers from long convergence time and design complexity. The other is an analog compensation approach utilizing PVT- dependent integration time for the dynamic amplifier [87]. However, it needs a static power-consuming amplifier, and the inherent mismatch between the dynamic amplifier and the static amplifier limits its compensation effect.

Usually, the process variation can be corrected through foreground calibration, and the supply voltage variation is reasonably minimized by a supply voltage regulator in the pipelined-SAR ADC. In this work, we explore a temperature-compensated dynamic amplifier. While a time-based residue amplifier in [20] achieves temperature-insensitive high gain ($32\times$), it requires a higher design complexity than a conventional dynamic amplifier due to time-domain conversion. Here, we propose a temperature-insensitive dynamic amplifier with moderate gain ($12\times$) but lower design complexity. The proposed dynamic amplifier employs a temperature-dependent common-mode (CM) detector, which has a fully dynamic operation and simple configuration. The prototype single-stage dynamic amplifier achieves 2.1% gain variation across -20 °C to 85 °C with the proposed technique.

This chapter is organized as follows. Section 5.3 shows how the gain variation of the residue amplifier affects the performance of the pipelined-SAR ADC. Section 5.4 illustrates the principle and implementation of the temperature-compensated dynamic amplifier. Section 5.5 reports the measurement results, and Section 5.6 concludes this work.

5.3 Residue Gain Variation in Pipelined-SAR ADCs

Fig. 5.2 shows a 12-bit pipelined-SAR ADC. A 6-bit first-stage SAR ADC and a 7-bit second-stage SAR ADC are connected by a dynamic amplifier with a gain of 12. An attenuation capacitor C_a in the second-stage SAR ADC is used to relax the gain of the dynamic amplifier from 32 to 12. Both the first stage and the second stage adopt bottom-plate input sampling to enhance the sampling accuracy. A V_{CM}-based switching technique [82] is adopted in both stages to maintain the constant CM voltage of the capacitive DAC. The pipeline timing diagram in Fig. 5.2(b) is similar to [73] and [20].

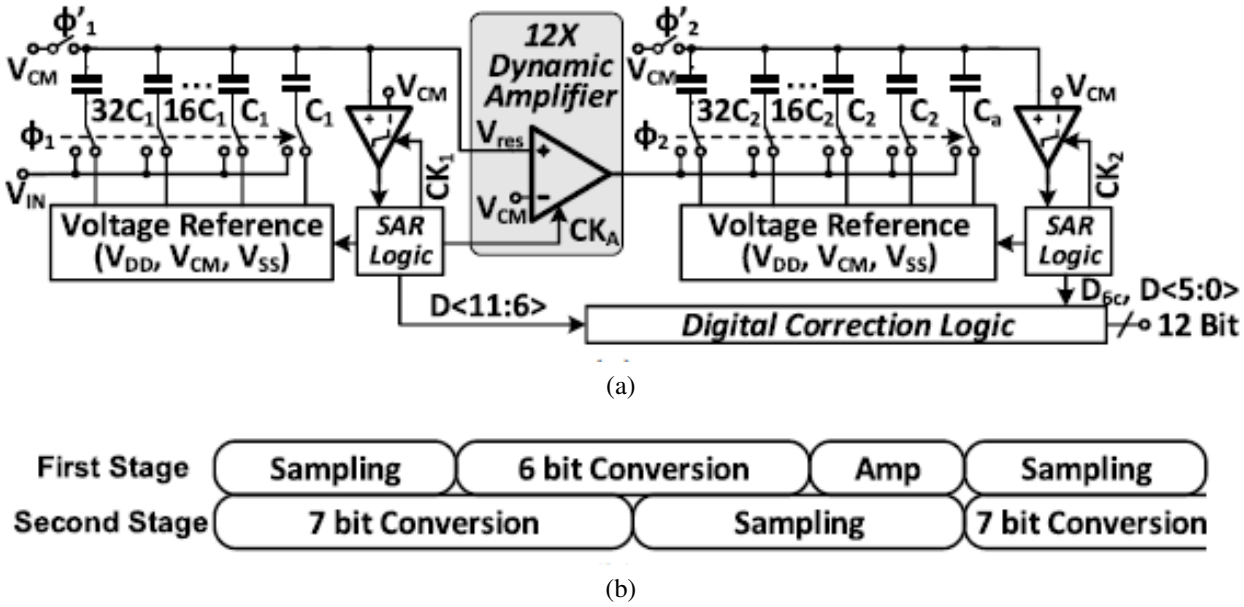


Figure 5.2: (a) Block and (b) timing diagram of a 12-bit pipelined-SAR ADC with a dynamic residue amplifier(single-ended version shown here).

To investigate how the gain of the dynamic amplifier affects the performance of the 12-bit pipelined-SAR ADC, we modeled the whole ADC of Fig. 5.2 in MATLAB with ideal first-stage and second-stage SAR ADCs. Fig. 5.3 shows the simulated SNDR versus the residue gain in the pipelined-SAR ADC. The residue gain should be within a range of 11.6 to 12.4 to achieve an SNDR greater than 66.5 dB.

5.4 Temperature-Compensated Dynamic Amplifier

5.4.1 Review of Conventional Dynamic Amplifier

A dynamic amplifier assists a pipelined-SAR ADC to realize fully dynamic operation, which is attractive to frequency-scalable applications. Fig. 5.4 shows the circuit and timing diagram of a conventional single-stage dynamic amplifier [76]. When CLK is low, the output node voltages (V_{ON} and V_{OP}) of the dynamic amplifier are reset to V_{DD}. At the rising edge of CLK, V_{ON} and V_{OP} start to be discharged at different rates based on the input differential voltages. When the CM voltage of V_{ON} and V_{OP} crosses V_{DET} (threshold voltage of the CM detector), the CM detector is triggered, and SW becomes low to cut off the capacitors CL from the discharging branches. Sub-

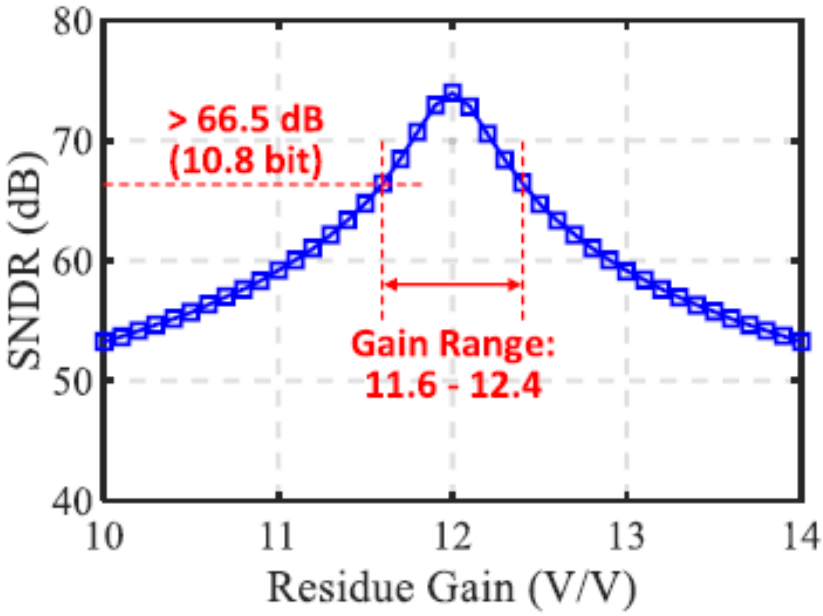


Figure 5.3: SNDR versus residue gain of the 12-bit pipelined-SAR ADC.

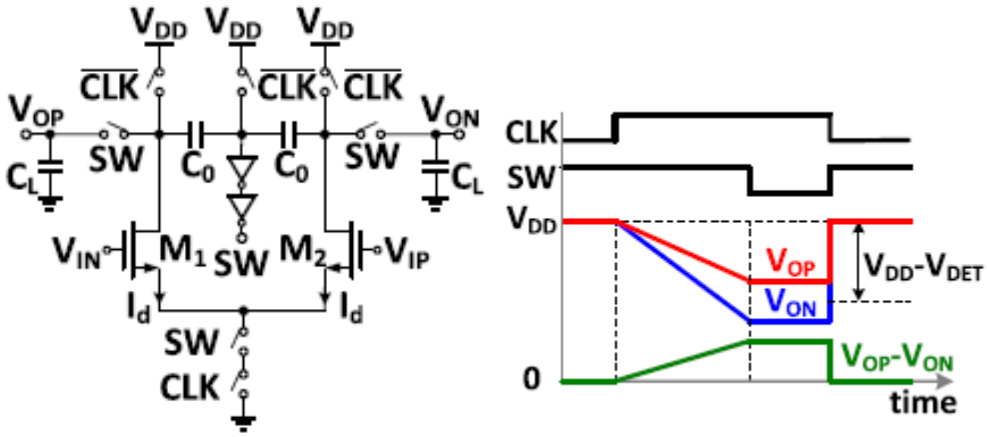
sequently, the output voltage V_{ON} and V_{OP} are maintained. The gain of the single-stage dynamic amplifier is given by [76]

$$\text{Gain} = \frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} \cdot (V_{\mathrm{DD}} - V_{\mathrm{DET}}) \tag{5.1}$$

where $g_{\mathrm{m}}/I_{\mathrm{d}}$ is the transconductance efficiency of the input transistors (M_1 and M_2). From (5.1), the gain of the dynamic amplifier relates to a temperature-sensitive term $g_{\mathrm{m}}/I_{\mathrm{d}}$. To achieve a temperature-insensitive gain, a temperature-dependent CM detector is presented in this work to make the $V_{\mathrm{DD}}V_{\mathrm{DET}}$ term in (5.1) offset the temperature variation of the $g_{\mathrm{m}}/I_{\mathrm{d}}$ term.

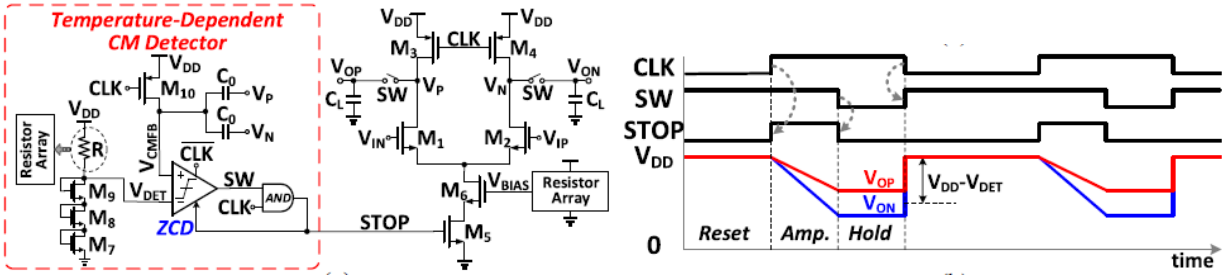
5.4.2 Temperature-Compensated Dynamic Amplifier

Fig. 5.5 shows the circuit and timing diagram of the temperature-compensated dynamic amplifier with a zero-crossing detector (ZCD)-based CM detector. Unlike a conventional inverter-based CM detector [76], the ZCD-based CM detector has a temperature-dependent threshold voltage, V_{DET}. To achieve a temperature- insensitive gain, the principle of multiplication-based temperature compensation [20] is adopted herein. Temperature dependence of $g_{\mathrm{m}}/I_{\mathrm{d}}$ and $V_{\mathrm{DD}} - V_{\mathrm{DET}}$ can



(a) (b)

Figure 5.4: (a) Circuit and (b) timing diagram of a conventional dynamic amplifier.



(a) (b)

Figure 5.5: (a) Circuit and (b) timing diagram of the temperature-compensated dynamic amplifier.

be modeled as $TC_{g_m/I_d} \times (T - T_0) + (g_m/I_d)T_0$ and $TC_{V_{DD}-V_{DET}} \times (T - T_0) + (V_{DD} - V_{DET})T_0$, respectively. Here, TC_X is the temperature coefficient (TC) of X, and T_0 is 25 °C. The linear temperature dependence of the dynamic amplifier gain can be removed, if the TCs of the g_m/I_d and the $V_{DD} - V_{DET}$ have different polarities, and their ratio has a certain value.

M_1 and M_6 in Fig. 5.5 are in the saturation region and linear region, respectively. Assuming square law devices for analyses, the TC of g_m/I_d is given by

$$TC_{g_m/I_d} = \frac{\partial (g_m/I_d)_{M1}}{\partial T} \approx \frac{\alpha}{2} \cdot \frac{V_{OV,M6}}{V_{OV,M1}^3} \cdot \frac{\partial V_{TH,M1}}{\partial T} < 0. \tag{5.2}$$

where $\alpha = 2 \times (W/L)_{\mathrm{M6}}/(W/L)_{\mathrm{M1}}$ in Fig. 5.5. $V_{\mathrm{OV,\,M1}}$ and $V_{\mathrm{TH,\,M1}}$ are the overdrive voltage and the threshold voltage of M_1, respectively. $V_{\mathrm{OV,\,M6}}$ is the overdrive voltage of M_6. According to (5.2), $g_{\mathrm{m}}/I_{\mathrm{d}}$ has a negative TC because of a negative TC of $V_{\mathrm{TH,\,M1}}$ [20], and its value varies with V_{BIAS} in Fig. 5.5. In order to compensate for the negative TC of (5.2), a temperature-dependent voltage V_{DET} is introduced in Fig. 5.5. The TC of $V_{\mathrm{DD}} - V_{\mathrm{DET}}$ is given by

$$\mathrm{TC}_{\mathrm{V_{DD}\text{-}V_{DET}}} = \frac{\partial(V_{\mathrm{DD}} - V_{\mathrm{DET}})}{\partial T} \approx 3 \times (\frac{V_{\mathrm{OV,M7}}}{2K_{\mathrm{M7}}} \cdot \frac{\partial K_{\mathrm{M7}}}{\partial T} - \frac{\partial V_{\mathrm{TH,M7}}}{\partial T}) > 0. \tag{5.3}$$

where $K_{\mathrm{M7}} = \frac{1}{2} \times \mu_{\mathrm{n}} C_{\mathrm{ox}} (W/L)_{\mathrm{M7}}$. $V_{\mathrm{OV,\,M7}}$ and $V_{\mathrm{TH,M7}}$ are the over-drive voltage and threshold voltage of M_7, respectively. Stacking of M_7, M_8, and M_9 reduces $V_{\mathrm{OV,\,M7}}$, making the TC of $V_{\mathrm{DD}} - V_{\mathrm{DET}}$ positive [20]. The TC of $V_{\mathrm{DD}} - V_{\mathrm{DET}}$ can be changed by the resistor R in Fig. 5.5 (by changing $V_{\mathrm{OV,\,M7}}$). The detailed derivations of (5.2) and (5.3) can refer to [20]. By multiplying the $g_{\mathrm{m}}/I_{\mathrm{d}}$ and the $V_{\mathrm{DD}} - V_{\mathrm{DET}}$, a condition to remove linear temperature dependence of the dynamic amplifier gain is given by

$$\frac{\mathrm{TC}_{\mathrm{g_m/I_d}}}{\mathrm{TC}_{\mathrm{V_{DD}\text{-}V_{DET}}}} \approx -\frac{(g_{\mathrm{m}}/I_{\mathrm{d}})_{\mathrm{M1,T_0}}}{(V_{\mathrm{DD}} - V_{\mathrm{DET}})_{\mathrm{T_0}}}. \tag{5.4}$$

Equation (5.4) can be satisfied by tuning both resistor arrays in Fig. 5.5. Fig. 5.6 shows the simulation results of the temperature compensation effect at a 1.2-V power supply and the TT corner. The TC of $g_{\mathrm{m}}/I_{\mathrm{d}}$ is negative, and the TC of $V_{\mathrm{DD}}V_{\mathrm{DET}}$ is positive as shown in Fig. 5.6. When temperature varies from -20 °C to 85 °C, the gain of the dynamic amplifier changes from 11.78 to 12.25 with the proposed temperature compensation technique. The bias voltage V_{BIAS} and resistor R in Fig. 5.5 are programmable to cover supply voltage variations and different process corners. In Fig. 5.7, the gain of the dynamic amplifier is within a range of 11.70 to 12.32 with different process corners (TT, FF, SS, FS, and SF), and supply voltages (1.15 V, 1.2 V, and 1.25 V) across a temperature range of -20 °C to 85 °C.

With a noise filtering feature [73], the simulated input-referred noise of the dynamic amplifier is 1.5 nV^2 with a load capacitor $\mathrm{C_L}$ of 250 fF in Fig. 5.5. Fig. 5.8 shows the simulated total

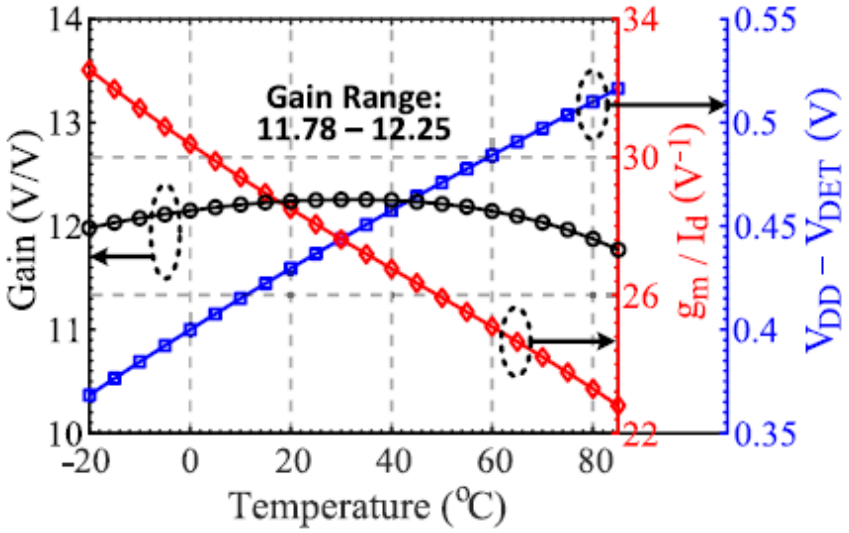


Figure 5.6: Simulation results of the temperature compensation.

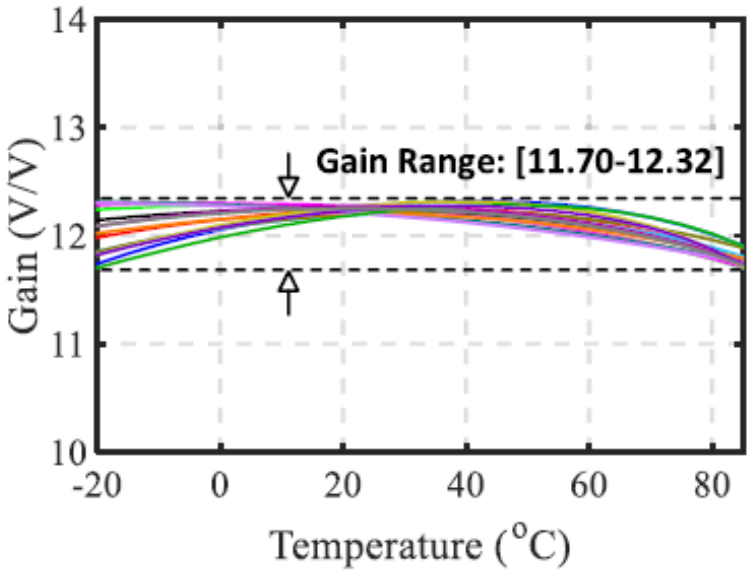


Figure 5.7: Simulation results of the dynamic amplifier gain versus temperature with different supply voltages (1.2 V $\pm$ 0.05 V) and process corners (TT, FF, SS, FS, and SF).

harmonic distortion (THD), amplification time, and the output CM voltage of the dynamic amplifier under 1.2-V power supply, TT corner, and an 11-MHz stair-case sinusoidal input signal with a voltage swing of 37.5 $mV_{pp,\,diff}$ (maximum residue voltage of the first-stage SAR ADC in Fig. 5.2).

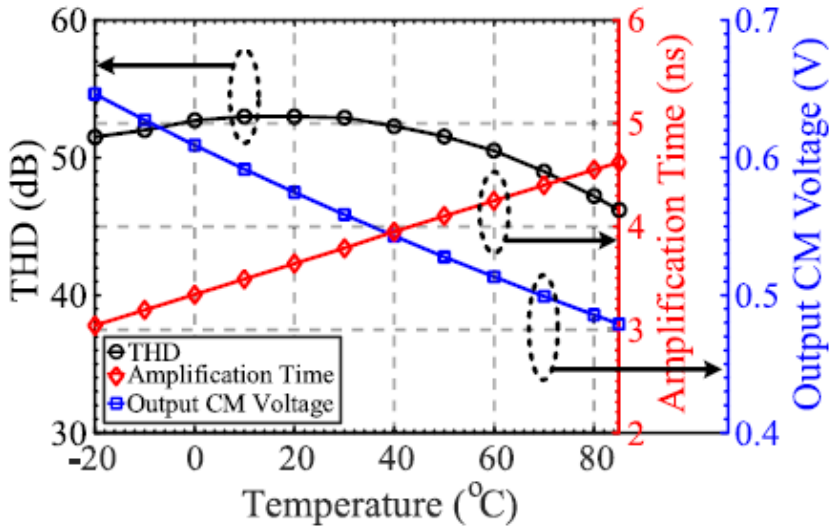


Figure 5.8: Simulated THD, amplification time, and output CM voltage of the dynamic amplifier versus temperature.

The linearity of the temperature-compensated dynamic amplifier is sufficient for the 7-bit second-stage SAR ADC. The gain of the dynamic amplifier is within the range of 11.6 to 12.4 across -20 °C to 85 °C with an input CM voltage range of 300 mV to 700 mV. The output CM voltage of the dynamic amplifier varies with temperature as shown in Fig. 5.8 because of the temperature-dependent CM detector. However, the output CM voltage variation has no significant effect on the ADC performance because the second-stage SAR ADC adopts the fully differential V_{CM}-based switching scheme, which is insensitive to the input CM voltage [82], and the temperature variation is a slow process. The output CM voltage in Fig. 5.8 is less than the V_{DET} in Fig. 5.6 because of the time delay of the ZCD.

5.4.3 Zero-Crossing Detector

The ZCD [91] in the temperature-dependent CM detector consists of a single-stage pre-amplifier, a dynamic inverter, and a normal inverter as shown in Fig. 5.9. The pre-amplifier is cut off after the amplification process of the dynamic amplifier for energy efficiency, and its timing information is shown in Fig. 5.5(b). The temperature- dependent offset of the ZCD is much less than $V_{\mathrm{DD}} - V_{\mathrm{DET}}$, so it does not affect the temperature compensation process significantly.

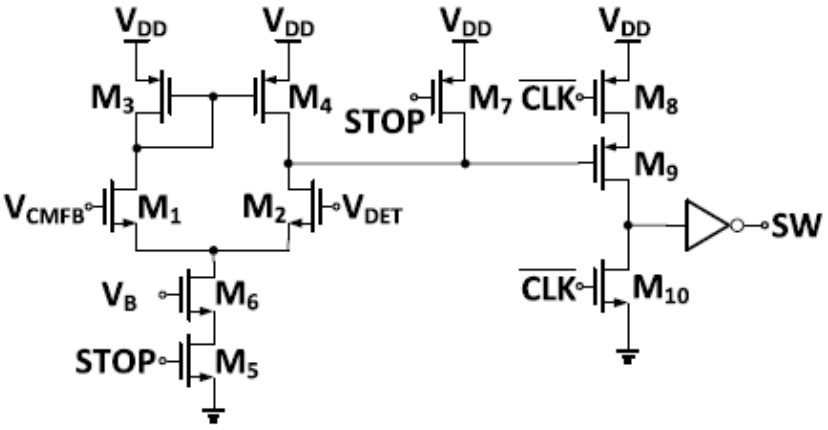


Figure 5.9: Schematic of the ZCD.

5.5 Measurement Results

The prototype temperature-compensated dynamic amplifier was fabricated in a 1P8M 130 nm CMOS process. Fig. 5.10 shows a die photograph and its corresponding layout. The active area of the dynamic amplifier with output buffers is 0.0135 mm^2. Fig. 5.11 shows the measurement setup including on-chip output buffers and off-chip transformers. The direct path is measured to eliminate the effect of the output buffers on the gain of the dynamic amplifier. The output buffer is comprised of a pseudo-differential PMOS source follower pair that is terminated with the off-chip transformer to mitigate the effects of pads and bonding wires. The center taps of the output transformers are supplied with 2.5 V for high linearity by increasing the source-to-gate voltage of the PMOS source followers.

Gain of the proposed dynamic amplifier was measured with the 500 kHz 50 $mV_{pp,\,diff}$ sinusoidal input and 1.2-V power supply voltage at the conversion rate of 50 MS/s. The transformer bandwidth should be much higher than the conversion rate to avoid high frequency attenuation because the output voltage waveform of the dynamic amplifier is a pulse-amplitude modulation signal. For accurate gain measurements, we measured input attenuation by the transformer T_1 with the connecting cable and output attenuation by the output buffer and the following transformer with the connecting cable. Measured input and output attenuation are 2.5 dB and 9.9 dB at 500 kHz,

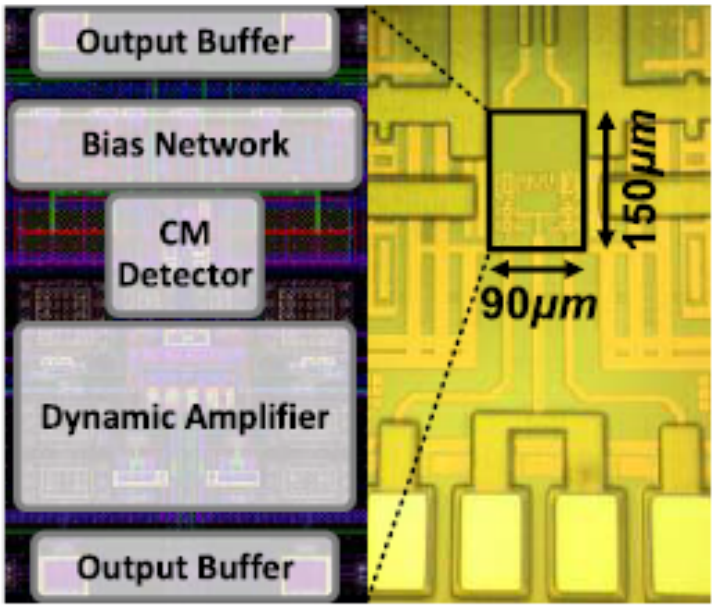


Figure 5.10: Die microphotograph and its corresponding layout.

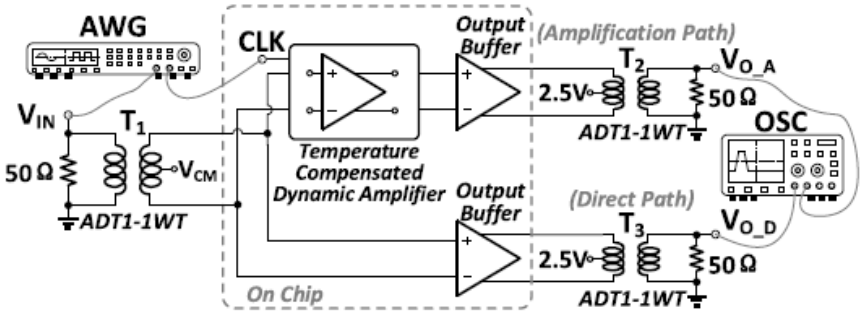


Figure 5.11: Measurement setup.

respectively. The peak output and input voltages are used to evaluate the gain of the dynamic amplifier. Fig. 11 shows the measured output transient waveforms of the dynamic amplifier at CLK and V_{O_A}. Measured gain and amplification time of the dynamic amplifier are 12.2 and 3.7 ns, respectively as shown in Fig. 5.12.

To evaluate the linearity of the dynamic amplifier, the gain versus input swing (after T_1) is measured in Fig. 5.13. The gain of the dynamic amplifier is larger than 11.6 when the input swing (after T_1) is less than 80 $mV_{pp,diff}$. The simulated SNDR of the pipelined-SAR ADC in Fig. 5.2

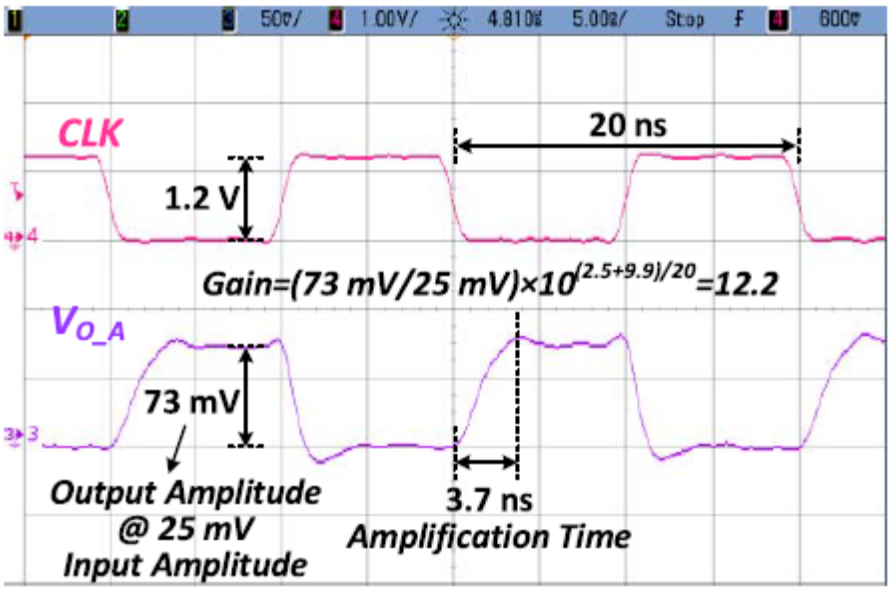


Figure 5.12: Measured output transient waveforms of the dynamic amplifier after the transformer T_2 at 50 MS/s.

with the ideal SAR ADCs and the measured gain profile in Fig. 5.13 is 73.5 dB. Fig. 5.14 shows the measured temperature compensation effect of the dynamic amplifier with three chips. The presented temperature compensation technique reduces the gain range from [10.85 to 13.50] to [11.75 to 12.21], resulting in reduced maximum gain variation from 12.5% to 2.1% across -20 °C to 85 °C.

The total power of the dynamic amplifier is 0.11 mW except the output buffers at 1.2-V power supply and 50-MHz clock. The temperature-dependent CM detector consumes 31.8% of the total power, which is dynamic power and scalable with the needed conversion speed. Table 5.1 shows a comparison among [20, 87], and the prototype dynamic amplifier. Compared with our former temperature- insensitive time-based amplifier [20], the prototype dynamic amplifier eliminates the complicated time-domain operation and is more suitable for the energy-efficient applications. The prototype dynamic amplifier achieves a higher gain than [87] with a similar gain variation over a wider temperature range. Fully dynamic operation makes this work superior to [87] in terms of a power-to-conversion-speed ratio and power overhead of the compensation circuit.

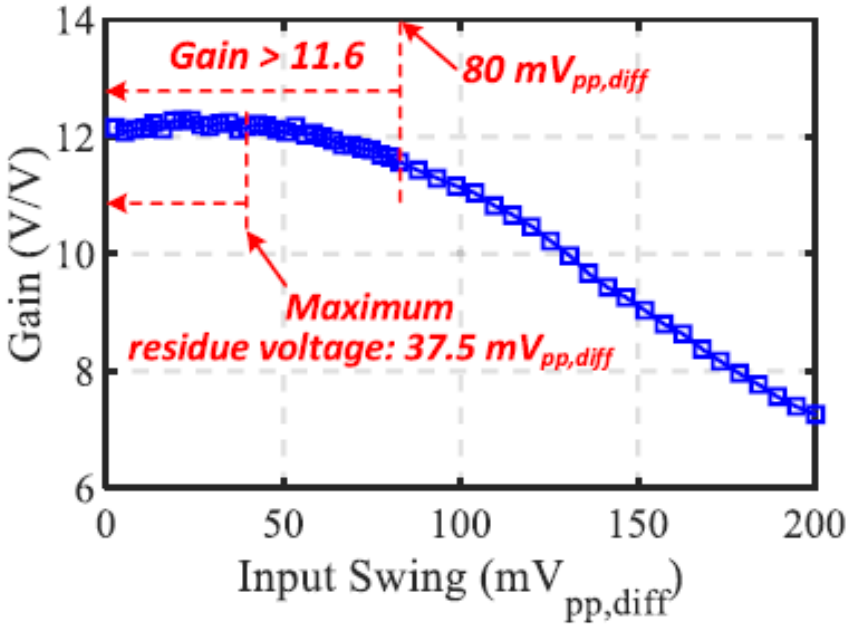


Figure 5.13: Measured dynamic amplifier gain versus input swing.

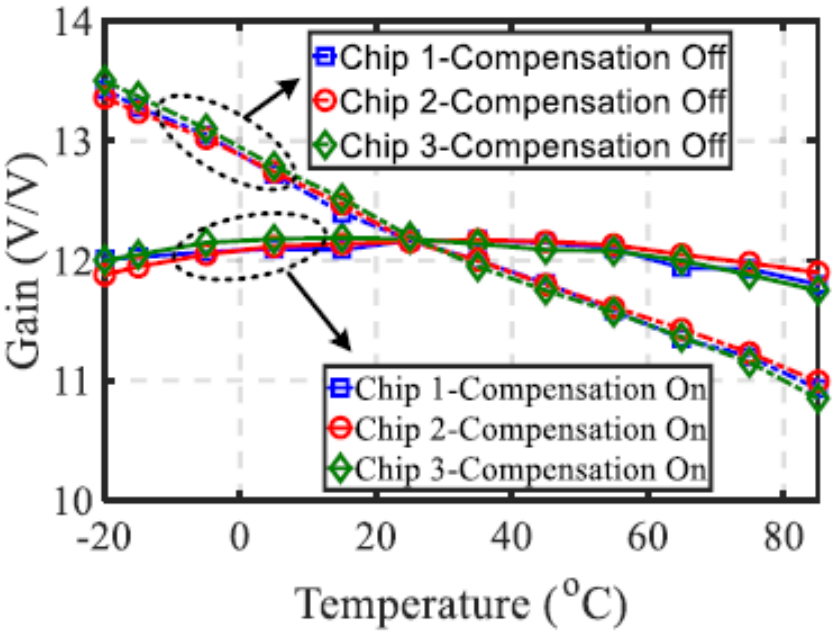


Figure 5.14: Measured dynamic amplifier gain versus temperature.

Table 5.1: Performance Comparison

	[87]	[20]	This work
Technology (nm)	65	130	130
Supply Voltage (V)	1.3	1.2	1.2
Gain (V/V)	5	32	12
Temperature Range (°C)	[-5 to 85]	[-40 to 85]	[-20 to 85]
$\frac{\lvert\Delta\text{Gain}\rvert/\text{Gain}}{\text{Temperature Range}}$ (%/°C)	0.017	0.0025*	0.020
Power/Speed (W/Hz)	3.33×10^{-12}	6.90×10^{-12}	2.20×10^{-12}
Power Percent of Compensation Circuits (%)	49.1	-**	31.8

*Simulation result without process and supply voltage variatons.
** [20] is not a dynamic amplifier. There is no separate compensation circuit.

5.6 Conclusion

This chapter presents a temperature compensation technique for a dynamic amplifier. The proposed temperature-dependent ZCD-based CM detector reduced the gain variation of the dynamic amplifier from 12.5% to 2.1% across the temperature range of -20 °C to 85 °C.

6. CONCLUSIONS

6.1 Summary

Since portable or implantable devices operate in the energy-constrained environment, their low-power operations in combination with efficiently sourcing energy to them are key problems to extend device life. This research discusses two essential functions of a PRU in the energy-constrained environment, which are power management and signal processing.

From a power management perspective, the most critical two circuit blocks are a front-end rectifier and a battery charger. The front-end CMOS active rectifier converts transmitted AC power into DC power. High PCE is required to reduce power loss during the power transfer, and high VCR is required for the rectifier to enable low-voltage operations. The proposed rectifier in Chapter 2 adopts novel low-power comparators for active diodes and dynamic logic-based feedback controllers to further reduce power consumption from active diodes and control logic circuits. Consequently, high PCE and VCR are maintained, while robust operations to PVT variations are achieved.

The linear battery charger stores the converted DC power into a battery. Since even small power saving can be enough to run the low-power PRU, a battery charger with low I_{Q} is desirable. Chapter 3 introduces a unified amplifier-based linear battery charger and analyzes stability of the proposed charger. In contrast to conventional chargers, the proposed charger adopts a single amplifier that utilizes current-steering for the CC-CV transition, which results in low I_{Q}.

From a signal processing perspective, an ADC is one of the most important circuit blocks in the PRU. It can be used to sense environmental changes such as temperature change and humidity change, while it can be used for wireless communication among other near PRUs as well. Hence, an energy-efficient ADC is essential in the energy-constrained environment. Recently a hybrid architecture, a pipelind-SAR ADC, emerged to achieve moderate-to-high speeds and resolutions with decent energy efficiency. A conventional OTA-based residue amplifier of the pipelined-SAR

ADC consumes more power and its design difficulty increases in advanced CMOS technology. To overcome these hurdles, a dynamic amplifier is investigated. However, PVT variation of its gain is critical. Chapter 4 and Chapter 5 discusses temperature compensation techniques of dynamic amplifier's gain. Chapter 4 introduces a temperature-insensitive time-based residue amplifier. It consists of a VTC and a TVC. Their temperature coefficients have different polarities, and the multiplication-based temperature compensation removes the overall gain's linear dependence on temperature. Additionally, high gain is achieved by cascading a VTC and a TVC. In contrast, Chapter 5 introduces a simpler temperature compensation technique using a conventional dynamic amplifier. A temperature-dependent common-mode detector in this compensation technique achieves temperature-insensitiveness, using the same multiplication-based compensation principle. However, gain is still determined by a conventional dynamic amplifier.

6.2 Future Work

6.2.1 Trends of wireless power transfer

End-to-end efficiency of a magnetically coupled WPT system is significantly affected by distance and coil orientation between a PTU and a PRU, and a coupling coefficient between a TX coil and a RX coil is a parameter that includes the effects of distance and orientation. Moreover, load resistance affects PCE significantly because light-load efficiency is mainly degraded by excessive switching power of the power transistors. To achieve stable power transfer, regulating rectifiers were proposed [45, 92, 93], and a load-sensing scheme was combined with a regulating rectifier [93]. However, these works did not adopt offset-calibrated active diodes. Therefore, higher PCE and VCR are expected if offset-calibrated active diodes are combined with regulating rectifiers. Moreover, different load-sensing schemes, different active diode feedback control loops [42], bidirectional wireless power transfer [94], and GaN-based power transistors for TX and RX [42, 95] can be explored further.

6.2.2 Trends of battery chargers

A switching battery charger is another popular battery charger architecture. It utilizes an inductor, and its fundamental operation is similar to an inductor-based switching DC-DC converter. Conventionally, this charger also adopts multiple feedback loops to achieve CC-CV regulation. Unified amplifier-based regulation can apply to this type of charger to reduce I_{Q}. Moreover, monitoring and compensation of battery's built-in resistance [50,53,96] and different charging methods such as pulse charging optimization [97] and sinusoidal charging [98] can be explored further.

6.2.3 Trends of low-power high-speed ADCs

As a sampling frequency approaches technology limit, power consumption of a high-speed ADC increases dramatically, whereas power consumption of the ADC is linearly proportional to the sampling frequency when the sampling frequency is much lower than technology limit. To overcome this speed-power bottleneck, a time-interleaving scheme can be used. Therefore, time-interleaved pipelined-SAR or SAR ADCs for hundreds MS/s-to-GS/s can be explored with a careful consideration of channel mismatches [73,99,100].

Dynamic or digital amplifier techniques still have room for further exploration [87, 90, 101, 102]. In particular, linearity enhancement and PVT-stabilization are emerging topics. In this dissertation, we assumed that foreground calibration calibrates process variation of a dynamic amplifier. For future work, background calibration techniques can be explored in combination with a time-interleaving scheme to achieve low-power high-speed operations.

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APPENDIX A

ANALYSIS OF CMOS ACTIVE RECTIFIER POWER CONVERSION EFFICIENCY

Power conversion efficiency (PCE) is a key figure-of-merit of a rectifier. PCE of a CMOS active rectifier was analyzed comprehensively in the previous works [39, 48]. Here, we derive compact closed-form equations for conduction loss and switching loss as functions of a duty ratio. To simplify the analysis, we assume that i) the rectifier input voltage is sinusoidal, ii) the rectified output voltage is constant, and iii) an active diode is switched at right on/off timings. These assumptions are valid if heavy load does not distort the input waveform much, the output capacitance is large, and offset/delay calibration works properly.

Fig. A.1 shows the simplified voltage waveform for the PCE analysis. Conduction time, T_{ON}, and duty ratio, D, can be expressed as

$$\begin{aligned} T_{\text{ON}} &= T - \frac{2}{\omega_0} \cdot \sin^{-1}(VCR) \\ D &= 1 - \frac{2}{\pi} \cdot \sin^{-1}(VCR) \end{aligned} \tag{A.1}$$

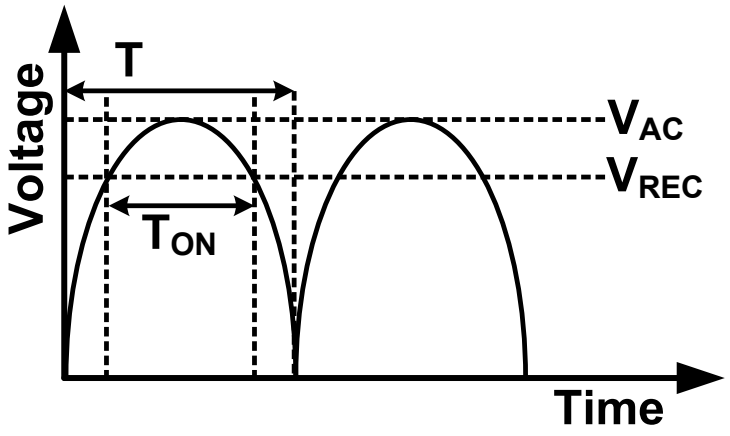


Figure A.1: Simplified rectifier input waveform.

where ω_0 is the input carrier angular frequency and $T = \dfrac{1}{2f_0}$. VCR is defined as $V_{\text{REC}}/V_{\text{AC}}$. Therefore, VCR is given by

$$VCR = \sin(\frac{\pi}{2}(1-D)) = \cos(\frac{\pi}{2}\cdot D) \tag{A.2}$$

From the average load current equation,

$$I_{\text{L,avg}} = \frac{V_{\text{R}}}{R_{\text{L}}} = \frac{2}{T}\int_{t_0}^{T/2} \frac{V_{\text{AC}}\sin(\omega_0 t) - V_{\text{R}}}{R_{\text{SW}}} dt \tag{A.3}$$

$$\frac{R_{\text{SW}}}{R_L} = \frac{2}{\pi}\cdot\frac{\sqrt{1-VCR^2}}{VCR} - D = \frac{2}{\pi}\cdot\tan(\frac{\pi}{2}\cdot D) - D \tag{A.4}$$

where R_{L} is the load resistance and R_{SW} is the total on-resistance, $R_{\text{on, p}} + R_{\text{on, n}}$, of the power transistors along the current path. From this resistance ratio, we can obtain the power ratio of $P_{\text{COND}}/P_{\text{LOAD}}$ as a function of the duty ratio.

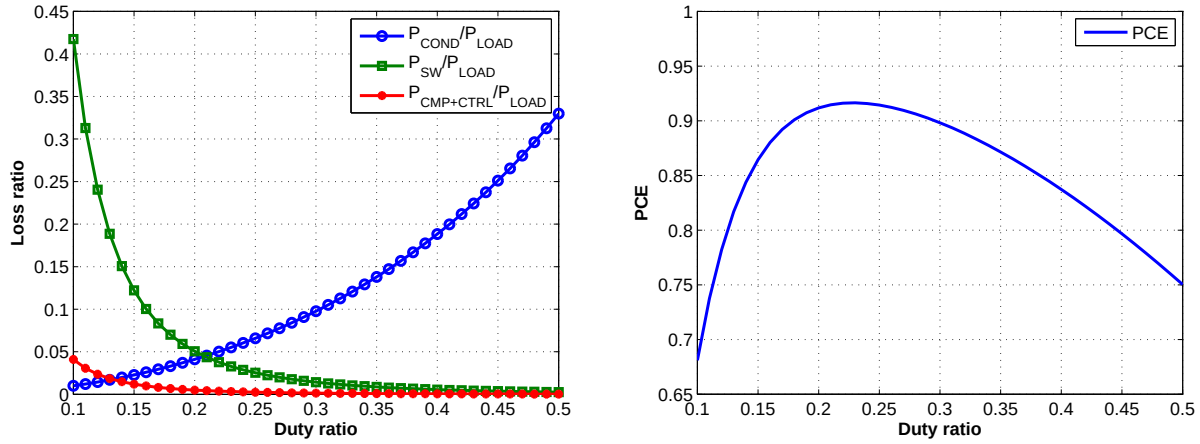
$$\begin{aligned} P_{\text{COND}} &= \frac{2}{T}\int_{t_0}^{T/2} \frac{(V_{\text{AC}}\sin(\omega_0 t) - V_{\text{REC}})^2}{R_{\text{SW}}} dt \\ &= \frac{2}{T}\cdot\frac{{V_{\text{REC}}}^2}{R_{\text{L}}}\cdot\frac{R_{\text{L}}}{R_{\text{SW}}}\int_{t_0}^{T/2}(\frac{\sin(\omega_0 t)}{VCR} - 1)^2 dt \\ &= \frac{2}{T}\cdot P_{\text{LOAD}}\cdot\frac{R_{\text{L}}}{R_{\text{SW}}}\int_{t_0}^{T/2}(\frac{\sin(\omega_0 t)}{VCR} - 1)^2 dt \end{aligned} \tag{A.5}$$

$$\frac{P_{\text{COND}}}{P_{\text{LOAD}}} = \frac{\pi D}{4}\cdot\frac{\tan^2(\frac{\pi}{2}\cdot D) - \frac{6}{\pi D}\cdot\tan(\frac{\pi}{2}\cdot D) + 3}{\tan(\frac{\pi}{2}\cdot D) - \frac{\pi}{2}\cdot D} \tag{A.6}$$

Interestingly, (A.6) reveals that the conduction loss ratio is independent of the output DC voltage and physical constants relevant to the technology.

On the other hand, switching loss ratio is given by

$$\frac{P_{\text{SW}}}{P_{\text{LOAD}}} = \frac{\pi f_0 C_{\text{gate,n,unit}} R_{\text{on, n,unit}}}{\alpha\cdot(\tan(\frac{\pi}{2}\cdot D) - \frac{\pi}{2}\cdot D)} \tag{A.7}$$



(a) (b)

Figure A.2: (a) Loss ratio vs. Duty ratio and (b) PCE vs. Duty ratio

where f_0 is the input carrier frequency, $C_{\text{gate,n,unit}}$ and $R_{\text{on, n,unit}}$ are the unit gate capacitance and the unit on resistance of the NMOS power transistor, and α is $R_{\text{on,n}}/R_{\text{SW}}$. We can observe that the switching loss ratio is a function of a duty ratio and technology-dependent constants. P_{CMP} and P_{CTRL} are mixed with static power consumption and dynamic power consumption. Therefore, they can be modeled by

$$P_{\text{CMP}} + P_{\text{CTRL}} = V_{\text{REC}} I_{\text{BIAS,equiv}} + f_0 C_{\text{equiv}} V^2{}_{\text{REC}} \tag{A.8}$$

where $I_{BIAS,equiv}$ is equivalent current for static power consumption modeling an C_{equiv} is equivalent capacitance for dynamic power consumption modeling. Therefore, the loss ratio of comparators and control circuits is given by

$$\frac{P_{\text{CMP}} + P_{\text{CTRL}}}{P_{\text{LOAD}}} = \frac{\pi}{2} \cdot \frac{R_{\text{SW}} \cdot (\frac{I_{\text{BIAS,equiv}}}{V_{\text{REC}}} + f_0 C_{\text{equiv}})}{\tan(\frac{\pi}{2} \cdot D) - \frac{\pi}{2} \cdot D} \tag{A.9}$$

Fig. A.2(a) shows each loss ratio, assuming unit transistors are $W_{\text{P}}/L_{\text{P}} = 175\,\mu\text{m}/0.5\ \mu\text{m}$ and $W_{\text{N}}/L_{\text{N}} = 75\,\mu\text{m}/0.5\,\mu\text{m}$ in TSMC 350-nm 5-V devices. Technology parameters are assumed to be $C_{\text{gate,n,unit}} = 112.5\,\text{pF}$, $R_{\text{on, n, unit}} = 41.13\,\Omega$, $\alpha = 0.36$, $V_{\text{REC}} = 3.6\,\text{V}$, $I_{\text{BIAS,equiv}} = 10\,\mu\text{A}$,

$C_{\text{equiv}} = 1\,\text{pF}$, and $R_{\text{SW}} = 1.13\,\Omega$. As expected, switching loss dominates total loss in low duty ratio region and conduction loss does in low-to-medium duty ratio region. The corresponding PCE is plotted in Fig. A.2(b) and the optimal duty ratio is found between 0.2 and 0.25 for the above technology parameters.

While the above example shows loss ratios and the PCEs with respect to duty ratios, the equation (A.4) reveals that R_{SW} is a monotonically increasing function of D under the constant R_{L}. Therefore, a large duty ratio corresponds to large R_{SW}, vice versa. Note that R_{SW} is a function of transistor widths and V_{REC}. Therefore, there exists the optimal area of a rectifier to maximize PCE under certain R_{L} and V_{REC}. Adaptive power transistor sizing utilizes this property to maintain high PCE over a wide range of R_{L}.

APPENDIX B

TEMPERATURE COMPENSATION AND NOISE ANALYSIS

OF THE TIME-BASED RESIDUE AMPLIFIER

B.1 Temperature compensation analysis of the time-based residue amplifier

The conversion factor of the VTC in Fig. 4.11 and Fig. 4.12 is given by

$$F_{\text{VTC}} = \frac{\Delta t}{V_{\text{res,diff}}} \approx \frac{g_{\text{m,MD1}}}{I_{\text{MD1}}^2} \cdot (V_{\text{DD}} - V_{\text{CM}}) \cdot C_{\text{A}} = \frac{2(V_{\text{DD}} - V_{\text{CM}}) \cdot C_{\text{A}}}{K_{\text{MD1}} \cdot V_{\text{OV,MD1}}^3} \tag{B.1}$$

where $K_{\text{MD1}} = 1/2 \times \mu_{\text{n}} \times C_{\text{ox}} \times (W/L)_{\text{MD1}}$. $V_{\text{OV, MD1}}$ is the overdrive voltage of MD_1. C_{A} is the output capacitance of dynamic integrator (assume the SWC switch is off in Fig. 4.11). The TC of (B.1) is given by

$$\frac{\partial F_{\text{VTC}}}{\partial T} = -\frac{2(V_{\text{DD}} - V_{\text{CM}}) \cdot C_{\text{A}}}{K_{\text{MD1}} \cdot V_{\text{OV,MD1}}^3} \cdot (\frac{1}{K_{\text{MD1}}} \cdot \frac{\partial K_{\text{MD1}}}{\partial T} + \frac{3}{V_{\text{OV,MD1}}} \cdot \frac{\partial V_{\text{OV,MD1}}}{\partial T}) \tag{B.2}$$

MD_1 is biased in the saturation region, and MD_4 is in the triode region in Fig. 4.11. The current passing MD_4 is given by

$$2 \cdot K_{\text{MD1}} \cdot V_{\text{OV,MD1}}^2 = K_{\text{MD4}} \cdot (V_{\text{OV,MD4}} - \frac{1}{2} \cdot V_{\text{DS,MD4}}) \cdot V_{\text{DS,MD4}} \tag{B.3}$$

where $K_{\text{MD4}} = \mu_{\text{n}} \times C_{\text{ox}} \times (W/L)_{\text{MD4}}$. $\text{V}_{\text{OV, MD4}}$ and $\text{V}_{\text{DS, MD4}}$ are the overdrive voltage and drain-to-source voltage of MD4, respectively. Taking a derivative to (B.3) with respect to temperature to get the TC of $\text{V}_{\text{OV, MD1}}$, the result is

$$\frac{\partial V_{\text{OV,MD1}}}{\partial T} = -\frac{\alpha \cdot V_{\text{OV,MD4}}}{\alpha \cdot (V_{\text{OV,MD4}} - V_{\text{DS,MD4}}) + 4 \cdot V_{\text{OV,MD1}}} \cdot \frac{\partial V_{\text{TH,MD1}}}{\partial T} = \beta \cdot \frac{\partial V_{\text{TH,MD1}}}{\partial T}. \tag{B.4}$$

where α is K_{MD4}/K_{MD1}, which is temperature insensitive, and $V_{TH,\,MD1}$ is the threshold voltage of MD_1 with negative TC [103]. The resulting β is negative. When deriving (B.4), body effect of MD_1 is neglected. Therefore, the TC of the conversion factor of the VTC is given by

$$\frac{\partial F_{\text{VTC}}}{\partial T} = -\frac{2(V_{\text{DD}} - V_{\text{CM}}) \cdot C_{\text{A}}}{K_{\text{MD1}} \cdot V_{\text{OV,MD1}}^3} \cdot \left(\frac{1}{K_{\text{MD1}}} \cdot \frac{\partial K_{\text{MD1}}}{\partial T} + \frac{3\beta}{V_{\text{OV,MD1}}} \cdot \frac{\partial V_{\text{TH,MD1}}}{\partial T}\right) \tag{B.5}$$

MD_1 in Fig. 4.11 is biased with $V_{OV,\,MD1}$ smaller than 100 mV to make the TC of $V_{TH,\,MD1}$ dominant in (B.5). Therefore, F_{VTC} has a negative TC.

On the other hand, the conversion factor of the TVC in Fig. 4.11 and Fig. 4.13 is given by

$$\begin{aligned} F_{\text{TVC}} &= \frac{V_{\text{out,diff}}}{\Delta t} = \frac{2 \cdot I_{\text{CP}}}{C_{\text{S}}} = \frac{2 \cdot K_{\text{MC1}} \cdot {V_{\text{OV,MC1}}}^2}{C_{\text{S}}} \\ &= \frac{2 \cdot K_{\text{MC1}}}{C_{\text{S}}} \cdot (V_{\text{DD}} - \frac{I_{\text{CP}}}{\gamma} \cdot R - V_{\text{TH,MC1}})^2 \end{aligned} \tag{B.6}$$

where $K_{\text{MC1}} = 1/2 \times \mu_{\text{n}} \times C_{\text{ox}} \times (W/L)_{\text{MC1}}$. I_{CP} is the drain current of MC_1. γ is the current mirror factor between MC_1 and MC_0. $V_{TH,\,MC1}$ and $V_{OV,\,MC1}$ are the threshold voltage and the overdrive voltage of MC_1, respectively. C_S is the total sampling capacitance in the second-stage SAR ADC. The TC of (B.6) is given by

$$\frac{\partial F_{\text{TVC}}}{\partial T} = \frac{-\frac{\gamma}{R} \cdot \frac{2}{C_{\text{S}}}}{\frac{\gamma \cdot V_{\text{OV,MC1}}}{2 \cdot I_{\text{CP}} \cdot R} + 1} \cdot \left(\frac{\partial V_{\text{TH,MC1}}}{\partial T} - \frac{V_{\text{OV,MC1}}}{2 \cdot K_{\text{MC1}}} \cdot \frac{\partial K_{\text{MC1}}}{\partial T}\right) \tag{B.7}$$

As $I_{\text{CP}} \times R = \gamma \times (V_{\text{DD}} - V_{\text{GS,\,MC1}})$, where $V_{\text{GS,\,MC}_1}$ is the gate-to-source voltage of MC_1. Therefore, the TC of conversion factor of the TVC is simplified as

$$\frac{\partial F_{\text{TVC}}}{\partial T} \approx -\frac{2 \cdot \gamma}{R \cdot C_{\text{S}}} \cdot \left(\frac{\partial V_{\text{TH,MC1}}}{\partial T} - \frac{V_{\text{OV,MC1}}}{2 \cdot K_{\text{MC1}}} \cdot \frac{\partial K_{\text{MC1}}}{\partial T}\right) \tag{B.8}$$

MC_1 is biased with $V_{OV,\,MC1}$, which is about 120 mV to make the TC of $V_{TH,\,MC1}$ (negative TC [103]) dominant in (B.8). Here, thermal variation of R is ignored. Therefore, F_{TVC} has a positive TC.

Similarly, using the same derivation procedure of the temperature variation analysis, (B.9) and (B.10) show the supply voltage coefficient of VTC and TVC, respectively.

$$\frac{\partial F_{\text{VTC}}}{\partial V_{\text{DD}}} = \frac{C_{\text{A}}}{K_{\text{MD1}} \cdot V_{\text{OV,MD1}}^3} \cdot (1 - \frac{3 \cdot \delta \cdot V_{\text{DD}}}{V_{\text{OV,MD1}}} \cdot \frac{\partial V_{\text{TUNE}}}{\partial V_{\text{DD}}}) \tag{B.9}$$

$$\begin{aligned} \frac{\partial F_{\text{TVC}}}{\partial V_{\text{DD}}} &= \frac{4}{C_{\text{S}}} \cdot \frac{V_{\text{DD}} - V_{\text{TH,MC1}} - \frac{I_{\text{CP}} \cdot R}{\gamma}}{\frac{1}{K_{\text{MC1}}} + \frac{2R}{\gamma} \cdot (V_{\text{DD}} - V_{\text{TH,MC1}} - \frac{I_{\text{CP}} \cdot R}{\gamma})} \\ &= \frac{4}{C_{\text{S}}} \cdot \frac{V_{\text{OV,MC1}}}{\frac{1}{K_{\text{MC1}}} + \frac{2R}{\gamma} \cdot V_{\text{OV,MC1}}} \end{aligned} \tag{B.10}$$

where $\delta = \beta \times (V_{\text{DS, MD4}}/V_{\text{OV, MD4}})$, β is the factor in (B.4). When deriving (B.9), we assume $V_{\text{DD}} = 2 \times V_{\text{CM}}$. Under the same bias conditions, (B.9) and (B.10) have a negative VC and a positive VC, respectively.

B.2 Noise analysis of the time-based residue amplifier

The noise of the time-based residue amplifier consists of noise from the VTC and TVC. For the stochastic zero-crossing delay variables td_P and td_N in Fig. 4.11 and Fig. 4.12, their delay difference variance due to circuit noise is given by

$$\sigma_{td_P - td_N}^2 = \sigma_{td_P}^2 + \sigma_{td_P}^2 - 2 \cdot COV[td_P, td_N] \tag{B.11}$$

Since td_P and td_N are correlated due to the same noise sources, calculation of their covariance, $COV[td_P, td_N]$, is complex. For simplicity, the worst case output noise power of the VTC is given by

$$(\sigma_{td_P - td_N}^2)_{\text{WORST}} = (\sigma_{td_P} + \sigma_{td_N})^2 \tag{B.12}$$

The zero-crossing delay variance is affected by three terms which are windowed integrals of thermal noise, initial integrated thermal noise (kT/C), and noise from a ZCD [104]. The jitter deriva-

tion for an inverter-based ring oscillator in [104] is still applicable to our noise analysis. According to [104], the time delay variance is given by

$$\sigma_{td_P}^2 = \frac{td_{P0}}{2I_{MD1,P}^2} \cdot S_{\text{iP,noise}} + \frac{kTC_{\text{A}}}{I_{MD1,P}^2} + \frac{C_A^2\overline{v_{i,noise-ZCD}^2}}{I_{MD1,P}^2} \tag{B.13}$$

$$\sigma_{td_N}^2 = \frac{td_{N0}}{2I_{MD1,N}^2} \cdot S_{\text{iN,noise}} + \frac{kTC_{\text{A}}}{I_{MD1,N}^2} + \frac{C_A^2\overline{v_{i,noise-ZCD}^2}}{I_{MD1,N}^2} \tag{B.14}$$

$$S_{\text{iP,noise}} = S_{\text{iN,noise}} = 2kT\gamma g_{\text{m,MD1}} + kTg_{\text{ds0,MD4}} \tag{B.15}$$

$$td_{P0} = \frac{C_{\text{A}}(V_{\text{DD}} - V_{\text{CM}})}{I_{MD1,P}} \tag{B.16}$$

$$td_{N0} = \frac{C_{\text{A}}(V_{\text{DD}} - V_{\text{CM}})}{I_{MD1,N}} \tag{B.17}$$

where $S_{\text{iP,noise}}$ and $S_{\text{iN,noise}}$ are noise power spectral densities due to MD_1 and MD_4 at V_P and V_N in Fig. 4.11 before zero-crossing occurs, respectively. The last two terms of (B.13) and (B.14) are much less than the first term, and the second term of (B.15) is much less than the first term. Because of a small input voltage (the difference between $I_{\text{MD1,P}}$ and $I_{\text{MD1,N}}$ is small), the input-referred noise of the time-based residue amplifier due to the VTC in the worst case is given by

$$\overline{v_{i,noise-VTC}^2} = \frac{(\sigma_{td_P} + \sigma_{td_N})^2}{F_{\text{VTC}}^2} \approx \frac{4kT\gamma}{C_{\text{A}}} \cdot \frac{I_{\text{MD1}}}{g_{\text{m,MD1}}(V_{\text{DD}} - V_{\text{CM}})}. \tag{B.18}$$

The output noise of the TVC is given by [79]

$$\overline{v_{o,noise-TVC}^2} = \frac{4kT\gamma}{2C_{\text{A}}^2} \cdot (g_{\text{m,MC1}} + g_{\text{m,MC4}}) \cdot T_{\text{ON}} \tag{B.19}$$

where T_{ON} is the time used for dead zone elimination in Fig. 4.12. According to (B.1) and (B.19), the input-referred noise of the time-based residue amplifier due to the TVC is given by

$$\overline{v_{i,noise-TVC}^2} = \overline{v_{i,noise-VTC}^2} \cdot \frac{I_{\text{MD1}}^3 \cdot T_{\text{ON}} \cdot (g_{\text{m,MC1}} + g_{\text{m,MC4}})}{8 \cdot I_{\text{CP}}^2 \cdot C_{\text{A}} \cdot (V_{\text{DD}} - V_{\text{CM}}) \cdot g_{\text{m,MD1}}} \tag{B.20}$$

Since T_{ON} is much less than the integration time (td_P and td_N) of the dynamic integrator, the noise in (B.20) is much less than the noise in (B.18). Therefore, the input-referred noise of the time-based residue amplifier in Fig. 4.11 is dominated by the noise from the VTC.