AN OPEN-LOOP AMPLIFIER MULTI-BIT SIGMA DELTA MODULATOR

A Thesis

by

TAKASHI MIKI

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Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Peng Li
	Suman Chakravorty
Head of Department,	Miroslav M. Begovic

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ABSTRACT

A new multi-bit quantizer for sigma delta modulators is proposed. The multi-bit quantizer has multiple single-bit quantizers, and the output of one of the single-bit quantizers is fed back to the input of another single-bit quantizer via a filter. Multi-bit quantization is achieved by averaging the outputs of the single-bit quantizers. Because of this architecture, the multi-bit quantizer realizes multi-bit quantization without external signals such as dithering signals that are needed in conventional architectures. The multi-bit quantizer allows for designing a new open-loop amplifier multi-bit sigma delta modulator. The open-loop amplifier multi-bit sigma delta modulator uses differential pairs for its loop filter instead of closed-loop amplifiers that consume considerable power for high frequency applications. The open-loop amplifier multi-bit sigma delta modulator is designed with a 90nm CMOS process. The achievable SNDR is 43dB with the bandwidth of 80MHz when noises other than quantization noises are not taken into consideration. The sampling frequency is 2.56GHz, and the power consumption of main analog parts is 15mA.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

The thesis committee consists of Professors Jose Silva-Martinez [Advisor], Edgar Sanchez-Sinencio, and Peng Li of the Department of Electrical and Computer Engineering and Professor Suman Chakravorty of the Department of Aerospace Engineering.

All work conducted for the thesis was completed by the student independently. The student is the one who came up with the idea on which this research is based without any input from any person. He developed the idea and planed the research project without any help of other people. All analysis made for this work was carried out all by the student himself without any support even in the form of discussion. There exists no joint researcher of the student on this project.

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1. INTRODUCTION

In order to achieve a high SNDR with a single-loop sigma delta modulator, there are two major matters to be considered: the order of the loop filter and the bit number of the quantizer. The SNDR of a single loop sigma delta modulator can be improved by using a loop filter of a high order. Also, a higher SNDR can be obtained by increasing the bit number of its quantizer, an internal ADC.

There are many possible architectures for a multi-bit quantizer, a quantizer whose bit number is larger than one. One of the most popular multi-bit quantizers is a flash ADC. A VCO based quantizer is another popular multi-bit quantizer [2, 3]. When these multi-bit quantizers are used, the input analog signal to the quantizer is mapped into a digital output which is tied to a certain range of the input analog signal. Thus, the signal amplitude at the input of the quantizer has to be well controlled. Partly for this purpose, not only to provide sufficient loop gain, opamps with a high gain are vital building blocks for conventional multi-bit sigma delta modulators. It is true especially when a flash ADC is chosen as a quantizer. A flash ADC divides an input signal into discrete several levels which result in the steps of the output digital signal. If the input signal for the flash ADC is too small or not well controlled, the performance of the flash ADC deteriorates. As to VCO based quantizers, the input signal can be made small when the phase of the ring oscillator of the VCO is chosen as an output signal [3]. Still, however, closed-loop amplifiers are needed in order to have the input signal of the quantizer well controlled.

As described briefly so far, closed-loop amplifiers are a building block which can hardly be omitted when a multi-bit sigma delta modulator is designed. In contrary, if a single-bit quantizer is chosen as an internal ADC, open-loop amplifier sigma delta modulators can be designed. This is because the single-bit quantizer, which is a comparator

in most cases, has its own gain and that the gain is used as the loop gain [4]. Meanwhile, this means the signal amplitude at the input of the quantizer is not controlled well in a single-bit sigma delta modulator. If it is possible that a multi-bit quantization is realized while making full use of the intrinsic gain of single-bit quantizers, an open-loop amplifier multi-bit sigma delta modulator may be able to be designed. That architecture can be power efficient because power consuming closed-loop amplifiers can be omitted. In this research, a new multi-bit sigma-delta architecture is to be proposed, which is a candidate for an open-loop amplifier multi-bit sigma delta modulator.

As mentioned previously, a VCO-based multi-bit quantizer can produce a high gain when the phase of the ring oscillator is used as the output signal. There is another multi-bit quantizer that can provide loop gain, and it has been proposed in the context of stochastic analog-digital conversion [5]. The basic idea of the stochastic analog-digital conversion is that when uncorrelated N variables with common variation are averaged, the variation of the averaged variable is the one N^{th} of the original variation. Now this idea is applied to a situation where an input signal is quantized by N single-bit quantizers in parallel. When the quantization noises from the N single-bit quantizers are uncorrelated from each other, the average of the outputs of the N single-bit quantizers contains the quantization noise whose power is the one N^{th} of that of the individual quantizers. Dithering signals can be used to make the N quantization noises uncorrelated [5], but adding dithering signals makes circuits more complex. It has been also proposed that predefined reference voltages instead of dithering signals are mixed into an input signal at some point before each of the single-bit quantizers to make the quantization noises uncorrelated [6]. External signals such as dithering signals and reference voltages are needed to make quantization signals uncorrelated from one another in these preexisting works. This kind of quantizer in which multiple single-bit quantizers are provided in parallel and an output signal are obtained by averaging the quantized signals from the multiple quantizers are called an averaging

multi-bit quantizer in this thesis thereafter.

In this thesis, a past work of an averaging multi-bit quantizer is reviewed first. Secondly, averaging multi-bit quantizers that can be constructed without using external signals such as dithering signals are introduced. Thirdly, a multi-bit sigma delta modulator with an averaging multi-bit quantizer is designed. Finally, some simulation results will be presented.

This research will show an open-loop amplifier multi-bit sigma delta modulator can be designed using the newly proposed averaging multi-bit quantizers. The simulation results indicate that the proposed sigma delta modulator has a potential of suppressing power consumption at high frequency sampling.

2. AVERAGING MULTI-BIT QUANTIZERS*

2.1 Averaging Multi-bit Quantizers Prior to This Work

The primitive idea of an averaging multi-bit quantizer is shown in [5], where a dithering signal is applied to just before each single-bit quantizer. Even if a dithering signal is added to the input signal of a single-bit quantizer, the dithering signal does not increase much the power of the quantization noise in the digitized signal coming out of the single-bit quantizer. The effect of the dithering signal to the digitized output from the single-bit quantizer is randomizing the quantization noise. In other words, the quantization noise from each of the single-bit quantizers is randomized independently. As a result, the quantization noises from the single-bit quantizers become uncorrelated from one another. Remember that when N of uncorrelated variables with common variation are averaged, the variation of the averaged variable is the one N^{th} of the original variation. This is the basic principle on which an averaging multi-bit quantizer is based. Because of this nature, the quantization noise in the average of N quantized signals, which have been made uncorrelated by the dithering signals, reduces by $10log(N)$.

DC reference voltages can be used instead of dithering signals to make the quantized signals from multiple single-bit quantizers uncorrelated [6]. This is base on the assumed fact that if there are two different input signals into a sigma delta modulator, the two quantization noises that are generated from the two different input signals are uncorrelated from each other. In the architecture in [6], the last stage of the loop filter is composed of multiple and identical sigma delta units with the second loop filter which are connected in parallel to the common first loop filter, and the reference voltages are added at the inputs of the sigma delta units. The reference voltages are chosen so that they are different from one another but that the sum of them is equal to zero. Because of the latter condition, the

* Part of this section is reprinted from "Sigma-delta Modulator with Averaged-signal Feedback," Aug. 15 2017. US Patent 9,735,801.

components of the quantized signals coming from the reference voltages are canceled out when the quantized signals are averaged, and the digitized input signal is not affected by the reference voltages. The quantization noises, however, are influenced by the reference voltages and are made uncorrelated from one another because of the assumed fact noted above.

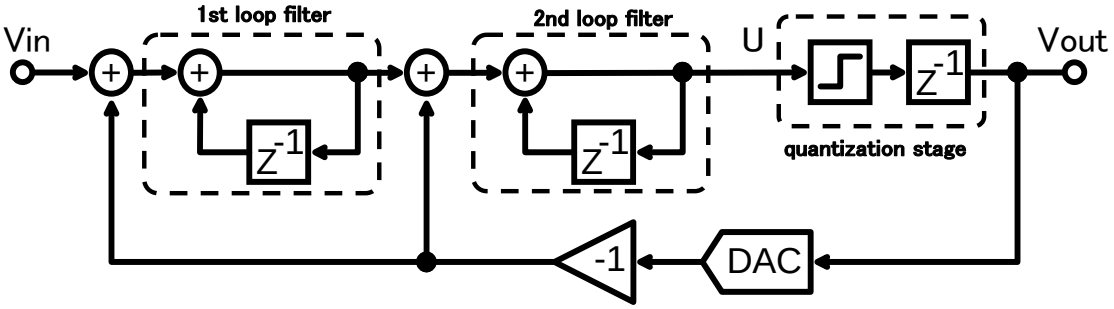

Figure 2.1: The diagram of a simple second order sigma delta modulator with two zeros at the origin

The effect of the reference voltages was demonstrated in the case of a second order sigma delta modulator with two zeros at the origin, whose diagram is shown in Figure 2.1. The second loop filter and single-bit quantizers are duplicated into 16 branches. The output signal of the single-bit quantizer is ± 1. The reference DC signals are -0.2, -0.175, -0.15, -0.125, -0.1, -0.075, -0.05, -0.025, 0.025, 0.05, 0.075, 0.1, 0.15, 0.175, and 0.2. The SNDR was simulated for both of a single-bit and averaging multi-bit quantizers, and the result is shown in Figure 2.2. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling frequency. In short, the input frequency is about the one third of the bandwidth. The results show that the SNDR improves about 12 dB, which well matches the predicted value, $10log_{10}(16)$. The FFT spectrum of the second order averaging multi-bit sigma delta modulator with reference signals is shown in Figure 2.3, and it can be seen

that the noise level is lower than that of the simple second order sigma delta modulator by about 12dB. Figure 2.4 illustrates the time transient input and output waveforms of the second order averaging multi-bit sigma delta modulator with reference signals. The output digital signals can be values other than ± 1, which results in the reduced power of the quantization noise in the output signal.

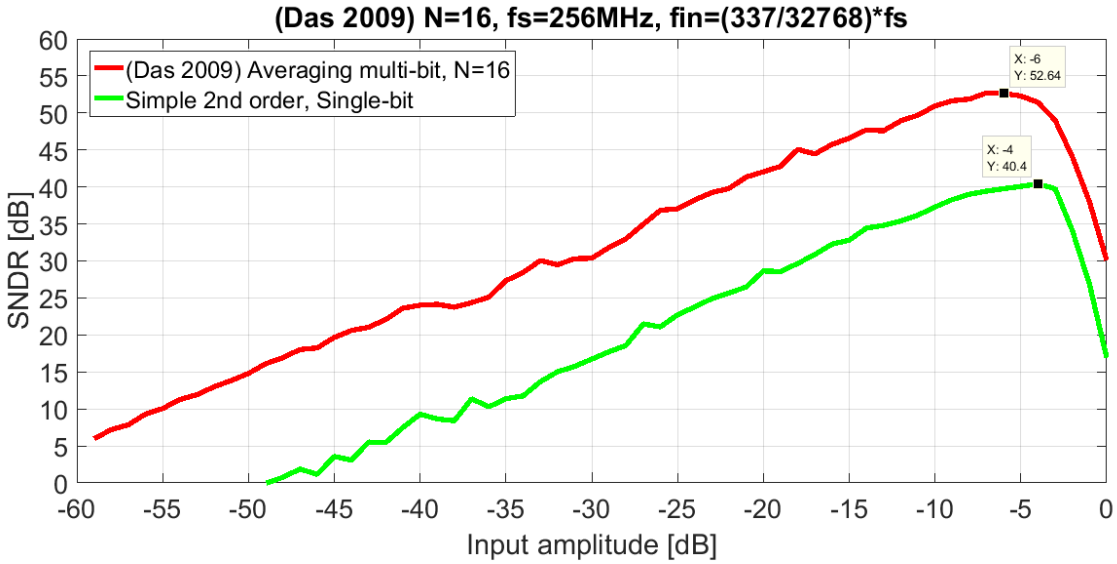

Figure 2.2: The SNDR of the second order averaging multi-bit sigma delta modulator with reference signals

It should be noted that the multiple second loop filters are parts of the averaging multi-bit quantizers in [6]. They are also a part of a loop filter. Thus, the averaging multi-bit quantizer in [6] is a multi-bit quantizer with noise shaping like some types of VCO-based multi-bit quantizer [2].

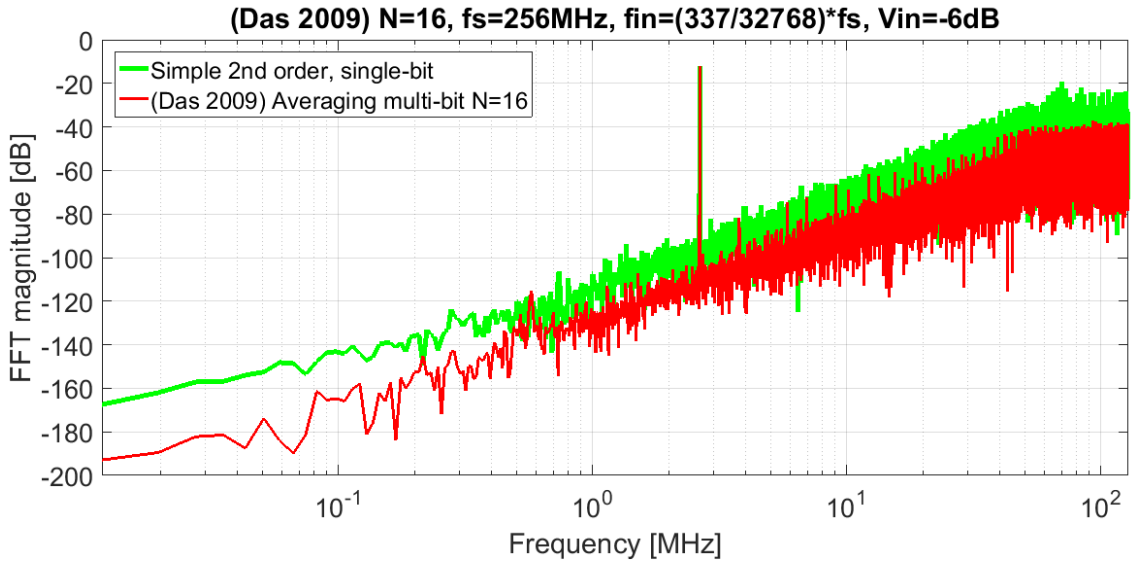

Figure 2.3: The spectrum of the second order sigma delta modulator having the averaging multi-bit quantizer with reference signals

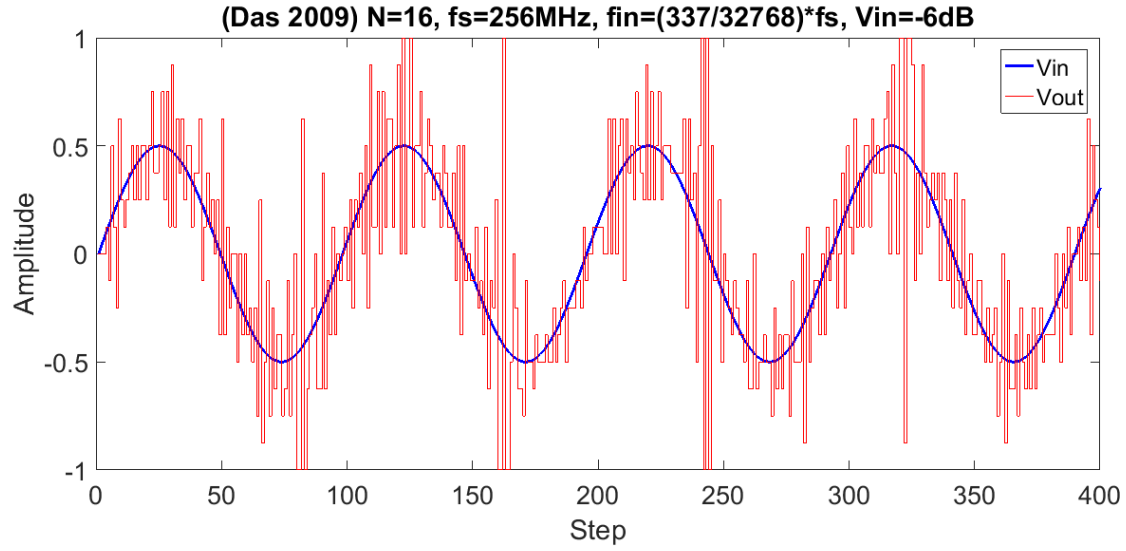

Figure 2.4: The time transient input and output waveforms of the second order sigma delta modulator having the averaging multi-bit quantizer with reference signals

2.2 Averaging Multi-bit Quantizers without External Signals

As discussed previously, the quantization noises from multiple single-bit quantizers can be randomized directly by adding dithering signals just before the single-bit quantizers or by adding some reference signals to the single-bit quantizers via a sigma delta unit. In this section, how to realize an averaging multi-bit quantizer without external signals is examined.

The starting point for expanding the averaging multi-bit quantizers in [5] and [6] is the following observation: the transfer function of the quantization stage is Z^{-1}. In the simple second order sigma delta modulator in Figure 2.1, the quantization stage consists of a single-bit quantizer and the delay of one sampling period. As mentioned above, the averaging multi-bit quantizer in [6] includes the multiple second loop filters, thus the quantization stage begins at the point from which the input path diverges to each second loop filter and ends at the node of the averaged digital outputs. The transfer function of the averaging multi-bit quantizer is still Z^{-1} when it is assumed that the gain of the signal-bit quantizer is unity. Based on this observation, it is natural to think of replacing the quantization stage with a block which includes multiple single-bit quantizers but whose transfer function is Z^{-1}.

There is another feature that the averaging multi-bit quantizers mentioned above have in common: there exists an architecture with which the quantization noises from single-bit quantizers differ from one another. In the averaging multi-bit quantizer in [5], the dithering signals that are added at the inputs of single-bit quantizers are different from one another, and thus the quantization noises produced by the single-bit quantizers are different from one another. Also, the quantization noises generated by the single-bit quantizers in [6]

are different from one another because different reference signals are added and processed by the sigma delta unit at each branch. In both cases, the differences in the quantization noises are created by changing the externally added signals. Advancing this finding, it may be possible to create the differences in the quantization noises from multiple branches by making differences in the noise transfer functions which the quantization noises go through.

Accordingly, the clues for finding a new architecture of an averaging multi-bit quantizer are: the transfer function of the quantization stage is Z^{-1}, and the noise transfer functions of the quantization noises from the single-bit quantizers are different from one another.

2.2.1 Type 1 Averaging Multi-bit Quantizer

If N of different transfer functions are needed, a natural choice is to prepare them individually. When N is small, it will be a good tactic. When N becomes larger, however, it is not realistic to construct N different transfer functions one by one. A possible way to avoid this complexity is to connect N of simple transfer functions one after another like a chain. If an input signal is applied to the one end of the chain and if the signal at each connection node is appointed as an output signal, the transfer function which the input signal goes through differs depending on which output node is selected. One of possible example of this chain-like averaging multi-bit quantizer is shown in Figure 2.5. This averaging multi-bit quantizer will be mentioned as type 1 thereafter. In the diagram of Figure 2.5, the filters, Km (m = 1, 2, . . ., N), can have a transfer function of any form. It can be proven that the transfer function of $Vout/U$ is Z^{-1} by the inductive method for any sets of Km. In the case of sigma delta modulation, however, each of the filters Km has to be a constant or low pass filter. Otherwise, it is difficult to stabilize the feedback loop of the modulator. The quantization noise generated at one single-bit quantizer is led

to the input of another single-bit quantizer via one of the filters Km, and the noise transfer functions for the quantization noises from the single-bit quantizers will become different from one another when the filters Km are chosen properly.

As the simplest example, type 1 averaging multi-bit quantizer when N is two is shown in Figure 2.6. The quantizer is used as a part of a sigma delta modulator. LP denotes the loop filter of the sigma delta modulator. Q_1 and Q_2 denote the quantization noises from the first and second single-bit quantizers, respectively. The transfer function of the quantizer, $Vout/U$, the signal transfer function (STF), the first noise transfer function (NTF1), and the second noise transfer function (NTF2) have the following expressions.

$$\frac{Vout}{U} = Z^{-1} \tag{2.1}$$

$$\text{STF} = \frac{Vout}{Vin} = \frac{LF \cdot Z^{-1}}{1 + LF \cdot Z^{-1}} \tag{2.2}$$

$$\text{NTF1} = \frac{Vout}{Q_1} = \left(\frac{Z^{-1}}{2}\right) \frac{(1 - K_1 \cdot Z^{-1})(1 - 2K_2 \cdot Z^{-1})}{1 + LF \cdot Z^{-1}} \tag{2.3}$$

$$\text{NTF2} = \frac{Vout}{Q_1} = \left(\frac{Z^{-1}}{2}\right) \frac{(1 - 2K_1 \cdot Z^{-1})(1 - K_2 \cdot Z^{-1})}{1 + LF \cdot Z^{-1}} \tag{2.4}$$

It can be understood form Equations 2.3 and 2.4 that NTF1 $\neq$ NTF2 when $K_1 \neq K_2$.

There is no universal answer about how to determine the forms of the filters Km because of the complexity of the transfer function. However, it is still possible to see the validity of this quantizer by assuming some simple forms for the filters Km and by simulating it. It is assumed that the filters Km are a constant or first order low pass filter as in Equation 2.5.

$$K_m(\text{Z}) = \alpha_m \left(\frac{1 - \beta_m}{1 - \beta_m \text{Z}^{-1}}\right), \quad (m = 1, 2, \ \ldots, N) \tag{2.5}$$

where αm and βm are constants.

The performance of the averaging multi-bit quantizer in Figure 2.5 was evaluated by

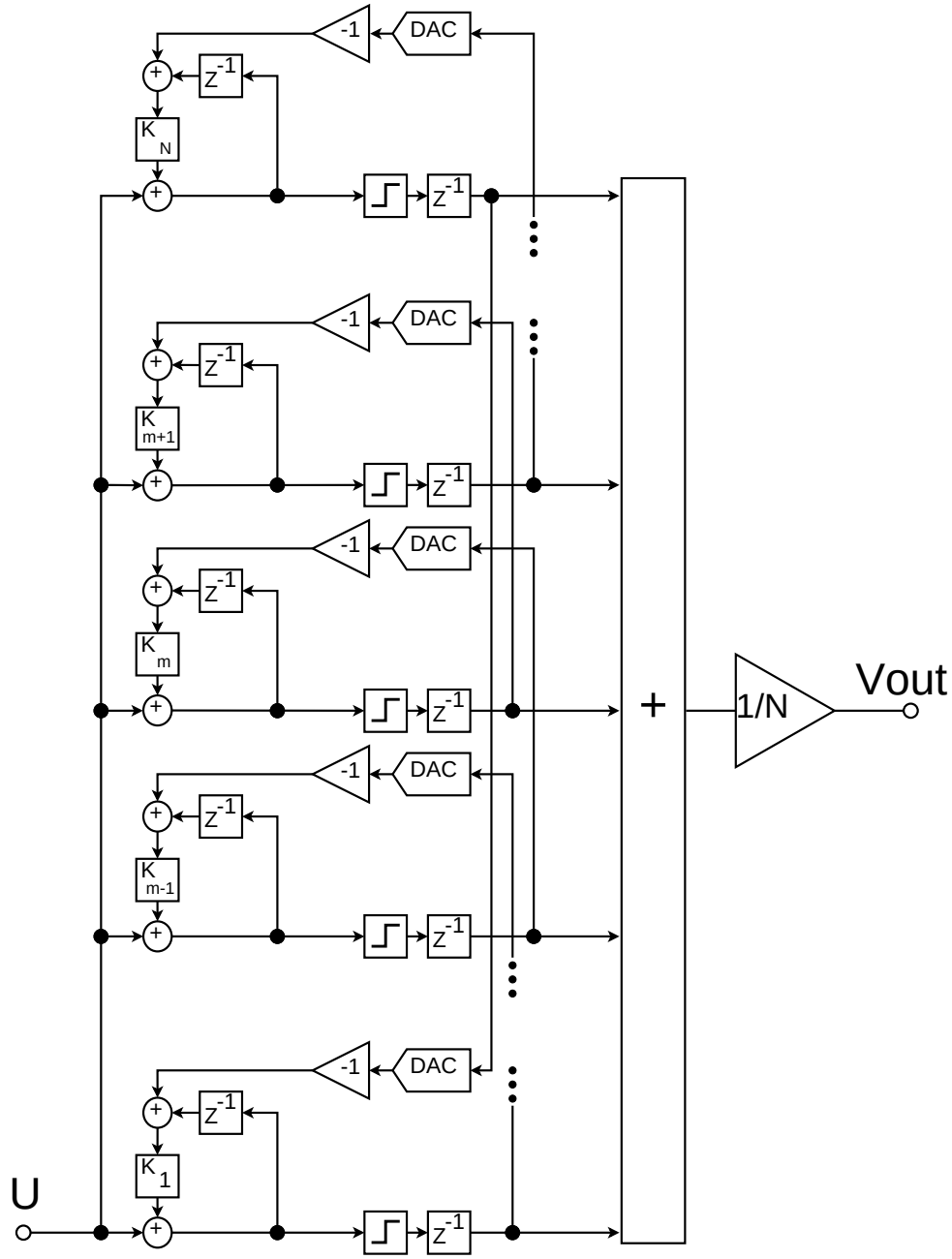

Figure 2.5: The block diagram of the quantization stage of type 1 averaging multi-bit quantizer. Reprinted from [1]

simulation when N was 8. SIMULINK is the simulation tool. The second order sigma delta modulator in Figure 2.1 was used as the test bench, and the quantization stage in

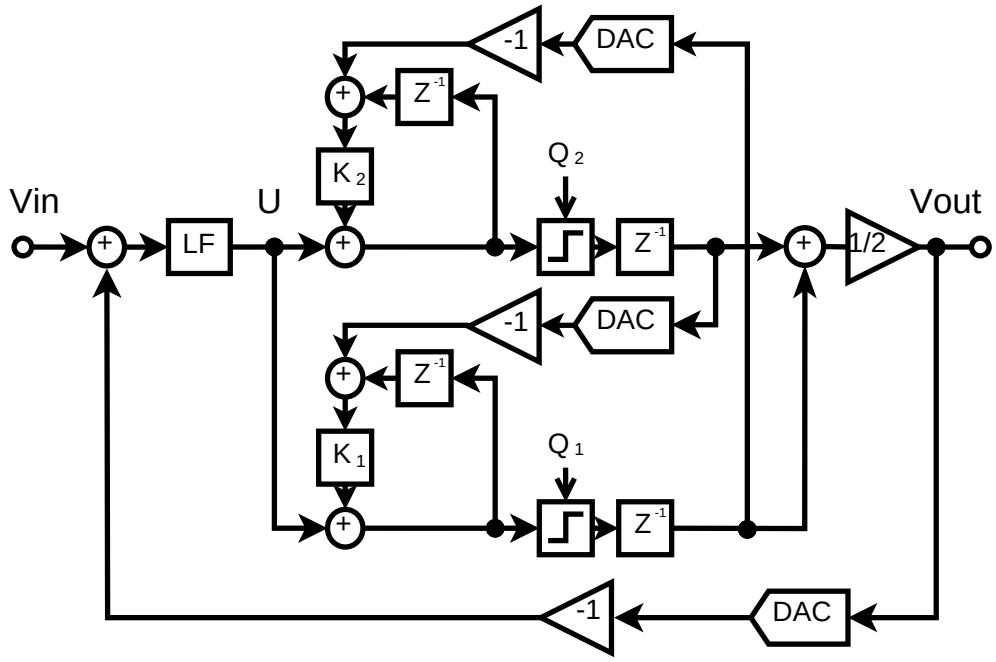

Figure 2.6: The block diagram of a sigma delta modulator with type 1 averaging multi-bit quantizer when N is two

Figure 2.1 was replaced with the one in Figure 2.5. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling frequency. Figure 2.7 shows the SNDR when the coefficients αm and βm are selected as follows: α1 = 0, α2 = 0.8, α3 = 0.8, α4 = 0.8, α5 = 0.769, α6 = 0.538, α7 = 0.308, α8 = 0.091, β1 = 0, β2 = 0, β3 = 0, β4 = 0, β5 = 0, β6 = 0, β7 = 2.462, and β8 = 3.545. The SNDR improves by ten when the single-bit quantizer is replaced by type 1 multi-bit quantizer in Figure 2.5. The FFT spectrum of the second order sigma delta modulator with type 1 averaging multi-bit quantizer is shown in Figure 2.8.

The improvement of the SNDR is obtained at the expense of the stability at the larger input amplitudes. This is because the quantization stage of type 1 works as an integration stage and increases the order of the sigma delta modulator. It can also be understood from the transfer function of the quantization stage in Figure 2.5. Each small loop including one

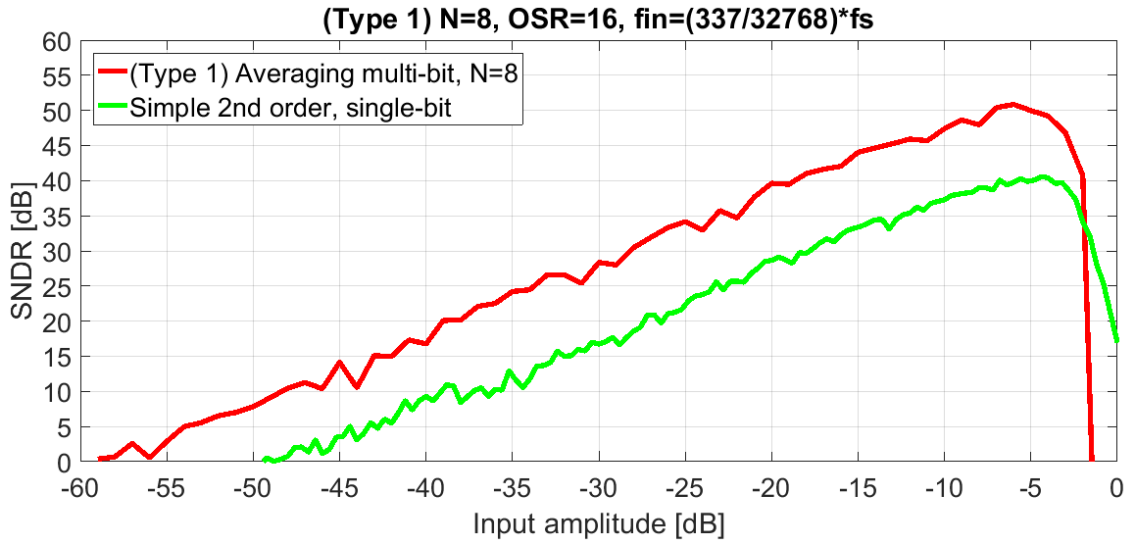

Figure 2.7: The SNDR of the second order averaging multi-bit sigma delta modulator with type 1 averaging multi-bit quantizer. Reprinted from [1]

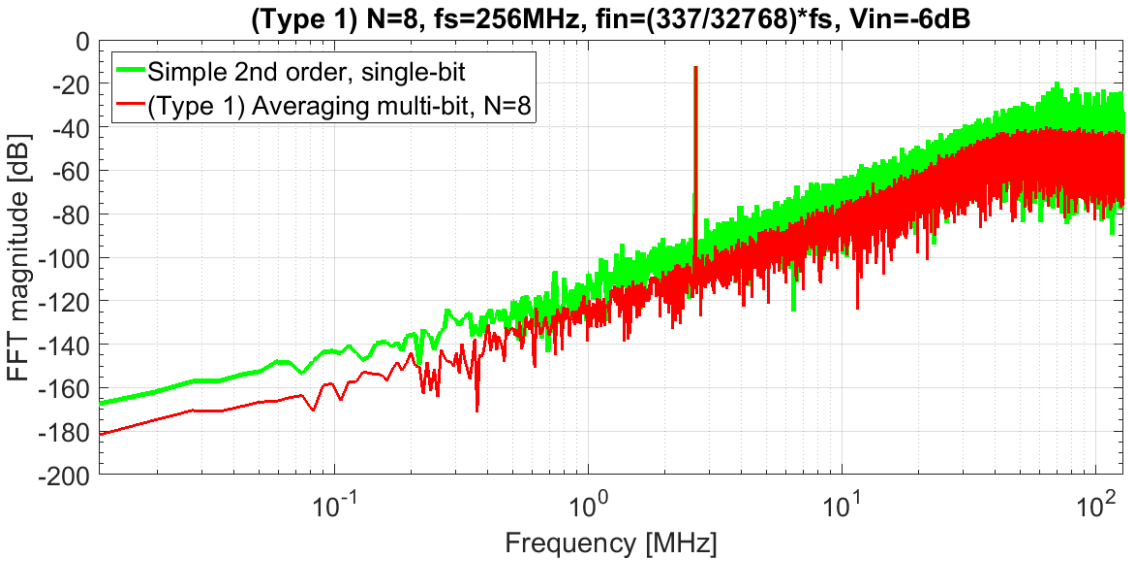

Figure 2.8: The spectrum of the second order averaging multi-bit sigma delta modulator with type 1 averaging multi-bit quantizer

of the filters Km forms a low pass filter. If αm, the DC gain of the filter Km, is close to one, the poles of the low pass filter are close to the origin in the s-domain, which makes the

sigma delta modulator more unstable. This means there is a trade off between the stability and SNDR with this type of averaging multi-bit quantizer. With smaller DC gains of the filters Km, stability improves, but the improvement in SNDR drops. When an averaging multi-bit quantizer affects the order of a sigma delta modulator, the influence has to be taken into consideration when the modulator is designed, and this type of quantizer may be difficult to handle and inconvenient. How to mitigate this disadvantage is the topic for the next subsection.

2.2.2 Type 2 Averaging Multi-bit Quantizer

In type 1 averaging multi-bit quantizer in Figure 2.5, both of the degree of integration and the amount of feedback are controlled by the filter Km. If the amount of the feedback is increased by making the DC gain of the filter Km larger, it also means the pole of the integrator goes to the low frequency direction, which results in the instability of the sigma delta modulator. This seems to be the cause of the trade-off between stability and SNDR, and one can come up with an idea: the parameters for integration and feedback can be separated. Figure 2.9 shows the diagram of type 2 averaging multi-bit quantizer in which the parameters for integration and feedback are separated. The parameters for integration and feedback are denoted as hm and km (m = 1, 2, . . ., N), respectively. Notice that the transfer function of the quantization stage of type 2 is no longer Z^{-1}. The feedback signal from the m-1^{st} single-bit quantizer and the input signal are processed by the m^{th} pre-filter, PFm, consisting of a delay and gain hm.

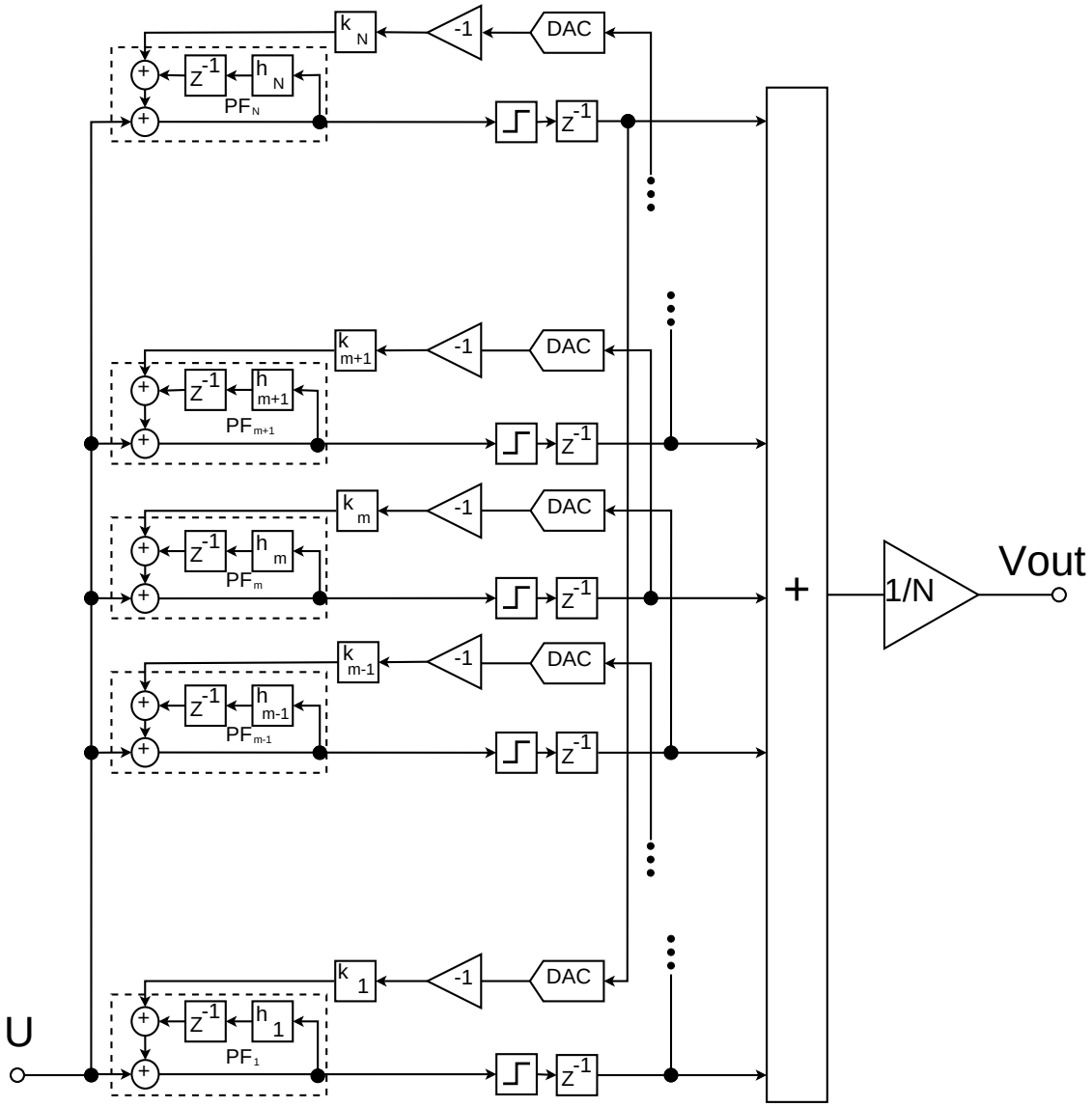

Figure 2.9: The block diagram of the quantization stage of type 2 averaging multi-bit quantizer. Reprinted from [1]

The performance of type 2 averaging multi-bit quantizer was evaluated by simulations when N was 16. The second order sigma delta modulator in Figure 2.1 was used as the test bench, and the quantization stage in Figure 2.1 was replaced with the one in Figure 2.9. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling

frequency. Figure 2.10 shows the SNDR when the coefficients km and hm are those in Table 2.1. The SNDR improves by fifteen when the single-bit quantizer is replaced by type 2 averaging multi-bit quantizer in Figure 2.9. With type 2 averaging multi-bit quantizer, the SNDR improvement at 0dB input is still 12dB, and the sigma delta modulator is as stable as the one with a single-bit quantizer in Figure 2.1. The FFT spectrum of the second order sigma delta modulator with type 2 averaging multi-bit quantizer is shown in Figure 2.11.

m	h_m	k_m
1	0.35	0.7696
2	0.35	0.9541
3	0.35	0.9953
4	0.35	0.8802
5	0.35	0.6451
6	0.35	0.3643
7	0.35	0.1262
8	0.35	0.0062
9	0.35	0.0419
10	0.35	0.2222
11	0.35	0.4902
12	0.35	0.7612
13	0.35	0.9499
14	0.35	0.9965
15	0.35	0.8865
16	0.35	0.6545

Table 2.1: Coefficients for type 2 averaging multi-bit quantizer

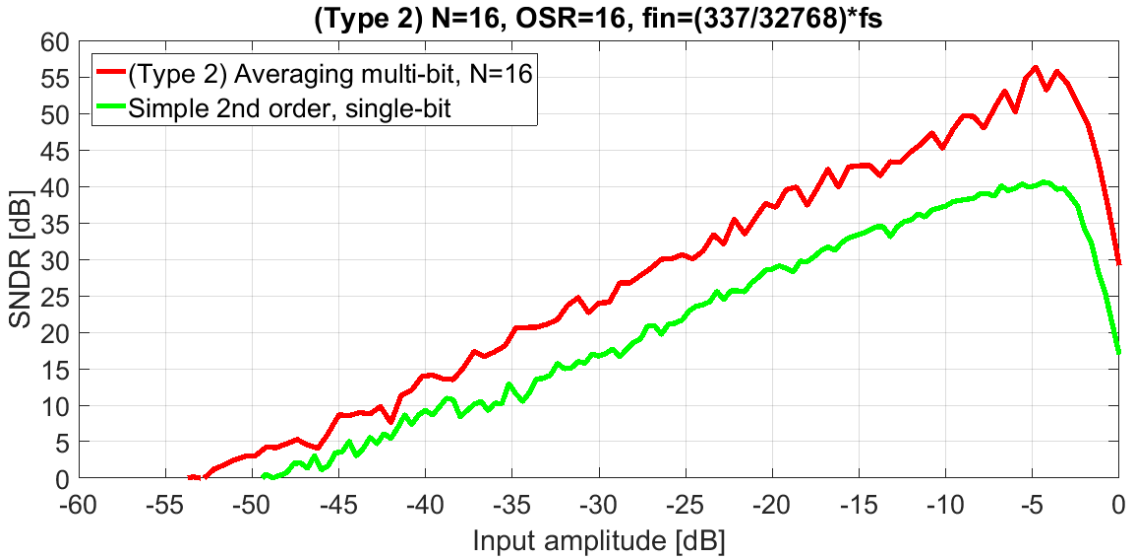

Figure 2.10: The SNDR of the second order averaging multi-bit sigma delta modulator with type 2 averaging multi-bit quantizer

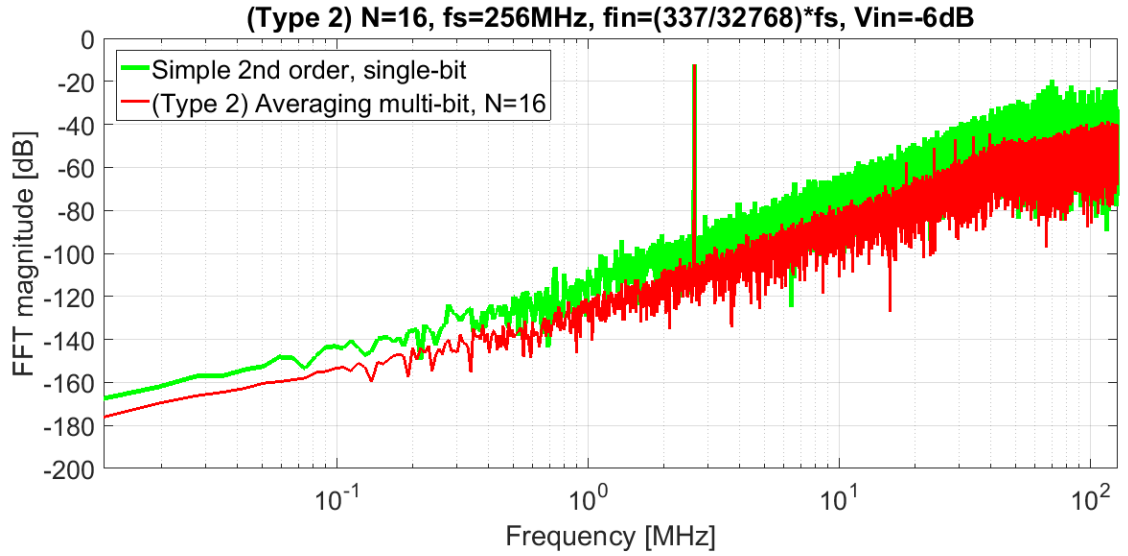

Figure 2.11: The spectrum of the second order averaging multi-bit sigma delta modulator with type 2 averaging multi-bit quantizer

3. DESIGN OF A SIGMA DELTA MODULATOR

In the previous chapter, it was demonstrated that it is possible to construct an averaging multi-bit quantizer without external signals such as dithering and reference signals. In this chapter, how to design a continuous time (CT) sigma delta modulator using an averaging multi-bit quantizer is explored. The CT version of the second order sigma delta modulator with an averaging multi-bit quantizer is discussed first. Then, an open-loop amplifier sigma delta modulator is examined. Because the purpose of this thesis is to present a design of an open-loop amplifier sigma delta modulator with an averaging multi-bit quantizer, it is not necessarily required to consider the CT version of the second order sigma delta modulator in Figure 2.1. The reason why the CT version of the second order sigma delta modulator is discussed here is showing that an averaging multi-bit quantizer can be realized without using active filters.

3.1 A Second Order Continuous Time Averaging Multi-bit Sigma Delta Modulator

The CT transfer function of the second order modulator in Figure 2.1 combined with type 2 averaging multi-bit quantizer in Figure 2.9 is easily obtained by the impulse-invariant transform. The result of the impulse-invariant transform is shown in Figure 3.1, where the coefficients am1 to am4 have the following expressions.

$$a_{m1} = 3\left[-\frac{2-3h_m}{(1-h_m)\ln(h_m)} + \frac{1}{2\ln(h_m)} + \frac{h_m(2h_m-1)}{(1-h_m)^2}\right] \tag{3.1}$$

$$a_{m2} = 3\left[-2 + \frac{2-3h_m}{1-h_m} - \frac{1}{\ln(h_m)}\right] \tag{3.2}$$

$$a_{m3} = 3 \tag{3.3}$$

$$a_{m4} = k_m \tag{3.4}$$

The transfer function Fm(s) has the following expression.

$$F_m(s) = \frac{-f_s \ln(h_m)}{(1-h_m)\left[s - f_s \ln(h_m)\right]} \tag{3.5}$$

where fs denotes the sampling frequency. The macro model of the second order sigma delta modulator is shown in Figure 3.2. Note that the transfer function Fm(s) is realized using only passive elements. $Z^{-t\ ELD}$ represents the excess loop delay (ELD), and its amount is the 20% of one sampling period. Two opamps are modeled as ideal one, which means the band width is infinity and the DC gain is sufficiently high, 60dB. No non-ideality is taken into consideration. The values of the components in the macro model are summarized in Table 3.1. These components are determined for the sampling frequency of 256MHz. The simulation result with the macro model is shown in Figure 3.3. The simulation tool is SIMULINK. The SNDR matches that of the discrete time (DT) model which was already shown in Figure 2.10.

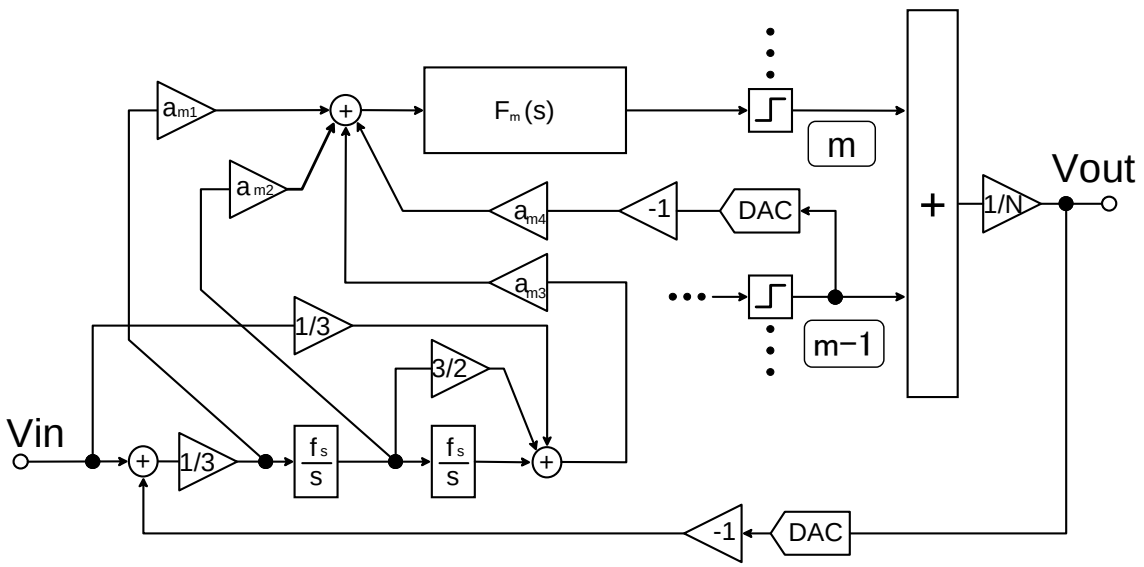

Figure 3.1: The block diagram of the CT version of the second order sigma delta modulator with type 2 averaging multi-bit quantizer. Reprinted from [1]

The second order sigma delta modulator with an averaging multi-bit quantizer may work well at a low sampling frequency, but it is not the goal for this thesis. It still needs closed-loop amplifiers. In the next section, an open-loop amplifier architecture is going to be explored.

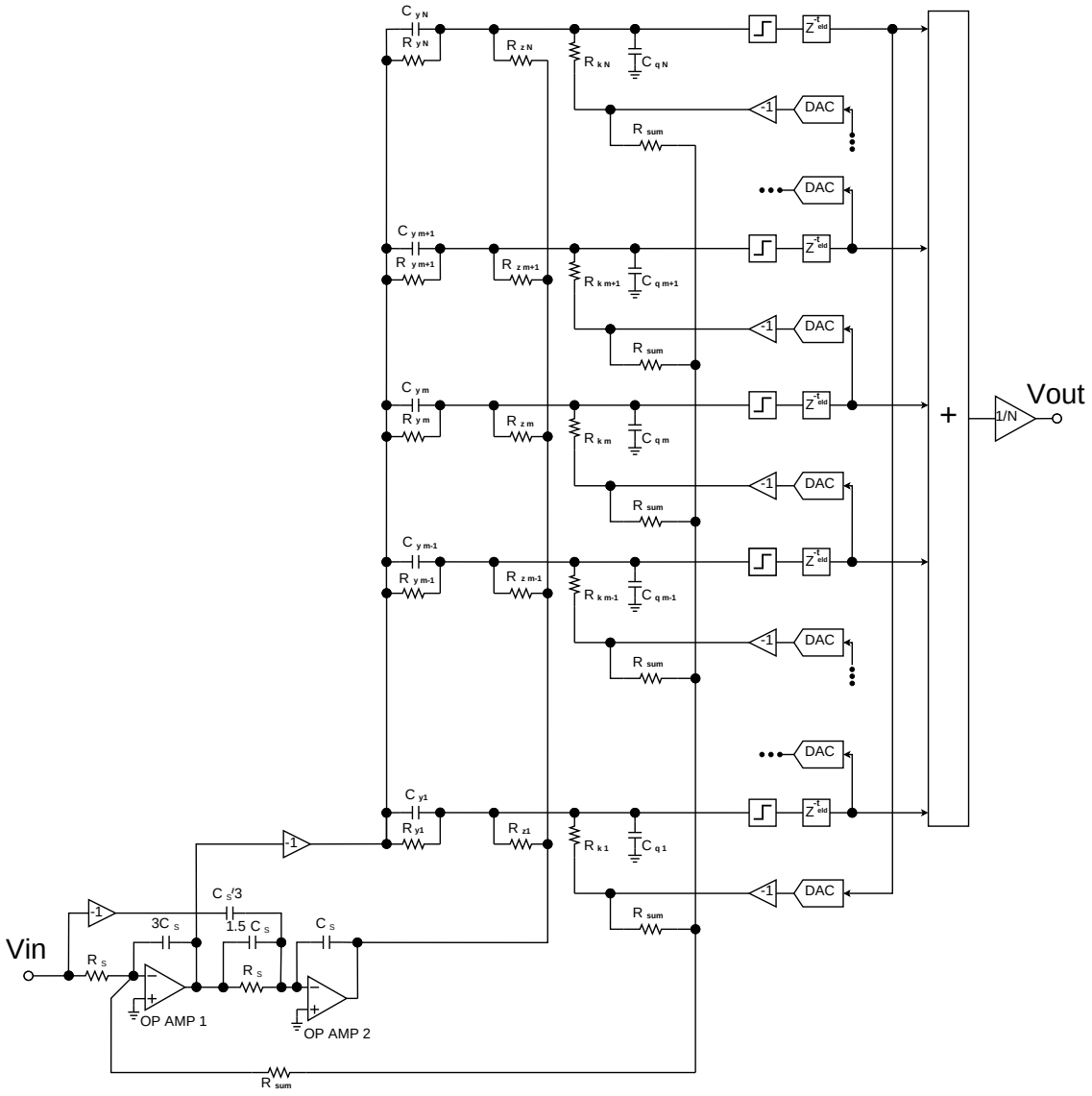

Figure 3.2: The macro model for the CT version of the second order sigma delta modulator with type 2 averaging multi-bit quantizer. Reprinted from [1]

m	Cy (pF)	Cq (pF)	Rk (kΩ)	Rz (kΩ)	Ry (kΩ)
1	0.361	0.500	28.1	7.22	17.4
2	0.340	0.500	24.1	7.68	18.5
3	0.335	0.500	23.4	7.78	18.8
4	0.348	0.500	25.5	7.49	18.1
5	0.377	0.500	32.1	6.91	16.7
6	0.420	0.500	51.2	6.21	15.0
7	0.464	0.500	133.6	5.62	13.6
8	0.490	0.500	2594.9	5.32	12.9
9	0.482	0.500	387.5	5.41	13.1
10	0.445	0.500	79.1	5.86	14.2
11	0.400	0.500	39.9	6.53	15.8
12	0.362	0.500	28.4	7.20	17.4
13	0.340	0.500	24.2	7.67	18.5
14	0.335	0.500	23.4	7.78	18.8
15	0.347	0.500	25.4	7.51	18.1
16	0.376	0.500	31.8	6.93	16.7

Rs (kΩ)	Rsum (kΩ)	Cs (pF)
7.813	7.353	0.5

Rsum = Rs·N/(N+1)

Table 3.1: The values of components used in the macro model of the second order sigma delta modulator with type 2 averaged multi-bit quantizer

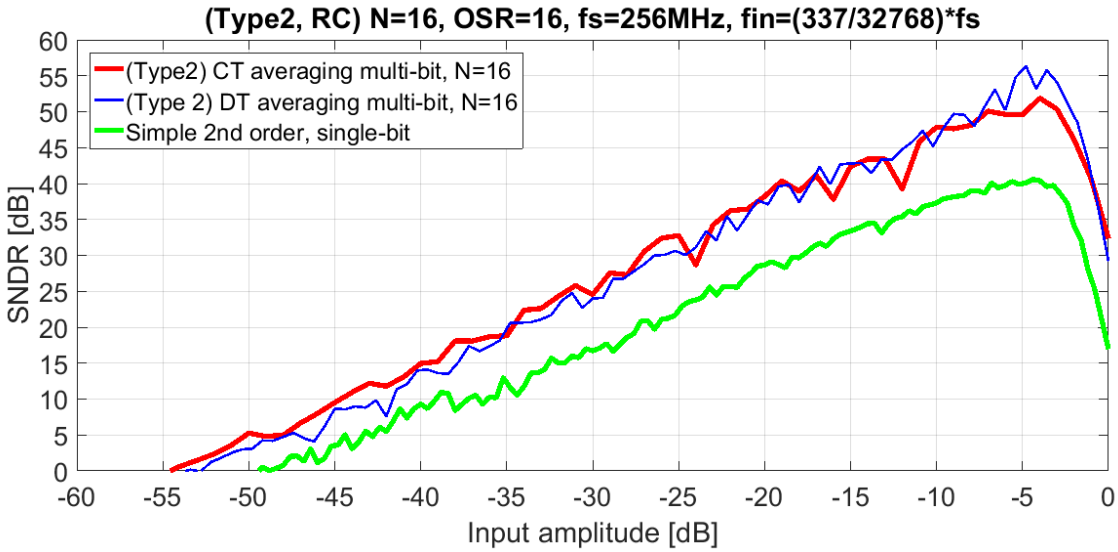

Figure 3.3: The SNDR of the CT version of the second order sigma delta modulator with type 2 averaging multi-bit quantizer. Reprinted from [1]

3.2 An Open-loop Amplifier Multi-bit Sigma Delta Modulator

3.2.1 The Basic Architecture of Averaging Multi-bit Sigma Delta Modulator

Figure 3.4 shows a conceptual diagram of a sigma delta modulator with type 2 averaging multi-bit quantizer. The modulator has N single-bit quantizers and N single-bit DACs, and the outputs of the DACs are averaged and fed back. The loop-filter (LF) shapes the quantization noise. In the averaging multi-bit quantizer, the output of the m^{th} DAC (m = 1, 2,. . ., N) is locally fed back to the $m+1^{st}$ single-bit quantizer via a pre-filter (PF), and the pre-filter is provided to make the quantization noises uncorrelated from one another. The forms of the pre-filters and values of the feedback coefficient, km, are chosen by simulations so that the quantized signals are sufficiently uncorrelated and the distortion is suppressed as much as possible. The process of producing the feedback signal by averaging the output signals from the single-bit quantizers is done in the analog domain. One delay of the sampling period is explicitly shown after each single-bit quantizer to take care of the response time of the single-bit quantizers. Comparators are usually used as single-bit quantizers, and the sampling and regeneration time of a comparator varies depending on the input signal; it responds fast when the input voltage large and slowly when the input voltage is small. Simulations tell that the amplitudes of signals at the inputs of the single-bit quantizers are different from branch to branch and that it takes a while all of the single-bit quantizers to finish their quantization process. Thus, in order to average the signals sampled at the same timing, it will be necessary to provide a reasonable time for the single bit quantizers to finish the judgment process. This is why it is waited for one sampling period before the average is calculated.

3.2.2 The Architecture of an Open-loop Amplifier Multi-bit Sigma Delta Modulator

There are restrictions on designing a loop filter when closed-loop amplifiers are not allowed in the loop filter. Firstly, lossy integrators are available, but integrators whose poles

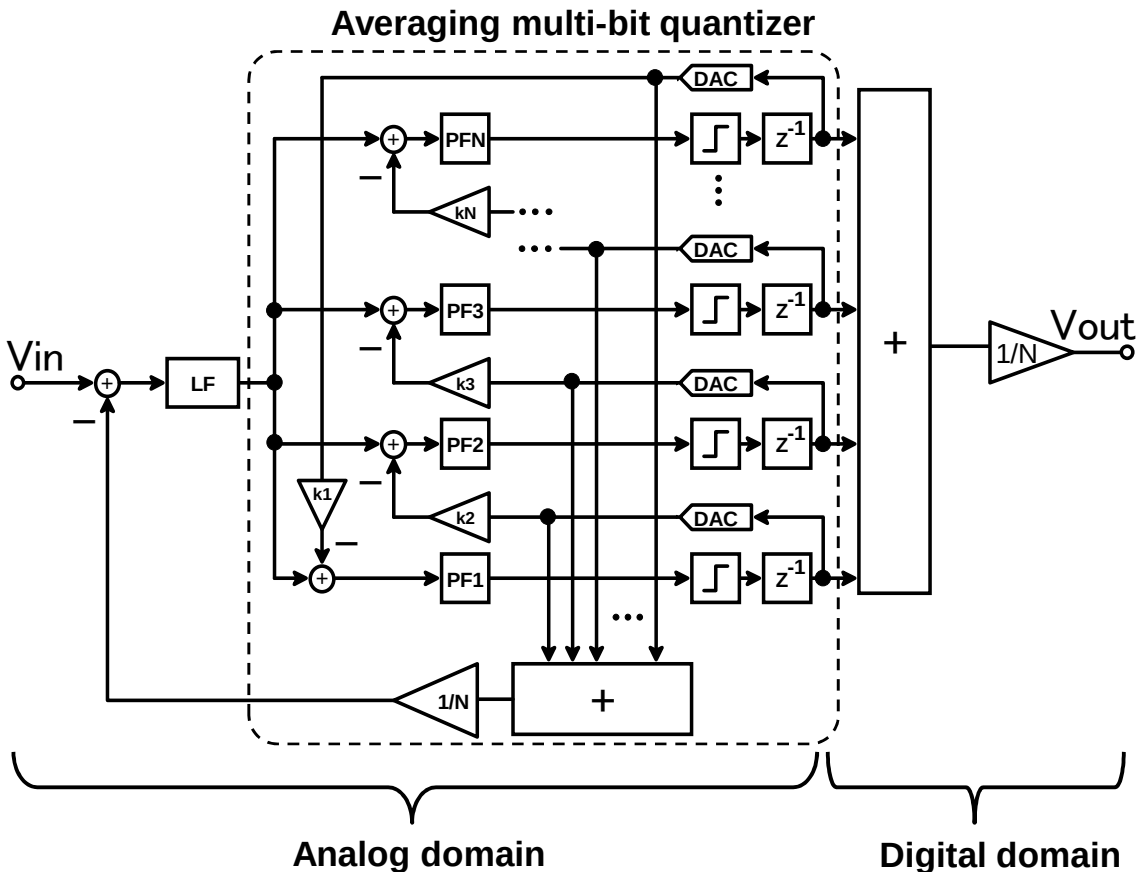

Figure 3.4: The conceptual diagram illustrating a sigma delta modulator with type 2 averaging multi-bit quantizer

are really close to the origin in the s-domain are not available. Secondly, the summation of the signals at the output nodes of the integrators is hard to be executed with precision. Precise summation of signals is possible with either a passive or active adder. Active adders are not a choice for an open-loop amplifier architecture. On the other hand, passive adders are difficult to handle because of the loading. Consequently, a desirable transfer function in this case is the one in which no summation of signals is required inside the loop filter. Considering these restrictions, passive RC filters in [7] are chosen to use for the loop filter, and Figure 3.5 shows the transfer function selected for this study, a fourth order sigma delta modulator.

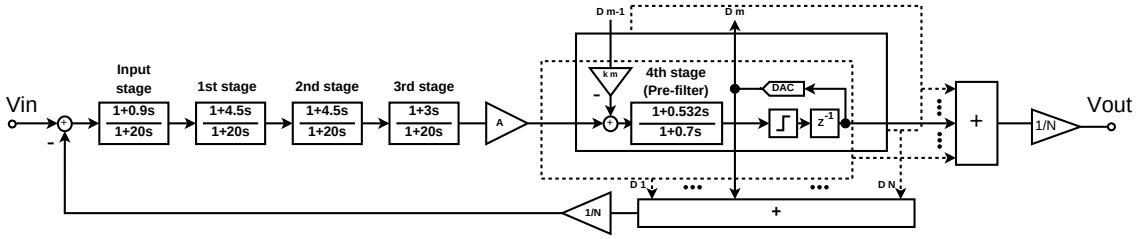

Figure 3.5: The transfer function of the open-loop amplifier multi-bit sigma delta modulator

The fourth stage of the transfer function corresponds to the pre-filters of type 2 averaging multi-bit quantizer in Figure 3.4, but a summation of signals is required at the input of the fourth stage, which is not preferable as explained before. It has been shown that it is possible to make a summation of signals at the input of a comparator [8], and it can be applied to the initially designed transfer function in Figure 3.5. Figure 3.6 shows the modified transfer function of the open-loop amplifier sigma delta modulator in Figure 3.5. The filter of the fourth stage in Figure 3.5 is separated into two: one is incorporated into the modified loop filter as the new third stage, and the other is put at the output of a local DAC. Note that the blocks of the original third and fourth stages are exchanged in the modified transfer function, and the block which includes a pole of a lower frequency than the other is located just before the single-bit quantizers. This exchange is made considering the large parasitic capacitance associated with the node connected to a number of comparators as the single-bit quantizers. A large parasitic capacitance makes it difficult to create a high frequency pole. Another modification is that the transfer function of the new third stage is slightly changed from the original fourth stage to adapt to the change of the point of summation. As a result, the modified loop filter consists of consecutive five stages. Each of the stages of the loop filter is a lead-lag filter which provides a zero to stabilize the modulator. It should be noted that part of the feedback signal is directly comes into the single-bit quantizers, and the excess loop delay of one sampling period is

compensated by this direct path. The pre-filter has the same form for all branches, and the coefficients Km (m = 1, 2. . ., N=16) in this modulator are given in Table 3.2. Dm (m = 1, 2,. . ., N=16) denotes the output signal from the m^{th} single-bit quantizer.

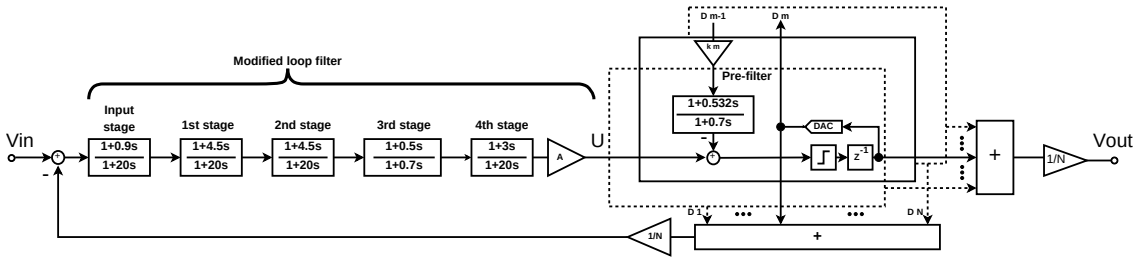

Figure 3.6: The modified transfer function of the open-loop amplifier multi-bit sigma delta modulator

m	km
1	0.7939
2	0.9755
3	0.9755
4	0.7939
5	0.5000
6	0.2061
7	0.0245
8	0.0245
9	0.2061
10	0.5000
11	0.7939
12	0.9755
13	0.9755
14	0.7939
15	0.5000
16	0.2061

Table 3.2: The coefficients for the local feedback of the open-loop amplifier averaging multi-bit sigma delta modulator

The gain of the loop filter, which is denoted as A, can be determined by simulations and is 3,000 when the high value of Dm is +1 and the low value is -1 in the single-ended mode or, in other words, when the full scale of the system is one. The value of A is important because whether multi-bit quantization works or not strongly depends on it. The basic idea of an averaging multi-bit quantizer is that a signal coming out of the loop filter is mixed with a signal that is locally fed back from one of the single-bit quantizers. If the gain of the loop filter is too large, the signal coming from the loop filter is much larger than the local feedback signals and affected little by those local feedback signals. This means that N of the quantization noises are strongly correlated with one another because every signal-bit quantizer quantizes substantially the same signal, and sufficient multi-bit quantization cannot be obtained. On the other side, if the gain of loop filter is too small, the local feedback signals becomes dominant and turn into the source of noises and distortion, which makes SNDR worse. The ratio of the local feedback signals to the gain of the loop filter is of importance. The gain of the loop filter is allowed to vary, but the intensity of the local feedback signals have to be adjusted so that the ratio keeps unchanged. The gain of loop filter can be much smaller than 3,000, in practice, because the loop filter does not need to provide all of the loop gain needed. Part of the loop gain is provided by the single-bit quantizers [4].

The ideal model in Figure 3.6 was simulated with SIMULINK, and Figure 3.7 shows the simulated SNDR. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling frequency. The broken line in the figure is the SNDR when the number of single-bit quantizer is one instead of sixteen. SNDR improves by 20dB by replacing the single-bit quantizer with the averaging multi-bit quantizer.

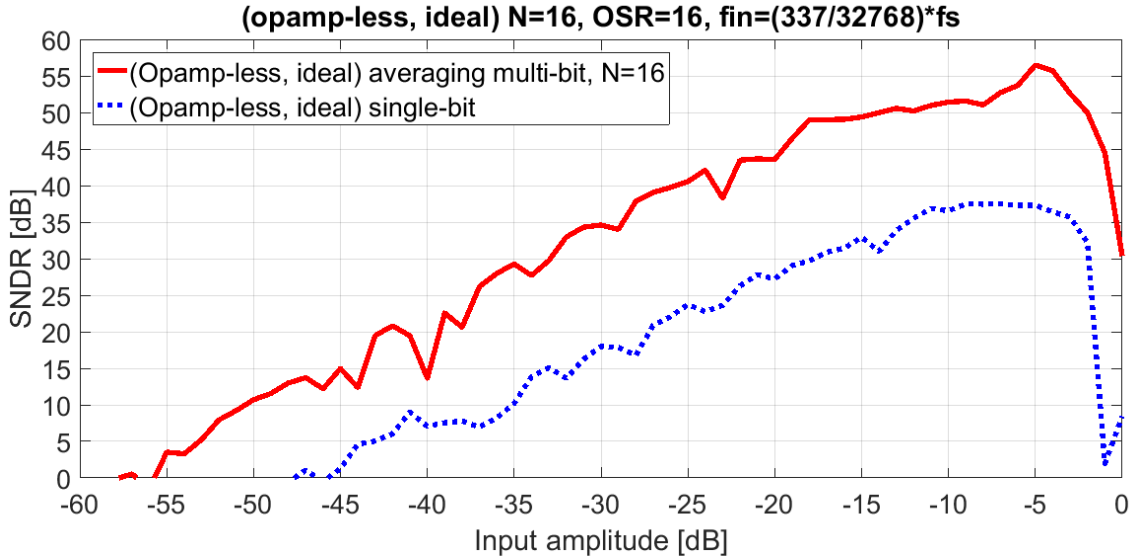

Figure 3.7: The SNDR of the ideal model of the open-loop amplifier multi-bit sigma delta modulator

3.2.3 Gain Distribution

The loop filter should provide gain to some extent. There are at least two reasons: to suppress the effects of the mismatches in comparators used as single-bit quantizers and to reduce the effects of noises. A sigma delta modulator forms a unity gain buffer with feedback, thus the difference between an input signal and the feedback signal is amplified with a large loop gain to recover the input signal. All of the loop gain could be provided by the single-bit quantizers in the case of an averaging multi-bit sigma delta modulator, but the signals at the inputs of the single-bit quantizers will be very small, smaller than 1mV, if the single-bit quantizers are the only sources of gain. The signals inside the modulator will be very small not only at the input of the signal-bit quantizers but also at every stage of the loop filter. These small signals are vulnerable to noises produced by elements such as transistors and resistors. Too small signals are also vulnerable to mismatches in the comparators as the single-bit quantizers.

In order to see the levels of signals at the stages of the loop filter, gains were distributed to each stage, and signals were monitored when the frequency of the input sinusoidal was 337/32768 times the sampling frequency and the amplitude was -6dB. The gains are distributed as shown in Figure 3.8. A1, A2, A3, and A4 are the gain for the first, second, third, and fourth stages, respectively. The product of A1, A2, A3, A4, and Acomp is equal to A, which is 3,000 in this case. Figure 3.9 shows the time transients of the signals when A1 = A2 = A3 = A4 = 1 and Acomp = 3,000. The signal levels are scaled by the full scale (FS) of the system. When the amplitude of a signal is 40mV/FS in the plot and the FS is 1V, the real signal level is 40mV. If the amplitude of a signal is 40mV/FS in the plot and the FS is 1.2V, the real signal level is 48mV. As shown in Figure 3.9, the signal level is as low as 0.4mV/FS at the output of the fourth stage. In order to increase the signal levels especially at the second to fourth stages, gains are distributed to the stages such that A1 = 4, A2 = 4, A3 = 1.25, A4 = 3, and Acomp = 50, and the simulation results are shown in Figure 3.10. The signal levels at the first to fourth stages are roughly equal and about 25mV/FS, which is 30mV when the FS is 1.2V. These gains A1 to A4 with which the signal levels at the stages become flat will be used to determine the intensity of the local feedback later in the design process, though some adjustment in gain distribution will be required too.

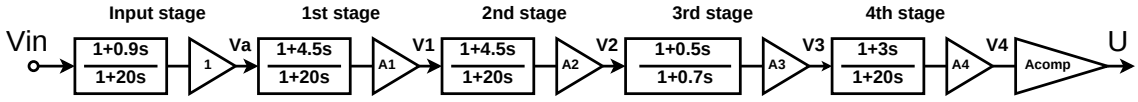

Figure 3.8: The diagram illustrating the distributed gains of the loop filter

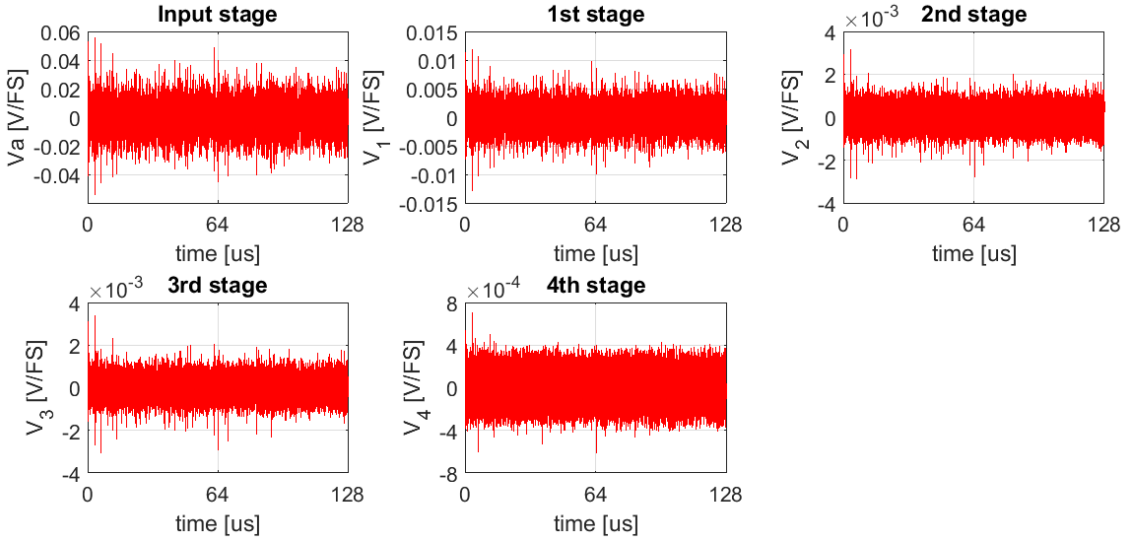

Figure 3.9: The time transient waveforms of the signals at the outputs of the stages of the loop filter when A1 = A2 = A3 = A4 = 1, and Acomp = 3,000

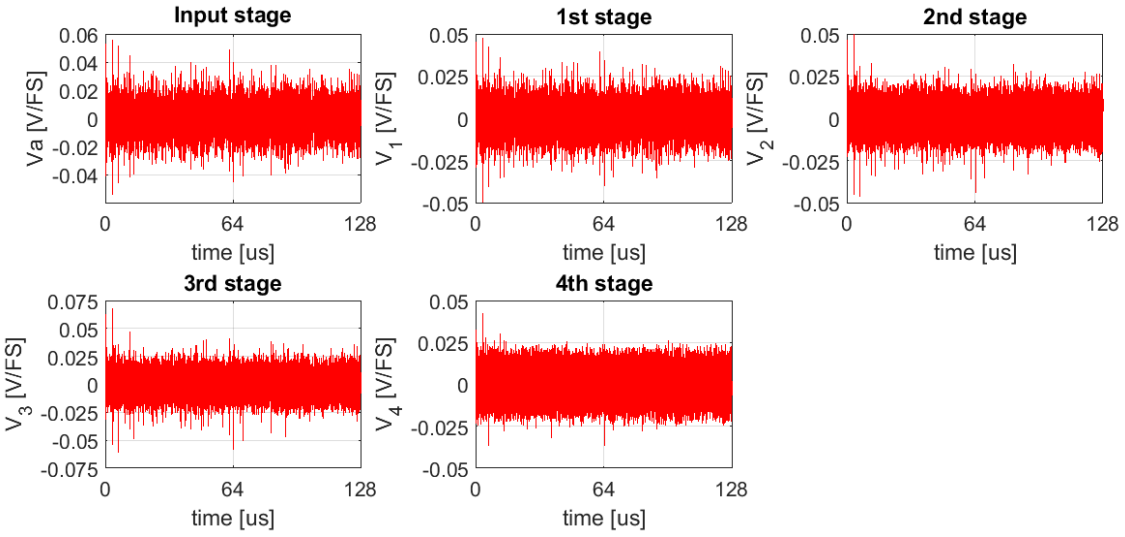

Figure 3.10: The time transient waveforms of the signals at the outputs of the stages of the loop filter when A1 = 4, A2 = 4, A3 = 1.25, A4 = 3, and Acomp = 50

3.2.4 Mismatch among DAC elements

One of the major issues associated with conventional multi-bit quantizers is the non-linearity which is cased by mismatches among the unit elements of DACs. A solution often used to overcome this problem of non-linearity is to choose these elements randomly at every quantization cycle. There are several methods available for applying this technique to a sigma delta modulator [9]. Although averaging multi-bit quantizers use multiple of single-bit quantizers as other conventional multi-bit quantizers do, the non-linearity caused by mismatches among the unit elements of DACs is not a problem for averaging multi-bit quantizers. This is simply because of the fact: the feedback signal is the summation of the outputs from multiple DACs in conventional multi-bit quantizers, but the feedback signal is the average of the output from multiple DACs in averaging multi-bit quantizers. In conventional multi-bit quantization, each of the outputs of the single-bit quantizers represents each of the different signal levels into which the input signal of the internal ADC is divided. With conventional multi-bit quantizers, if one of the outputs of the single-bit quantizers failed to be converted correctly to an analog signal, that failure cannot be made up for by the output signals from the other single-bit quantizers because they are different components. In contrast, each output signal from the single-bit quantizers of an averaging multi-bit quantizer covers the whole range of the input signal of the internal ADC, not a specific portion of the input signal. In other words, the outputs from the single-bit quantizers of an averaging multi-bit quantizer are independent interpretations of the same input signal of the internal ADC. When the digital-analog conversion is perturbed in a slight but random way because of the mismatches among elements, the analog signals which have been converted from the output signals of the single-bit quantizers of an averaging multi-bit quantizer will be also perturbed slightly and randomly. Thus, what is considered here is an average of multiple independent signals which are perturbed slightly and randomly.

In this situation, it is expected that the mismatches among the DAC elements produces random errors, and it will appear as a noise in the spectrum, not as distortion.

Figure 3.11 shows the spectra of the output signals with and without mismatches among the DAC elements. The spectra were analyzed with the mismatches of 0.5% and 1%. It can be seen that there is the third order distortion even when the DACs are ideal, but the distortion does not increase when mismatches are introduced to the DAC elements. The influence of the mismatch is seen as a rise in the noise floor.

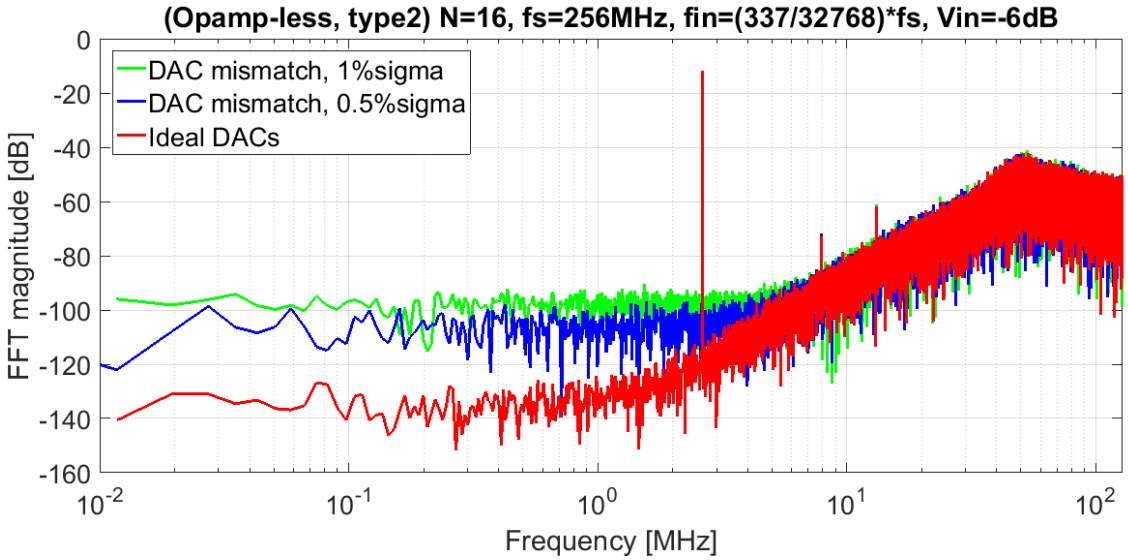

Figure 3.11: The spectra of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with mismatches among the DAC elements

The effects of 0.1% and 1% mismatches on the SNDR are shown in Figure 3.12 and Figure 3.13, respectively. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling frequency. The number of samples is ten in both cases of 0.1% and 1%, and the error bars indicate one sigma of the resultant SNDR distributions. The SNDR can vary by 2 to 3 dB because of the mismatches among DACs, but the

degradation in SNDR is not so large even with the 1% mismatch. Figure 3.14 shows the averaged SNDR for 0.1% and 1% mismatches in comparison.

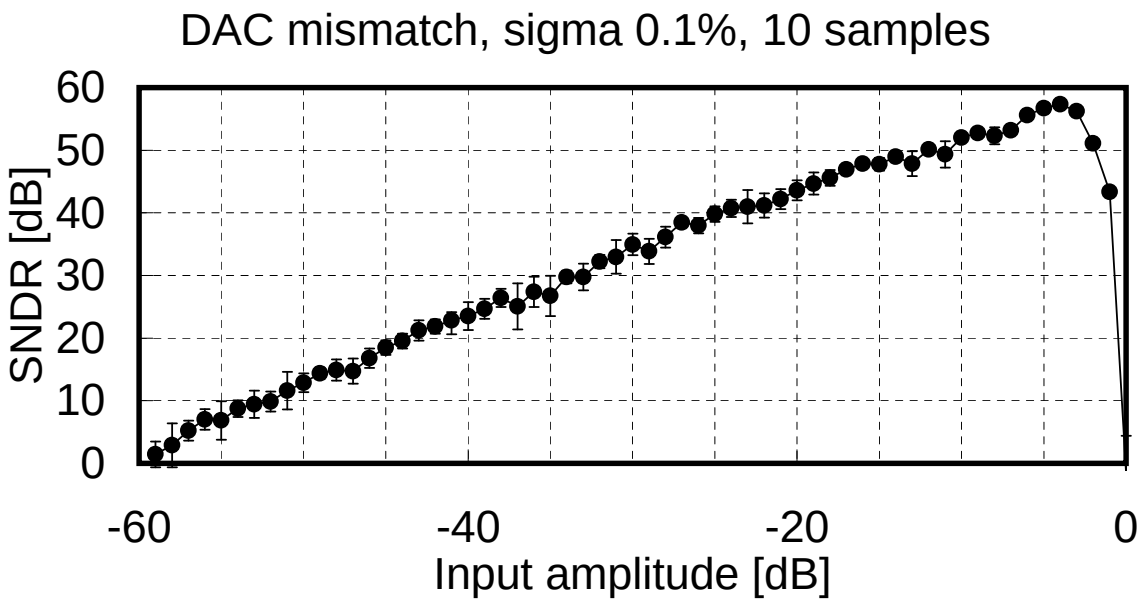

Figure 3.12: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatch of 0.1% among the DAC elements

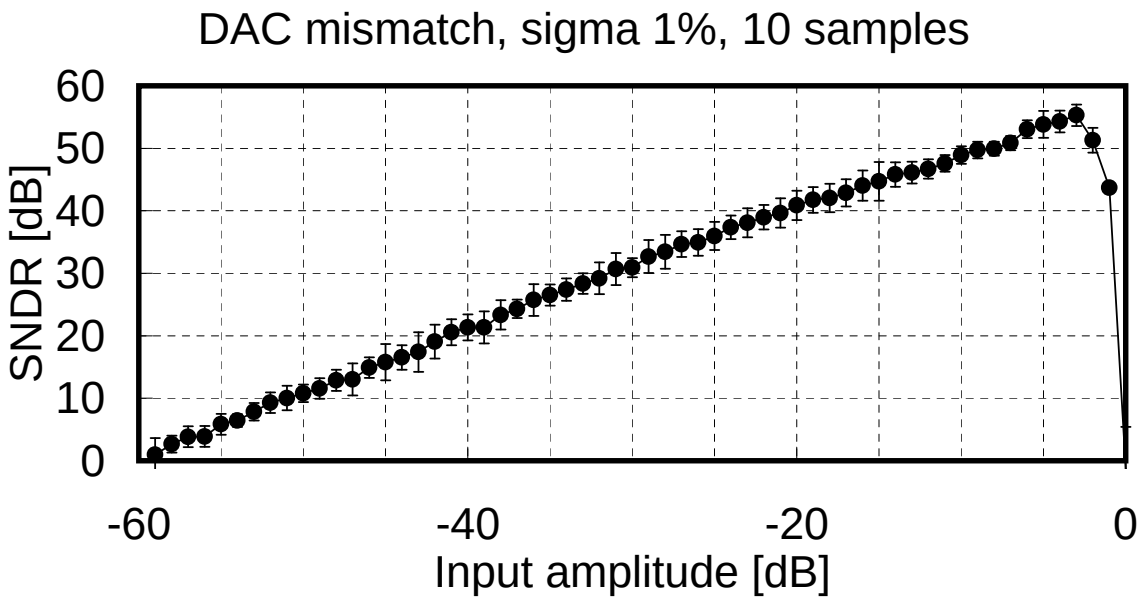

Figure 3.13: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatch of 1% among the DAC elements

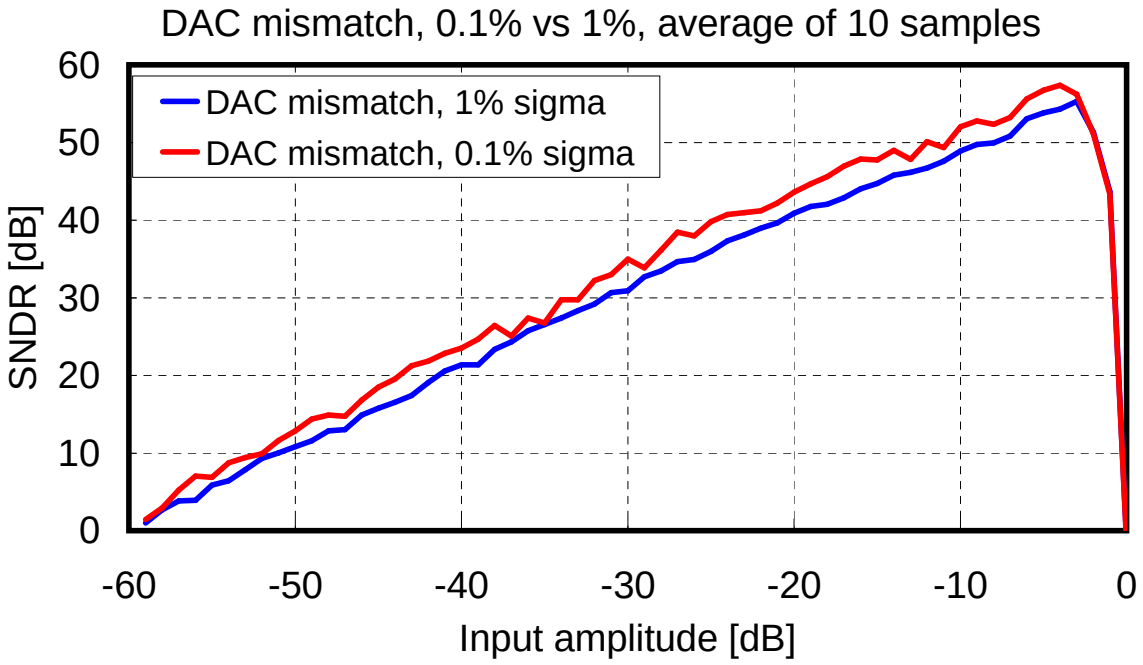

Figure 3.14: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatches of 0.1% and 1% among the DAC elements

3.2.5 Mismatch in Comparators as Single-bit Quantizers

Mismatches in comparators are usually not a problem for conventional multi-bit quantizers for a couple of reasons. Firstly, the bit number of a multi-bit quantizer is five at most, and the requirement for a mismatch is not so demanding. Secondly, the loop gain provided by a loop filter is high enough to shape the noise generated due to mismatches in comparators. In an open-loop amplifier sigma delta modulator with an averaging multi-bit quantizer, in contrast, mismatches in comparators can be a serious problem. As mentioned previously, part of the loop gain of an averaging multi-bit sigma delta modulator is provided by each of the single-bit quantizers when the gain of the loop filter is not high enough. In that case, the amplitude of the internal signal is much smaller than the full scale of the system that is normally defined by supply voltages. The range of the internal signals could be less than one percentage of the full scale. With such small signals at the inputs of the single-bit quantizers, which are a comparator in most cases, the chances of the comparators making wrong judgment on the signs of input signals are not ignorable.

The effect of mismatches in comparators can be evaluated by simulations where mismatches are modeled as a random shift added at the input of the comparators. The effects of 10% and 50% mismatches in comparators are shown in Figure 3.15 and Figure 3.16, respectively. The OSR is 16, and the frequency of the input sinusoidal is 337/32768 times the sampling frequency. Each percentage represents the ratio of the sigma of the Gaussian distribution for the shifts added at the inputs of the comparators to the full scale of the system. The full scale is one in this case. The number of samples is ten in both cases of 10% and 50%, and the error bars indicate one sigma of the resultant SNDR distributions. Figure 3.17 shows the averaged SNDR for 10% and 50% mismatches in comparison together with the plot of the SNDR with ideal comparators. These simulation results suggest that the mismatch of 10% can be tolerable.

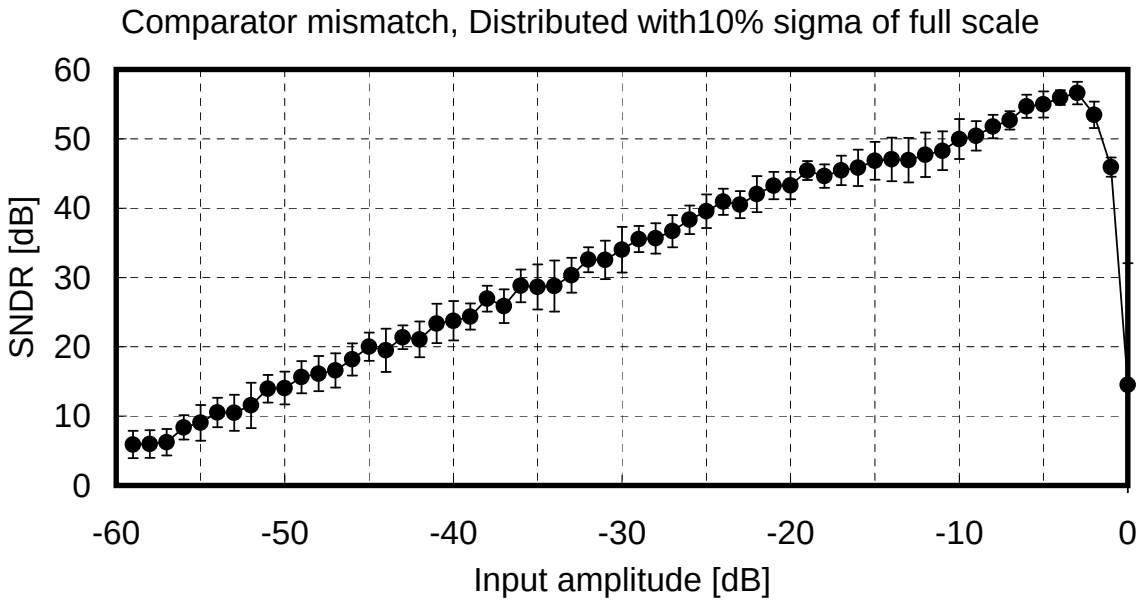

Figure 3.15: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatch of 10% with respect to the full scale of the system

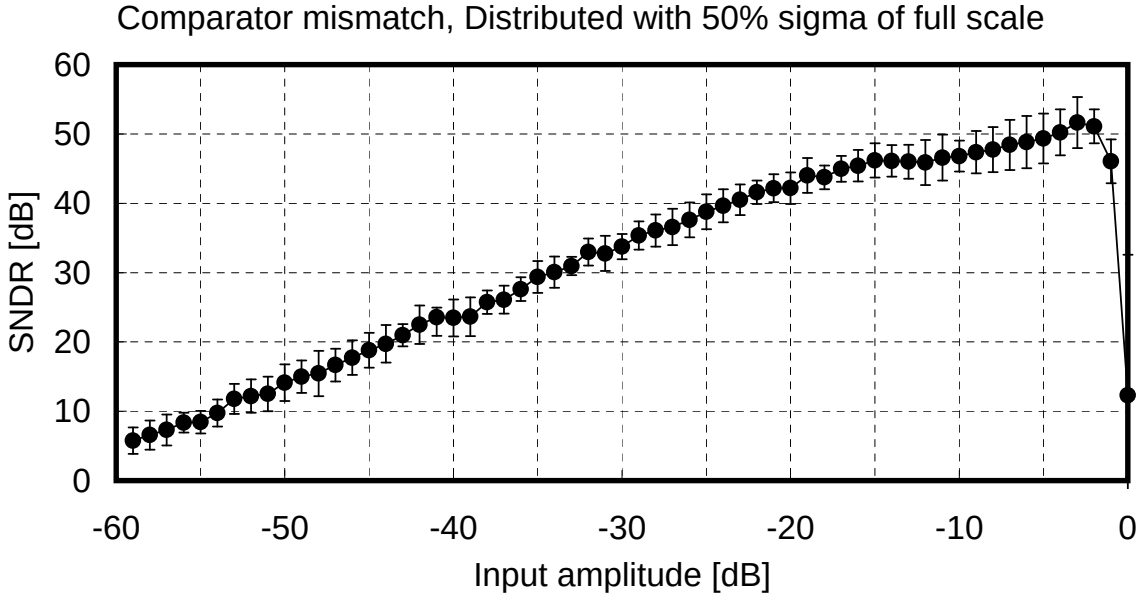

Figure 3.16: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatch of 50% with respect to the full scale of the system

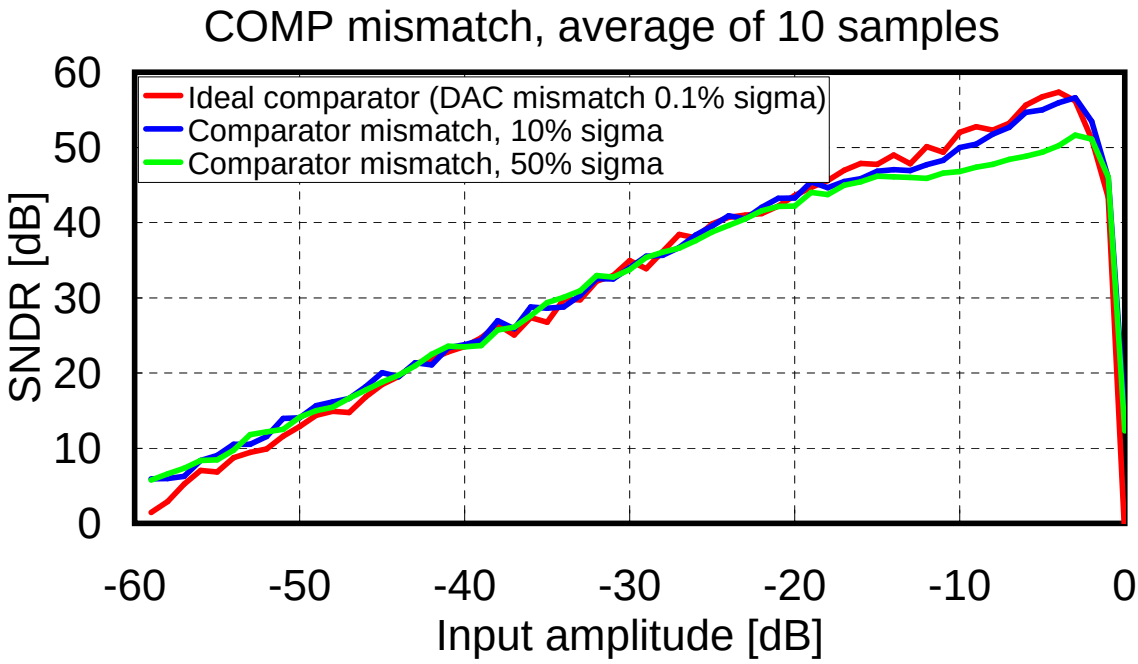

Figure 3.17: The averaged SNDR of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer with the mismatches of 10% and 50% with respect to the full scale of the system

The requirement for the mismatches in comparators can be estimated by assuming the gain of the loop filter. Given the gain of the loop filter is 50V/V, the full scale seems like scaled down by the factor of 50/3,000 at the input node of the comparators, where 3,000 is the total gain of the loop filter. Considering the full scale is 1.2V, the effective full scale at the input node of the comparators is 1.2V times 50/3,000, which turns out to be 20mV. Consequently, the tolerable mismatch in the comparators in this case is 2mV, the 10% of 20mV. In a more practical way, mismatches should be compared with the standard deviation of the signal at the input node of the averaging multi-bit quantizer. That node is denoted as U in Figure 3.6. When the amplitude of -6dB is selected for the input signal of the modulator and when the standard deviation of the signal at node U is simulated, it is 0.49, which is almost the expected value, 0.5. This value of standard deviation should be

compared to the sigma of the distribution of mismatches. If the sigma for mismatches is the 10% of the effective full scale, its percentage with respect to the standard deviation of the signal at node U is 20% (= 0.1/0.5). This criterion for tolerance to mismatches is much more practical in a design process. A modulator can be simulated without mismatches in comparators being taken into consideration, and the standard deviation at the input of the quantizer is evaluated. If the sigma of the distribution of mismatches in comparators is within 20% of the evaluated standard deviation, it can be said that the mismatch will be tolerable.

4. CIRCUIT DESIGN

All the building blocks are designed using model files of a 90nm CMOS process, and the supply voltage is 1.2V. Circuits are designed for the sampling frequency of 2.56GHz. The simulation tool is LTspice.

The open-loop amplifier multi-bit sigma delta modulator consists mainly of five blocks shown in Figure 4.1: the part of the digital domain, the units including comparators and latches, the part forming global feedback, the units of local feedback, and the loop filter including five stages of filters. The digital part calculates the average of the digital signals, Dm (m = 1, 2,. . ., 16), and it is not the subject of this thesis. The detail of the loop filter is discussed first, and then comparators, latches, and DACs will be explained later in this chapter.

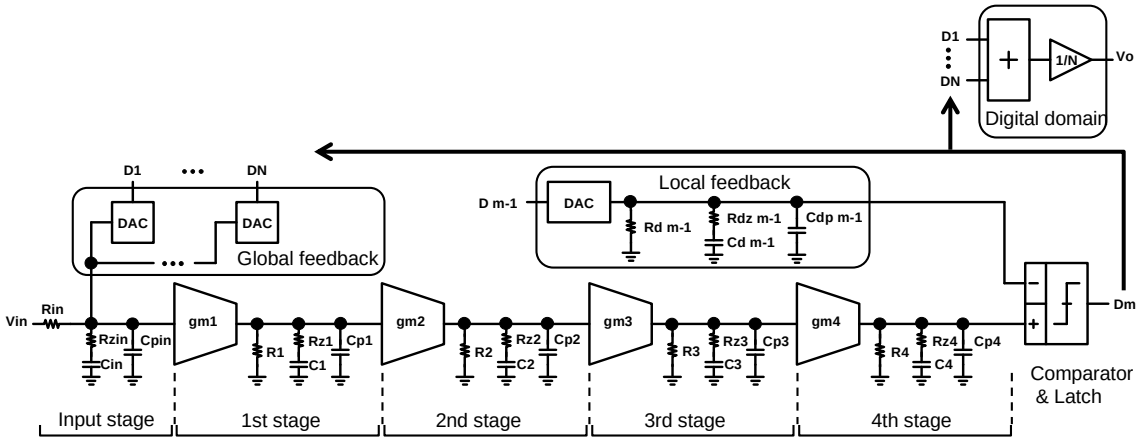

Figure 4.1: The macro model of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer described in single mode

Stage									
Input		1st		2nd		3rd		4th	
Rin	2.50 kΩ	R1	2.00 kΩ	R2	3.33 kΩ	R3 *	150 Ω	R4	1.00 kΩ
Rzin	132 Ω	Rz1	580 Ω	Rz2	967 Ω	Rz3	375 Ω	Rz4	176 Ω
Cin	2.97 pF	C1	3.03 pF	C2	1.82 pF	C3	521 fF	C4	6.64 pF
Cpin	90.0 fF	Cp1	90.0 fF	Cp2	60.0 fF	Cp3	60.0 fF	Cp4	250 fF

*R3 = R3_1||R3_2, R3_1: 1.00kΩ, R3_2: 177Ω

Table 4.1: The values of the resistance and capacitance in the loop filter

4.1 Loop Filter

The loop filter is divided into five stages: the input stage and the first to fourth stages. Each of the five stages includes a resistor, Rin or R1 to R4, defining a DC gain, a capacitor, Cin or C1 to C4, defining a pole, and a resistor, Rzin or Rz1 to Rz4, defining a zero. Each stage is accompanied with parasitic capacitance, Cpin or Cp1 to Cp4. The values of the components are in Table 4.1. At each of the first to fourth stages, a transconductance, gm1 to gm4, and the resistor, R1 to R4, produces a DC gain. These structures are formed using differential pairs 1 to 4, as shown in Figure 4.2. The technique of source degeneration using MOS transistors [10] is applied to the differential pairs for better linearity.

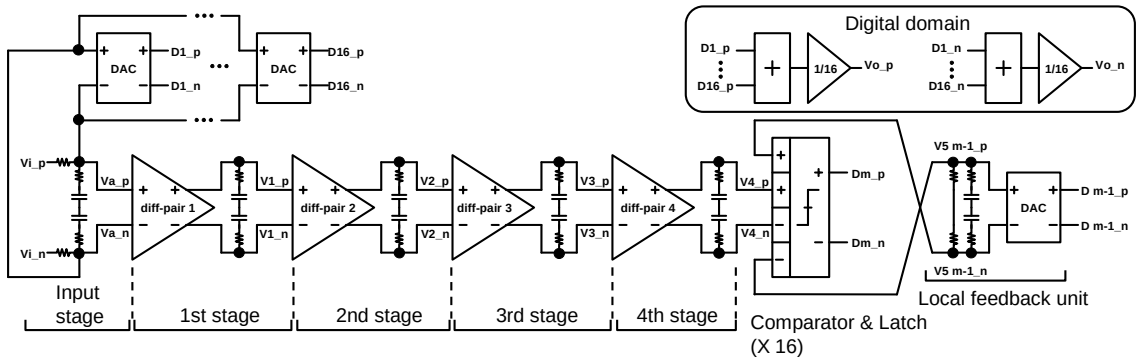

Figure 4.2: The macro model of the open-loop amplifier sigma delta modulator with type 2 averaging multi-bit quantizer described by using differential pairs 1 to 4

The frequency response of each stage was evaluated by simulations. Figure 4.3(a) shows the setting to see the frequency response of the input stage, and Figure 4.3(b) is the modeled version of the input stage where differential pair 1 in Figure 4.3(a) is replaced by the parasitic capacitance, Cpin. The frequency response of the input stage is shown in Figure 4.4 along with the result of the modeled version in Figure 4.3(b) denoted as (op-on)/(ip-in).

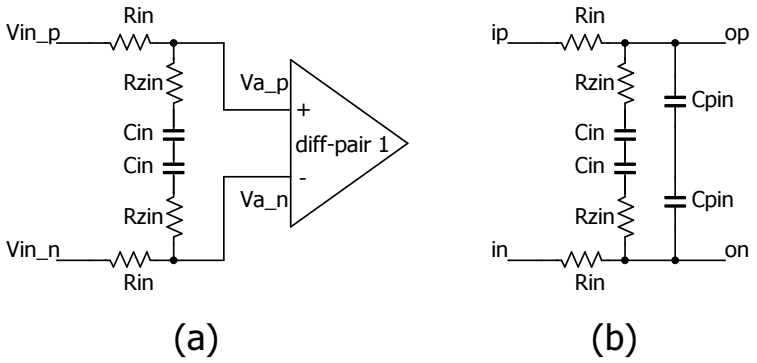

Figure 4.3: (a)The schematic of the input stage of the loop filter (b) The modeled version of the input stage of the loop filter

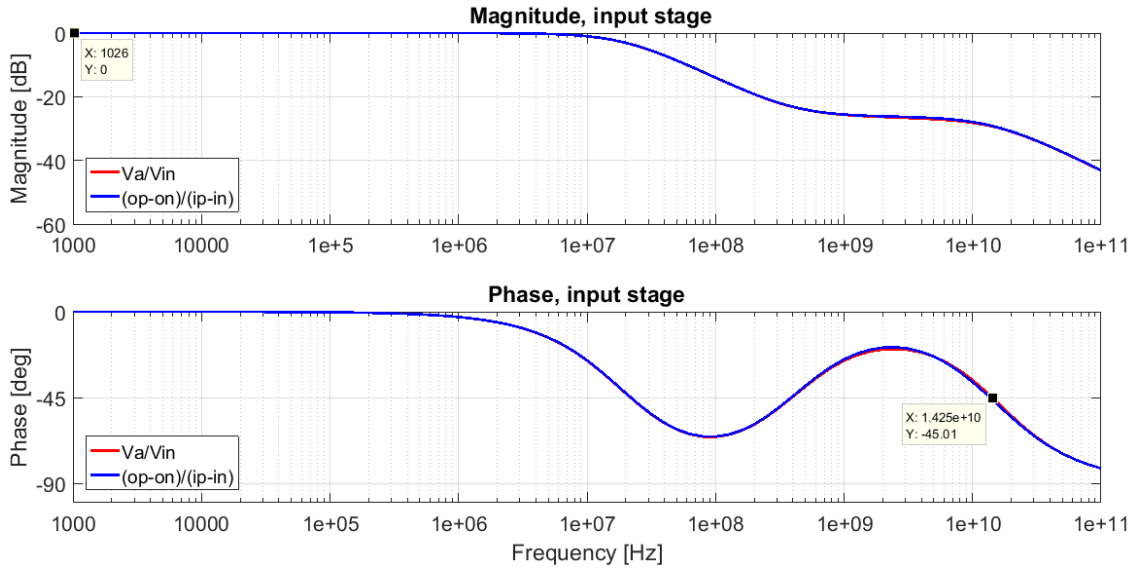

Figure 4.4: The frequency response of the input stage of the loop filter

Figure 4.5(a) shows differential pair 1 in the setting to see the frequency response of the first stage, and Figure 4.5(b) is the modeled version of the first stage. The frequency response of the first stage is shown in Figure 4.6 along with the result of the modeled version of the first stage.

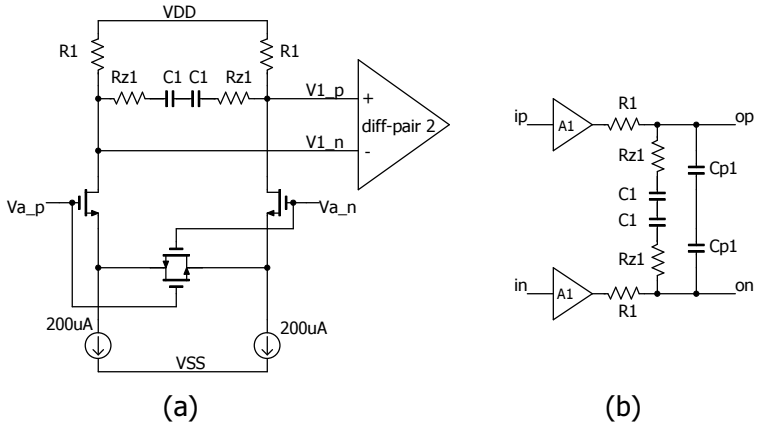

Figure 4.5: (a)The schematic of the first stage of the loop filter (b) The modeled version of the first stage of the loop filter

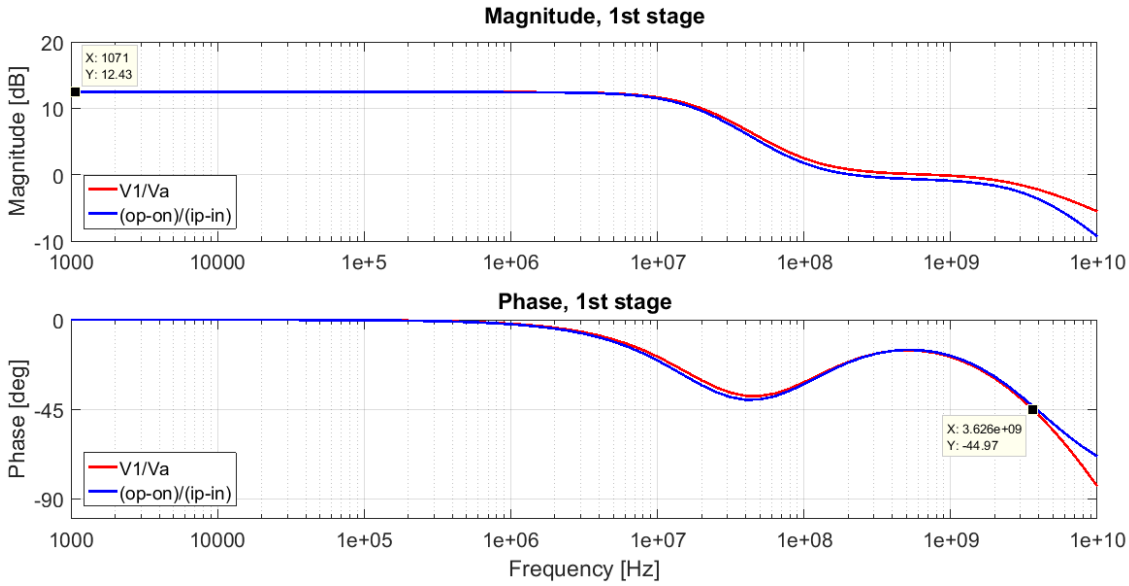

Figure 4.6: The frequency response of the first stage of the loop filter

Figure 4.7(a) shows differential pair 2 in the setting to see the frequency response of the second stage, and Figure 4.7(b) is the modeled version of the second stage. The frequency response of the second stage is shown in Figure 4.8 along with the result of the modeled version of the second stage.

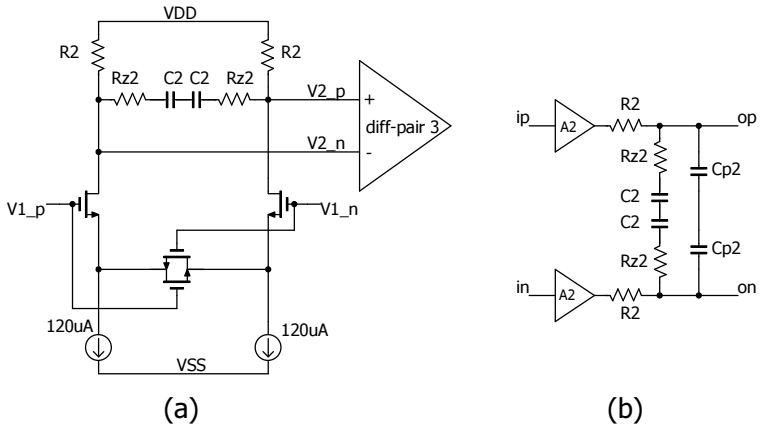

Figure 4.7: (a)The schematic of the second stage of the loop filter (b)The modeled version of the second stage of the loop filter

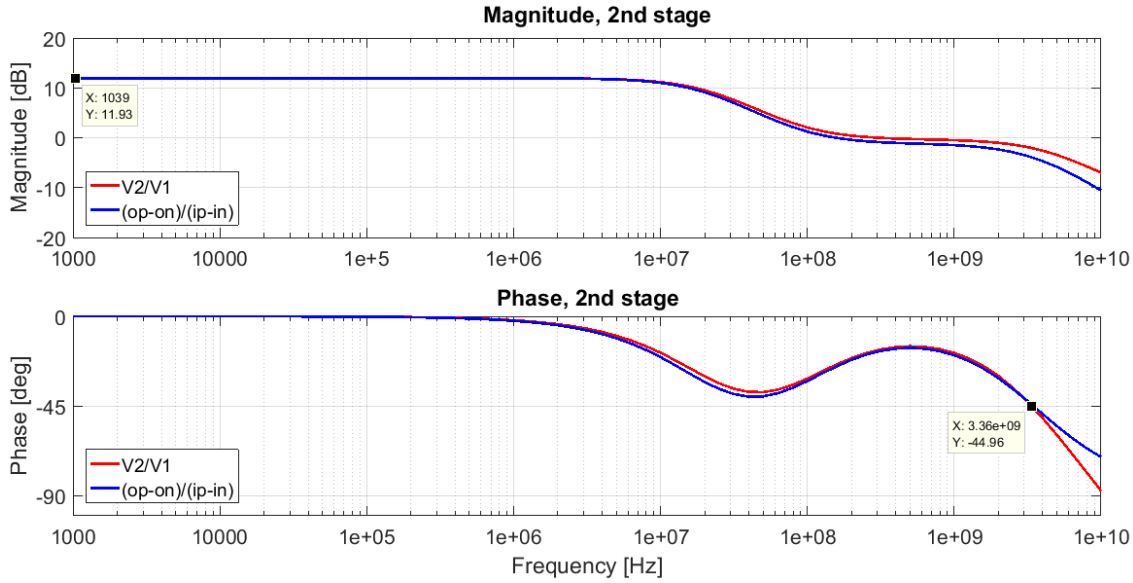

Figure 4.8: The frequency response of the second stage of the loop filter

Figure 4.9(a) shows differential pair 3 in the setting to see the frequency response of the third stage, and Figure 4.9(b) is the modeled version of the third stage. The frequency

response of the third stage is shown in Figure 4.10 along with the result of the modeled version of the third stage.

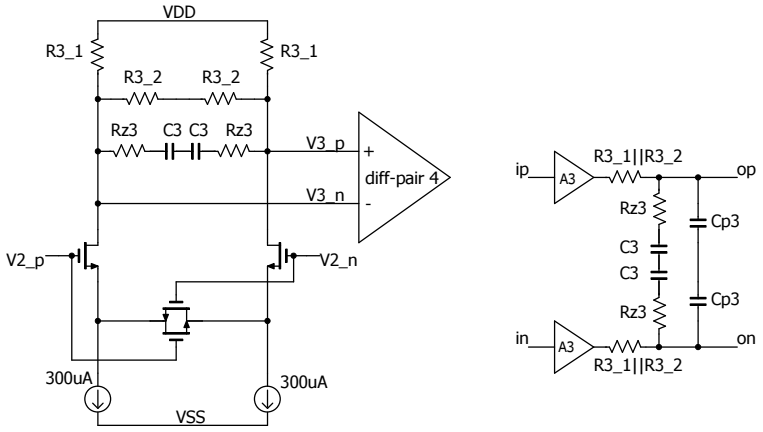

Figure 4.9: (a)The schematic of the third stage of the loop filter (b)The modeled version of the third stage of the loop filter

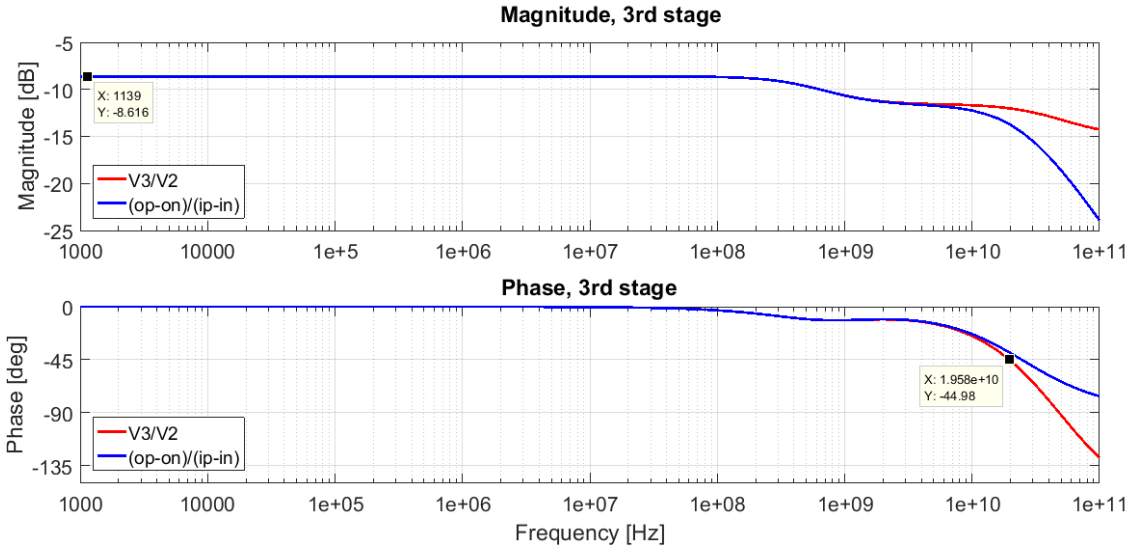

Figure 4.10: The frequency response of the third stage of the loop filter

Figure 4.11(a) shows differential pair 4 in the setting to see the frequency response of the fourth stage, and Figure 4.11(b) is the modeled version of the fourth stage. The frequency response of the fourth stage is shown in Figure 4.12 along with the result of the modeled version of the fourth stage.

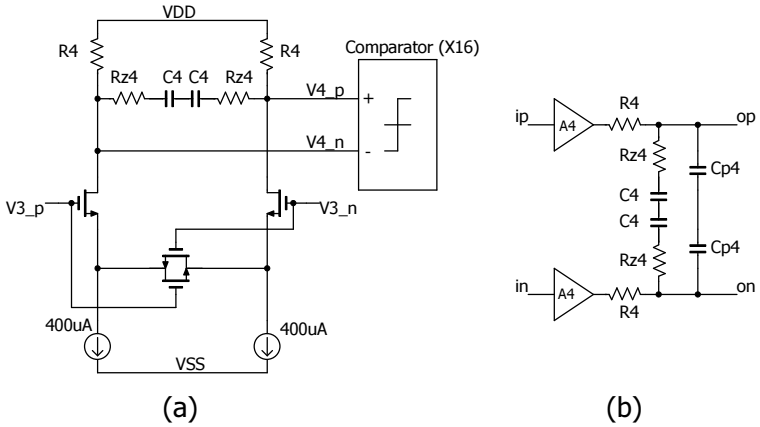

Figure 4.11: (a)The schematic of the fourth stage of the loop filter (b)The modeled version of the fourth stage of the loop filter

The performances of the differential pairs are summarized in Table 4.2. The parasitic capacitances are the most significant factor which can make the transfer function of the loop filter differ from the ideal one. The influences of the parasitic capacitances can be seen as the locations of the second poles in the frequency responses of the stages. The location of the second pole of a stage is defined as the point where the phase crosses -45 degree at a higher frequency than the zero of the stage. The further away the second pole locates from the sampling frequency, the smaller the effect of the parasitic capacitance will be. The frequencies of the second poles are at least as 1.3 times high as the sampling frequency. The THD is tested with an input signal whose frequency is 25.625MHz. This frequency is the one third of the target band width, which is 80MHz. The amplitude of the

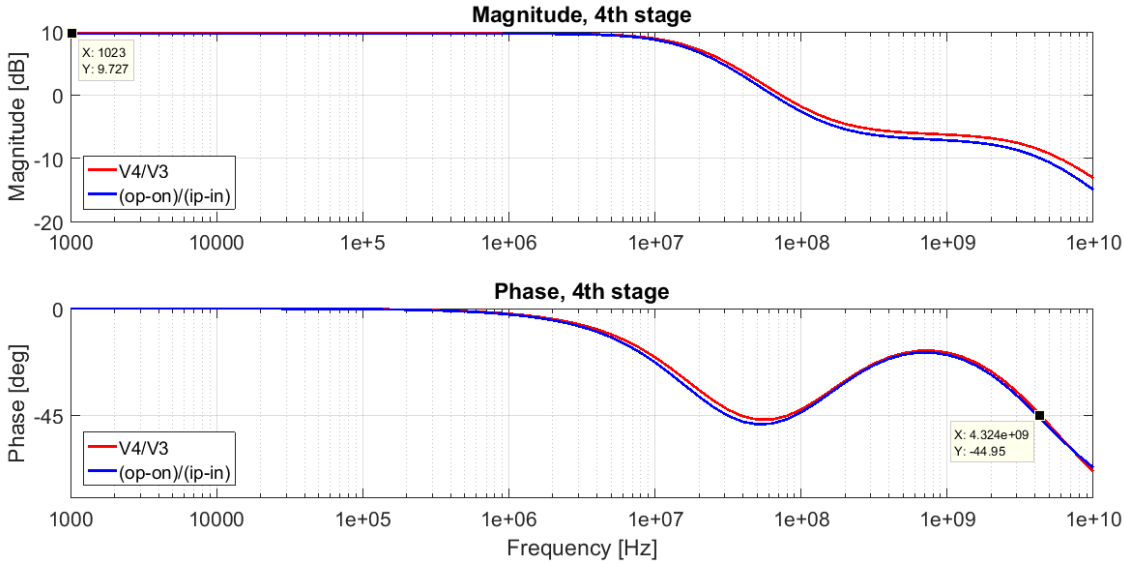

Figure 4.12: The frequency response of the fourth stage of the loop filter

input signal at which THD was measured is 60mVpp for differential pair 1 and 40mVpp for other differential pairs. It is assumed that the input amplitude does not exceed 60mV in differential mode at the input of the first stage and 40mV at the inputs of the second to fourth stages.

Differential pair	1	2	3	4
Gain [V/V]	4.2	4.0	0.4	3.1
Gain [dB]	12.5	12.0	-8.64	9.83
fc [GHz] (*1)	3.63	3.36	19.6	4.32
fc [/fs]	1.4	1.3	7.7	1.7
THD [dB] (*2)	-69	-68	-65	-64
Power [mW] (*3)	0.48	0.29	0.72	0.96

(*1) fc: frequency of the second pole
(*2) Vin: 25.625MHz, 60mVpp for the diff-pair 1, 40mVpp for the others
(*3) 1.2V supply voltage

Table 4.2: The performances of differential pairs 1 to 4

In order to see what changes occur when these differential pairs are incorporated in the loop filter, simulations were run to obtain SNDR and SNR when the designed differential pairs were used in the loop filter. As shown in Figure 4.13, the SNDR achieved with the designed differential pairs is lower than the ideal one at large input amplitudes, while SNR is close to the ideal case.

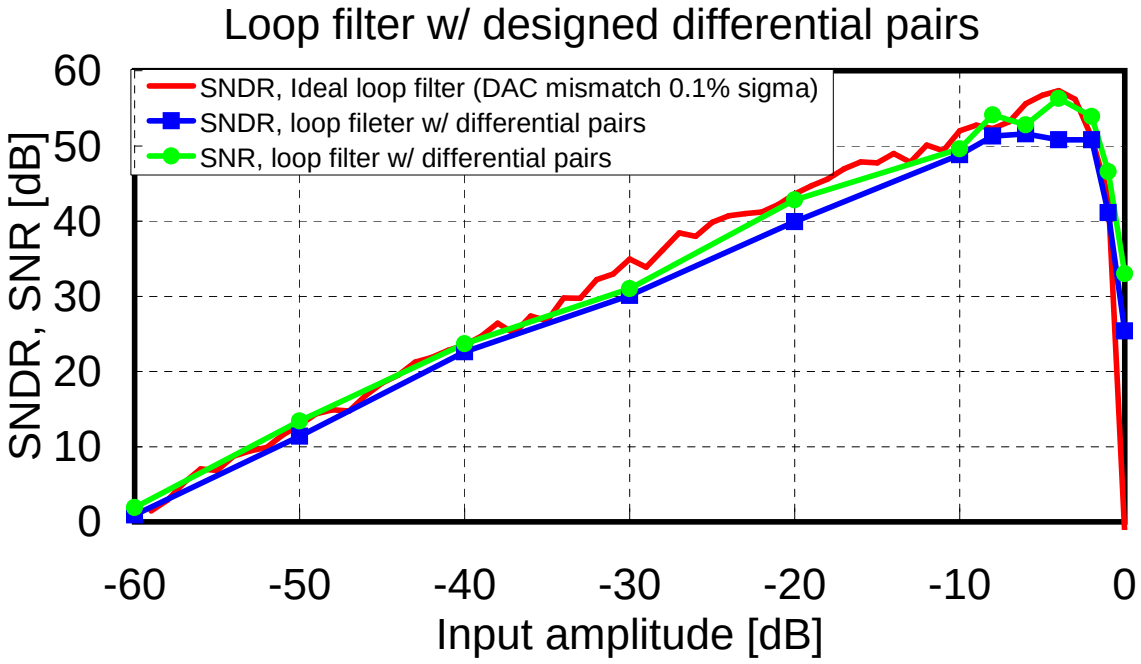

Figure 4.13: The SNDR and SNR of the open-loop amplifier multi-bit sigma delta modulator with the designed differential pairs used in the loop filter

4.2 Comparators and Latches

The unit of comparators and latches consists of two SA latches, two SR latches, and two 2-1 multiplexers as shown in Figure 4.14. One SA latch is triggered by the rising edge of the clock (CLK), and the other is trigged by the rising edge of the negative clock ($\overline{\text{CLK}}$). The output signals of the SA latches are hold by the SR latches. The latch in [11] is used for the SR latches for shorter response time. The output signals of the two SR latches are selected alternately by the multiplexers which are triggered by the rising edge of $\overline{\text{CLK}}$. The CLK frequency is one half of the sampling frequency, and thus the signals are sampled once every sampling period [12]. The output signals, Dm_p and Dm_n, are a high or low value representing the sign of the signal at the input node of the SA latches one sampling period ago. In other words, the ELD is one sampling period. This fixed ELD ensures that the quantized signals which are to be averaged have been sampled at the same timing. The latch introduced in [13] was used for the SA latch as shown in Figure 4.15, and this latch is advantageous in calibrating the mismatch in a SA latch to make it as small as 1.6mV in standard deviation. Also, two input signals are summed at the input of the SA latch [8]: V4_p and V4_n coming from the loop filter and V5 m-1_p and V5 m-1_n coming from the local feedback path in Figure 4.2.

One example of the transient waveforms of the SA latch is shown in Figure 4.16, where the input signals are selected such that V4_p - V4_n = -2mV and V5 m-1_n - V5 m-1_p = 3mV. The expected result is that Vsa_p is high and Vsa_n is low because Δ = V4_p + V5 m-1_n - (V4_n + V5 m-1_p) = 1mV > 0, and the waveforms confirm that it is true. The effective input voltage for the SA latch was symbolized as Δ.

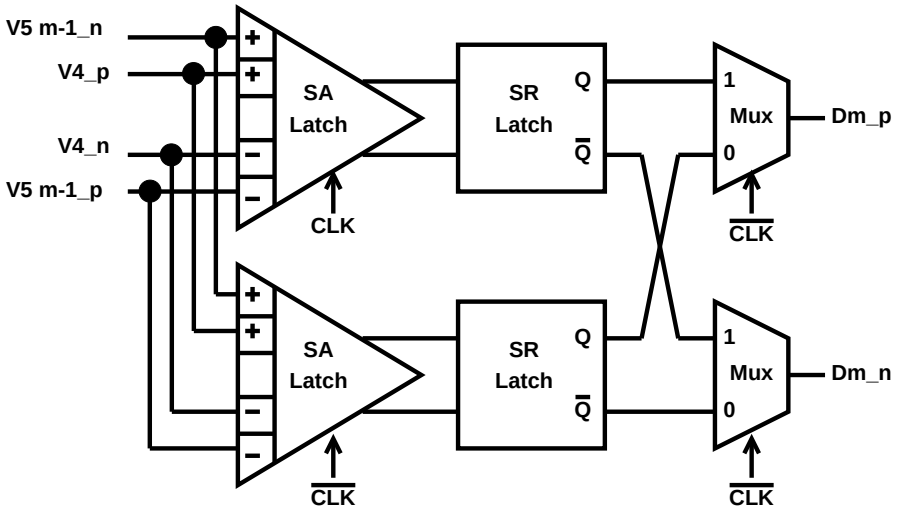

Figure 4.14: The block diagram of the m[th] unit of comparators and latches

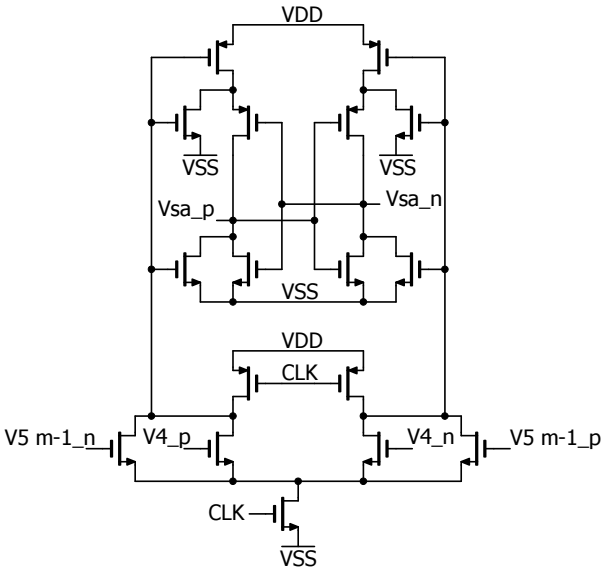

Figure 4.15: The schematic of the SA latch

The function of the unit of comparators and latches in Figure 4.14 is illustrated in the waveforms in Figure 4.17. In this transient simulation, V5 m-1_n - V5 m-1_p is fixed at -20mV, and V4_p - V4_n is given in a pulse oscillating between -22mV and 22mV. When

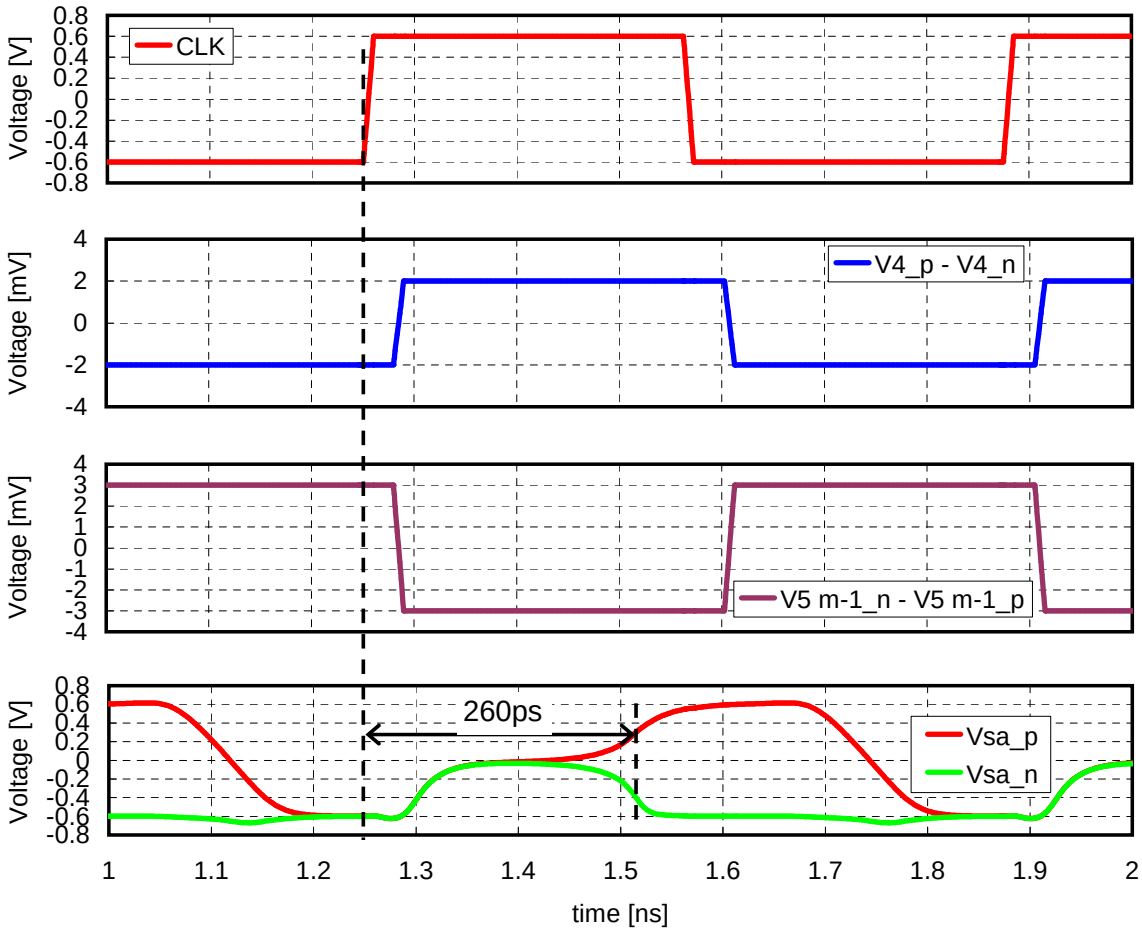

Figure 4.16: The transient waveforms illustrating the function of the SA latch

the input signals are sampled at the rising edge of CLK, the effective input voltage, Δ, is 2mV and the digitized output Dm_p becomes high one sampling period after. At the next quantization cycle, when the input signals are sampled at the rising edge of $\overline{\text{CLK}}$, Δ is -42mV and the digitized output Dm_p becomes low one sampling period after as expected.

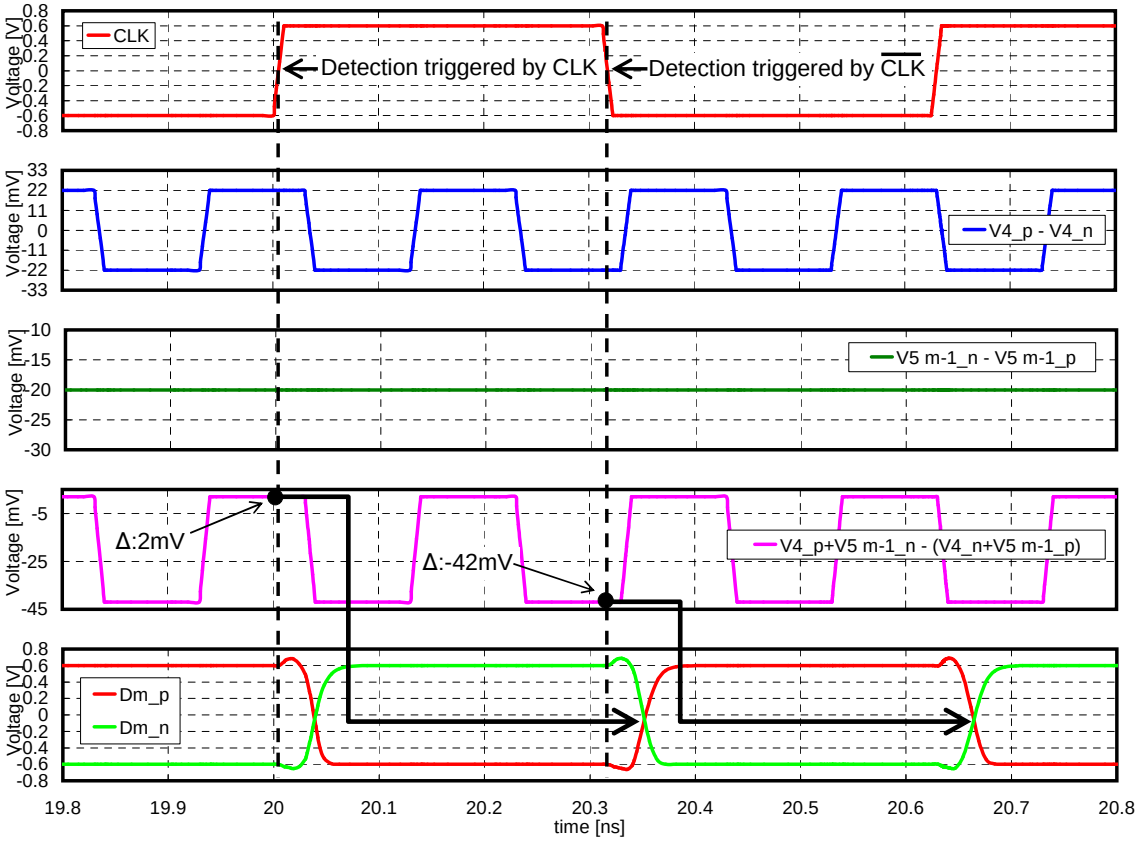

Figure 4.17: The transient waveforms illustrating the function of the unit of comparators and latches

4.3 DACs

There are two sorts of feedbacks in the averaging multi-bit sigma delta modulator: the global feedback and local feedback. Because a sigma delta modulator works as a unity gain buffer at the frequencies within the band width, its basic mechanism is that the difference between the input signal and feedback signal is amplified with a large gain. The global feedback is a system in which a feedback signal is generated and then subtracted from the input signal. The term of global is used because the feedback signal goes all the way back to the input stage to make a loop involving the whole. The local feedback has a different function from the global feedback. The output of one of the single-bit quantizers is connected to the input of another single-bit quantizer via a pre-filter, and this system is called local feedback. The local feedback is provided for the purpose of making quantization noises from multiple single-bit quantizers uncorrelated from one another as explained previously.

The global feedback consists of sixteen current steering DACs, each of which has the same circuit shown in Figure 4.18. The input of the m^{th} (m = 1, 2,. . .,16) current steering DAC is connected to the output of the m^{th} unit of comparators and latches, and its output is connected to the node of Va in the input stage. The bias current, Ibg, is determined so that the output currents of the current steering DACs are averaged at the node of Va. When all Dm_p are high, the current flowing into the node of Va_p is 16 times Ibg. Considering the input resistor, Rin, is 2.5kΩ, the voltage made by the feedback currents is 16 times 2.5kΩ times Ibg, and this should be equal to the half of supply voltage, which makes Ibg be 15μA. The output impedance of each current steering DAC should be sufficiently high because loading occurs when these output nodes are connected in parallel, and the output impedance of every current steering DAC is designed to be larger than 5MΩ.

A local feedback unit is made of a current steering DAC and a pre-filter as shown in

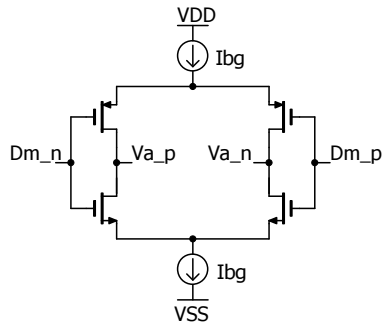

Figure 4.18: The DAC cell for the global feedback

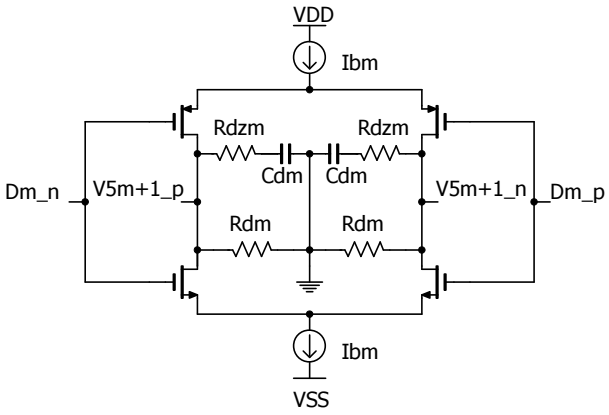

Figure 4.19: The local feedback unit, a current steering DAC with a pre-filter

Figure 4.19. The input of the m^{th} (m = 1, 2, . . . ,16) local feedback unit DAC is connected to the output of the m^{th} unit of comparators and latches, and its output is connected to the input node of the $m+1^{st}$ unit of comparator and latches, V5 m+1. The output of the sixteenth local DAC is connected to the first unit of comparators and latches. The bias currents Ibm should be determined properly because the intensity of local feedback should be changed according to the change in the gain of the loop filter as explained previously. The values of the components and bias currents are decided on the assumption that the gain provided by the loop filter is 61V/V, and they are summarized in Table 4.3. It should be pointed out that there is a difference between the gain assigned to the loop filter, which

is 20.1V/V as in Table 4.2, and the one assumed here. The reason is unknown, but the component values of the local feedback determined referring to the assumed gain of 61V/V is suitable for multi-bit quantization occurring when the actual gain of the loop filter is 20.1V/V.

m	Ib (μA)	Rd (kΩ)	Rdz (kΩ)	Cd (pF)	Ib·Rd/82	k	Ib/1.2
1	32.3	0.300	0.950	0.22	0.795	0.794	27
2	39.7	0.300	0.950	0.22	0.977	0.976	33
3	39.7	0.300	0.950	0.22	0.977	0.976	33
4	32.3	0.300	0.950	0.22	0.795	0.794	27
5	20.4	0.300	0.950	0.22	0.501	0.500	17
6	8.40	0.300	0.950	0.22	0.206	0.206	7
7	1.20	0.250	0.792	0.26	0.025	0.024	1
8	1.20	0.250	0.792	0.26	0.025	0.024	1
9	8.40	0.300	0.950	0.22	0.206	0.206	7
10	20.4	0.300	0.950	0.22	0.501	0.500	17
11	32.3	0.300	0.950	0.22	0.795	0.794	27
12	39.7	0.300	0.950	0.22	0.977	0.976	33
13	39.7	0.300	0.950	0.22	0.977	0.976	33
14	32.3	0.300	0.950	0.22	0.795	0.794	27
15	20.4	0.300	0.950	0.22	0.501	0.500	17
16	8.40	0.300	0.950	0.22	0.206	0.206	7

Table 4.3: The values of the components and bias currents for the local feedback units

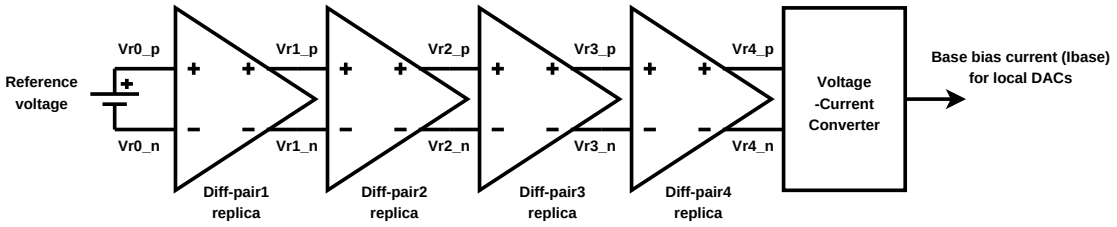

Figure 4.20: The block diagram of the bias generator by which the base bias current for the local feedback units is generated

4.4 Bias Generator

It has been repeatedly stressed that the intensity of local feedback has to be changed when the gain of the loop filter varies, and the variation in the gain does occur because the loop filter consists of open loop differential pairs. The cause of the deviation of the gain of loop filter from the intended gain is mainly the change in the threshold voltages of transistors because of process variations. When a change in the gain of the loop filter occurs, it will be possible to correct the error by adjusting the bias currents, Ibm, of the local feedback units by the same factor as the gain of the loop filter has changed by. Based on this idea, the bias currents, Ibm, of the local feedback units are generated using the bias generator in Figure 4.20. The bias generator consists of a reference voltage, the replicas of differential pairs 1 to 4, and a voltage-current converter. The replicas of the differential pairs have the framework shown in Figure 4.21, where M denotes 1 to 4. Each replica is identical to the corresponding original differential pair except the additional resistors, RrM (M = 1, 2, 3, and 4), These additional resistors are to adjust the gains of the replicas so that the total gain of the cascade of the replicas is nearly equal to one. The voltage-current converter receives the output voltage of the cascade of the replicas and changes it to a current, and its circuit is shown in Figure 4.22. The input voltages of the voltage-current converter, Vr0_p and Vr0_n, are converted to currents by a pair of resistors, Ra,

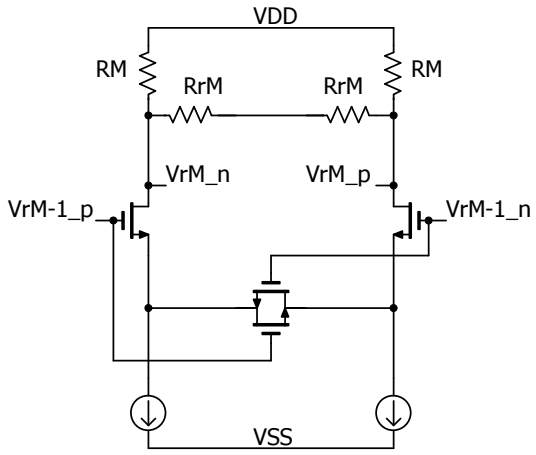

Figure 4.21: The diagram of the replicas of differential piar 1 to 4

and the difference between the two currents is obtained as Ibase. Ibase is proportional to the gain of the cascade of the replicas as well as the reference voltage. Thus, on condition that the precision of the ratios of resistors is good enough, the change in the gain of the loop filter causes Ibase to change in the same proportion. In the present design, Ibase is adjusted to 1.2uA, and the bias currents for the local feedback units are the multiples of Ibase as in Table 4.3. As a result, even when the gain of the loop filter varies because of process variations for example, the intensity of the local feedback is adjusted because the bias currents follow the change.

There is a comment about the closed-loop amplifiers in the bias generator. Although it is true closed-loop amplifiers are used in the bias generator, they work at DC, and they can be realized with very low power. They do not incur the problems associated with designing high speed opamps. In this sense, those closed-loop amplifiers in the bias generator are not counted as a closed-loop amplifier.

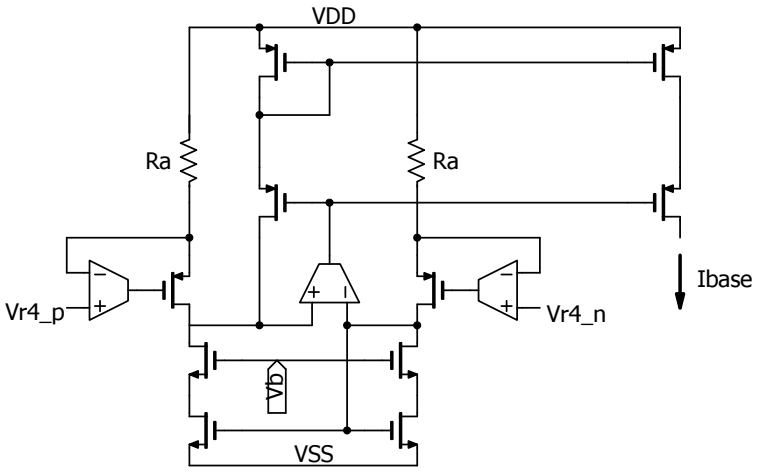

Figure 4.22: The voltage-current converter

5. SIMULATION RESULTS

The set-up for simulations is that the sampling frequency is 2.56GHz, OSR is 16, and the input frequency is 25.625MHz. The SNDR and SNR were simulated, and the plots are shown in Figure 5.1. The maximum SNDR is 43dB. It should be noted that noises except quantization noise were not modeled in the simulations. Clock jitters were not modeled either. Power consumption is 15mW, but it does not include the power consumed by the parts of digital signal processing and clock generation and distribution since these parts are idealized without any power consumption. The FFT spectrum when input amplitude is -6dB is shown in Figure 5.2 along with that of a single-bit quantizer. The noise floors for both cases are at the same level, but quantization noise of the averaging multi-bit quantizer is lower than the single-bit quantizer at high frequencies. The simulation results are summarized in Table 5.1.

	This work	Sun '16 [14]	Weaver '11 [15]	Shettigar '12 [16]
Tech.	90nm	180nm	90nm	90nm
Type	Averaging Multi-bit	VCO-based	Nyquist Flash	Single-bit $\Sigma\Delta$
OSR	16	4	-	50
fs	2.56GHz	800MHz	210MHz	3.6GHz
fBW	80MHz	100MHz	105MHz	36MHz
SNDR	43.0dB*	45.4dB	35.9dB	70.9dB
fin	25.625MHz	1MHz	1MHz	10MHz
Supply	1.2V	1.3/1.6/1.8V	1.2V	1.2V
Power	15mW**	116mW	35.8mW	15mW

* Not including noises except quantization noise

** Not including the parts of the digital domain and the clock

Table 5.1: The performance summary of the open-loop amplifier multi-bit sigma delta modulator and comparison

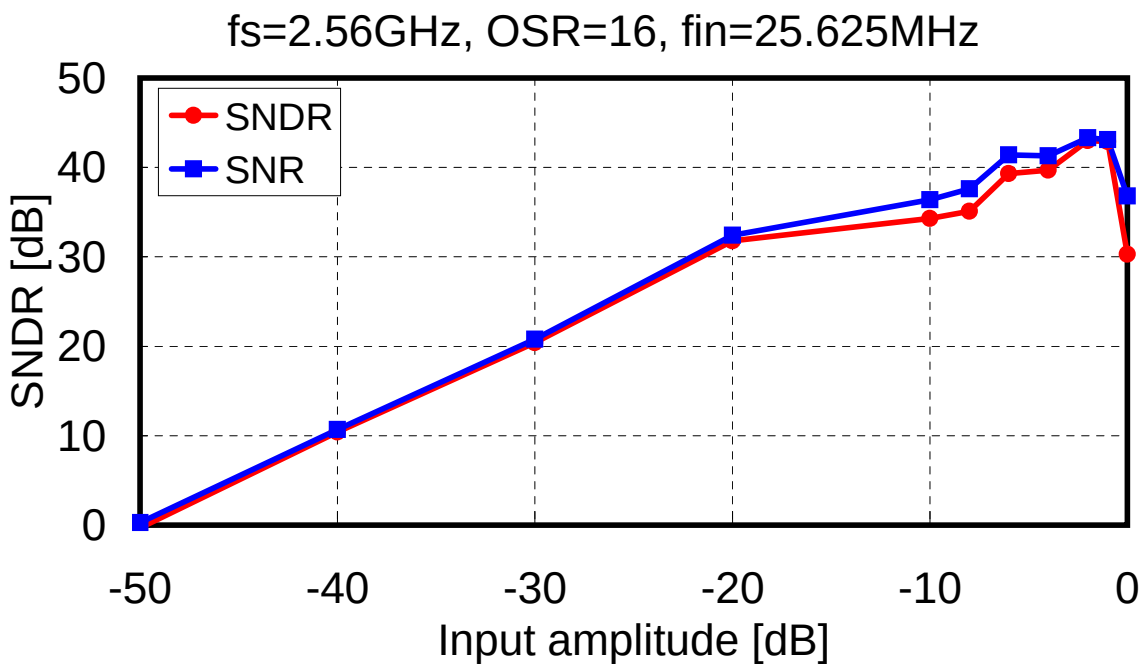

Figure 5.1: The SNDR and SNR of the open-loop amplifier multi-bit sigma delta modulator

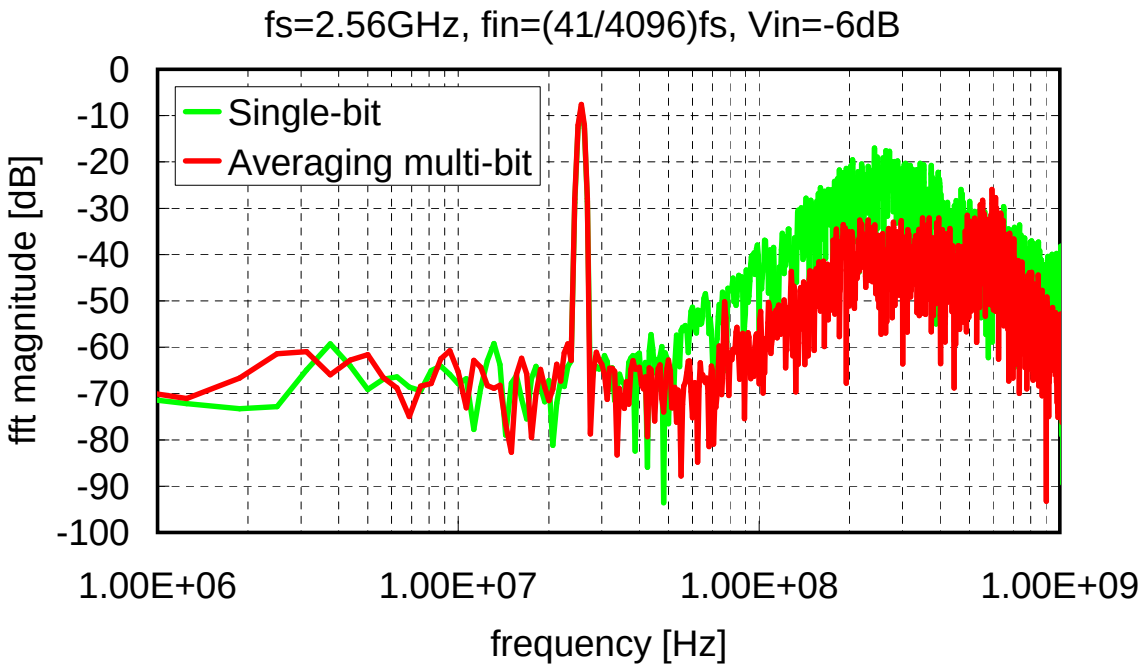

Figure 5.2: The spectrum of the open-loop amplifier multi-bit sigma delta modulator

6. CONCLUSIONS

New types of averaging multi-bit quantizers were proposed. It was demonstrated that these averaging multi-bit quantizers can reduce quantization noises when they are incorporated in a second order sigma delta modulator. Also, an open-loop amplifier multi-bit sigma delta modulator having the newly proposed averaging multi-bit quantizer was proposed. It was demonstrated that the open-loop amplifier multi-bit sigma delta modulator can achieve better SNDR than an open-loop amplifier sigma delta modulator with a conventional single-bit quantizer. The open-loop amplifier multi-bit sigma delta modulator was demonstrated at the sampling frequency of 2.56GHz, but suppressed power consumption was achieved by using differential pairs instead of closed-loop amplifiers.

6.1 Plans for Future Study

The ultimate goal of this research project is to design an ADC that achieves the following specifications:

- SNDR higher than 60dB
- BW wider than 100MHz
- Power consumption less than 10mW

The open-loop amplifier multi-bit sigma delta modulator proposed in this thesis is one of the promising candidates for reaching the goal. There are mainly two reasons. Firstly, it does not need closed-loop amplifiers which consume a lot of power when they are used for high frequency applications. Secondly, it is true that major part of the total power consumption is taken by the array of comparators, but the power consumption can be reduced when a more scaled down technology is used. Though the open-loop amplifier sigma delta

modulator with an averaging multi-bit quantizer looks an interesting architecture, is has to be studied more in detail to know if it is really useful or not. In the following, plans to cover issues which were not dealt with in this thesis will be outlined.

- Noises

  Resistors and transistors produce noises such as thermal noise, but these noises were not taken into consideration in this thesis. This is because no noise model was available to the author. This project is completely self funded and conducted by the author independently. So, the resource was very limited. All the simulations in this study were done with SIMULINK or LTspice. The author had model files of a CMOS 90nm technology by luck, but it did not include any noise models. In the future study, evaluating the effect of noises will be the first thing to do. Because the loop filter has a low gain, the noises caused by the transistors and resistors are less shaped than with conventional closed-loop amplifier based sigma delta modulators. This could bring about harmful effects on the noise performance.

- Clock jitter

  Clock jitter is another important factor that impacts on the performance and should be studied carefully.

- DAC

  The current steering DACs are sources of noise especially when they switch the current directions. A design that can reduce the noisy effects will be examined. Non-return-to-zero pulses were used for the designs in this thesis, but it will also be checked whether this type of feedback pulse is the best or not.

- Corner and Monte Carlo simulations

  The influences of the variations in process, temperature etc have to be studied by

simulations. The variation in the gains of the loop filter is supposed to be taken care of by the adoptive local feedbacks. It is a vital mechanism but has not been tested yet, so it is inevitably necessary to prove that this mechanism works properly.

The research will proceed further with examining the following matters:

- Low power comparators

  A more advanced process will be used for designing comparators to reduce their power consumption. Other techniques such as charge steering which is proposed in [17] will be considered too to reduce the power consumption.

- Increase in the number of branches

  In order to reduce the quantization noises more, the number of branches can be increased. When the number is 64, the effective bit number of an averaging multi-bit quantizer is three, which will be the next target.

- Optimization of the loop filter

  How the locations of poles and zeros should be determined in order to obtain better performances will be studied. How the pre-filters can be improved will be explored as well.

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