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DESIGN OF A CLASS D AUDIO AMPLIFIER WITH OPTIMIZED EFFICIENCY FOR LOW INPUT POWER

An Undergraduate Research Scholars Thesis

by

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Submitted to the Undergraduate Research Scholars program
Texas A&M University
in partial fulfillment of the requirements for the designation as an

UNDERGRADUATE RESEARCH SCHOLAR

Approved by
Research Advisor: Dr. Edgar Sanchez-Sinencio

May 2016

Major: Electrical Engineering

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ABSTRACT

Design of a Class D Audio Amplifier with Optimized Efficiency for Low Input Power

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Audio amplifiers are devices that provide power in the form of current to a speaker in a sound system. Efficiency has been one of the main topics in the VLSI industry as technology grows and analog devices shrink in size. The past years, this parameter has become extremely crucial as we look for ways to extend the battery life of our devices. A Class D Audio Amplifier (CDA) is mostly known for its ability to provide power to a load in an efficient manner. However, due to losses in the power stage, it can never reach 100% efficiency. Different approaches to increase the efficiency have been developed, but all of them target a small range of input power.

After analyzing the dominant losses of the system, we were able to identify that splitting the transistor level power stage into small stages can dramatically increase the efficiency for small input power and maintain the same efficiency for high input power. This improvement in efficiency for a wider power range was accomplished without affecting the overall area of the system. Developing systems that perform better without altering the area that it occupies in the chip is extremely important as we tend to reduce the size of our analog and digital devices.

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ACKNOWLEDGMENTS

I would like to thank my faculty mentor Dr. Edgar Sanchez-Sinencio and my graduate advisor Fernando Lavalle for helping me through the completion of this thesis.

CHAPTER I

INTRODUCTION

A class D audio amplifier (CDA) has been mostly used in the cell phone industry because of its high efficiency and low power consumption compared in Class A, B and AB audio amplifiers. The CDA can provide the best possible efficiency for different input power compared to other audio amplifiers (Fig.I.1). Low power dissipation and high efficiency are what make this amplifier very attractive for future audio applications [1]. Conventional CDA consists of 5 fundamental blocks that make up the system level design (Fig.I.2). The first block is commonly known as compensator or filter of order N. This block eliminates the high frequency component coming from the feedback network block of the amplifier and adds a phase shift of -90*N degrees. As N increases, the filter becomes more complex and expensive but at the same time it can attenuate more undesired frequencies.

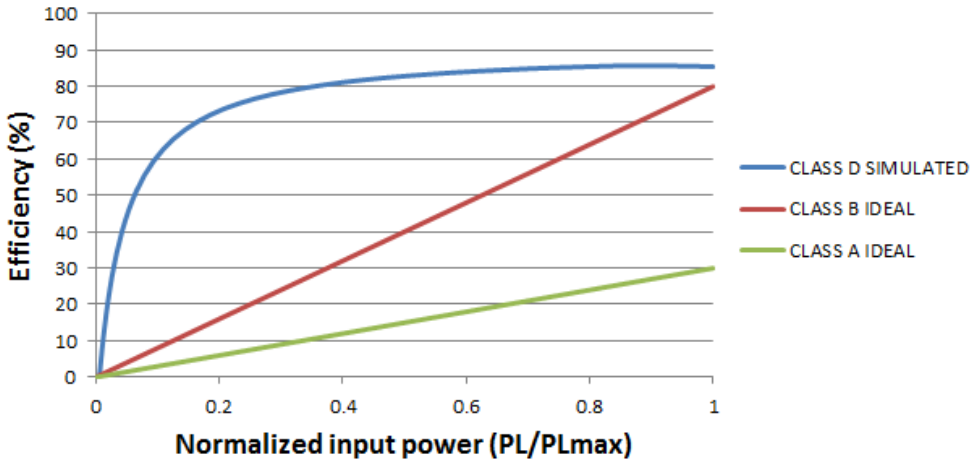

Fig.I.1. Comparison among three different amplifiers

The next block of the system is the pulse width modulation (PWM) modulator. It generates a PWM signal as output when two inputs, the output of the compensator and a highly accurate carrier signal or triangular waveform, enter the block. Other architectures (e.g., Sigma-delta modulation or Self-oscillating modulation) can be implemented replacing the first two blocks, but they require more complex circuitry and power [2]-[3]. The third block's input is connected directly from the output of the second block; this stage is commonly known as the power stage. It provides a large amount of current for the speaker to operate as well as a rail-to-rail voltage in the form of a PWM signal. The topology normally used for the power stage is a push-pull configuration consisted of one NMOS and one PMOS transistor. In addition, a non-overlapping clock is added to ensure that only one of the transistors is turned "ON" at a time.

The fourth stage is connected directly to the speaker and its input consists of the rail to rail voltage provided by power stage. Normally, a second order low pass filter (LPF), which is constructed using an inductor and capacitors, is used due to the fact that it can attenuate high frequency noise coming from the forward path. The cutoff frequency of the LPF is designed to be around the frequency of the input signal which is around 20 kHz for audio signals. The last block, or feedback network, contains information from the power stage and feeds it to a summer in the form of negative feedback, where the input and the output are added before it enters the compensator again. This configuration makes the linearity of the overall system better, which means that variation in the forward gain does not vary as much with different inputs; however, it lowers the overall gain of the system. Closed loop architectures (e.g., CDA) are extremely important because they correct errors in the amplification process which is necessary to obtain a

good audio performance, as shown in Fig.I.1. If the closed loop system is not designed properly, the system can become unstable and ruin the output signal.

The problem with the conventional CDA is that we tend to ignore the efficiency for low input power. As shown in Fig.I.1, the efficiency decreases dramatically as the normalized input power reaches .2(W/W). A technique that has not been implemented on the CDA before is the improvement of efficiency for a wider range of output powers. By choosing the right transistor size in the power stage for a specific input power, it is possible to obtain higher efficiency for small input power and the same or higher for high input power. This could further improve the overall efficiency of a Low-Power Class D audio Power Amplifier [4].

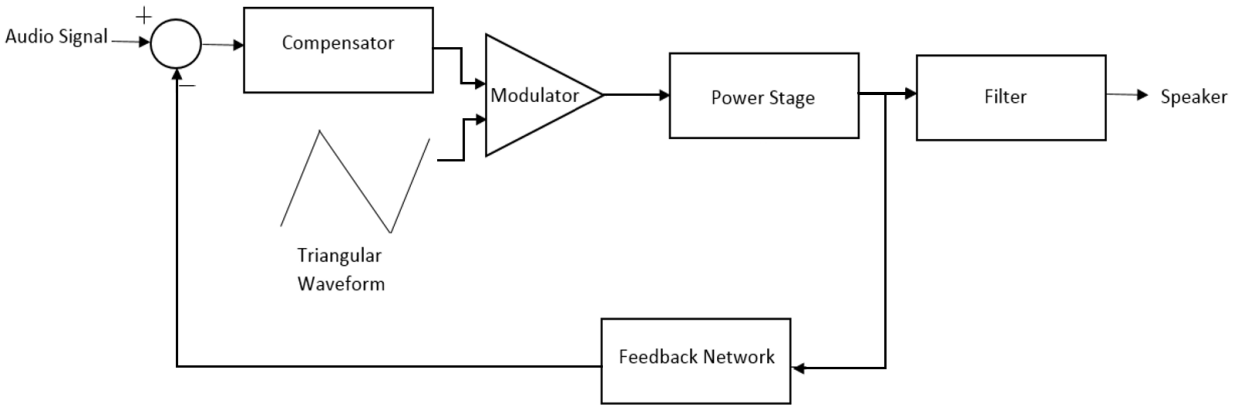

Fig.I.2. Conventional Class D Audio Amplifier

CHAPTER II

METHODS

In order to make the audio signal more robust and with a better efficiency, this signal needs to be converted into pulses. The increase in efficiency is due to the fact that common amplifiers have devices active all the time. On other hand, the CDA rapidly switches between the off and on states, reducing the time in which they are active. These pulses contain information of both the original signal and a high frequency signal needed for the modulation to happen (encoding). Furthermore, the current that these pulses generate is amplified using one NMOS and PMOS transistor and demodulated using an analog filter to recover the original signal (decoding).

Compensator design

The topology used for the compensator stage consists of a two-stage amplifier with Miller compensation (Fig.II.1). The capacitor Cc was designed to ensure pole-splitting. Adding this capacitor will essentially move one of the poles close to the origin (dominant pole) and the other pole of the system far away from the first pole. If chosen properly, this capacitor will prevent the amplifier from becoming unstable. The tail current was designed for providing a high slew rate (how fast the output changes with respect to time) to the amplifier given the capacitor Cc and C_1. The transconductance of M5 was determined in order to meet the phase margin requirement of the system which determines the settling time (the time that it takes for the output to follow the input) as well as ensuring stability. Transistors M1 and M2 were chosen given the minimum GBW requirement. In addition, transistors M3, M4 and M5 were chosen for maximum DC gain and high output swing.

The top level design consists of an integrator operational amplifier with unity gain at a frequency of 40 kHz which was accomplished by choosing the values of C1 and R1 to be 10pF and 400 KΩ respectively, as shown in Fig.II.2. Choosing a large resistor for R1 introduces a large thermal noise which could affect the SNR and THD+N of the system. Similarly, a big capacitor can load the output of the compensator which will make the quiescent current and therefore the power losses to increase. As a result, these two values were chosen to avoid these problems. This stage is extremely important for the system because it eliminates the high frequency component of the modulated signal from the output stage.

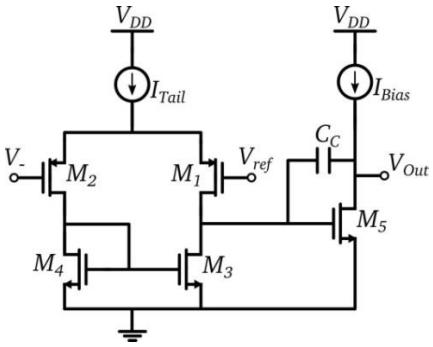

Fig.II.1. Transistor level design

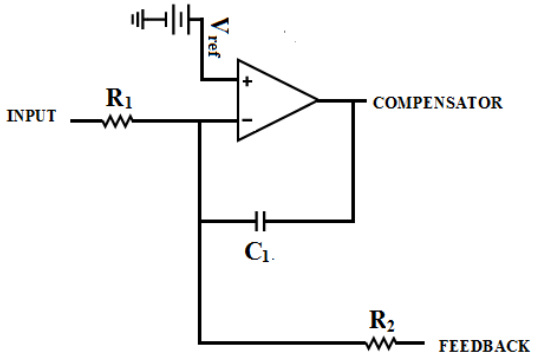

Fig. II.2. Top level design

Design procedure

To obtain a relatively good output noise without loading the output of the compensator, resistors R1 and R2 were chosen considering the resistor thermal noise equation for 1Hz bandwidth (II.1). Where k is Boltzmann constant and T is the temperature in Kelvin.

$$V_R{}^2 = 4kTR \quad (II.1)$$

Capacitor C1 was calculated precisely to meet the unity gain frequency of the integrator (ω_0) which was previously selected to eliminate the harmonics produced at the output (II.2).

$$C_1 = \frac{1}{\omega_0 R_1} \quad (II.2)$$

The compensator stage has to be to handle both the audio signal and the high frequency signal of the power stage. As a result, there must a minimum GBW that ensures this process (II.3). Where f_{max} is the frequency of the amplifier, V_{max} is the maximum expected input signal of transistor $M_{1\text{-}2}$ will receive and V_{sat} is the saturation voltage of the input transistors.

$$GBW_{min} = \frac{f_{max} * V_{max}}{V_{dsat}} \quad (II.3)$$

After selecting capacitor C_c as a trade-off between area and stability and extracting the maximum input capacitance of the modulator stage (C_L), the transconductance of M_5 was found such that the stability of the system (phase margin of 60 degrees) was met (II.6).

$$P_2 = \frac{g_{m5}}{C_L} \quad (II.4)$$

$$Z = \frac{g_{m5}}{C_c} \quad (II.5)$$

$$PM = 90 - \arctan\left(\frac{GBW}{P_2}\right) - \arctan\left(\frac{GBW}{Z}\right) \quad (II.6)$$

The compensator needs a minimum slew rate in order to operate without yielding an undistorted AC output signal (II.7). Given the minimum slew rate, the I_{tail} of the system was found (II.8). The remaining two transistors, $M_{3\text{-}4}$, were designed to maximize output swing and the gain of the system.

$$SR_{min} = 2\pi * f_{max} * V_{max} \quad (II.7)$$

$$I_{tail} \cong SR * C_c \quad (II.8)$$

Modulator design

The topology used for the modulator stage consists of a three current mirror OTA (Fig.II.3). This topology is mostly used as a comparator because of the high slew rate and relatively high gain that it can provide to the system. The reason behind this enhancement in slew rate is due to β factor which is described as the ratio between the transconductance of M5-M6 and M3-M4. This ratio will increase the current from one of the branches of the differential pair (M1 and M2) in such a way that the output can provide more current to the load capacitance. This load capacitance is composed of the gate capacitance of the next stage (Non- overlapping clock) and the drain-bulk capacitance of M6 and M8.

One trade-off that was considered when the modulator was designed was between the area of the system and the slew rate. Increasing the β factor which increases the slew rate comes with a price as a bigger width for the transistors M6-M7 is needed. The gain of the circuit was determined by the transconductance of M1-M2 which was designed to 60 dB. This topology will not be used as an amplifier but rather as comparator. As a consequence, the output DC offset does not need to

be centered between the power supply and ground which allows the width of transistor M7-M8 to be chosen for the given output swing and not the drain to source voltage. The top level design is implemented as an open loop system, as shown in Fig.II.4. The positive terminal of the comparator has as input a triangle wave and the output of the compensator for the negative terminal. The triangle wave was chosen as a trade-off between quiescent current and THD [5]. Whenever the triangle wave is greater compared to the signal in the negative terminal, the output will be high (V_{DD}). Similarly, if the triangle wave is less than the signal in the negative terminal, the output will be low (Ground). This stage is essential for transforming the analog signal to a PWM signal.

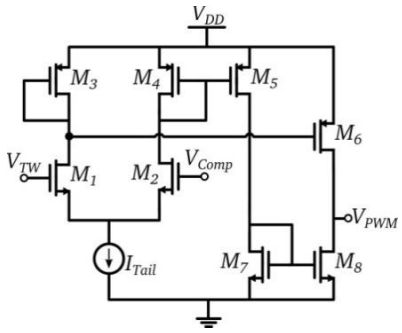

Fig.II.3. Transistor level design

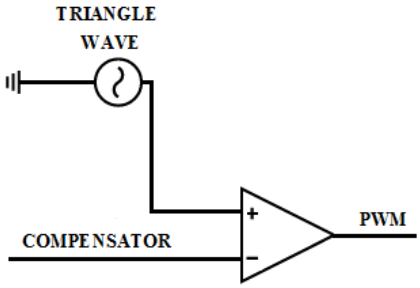

Fig.II.4. Top level design

Design procedure

The comparator for the CDA has to be able to switch between the power supply and ground relatively fast compared to the frequency of the triangle wave in order to minimize propagation delay. The rise/fall time of the output PWM signal was designed to be a .5% of the period of the triangular waveform (T_{SW}). Given this value and the amplitude of the PWM, the minimum slew rate of the modulator was found (II.9).

$$SR_{min} = \frac{V_{dd}}{\frac{.5}{100} * T_{sw}} \quad (II.9)$$

Setting equations II.10 and II.11 equal to each other, the Itail of the modulator and β factor were found. This was accomplished given the SR of the OTA, the maximum current draw from the power supply of the modulator (I_{DD}), and the input capacitance (C_L) of the next stage or non-overlapping clock.

$$SR = \frac{\beta * I_{tail}}{C_L} \quad (II.10)$$

$$I_{DD} = (\beta + 1) * I_{tail} \quad (II.11)$$

The gain of the comparator (A_v) depends on transconductance of $M_{1\text{-}2}$, output impedance, and the β factor which was already determined. Given the minimum gain and the β factor, the transconductance of $M_{1\text{-}2}$, $M_{3\text{-}4}$, and $M_{5\text{-}6}$ were found, as explained in equations II.12 and II.13. The gain of this stage can be further increased by increasing the transconductance of $M_{1\text{-}2;}$ however, the designer has to also consider the area increased as a result. Transistor $M_{7\text{-}8}$ was designed for maximizing output swing.

$$\beta = \frac{g_{m5,6}}{g_{m3,4}} \quad (II.12)$$

$$A_v = \beta * g_{m1,2} * (rds6//rds8) \quad (II.13)$$

Filter stage design and feedback network

The main purpose of the output filter is to recover the audio signal after amplification which was encoded within the PWM signal. This filter is normally found outside the chip due to the size of the components (Fig.II.5) [6]. An inductor and a capacitor are mostly used to reduce the losses of the system given the fact that the current provided by the power stage flows through these components. The filter accomplishes two things; it eliminates the dc component of the output signal such that it is centered in the x-axis and also gets rid of the high frequency component from the output stage. Other topologies such as the filterless CDA can also be implemented as a way to reduce the area; however, the efficiency of the system is reduced compared to the conventional CDA [7]. Given the load R_L which can be represented as an 8 ohm resistor, the value of L1 and C2 were chosen precisely to have a cut-off frequency of 25 KHz. Similarly, C3 was chosen to eliminate the DC component. The feedback network which completes the closed loop system is composed of a resistor R2 (Fig.II.6). The resistor R2 in conjugation with the capacitor C1 will act as a first order filter that is in charge of eliminating all frequencies beyond the unity gain frequency of the amplifier. The value of R2 determines the gain of the overall closed loop system and the position of unity gain frequency. If R2 increases, there will be more attenuation; however, the thermal noise produced by a bigger resistor can affect other parameters.

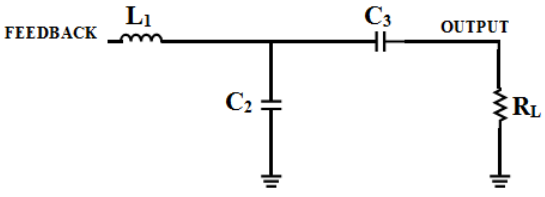

Fig.II.5. Bandpass filter.

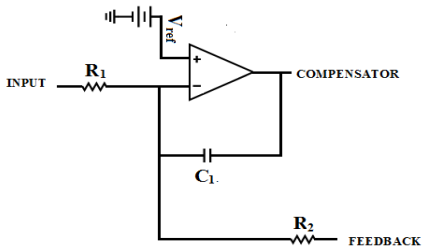

Fig.II.6. Feedback Network

Power stage design

The CDA power stage is typically designed to minimize the short current losses, switching losses and conduction losses; however, none of them can be improved at the same time. The short circuit losses can be reduced by incorporating a non-overlapping clock to the system [8]. The delay created by the non-overlapping clock was chosen as a trade-off between distortion and efficiency [9], [10]. As shown in Fig.II.7, the non-overlapping clock is composed of 2 NAND gates and 5 NOT gates. This circuit ensures the NMOS transistor (N1) is completely off before the PMOS transistor (P1) is turned on. Three power stages in parallel with the same R_{on}'s were chosen for this experiment. Whenever the first stage is activated, the overall On-resistance equals 1.2 Ohms. Since all the stages are parallel to each other, 2 stages will generate a total On-resistance of .6 Ohms. Similarly, three stages will introduce the system with a total On-resistance equal to .4 Ohms.

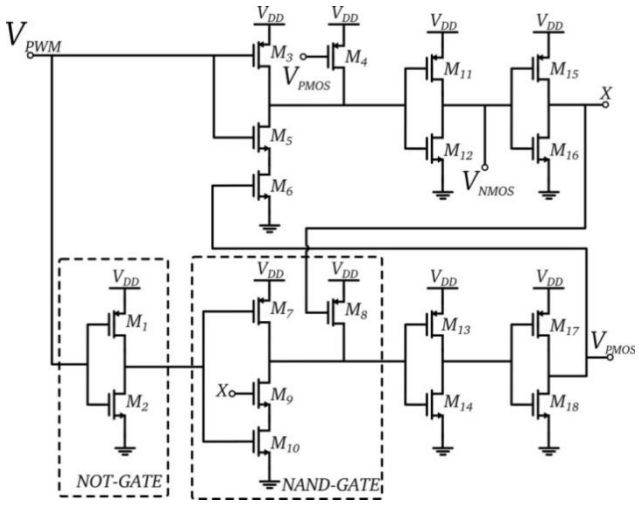

Fig.II.7. Non-overlapping clock

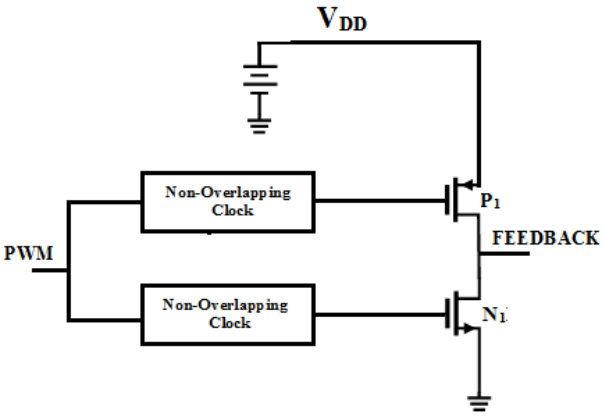

Fig.II.8. Power stage

Design procedure

The waveforms at each node within the non-overlapping clock were first analyzed. This was accomplished by applying a clock signal at the input and checking the overall delay contribution as the signal passes through the NOT gates and NAND gates for both positive edge and negative edge of the clock. The delay by each NOT and NAND gates was determined by calculating the overall resistance and capacitance to ground of the output node, as shown in II.14.

$$\text{Delay} = R_{\text{total}} * C_{\text{total}} \quad (\text{II}.14)$$

Given the input capacitance of the power stage, the width of the transistors $M_{11\text{-}12}$ and $M_{17\text{-}18}$ were adjusted such that the delay requirement was met. Similarly, the same method was applied from the output to input in order to find the rest of the transistors widths given the delay needed.

Dominant power losses

The efficiency curve of a class D can never reach 100 % efficiency due to power dissipation within the system. The main four sources that cause this problem are quiescent losses, short circuit losses, conduction losses and switching losses which originate in different places within the system. A quiescent loss is the power that is dissipated by the overall system when no input is applied and normally depends on the architecture used. Although this loss occurs in almost every stage of the class D, the power stage is not the major source that creates this dissipation. Short circuit losses can dramatically affect the system; however, they can be avoided or reduced to a relatively small value by designing the non-overlapping clock correctly between the modulator and power stage. This leaves us with only two sources, conduction and switching

losses that can be improved. These sources are constantly changing with different output powers, size of transistors and switching frequency, but only one is dominant at a time for low and high output powers.

Examining power losses

The dominant loss for low input power is due to switching losses of both MOSFETs in the power stage, which depends on the power supply, parasitic capacitors and the frequency of the triangular waveform (II.15). Conversely, the dominant loss for high input powers is due to conduction losses, which solely depends on the output current and R_{on} (On-resistance), as described in II.16. In addition, both losses are present for intermediate output powers. For a given power supply, switching losses can be reduced by decreasing the frequency of the carrier signal or decreasing the parasitic capacitors which is directly proportional to the width of each MOSFET. Similarly, conduction losses are proportional to the output power with a slope that is equal to R_{on} of the MOSFET divided by the load resistance (R_L). The On-resistance is inversely proportional to the width of the transistor, which means that in order to reduce this loss, W has to increase for a given L.

$$P_{Switching} = {V_{DD}}^2 C_p f_{sw} \approx {V_{DD}}^2 \mathbf{W} L C_{gg} f_{sw} \qquad (II.15)$$

$$P_{Conduction} = {I_o}^2 R_{on} = \frac{P_o}{R_L} \frac{L}{\mathbf{W} \mu_{n,p} C_{ox} (VDD - V_t)} \qquad (II.16)$$

Proposed system

In order to have a better efficiency for low input powers and maintain the same efficiency for high output powers, the power loss due to switching has to decrease significantly. One way to

solve this problem is by splitting the big transistor stage into N small stages such that the overall area stays the same, as shown in Fig.II.9. Implementing this approach will allow us to have a better control of the area or Width (W) that we want to use at a certain moment. For instance, if we decide to use a fraction of the overall stage, the area and the value of the parasitic capacitors will decrease thus reducing the switching power loss and increasing the efficiency.

Given the fact that it is impossible to reduce both losses at the same time, it's necessary to find the point of intersection in which both losses are equal in order to know how to effectively increase or decrease the width of the power stage for different input powers. In other words, if the input power is less than the value at the intersection, which is dominant by switching losses, then we can decrease the width of MOSFET by only activating one part of the divided power stage and if it is greater than the value at the intersection, which is dominant by conduction losses, then we can increase the width of the MOSFET by simply adding one more stage in parallel.

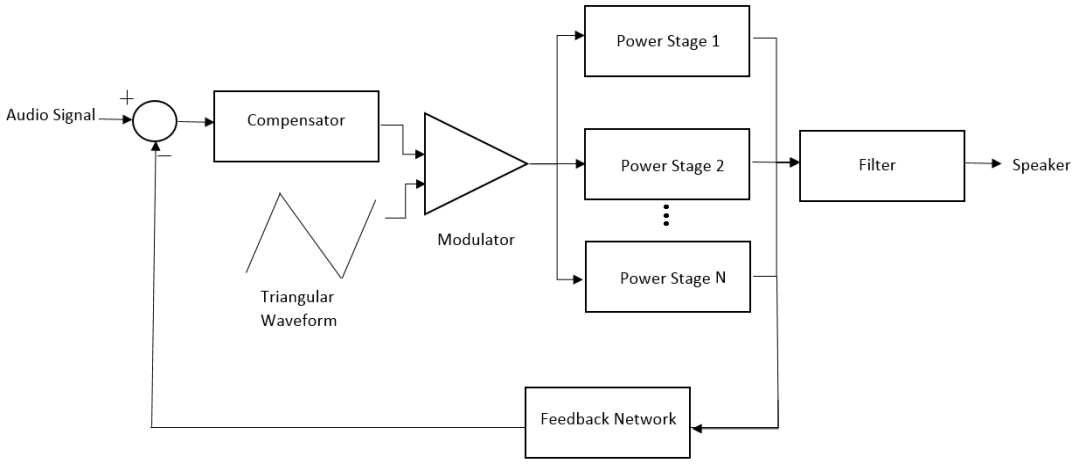

Fig.II.9. Block design for efficiency improvement

The technology used for this research corresponds to CMOS IBM 130nm. The length of the transistors implemented for the power stage was the minimum in order to minimize losses and 5 times the minimum for the compensator and modulator stage to increase the output impedance and the gain of the block.

CHAPTER III

RESULTS

After analyzing the dominant losses of the system, we were able to identify that splitting the transistor level power stage into small stages can dramatically increase the efficiency for small input power and maintain the same efficiency for high input power. This improvement in efficiency for a wider power range was accomplished without affecting the overall area of the system, as shown in Fig.III.1.

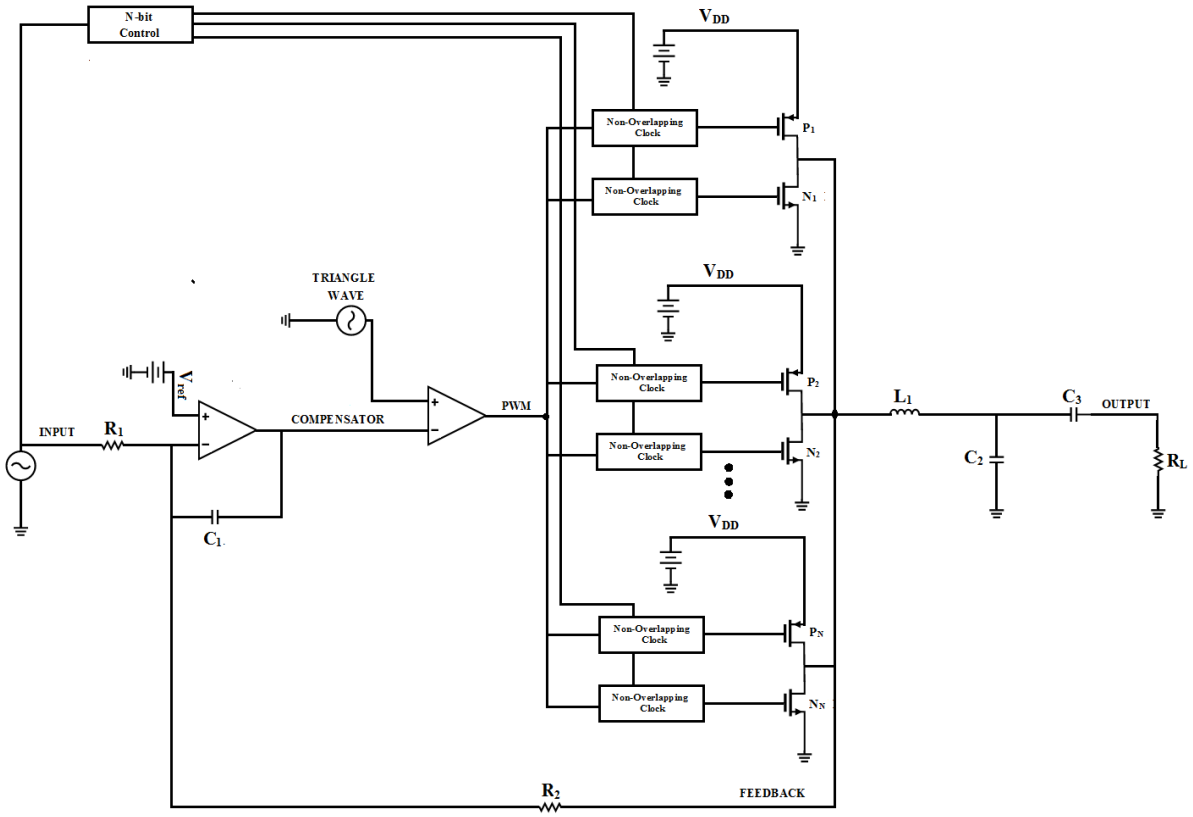

Fig.III.1. System level design of the proposed Class D Amplifier

As explained in the method section, the audio signal is compared to a triangle wave. The result of these two waveforms produces a PWM signal (Fig.III.2). It is important to note that less power is dissipated within the system if the audio signal is encoded within another signal (PWM) before amplification. This is due to the fact that the transistor in the power stage has a zero current when not switching and low voltage (VDS), thus giving a small power dissipation.

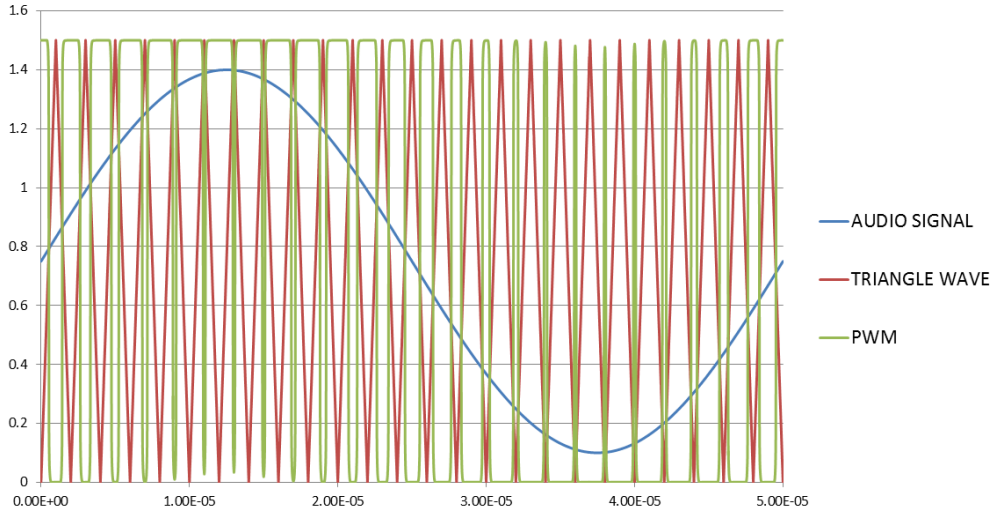

Fig.III.2. Modulation of audio signal

The delay that the non-overlapping clock generates will not allow both transistors to operate at the same time, thus avoiding a spike in current which is caused due to a short circuit from the power supply to ground (Fig.III.3). This spike dramatically affects the CDA because most of current is not transferred to the output directly but instead goes to both R_{on}'s (PMOS and NMOS). This event creates extra power dissipation in the power stage and decreases the efficiency.

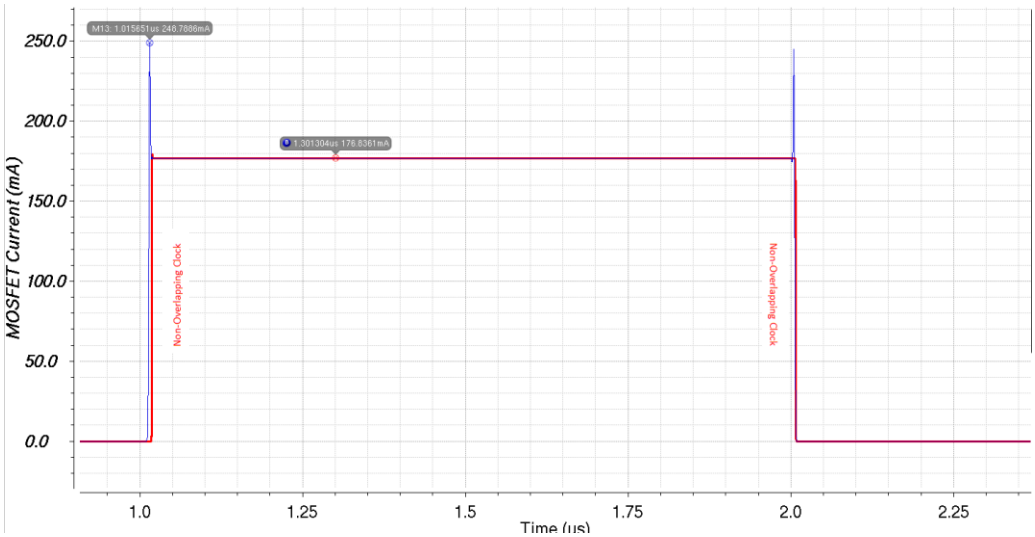

Fig.III.3. Drain current of power stage

For this experiment, three R_{on}'s equal to 1.2 Ohms, .6 Ohms, .4 Ohms were chosen. As shown in Fig.III.4, the widths of the PMOS transistors were 1.27mm, 2.55mm, 3.8mm respectively. Equivalently, the widths of the NMOS transistors were 312.9um, 625.6um, and 938.4um respectively. It can be noticed that as the width of the transistor increases, the on-resistance decreases. This corresponds to a reduction in conduction losses and therefore an increase in efficiency for high input power.

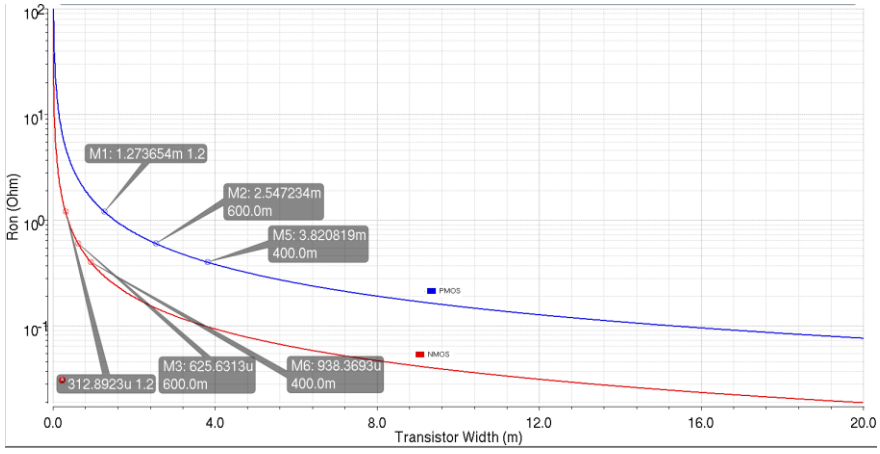

Fig.III.4. R_{on} (Ohm) vs Transistor Width (mm)

Similarly to the Ron resistance, The total capacitance at the gate (dominant capacitance) of the MOSFETs was analyzed for every stage (Fig.III.5). It was observed that the capacitance increases as the width of of the transistor increases for both the NMOS and PMOS. This corresponds to an increase in switching losses and therefore a decrease in efficiency for low input power.

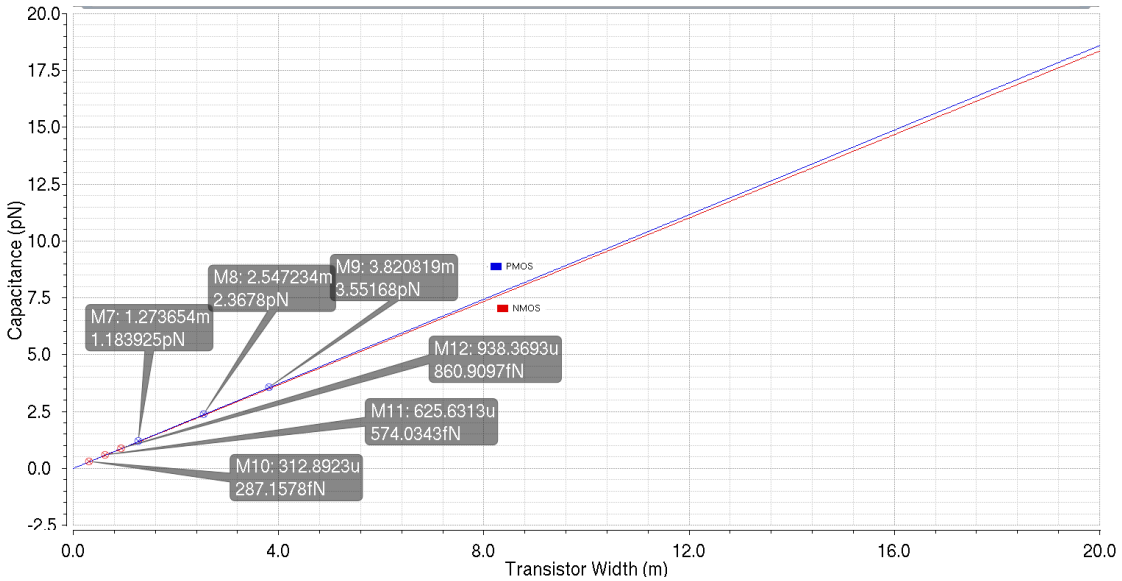

Fig.III.5. Gate Capacitance (pF) vs Transistor Width (mm)

The efficiency vs input power curve shown in Fig.III.6 was accomplished by sweeping the input signal from 10 mV to 750 mV. Each signal generates a specific input power and therefore a point in the efficiency curves. The control block which determines how many stages are “ON” at a certain time depending of the input will generate a new curve that contains the highest efficiency out the three curves below. An improvement of efficiency of more than 50 % was obtained for an input power of 3mW. The control block that will be implemented in future research will detect the input signal using a peak detector and transform the signal to digital using some type of ADC

technique. This digital signal will pass through a digital logic block which will decide how many stages should be operating to obtain the maximum efficiency possible.

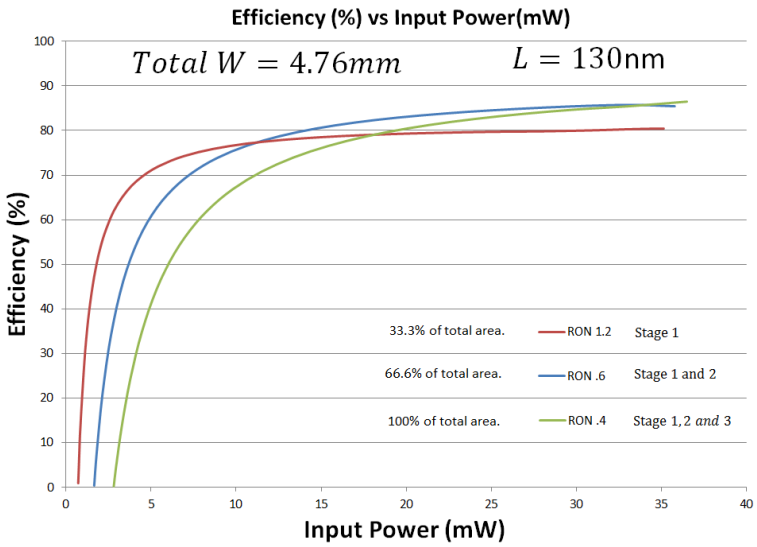

Fig.III.6. Efficiency (%) vs Input Power (mW)

CHAPTER IV

CONCLUSION

From the results of this research, we can see that it is in fact possible to achieve higher efficiency for low input power without affecting the area of the system. Understanding the fundamental components and blocks that make up the CDA is essential for determining the losses of the system. Although this paper focuses primarily on the efficiency of the CDA, other parameters such as THD+N, SNR, and PSRR have to be considered before the implementation of this design on an actual integrated chip. Future research will be focused on the implementation of the control block which will make the proposed CDA function with an actual audio signal.

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