INTERCONNECTED MODULAR MULTILEVEL CONVERTER (IMMC) USING WIDE BAND GAP DEVICES FOR MULTIPLE APPLICATIONS

A Dissertation

By

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ABSTRACT

This dissertation proposes a high-power density Interconnected Modular Multilevel Converter (IMMC) with sinusoidal output voltage for multiple applications. The proposed converter utilizes wide band gap devices at a high switching frequency to achieve compact size/weight/volume. The proposed converter is modular in construction, employs high frequency L-C components and can be stacked for voltage sharing.

The IMMC is proposed for motor drives applications due to the following advantages: sinusoidal output with adjustable voltage and frequency (v/f), no acoustic noise, low EMI and absence of dv/dt related issues due to long motor leads. Two design examples for low voltage drives using Gallium Nitride (GaN) devices and medium voltage drives using Silicon Carbide (SiC) are discussed in this dissertation.

The proposed converter is also evaluated for solar micro-inverter applications due to its compact size and the high-quality output. The proposed system connects the inverter to the PV solar panel through a flyback converter for stepping up the voltage to the grid level, isolation and Maximum Power Point Tracking (MPPT). The proposed inverter eliminates the need for a bulky grid-tie inductor or complex LCL filter. The power can be injected to the grid using a small iron-core inductor due to the sinusoidal nature of the output voltage. A grid-tie control using Fictive Axis Emulation (FAE) is implemented on the converter to optimize the power injected to the grid. Moreover, a DC-AC IMMC to integrate two PV power plants through medium voltage DC collection grid (MVDC) system is proposed. The sinusoidal output of the IMMC facilitates the integration of the solar plants. The inductance required to connect the inverter to the grid is less due to the sinusoidal nature of the output of the IMMC.

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CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a dissertation committee consisting of Professor Prasad Enjeti [advisor], Le Xie and Jun Zou of the Department of [Electrical Engineering] and Professor Mahmoud El-Halwagi of the Department of [Chemical Engineering].

All work conducted for this dissertation was completed by the student independently.

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1. INTRODUCTION

1.1 Wide Band Gap (WBG) Devices.

The rapid progress of renewable energy resources integration has resulted a need for efficient, high power, fast and high temperature semiconductor switches. Because of that, Wide Band Gap (WBG) devices came into existence. The emergence of the WBG devices improved the power density and the efficiency of the power electronic interface of renewable energy resources. The most commercially available WBG devices are the Gallium Nitride (GaN) and Silicon Carbide (SiC) due to their superior performance in the blocking voltage, switching losses, temperature and switching speed [1].

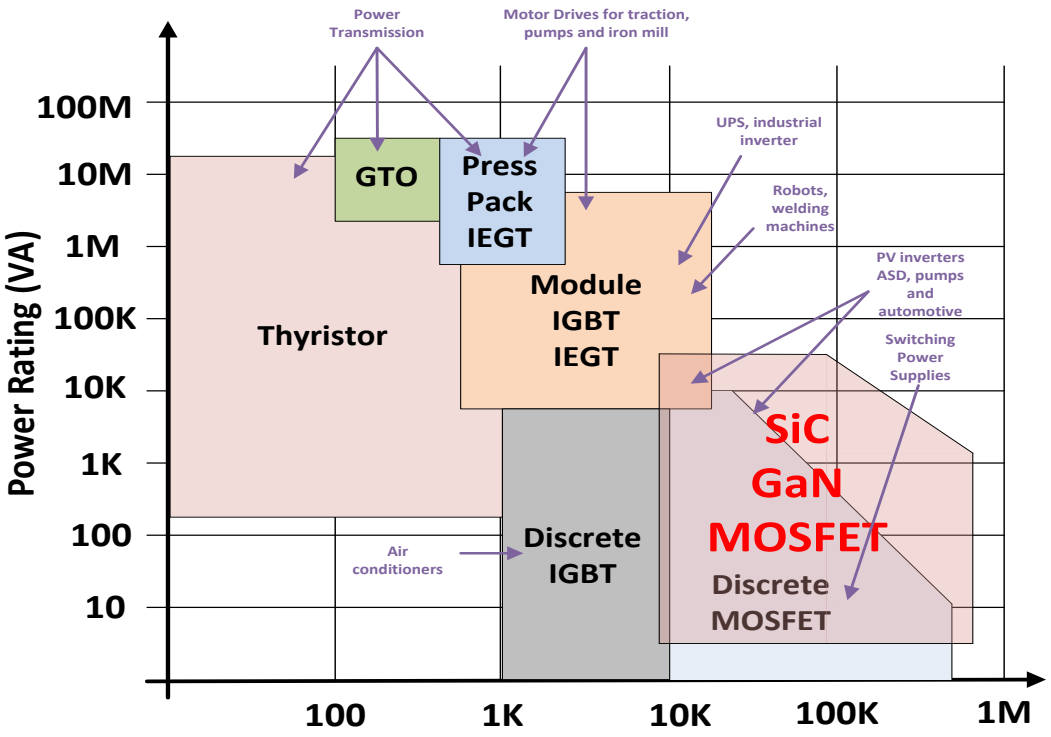


Fig. 1 Market integration of devices applications (Reprinted with permission from IEEE [2] - Copyright © 2014, IEEE).

Fig. 1 shows that the future predicted market will be dominated by WBG devices (SiC and GaN) in multiple applications. The blocking voltage of the GaN is limited to 1200 V using the deposition of GaN on a silicon substrate [3]. Therefore, preventing GaN devices from entering medium and high-power range applications. However, GaN is still a suitable candidate for applications that require high switching frequency as shown in Fig. 2. For higher power applications, SiC devices become a better candidate due to the higher blocking voltage and higher temperature limit.

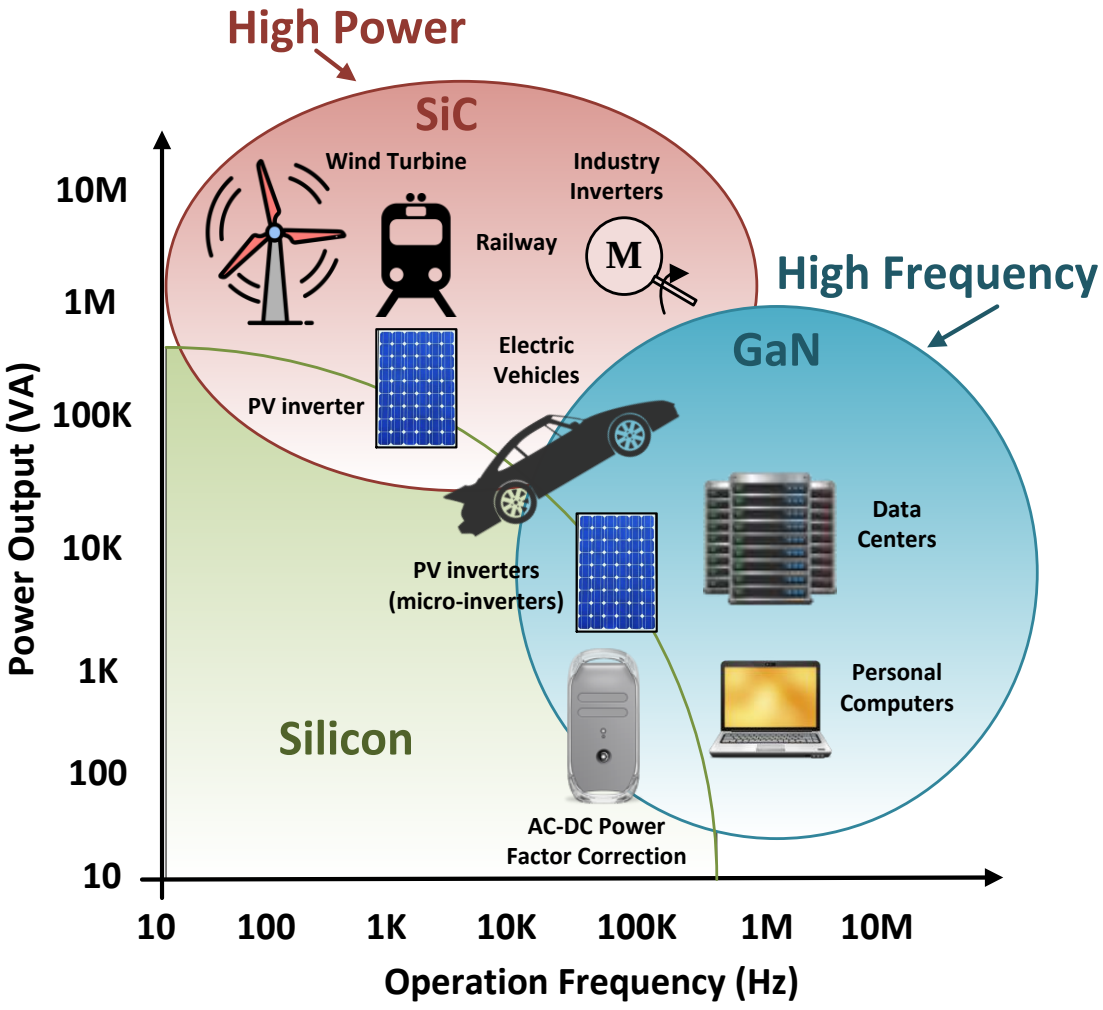


Fig. 2 Predicted applications for transistors (Reprinted with permission from IEEE [3] - Copyright © 2014, IEEE).

Operating a converter with a high switching frequency using Silicon (Si) based devices affects the efficiency and the performance of the converter adversely [4]. The high switching losses of the Si devices resulted from the low bandgap (1.1 eV) and critical electric field (0.3 MV/cm) of the Si decreases the efficiency of the converter. Moreover, the low bandgap of the Si limits the maximum junction temperature of the devices. With the development of Wide Band Gap (WBG) semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC), switches can operate at a higher switching frequency and temperature with higher efficiency. Fig. 3 summarizes the impact of each material property on operation, power module and power system. Table 1 shows the material properties of WBG devices compared to Si [4].

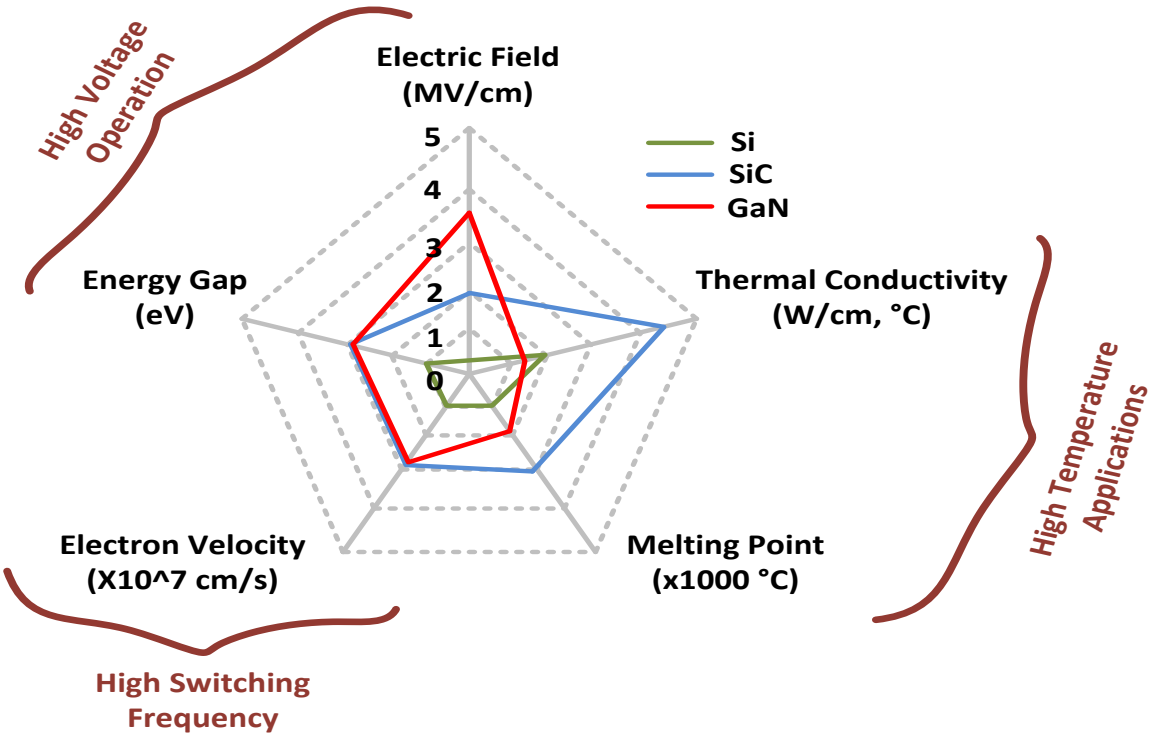


Fig. 3 Material property analysis of Wide Bandgap Devices (Reprinted with permission from IEEE [5] - Copyright © 2014, IEEE).

Table 1 Material Properties of Si, SiC and GaN

Property	**Si**	**SiC**	**GaN**
Bandgap Energy (eV)	1.1	3.2	3.4
Electron Mobility (cm2/Vs)	1350	700	1500
Critical Electric Field (MV/cm)	0.3	3	3.3
Saturated Electron Drift Velocity (107 cm/s)	1	2	2.5

1.2 Literature Review: Multilevel Converters.

The evolution of inverters started with the two levels inverter as shown in Fig. 4. Research continued to improve the output of inverters to serve different applications. Therefore, proposing a higher number of levels to resemble a sinusoidal waveform leading to the birth of multilevel converters. The first concept of multilevel converter was proposed in 1975 [6]. After that, multilevel converters gained the attention of researchers from all around the world due to their advantages over the two levels inverter shown in Fig. 4 (A). Great effort is spent to improve their performance and optimize their control to suit several applications.

Consequently, new multilevel topologies are invented and proposed. The fundamental mechanism of multilevel converters is to synthesize a staircase waveform by switching a series of semiconductors. This section presents an overview of the existing state of the art multilevel converters since the proposed converter in this thesis will be compared with existing multilevel converter topologies.

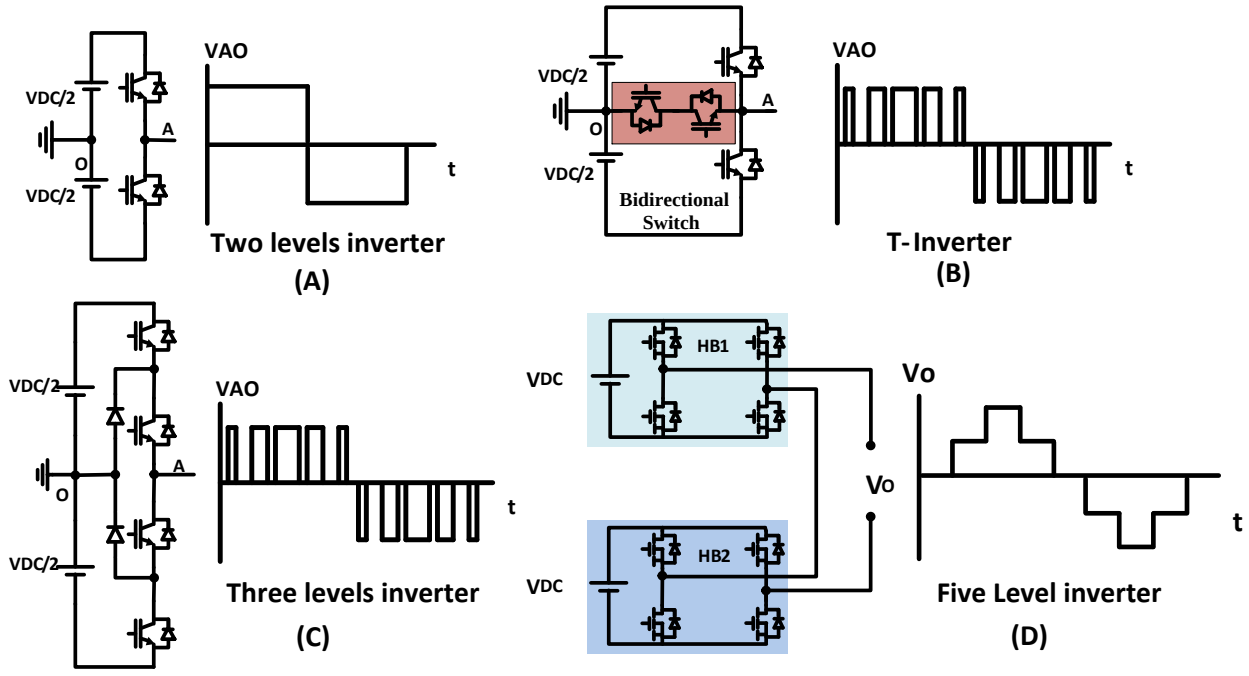
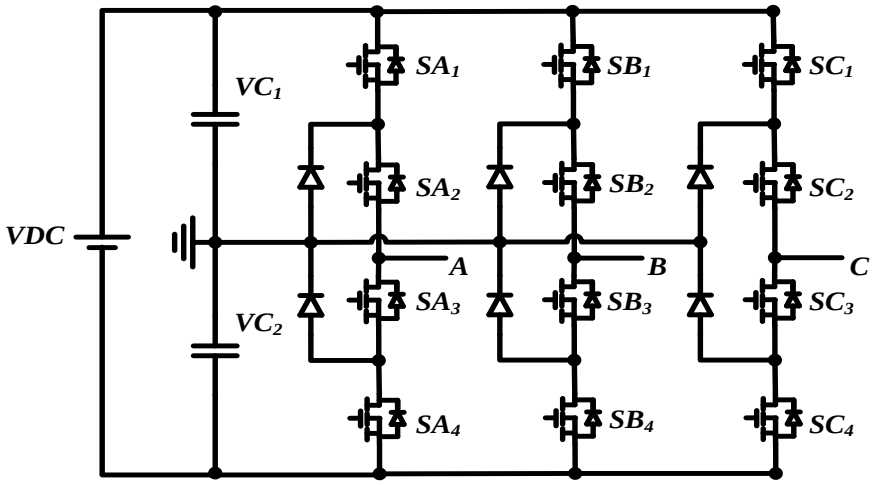


Fig. 4 Evolution of inverters (A) Two levels inverter (B) T-inverter (C) Three levels inverter (D) Five levels inverter.

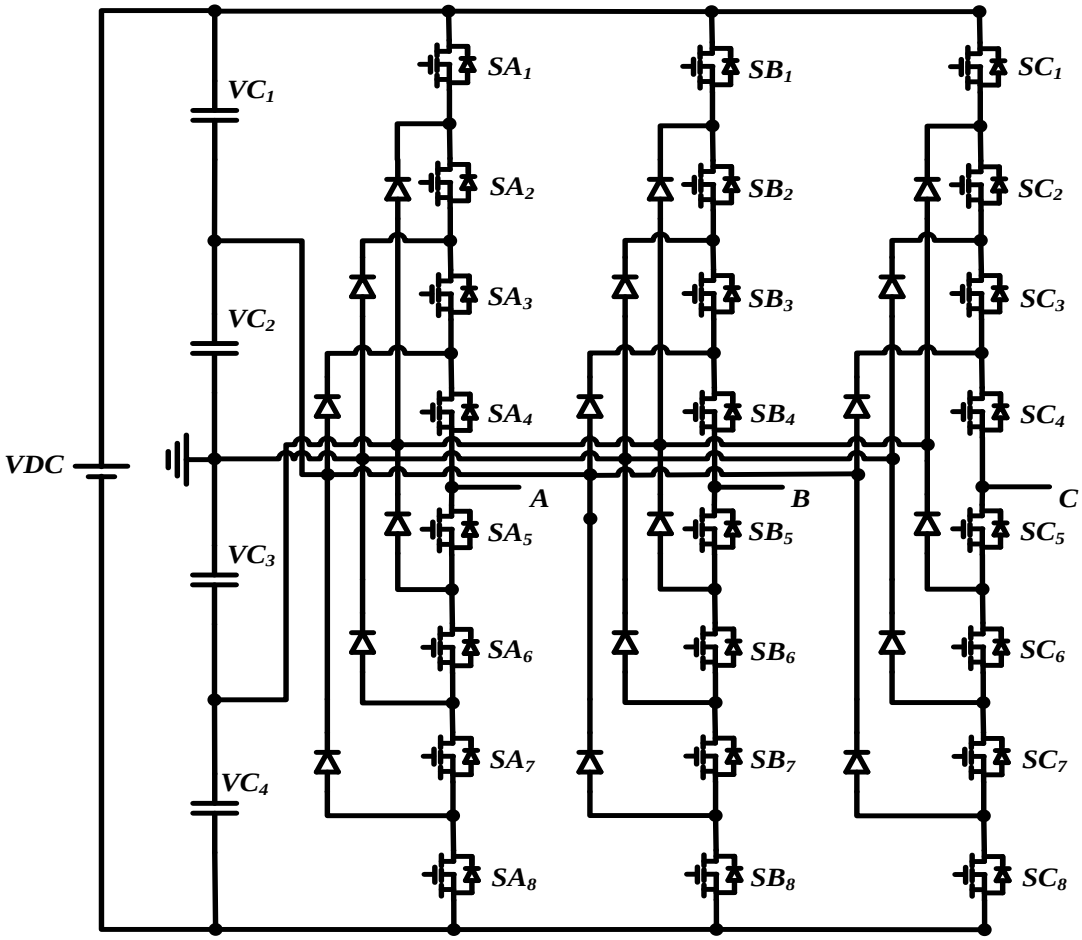
There are many existing multilevel topologies and the number is expanding every year. However, this section will provide an overview of most popular topologies which are Neutral Point Clamped Converter (NPC) Modular Multilevel Converter (MMC) Cascaded H-bridge (CHB) Flying Capacitor Converter (FCC).

1.2.1 Neutral Point Clamped Converter (NPC)

The Neutral Point Clamped Converter (NPC) was proposed in 1981 by Nabae, Takahashi, and Akagi as a three levels inverter [7]. The NPC topology gained success in the field and researchers published many papers to investigate the topology and propose higher number of levels. Fig. 5 shows the three level and five level NPC. The NPC found a place in multiple applications such as high power medium voltage drives and solar Photo-Voltaic (PV) inverters.



(A)



(B)

Fig. 5 The Neutral Point Clamped Converter (NPC) (A) Three levels (B) Five levels

Advantages:

- Low number of passive components (capacitors and inductors)
- Simple structure and low cost

Disadvantages:

- High $\frac{dV}{dt}$ and common mode voltages.
- Complex balancing control is required to balance the DC link capacitors.
- Asymmetrical loss distribution in the clamping diodes.
- Large number of components when operated with high number of levels.

1.2.2 Modular Multilevel Converter (MMC)

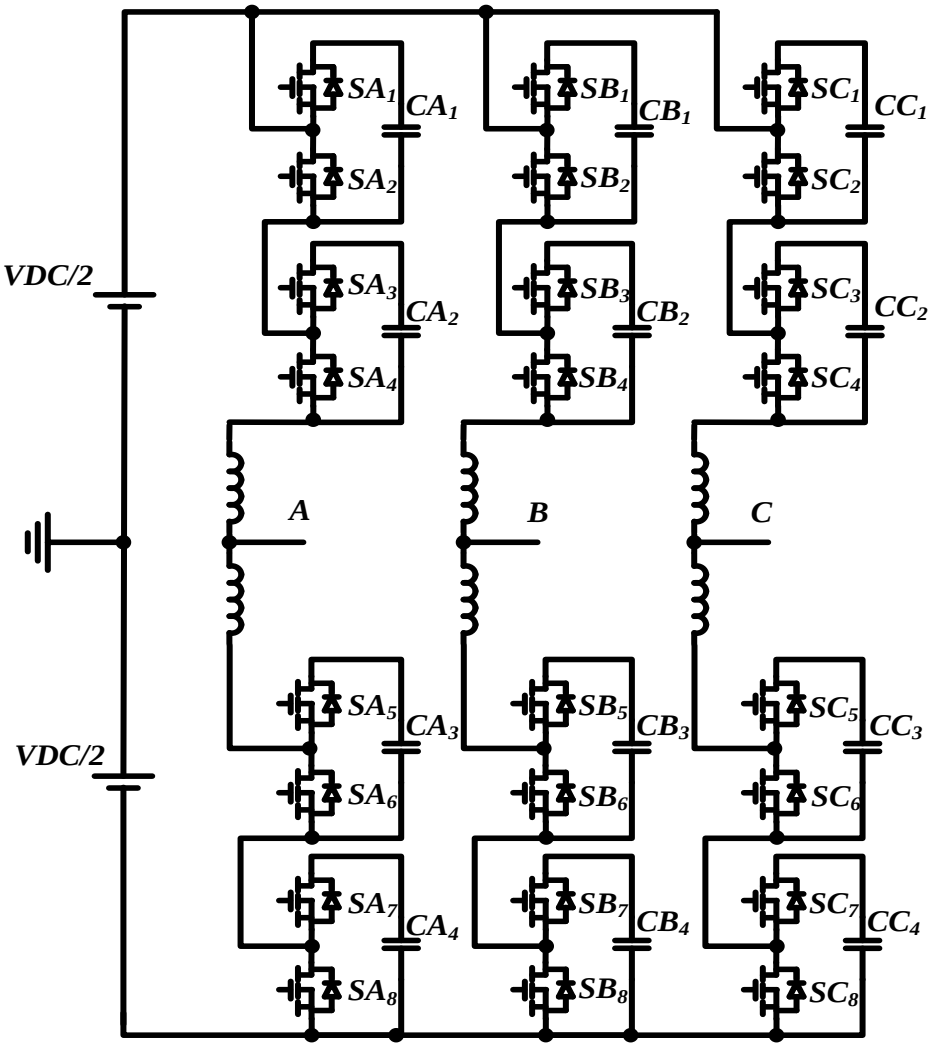


Fig. 6 Three level Modular Multilevel Converter (MMC).

The modular multilevel converter (MMC) was proposed by A. Lesnicar and R. Marquardt in 2003 [8]. The MMC is one of the most popular multilevel topologies for High Voltage Direct Current Transmission (HVDC). It a consists of submodules stacked in series, each submodules contains half bridge switches and a capacitor as shown in Fig. 6 and Fig. 7. The output is a staircase waveform that depends on the number of half-bridge submodules.

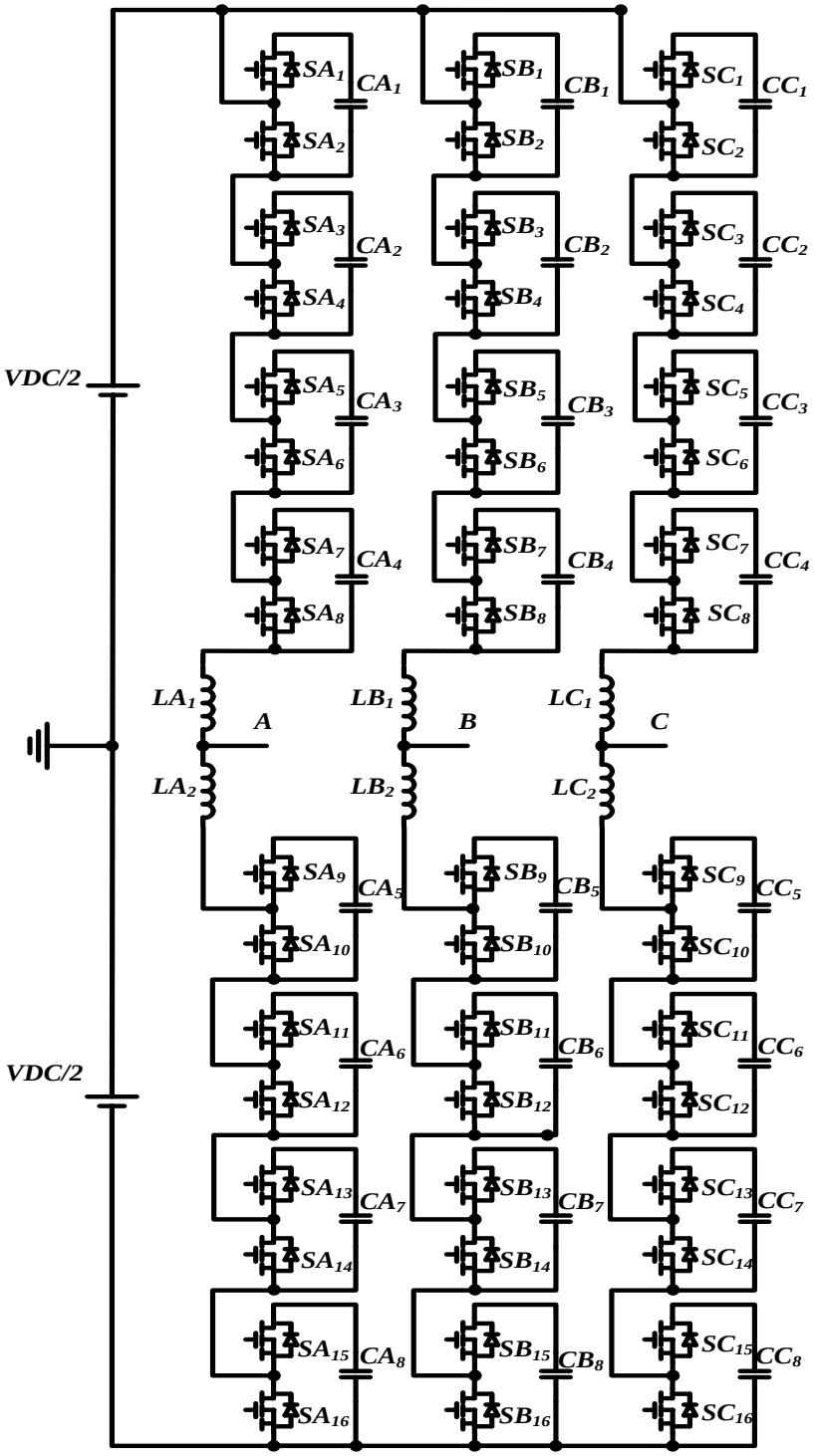


Fig. 7 Five Level Modular Multilevel Converter (MMC)

Fig. 6 shows a three-level MMC that contains four submodules per leg and Fig. 7 shows a five-level MMC that contains six submodules per leg.

Advantages:

- Scalability and modularity to suit high voltage/power applications.
- Fault tolerant: submodules can be replaced easily in case of faults.

Disadvantages:

- High $\frac{dV}{dt}$ and common mode voltages.
- Large submodules capacitors.
- Low frequency operation (10Hz) results low frequency harmonic (10Hz) on the submodule capacitors when the submodule is a half bridge.

1.2.3 Cascaded H-Bridge Converter (CHB)

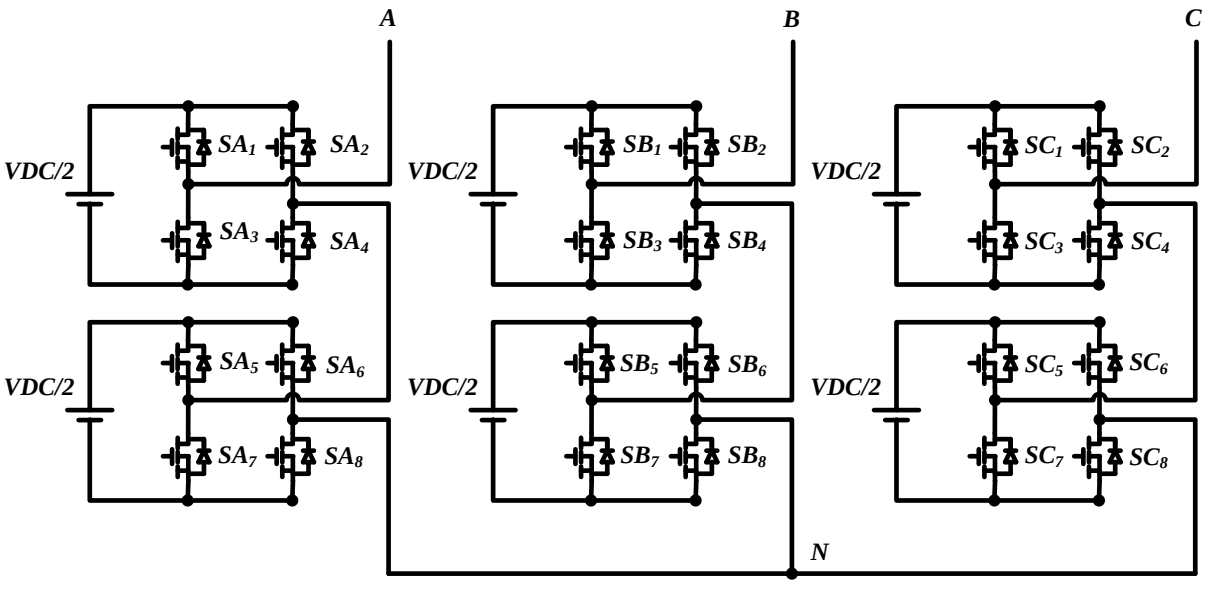


Fig. 8 Five level Cascaded H-Bridge Converter.

The cascaded H-Bridge (CHB) consists of several stacked single-phase H-Bridge inverters (full bridge) connected in series as seen in Fig. 8. The series connection builds the steps of the multilevel (staircase) output of the converter. The advantages of CHB paved the way for the topology to become a popular choice for many applications such as AC motor drives, Static Synchronous Compensation (SVC) and renewable energy resources integrations.

Advantages:

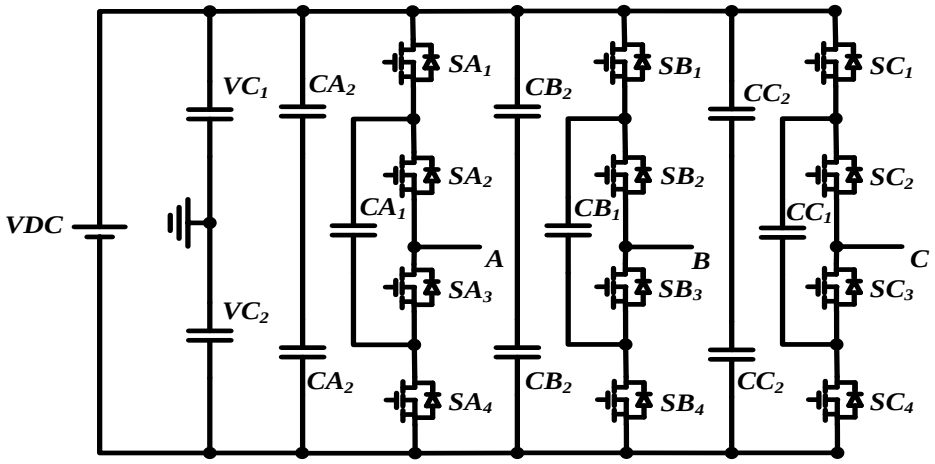
- The number of levels in the output voltage is more than two times the dc sources.
- Scalability and modularity to suit high voltage/power applications.
- Fault tolerant: submodules can be replaced easily in case of faults.

Disadvantages:

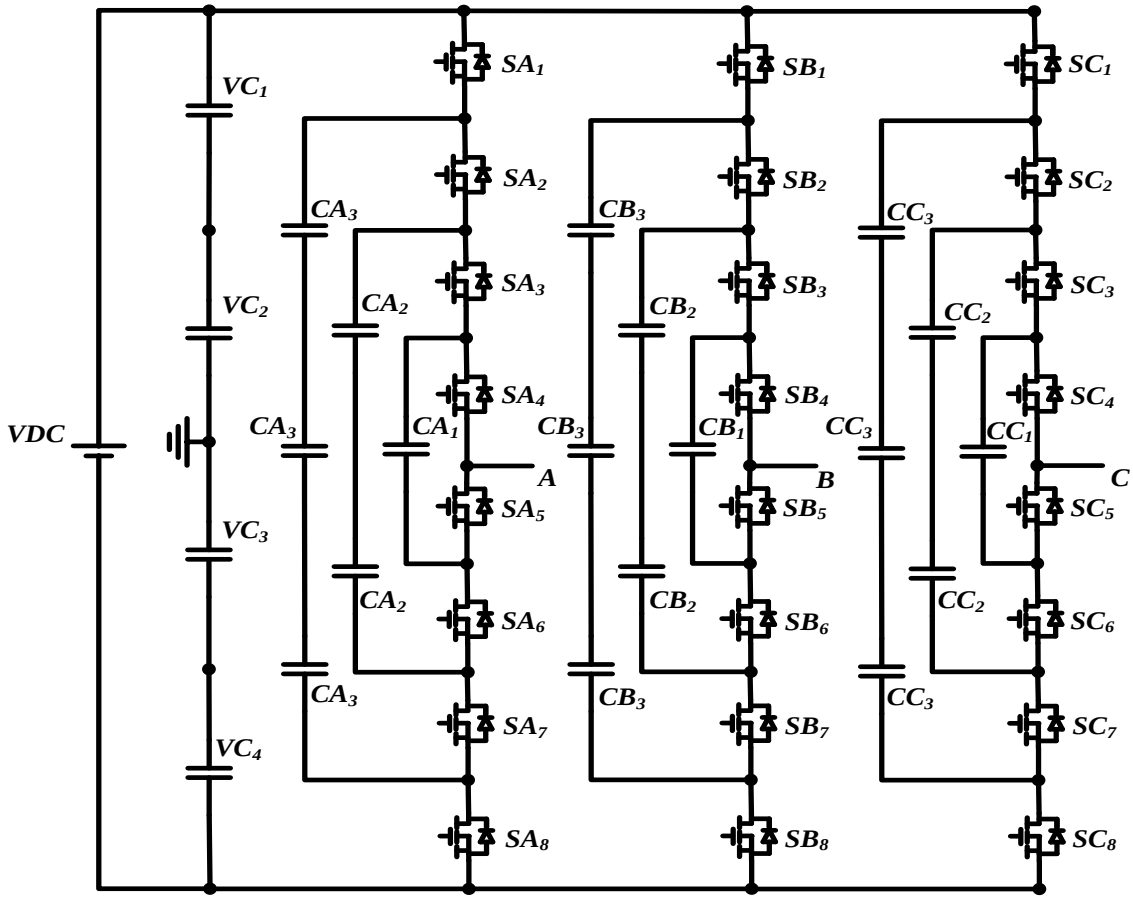
- High $\frac{dV}{dt}$ and common mode voltages.
- Each H-Bridge requires a separate DC source. Therefore, several transformers and rectifier stages are required.
- Low frequency operation results low frequency harmonic in the DC link.

1.2.4 Flying Capacitor Converter (FCC)

The flying capacitor converter (FCC) was proposed by Meynard and Foch in 1992 [9]. The FCC was inspired by the NPC topology, but the NPC diodes were replaced with capacitors. The output of the FCC is a multilevel staircase waveform. A step in the waveform results from two neighboring capacitor legs. Increasing the number of levels in the output can be achieved by increasing the number of capacitor legs. Fig. 9 (A) and Fig. 9 (B) show a three level and five level FCC respectively.



(A)



(B)

Fig. 9 Flying Capacitor Converter (FCC) (A) Three levels (B) Five Levels

Advantages:

- Scalability to any number of levels.
- Ride through capability due to the high number of capacitors.

Disadvantages:

- High $\frac{dV}{dt}$ and common mode voltages.
- Large number of capacitors.
- Complex control is required to balance the capacitors.

1.3 Research Objective

The main objective of this dissertation is to exploit the emergence of the wide band gap devices to develop high efficiency and power density converters. Wide band gap devices are not fully utilized and there are several research opportunities to optimize the power conversion process. This dissertation introduces wide band gap solutions for motor drives, solar micro-inverter and large scale PV power plants integration applications.

The first objective of this dissertation is to propose a new high-power density converter using wide band gap devices for motor drives. The proposed converter solves major problems with existing converters used for motor drives. The proposed converter produces a sinusoidal output that eliminates the need for an output filter. Therefore, eliminating the dv/dt related issues due to long motor lead. Moreover, the sinusoidal output of the proposed converter diminishes the acoustic noise resulted from the pulsating torque in the existing PWM converter. A low voltage drive converter using GaN and a Medium voltage drive converter using SiC are built in the laboratory to validate the operation of the converter.

The second objective is to propose a new micro-inverter that solves the grid-tie filter issues. Existing micro-inverters could be tied to the grid using a bulky and unfeasible inductor or a complex LCL-filter that has several design issues. The proposed micro-inverter produces a sinusoidal output that reduces the grid-tie inductor requirements. The grid-tie inductor used with the proposed micro-inverter is small due to the sinusoidal nature of the output. Moreover, an iron core can be used due to the line frequency of the voltage on the inductor. Additionally, low voltage GaN can be used due to the multilevel feature and the passive components are small due to the high switching frequency of the converter.

The third objective of the dissertation is to propose a full system to integrate large PV power plants to the grid using medium voltage DC collection grid. The power sharing stage has an essential role in allowing the series connected PV power plants to supply different powers under partial shading conditions. The DC collection side of the proposed system eliminates the bulky 50/60 HZ AC collection transformers. The proposed medium voltage class central inverter is a high-power density IMMC using SiC that inject power to the grid with minimum grid-tie inductor requirements.

1.4 Thesis Outline

The first chapter introduces an overview of wide bandgap devices and a comparison with the other existing devices. The comparison includes the material properties that gave wide band gap devices a superior performance compared to the traditional Silicon based devices. The predicted applications for each device are discussed. Moreover, a literature review on existing multilevel topologies such as Neutral Point Clamped Converter (NPC) Modular Multilevel Converter (MMC) Cascaded H-bridge (CHB) Flying Capacitor Converter (FCC) is covered.

The second chapter introduces the Interconnected Modular Multilevel Converter (IMMC) as a new high-power density converter that utilizes Wide Band Gap devices. The operation and modulation of the converter are discussed in detail. Additionally, the derivation of the equations started for the three submodules design and then it is extended to an N number of submodules. After that, the proposed IMMC is compared with existing multilevel topologies to evaluate the proposed converter in different comparison aspects.

The third chapter introduces the converter for motor drives application. A low voltage drive design IMMC is proposed and a low voltage laboratory prototype is built using Gallium Nitride (GaN) devices to prove the concept. Another design for medium voltage applications using Silicon Carbide (SiC) is proposed. A laboratory prototype is built using SiC and experimental results are demonstrated.

In the fourth chapter, a micro-inverter using the IMMC is introduced. The solar panel is connected to the IMMC using a flyback converter to provide isolation and Maximum Power Point Tracking (MPPT) operation. A full design of the micro-inverter elements is covered. Additionally, a micro-inverter grid tie control using Fictive-Axis-Emulation method is explained. The grid-tie control is simulated to demonstrate the viability of the proposed micro-inverter.

The fifth chapter proposes a full system to integrate two PV power plants to the grid. The focus of the chapter is on the DC/AC IMMC that integrates the PV power plants to the grid. Experimental results of a DC/DC and DC/AC IMMC laboratory prototype are presented as well.

2. INTERCONNECTED MODULAR MULTILEVEL CONVERTER (IMMC)*

2.1 DC-DC IMMC

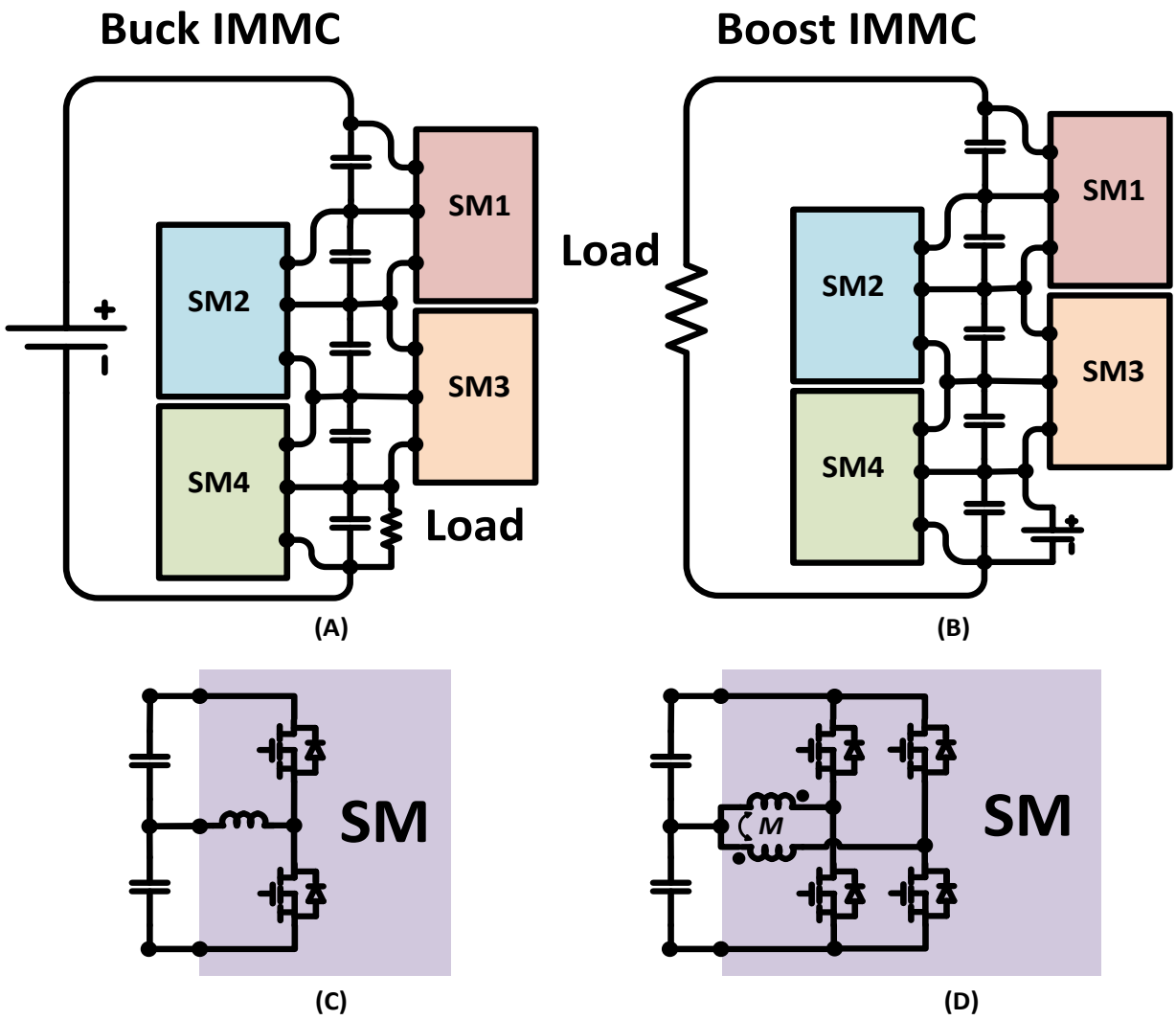


Fig. 10 The DC-DC version of the IMMC that can step up or step down the input voltage. Each submodule can be a half of full bridge (A) Buck IMMC (B) Boost IMMC (C) Half-bridge submodule (D) Full Bridge submodule.

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A. Allehyani, A. Morsy and P. Enjeti, "A new Interconnected Modular Multilevel Converter (IMMC) with sinusoidal voltage output suitable for high performance AC drives," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8. Copyright 2017 by IEEE.

The DC-DC version of the IMMC is proposed in [10, 11]. It can operate as a buck or boost converter by operating the stacked submodules as step-down or step-up stages as shown in Fig. 10 and Fig. 11. The modulation and control of the DC-DC converter is a simple 50% duty cycle on each submodule. The 50% operation of the submodules achieves capacitor balancing for each submodule. Therefore, achieving charge equalization for the stacked capacitors.

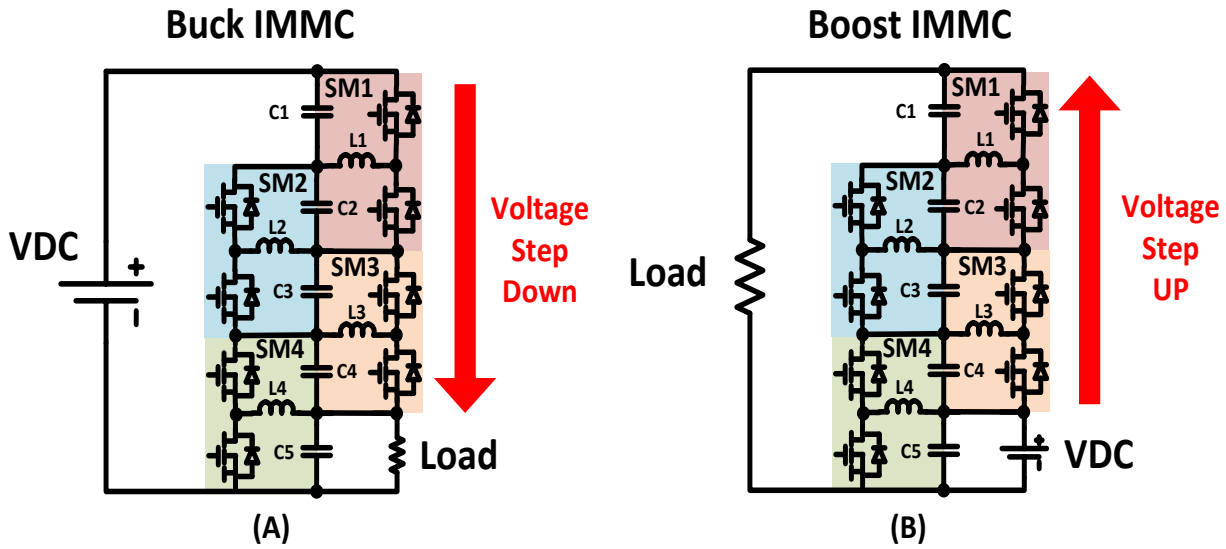

Fig. 11 The DC-DC IMMC with the half-bridge submodules structure to step the voltage up or down (A) Buck IMMC (B) Boost IMMC.

2.1.1 DC-DC IMMC Circuit Analysis

This section focuses on the half bridge submodule DC-DC IMMC. The equations derivations of the inductors and capacitors are covered due to the similarity to the proposed DC-AC IMMC in this dissertation.

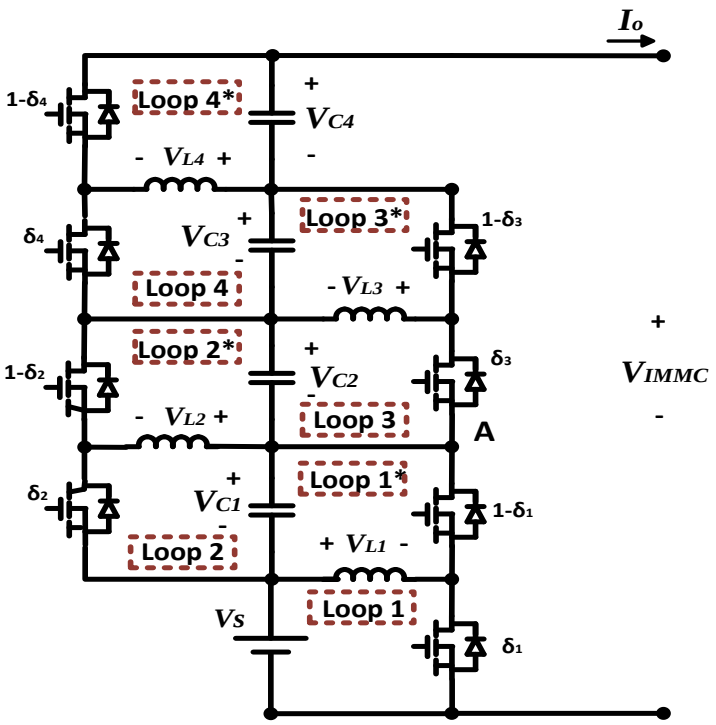

Fig. 12 Loops to determine the inductor equations.

The most fundamental rule in power electronics is that the sum of the voltage on an inductor in a full cycle must be zero. The previous rule is used to derive the voltages of the capacitors. It is shown in Loop 1 in Fig. 12 that applying the rule on L_1 derives the equation of the voltage across C_1. Therefore, the voltage on C_1 is expressed in (1).

$$V_{C1} = \frac{\delta_1}{1-\delta_1} V_s \tag{1}$$

The same approach is applied on the rest of the inductors to derive the voltage on each capacitor. The voltage on C_2, C_3 and C_4 are expressed in (2), (3) and (4) respectively.

$$V_{C2} = \frac{\delta_2}{1-\delta_2} V_{C1} \tag{2}$$

$$V_{C3} = \frac{\delta_3}{1-\delta_3} V_{C2} \tag{3}$$

$$V_{C4} = \frac{\delta_4}{1-\delta_4} V_{C3} \tag{4}$$

Therefore, a generalized equation for capacitors voltage for an N number of submodules can be calculated using (5).

$$V_{CN} = \frac{\delta_N}{1-\delta_N} V_{C(N-1)} \tag{5}$$

As seen in Fig. 13, the output voltage of the DC-DC IMMC is the sum of the source voltage and the capacitors voltages. Thus, the output voltage of the IMMC (V_{IMMC}) is expressed in (6).

$$V_{IMMC} = V_s + V_{C1} + V_{C2} + \ldots + V_{CN} \tag{6}$$

The output voltage of the IMMC (V_{IMMC}) is dependent on the capacitors voltages. The capacitor voltages are dependent on the submodules duty ratio as explained in the previous equations. However, it is recommended to operate the duties of the submodules at %50 to ensure the capacitors are balanced.

The size equation of the inductor, as a function of the ripple, is found from the equation of the voltage on the inductor shown in Fig. 12 in the first segment of the cycle. Therefore, (7) represent the sizing equation of the L_1.

$$L_1 = \frac{V_s}{(\frac{\Delta i_{L1}}{\delta_1 T})} \tag{7}$$

The same approach is applied on the rest of the inductors. The sizing equation for L_2, L_3 and L_4 are indicated in (8), (9) and (10) respectively.

$$L_2 = \frac{V_{C1}}{(\frac{\Delta i_{L2}}{\delta_2 T})} \tag{8}$$

$$\mathrm{L_3} = \frac{\mathrm{V_{C2}}}{(\frac{\Delta \mathrm{i_{L3}}}{\delta_3 \mathrm{T}})} \tag{9}$$

$$\mathrm{L_4} = \frac{\mathrm{V_{C3}}}{(\frac{\Delta \mathrm{i_{L4}}}{\delta_4 \mathrm{T}})} \tag{10}$$

Therefore, for an N≠1, The generalized inductor equation for a converter that has an N number of levels is expressed in (11).

$$\mathrm{L}_N = \frac{V_{C(N-1)}}{\frac{\Delta i_{LN}}{\delta_N T}} \tag{11}$$

Fig. 13 defines the currents and the nodes used to derive the capacitors currents equations. Therefore, the capacitors currents I_{C1}, I_{C2}, I_{C3} and I_{C4} are calculated in (12), (13), (14) and (15) respectively.

$$I_{C1} = I_s + \delta_2 I_{L2} - I_{L1} \tag{12}$$

$$I_{C2} = I_s - \delta_1 I_{L1} - (1 - \delta_2) I_{L2} + \delta_3 I_{L3} \tag{13}$$

$$I_{C3} = I_s - \delta_1 I_{L1} - (1 - \delta_3)\mathrm{I_{L3}} + \delta_4 \mathrm{I_{L4}} \tag{14}$$

$$I_{C4} = I_o - (1 - \delta_4) I_{L4} \tag{15}$$

The equation for the first capacitor current is always the same regardless to the number of submodules. The equations for the rest of the capacitors currents can be extended to an N number of capacitors. The general capacitor current equation for I_{C2} to $I_{C(N-1)}$ is found in (16).

$$I_{C(N-1)} = I_s - \delta_1 I_{L1} - \big(1 - \delta_{(N-1)}\big) I_{L(N-1)} + \delta_N I_{LN} \tag{16}$$

The equation for the last capacitor (N) is always expressed in (17).

$$I_{C(N)} = I_o - (1 - \delta_\mathrm{N}) I_{LN} \tag{17}$$

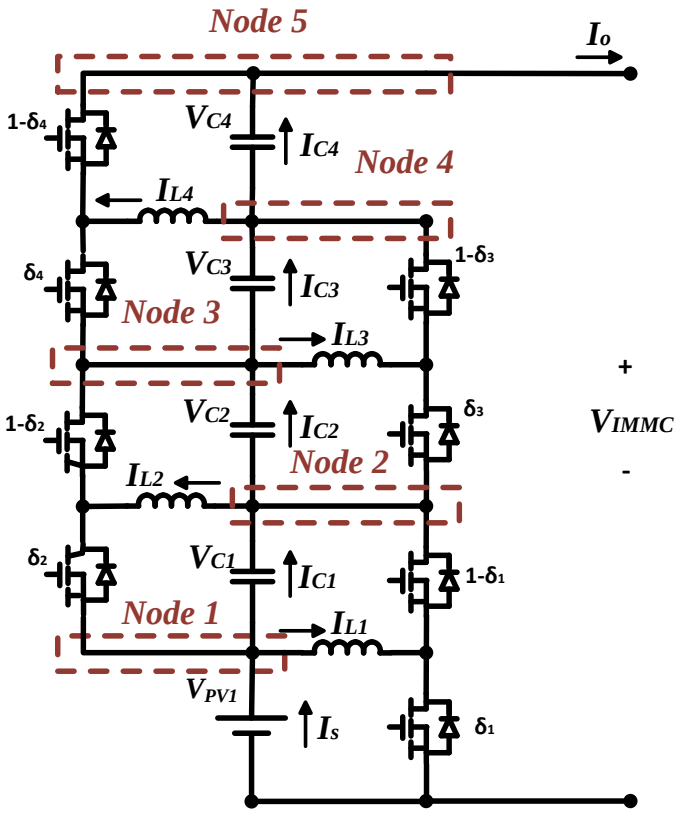

Fig. 13 Nodes to derive the capacitors current equations.

The average capacitor current is always zero. Therefore, average inductors currents can be derived from the capacitor current equations (12), (16) and (17). I_{L1}, I_{C1} and I_{C1} are expressed in (18), (19) and (20) respectively.

$$I_{L1} = I_s + \delta_2 I_{L2} \tag{18}$$

$$I_{LN-1} = \frac{[I_s - \delta_1 I_{L1} + \delta_N I_{LN}]}{1 - \delta_{N-1}} \tag{19}$$

$$I_{LN} = \frac{I_o}{1 - \delta_N} \tag{20}$$

2.2 Proposed DC – AC Topology

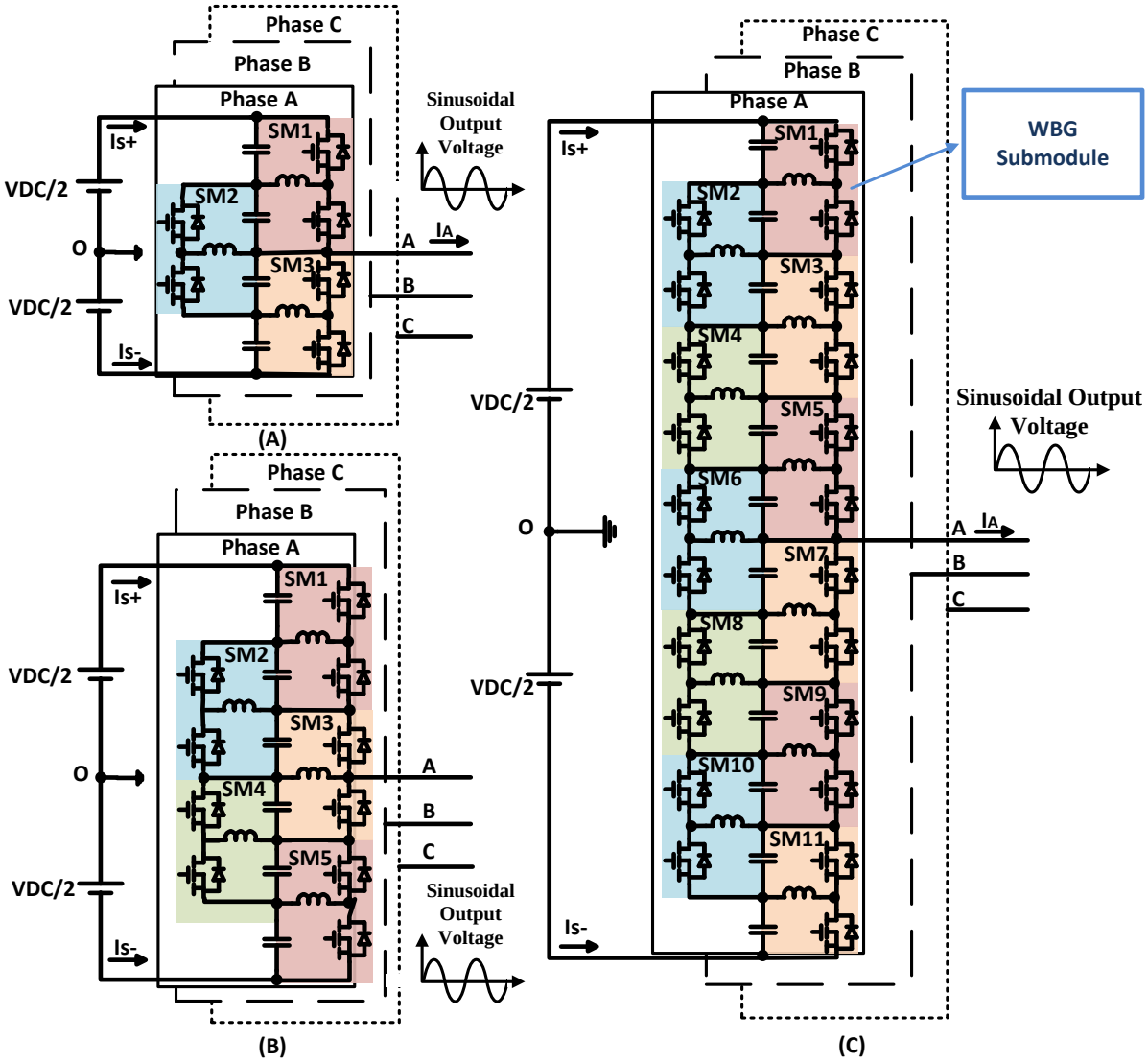

Fig. 14 (A), (B) and (C) shows the proposed IMMC with 3, 5 and 11 submodules respectively.

In this chapter the new DC-AC Interconnected Modular Multilevel Converter (IMMC) is presented. The proposed converter produces a sinusoidal output with adjustable voltage and frequency (v/f) suitable for multitude of applications. The output voltage/frequency can be varied over a wider range. The proposed converter is a promising candidate for applications that require

sinusoidal voltage or current. The proposed converter has the following advantages: sinusoidal output voltage with v/f control; no acoustic noise in motor drives applications; absence of dv/dt related issues due to long wire connections; compact size/weight/volume. The converter is modular in construction, employs high frequency L-C components and semiconductor switches can be stacked for voltage sharing. This chapter details the operating modes, control aspects along with an illustrative design example for a three and eleven submodules converter. Experimental results on a laboratory prototype converter employing 600V GaN and 1200 V SiC devices are discussed in the following chapters.

The IMMC consists of several interconnected modular submodules as seen in Fig. 14. Each submodule is connected across two capacitors and has two wide bandgap switches and an inductor. The DC-AC conversion is achieved by switching on and off capacitors to produce the desired output. On the contrary to several switched capacitors multilevel converters, the proposed IMMC requires small capacitors to filter the switching frequency. The size of the LC components of the converter can be decreased by operating the converter at a high switching frequency.

2.3 Operation and Modulation

The IMMC operation and modulation can be explained using the 3-submodule topology shown in Fig. 15 (A). The capacitors will share the total input DC voltage. Fig. 15 shows the voltage across the capacitors V_{C1}, V_{C2}, V_{C3}, and V_{C4}.

Fig. 16 shows the modulating signal that controls the voltage across the capacitors. The sum of V_{C1}, and V_{C2} or V_{C3}, and V_{C4} shown in Fig. 17 gives a full sinusoidal wave which is the output voltage V_{AO}.

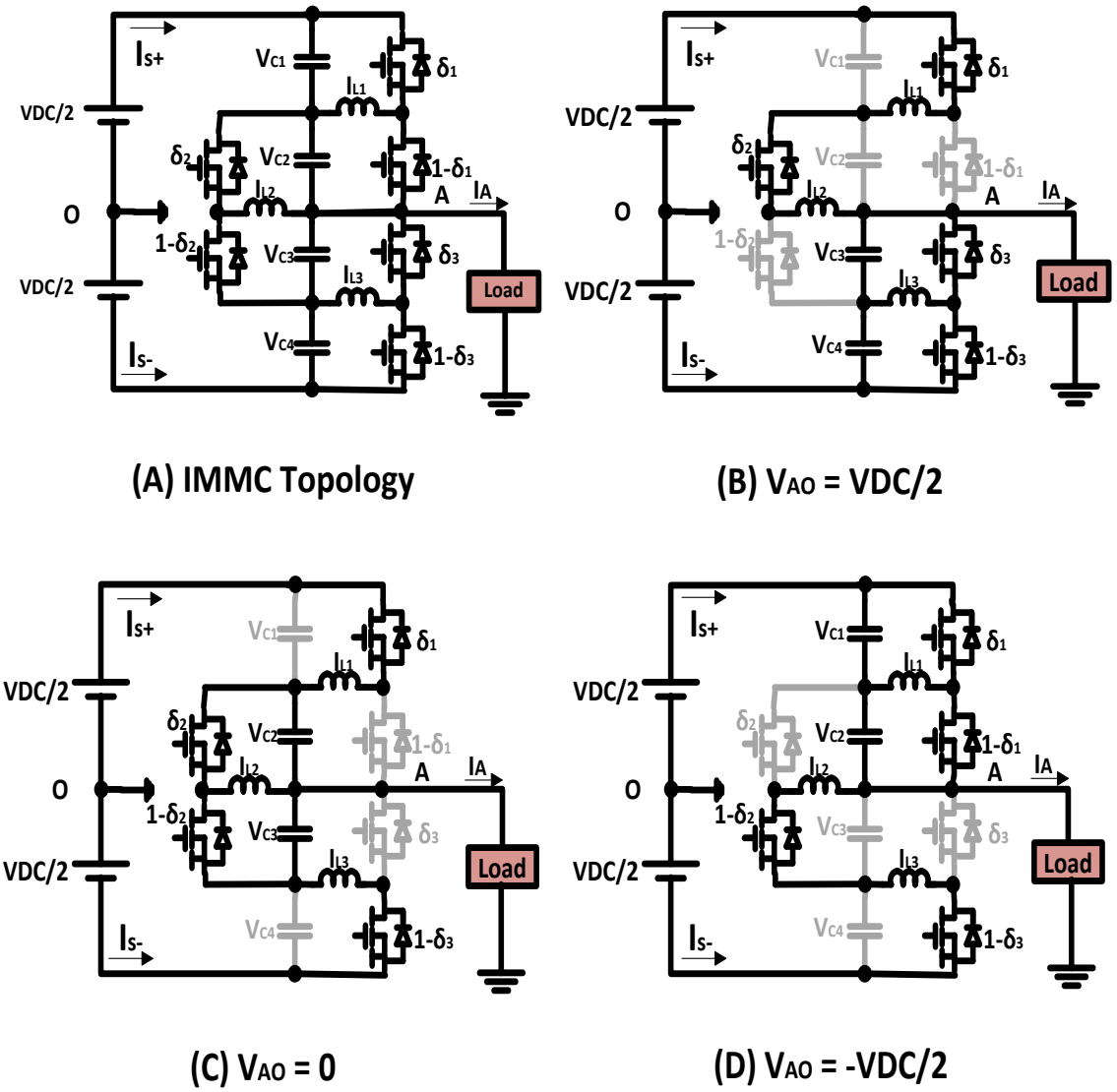

Fig. 15 (A) The proposed IMMC with for different operating modes. (B) The state to generate Vout= VDC/2. (C) The state to generate Vout= 0. (D) The state to generate Vout= -VDC/2. Note: δ is the duty ratio of the submodule.

To illustrate that using the 3 submodules design, two capacitors are bypassed and the other two are in the balancing mode as seen in Fig. 15. For the 11 submodules design, six capacitors will be bypassed and the remaining six are in the balancing mode. The sum of the voltages across the balancing mode capacitors is the sinusoidal voltage.

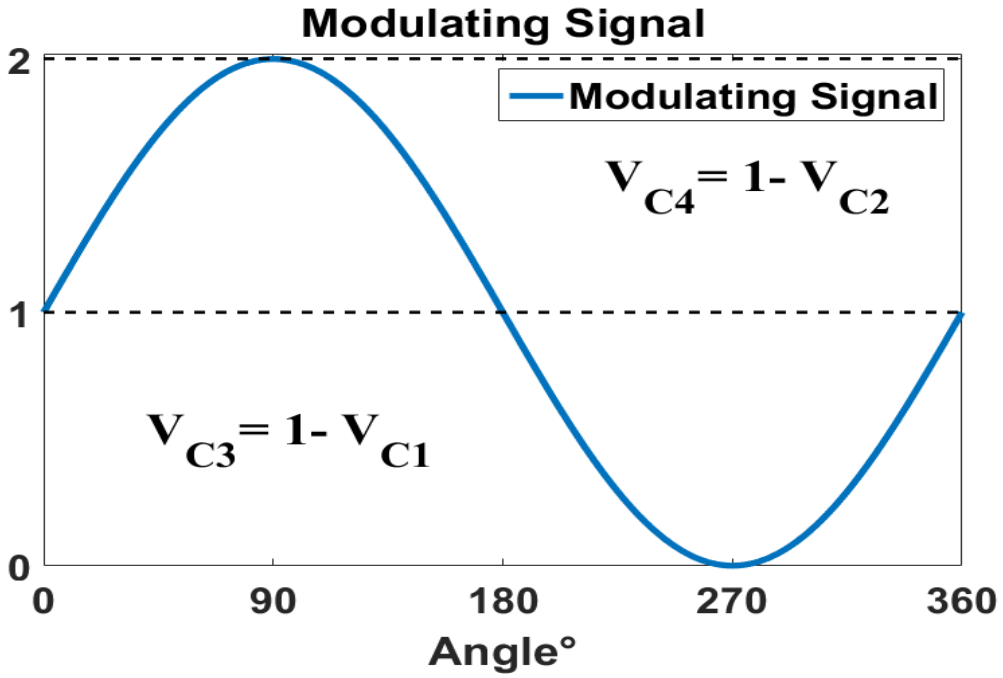

Fig. 16 The modulating signal for the 3 submodules design.

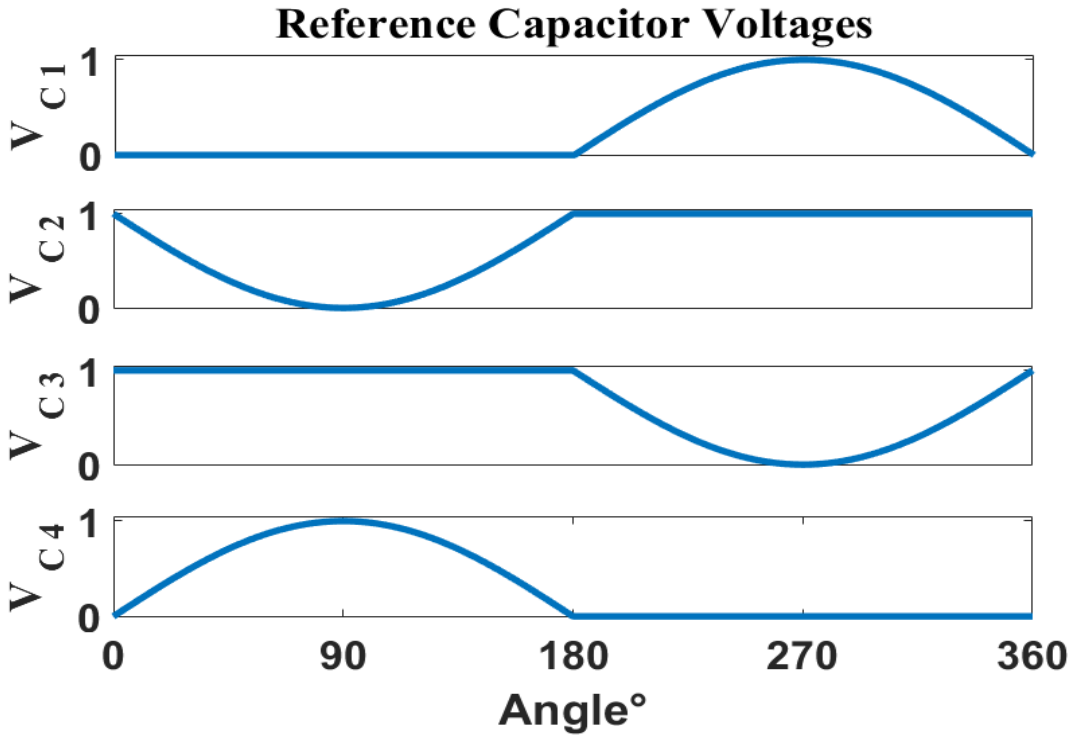

Fig. 17 The reference capacitor voltages for the 3 submodules design. The lower two capacitors reference voltages are one minus the corresponding upper capacitor reference voltage.

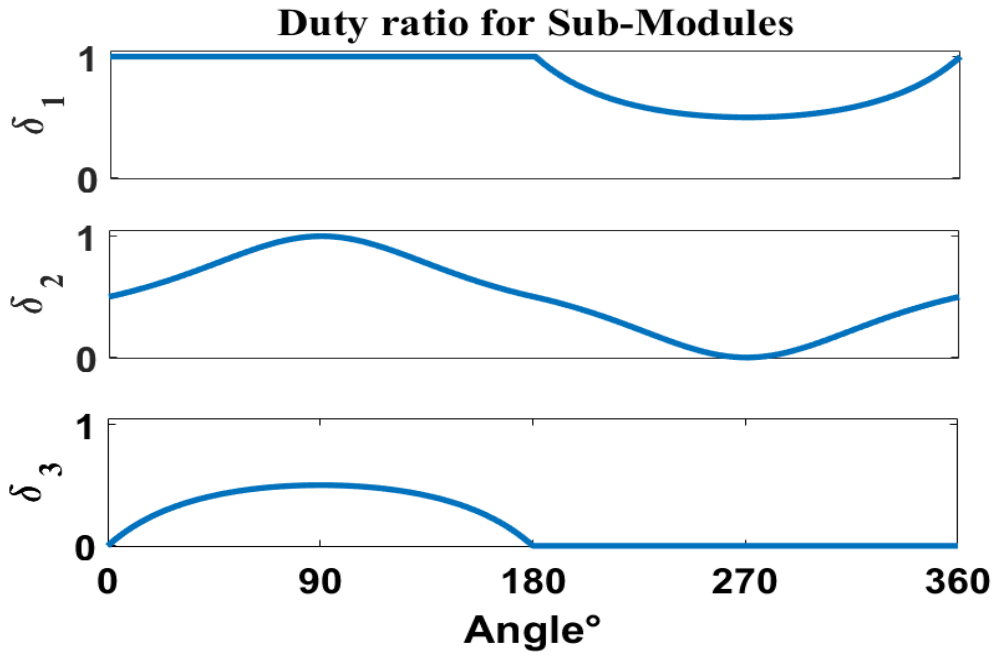

Fig. 18 The duty cycle for the three submodules. $\delta_1$is the duty for SM1; δ_2 for SM2; δ_3 for SM3. The duty is calculated from the ratio of the two reference voltages of the submodules capacitors as illustrated in equation (21) and (22). Each submodule has two switches that work in a complementary manner to each other.

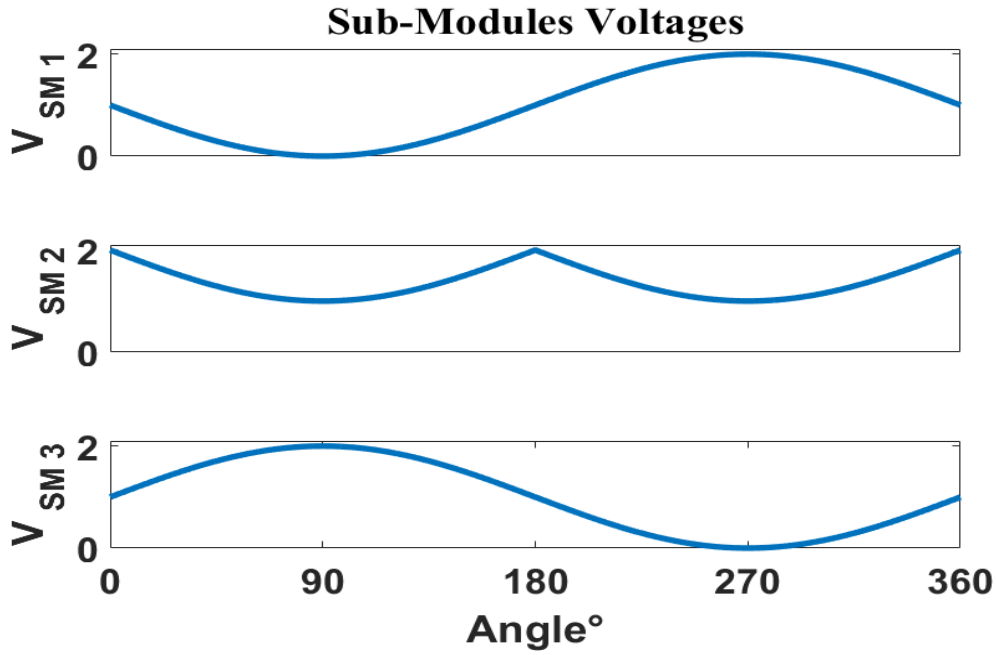

Fig. 19 The submodules voltage with 3 submodules. Note: $V_{SM1} = V_{C1} + V_{C2}$; $V_{SM2} = V_{C2} + V_{C3}$; $V_{SM3} = V_{C3} + V_{C4}$.

Fig. 15 shows the operating states of the proposed IMMC. Two capacitors are equally balanced at a time to generate a certain output voltage. Fig. 15 (B) shows that balancing the V_{C3}, and V_{C4} while bypassing the rest gives $V_{AO} = V_{DC}/2$. When V_{C2} and V_{C3} are balancing, V_{AO}= 0 as in Fig. 15 (C). Moreover, balancing V_{C1} and V_{C2} yields an output voltage of - $V_{DC}/2$.

The modulation technique to produce a sinusoidal output voltage is achieved by slicing the modulating sinusoidal signal according to half the number of capacitors used in the topology. The reference capacitor voltages for all capacitors are generated as shown in Fig. 17. From the reference capacitor voltages, the duty cycle of each submodule is generated using (21) for the upper submodules and (22) for the lower submodules. The factor ϵ is a very small number introduced to the equation to avoid the division by zero. The term (n) in (21) and (22) is the submodule's number and N is the number of capacitors +1.

The duties for the upper submodules for $0 < \mathrm{n} < \frac{\mathrm{N}}{2}$:

$$\delta_{\mathrm{n}} = 1 - \frac{V_{C(n+1)}}{V_{C(n)} + V_{C(n+1)} + \epsilon} \tag{21}$$

The duties for the lower submodules for $\frac{\mathrm{N}}{2} < \mathrm{n} \leq \mathrm{N} - 2$:

$$\delta_{\mathrm{n}} = \frac{V_{C(n)}}{V_{C(n)} + V_{C(n+1)} + \epsilon} \tag{22}$$

As shown in Fig. 18, the duties smoothly change between 0 that bypasses the lower capacitor of the submodule, 0.5 that balances the two submodules capacitors and 1 that bypasses the upper capacitor of the submodule. The submodules voltages are illustrated in Fig. 19.

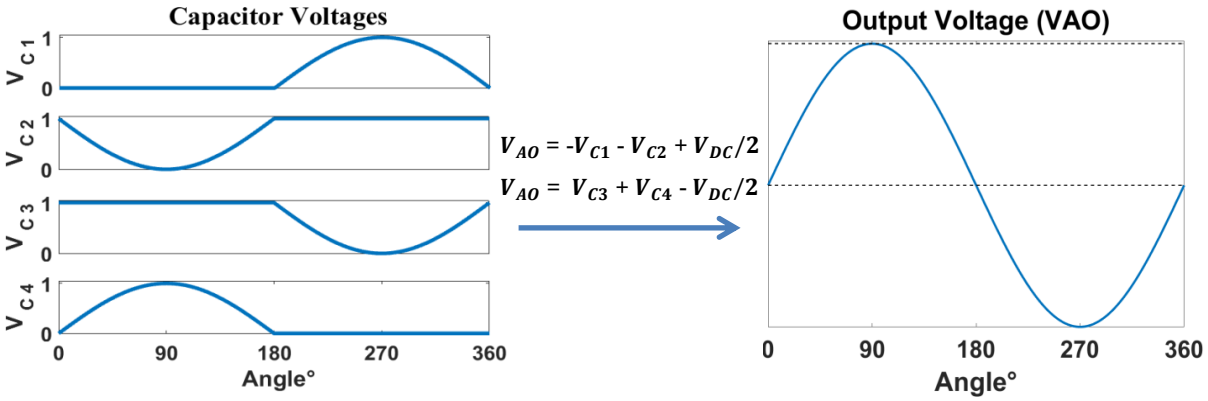

Fig. 20 shows how the converter works. Each capacitor is switched to have a slice of the sine wave and the output voltage is the sum of two capacitors minus $V_{DC}/2$.

In summary, the output voltage is the sum of the voltage of two capacitors minus half the DC link voltage as seen in Fig. 20. Therefore, producing a pure sinusoidal output with any frequency (it can be as low as 1 Hz) is possible by synthesizing the desired waveform shape and frequency on the capacitors.

The mechanism of the five submodules IMMC is explained as well to strengthening the understanding of how the converter works for any number of submodules. Fig. 21 shows the states to generate the major values of the output sine wave (V_{DC}, 0 and -V_{DC}). Each state represents a point on the sinusoidal waveform. Fig. 22 shows the modulating signal used in the modulation of the converter. The modulating signal is sliced according to half the number of the capacitors in the converter. For example, the five submodules IMMC has six capacitors in total; therefore, the modulating signal is sliced to three slices as shown in Fig. 22. The upper three capacitors will have reference voltages that are opposite to the three lower capacitors as seen in Fig. 23. The duty ratio of each submodule is calculated from equation (21) and (22) to result the duty ratios seen in Fig. 24.

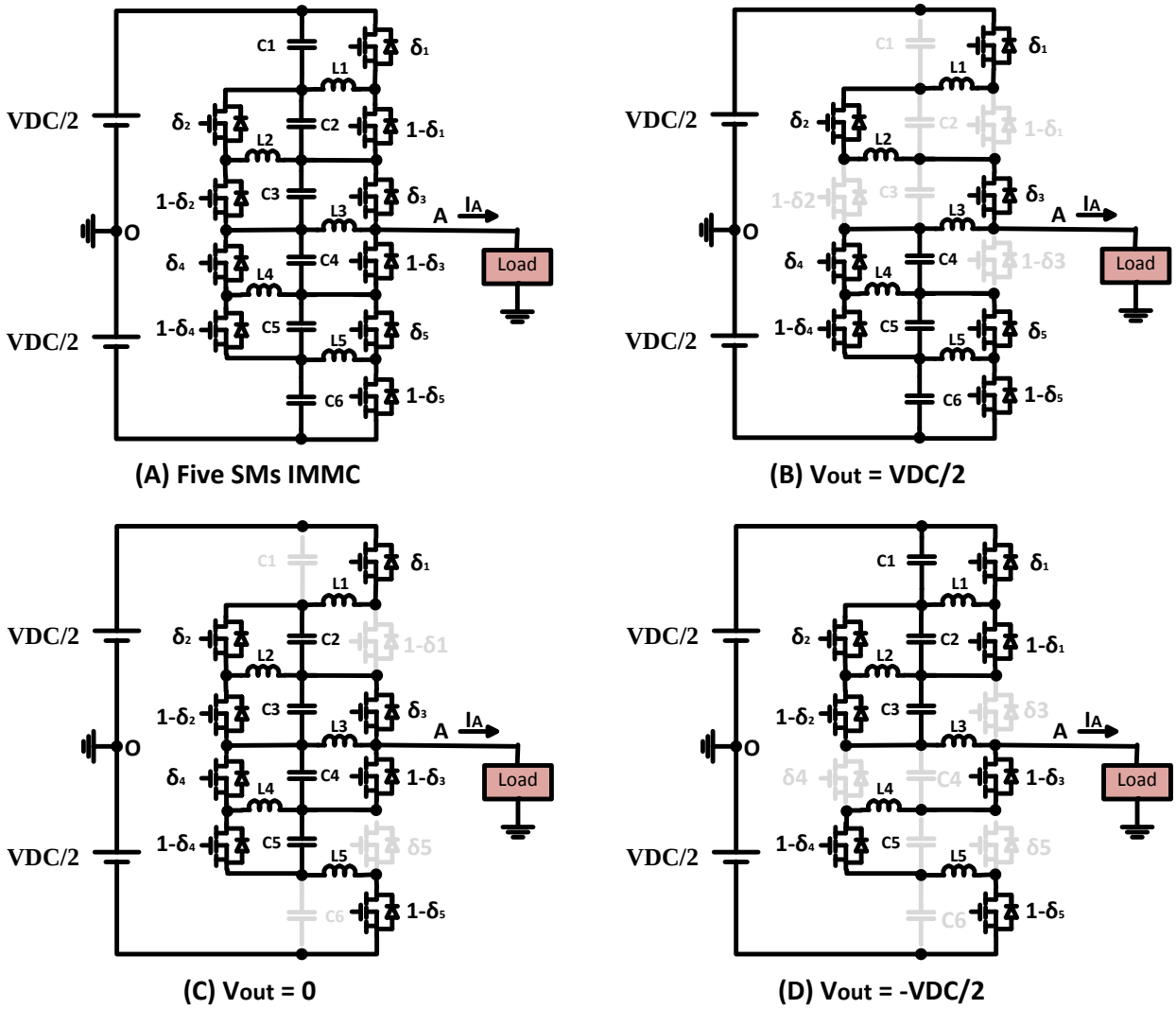

Fig. 21 (A) The proposed IMMC with five submodules. (B) The state to generate Vout= VDC/2. (C) The state to generate Vout= 0. (D) The state to generate Vout= -VDC/2. Note: δ is the duty ratio of the submodule.

Fig. 25 shows the submodules voltages of the five submodules IMMC. Each submodule's voltage is the sum of the two capacitors voltages connected to the submodule. For example, the voltage across SM_1 (V_{SM1}) is the sum of V_{C1} and V_{C2}. The same principal is applied to the rest of the submodules as shown in Fig. 25.

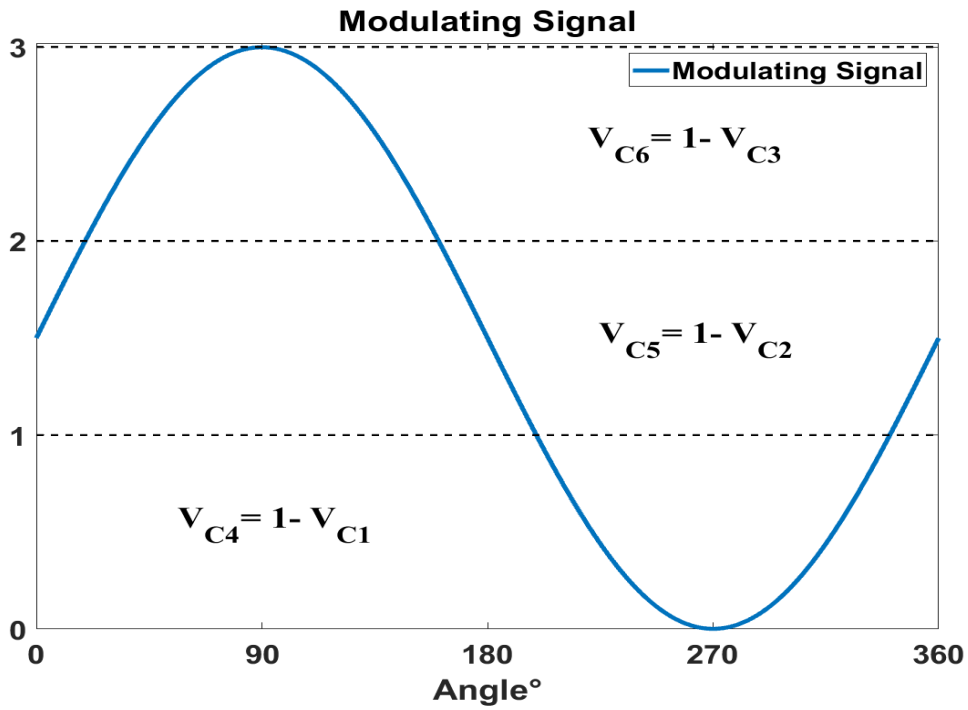

Fig. 22 The modulating signal for the 5 submodules design.

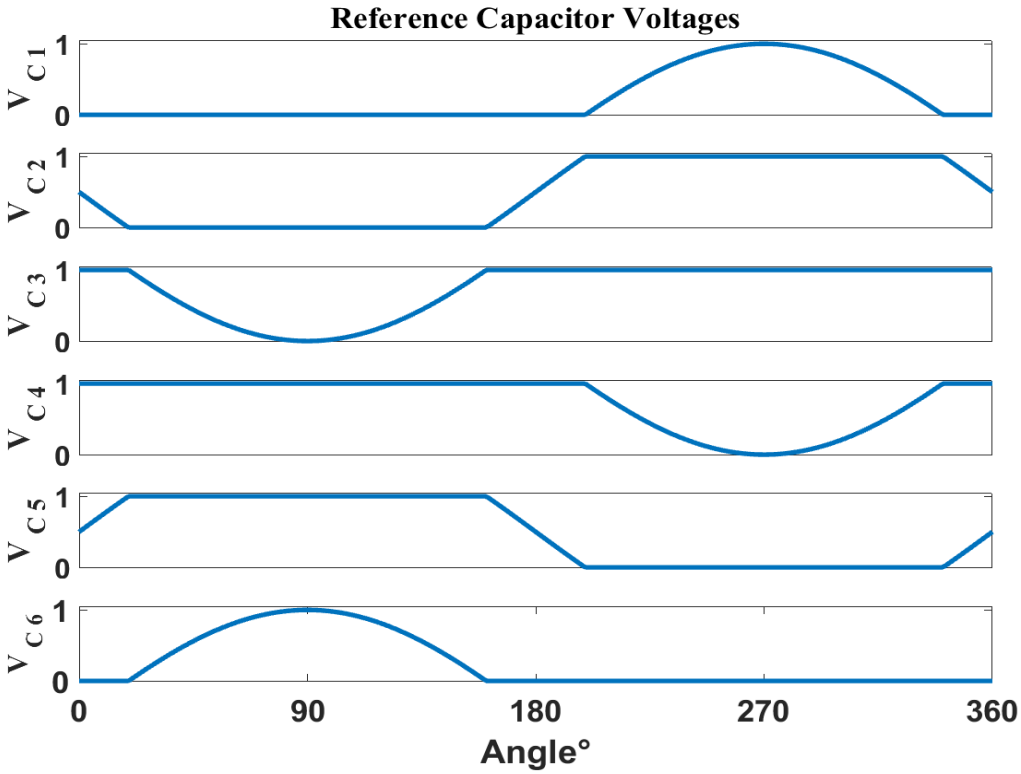

Fig. 23 The reference capacitor voltages for the 3 submodules design. The lower two capacitors reference voltages are one minus the corresponding upper capacitor reference voltage.

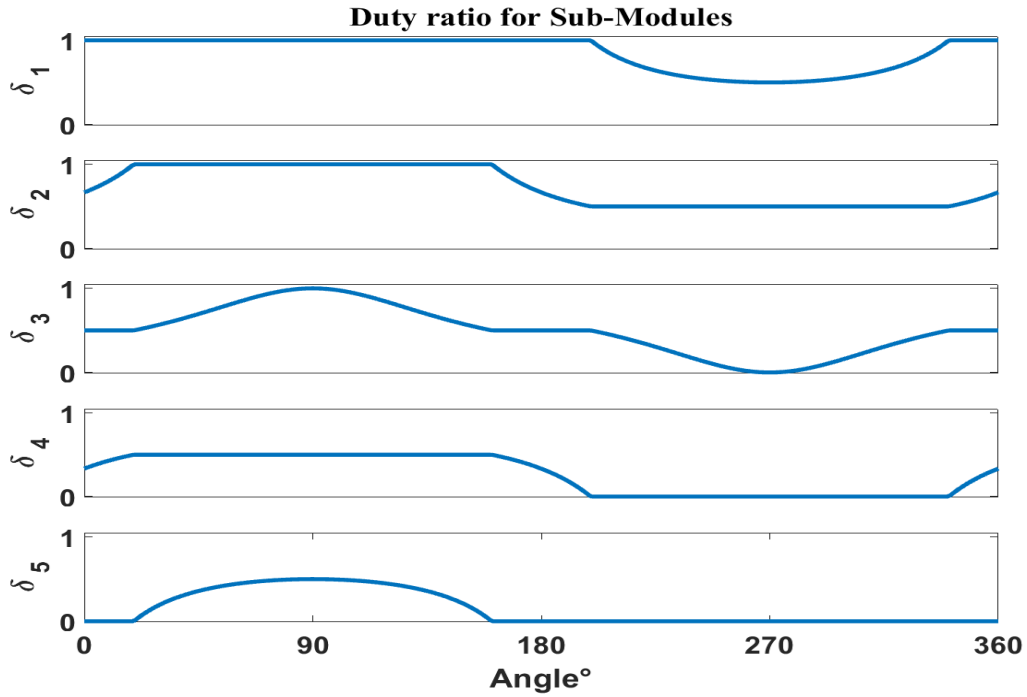

Fig. 24 The duty cycle for the three submodules. $\delta_1$is the duty for SM1; δ_2 for SM2; δ_3 for SM3 ; δ_4 for SM4;. δ_5 for SM5.

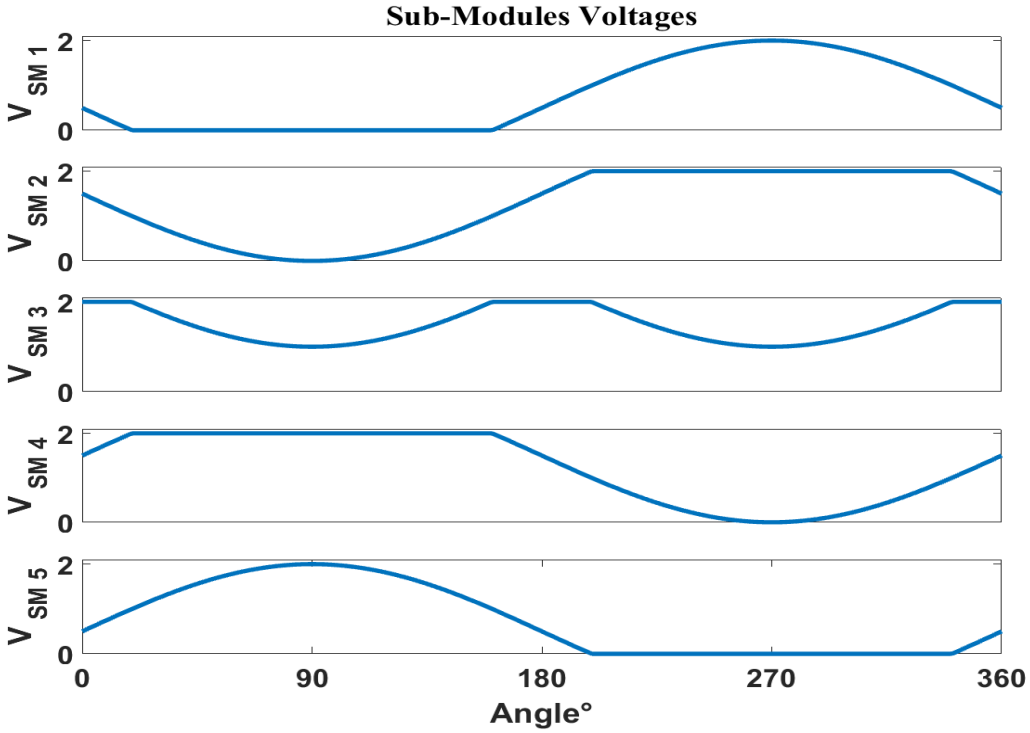

Fig. 25 The submodules voltage with 3 submodules. Note: $V_{SM1} = V_{C1} + V_{C2}$; $V_{SM2} = V_{C2} + V_{C3}$; $V_{SM3} = V_{C3} + V_{C4}$; $V_{SM4} = V_{C4} + V_{C5}$; $V_{SM5} = V_{C5} + V_{C6}$.

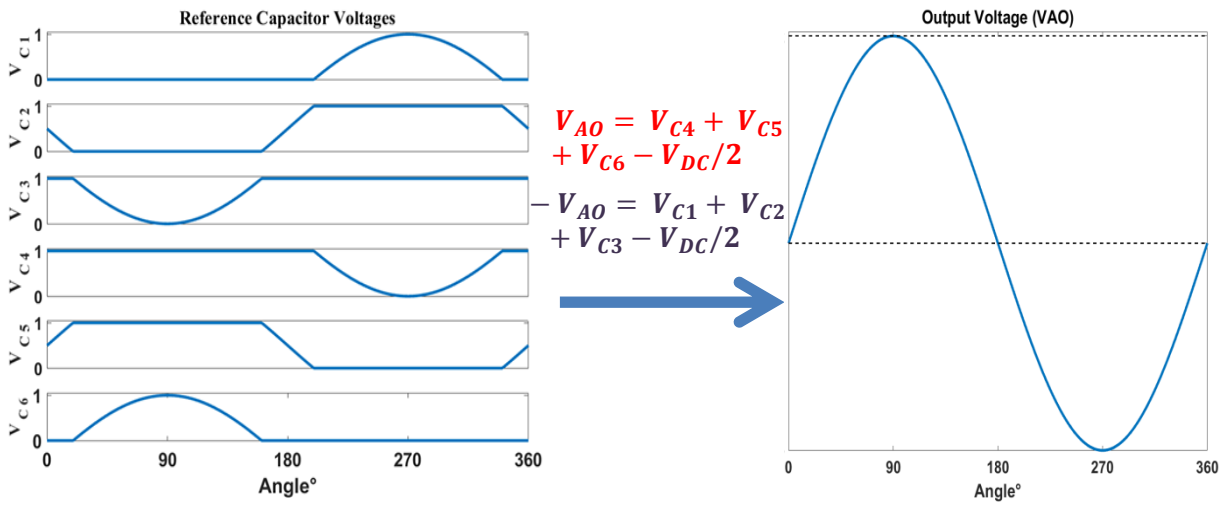

Fig. 26 The mechanism of the five submodule IMMC. Each capacitor is switched to have a slice of the sine wave and the output voltage is the sum of two capacitors minus VDC/2.

Fig. 26 summarizes the basic principal of how the five submodules IMMC works. The principal is similar to the three submodules IMMC. Each capacitor voltage is synthesized to have a slice of a sine wave. Therefore, the sum of the slices minus the half the DC link (for the one phase inverter) is a full sine wave at the output.

2.4 DC-AC IMMC Circuit Analysis

The modeling of the topology is derived for the three submodules design seen in Fig. 14 (A) and then extended to an arbitrary number of submodules similar to Fig. 14 (B) and (C). For modeling purposes, the topology is subdivided into four nodes and the dc-link voltage with center point ground is shown. The currents of the capacitors are derived by applying the Kirchhoff's Current Law (KCL) at the nodes defined in Fig. 27. The currents of the capacitors are written in (23), (24), (25) and (26).

$$\mathrm{I_{C1}} = C\frac{dV_{C1}}{dt} = -\delta_1 * \mathrm{I_{L1}} + \mathrm{I_{s+}} \tag{23}$$

$$\mathrm{I_{C2}} = C\frac{dV_{C2}}{dt} = (1-\delta_1) * \mathrm{I_{L1}} - \delta_2 * \mathrm{I_{L2}} + \mathrm{I_{s+}} \tag{24}$$

$$\mathrm{I_{C3}} = C\frac{dV_{C3}}{dt} = (1-\delta_2) * \mathrm{I_{L2}} - \delta_3 * \mathrm{I_{L3}} - \mathrm{I_{s-}} \tag{25}$$

$$\mathrm{I_{C4}} = C\frac{dV_{C4}}{dt} = (1-\delta_3) * \mathrm{I_{L3}} - \mathrm{I_{s-}} \tag{26}$$

The currents for the inductors (submodules) written in (27), (28) and (29) are found by rearranging (23), (25) and (26).

$$\mathrm{I_{SM1}} = \mathrm{I_{L1}} = \frac{\mathrm{I_{s+}} - \mathrm{I_{C1}}}{\delta_1} \tag{27}$$

$$I_{SM2} = I_{L2} = \frac{I_{C3}}{1-\delta_2} + \frac{\delta_3}{(1-\delta_2)(1-\delta_3)} I_{C4} + \frac{1+\delta_3}{(1-\delta_2)(1-\delta_3)} I_{s-} \tag{28}$$

$$\mathrm{I_{SM3}} = \mathrm{I_{L3}} = \frac{\mathrm{I_{C4}} + \mathrm{I_{s-}}}{1-\delta_3} \tag{29}$$

Similarly, the converter is subdivided into 6 loops that contain an inductor as seen in Fig. 28. Kirchhoff's Voltage Law (KVL) is applied to the loops to find the inductors voltages. The voltages of the inductors for the topology shown in Fig. 28 are represented in (30), (31) and (32).

$$\mathrm{V_{L1}} = L\frac{di_{L1}}{dt} = \delta_1 * V_{C1} + (\delta_1 - 1) * V_{C2} \tag{30}$$

$$\mathrm{V_{L2}} = L\frac{di_{L2}}{dt} = \delta_2 * V_{C2} + (\delta_2 - 1) * V_{C3} \tag{31}$$

$$\mathrm{V_{L3}} = L\frac{di_{L3}}{dt} = \delta_3 * V_{C3} + (\delta_3 - 1) * V_{C4} \tag{32}$$

Increasing the number of submodules reduces the voltage stress on the devices allowing lower device ratings as shown in Fig. 14. Thus, (23), (24), (25) and (26) are expressed in the matrix format as shown in (33) and then extended to an N number of submodules as seen in (34). Similarly, (30), (31) and (32) are written in the matrix format shown in (35) and then extended to an N number of submodules as shown in (36).

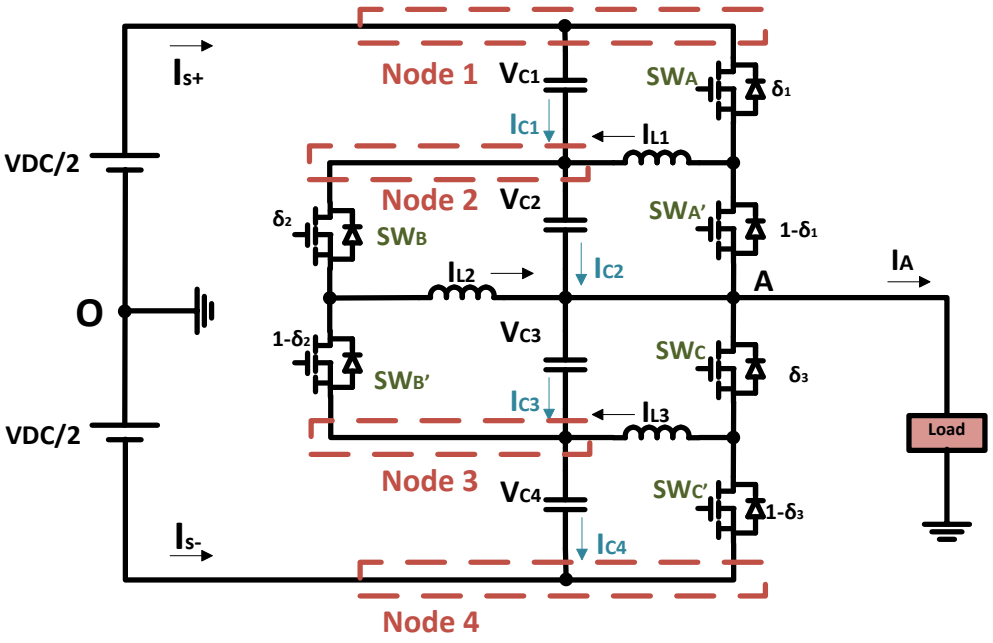

Fig. 27 Nodes to obtain the capacitors current equations.

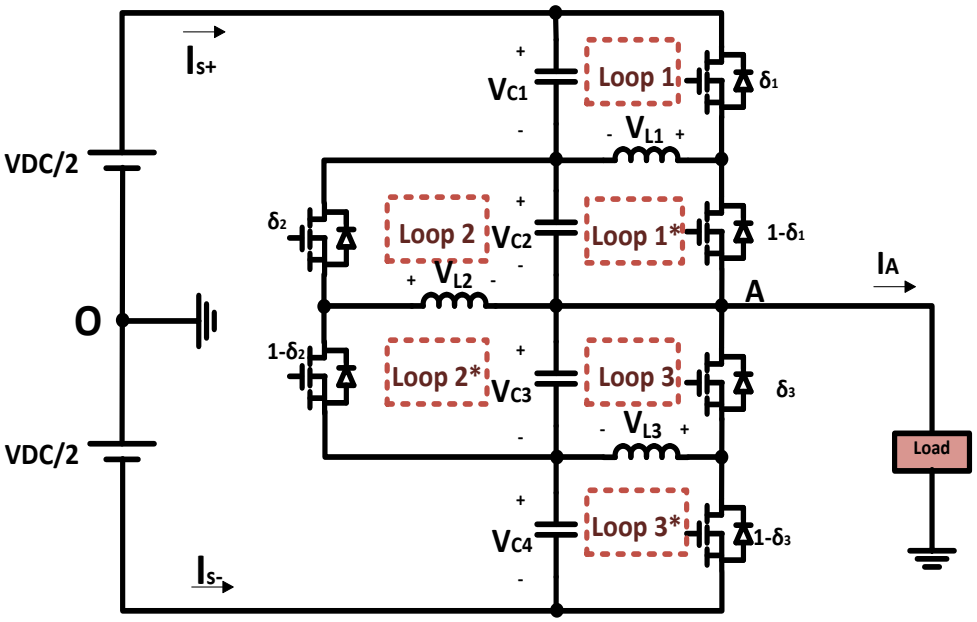

Fig. 28 Loops to obtain the inductors voltage equations.

$$\begin{bmatrix} C\frac{dVC_1}{dt} \\ C\frac{dVC_2}{dt} \\ C\frac{dVC_3}{dt} \\ C\frac{dVC_4}{dt} \end{bmatrix} = \begin{bmatrix} -\delta_1 & & \\ 1-\delta_1 & -\delta_2 & \\ & 1-\delta_2 & -\delta_3 \\ & & 1-\delta_3 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \end{bmatrix} + \begin{bmatrix} I_{s+} \\ I_{s+} \\ -I_{s-} \\ -I_{s-} \end{bmatrix} \quad (33)$$

For N number of Submodules

$$\begin{bmatrix} C\frac{dVC_1}{dt} \\ C\frac{dVC_2}{dt} \\ C\frac{dVC_3}{dt} \\ \vdots \\ C\frac{dVC_{\frac{N}{2}}}{dt} \\ C\frac{dVC_{\frac{N}{2}+1}}{dt} \\ \vdots \\ C\frac{dVC_{N-2}}{dt} \\ C\frac{dVC_{N-1}}{dt} \\ C\frac{dVC_N}{dt} \end{bmatrix} = \begin{bmatrix} -\delta_1 & & & & & & & & \\ 1-\delta_1 & -\delta_2 & & & & & & & \\ & 1-\delta_2 & -\delta_3 & & & & & & \\ & & \vdots & \vdots & & & & & \\ & & & 1-\delta_{\frac{N}{2}-1} & -\delta_{\frac{N}{2}} & & & & \\ & & & & 1-\delta_{\frac{N}{2}} & -\delta_{\frac{N}{2}+1} & & & \\ & & & & & \vdots & \vdots & & \\ & & & & & 1-\delta_{N-3} & -\delta_{N-2} & & \\ & & & & & & 1-\delta_{N-2} & -\delta_{N-1} & \\ & & & & & & & 1-\delta_{N-1} & \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ \vdots \\ i_{L\frac{N}{2}} \\ \vdots \\ i_{LN-3} \\ i_{LN-2} \\ i_{LN-1} \end{bmatrix} + \begin{bmatrix} I_{s+} \\ I_{s+} \\ I_{s+} \\ \vdots \\ I_{s+} \\ -I_{s-} \\ \vdots \\ -I_{s-} \\ -I_{s-} \\ -I_{s-} \end{bmatrix} \quad (34)$$

$$\begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ L\frac{di_{L3}}{dt} \end{bmatrix} = \begin{bmatrix} \delta_1 & \delta_1 - 1 & & \\ & \delta_2 & \delta_2 - 1 & \\ & & \delta_3 & \delta_3 - 1 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \end{bmatrix} \tag{35}$$

For N number of Submodules

$$\begin{bmatrix} L\frac{di_{L1}}{dt} \\ L\frac{di_{L2}}{dt} \\ L\frac{di_{L3}}{dt} \\ \vdots \\ L\frac{di_{L\frac{N}{2}}}{dt} \\ \vdots \\ L\frac{di_{LN-3}}{dt} \\ L\frac{di_{LN-2}}{dt} \\ L\frac{di_{LN-1}}{dt} \end{bmatrix} = \begin{bmatrix} \delta_1 & \delta_1 - 1 & & & & & & & \\ & \delta_2 & \delta_2 - 1 & & & & & & \\ & & \delta_3 & \delta_3 - 1 & & & & & \\ & & & \vdots & \vdots & & & & \\ & & & \delta_{\frac{N}{2}} & \delta_{\frac{N}{2}} - 1 & & & & \\ & & & & \vdots & \vdots & & & \\ & & & & & \delta_{N-3} & \delta_{N-3} - 1 & & \\ & & & & & & \delta_{N-2} & \delta_{N-2} - 1 & \\ & & & & & & & \delta_{N-1} & \delta_{N-1} - 1 \end{bmatrix} \begin{bmatrix} V_{C1} \\ V_{C2} \\ V_{C3} \\ \vdots \\ V_{C\frac{N}{2}} \\ V_{C\frac{N}{2}+1} \\ \vdots \\ V_{CN-2} \\ V_{CN-1} \\ V_{CN} \end{bmatrix} \tag{36}$$

The normalized current rating of the submodules with respect to the output current is calculated in (37). The submodules current RMS ratings are found by dividing the RMS value of the inductor current ($I_{L(N)}$) by the RMS value of the output current (I_A) shown in Fig. 27.

$$\mathrm{I_{SM(N)-pu}} = \frac{I_{L(N)-RMS}}{I_{A-RMS}} \tag{37}$$

The Normalized RMS current of the submodules (as a function of the RMS output current) of the 3, 5 and 11 submodules IMMC are shown in Fig. 29, Fig. 30 and Fig. 31. The middle submodule has the highest current ratings. Increasing the number of submodules decreases the voltage stress but increases the current stress.

The voltage stress on the devices is reduced when the number of submodules increases. Table 2 summarizes the voltage stress on the devices with respect to the number of submodules.

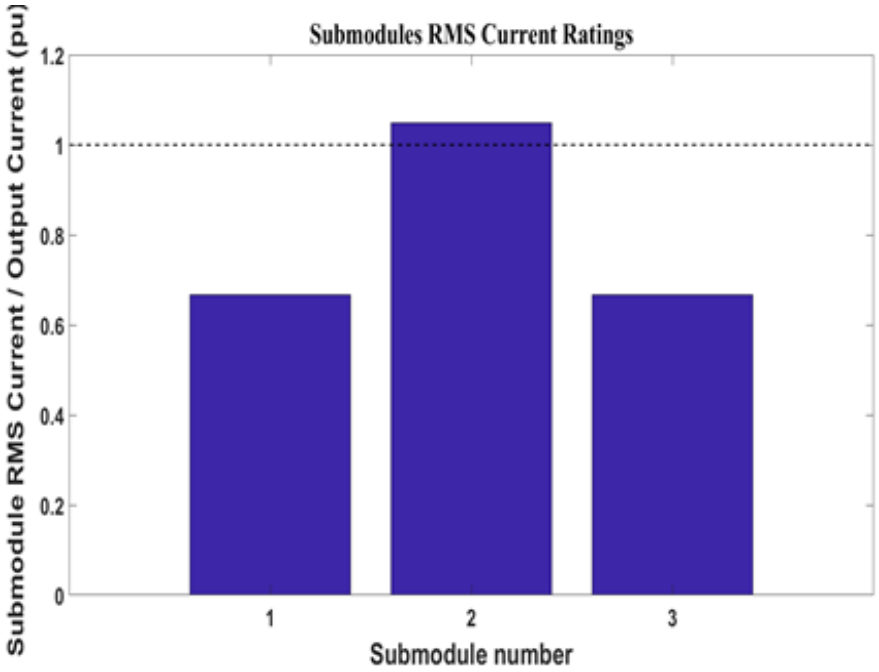

Fig. 29 Submodules current RMS rating as a function of the RMS output current in per unit for the 3 submodules design.

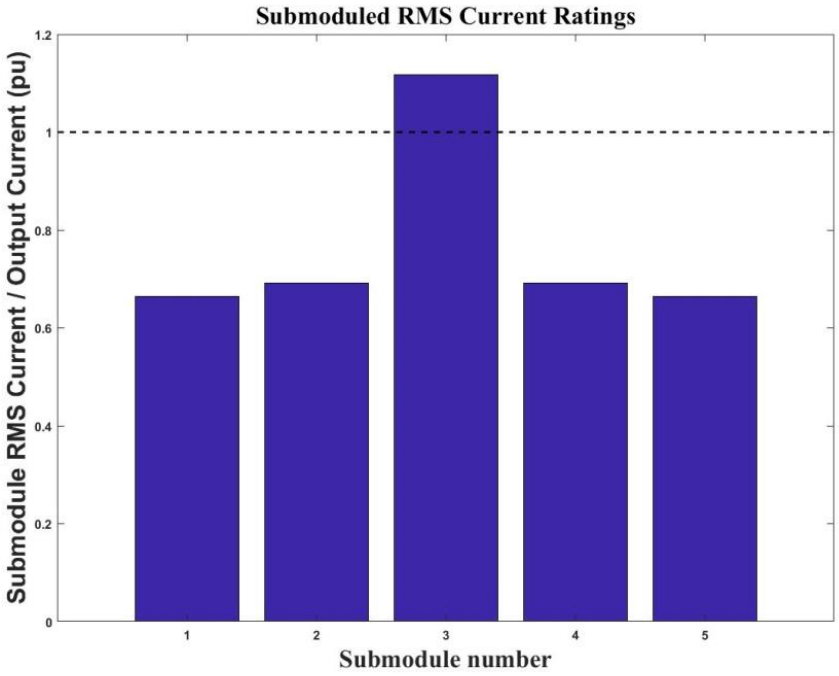

Fig. 30 Submodules current RMS rating as a function of the RMS output current in per unit for the 5 submodules design.

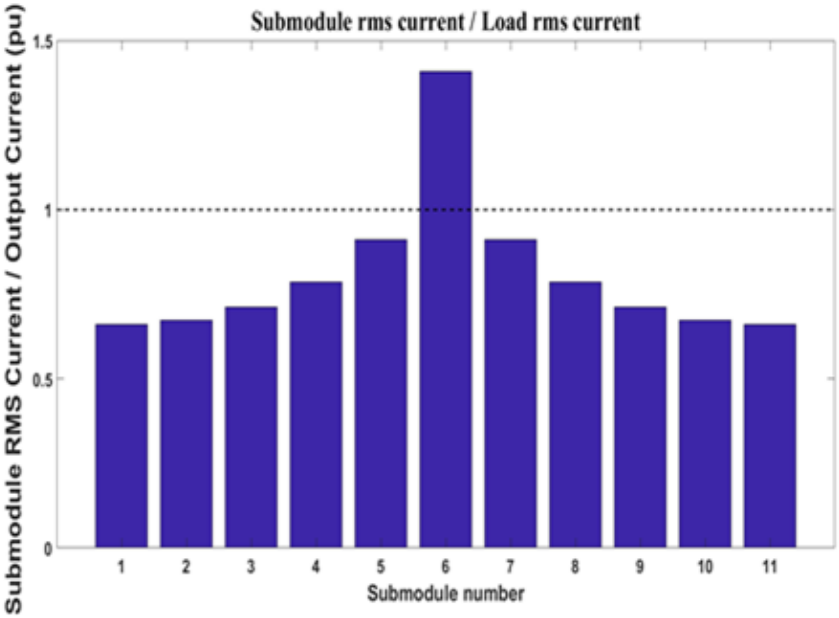

Fig. 31 Submodules current RMS rating as a function of the RMS output current in per unit for the 11 submodules design

Table 2 voltage stress on switches with respect to the number of SMs

Number of SMs	**Blocking voltage**	**Total # of Cs**	**Total # of Ls**
3	VDC	4	3
5	$\frac{2\,VDC}{3}$	6	5
7	$\frac{VDC}{2}$	8	7
9	$\frac{2\,VDC}{5}$	10	9
11	$\frac{VDC}{3}$	12	11
13	$\frac{2\,VDC}{7}$	14	13
15	$\frac{VDC}{4}$	16	15
17	$\frac{2\,VDC}{9}$	18	17
19	$\frac{VDC}{5}$	20	19
N	$\frac{4}{N+1}VDC$	N+1	N

2.5 Comparison

Table 3 compares the number of switches, diodes, passive components, and size index for the IMMC to the major multilevel topologies which are Neutral Point Clamped Converter (NPC), Flying Capacitor Converter (FCC), Modular Multilevel Converter (MMC), and the Cascaded H-Bridge Converter (CHB).

Table 3 Comparison between single phase IMMC and popular multilevel existing topologies.

Number of levels = n	**NPC [7, 12, 13]**	**FCC [14, 15]**	**MMC [8, 16]**	**Proposed IMMC**	**CHB [17, 18]**
Number of modules	-	-	$2(n-1)$	$2(n-1.5)$	$(n-1)/2$
Number of switches	$2(n-1)$	$2(n-1)$	$4(n-1)$	$4(n-1.5)$	$2(n-1)$
Number of Clamping Diodes	$(n-1)(n-2)$	-	-	-	-
Number of capacitors	$n-1$	$\frac{1}{2}\mathrm{n}(n-1)$	$2(n-1)$	$2(n-1)$	$(n-1)/2$
Number of inductors	-	-	2	$2(n-1.5)$	-
Total Components count	$(n\text{^}2-1)$	$(n-1)(\mathrm{n}+4)/2$	$6(\mathrm{n}-1)+2$	$8\mathrm{n}-11$	$2.5(n-1)$
Capacitance ratio index	34	1	200	1	100
Capacitor Overall size index	$34(n-1)$	$\frac{1}{2}\mathrm{n}(n-1)$	$400(n-1)$	$2(n-1)$	$50(n-1)$
Inductance ratio index	-	-	100	1	-
Inductance Overall size index	-	-	200	$2(n-1.5)$	-

The total number of components is defined as an equation by adding all components together as function of the number of levels. Fig. 32 plots the total number of components needed to achieve a certain number of levels for each one of the topologies. It is important to note that the IMMC does not generate a multilevel output but a pure sinewave that does not need

filtering. The number of levels for the IMMC is the number of submodules which is half the number of capacitors +1 and it is just used as a common base for comparison.

The CHB displays a superior performance in terms of the total number of components needed. It requires the lowest number of components for all numbers of levels. However, CHB requires multi-winding transformers and rectifier circuits to provide the DC for each submodule which makes the CHB expensive and bulky [19].

The NPC needs the highest number of components for number of levels larger than 7 levels. Therefore, the NPC is an unpractical solution [20, 21].

The IMMC has a linear relationship between the number of levels and components. However, with only 3 submodules the quality of the output is a pure sinusoidal wave which the other multilevel cannot generate without a filter. Therefore, it is recommended to operate the IMMC with a small number of submodules if the quality of the output is the only concern.

The overall capacitor index of all topologies is shown in Fig. 33. The IMMC has the least capacitor size index for almost all number of levels. This is because the capacitors are only used to filter the high switching frequency. Therefore, the IMMC reduces the overall capacitance requirements ensuring a high-power density operation.

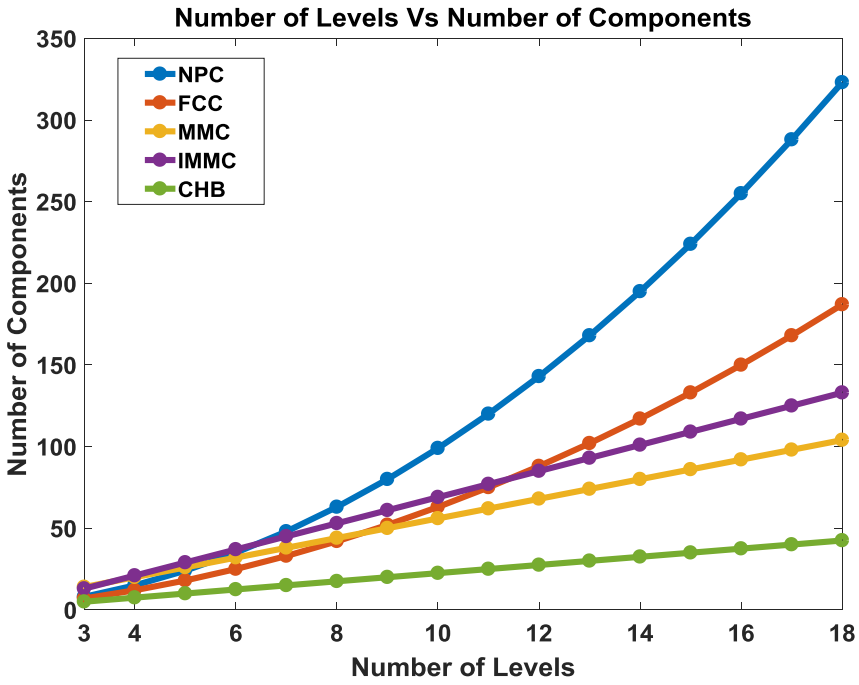

Fig. 32 Number of levels VS number of components.

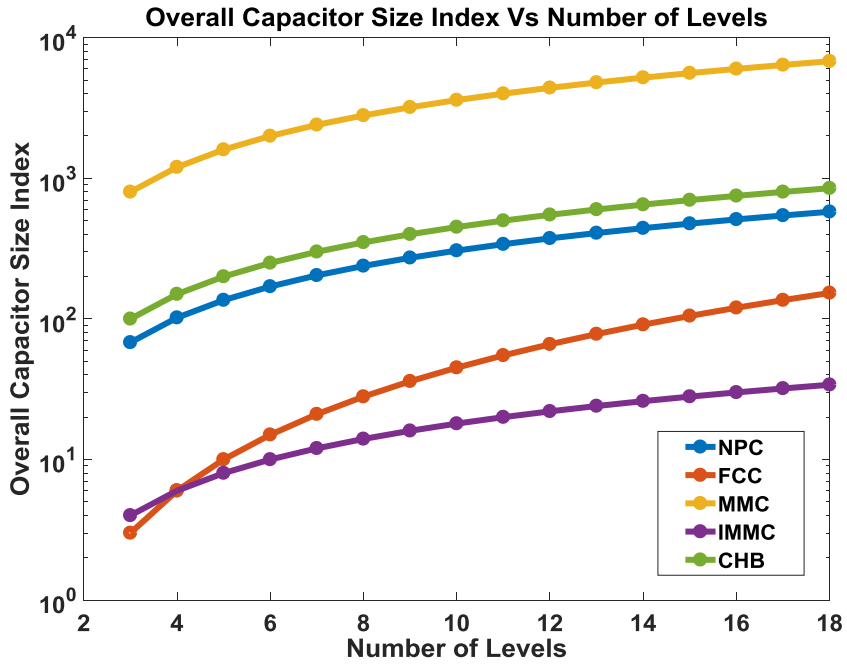

Fig. 33 Number of levels VS overall capacitor size index.

Table 4 Size Comparison

	MMC	**IMMC**	**CHB**	**FCC**	**NPC**
Capacitor Voltage Ripple ΔV	5%	1%	5%	1%	5%
Inductor Current Ripple ΔI	5%	1%	-	-	-
Switching Frequency f_s	6kHz	60kHz	6kHz	60kHz	6kHz
Output Frequency f_o	60Hz	60Hz	60Hz	60Hz	60Hz
Inductor Current Ripple Frequency $f_{\Delta IL}$	120Hz	60kHz	-	-	-
Capacitor Current Frequency f_{Ic}	60Hz	60kHz	120Hz	60kHz	360Hz
Capacitor Voltage Ripple Frequency $f_{\Delta V}$	60Hz	60kHz	120Hz	60kHz	360Hz
Capacitor Ratio Index	200	1	100	1	34

A detailed comparison between the proposed converter and the other multilevel converter topologies is established in Table 4. The approach to compare the passive elements size is to study the ripple on the capacitor and the inductor. After that, the size needed to minimize the ripple to an acceptable range is calculated. The size comparison is discussed for the proposed converter and the MMC converter seen in Fig. 6 to illustrate the comparison process. The same approach can be taken for the other multilevel topologies.

The capacitance ratio index in Table 3 is a term introduced to compare the capacitor size requirement for each to topology. Table 4 defines the parameters for the proposed IMMC and MMC with the following assumptions: the maximum allowed ripple on the capacitor for the IMMC and MMC are 1% and 5% respectively; the proposed converter is switching at 60 kHz.

The choice of 5% allowed ripple of the MMC is given a higher margin because an output filter is used with the MMC. On the other hand, the IMMC does not require an output filter; thus, the ripple must be minimized to generate a high quality sinusoidal output voltage. The capacitor of the MMC has a low frequency ripple component (60 Hz) and the capacitors of proposed converter are used to filter the high switching frequency (60kHz). Therefore, the capacitance ratio index is calculated in (38):

$$\text{Capacitor Ratio Index} = \frac{C_{MMC}}{C_{IMMC}} = \frac{f_{Ic-IMMC} * \Delta V_{IMMC}}{f_{Ic-MMC} * \Delta V_{MMC}} = \frac{60000\ Hz * 1\%}{60\ Hz * 5\%} = 200 \quad (38)$$

The size of the capacitor needed to filter the 60 Hz ripple of the MMC is 200 times the capacitor size needed for the proposed IMMC.

The same approach can be used for the inductor ratio index. The inductor in the MMC is used to suppress the circulating current which is a negative sequence current at double-fundamental frequency (120Hz). On the other hand, the ripple in the inductor current in the IMMC is a high frequency ripple. Inductor Ratio Index is calculated in equation (39):

$$\text{Inductor Ratio Index} = \frac{L_{MMC}}{L_{IMMC}} = \frac{f_{\Delta IL-IMMC} * \Delta I_{IMMC}}{f_{\Delta IL-MMC} * \Delta I_{MMC}} = \frac{60000\ Hz * 1\%}{120\ Hz * 5\%} = 100 \quad (39)$$

Additionally, the proposed converter has more number of inductors for any number of levels. Therefore, Table 3 introduced inductance overall size index to indicate the overall inductance size of the system defined in (40).

Inductance Overall Size Index = Total Number of Inductors * Inductance Ratio Index (40)

3. DC TO AC IMMC FOR ADJUSTABLE SPEED AC MOTOR DRIVES

3.1 Low Voltage Drives

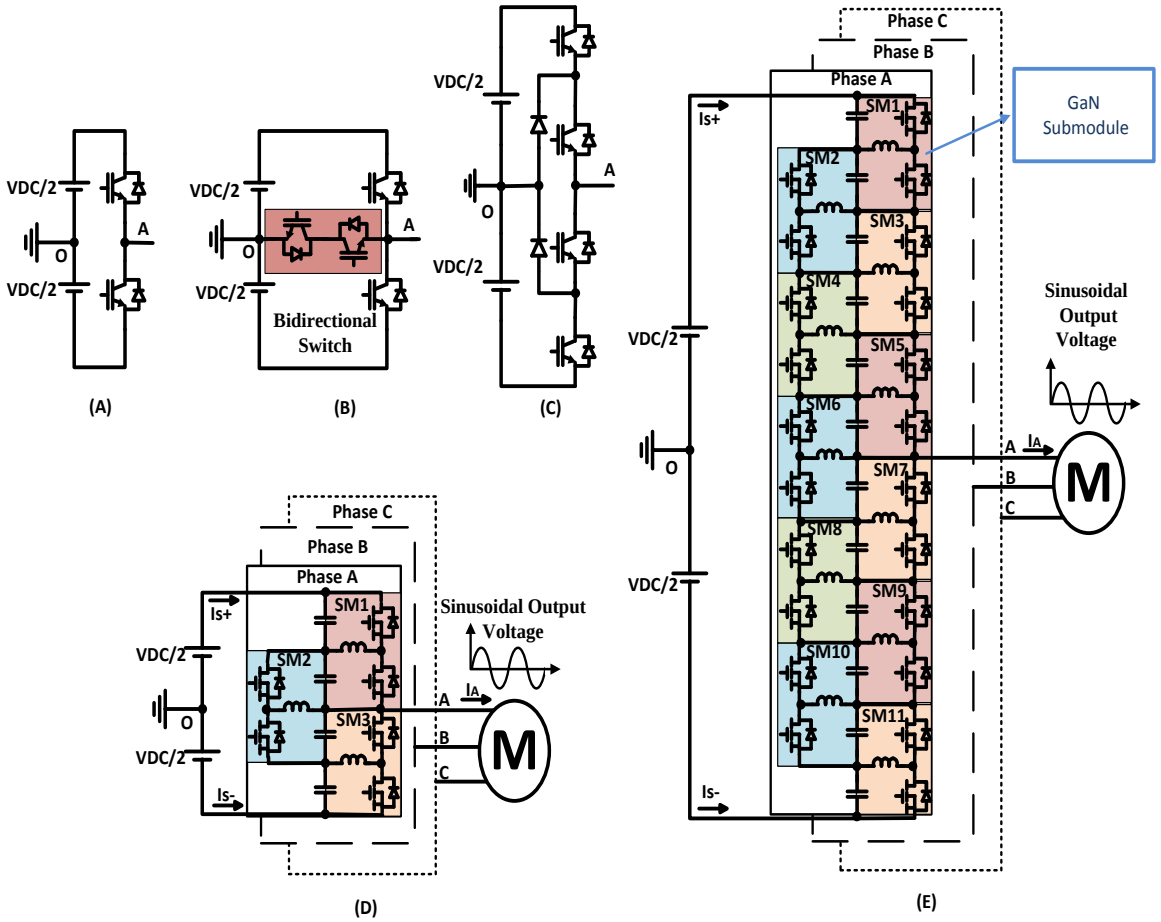

Fig. 34 (A) Two level inverter [22] (B) T-type three level inverter [20], (C) NPC inverter [4], (D) Proposed IMMC with 3 submodules to realize sinusoidal output voltage. (E) IMMC with 11 submodules. Note: The number of submodules can be increased to reduce the blocking voltage of the devices and to scale the voltage and power levels.

Fig. 34 shows the evolution of a switch mode DC-AC inverter half bridge – a building block for a two level and three level inverters [22]. The two-level inverter in Fig. 34 (A) does not have a zero state and is a widely used topology to power adjustable speed AC motor drives. Fig. 34 (B) and (C) show one phase of a three level inverter that incorporates a zero state with the addition of two switches [23]. Multilevel converter topologies continued to develop and offer

higher output voltage quality with simultaneous voltage sharing features [24]. Among numerous multilevel converter topologies, the neutral point clamped (NPC) inverter, Cascaded H-Bridge (CHB) inverter and Modular Multilevel Converter (MMC) have found widespread industrial applications [20]. The NPC is the most popular and common topology for medium voltage motor drives. However, this topology suffers from limited output voltage quality; voltage balancing issues related to series connected dc-link capacitors; asymmetrical loss distribution in the clamping diodes [25]. The CHB generates higher voltage levels by increasing the number of series connected H-Bridge cells. However, increasing the number of cells require a complicated multi-winding transformer and rectifier circuits to power the required isolated dc-link voltage levels. The MMC suffers from the requirement of large dc-link capacitors across each cascaded bridge and is incapable of operating at lower output frequencies with v/f control.

There are many commercially available low-voltage drives manufactured by companies like Siemens, ABB and PowerFlex as shown in Table 5. The commercial products are available with wide range of voltages and powers (208V-690V RMS and 0.5hp-7500hp) [26-28].

Table 5 Low voltage drives Commercial products

Company	**Product Name**	**Power (HP)**	**Voltage (V)**
ABB [28]	ACS310	0.5-30	200-480
	ACS800	1-6000	380-240
Siemens [26]	MICROMASTER 430 / 440	7.5-75	200-240
	SINAMICS G120E	1-200	380-480
PowerFlex [27]	PowerFlex 523 AC Drive	0.25-20	200-240
	PowerFlex 753 AC Drive	1-400	200-240

3.1.1 Low Voltage Drive Design Example

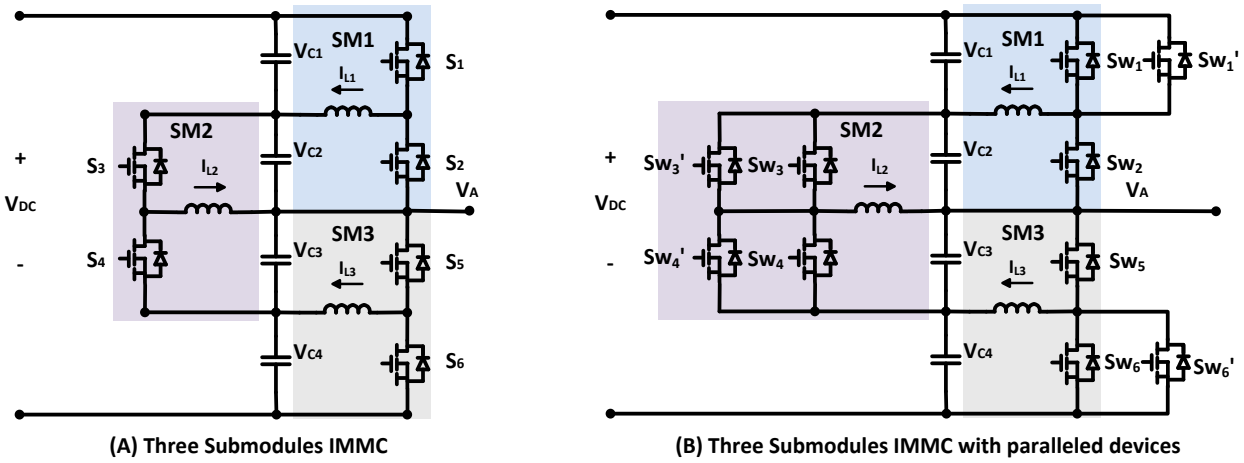

Fig. 35 The proposed 3 submodules IMMC shown in Fig. 34 (E) with parallel submodules to reduce current stress on the devices.

Table 6 IMMC designs for different motors.

Motor Voltage (V)		**230**	**400**	**500**	**690**
Required DC Link		327	568	710	980
GaN Device Rating (V)		**Number of Submodules**			
	100	23	39	49	69
	200	11	19	25	33
	650	3	5	7	11

According to [26-28], low voltage motors are classified to have a voltage rating range of 200V – 690V. The most popular voltage ratings of low voltage motors are 230V, 400V, 500V, and 690V. Table 6 summarizes the DC link requirement and number of submodules needed for the IMMC to drive each motor with a specific voltage rating. The DC link requirement is

calculated taking a third harmonic injection into consideration. The third harmonic injection allows %15 increase in voltage. The DC link is calculated using (41).

$$VDC = \frac{2\sqrt{2}\, V_{L-L,RMS}}{1.15\sqrt{3}} \tag{41}$$

The voltage stress on the devices can be calculated using (42).

$$Vsw = \frac{4}{N+1} VDC \tag{42}$$

The number of submodules in Table 6 is calculated while keeping the voltage stress on the devices below %55 the device's rating. For, example, when using the 100V GaN, the blocking voltage on the device must not exceed 55V. Therefore, allowing for a safe operation of the converter. The number of submodules can be paralleled to reduce the current stress on the switches. Fig. 36 converts Table 6 to a chart format to indicate the number of submodules needed for each motor rating.

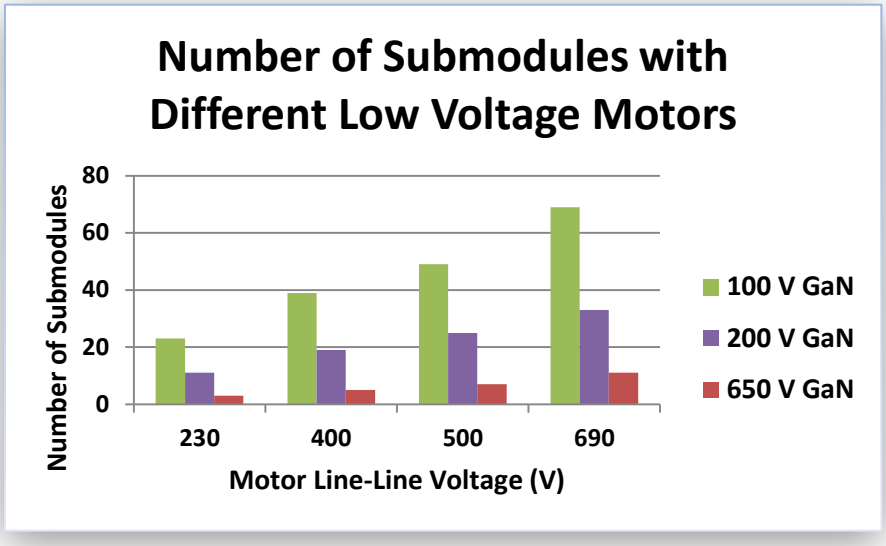

Fig. 36 The number of submodules needed for each motor rating.

This design example is introduced to resemble a 230 V ACS310 motor drive with a power of 11000 W [28]. The 3 submodules design using the 650 V GaN devices is chosen to minimize the number of switches needed. Using (41), the V_{DC} required to power the motor is 327 V. Using (42), the switch blocking voltage is V_{DC} which equals to 327 V. The switching frequency is chosen to be 200 kHz to stay in balance between compact size and low switching losses. The RMS current ratings of the devices are calculated in Amperes. Table 8 represents the design example parameters.

Table 7 Design example parameters

Parameter	**Value**
Output Voltage (V)	230
Output Current (A)	32.485
Output Power (kW)	11
Input DC Voltage (V)	327
Switching Frequency (kHz)	200
Inductor (µH)	100
Capacitor (µF)	2.2
Load Power Factor	0.85

Capacitor RMS currents are shown in Fig. 27 are calculated in (43), (44), (45) and (46).

$$\mathrm{I_{C1}} = -\delta_1 * \mathrm{I_{L1}} + \mathrm{I_{s+}} = 7.8\ A \tag{43}$$

$$\mathrm{I_{C2}} = (1-\delta_1) * \mathrm{I_{L1}} - \delta_2 * \mathrm{I_{L2}} + \mathrm{I_{s+}} = 9.5\ A \tag{44}$$

$$I_{C3} = (1 - \delta_2) * I_{L2} - \delta_3 * I_{L3} - I_{s-} = 9.5\ A \quad (45)$$

$$I_{C4} = (1 - \delta_3) * I_{L3} - I_{s-} = 7.8\ A \quad (46)$$

Inductor RMS currents are shown in Fig. 27 are calculated in (47), (48) and (49).

$$I_{L1} = \frac{I_{s+} - I_{C1}}{\delta_1} = 22.09\ A \quad (47)$$

$$I_{L2} = \frac{I_{C3}}{1 - \delta_2} + \frac{\delta_3}{(1 - \delta_2)(1 - \delta_3)} I_{C4} + \frac{1 + \delta_3}{(1 - \delta_2)(1 - \delta_3)} I_{s-} = 35.73\ A \quad (48)$$

$$I_{L3} = \frac{-I_{C4} - I_{s-}}{\delta_3} = 22.09\ A \quad (49)$$

The RMS currents of the switches shown in Fig. 35 (A) are calculated in (50), (51), (52), (53), (54) and (55)

$$I_{S1} = \delta_1 I_{L1} = 21.45\ A \quad (50)$$

$$I_{S2} = (1 - \delta_1)\ I_{L1} = 3.9\ A \quad (51)$$

$$I_{S3} = \delta_2 I_{L2} = 24.375\ A \quad (52)$$

$$I_{S4} = (1 - \delta_2)\ I_{L2} = 24.375\ A \quad (53)$$

$$I_{S5} = \delta_3 I_{L3} = 3.9\ A \quad (54)$$

$$I_{S6} = (1 - \delta_3)\ I_{L3} = 21.45\ A \quad (55)$$

By paralleling the devices as shown in Fig. 35 (B), the current stress on the devices is reduced. The RMS current ratings of the devices are calculated in (56), (57), (58), (59), (60) and (61)

$$I_{Sw1} = \frac{I_{S1}}{2} = 10.725\ A \quad (56)$$

$$I_{Sw2} = (1 - \delta_1)\ I_{L1} = 3.9\ A \quad (57)$$

$$I_{Sw3} = \frac{I_{S3}}{2} = 12.19\ A \quad (58)$$

$$I_{Sw4} = \frac{I_{S4}}{2} = 12.19\ A \tag{59}$$

$$I_{Sw5} = \delta_3 I_{L3} = 3.9\ A \tag{60}$$

$$I_{Sw6} = \frac{I_{S6}}{2} = 10.725\ A \tag{61}$$

The Total Active Switch Stress (S) is calculated in (62). The Switch Utilization Factor (U) is calculated in (63) by dividing the output power by (S).

$$S = \sum_{j=1}^{k} V_j\, I_j = 97605\ VAR \tag{62}$$

$$U = \frac{P_{Load}}{S} = \%11.3 \tag{63}$$

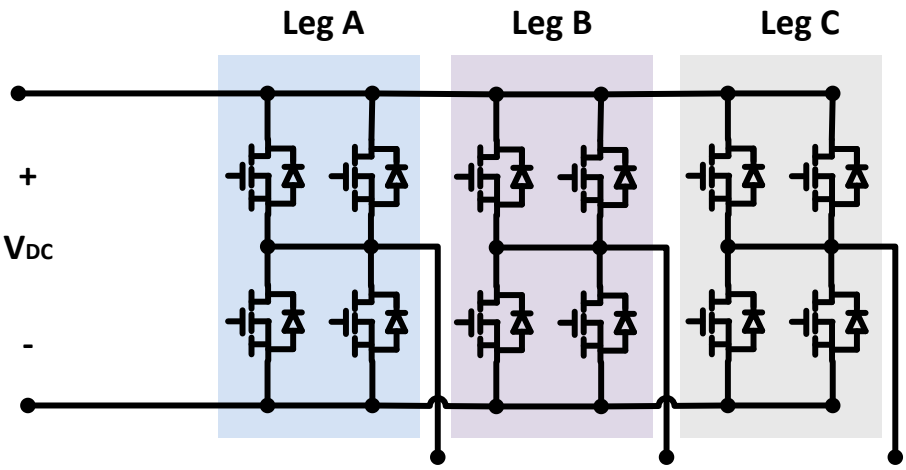

Fig. 37 A classic three phase inverter.

The motor can be driven by the classic three phase inverter seen in Fig. 37. The three-phase inverter seen in Fig. 37 is designed to drive the 230V motor to compare it to the proposed IMMC. The DC voltage required is calculated in (64).

$$V_{DC} = \frac{2\sqrt{2}\, V_{L-L,RMS}}{1.15\sqrt{3}} = 327V \tag{64}$$

The voltage stress on the switched is calculated in (65).

$$V_{sw} = V_{DC} = \frac{2\sqrt{2}\, V_{L-L,RMS}}{1.15\sqrt{3}} = 327\ V \tag{65}$$

The RMS current stress on the devices with the parallel scheme is computed in (66).

$$I_{sw} = \frac{I_{Load-,RMS}}{2\sqrt{2}} = 11.5\ A \tag{66}$$

3.1.2 Simulation Results

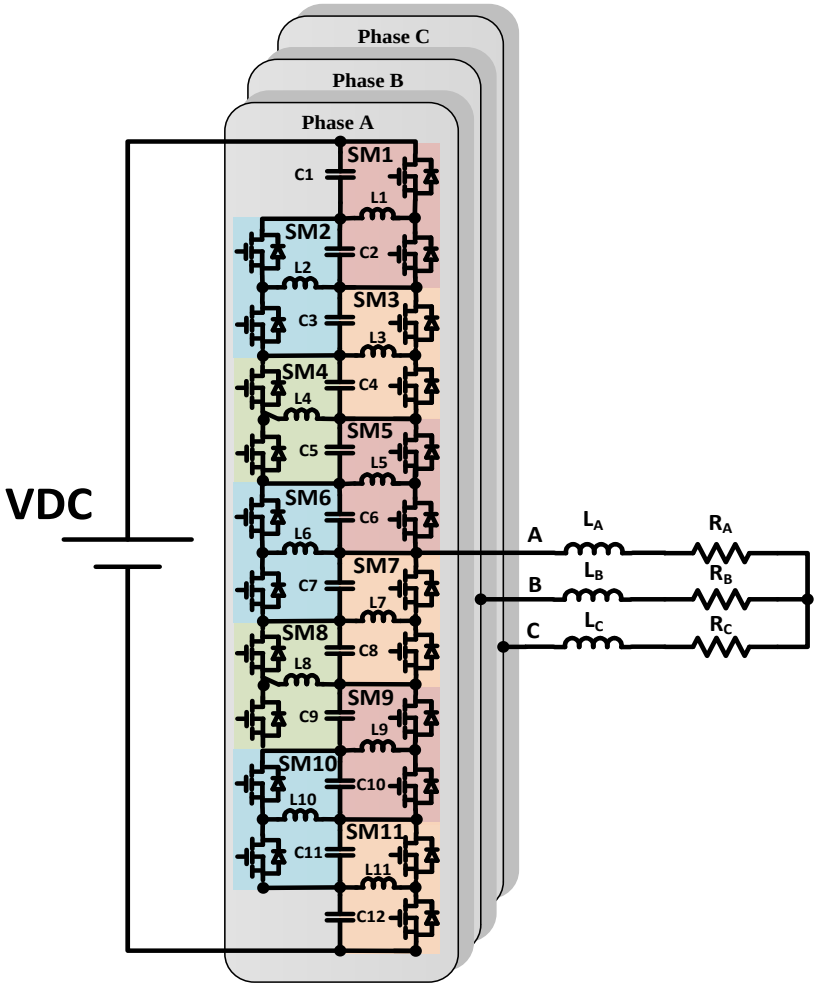

Fig. 38 The Simulated 11 submodules converter with a three phase RL-Load

Table 8 Simulation parameters

Parameter	**Value**
Input voltage (V)	375
Power (kW)	7
Switching Frequency (kHz)	500
Inductor (µH)	20
Capacitor (µF)	1
Load Resistor (Ω)	7
Load inductance (mH)	8

This IMMC simulation is designed to have a similar rating of a 230 V commercialized ABB motor drive (ACS310). The motor comes in different power ratings that ranges between 0-11 kW. The motor drive operates at frequency that ranges from 0-500 Hz. The proposed IMMC is an 11-submodule design using a 200V low voltage GaN. The VDC required to drive the motor is 375V (without third harmonic injection). The values of the capacitors and inductors are chosen to minimize the voltage and current ripples on the passive components as seen in Table 8. The motor is simulated as an R-L load to have realistic simulation results as shown in Fig. 38.

Fig. 39 and Fig. 40 show the high quality sinusoidal output voltage and current of the proposed 11 SMs IMMC. Fig. 41 and Fig. 42 demonstrate the voltages of the 12 capacitors of the converter. The voltage across each capacitor is a slice of the output sinewave. Fig. 43 and Fig. 44 show the current through each inductor in the proposed converter.

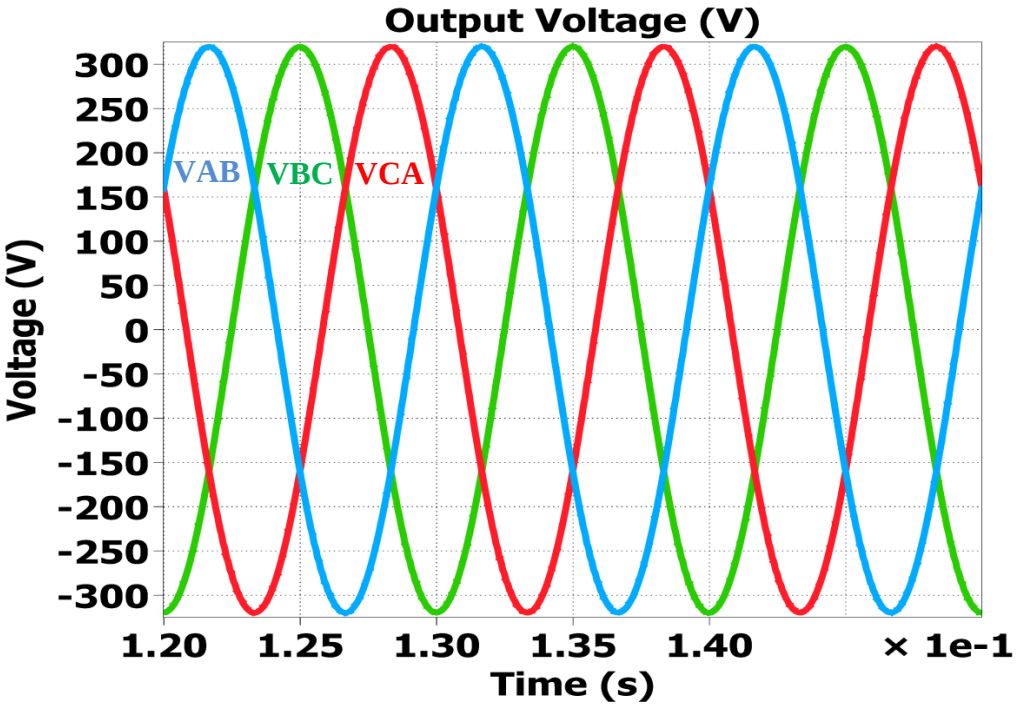

Fig. 39 The three-phase line-line output voltage of the IMMC.

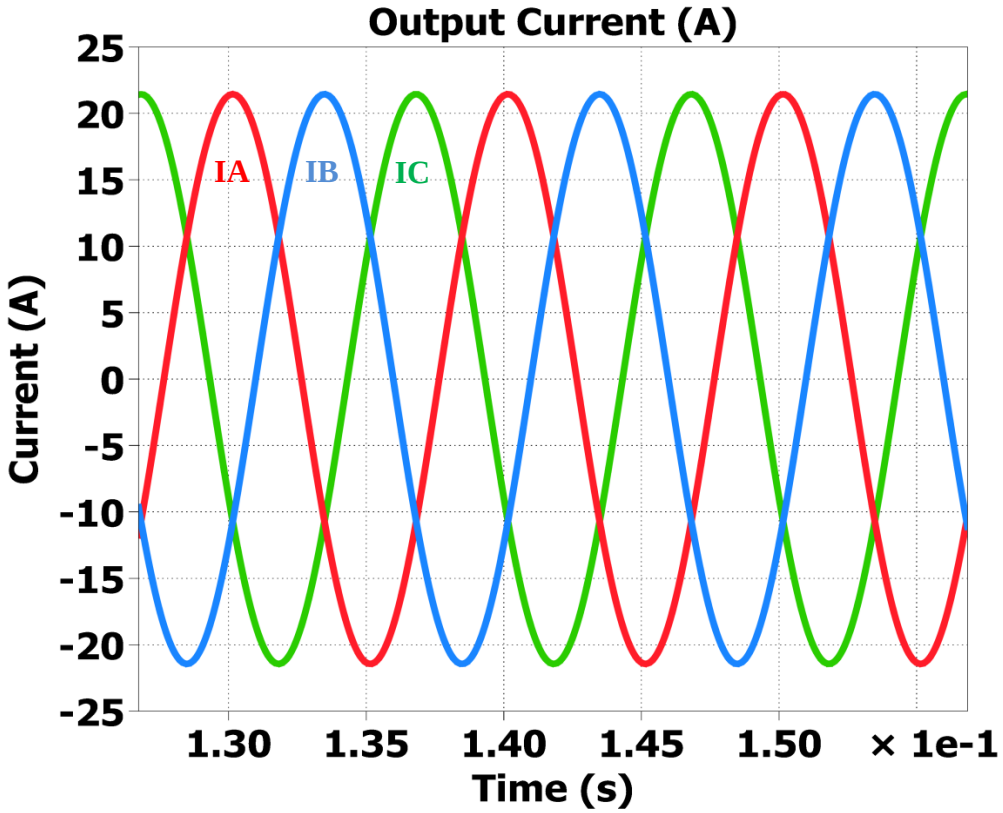

Fig. 40 The three-phase line-line output current of the IMMC.

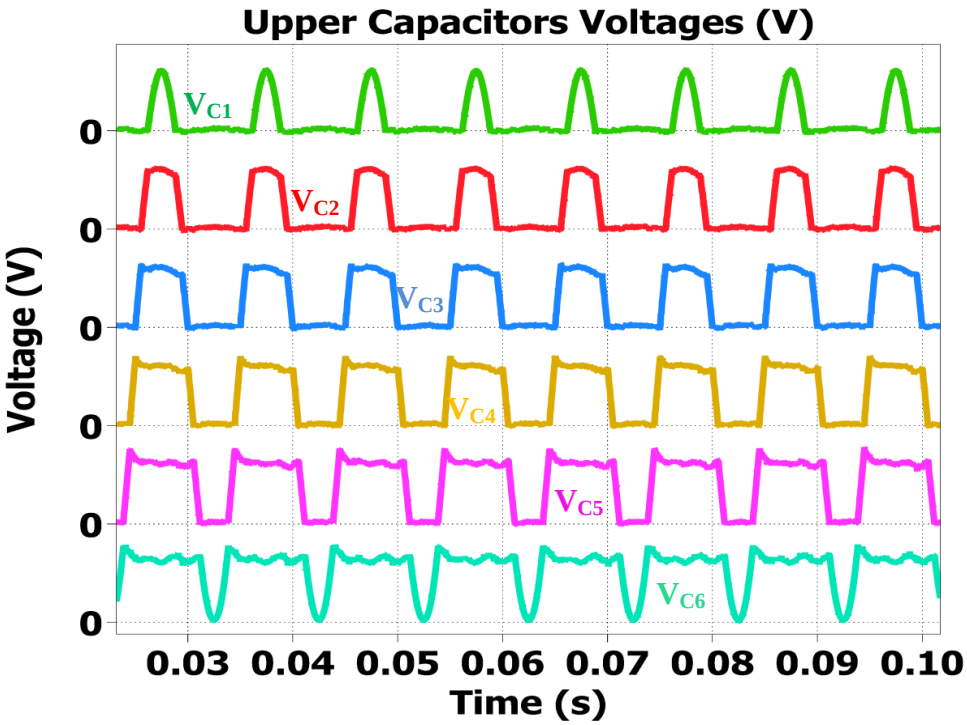

Fig. 41 The voltages of the upper capacitors (from C_1 to C_6).

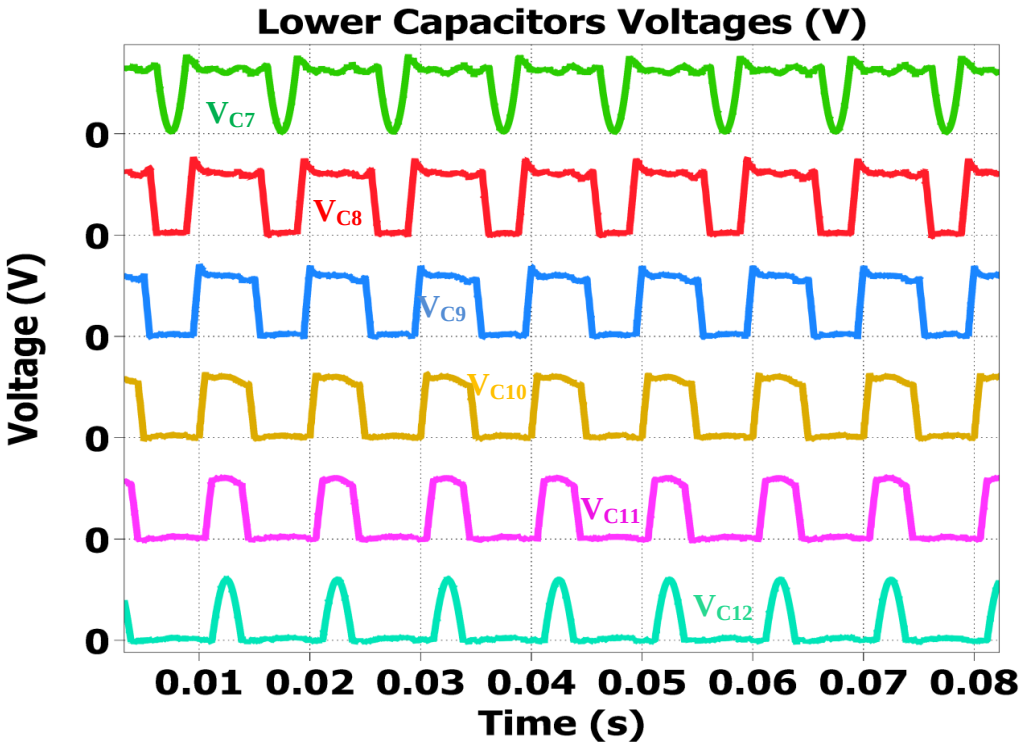

Fig. 42 The voltages of the lower capacitors (from C_7 to C_{12}).

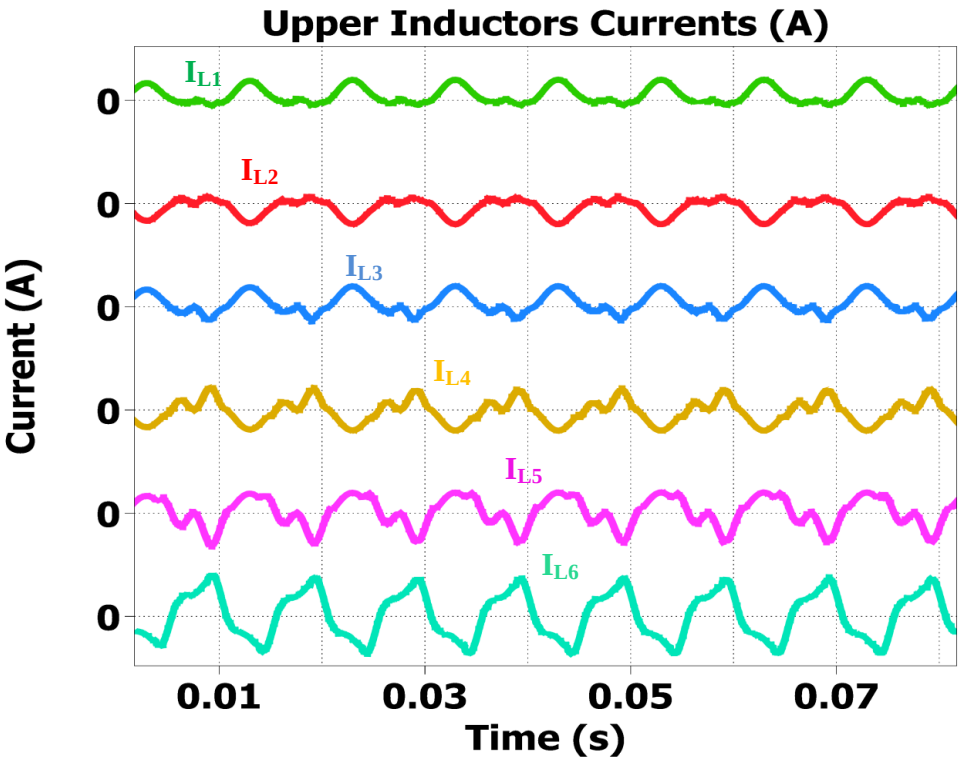

Fig. 43 The current through the upper inductors (from L_1 to L_6)

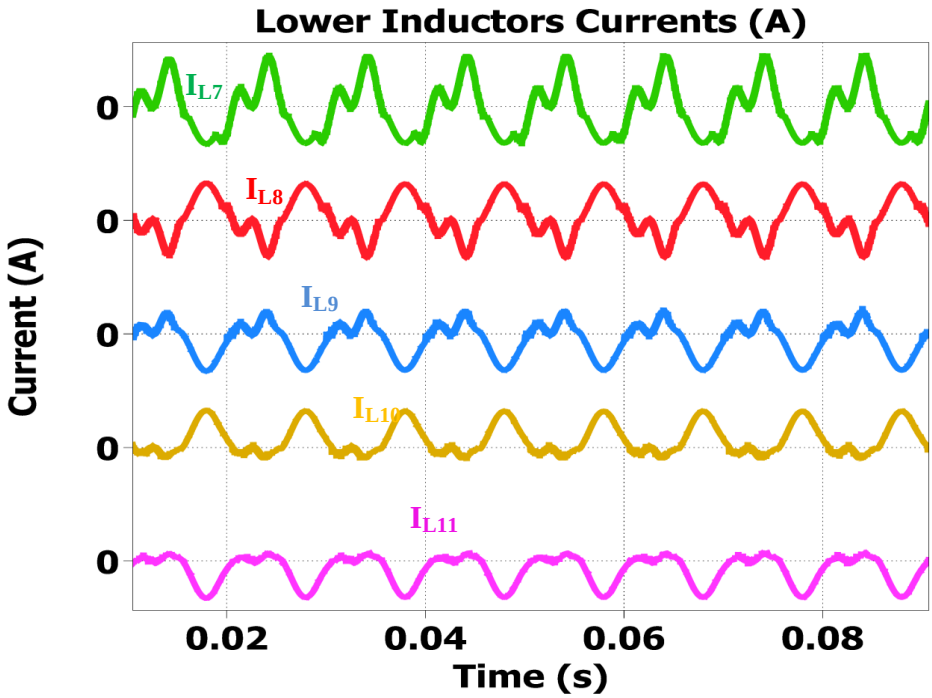

Fig. 44 The current through the lower inductors (from L_7 to L_{11})

3.1.3 Experimental Results

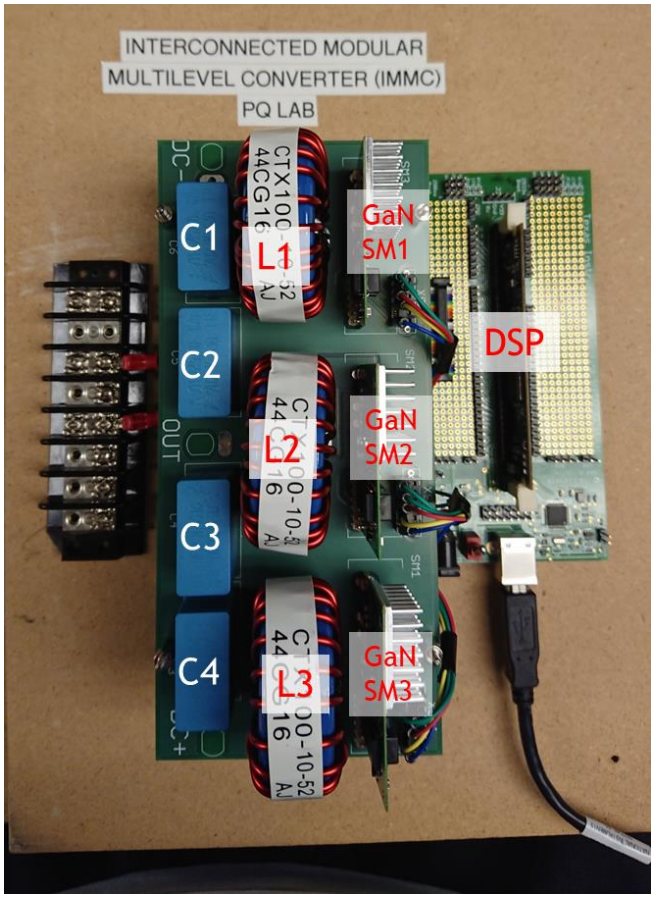

Fig. 45 The laboratory prototype built using TI LMG3410 GaN modules.

The hardware shown Fig. 45 of the proposed single phase IMMC is built in the laboratory to verify the concept. Three submodules design is tested to prove that the IMMC provides a sinusoidal output with the minimum number of submodules. The input DC voltage of the converter is 200 volts. The switches used for the converter are TI LMG3410 GaN modules that are chosen to operate at 200 kHz switching frequency [29]. The passive components size plays an important role in controlling the ripple on them. Therefore, inductors and capacitors are chosen to be 100 µH and 2.2 µF respectively to have an acceptable inductor current and capacitor voltage ripples. The load is an R-load with a value of 120 Ω as shown in Table 9.

Table 9 Experimental prototype parameters

Parameter	**Value**
Input voltage (V)	200
Switching Frequency (kHz)	200
Dead Time (ns)	50
Inductor (µH)	100
Capacitor (µF)	2.2
Load (Ω)	120

The output voltage and current of the laboratory prototype is proven to be a sinusoidal waveform with no output filter as opposed to the existing multilevel converter topologies. The voltage and current are in phase due to the resistive load at the output. As seen in Fig. 46 and Fig. 47 the high dv/dt is absent from the output waveforms which makes the topology a great option for motor drive applications [30]. It is worth mentioning that an inductor airgap is recommended to prevent core from saturation at low operating frequency.

The voltage across each capacitor is a sliced sinusoidal waveform as seen in Fig. 48. Therefore, having two capacitors on at the same time results a sinusoidal output. The voltages across the capacitors are achieved with a very simple control technique and do not require complex balancing methods. The currents through the inductors are shown in Fig. 49. The current ripple on the inductors can be minimized by increasing the inductor values or the switching frequency of the converter.

Fig. 50 and Fig. 51 show the voltage across each submodule with 60 Hz and 1 Hz. The experimental results match the calculated submodules voltage in Fig. 19.

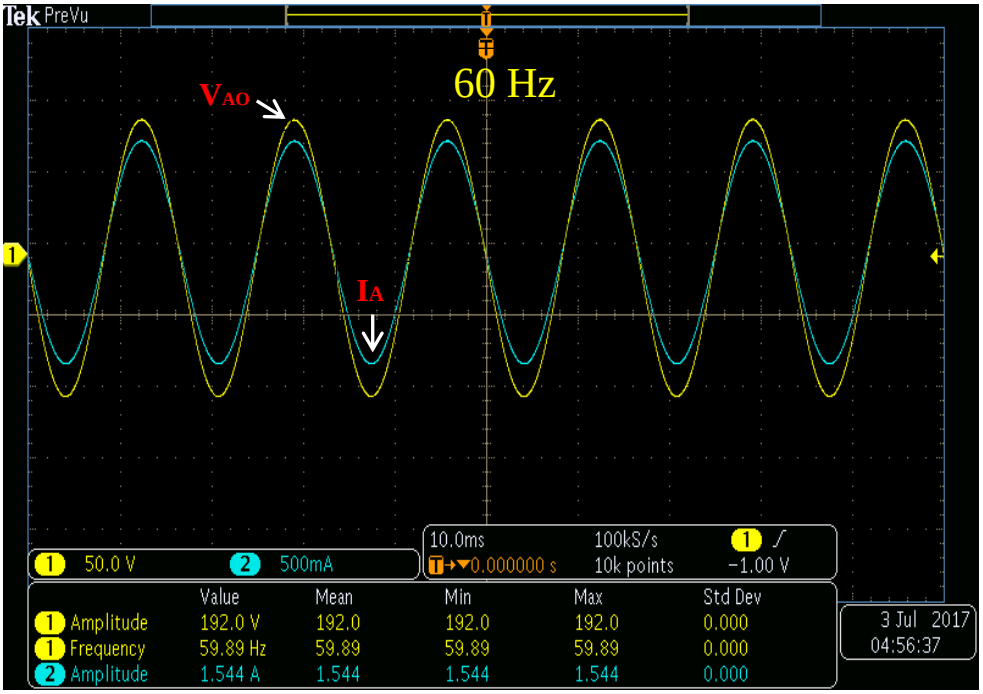

Fig. 46 The output voltage and current of the proposed IMMC shown in Fig. 27 is a sinusoidal wave with a fundamental frequency of 60 Hz.

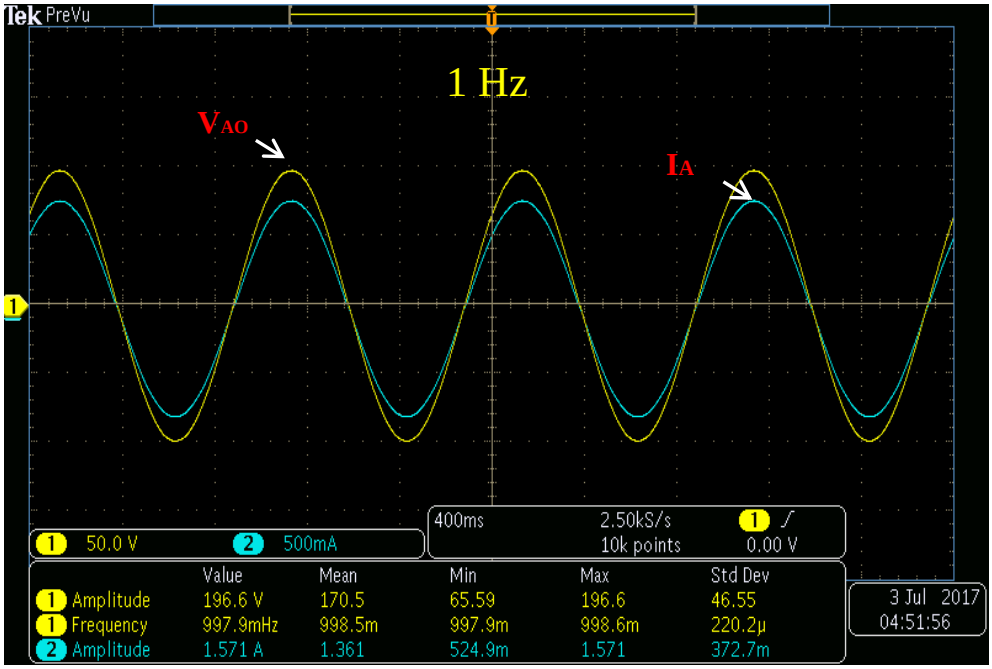

Fig. 47 The 1 Hz output voltage and current of the IMMC shown in Fig. 27 is a sinusoidal wave which proves the topology is a good candidate for ASD.

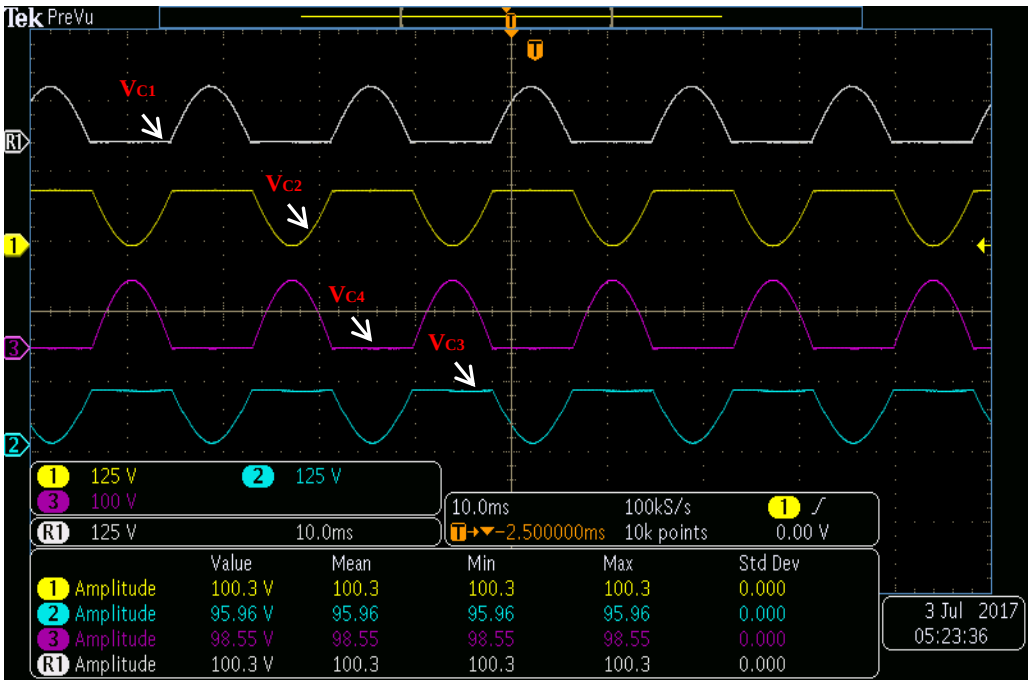

Fig. 48 The voltage across each capacitor as shown in Fig. 27 is a sliced sine wave which makes the sum of the output a full sinewave.

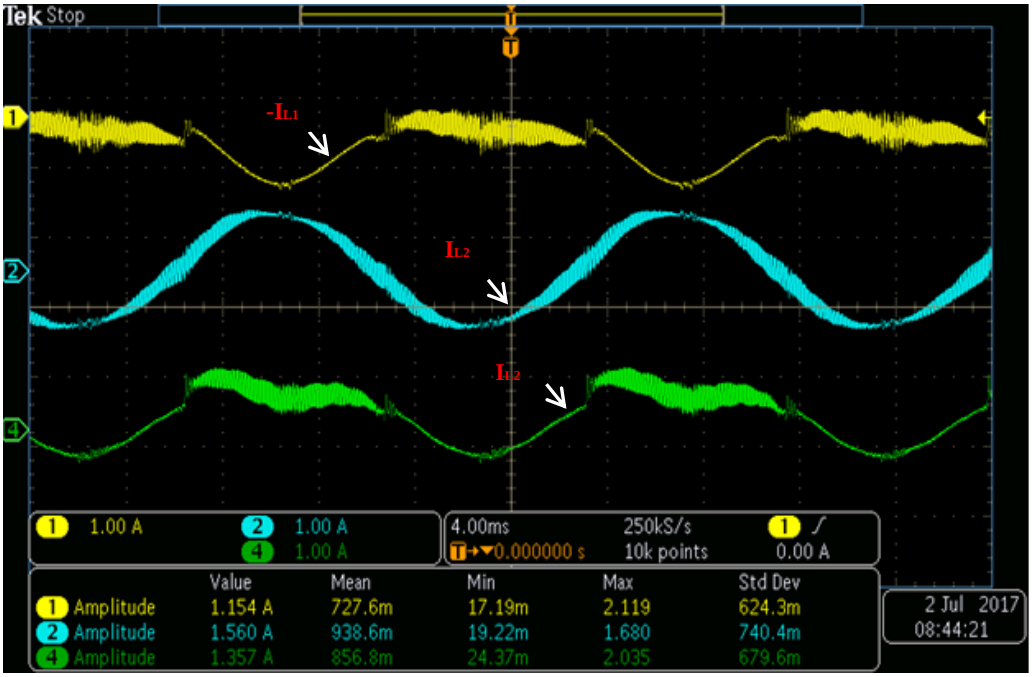

Fig. 49 The currents of the three inductors as seen in Fig. 27. The ripple can be minimized by increasing inductor size or the switching frequency of the converter.

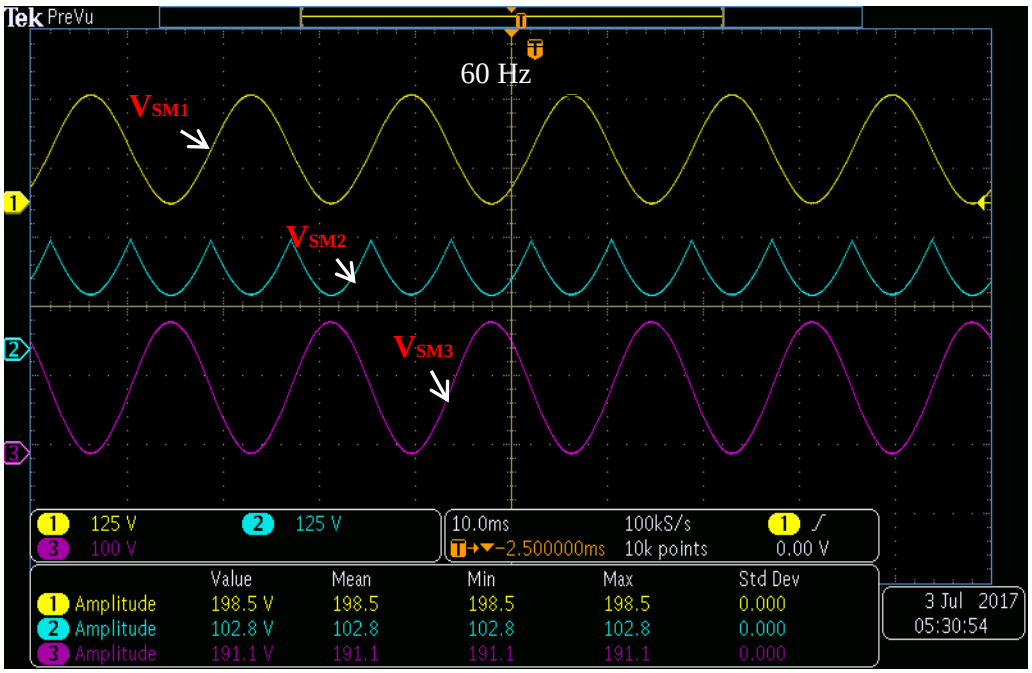

Fig. 50 Submodules (SM) voltages with 60 Hz shown in Fig. 27. Channel 1 (yellow) is submodule 1 voltage, channel 2 (light blue) is submodule 2 voltage and channel 3 (violet) is submodule 3 voltage.

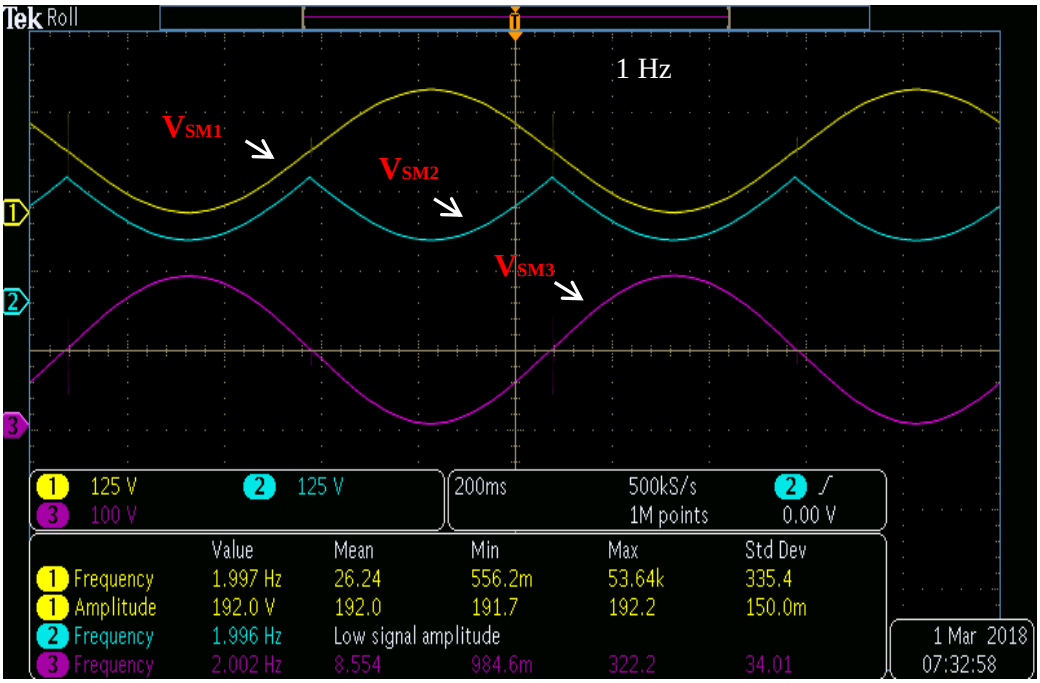

Fig. 51 Submodules (SM) voltages with 1 Hz shown in Fig. 27. Channel 1 (yellow) is submodule 1 voltage, channel 2 (light blue) is submodule 2 voltage and channel 3 (violet) is submodule 3 voltage.

It is important to note that the waveforms of the SM voltages do not change with frequency. The Output voltage is the sum of the voltage of two capacitors minus half the DC link voltage as seen in Fig. 20. Therefore, producing a pure sinusoidal output with low frequency (1 Hz) indicates the shape of the capacitor waveforms. In summary, the experimental results showed that the quality of the waveform of the 60 Hz and 1 Hz converter are both high quality sinusoidal waveforms that were synthesized from the capacitors. Therefore, both will have the same waveform for the SM voltages.

The main reason for choosing an R-load is to experiment the worst-case scenario of the motor. Using an RL load introduces a filtering action to the current. An R load is used to prove that the proposed converter produces a sinusoidal output at the worst-case scenario. Another experiment is done using an RL load as seen in Table 10 to test the converter's low frequency operation with different loads. The submodule voltages, output current and voltage are displayed for the RL load in Fig. 52, Fig. 53, Fig. 54 and Fig. 55.

Table 10 Another RL-Load prototype parameters

Parameter	**Value**
Input voltage (V)	100
Switching Frequency (kHz)	200
Dead Time (ns)	50
Inductor (μH)	100
Capacitor (μF)	2.2
Resistive Load (Ω)	120
Inductive Load (mH)	7.5

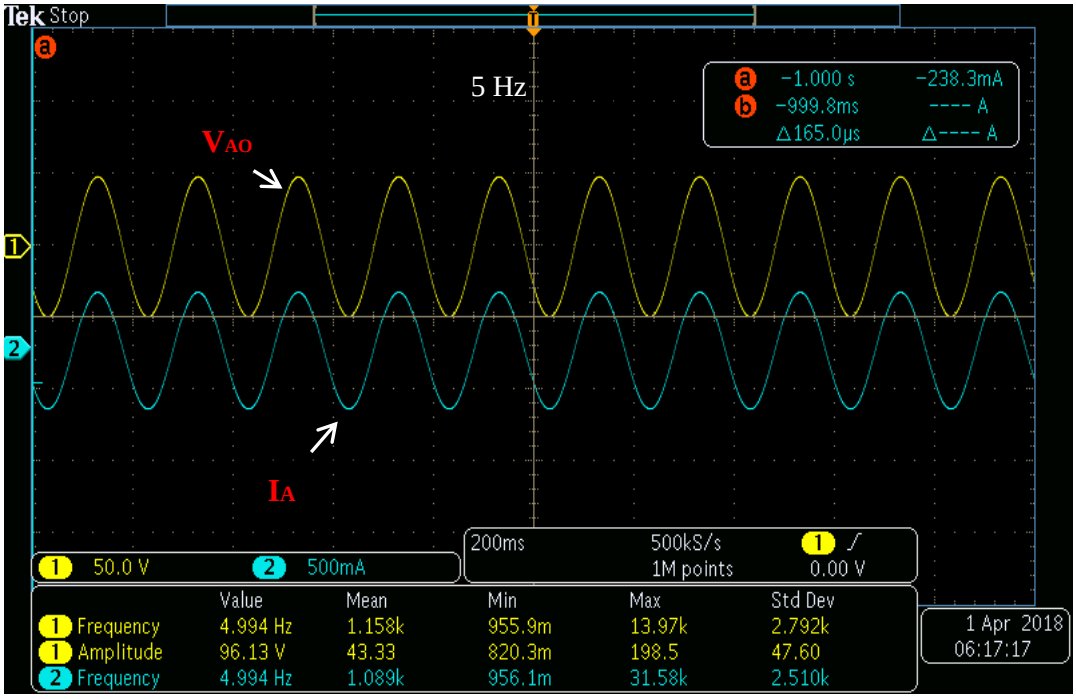

Fig. 52 The output voltage of the proposed IMMC shown in Fig. 27 is a sinusoidal wave with a fundamental frequency of 5 Hz.

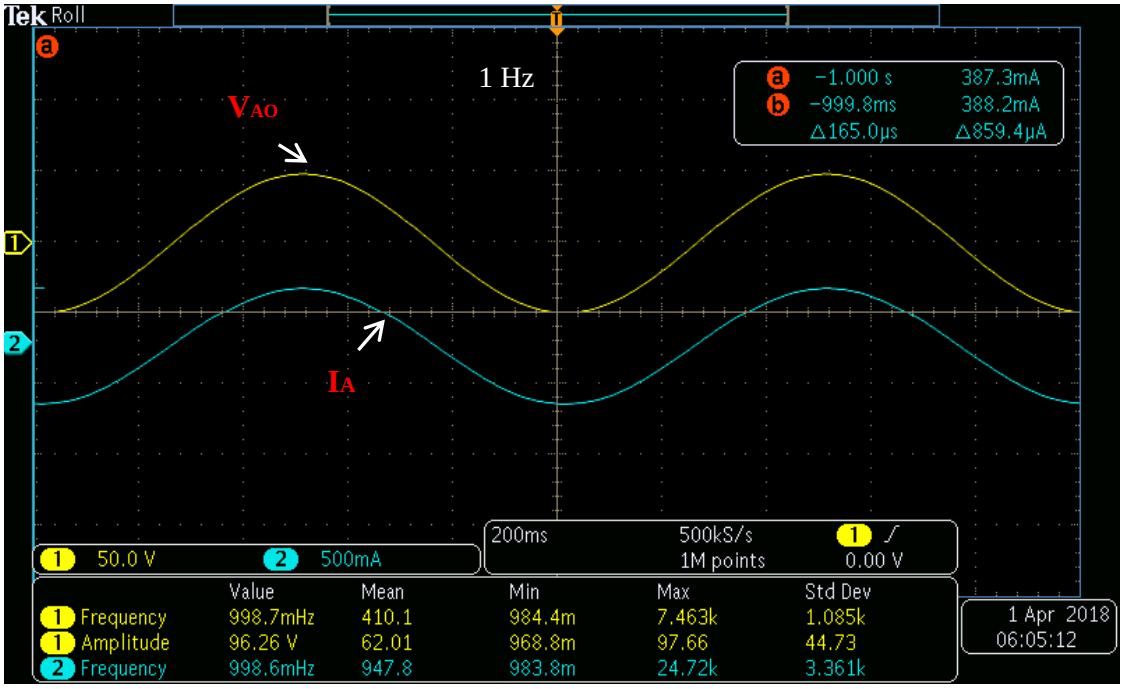

Fig. 53 The 1 Hz output voltage and current of the IMMC shown in Fig. 27 is a sinusoidal wave which proves the topology is a good candidate for ASD.

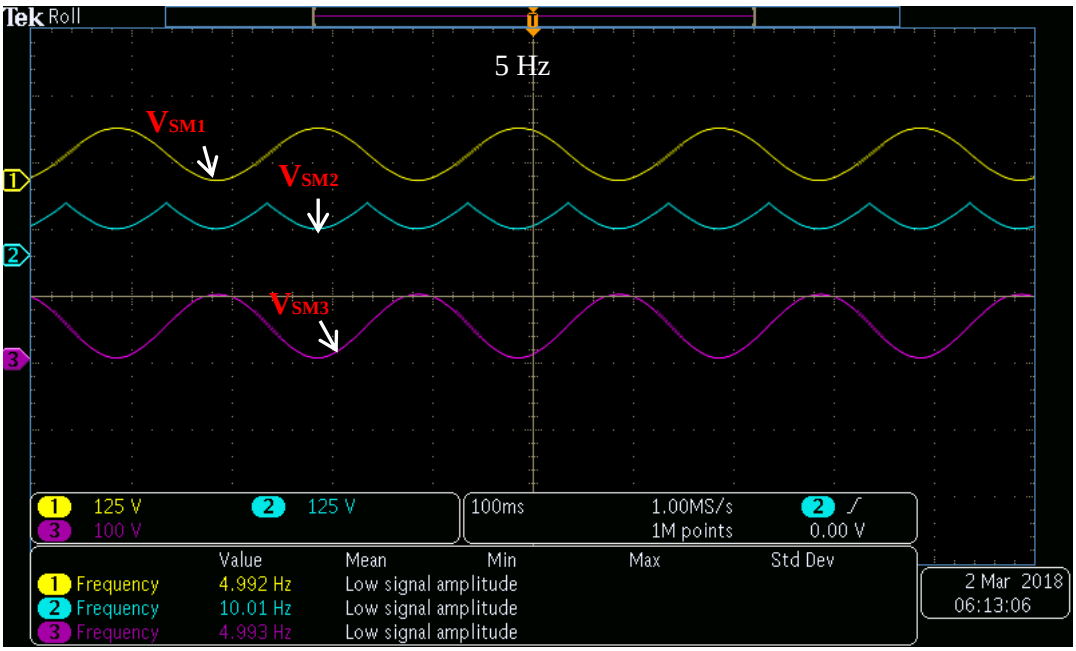

Fig. 54 Submodules voltages with 5 Hz with RL-load. Channel 1 (yellow) is submodule 1 voltage, channel 2 (light blue) is submodule 2 voltage and channel 3 (violet) is submodule 3 voltage.

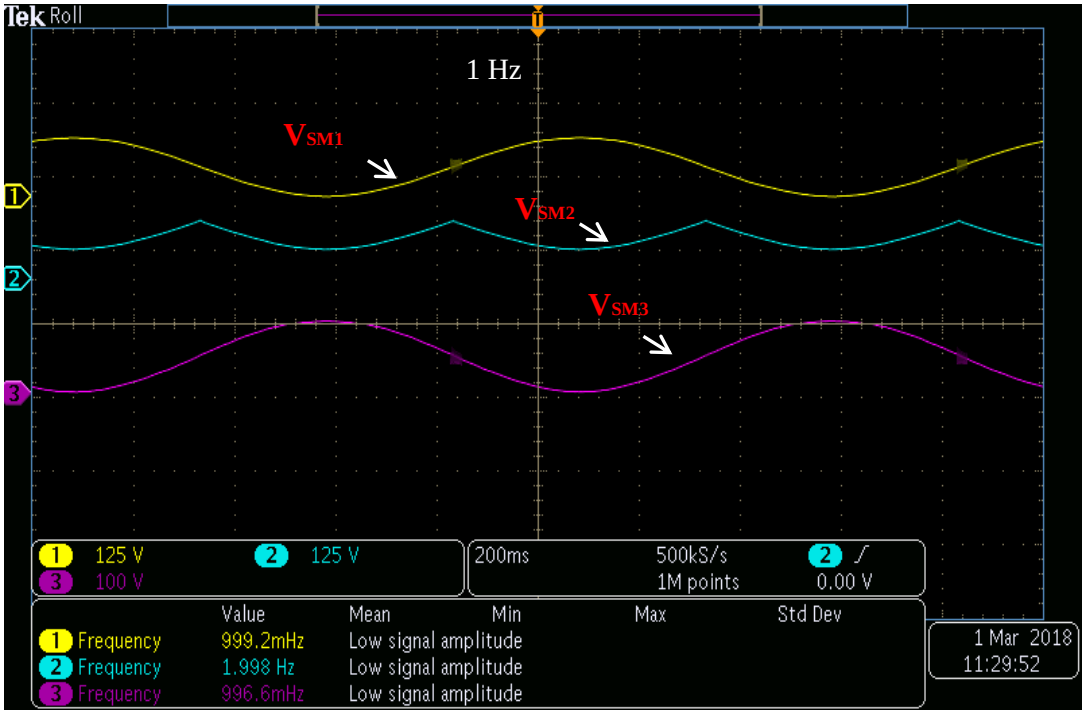

Fig. 55 Submodules voltages with 1 Hz with RL-load. Channel 1 (yellow) is submodule 1 voltage, channel 2 (light blue) is submodule 2 voltage and channel 3 (violet) is submodule 3 voltage.

3.2 Medium Voltage Drives

Table 11 Market products for medium voltage drives.

Company	Product Name	Topology
Siemens	GH150	MMC
	GH180	CHB
	GM150	NPC
	SM150	NPC
	SM120	MMC & NPC
ABB	ACS1000	NPC
	ACS2000	5L ANPC
	ACS5000	5L NPC/H-bridge
	ACS6000	NPC
Rockwell	PowerFlex6000	CHB
GE	MV6	NNPP
	MV7000	NPP
Eato	SC9000	NPC
Ingeteam	MV100	NPC
	MV500	NPC
	MV700	5L NPC/H-bridge
Yaskawa	MV1000	5L NPC/H-bridge
Schneider	Altivar1200	CHB

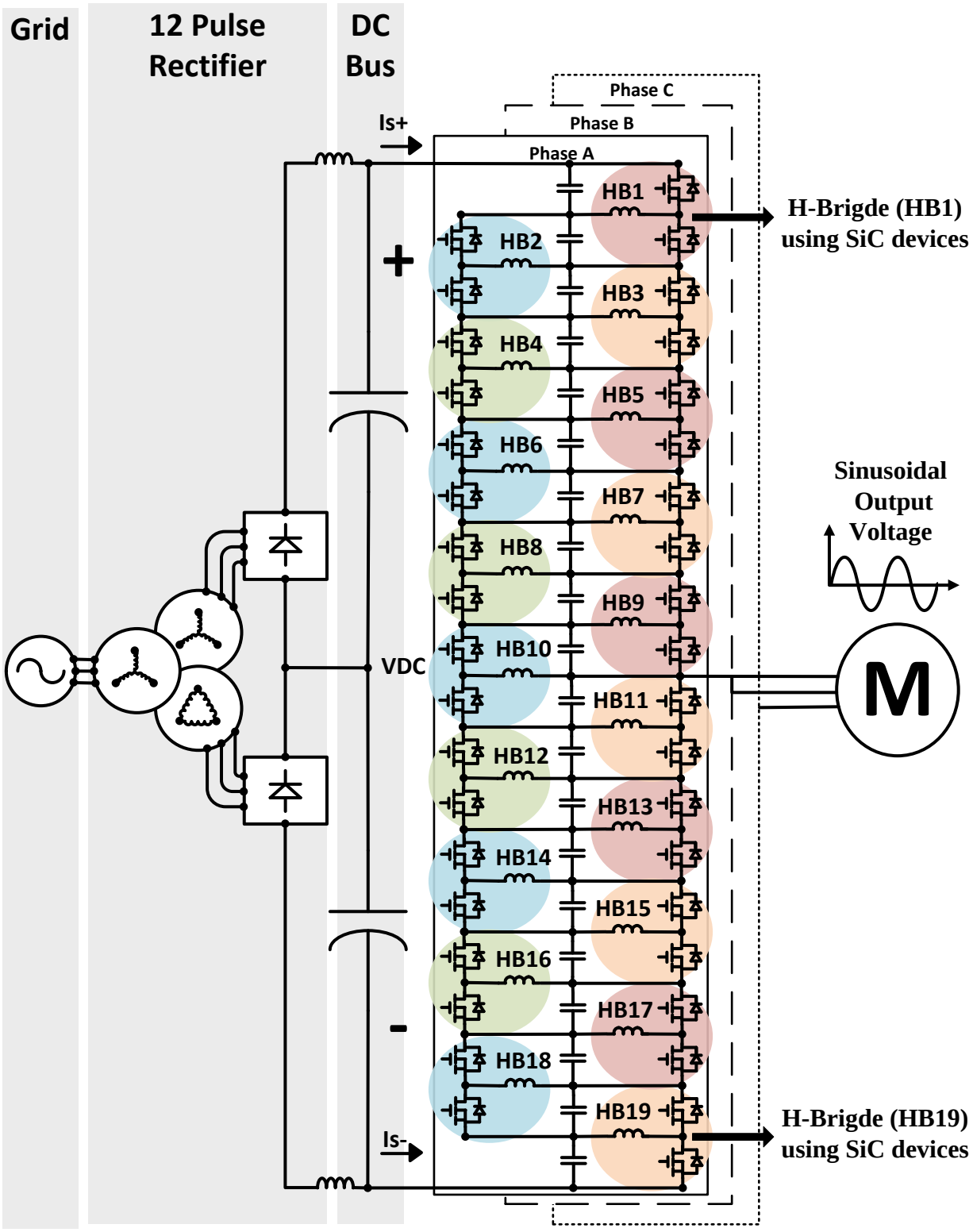

Fig. 56 The proposed medium voltage adjustable speed drive topology with IMMC and a 12-pulse rectifier dc-link.

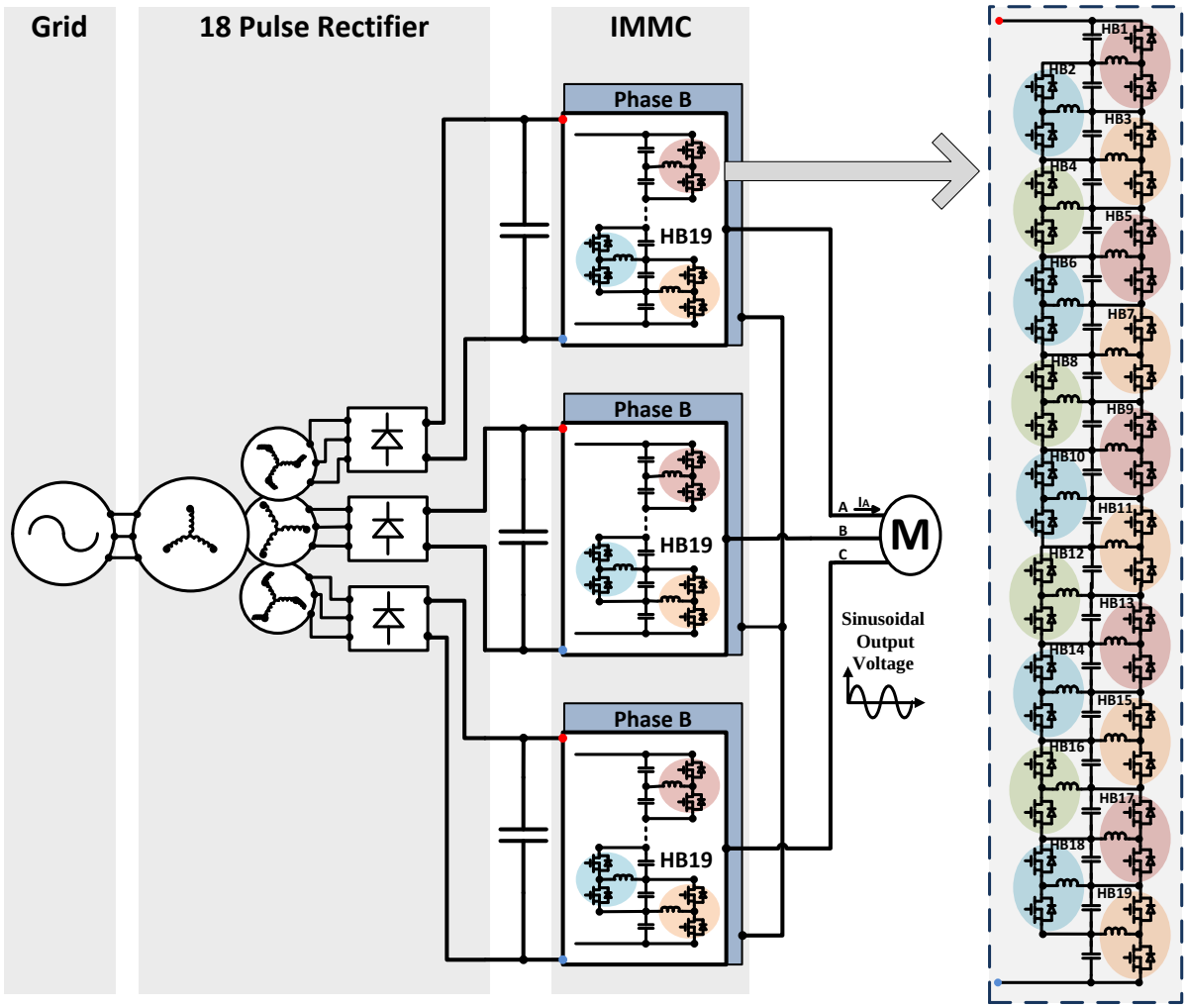

Fig. 57 Another variation of the proposed medium voltage adjustable speed drive with IMMC with 18-pulse rectifier.

Motor drives have been an active research area recently due to the industrial need for high performance medium voltage drive. Voltage Source Converters (VSC) has been the most popular converters for medium voltage drives [19]. This is due to their superior performance, scalability and low THD output. An example of a commercial medium voltage drive product is the Siemens GH150 [31]. The basic topology of the product is the Modular Multilevel Converter (MMC) proposed in [8]. The topology consists of several submodules that contain two switches in an H-bridge configuration and a large DC capacitor. The output of the MMC is a multilevel

staircase wave form that requires an output filter unit to produce a pure sinewave. Moreover, the MMC suffers from low frequency ripple on the DC capacitor and limited performance at low frequency operation. The low frequency issue was solved in [32] but it requires complex control and causes the available torque to be less than the nominal. Table 11 shows market products for medium voltage drives with the name of the product and topology used [33].

Fig. 56 and Fig. 57 show the different topologies for medium voltage drives using the IMMC. Fig. 56 shows the proposed medium voltage adjustable speed drive topology with IMMC and a 12-pulse rectifier dc-link. Fig. 57 shows another variation of the proposed medium voltage adjustable speed drive with IMMC using 18-pulse rectifier.

3.2.1 Medium Voltage Drive Design Example

Table 12 IMMC designs for different motors.

Motor Voltage (V)		**2300**	**4160**	**6900**	**13800**
Required DC Link		2840	5908	9798	19596
SiC Device Rating (V)		**Number of Submodules**			
	1200	15	33	53	107
	1700	11	23	37	75
	3300	5	11	19	39
	6500	3	5	9	19
	10000	3	3	5	11

The IMMC is a modular converter and the number of submodules can be increased to reduce the voltage stress on the devices. This design example is geared toward medium voltage motor drives.

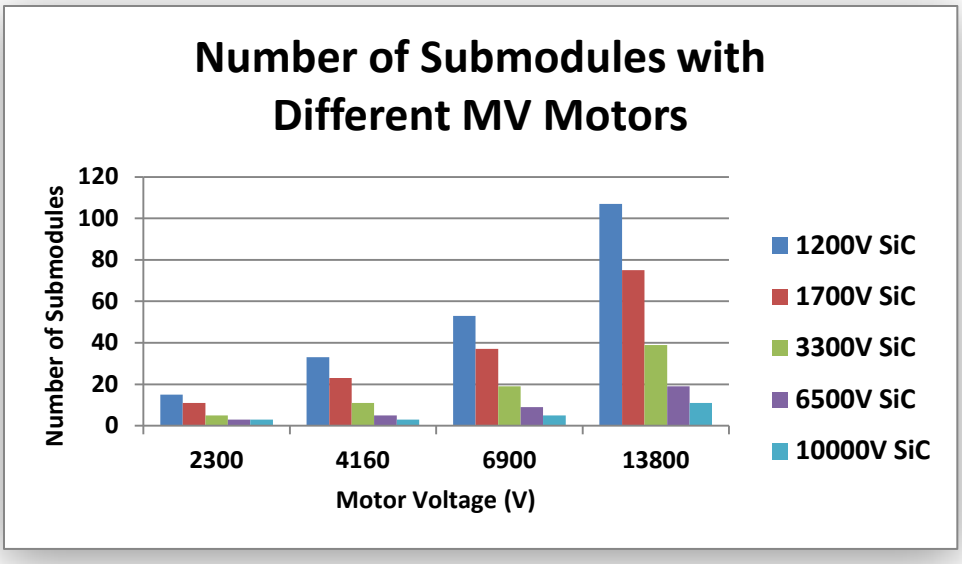

Fig. 58 The number of submodules recommended for different MV motors.

The most common voltage ratings for medium voltage motors in the industry are: 2300V, 4160V, 6900V and 13800V. Therefore, Table 12 proposes the recommended number of submodule to drive each motor based on the required DC link voltage with different SiC devices that has different voltage ratings. The modulation of the converter assumes a third harmonic injection to reduce the DC link voltage %15. Moreover, the voltage stress of the devices does not exceed %65. Table 12 is converted to a bar diagram in Fig. 58.

The medium voltage IMMC seen in Fig. 59 is designed to drive a 13.8kV motor. Table 13 shows the design example parameters. The DC voltages required for the 13.8kV is 19596V which require 19 SMs to 3920V as illustrated in Table 12. The switch RMS current ratings of the 38 switches is computed and shown in Fig. 60. The current RMS ratings are not uniform for all devices but tend to increase toward the middle SM.

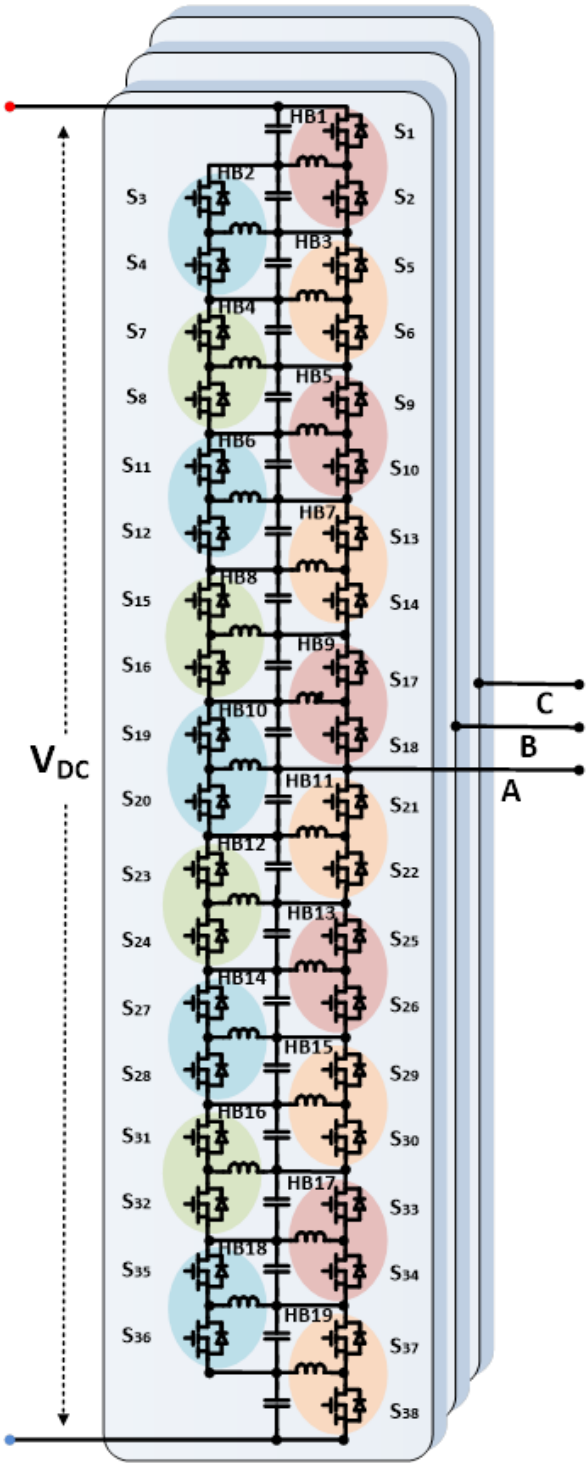

Fig. 59 Medium Voltage IMMC

Table 13 Design example parameters

Grid Voltage Vab (kV)	13.8
Output Power (MW)	2.7
Output Current (A)	120
Power Factor	0.94

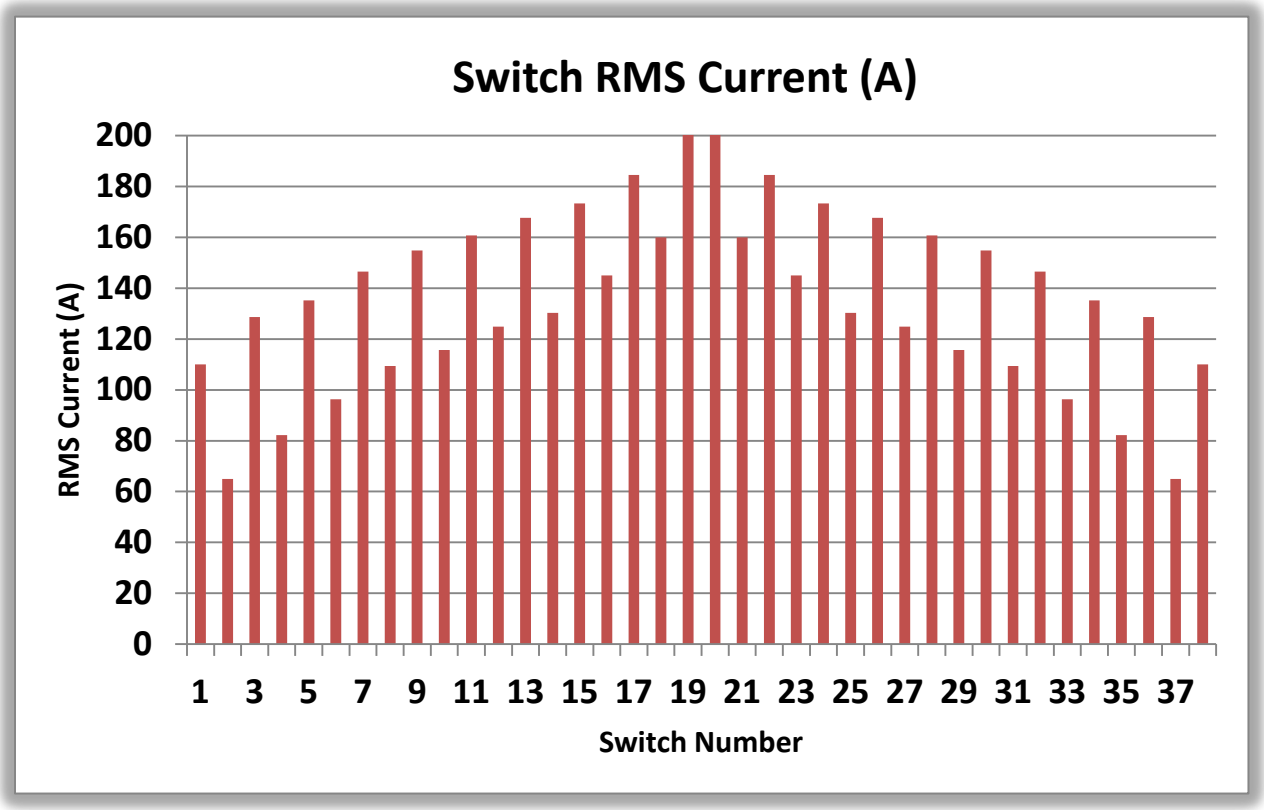

Fig. 60 RMS ratings of the devices seen Fig. 59

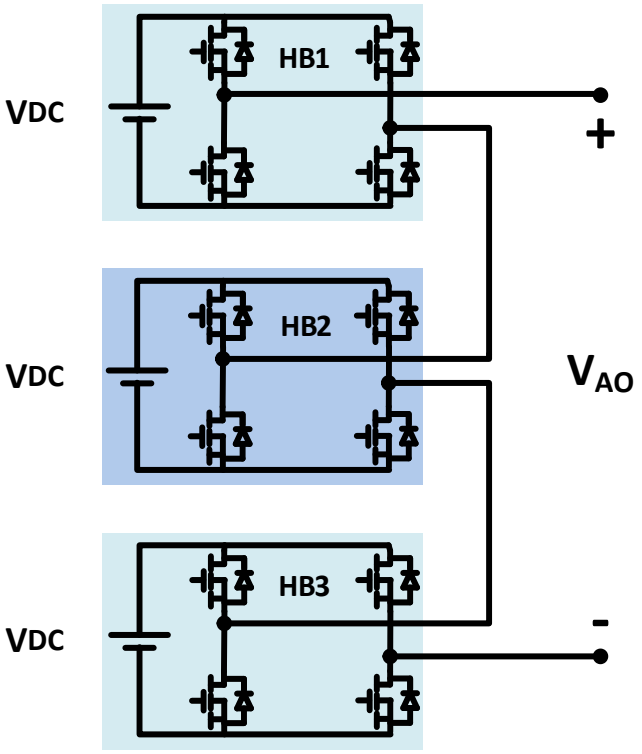

Fig. 61 An equivalent CHB design to drive the 13.8 kV motor

The 13.8kV motor can be driven with the CHB topology shown in Fig. 61. The number of Cascaded H-Bridges is chosen to have a similar voltage stress on the devices as the IMMC design shown in Fig. 59. The required DC voltage for each CHB is calculated in (67).

$$VDC = \frac{\sqrt{2}\, V_{L-L,RMS}}{3\sqrt{3}} = 3756V \tag{67}$$

The voltage stress on the devices is the same as the DC voltage. The current rating of the devices is calculated in (68).

$$I_{sw-RMS} = \frac{I_{Load-RMS}}{\sqrt{2}} = 85A \tag{68}$$

3.2.2 Simulation Results

This IMMC simulation is designed with the same ratings of a 13.8 kV commercialized ABB motor drive (ACS580MV). The motor drive comes in different power ratings that ranges between 200 kW – 6.3MW [34]. The proposed IMMC is a 19-submodule design using 6.5kV SiC devices as shown in Fig. 56. The VDC required to drive the motor is 22535V (without third harmonic injection).

The values of the capacitors and inductors are chosen to minimize the voltage and current ripples on the passive components. The motor is simulated as an R-L load to have realistic simulation results as seen in Table 14.

Fig. 62 and Fig. 63 show the high quality sinusoidal output voltage and current of the proposed 19 SMs IMMC. Fig. 64 and Fig. 65 demonstrate the voltages of the 20 capacitors of the converter. The voltage across each capacitor is a slice of the output sinewave. Fig. 66 and Fig. 67 show the current through each inductor in the proposed converter.

Table 14 Simulation parameters

Grid Voltage Vab (kV)	13.8
Switching Frequency (HZ)	20000
Output Power (MW)	2.7
Inductor (μH)	100
Capacitors (μF)	50
Turns Ratio (N1:N11:N21)	1:1:1
Load Resistance (Ω)	60
Load Inductance (mH)	60

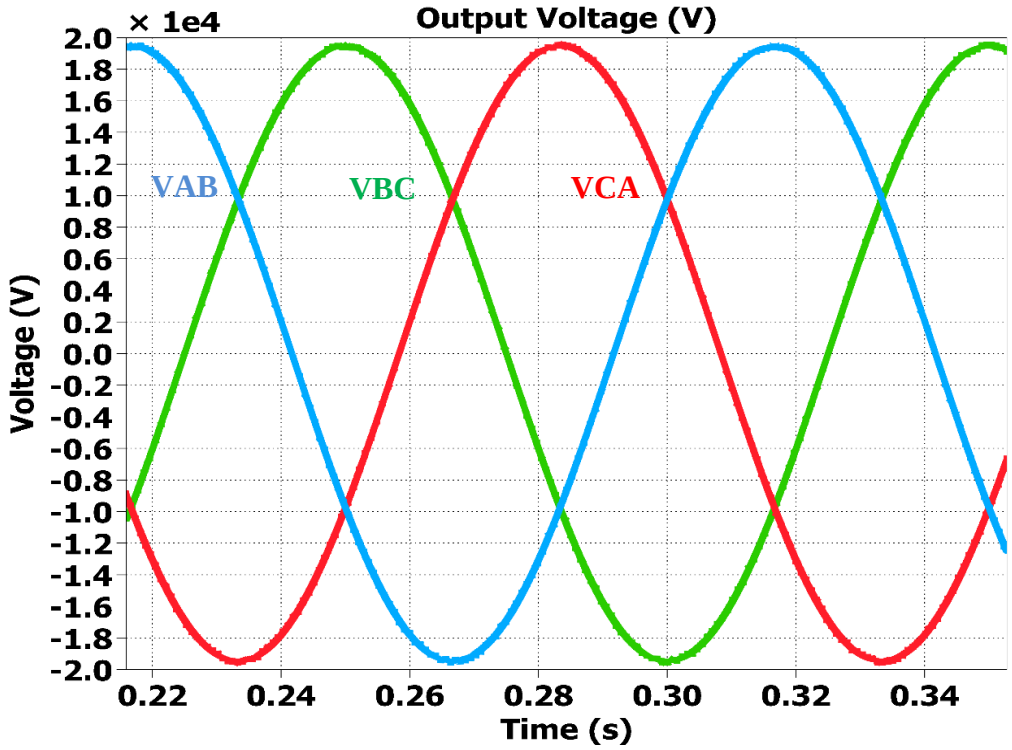

Fig. 62 The three-phase line-line output voltage of the IMMC.

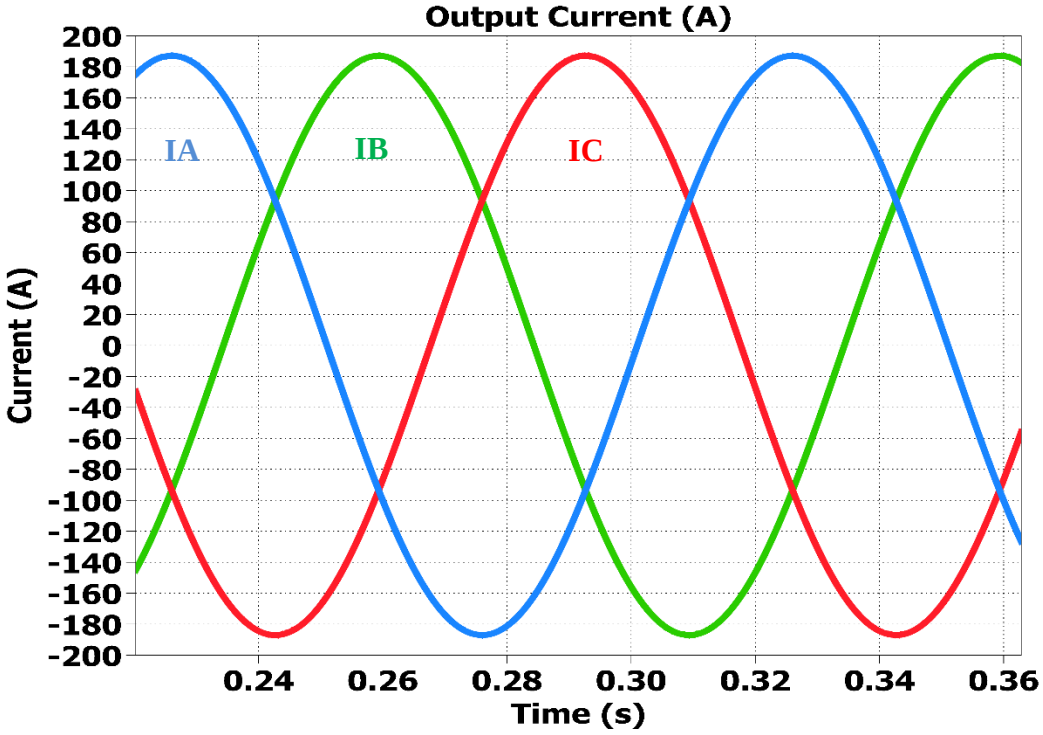

Fig. 63 The three-phase line-line output current of the IMMC.

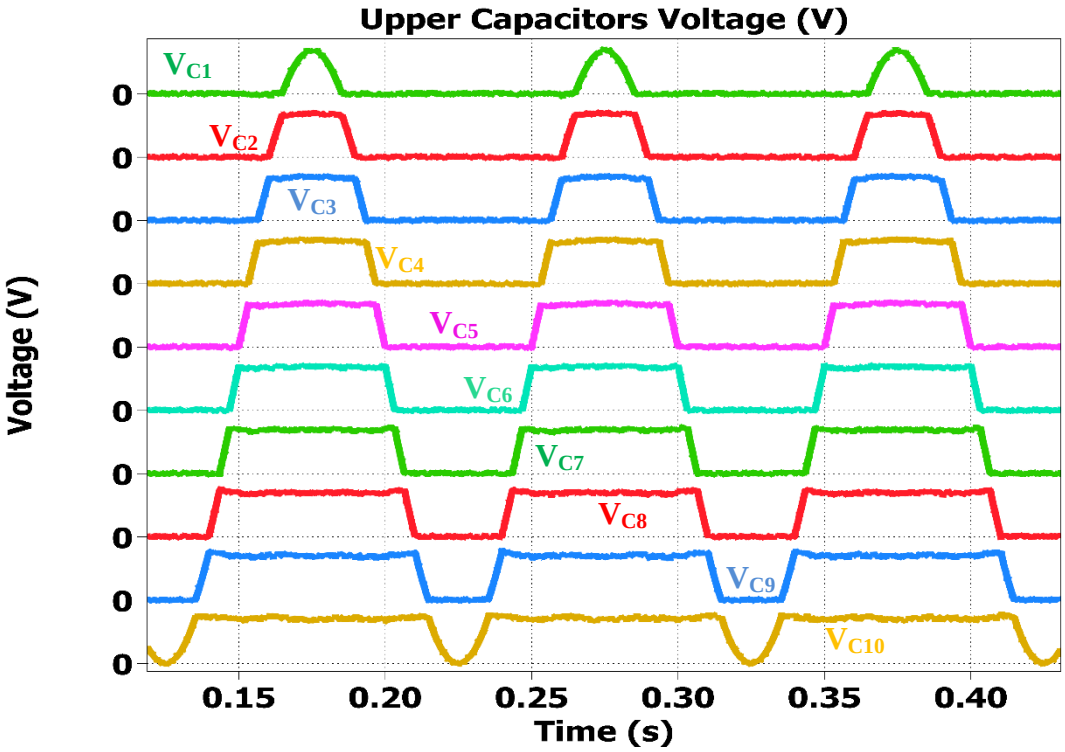

Fig. 64 The voltages of the upper capacitors (from C_1 to C_{10}).

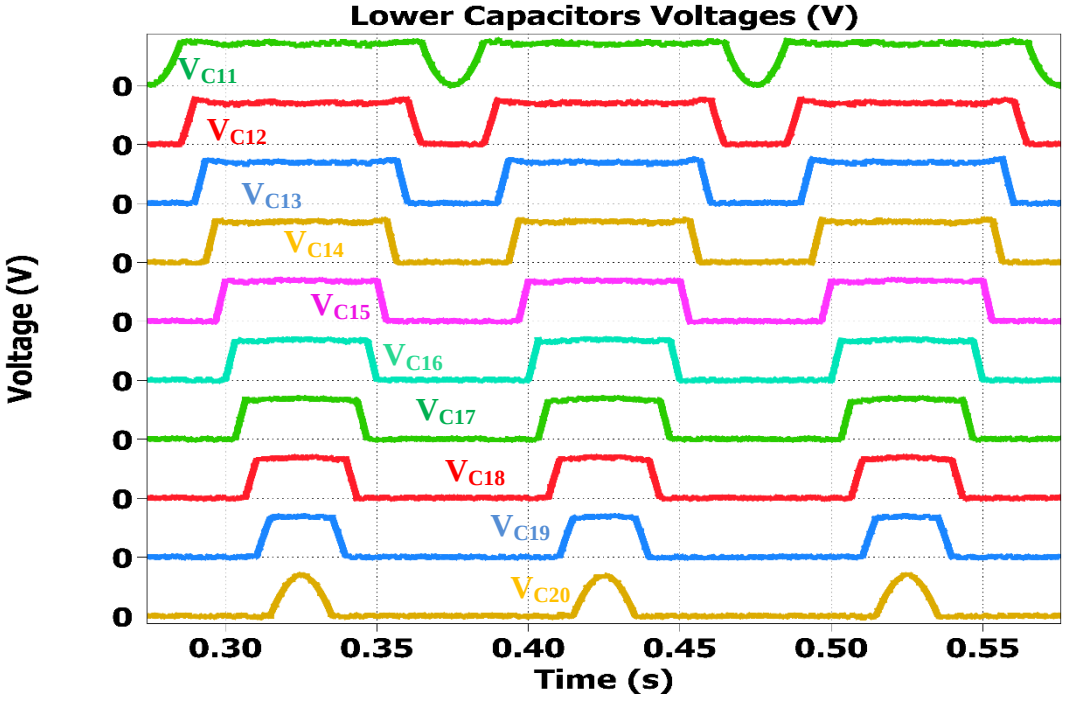

Fig. 65 The voltages of the lower capacitors (from C_{11} to C_{20}).

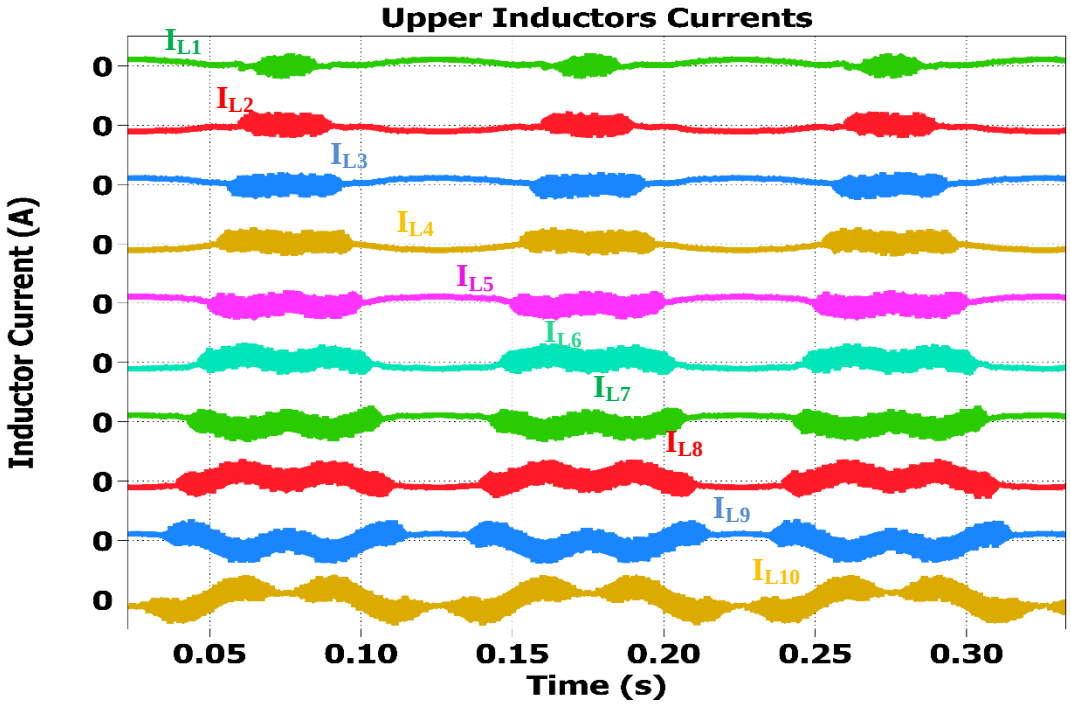

Fig. 66 The current through the upper inductors (from L_1 to L_{10})

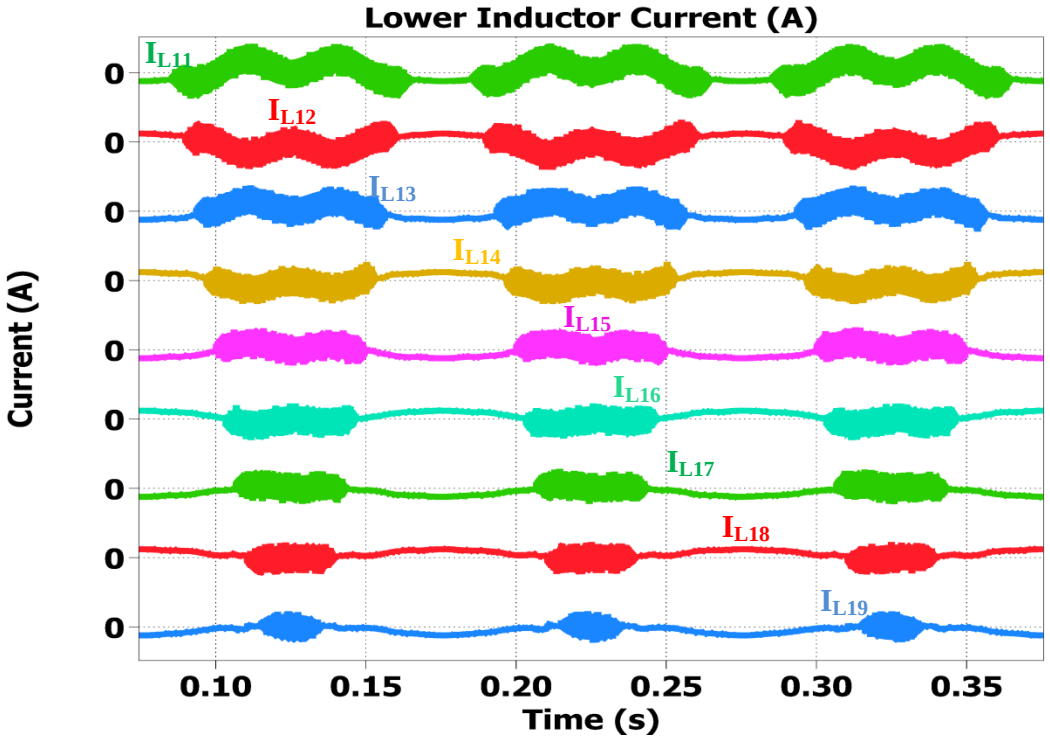

Fig. 67 The current through the Lower inductors (from L_{11} to L_{19})

3.2.3 Experimental Results

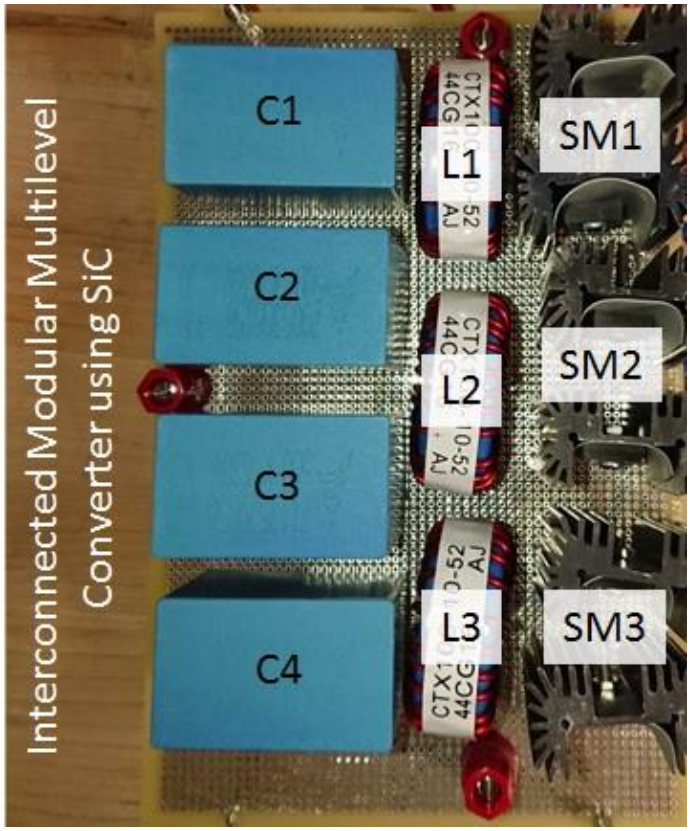

Fig. 68 The proposed IMMC using SiC devices.

Table 15 Experimental prototype parameters

Parameter	**Value**
Input voltage (V)	200
Switching Frequency (kHz)	15
Dead Time (ns)	200
Inductor (µH)	100
Capacitor (µF)	50
Load Resistor (Ω)	6.5
Load inductor (mH)	5

Another single-phase laboratory prototype is built using SiC devices to be proposed for higher power applications. The prototype is built using the three submodules design for the simplicity and to prove that the SiC IMMC provides a sinusoidal output with the minimum number of submodules. The hardware is tested for different input DC voltages and loading conditions. The switches used for the converter are LSIC1MO120E0080 SiC devices that are rated for 1200V and 25 A [35]. The devices are driven using the CREE CGD15HB62P1 gate driver board that can switch to a maximum switching frequency of 64 kHz [36]. However, since the target of the prototype is medium voltage motor drive, the switching frequency is chosen to be 15 kHz. The passive components size plays an important role in controlling the ripple on them. Therefore, inductors and capacitors are chosen to be 100 µH and 50 µF. The load is an RL-load with a resistor of 6.5 Ω and an inductor of 5mH to resemble the motor's load condition.

The hardware shown in Fig. 68 is tested for a wide range of frequencies. This section will demonstrate the operation of the converter with two out put frequencies of 60 and 30 Hz. Fig. 69 and Fig. 70 show the output voltage and current of the IMMC when the power factor of the load is lagging. The phase shift is 18.97^o when the output frequency is 60 Hz and 8.25^o when the output frequency is 30 Hz. Fig. 71 and Fig. 72 display the currents through the inductors when the output frequency is 60 Hz and 30 Hz respectively. Fig. 73 and Fig. 74 are the waveform of the capacitors voltages when the output is 60 and 30 Hz. Fig. 75 and Fig. 76 show the submodules voltages. The proposed IMMC is tested with a nonlinear load as seen in Fig. 77. The parameters of the nonlinear load seen in Fig. 77 are VDC=300V, R=60 ohm and C=870 uF. The inverter side voltage (V_{AO}), DC output voltage (V_R), current of the nonlinear load (I_R), are measured and displayed in Fig. 78.

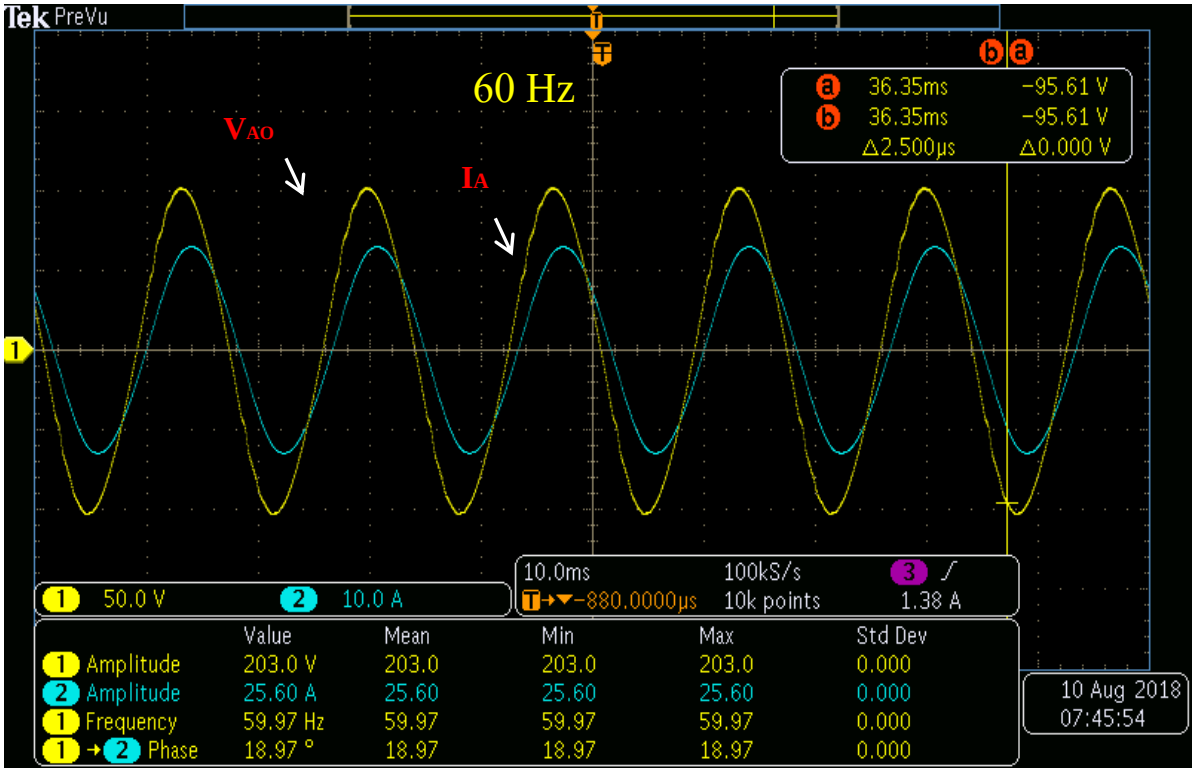

Fig. 69 The output voltage and current of the proposed SiC IMMC shown in Fig. 27 is a sinusoidal wave with a fundamental frequency of 60 Hz. The load is an RL-load with a phase shift of 18.97^{o}.

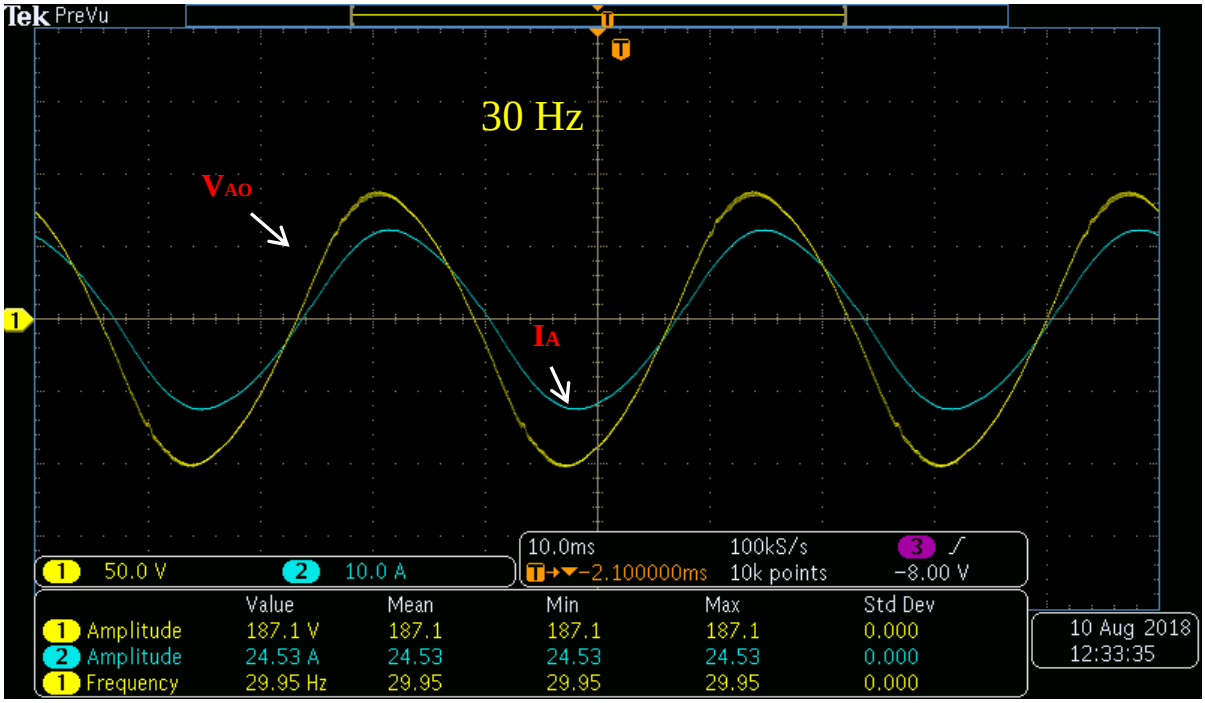

Fig. 70 The output voltage and current of the proposed SiC IMMC shown in Fig. 27 is a sinusoidal wave with a fundamental frequency of 30 Hz. The load is an RL-load with a phase shift of 8.25^{o}.

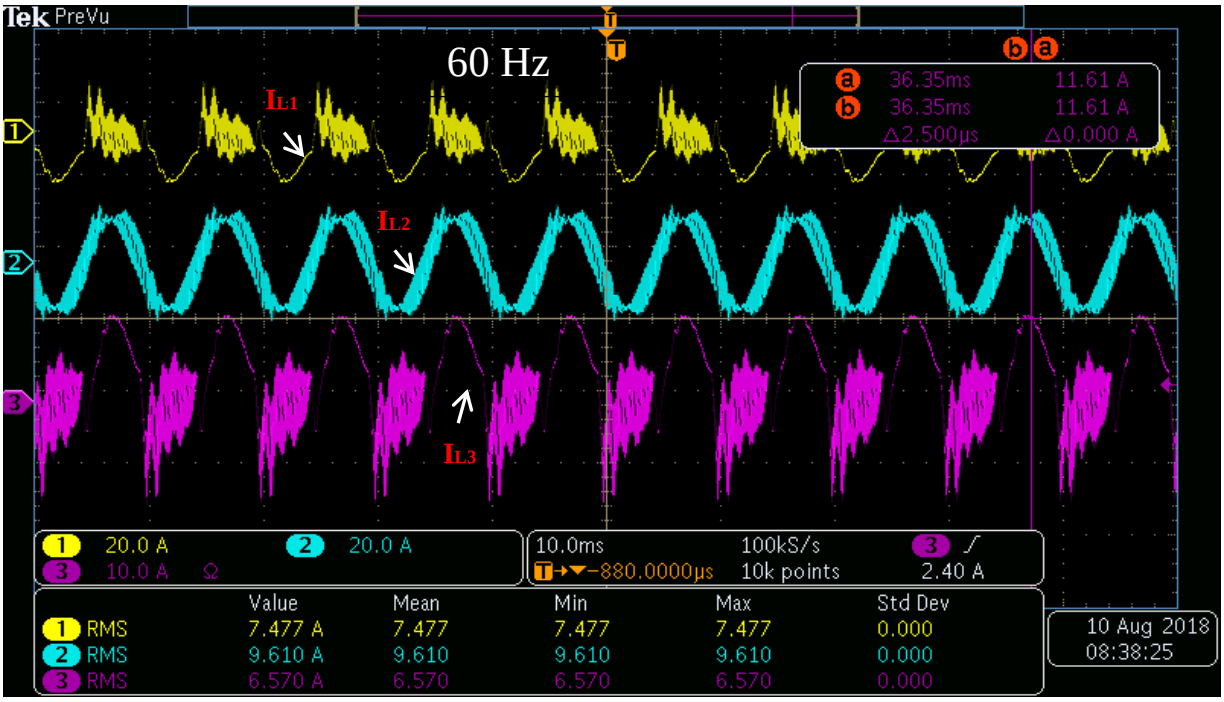

Fig. 71 The currents of the three inductors as seen in Fig. 27 when the output is 60 Hz. The ripple can be minimized by increasing inductor size or the switching frequency of the converter.

Fig. 72 The currents of the three inductors as seen in Fig. 27 when the output is 30 Hz. The ripple can be minimized by increasing inductor size or the switching frequency of the converter.

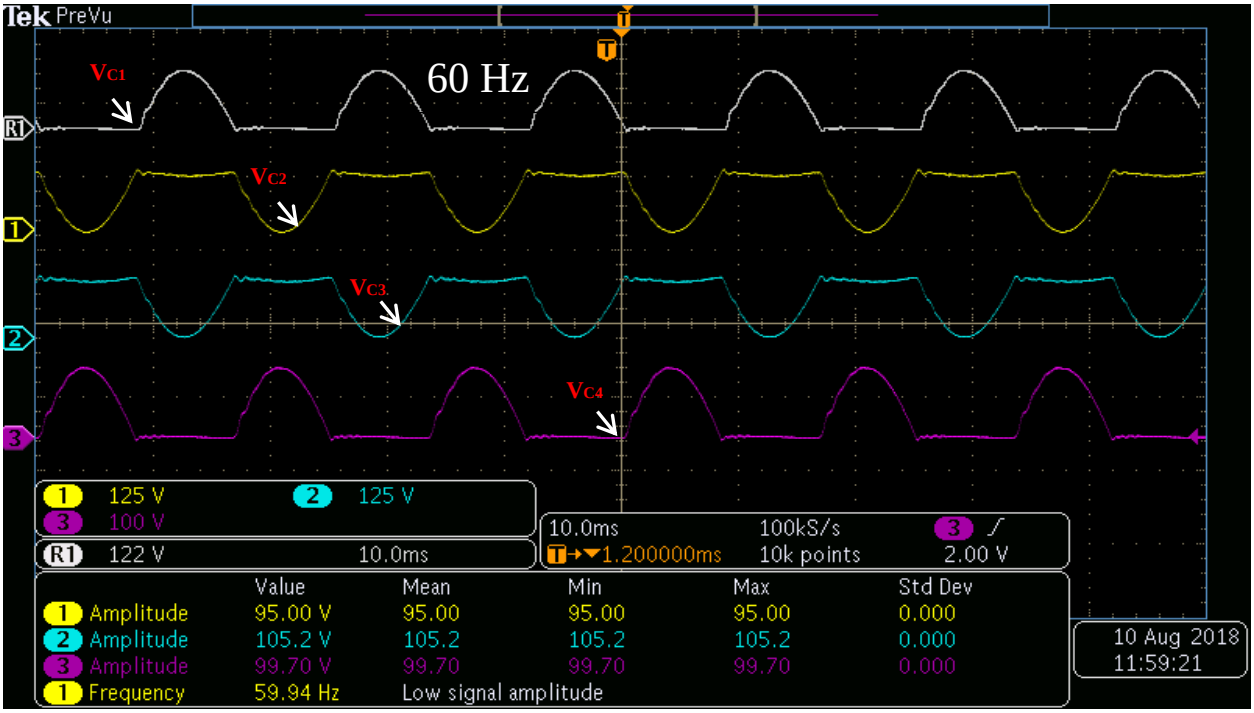

Fig. 73 The voltage across each capacitor when the output is 60 Hz as shown in Fig. 27 is a sliced sine wave which makes the sum of the output a full sinewave.

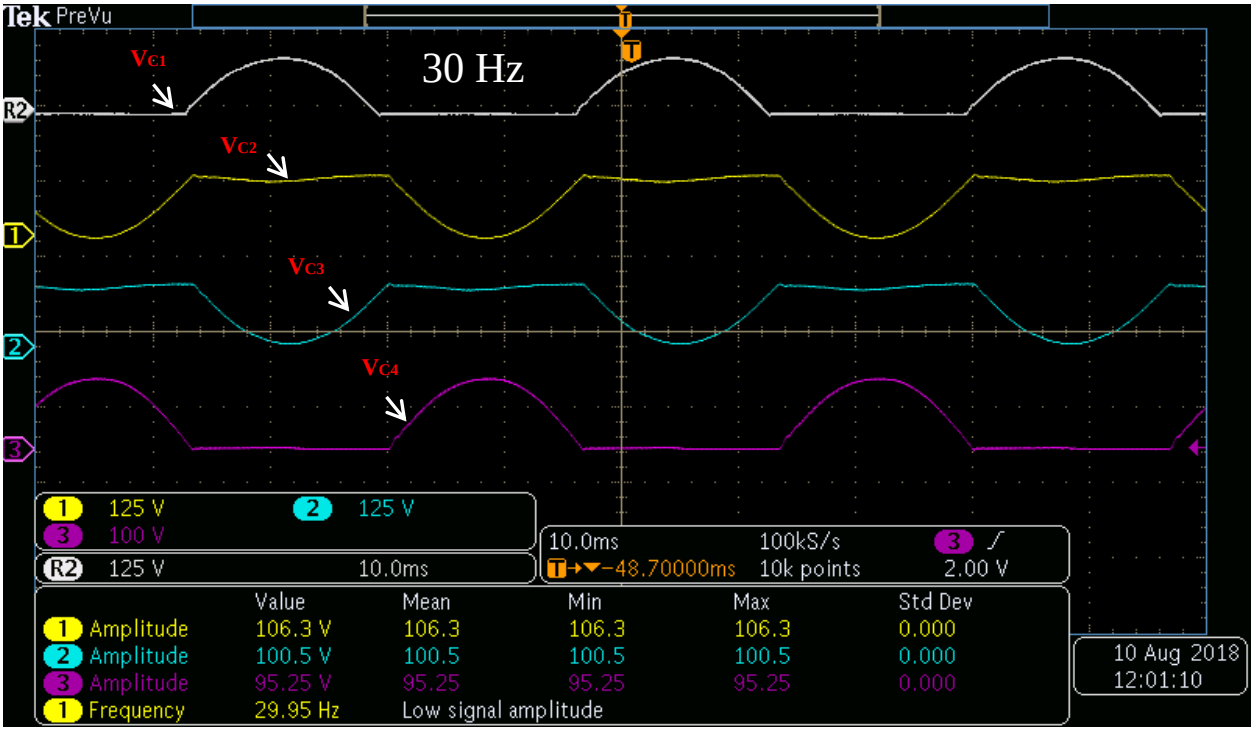

Fig. 74 The voltage across each capacitor when the output is 30 Hz as shown in Fig. 27 is a sliced sine wave which makes the sum of the output a full sinewave.

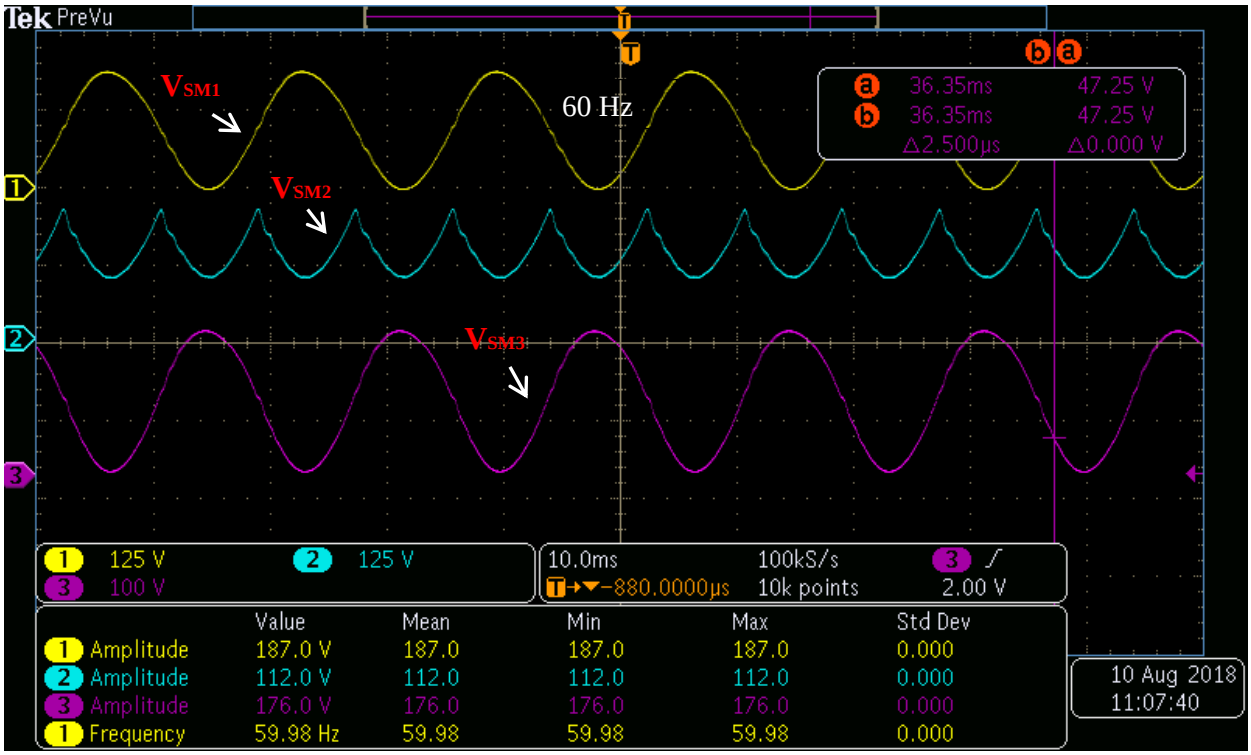

Fig. 75 Submodules voltages with 60 Hz shown in Fig. 27.

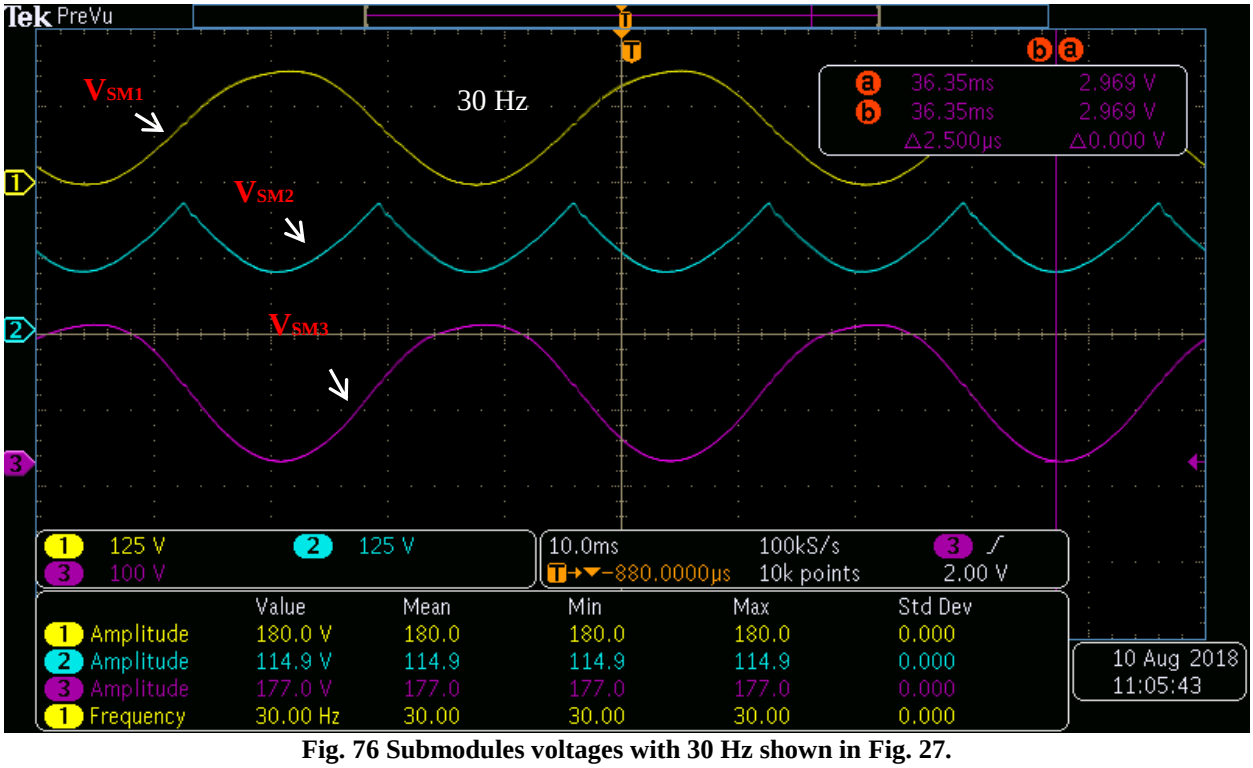

Fig. 76 Submodules voltages with 30 Hz shown in Fig. 27.

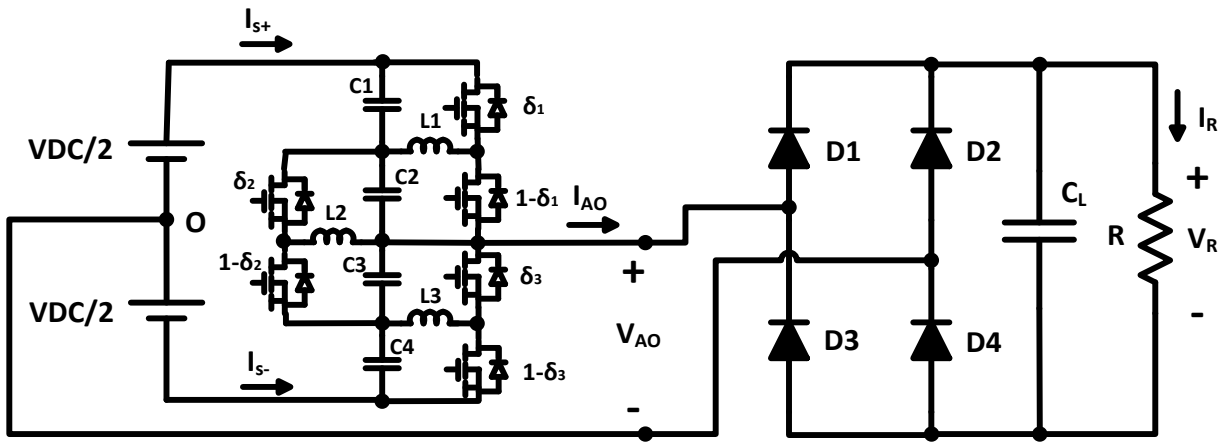

Fig. 77 Nonlinear rectified load is connected to the IMMC. VDC=300V, R=60 ohm and C=870 uF.

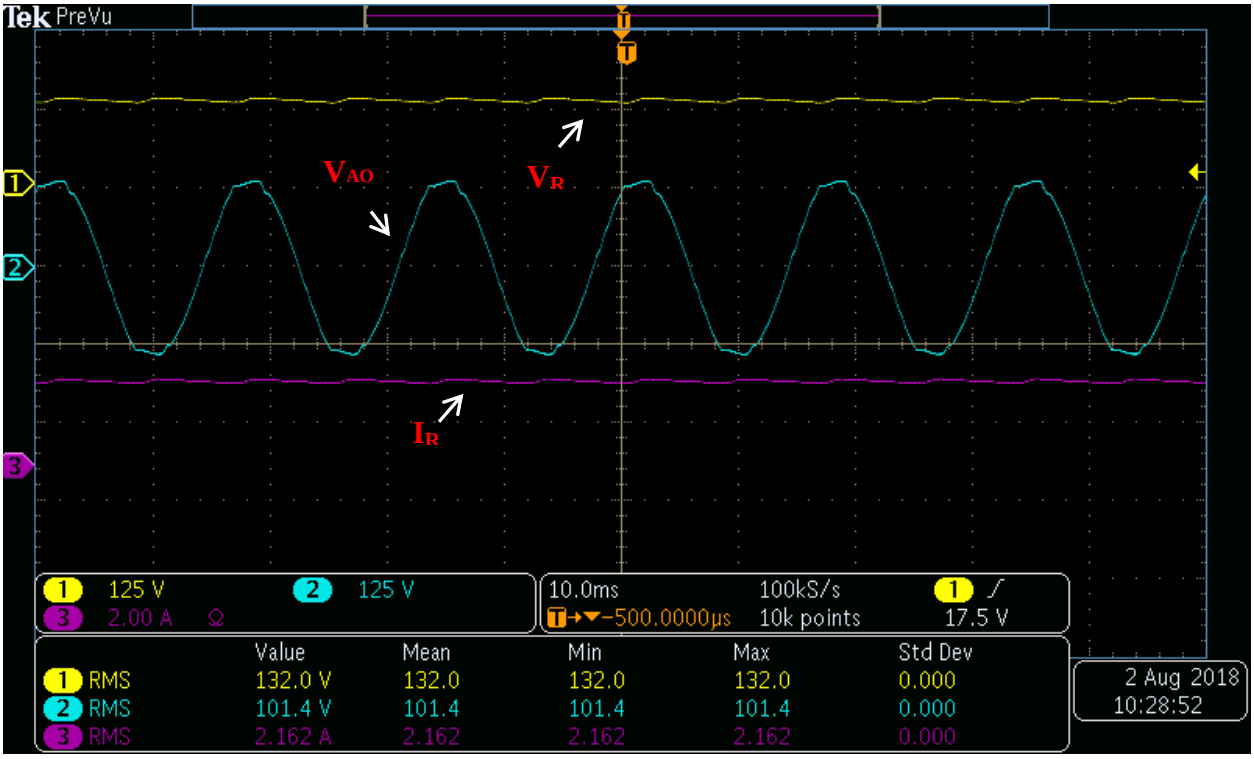

Fig. 78 The experimental result of the nonlinear load shown in Fig. 77.

4. SOLAR MICRO INVERTER*

4.1 Solar Photo-Voltaic (PV) Topologies

The grid-connected Photo-voltaic (PV) system consists of a PV module that converts solar irradiance into DC power. The DC power usually requires an inverter to convert it to an AC Power. The PV module is desired to operate at maximum power available because the solar irradiance changes throughout the day. The irradiance change impacts the output power from the PV system. Therefore, the PV system must take the irradiance change into consideration by performing Maximum Power Point Tracking (MPPT). The MPPT can be performed with a DC-DC stage before the inverter or by the inverter itself. However, the DC-DC stage is commonly used in several commercialized products to track the maximum power point and boost the voltage of the PV system to inject power to the electric grid.

When the solar system injects power to the grid, the voltage and frequency of the injected power from the solar system must be exactly similar to the grid. The value of the current is changed according to the available power from the solar system.

There are several topologies and configurations to harness solar energy from PV modules. The main themes of the configurations can be classified into (A) central inverter, (B) String inverter and (C) Micro inverters as seen in Fig. 79. The decision to use any of these configurations involves evaluating the trade-offs of each configuration with regards to the cost and overall efficiency that changes with partial shading conditions.

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A. Allehyani and P. Enjeti, "A New Modular Micro-inverter with Sinusoidal Output Voltage Using GaN Switches for PV Modules," 2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Charlotte, NC, 2018, pp. 1-6. Copyright 2018 by IEEE.

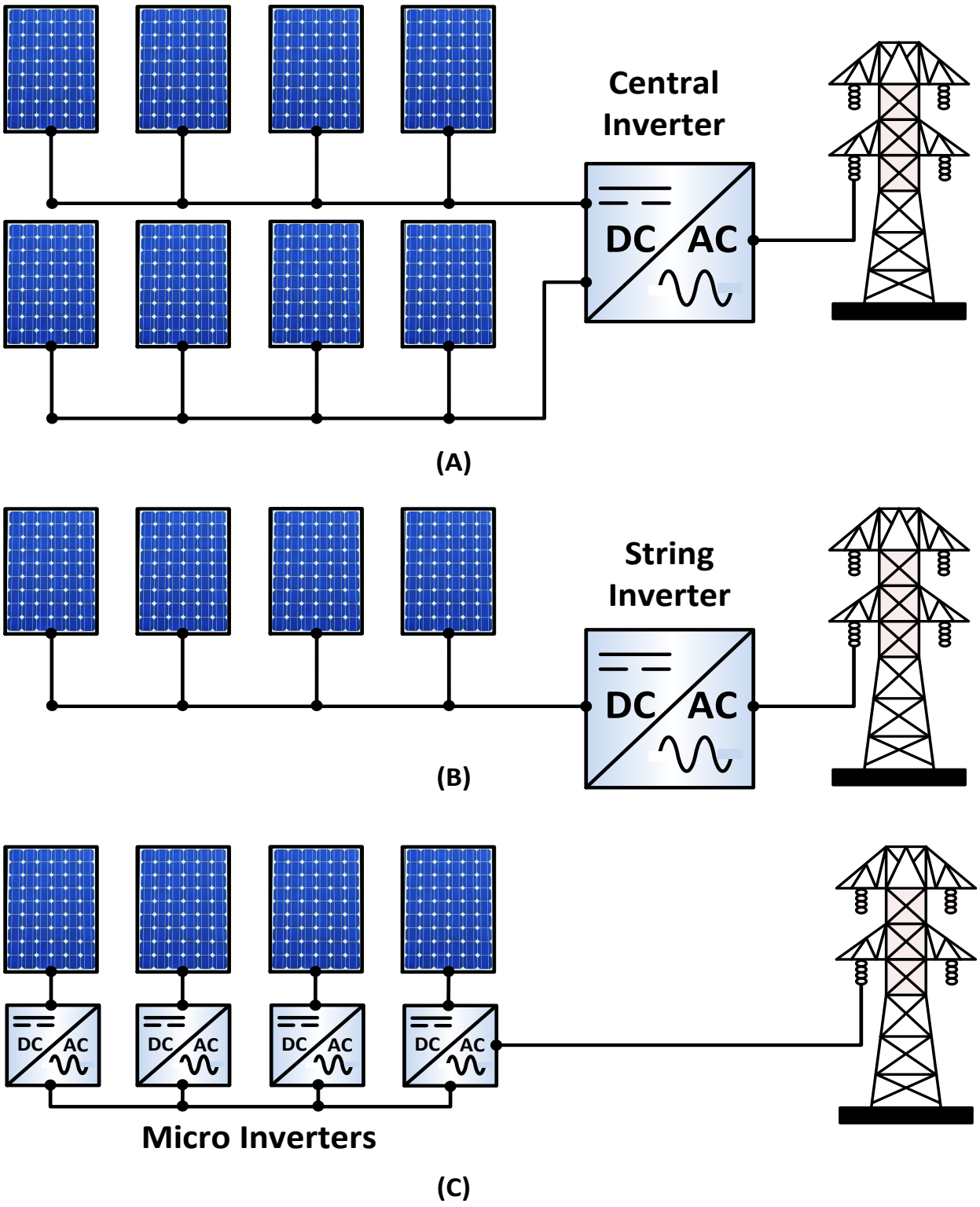

Fig. 79 The structures of PV energy harvesting systems (A) Central Inverter (B) String Inverter (C) Micro Inverters.

4.1.1 Central Inverter

The inverter in the central inverter scheme is centralized and used to connect several strings of PV modules as seen in Fig. 79 (A). The strings are connected in parallel to increase the power capability of the PV plant. Each string consists of several PV modules connected in series. The central inverter scheme suffers from several limitations such as higher number of high voltage DC cables to connect the strings to the central inverter. Moreover, the plant is operated at the centralized MPP not at the MPP for each PV module which mismatches the PV modules losses.

Advantages of Central inverter:

- Low capital cost.
- Fewer power electronics components.

Disadvantages of Central inverter:

- Less reliability (single point of failure)
- High current DC cables.

4.1.2 String Inverter

The string inverter is a more optimized version of the central inverter where each string of PV modules is connected to an inverter as shown in Fig. 79 (B). Therefore, operating at the MPP of the PV string which improves the energy harnessing compared to the string inverter structure. However, the string inverter still does not operate at the PV module MPP, it operates at the string MPP which decreases the power harnessed. Additionally, if there is shading on one of the PV modules, it would impact the entire string reducing the overall power of the string as seen in Fig. 80 and Fig. 81 [37].

Advantages of String inverter:

- More energy harnessing compared to central inverter.
- Modularity and reliability.

Disadvantages of String inverter:

- Performance impacted drastically based on one PV module condition.
- Energy harnessing not optimized.

4.1.3 Micro Inverter

The micro inverter configuration is seen in Fig. 79 (C). Each PV module is connected to an inverter. Each micro inverter is connected to the back of the PV module to maximize the harvested energy and enable MPPT for each PV module. Therefore, eliminating the loss mismatch that occurs in the central and string inverters due to partial shading conditions. Moreover, using micro inverters gives the PV plant the option of future expandability and increase the systems availability. However, micro inverters have several drawbacks such as high capital cost due to the use of more power electronics components.

Advantages of micro inverter:

- MPPT for each PV module.
- More system availability.
- Low current cables.

Disadvantages of micro inverter:

- High initial cost.
- Complex maintenance.

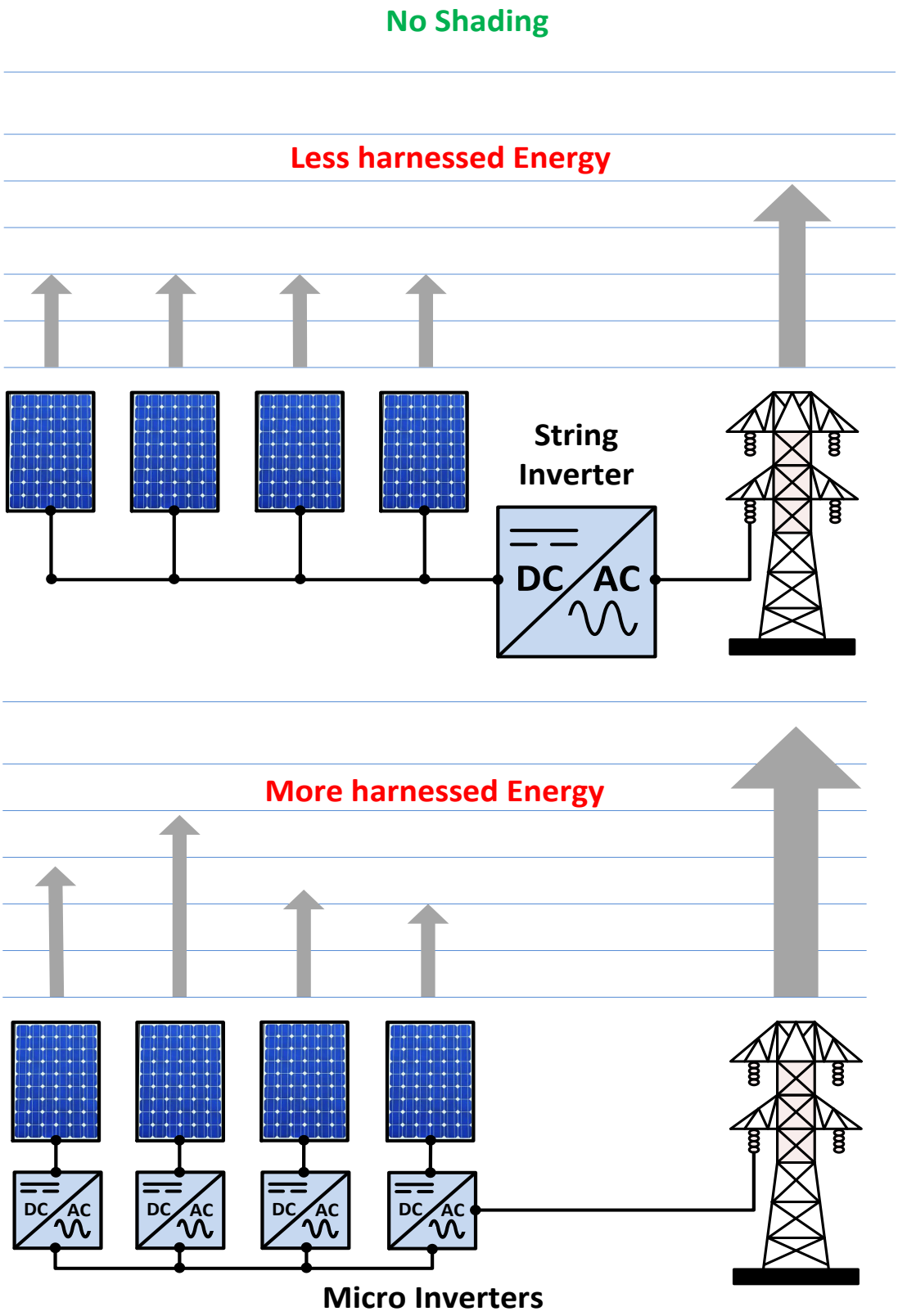

Fig. 80 harnessed energy comparison between string and micro-inverters with no shading conditions

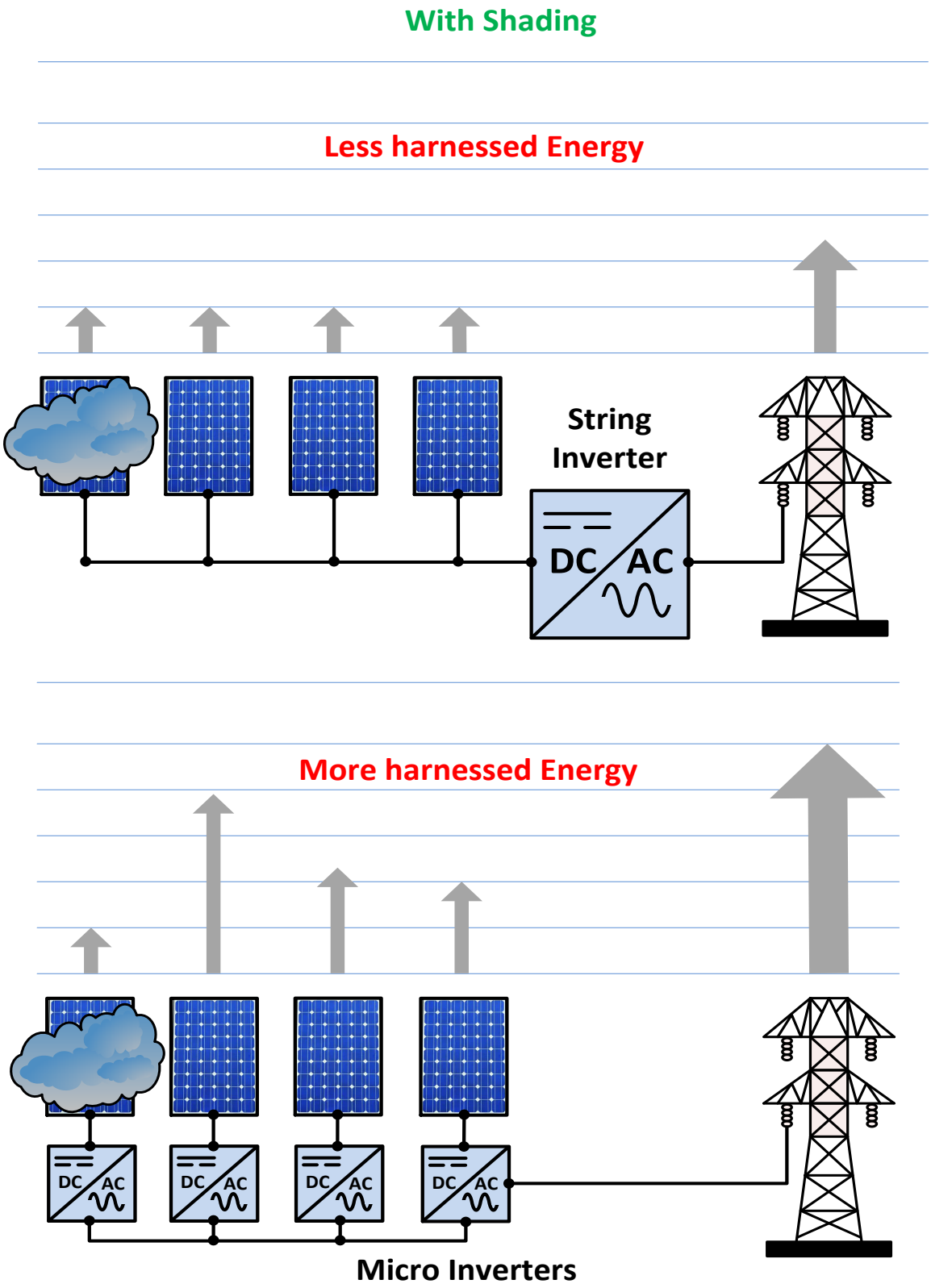

Fig. 81 harnessed energy comparison between string and micro-inverters with shading conditions

Isolation is required in many countries around the world (including the United Stated) for safety purposes. Moreover, the transformer isolation gives a chance to step up the voltage to a higher level compared to the traditional DC-DC converter. For example, the classic boost converter cannot achieve high conversion ratio. Therefore, galvanic isolation helps in stepping up the voltage to the grid level in order for the inverter to be able to inject power to the electric grid.

In the earliest stage of micro inverters developments, the isolation was done using a line frequency transformer. However, the line frequency transformer was bulky and expensive. Therefore, high frequency transformer was proposed to increase the efficiency and decrease the size of the transformer as shown in Fig. 82. Higher switching frequencies can be achieved using GaN devices while maintaining high efficiency.

The proposed converter in this chapter uses the double stage scheme for micro inverters shown in Fig. 83. The DC-DC stage performs the important task of stepping up the voltage from the PV panel to the desired DC bus voltage in order for the inverter to synchronize the output of the micro inverter to the grid. In other words, the DC-DC stage is responsible for regulating the DC bus voltage with the variation of operating conditions of the PV module. The typical PV panel voltage is 40 V, the DC-DC stage steps it up to 400V if the grid voltage is 120 Vrms. Additionally, The DC-DC converter is required to have high efficiency under any operating conditions as the PV module performance vary with environmental conditions such as temperature and solar insolation. Moreover, the DC-DC must be a high-power density converter with high efficiency to reduce the overall cost of the micro inverter. There are several DC-DC topologies that were proposed for micro-inverter applications. The most common topology for the DC-DC stage is the flyback converter due to the simple structure and isolation capability.

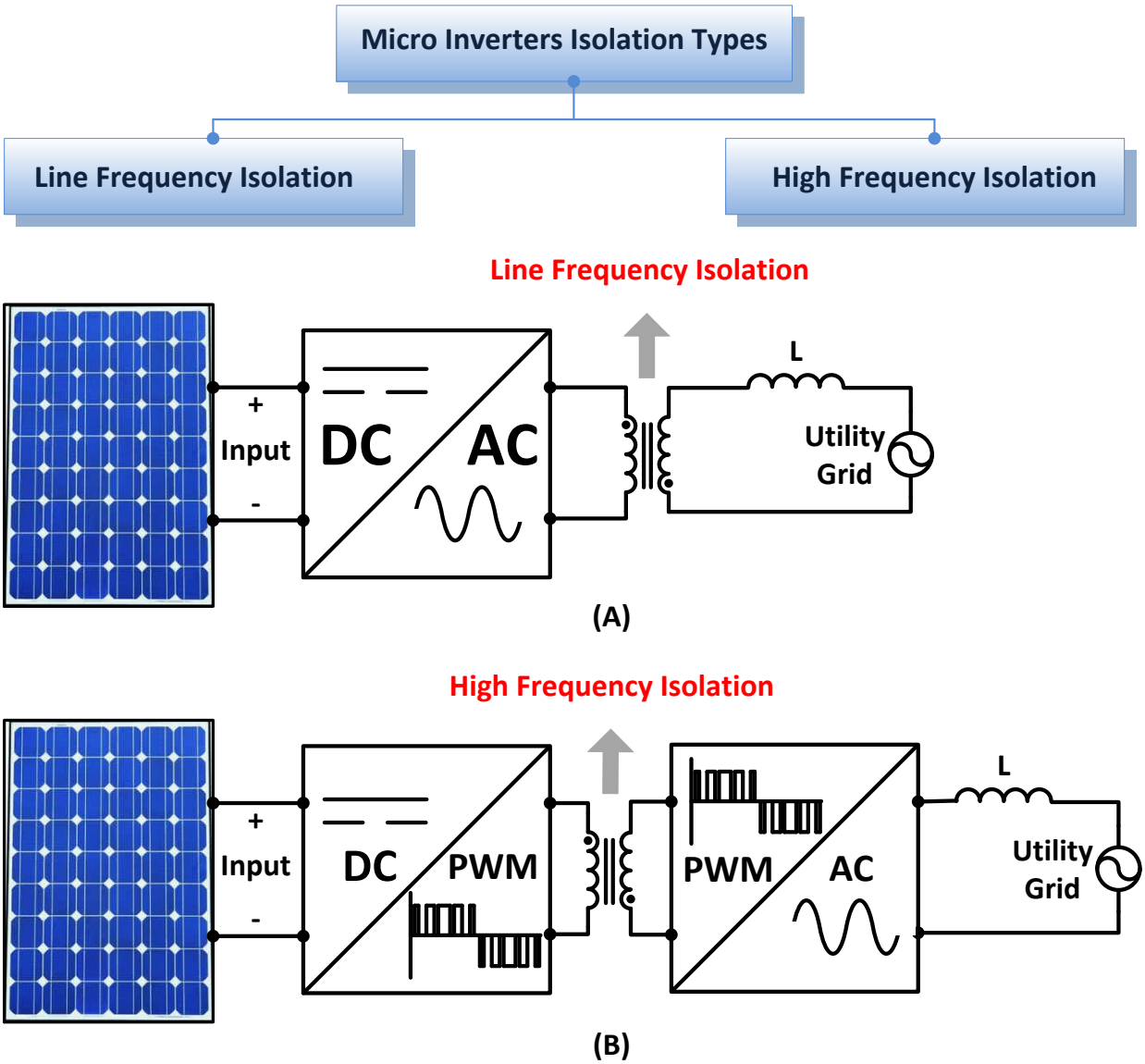

Fig. 82 Micro inverters isolation using: (A) Line frequency transformer (B) High frequency transformer.

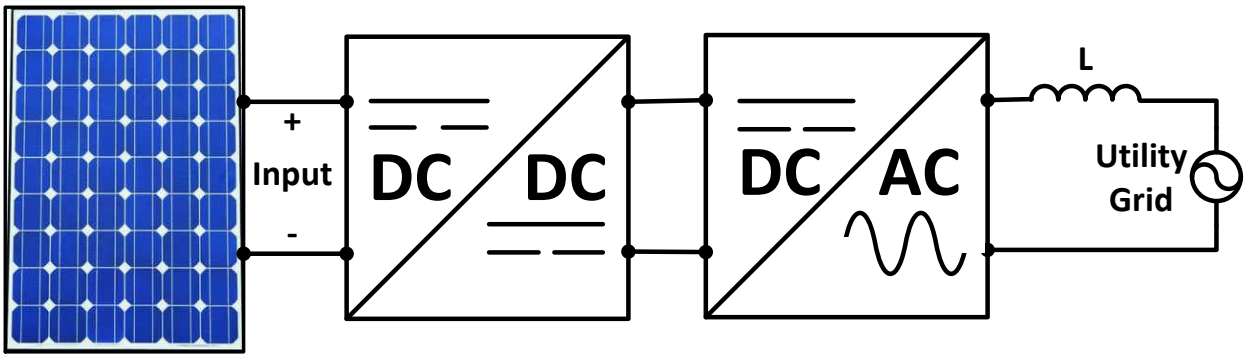

Fig. 83 Two Stage Micro-inverter.

4.2 Problem Definition

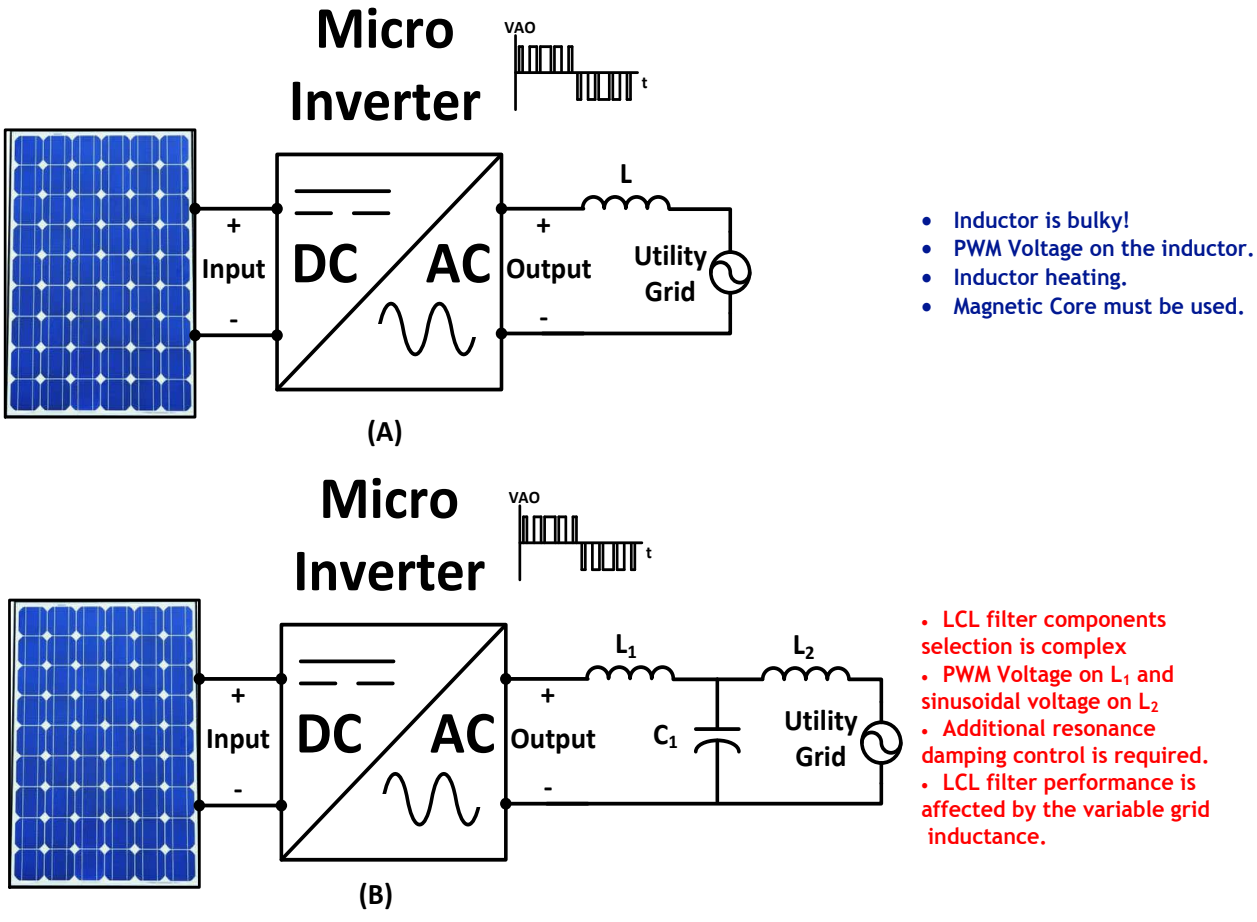

Fig. 84 Conventional methods to connect micro inverters to the grid using (A) L-filter (B) LCL-filter

Micro-inverters have been a hot topic recently in the industry to maximize the efficiency harnessed from the Photo-Voltaic (PV) panels. Micro-inverters have been commercialized by companies such as Enphase and SunPower with an output power range of 200W-400W. Most available micro-inverters from major suppliers are based on the flyback converter [38]. A popular structure of the micro-inverter is the PV panel connected to an inverter through a DC-DC converter. The inverter is connected to the utility to inject power to the grid. However, PWM inverters are switching using PWM technique that results a high dv/dt and di/dt on the output. The high dv/dt and di/dt can flow to the grid causing serious safety concerns [39]. Therefore, an output filter is essential to meet the grid requirements to interconnect distributed resources in the IEEE P1547.2-2003 standards [40]. The output filter can be a first order single inductor as shown in Fig. 84 (A). Nonetheless, the single inductor is inefficient and bulky [41]. Another widely used option is the LCL filter as seen in Fig. 84 (B) to reduce the size and improve the performance of the filter. However, the design and parameter selection of the LCL filter is complex. LCL filter requires extra control to provide resonance damping and stabilize the system [42]. Also, the performance of the LCL filter can be affected by the grid inductance which changes based on the grid conditions [43]. Moreover, the voltage across the inverter side inductor is a PWM voltage with switching frequency components. Thus, increasing the magnetic losses in the magnetic core and causing the inductor to overheat.

4.3 Proposed Topology

The proposed modular micro-inverter in Fig. 85 produces a sinusoidal output voltage and therefore can seamlessly interconnect with the grid requiring only a line frequency inductor. Fig. 85 (B) shows the IMMC structure with five submodules employing lower voltage GaN switches. The proposed modular micro-inverter solves several common PWM inverter problems as well and it has the following advantages:

- The output voltage is sinusoidal and distortion free with low EMI.
- No need for output filter since it is integrated within the converter topology.
- Grid-interface inductor is small due to the sinusoidal nature of the output voltage.
- Iron core can be used for the grid-tie inductor.
- Capacitors and inductors are smaller due to high frequency operation.
- Ability to employ low voltage GaN devices in a multilevel configuration (Fig. 85 (B)).
- Compact transformer size due to the use of a GaN switch in the flyback.

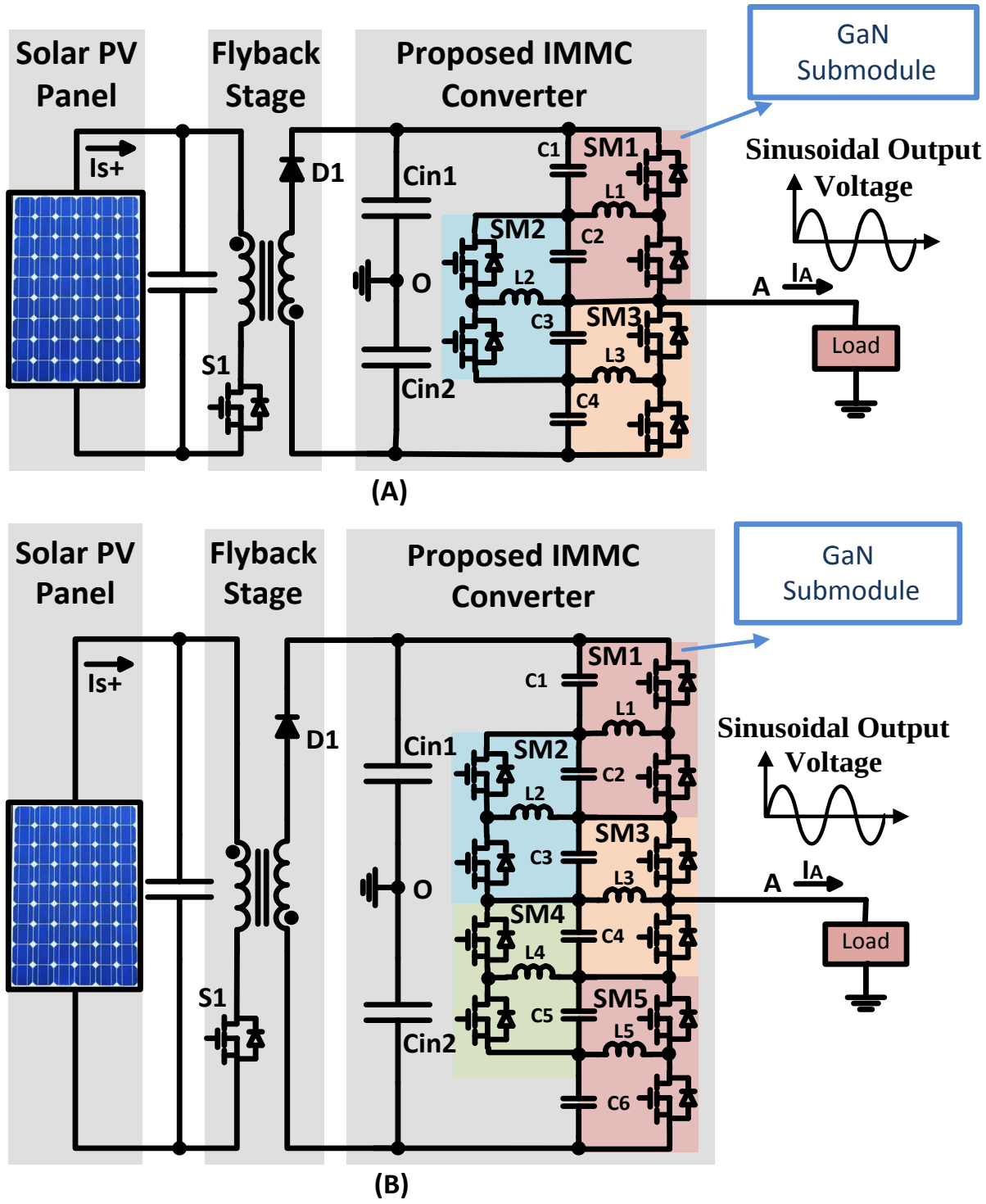

Fig. 85 The proposed micro-inverter (A) Three submodules (B) Five submodules stacked design to reduce the voltage stress on the GaN switches.

4.4 Inverter Control

Controlling a fixed component is easier than a changing component because it is more convenient for the controller to track constant values. For AC systems, control is usually done in a rotating dq frame in which AC components appear constant. The transformation to the dq frame for three phase systems is achieved by abc to αβ frame transformation and then αβ to dq frame transformation.

The αβ to dq frame transformation requires two orthogonal signals (αβ). For single phase systems, there is only one component. Therefore, to perform the current control in the dq frame, fictitious variables must be generated in order for the dq transformation to have two values. The α value represents the actual measured current in the system and the β value is only generated to do the dq transformation and it can be ignored.

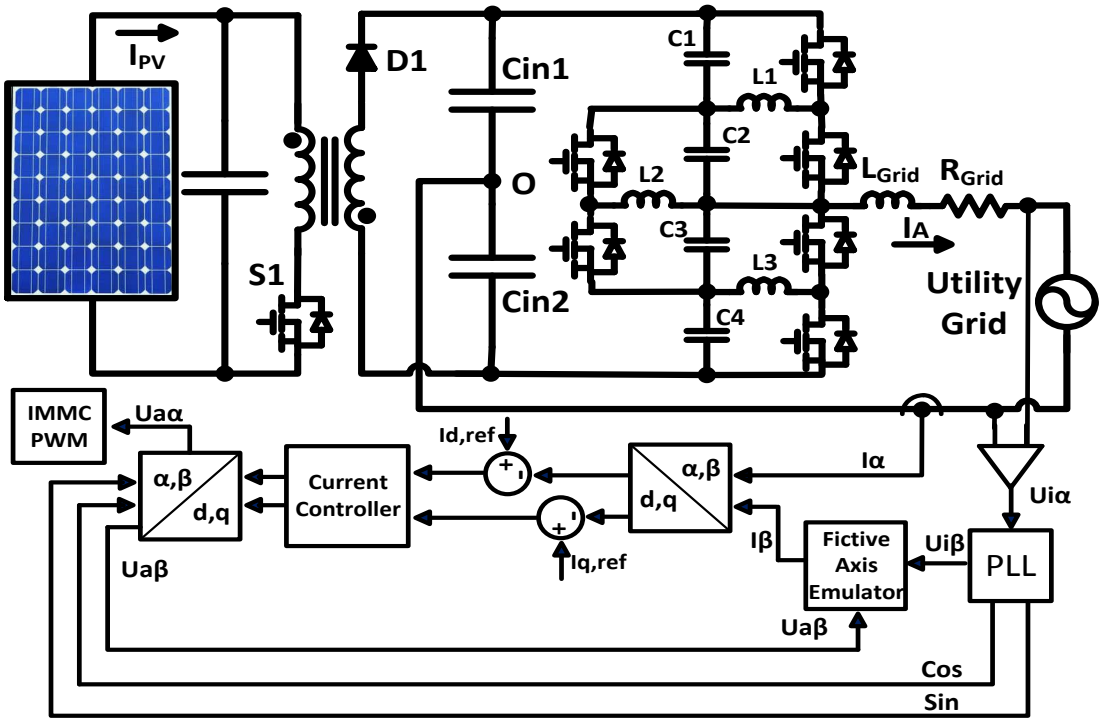

Fig. 86 Inverter current control using Fictive-Axis Emulation [44]

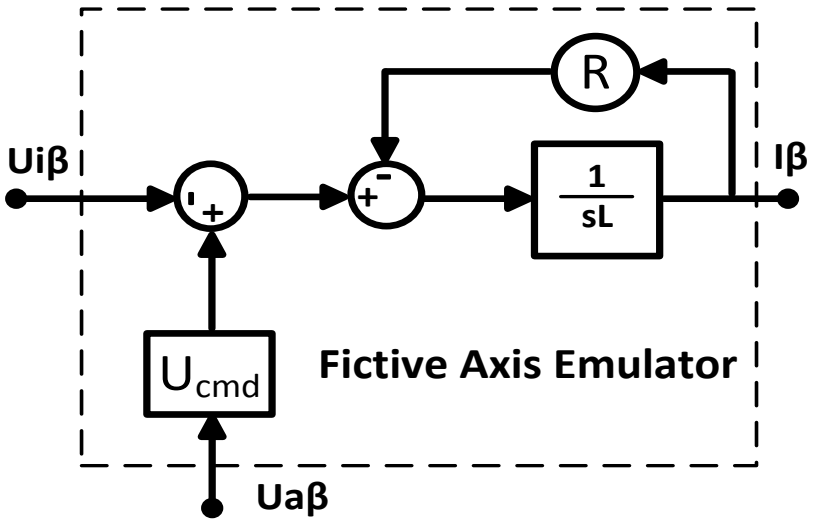

Fig. 87 Under mask diagram of the Fictive Axis Emulator [44].

Fig. 86 shows inverter current control using the Fictive-Axis Emulation (FAE) Current Control proposed in [44]. The fictitious β component of the current is created from the grid voltage measurement. The reference phase angle is generated for the αβ to dq transformation using a Phase Locked Loop (PLL) utilizing the second order generalized integrator (SOGI).

The current's orthogonal β component is concurrently generated using FAE. The voltage space phasor's imaginary component is obtained by feeding the voltage measurement to the PLL. After that, the orthogonal β component is emulated by the Fictive Axis Emulator block as shown in Fig. 87. The α component and the emulated β components are transformed to the rotating dq frame where the control takes place. Then, the quantities are transformed back to the stationery αβ frame. The α component is fed to the IMMC modulation block explained in [21] and the gate signals are fed to the switches and β is fed back to the FAE block. The block Ucmd is introduced to compensate for the fictive PWM modulator delay time constant.

4.5 Flyback

4.5.1 Boundary Condition Mode (BCM)

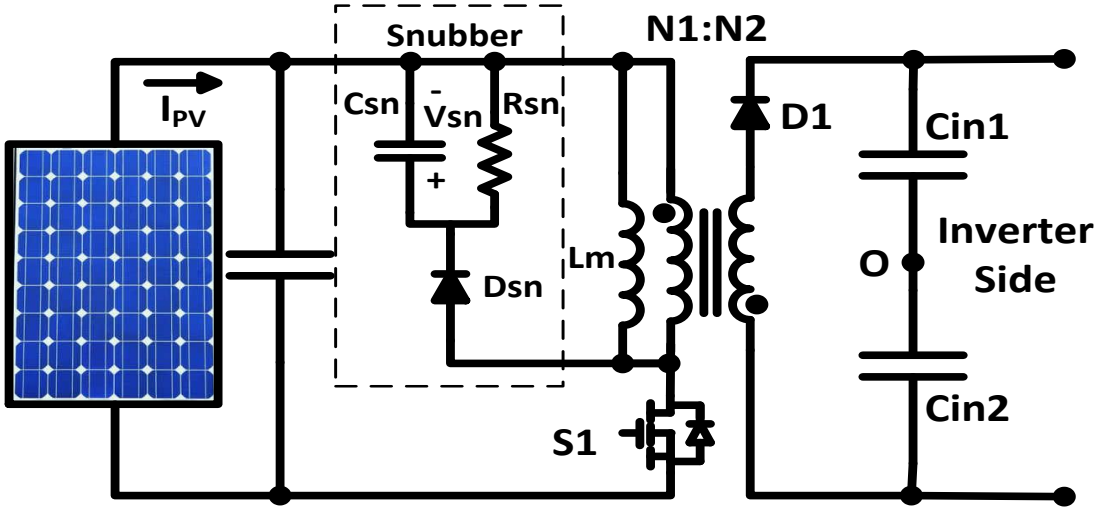

Fig. 88 The snubber circuit used for the flyback converter.

The flyback converter is used as a DC-DC converter to provide isolation, boost the voltage and operate at the maximum power point (MPP). Flyback is used due to its simple structure and low component count compared to other topologies.

The flyback can be designed in the Boundary Condition Mode (BCM) region where the input current reaches zero. When the current is zero, the zero-current switching (ZVS) can be implemented to reduce the switching losses and maximizing the efficiency. Moreover, BCM operation eliminates the diode reverse recovery losses because the current through diode decays to zero. The primary peak current (i_{pri-pk}) is calculated in (69).

$$i_{pri-pk} = \frac{V_{in} t_{on}}{L_m} \tag{69}$$

The leakage inductance (L_k) associated with the flyback transformer resonates with the parasitic capacitance of the switch S1 causing excessive voltage that can damage the switch. Thus, snubber circuit must be introduced to absorb and reduce the resonance voltage. A common snubber circuit is the RCD circuit shown in Fig. 88. The design equations for the RCD snubber are derived in [45]. The power absorbed by the snubber circuit (P_{sn}) is calculated using (70). The snubber resistance (R_{sn}) is calculated in (71) based on the power absorbed by the snubber circuit. The capacitor value (C_{sn}) is then calculated as shown in (72).

$$P_{sn} = \frac{1}{2} L_k {i_{pri-pk}}^2 \frac{V_{sn} f_s}{V_{sn} - \frac{N_1}{N_2} V_o} \tag{70}$$

$$R_{sn} = \frac{{V_{in}}^2}{\frac{1}{2} L_k {i_{pri-pk}}^2 \frac{V_{sn} f_s}{V_{sn} - \frac{N_1}{N_2} V_o}} \tag{71}$$

$$C_{sn} = \frac{V_{sn}}{\Delta V_{sn} R_{sn} f_s} \tag{72}$$

4.5.2 Design Example

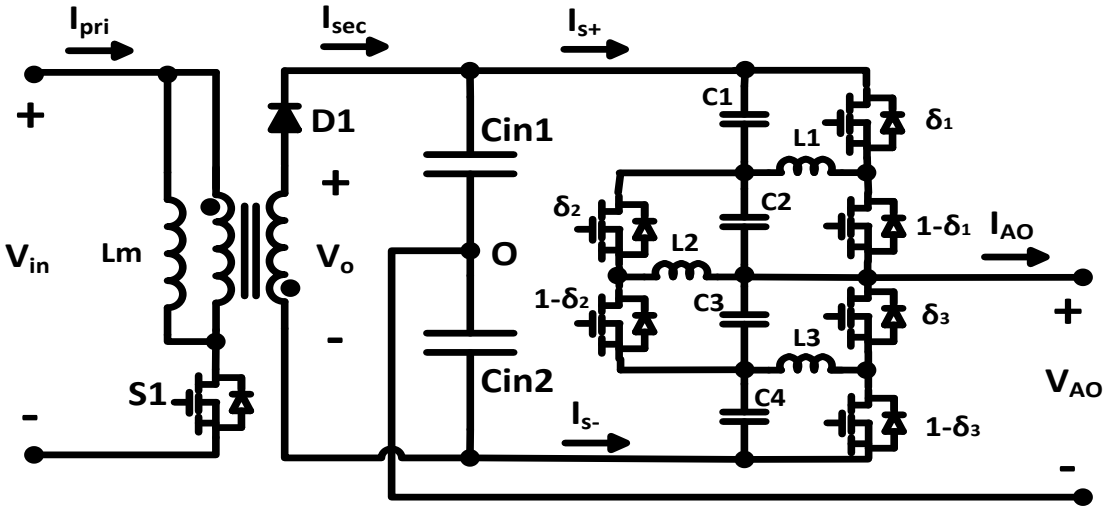

Fig. 89 The proposed topology.

Table 16 Design Example Parameters

Flyback	
Power (W)	500
Vin (V)	40
Vo (V)	340
$f_{s\text{-}flyback}$ (Hz)	100000
N_1:N_2	1:4
IMMC	
$V_{AO\text{-}RMS}$ (V)	120
C_{IMMC}(µF)	2.2
L_{IMMC}(µH)	100
$f_{s\text{-}IMMC}$ (Hz)	200000

The design example shown in Table 16 is for a 500 W PV panel. The input voltage to the flyback stage is 33 V and the output must be 340V in order for the inverter to match it to the grid voltage which is 120 VRMS. The flyback is designed to operate at BCM at full power to enable ZVS at the main switch S1. The switching frequency and primary to secondary turns ratio are chosen 30 kHz and 1:4 for the flyback respectively.

For Flyback converter: The duty cycle (D) of switch S_1 is found by the transfer function of the flyback converter as shown in (73).

$$\frac{Vo}{Vin} = \frac{D.N2}{(1-D).N1} \gg D = 0.62 \tag{73}$$

The leakage inductance to achieve BCM is calculated in (74).

$$Lm = \frac{Vs^2 D^2 \eta}{2\, fsw\, Po} = 6\ \mu H \tag{74}$$

The RMS current rating of the flyback switch S_1 shown in (Fig. 89) is calculated in (75).

$$I_{s1-RMS} = I_{pri-RMS} = \sqrt{\frac{D}{3}} \frac{Po}{0.5\eta * Vin * D} = 21.9A \tag{75}$$

The blocking voltage of the flyback switch S_1 and the flyback diode D_1 are found in (76) and (77) respectively.

$$V_{Flyback-switch} = Vin + \frac{N1}{N2} Vo = 125\ V \tag{76}$$

$$V_{Flyback-Diode} = Vo + \frac{N2}{N1} Vin = 500\ V \tag{77}$$

For the IMMC converter: The capacitors RMS current ratings in (78), (79), (80) and (81) are calculated when the PV panel operates at maximum power (500W).

$$I_{C1} = -\delta_1 * I_{L1} + I_{s+} = 1.2\ A \tag{78}$$

$$I_{C2} = (1 - \delta_1) * I_{L1} - \delta_2 * I_{L2} + I_{s+} = 1.375\ A \tag{79}$$

$$I_{C3} = (1 - \delta_2) * I_{L2} - \delta_3 * I_{L3} - I_{s-} = 1.375\ A \tag{80}$$

$$I_{C4} = (1 - \delta_3) * I_{L3} - I_{s-} = 1.2\ A \tag{81}$$

Similarly, the inductor RMS current ratings in (82), (83) and (84) are calculated when the PV panel operates at maximum power (500W).

$$I_{L1} = \frac{I_{s+} - I_{C1}}{\delta_1} = 2.833\ A \tag{82}$$

$$I_{L2} = \frac{I_{C3}}{1 - \delta_2} + \frac{\delta_3}{(1 - \delta_2)(1 - \delta_3)} I_{C4} + \frac{1 + \delta_3}{(1 - \delta_2)(1 - \delta_3)} I_{s-} = 4.5833\ A \tag{83}$$

$$I_{L3} = \frac{I_{C4} + I_{s-}}{1 - \delta_3} = 2.833\ A \tag{84}$$

The blocking voltage of the IMMC switches is calculated in (85).

$$V_{IMMC-switches} = \frac{D.N_2}{(1-D).N_1} Vs = 340\ V \quad (85)$$

4.6 Simulation Results

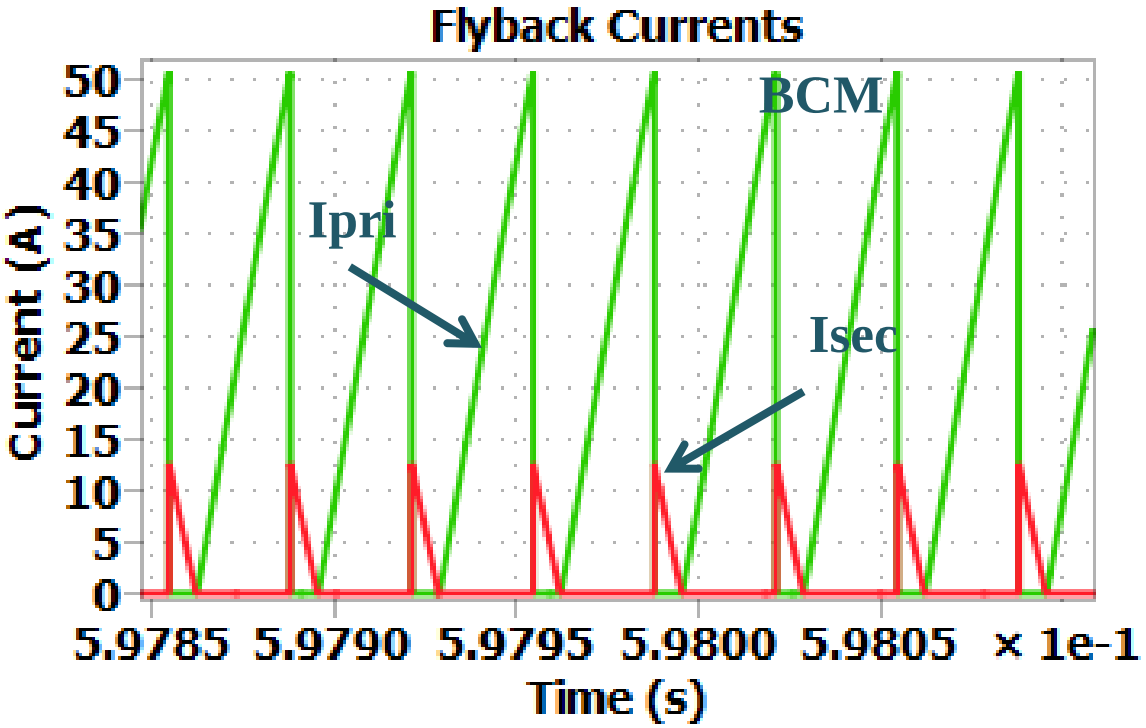

Fig. 90 The primary and secondary currents as shown in Fig. 89 are in the Boundary Conduction Mode (BCM).

The design example shown in Table 16 is simulated. The flyback MPPT is achieved by implementing the Perturb and Observe technique (P&O). The flyback is designed at BCM at full load as seen in Fig. 90. The primary switch S1 turns on at zero current (I_{pri}) which proves that the ZVS is achieved. The secondary current reaches zero which eliminates the reverse recovery losses in the diode. The BCM operation can be maintained using BCM variable frequency control.

The grid-inverter interface is controlled by the FAE current control shown in Fig. 86. The output voltage of the micro-inverter must be the same as the grid voltage. When the

irradiance changes, the available power decreases. The control of the inverter must react by keeping the output voltage constant to match the grid voltage and changing the output current as seen in Fig. 91. The controller reduced the injected current to the grid reduces as the irradiance changes.

Fig. 92 and Fig. 93 are the simulated PV and IV curves respectively. The simulation started with a 1000 W/m^2 and then a dynamic reduction is introduced to examine the MPPT operation of the flyback converter. The controller was able to locate the MPP at both irradiance conditions.

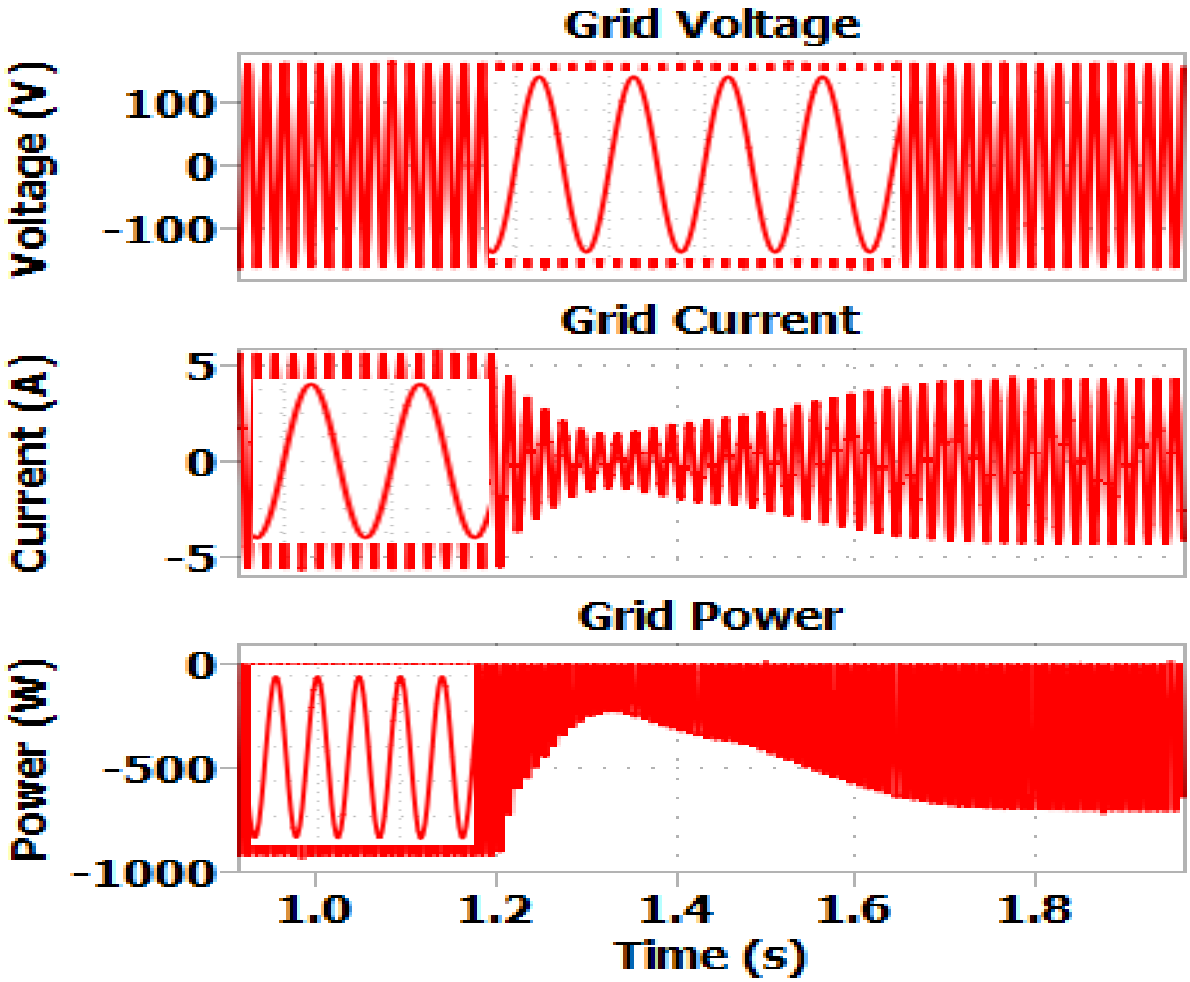

Fig. 91 The grid voltage, current and power behaviors when the irradiance changes. The controller injected the available current to the grid and the voltage of the grid does not change.

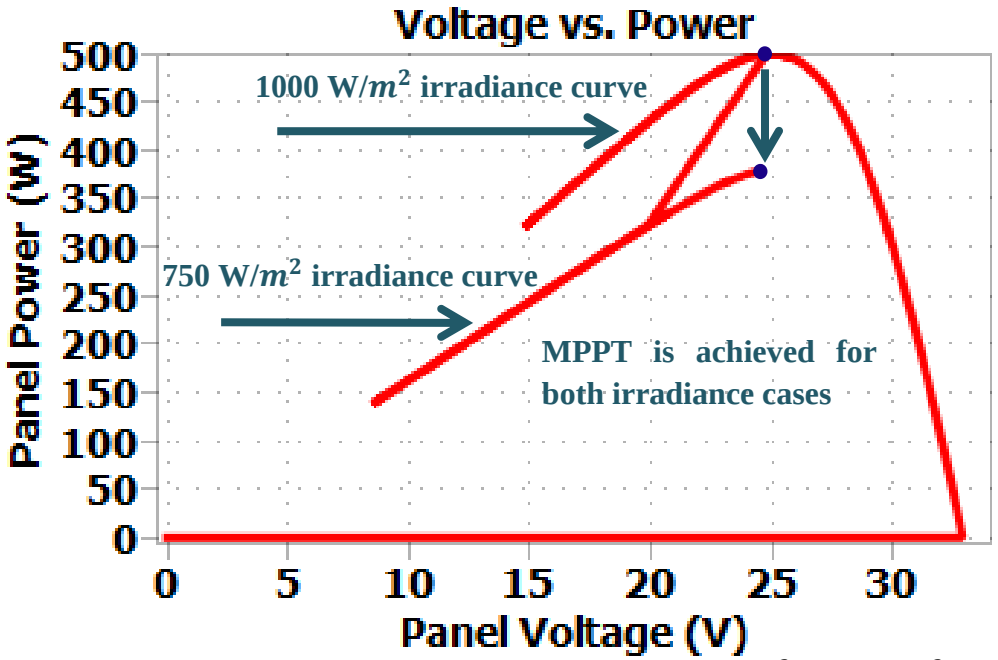

Fig. 92 PV-curve of the panel. When the irradiance changes from 1000 W/m^2 to 750 W/m^2, the controller operates the micro-inverter at the MPP of the new curve.

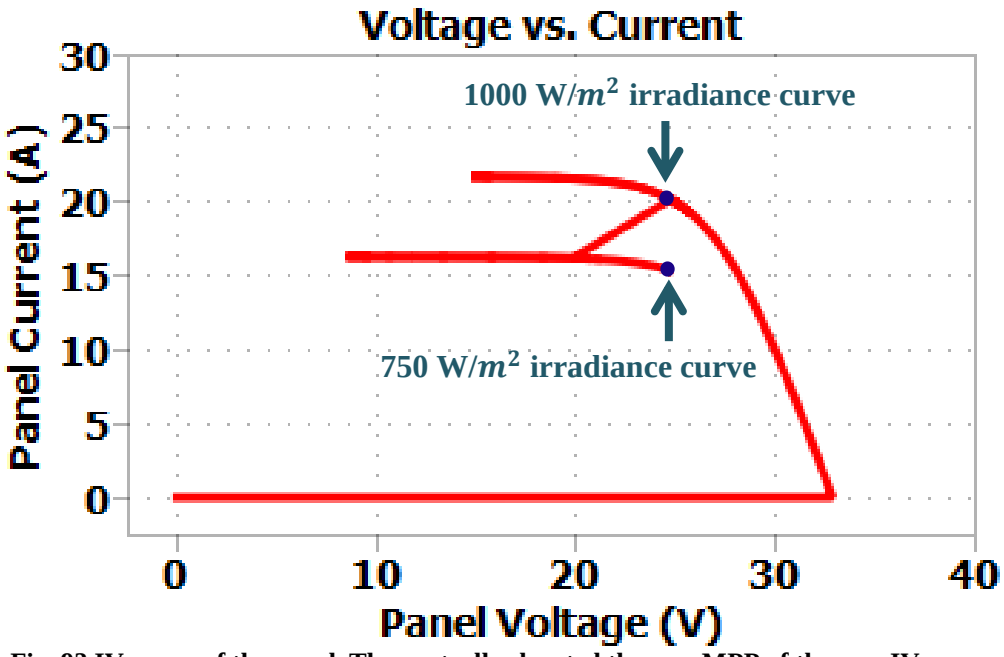

Fig. 93 IV-curve of the panel. The controller located the new MPP of the new IV-curve.

5. GRID-TIE MEDIUM VOLTAGE DC COLLECTION SYSTEM FOR LARGE SCALE SOLAR PV PLANTS

5.1 Conventional Solar Power Collection Systems

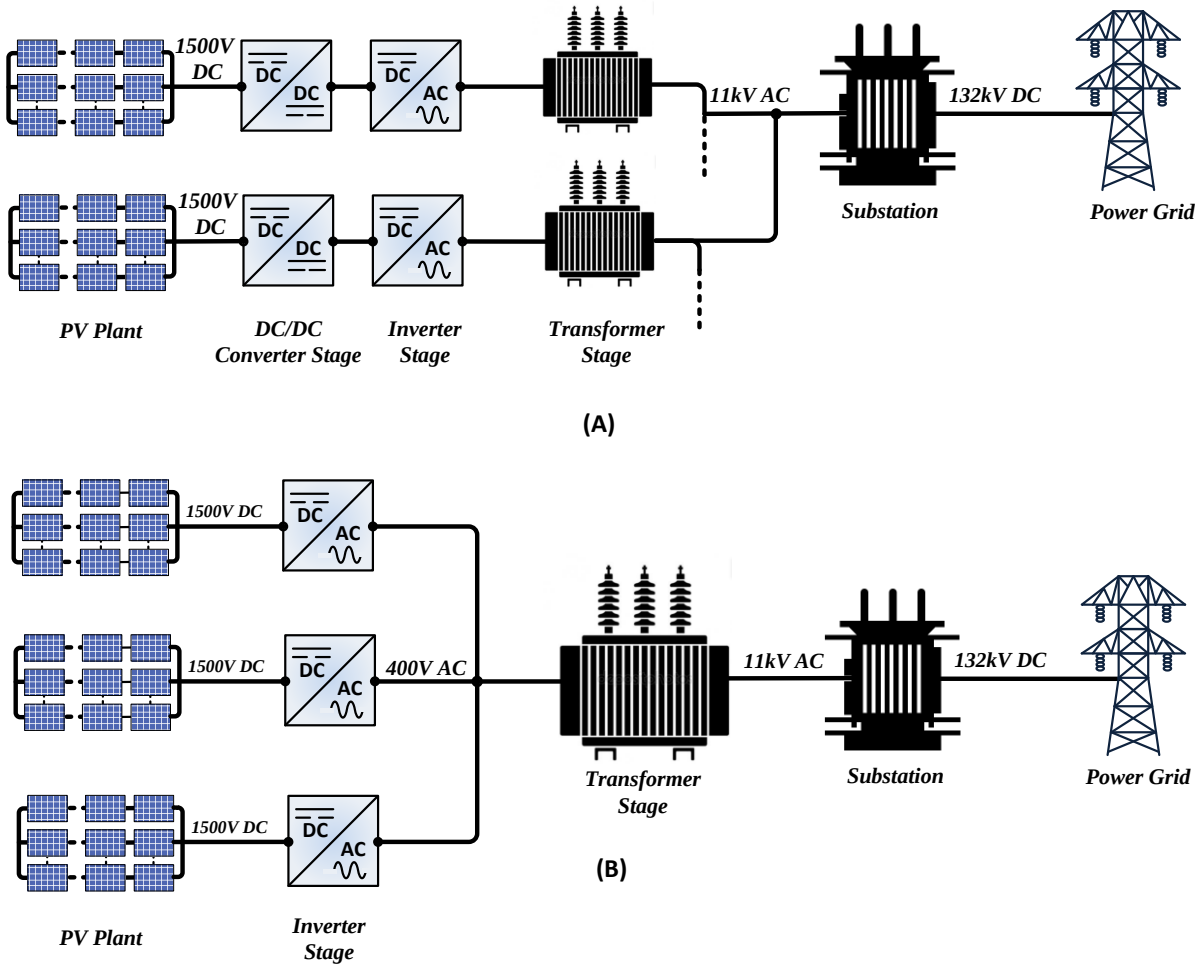

Fig. 94 The conventional AC solar power collection systems (A) Medium voltage AC collection grid (B) Low voltage AC collection grid.

There are several configurations to harness energy from large scale PV power plants. Fig. 94 shows the most common conventional AC collection systems for large scale PV power plants. The first method is the medium voltage collection system where power is collected in a medium

voltage (11kV) as shown in Fig. 94 (A). The other method is to collect power in with low voltage (400V) and then step it up through a transformer as seen in Fig. 94 (B).

5.2 Proposed Grid-Tie Solar Power Collection System

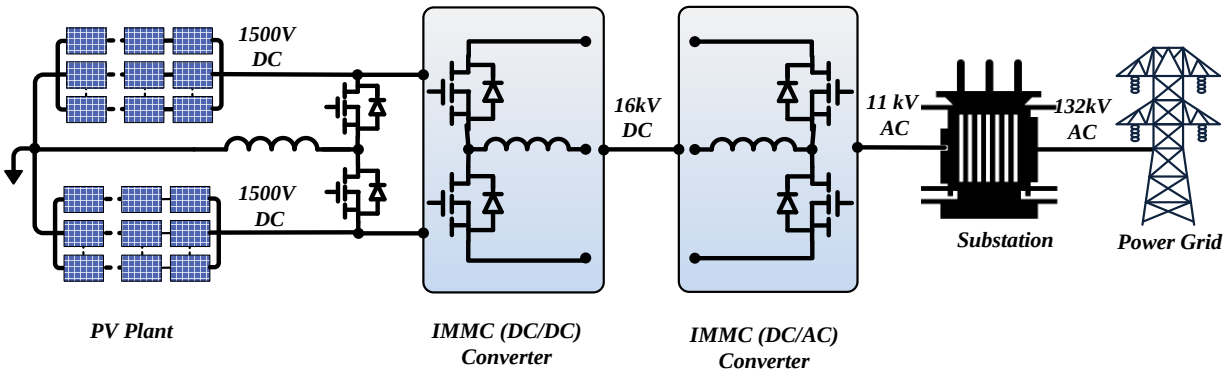

Fig. 95 Proposed medium voltage DC collection system.

This chapter proposes a new system to integrate large scale PV power plants to the grid. Fig. 95 and Fig. 96 show the single line diagram and the detailed configuration of the proposed system respectively. The proposed system harnesses the energy from the PV power plants via Medium Voltage Direct Current (MVDC) collection grid. The PV power plants are connected in series through a power sharing stage that allow the PV power plants to supply different powers under partial shading conditions. The voltage of the PV power plants is stepped up via a DC-DC IMMC to achieve the medium voltage level. The DC-DC IMMC consists of a series stack of half-bridge SiC switches to withstand the medium voltage stress. After that, the MVDC collection grid is followed by a medium voltage DC-AC IMMC to inject the harnessed power to the grid. The DC-AC IMMC is built using SiC to achieve higher temperature and efficiency. The AC output of the DC-AC IMMC is connected to a transformer to step up the voltage to the transmission line level.

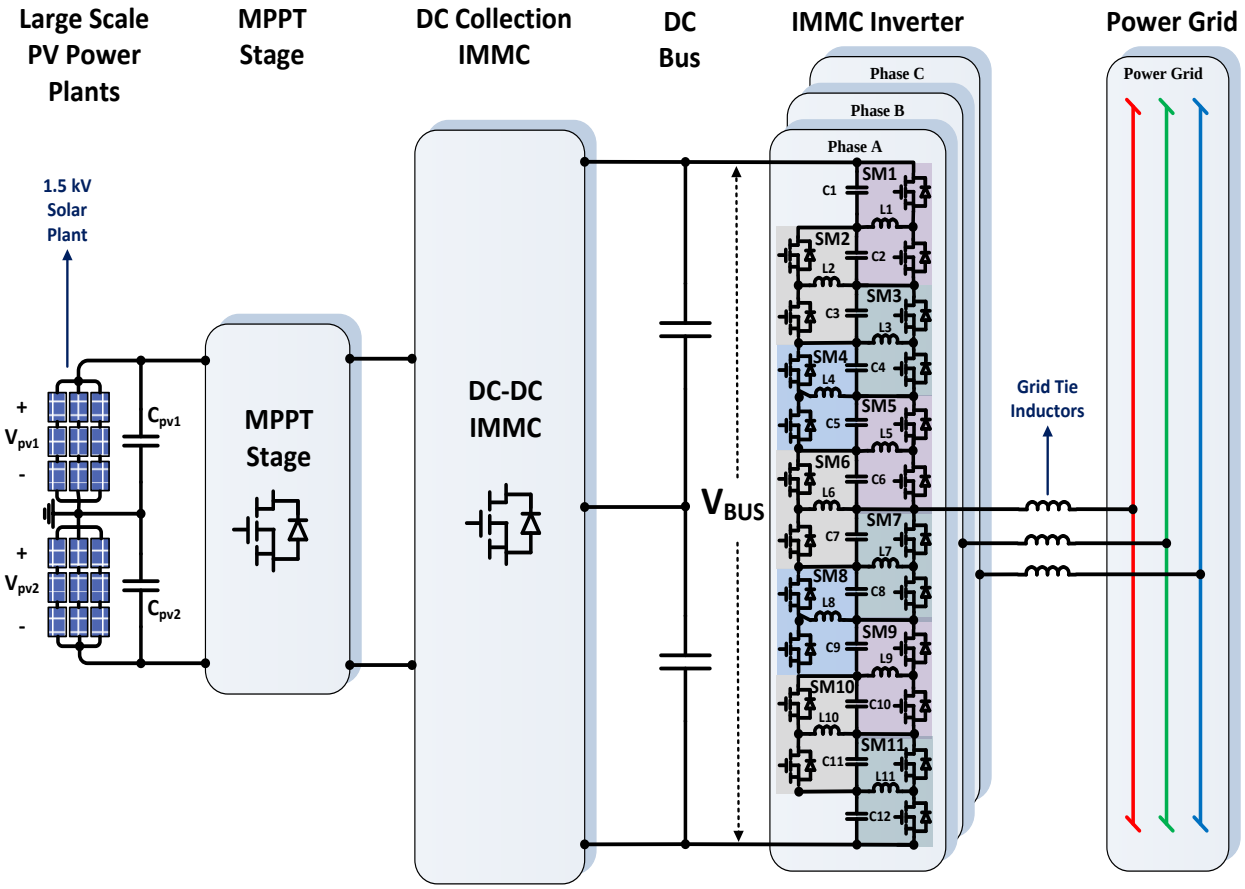

Fig. 96 Detailed schematic of the proposed Gird-tie Medium voltage DC collection System for Large Scale Solar PV Plants Using the IMMC [46].

5.3 Experimental Results

A laboratory prototype of the proposed step-up DC-DC and DC-AC IMMC is shown in Fig. 97 and Fig. 98. The DC-DC stage is used to step up the voltage to five times the input voltages using half-bridge (HB) GaN submodules. The output of the DC-DC stage is the input to the DC-AC IMMC to generate a sinusoidal voltage. The DC-AC IMMC stage is built using SiC devices. Table 17 shows the parameters for the two stages prototype.

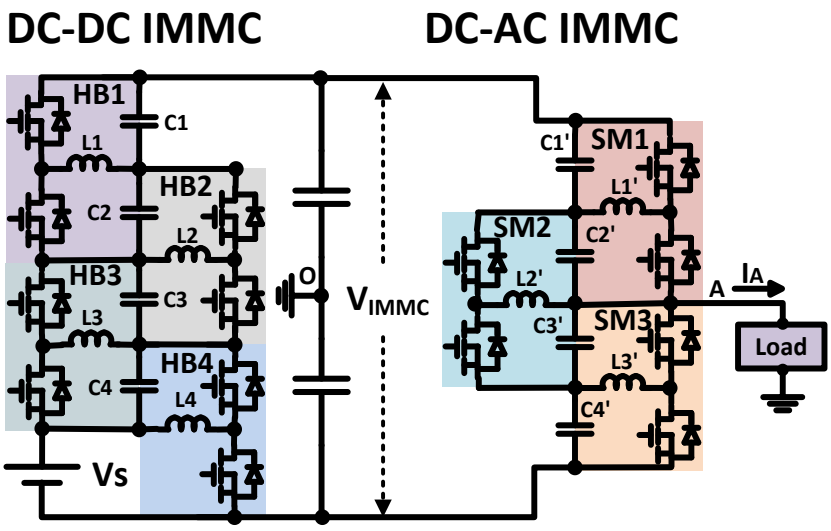

Fig. 97 Circuit diagram of the laboratory prototype.

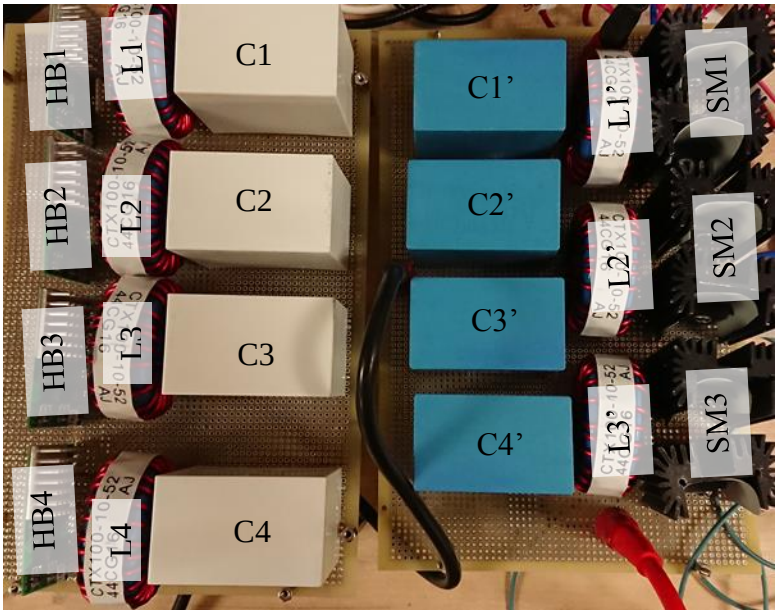

Fig. 98 The laboratory protoype of the proposed system shown in Fig. 97.

The modulation of the DC-DC stage is a 50% duty for all switches to achieve proper balancing of all capacitors. The modulation of the inverter stage is explained in the second chapter of this dissertation.

Fig. 99 shows the waveforms of the input DC voltage (V_s), stepped up DC voltage (V_{IMMC}), the AC output current (I_{AO}), and voltage (V_{AO}) when the grid frequency is 60 Hz as shown in Fig. 97. The DC voltage (V_{IMMC}) is 150 V which is five times the input DC voltage (V_s). Fig. 100 show the same measurement but with the DC-AC IMMC generating an output voltage and current with 50 Hz. Fig. 101 and Fig. 102 show the DC-AC IMMC output when a third harmonic component is injected at 60 Hz and 50 Hz respectively.

Table 17 Laboratory prototype parameters

Parameter	**Value**
DC-DC IMMC Parameters	
Input voltage (V)	30
Switching Frequency (kHz)	100
Inductor (µH)	100
Capacitor (µF)	100
Output Voltage	150
DC-AC IMMC Parameters	
Input voltage (V)	150
Switching Frequency (kHz)	60
Inductor (µH)	100
Capacitor (µF)	50
Load Resistor (Ω)	200

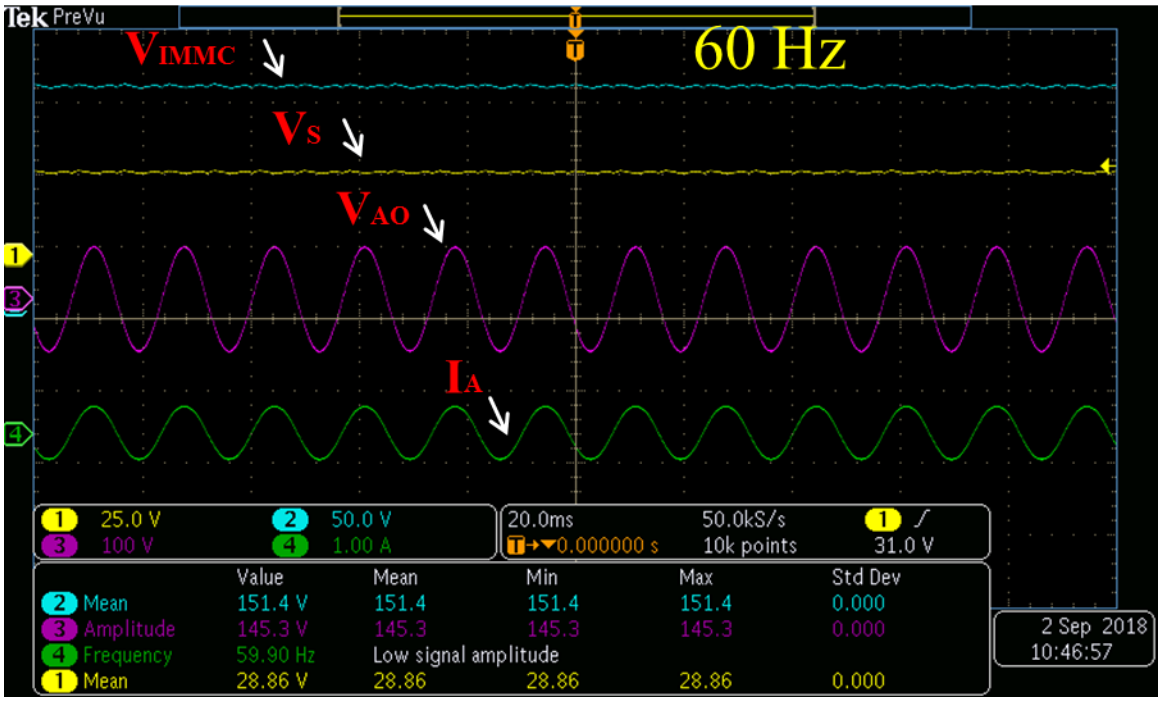

Fig. 99 The waveforms of the input DC voltage (V_s), stepped up DC voltage (V_{IMMC}), the AC output current (I_{AO}), and voltage (V_{AO}) when the grid frequency is 60 Hz.

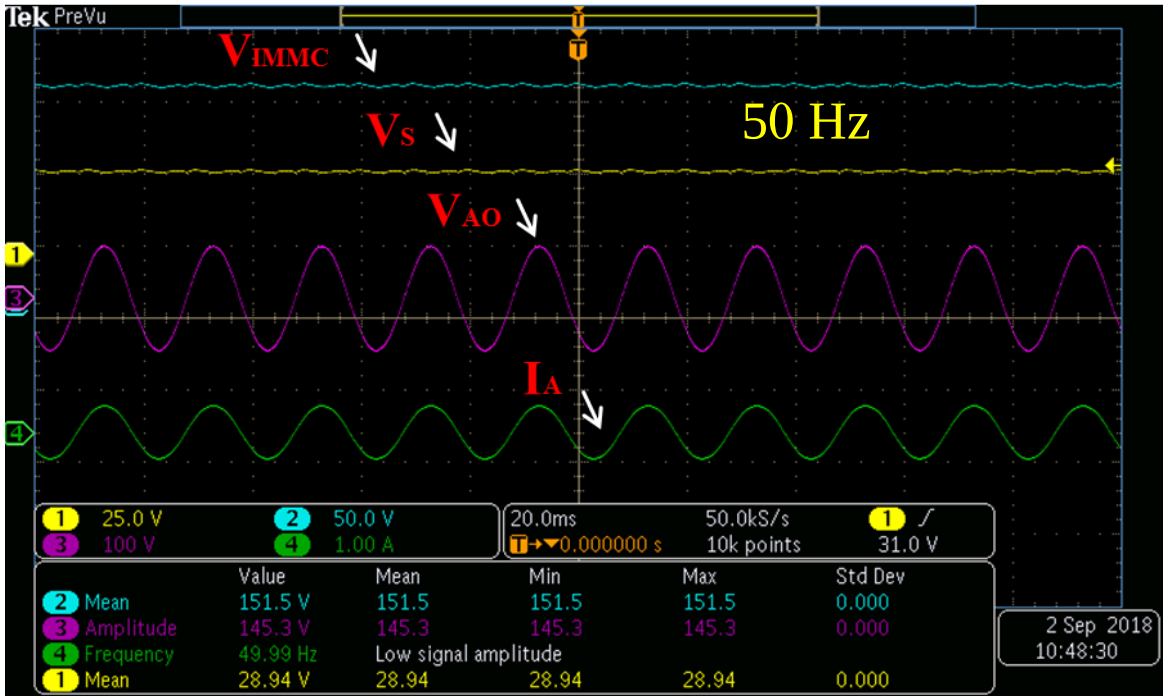

Fig. 100 The waveforms of the input DC voltage (V_s), stepped up DC voltage (V_{IMMC}), the AC output current (I_{AO}), and voltage (V_{AO}) when the grid frequency is 50 Hz.

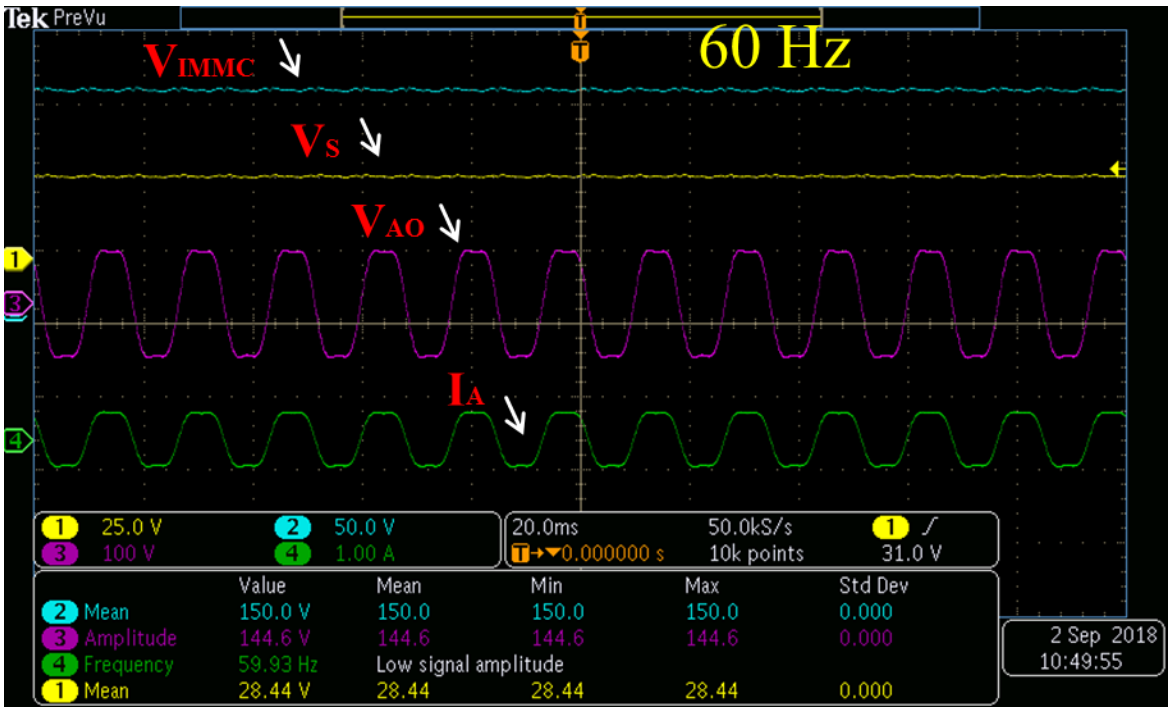

Fig. 101 The waveforms of the input DC voltage (V_s), stepped up DC voltage (V_{IMMC}), the AC output current (I_{AO}), and voltage (V_{AO}) when third harmonic is injected with a grid frequency of 60 Hz.

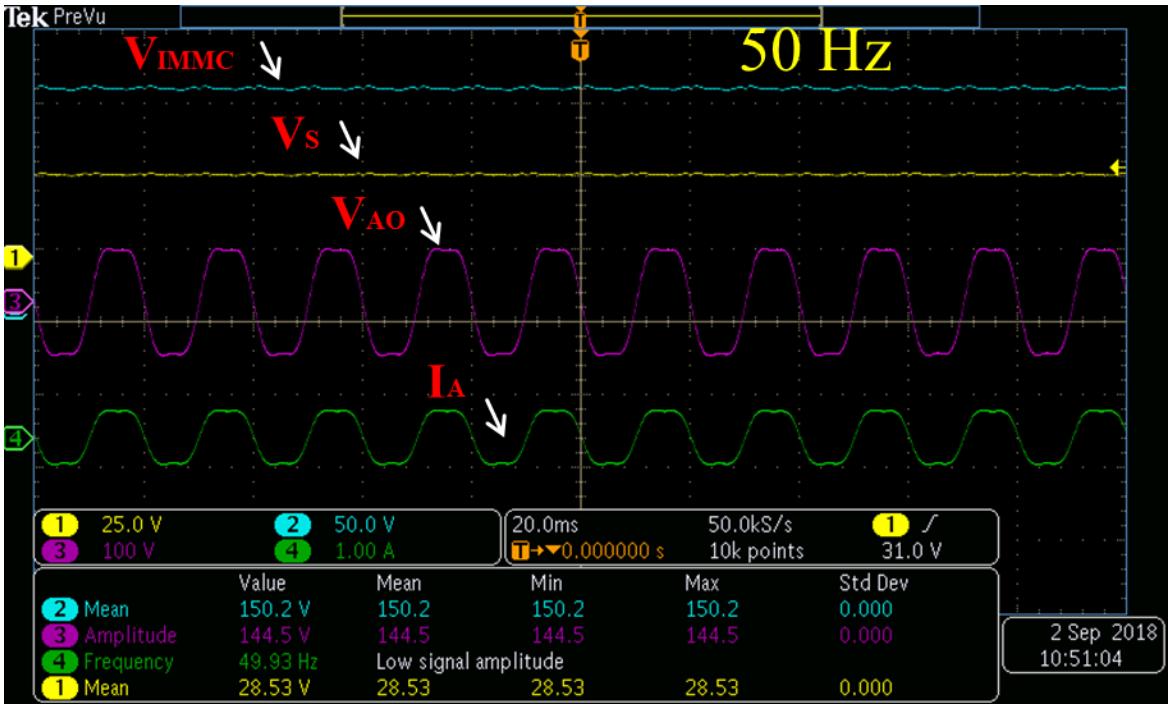

Fig. 102 The waveforms of the input DC voltage (V_s), stepped up DC voltage (V_{IMMC}), the AC output current (I_{AO}), and voltage (V_{AO}) when third harmonic is injected with a grid frequency of 50 Hz.

6. CONCLUSION AND FUTURE WORK

The focus of this dissertation is to propose a new converter that utilizes the Wide Band Gap (WBG) devices to achieve high power density and efficiency. The proposed converter, Interconnected Modular Multilevel Converter (IMMC), produces sinusoidal output voltage that can be used for multiple applications. The proposed converter is modular in construction, employs high frequency L-C components and can be stacked for voltage sharing.

The first application proposed for the IMMC is motor drives due to the following advantages: sinusoidal output with adjustable voltage and frequency (v/f), no acoustic noise, low EMI and absence of dv/dt related issues due to long motor leads. Two design examples for low voltage drives using Gallium Nitride (GaN) devices and medium voltage drives using Silicon Carbide (SiC) are discussed to evaluate the converter for the motor drives operation.

The second application tested for the proposed IMMC is solar micro-inverter applications due to its compact size and the high-quality output. The proposed system connects the inverter to the PV solar panel through a flyback converter for stepping up the voltage to the grid level, isolation and Maximum Power Point Tracking (MPPT). The proposed inverter eliminates the need for a bulky grid-tie inductor or complex LCL filter. The power can be injected to the grid using a small iron-core inductor due to the sinusoidal nature of the output voltage. A grid-tie control using Fictive Axis Emulation (FAE) is implemented on the converter to optimize the power injected to the grid.

In the last chapter, the proposed IMMC is tested as a medium voltage grid-tie inverter for a medium voltage DC collection grid (MVDC) system to integrate two PV power plants. The sinusoidal output of the IMMC facilitates the integration of the solar plants. The inductance

required to connect the inverter to the grid is less due to the sinusoidal nature of the output of the IMMC.

6.1 Future Work

Fault tolerance analysis of the converter under faulty conditions can be done to evaluate the converter for motor drives. Moreover, Field-Oriented Control (FOC) can be implemented to control the speed of the motor and to generate full torque when the speed is zero.

Suggested work for the micro-inverter application is to propose the converter as a transformer-less micro-inverter. The analysis includes implementing a common mode currents mitigation strategy to abide by the safety standard and increase the efficiency of the converter. Therefore, reducing the over size and cost and eliminating the additional transformer stage.

For the grid-tie medium voltage DC-AC IMMC, a robust current control method to improve the dynamics of the converter is a good research opportunity. Current control methods such as Repetitive Controller (RC) and Proportional Resonance (PR) controller can enhance the performance of the converter.

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