Capacitor Voltage Balancing Strategy Based on Sub-module Capacitor Voltage Estimation for Modular Multilevel Converters

Mahmoud Abdelsalam, Mostafa Marei, *Senior Member, IEEE*, Sarath Tennakoon, *Member, IEEE,* and Alison Griffiths

***Abstract*—The modular multilevel converter (MMC) is expected to be used extensively in high-voltage direct current (HVDC) transmission networks because of its superior characteristics over the line-commutated converter (LCC). A key issue of concern is balancing sub-module capacitor voltages in the MMCs, which is critical for the correct operation of these converters. The majority of voltage balancing techniques proposed thus far require that the measurement of the capacitor voltages use a reliable measuring system. This can increase the capital cost of the converters. This paper presents a voltage balancing strategy based on capacitor voltage estimation using the adaptive linear neuron (ADALINE) algorithm. The proposed estimation unit requires only three voltage sensors per phase for the arm reactors and the output phase voltages. Measurements of sub-module capacitor voltages and associated communication links with the central controller are not needed. The proposed strategy can be applied to MMC systems that contain a large number of sub-modules. The method uses PSCAD/EMTDC, with particular focus on dynamic performance under a variety of operating conditions.**

***Index Terms*—Capacitor balancing, HVDC, MMC.**

I. Introduction

VOLTAGE source converters (VSCs) are being used increasingly in high-voltage direct current (HVDC) transmission systems over line-commutated converters (LCCs), particularly for connecting off shore wind farms. The advantages of using VSC include the ability to control active and reactive power independently, the ability to supply weak or passive networks, and VSC's lower space footprint. Although VSCs have many topologies, the modular multilevel converter (MMC) is considered the most suitable topology for high voltage applications, especially for power transmission and distribution. Their advantages include potential to eliminate harmonic filters with a sufficient number of voltage levels, elimination of the DC-link capacitor, and low switching losses [1], [2].

The MMC consists of sub-modules connected in a series, and forming a leg in each phase. The sub-module can be a half-bridge or a full-bridge and each sub-module has a capacitor that buffers the energy from the DC to the AC side and vice versa, thus eliminating the DC-link capacitor. As shown in Fig. 1, each phase leg is divided into two arms—upper and lower. Each arm has an identical number of sub-modules to generate balanced voltage between the two arms of each phase. Inductors are installed in arms to smoothen and filter the currents [3], [4].

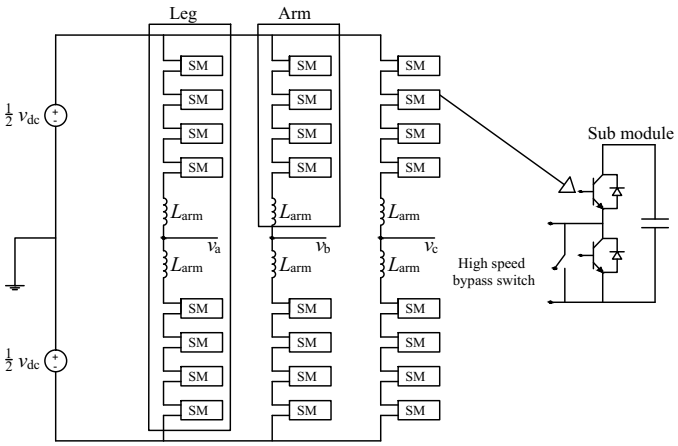

Fig. 1. Three-phase MMC topology and internal sub-module.

This paper presents a new voltage balancing control technique based on capacitor voltage estimation in place of traditional direct measurement. The main contribution of the proposed technique is the elimination of the communication burden used to send the voltage measurements from sub-modules to the central controller. As a result, not only the cost is reduced, but the wiring and associated problems are also minimized, which renders the proposed strategy attractive for the practical realization of a MMC with a large number of sub-modules. The proposed control technique has been evaluated using simulations where a number of case studies were conducted to test the dynamic performance under a variety of operating conditions. Section II shows the modeling of the

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MMC, including the mathematical representation and the switching algorithm. Section III shows the proposed balancing algorithm while presenting the capacitor voltage estimation technique. Section IV presents the simulation results with some discussions. Finally, a conclusion for the conducted work is presented in section V.

II. Modeling of MMC

Generally, the operation of the MMC depends on the switching of the sub-module IGBTs. The switching is performed by a switching algorithm, which generates the firing signals to each sub-module [5].

A. MMC Operating Modes

The MMC half bridge sub-module has four operation modes during which energy is transferred:

Mode 1: When S_1 is closed, S_2 is opened, and the arm has positive polarity. The current flows into the capacitor, charging it. The sub-module is then inserted. See Fig. 2(a).

Mode 2: When S_1 is opened, S_2 is closed, and the arm has positive polarity. The sub-module is bypassed, and the current flows towards the next sub-module, keeping the capacitor charge constant. The sub-module is then bypassed. See Fig. 2(b).

Mode 3: S_1 is closed, S_2 is opened, and the arm has negative polarity. The capacitor starts to discharge and then the sub-module is inserted. See Fig. 2(c).

Mode 4: When S_1 is opened, S_2 is closed, and the arm has negative polarity. The current flows towards the next module, keeping the capacitor charge constant, after which and the sub-module is bypassed. See Fig. 2(d).

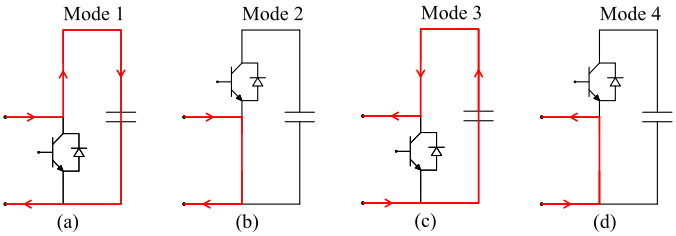

Fig. 2. Different operating modes of MMC sub-modules. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

B. Mathematical Model of MMC

For the purpose of designing an inner control system for the MMC, it is necessary to mathematically analyze the converter. The converter arms, shown in Fig. 3, are represented as variable capacitors connected in a series with arm resistance and inductance [6]. The number of sub-modules per arm and the switching frequency is assumed as infinite to simplify the analysis because of the perfect sinusoidal output voltage and total voltage balancing between arms. The arm capacitance insertion is represented with a modulation value $m_{\text{arm}\,x}$, where x may be u for upper arm or l for lower arm. The $m_{\text{arm}\,x}$ is varied from 0 to 1. For example, when $m_{\text{arm u}} = 0$, this indicates that all sub-modules in the upper arm are bypassed and when $m_{\text{arm l}} = 1$, this indicates that all sub-modules in the lower arm are inserted. The value $\Sigma v_{\text{C}x}$ is the sum of arm capacitor voltages. The arm voltage is given by:

$$v_x(t) = m_{\text{arm}\,x}(t).\Sigma v_{\text{C}x}. \tag{1}$$

The inserted arm capacitance is given by:

$$C_{\text{ins}\,x} = \frac{C_{\text{SM}}}{N.m_{\text{arm}\,x}(t)} \tag{2}$$

where C_{SM} is the capacitance of one sub-module and N is the number of sub-modules per arm. If the arm current is $i_x(t)$, the total capacitor voltage dynamics can be expressed by:

$$\frac{d\Sigma v_{\text{C}x}}{dt} = \frac{i_x(t)}{C_{\text{ins}\,x}}. \tag{3}$$

Substituting (2) in (3), the capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\Sigma v_{\text{Cu}}}{dt} = \frac{N.m_{\text{arm u}}.i_{\text{u}}}{C_{\text{SM}}} \tag{4}$$

$$\frac{d\Sigma v_{\text{Cl}}}{dt} = \frac{N.m_{\text{arm l}}.i_{\text{l}}}{C_{\text{SM}}}. \tag{5}$$

The current i_{diff} is the differential current, which circulates between the phase legs. The circulating current of any phase is described as follows:

$$i_{\text{diff}} = \frac{i_{\text{u}} + i_{\text{l}}}{2}. \tag{6}$$

By performing the necessary circuit analysis, the output phase voltage v_{o} is given by:

$$v_{\text{o}} = \frac{v_{\text{dc}}}{2} - L_{\text{arm}}\frac{di_{\text{u}}}{dt} - m_{\text{arm u}}\Sigma v_{\text{Cu}} \tag{7}$$

$$v_{\text{o}} = -\frac{v_{\text{dc}}}{2} + L_{\text{arm}}\frac{di_{\text{l}}}{dt} + m_{\text{arm l}}\Sigma v_{\text{Cl}}. \tag{8}$$

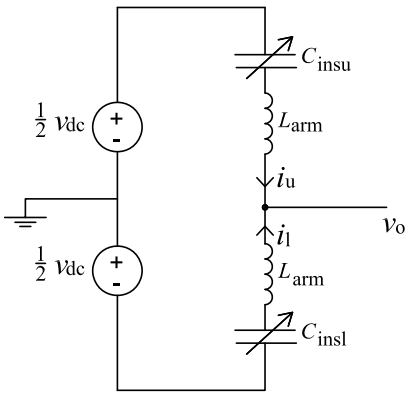

Fig. 3. The MMC average model.

C. MMC Switching Algorithm

Many switching algorithms have been proposed in the literature [7]–[10], and the modulation techniques that have been used can be divided into two main categories: 1) reference signal based and 2) carrier based. The phase shifted pulse width modulation (PS-PWM), which is one of the well-known

carrier based techniques, is utilized because of the following advantages [11]:

1) Ease of implementation;
2) lower losses due to reduced switching frequency; and
3) stable performance during dynamic changes.

In the PS-PWM technique, illustrated in Fig. 4, each sub-module has a dedicated triangular carrier waveform with the same magnitude, but with a different phase shift.

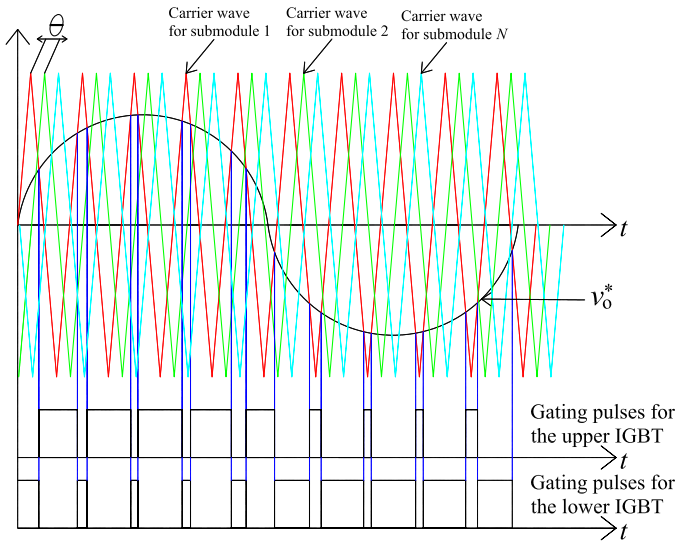

Fig. 4. The PS-PWM concept.

The switching signal for a sub-module results from comparing its corresponding carrier wave with the sinusoidal voltage reference signal v_o^*. The phase shift between each consecutive carrier signal is given by:

$$\theta = \frac{360}{N-1}. \tag{9}$$

III. Proposed Capacitor Voltage Estimation Technique

The voltage balancing process is vital for keeping the power quality at the standard level, as it significantly reduces the voltage ripples of the sub-module capacitors [12]–[14]. The proposed algorithm consists of three main stages:

1) Capacitor voltage estimation;
2) averaging control;
3) balancing control for capacitors' voltages.

A. Capacitor Voltage Estimation Technique

The capacitor voltage estimation is performed using the Adaptive Linear Neuron (ADALINE) algorithm. ADALINE is known for its efficiency and its rapid on-line tracking technique for dynamically changing voltage signals. It has been utilized in many applications because of its robust performance, low calculation burden, and accurate results [15], [16]. The ADALINE algorithm is formed by simple calculations that do not consume large computing time, which is very important in the application of capacitor voltage estimation. To estimate the capacitor voltages, the MMC governing equations given by (7) and (8) are rearranged and rewritten in the vector form as follows:

$$\frac{v_{\rm dc}}{2} - v_{\rm o} - v_{\rm Lu} = \begin{bmatrix} S_{\rm u1} & S_{\rm u2} & \dots & S_{{\rm u}N} \end{bmatrix} \begin{bmatrix} v_{\rm cu1\_est} \\ v_{\rm cu2\_est} \\ \vdots \\ v_{{\rm cu}N{\rm \_est}} \end{bmatrix} \tag{10}$$

$$\frac{v_{\rm dc}}{2} + v_{\rm o} - v_{\rm Ll} = \begin{bmatrix} S_{\rm l1} & S_{\rm l2} & \dots & S_{{\rm l}N} \end{bmatrix} \begin{bmatrix} v_{\rm cl1\_est} \\ v_{\rm cl2\_est} \\ \vdots \\ v_{{\rm cl}N{\rm \_est}} \end{bmatrix} \tag{11}$$

where S_{xi} is the switching state for the $i^{\rm th}$ sub-module, $v_{\rm Lu} = L_{\rm arm}\frac{di_{\rm u}}{dt}$, and $v_{\rm Ll} = L_{\rm arm}\frac{di_{\rm l}}{dt}$.

The ADALINE algorithm produces a linear combination of its input vector $X(k)$, which represents the switching state of each sub-module whether it is inserted or by-passed at time k, and it is written as follows:

$$\boldsymbol{X}(k) = \begin{bmatrix} S_{x1} & S_{x2} & \dots & S_{xN} \end{bmatrix}^{\rm T} \tag{12}$$

where the suffix T refers to the transpose operation. As shown in Fig. 5, the input vector is multiplied by the weight vector W, which resembles the estimated capacitor voltages, given in (10) and (11):

$$\boldsymbol{W}(k) = \begin{bmatrix} v_{{\rm c}x1\_{\rm est}} & v_{{\rm c}x2\_{\rm est}} & \dots & v_{{\rm c}xN\_{\rm est}} \end{bmatrix}. \tag{13}$$

This multiplication is performed to produce the predicted linear output $\hat{y}(k) = \boldsymbol{X}^{\rm T}\boldsymbol{W}(k)$. The next step is updating the weight vector using an adaptation algorithm called the Widrow-Hoff delta rule given by [17]:

$$\boldsymbol{W}\,(k+1) = \boldsymbol{W}\,(k) + \alpha \frac{\boldsymbol{X}(k)(y(k) - \hat{y}(k))}{\boldsymbol{X}\,(k)^{\rm T}\,\boldsymbol{X}(k)} \tag{14}$$

where α is the reduction factor and $y(k) = \frac{v_{\rm dc}}{2} \pm v_{\rm o} - v_{{\rm L}x}$. The adaptation algorithm is responsible for adjusting the weighting vector, which represents the estimated capacitor voltages so that the linear output of the ADALINE, $\hat{y}(k)$ is equal to its target value $y(k)$. When the error between the measured signal $y(k)$ and the estimated signal $\hat{y}\,(k)$ converges to zero, the ADALINE algorithm decomposes the signal and estimates capacitor voltages.

It is observed that increasing the reduction factor α increases the convergence speed on account of losing stability as the prediction error may increase dramatically. This observation is a common behavior of the Widrow-Hoff delta rule for all the study cases. A practical value for the reduction factor α is 0.002 for this application. This value is determined based on minimizing the error to guarantee system stability [18]. It is worth mentioning that the proposed capacitor voltage estimation unit is based on three voltage sensors per phase to measure the voltage across the arm reactors and the output phase voltage. This action enables the implementation of a low-cost centralized controller for the MMC with large numbers of sub-modules, since voltage measurements of sub-modules and their associated communication links are eliminated.

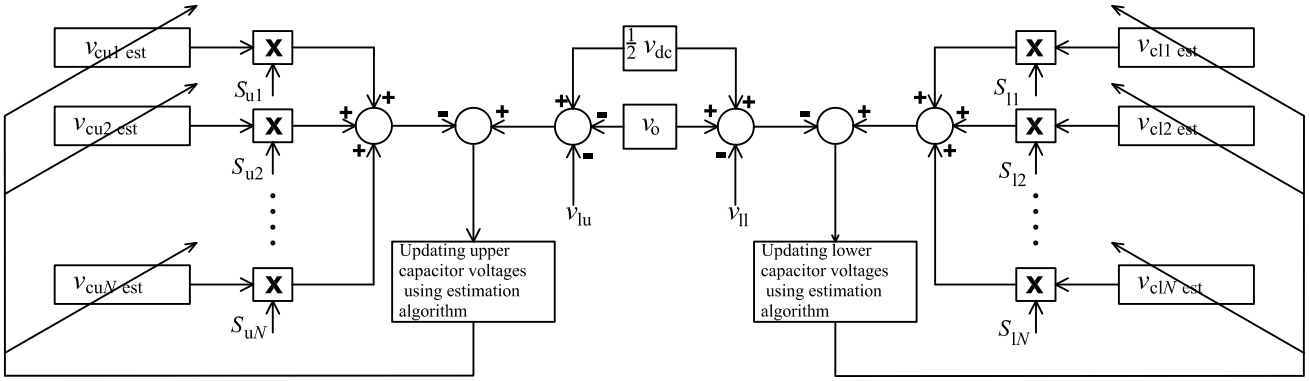

Fig. 5. Block diagram of the proposed capacitors voltages estimation unit based on the ADALINE algorithm.

B. Averaging Control

The concept of averaging control is responsible for controlling the average voltage across a complete leg. Averaging control is formed from two cascaded loops as shown in Fig. 6 [19]. The first loop is the voltage control loop where the estimated average voltage, $\hat{v}_{\text{avg}} = (\sum v_{\text{cu}_{\text{est}}} + \sum v_{\text{cl}_{\text{est}}})/2N$, is subtracted from the reference capacitor voltage, v_{C}^*, and the resultant error is processed through a PI controller to generate the reference signal for the differential current, i_{diff}^*. Another PI controller is utilized in the inner loop to regulate the differential current calculated from (6) at its reference signal. The action of the inner loop controller is the averaging voltage signal, v_{avg}^*.

C. Balancing Control for Capacitor Voltages

The balancing control method, presented in Fig. 7, is a centralized control system that generates reference signals for balancing the voltage across sub-module capacitors based on estimated voltages from the ADALINE processing unit. First, the controller subtracts the estimated capacitor voltage of each sub-module from the reference capacitor voltage, v_{c}^*. The resulting errors are passed to simple proportional (P) controllers. The outputs from the P-controllers are multiplied by the sign of their corresponding arm current to form reference signals for balancing the voltage across capacitors, $v_{\text{cul\_bal}}, \ldots, v_{\text{cu}N\text{\_bal}}, v_{\text{cll\_bal}}, \ldots, v_{\text{cl}N\text{\_bal}}$. Finally, to form the modulating signal for a sub-module, which is

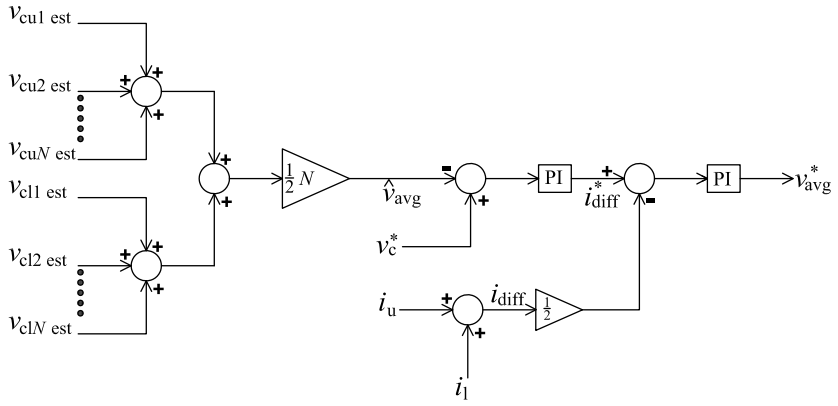

Fig. 6. Block diagram of the averaging controller.

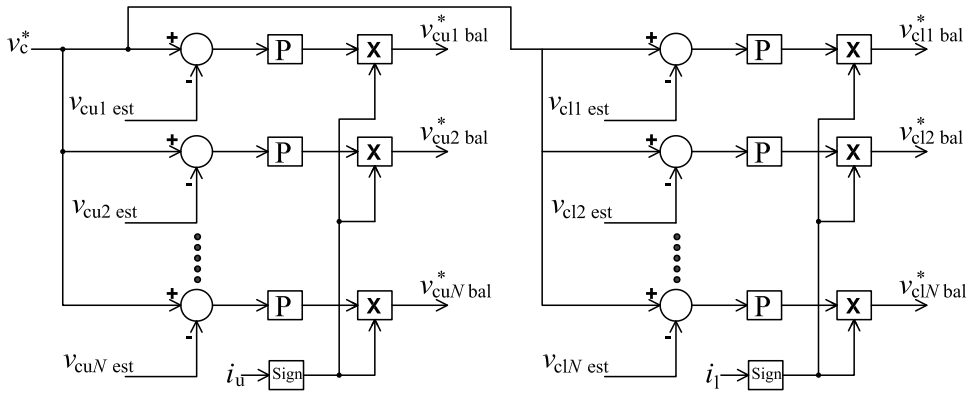

Fig. 7. Block diagram of the balancing controller.

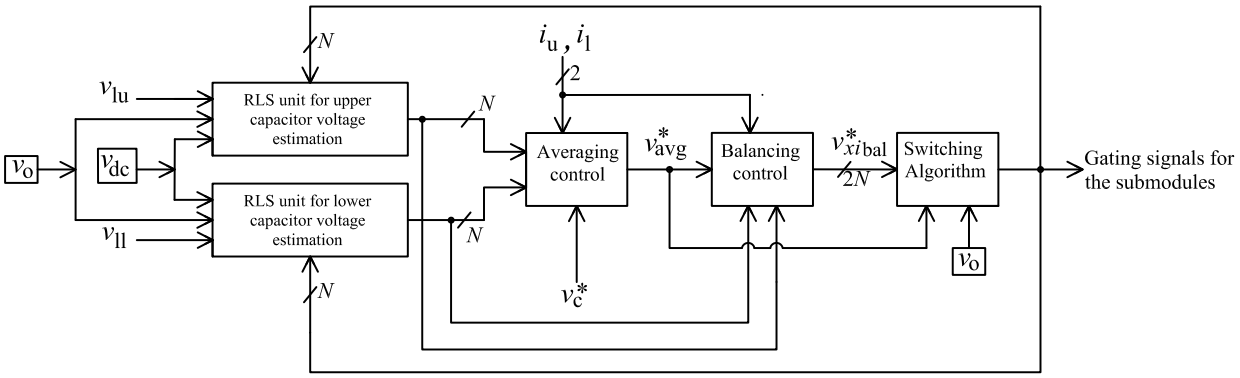

Fig. 8. Block diagram of the proposed MMC controller.

the balancing control signal for this sub-module, the average voltage command, v^*_{avg}, and the reference phase voltage, v^*_o, are all added. The PS-PWM technique is then utilized to generate the switching signals for the sub-modules of the MMC [20]. Fig. 8 illustrates a block diagram of the proposed integrated control system of the MMC. It is obvious that the proposed scheme eliminates the need for massive numbers of voltage sensors for the sub-module capacitors and their associated communication system with the central controllers. Consequently, the proposed strategy renders its application for an MMC system with a large number of sub-modules.

IV. Simulation Results and Discussions

The proposed control scheme for the MMC is simulated using PSCAD/EMTDC software package. The system parameters are shown in Table I. Different simulation cases are considered to examine the dynamic performance of the proposed control strategy for the MMC under different operating conditions. Primarily, the first task is dedicated to performance evaluation of the proposed ADALINE algorithm in order to estimate capacitor voltages used for controlling the MMC under dynamic reference phase voltage changing conditions. The second case is devoted to assessing the dynamic performance of the proposed control strategy during the boost operation of the MMC. Finally, the third case examines the capabilities of the proposed strategy for estimating capacitor voltages under fault conditions in a sub-module, and for determining the faulty sub-module.

TABLE I
MMC Model Parameters

Parameter	Value
Rated power	1 MW
Sub-module rated voltage	2,250 V
Rated DC voltage	4,500 V
Arm inductance	3 mH
Sub-module capacitance	1,900 μF
Number of sub-modules per leg	8
Load impedance	30 Ω, 6 mH

A. Dynamic Performance of the Proposed Capacitor Voltage Estimation Based Balancing Strategy

The purpose of this simulation case is to examine the performance of the proposed capacitor voltage estimation based control algorithm for the MMC under dynamic changes occuring in reference phase voltages. The reference capacitor voltage v^*_c is set at $v_{dc}/N = 2.25$ kV while the reference phase voltage signal v^*_o is dynamically changed from 0.7 p.u. to 1 p.u. at $t = 0.2$ s. First, the estimation units for capacitor voltages are disabled and the actual measurements are used in the control system. The three-phase voltages, currents, and capacitor voltages are shown in Fig. 9. A similar result to Fig. 9 is obtained in Fig. 10 where the proposed estimation unit for the capacitor voltages is enabled and utilized in the proposed control system shown in Fig. 8. As displayed in Fig. 10(a), the measured three-phase AC voltages follow their reference signals. As expected, only six sub-modules are utilized when $v^*_o = 0.7$ p.u., while all the sub-modules are involved when $v^*_o = 1$ p.u. The three-phase load currents are displayed in Fig. 10(b). Fig. 10(c) traces the capacitor voltages that are grouped in two main trajectories, one for the upper arm and the other for the lower arm. These two trajectories are out of phase and are identical to that presented in Fig. 9(c), where the measured capacitor voltages are used instead of their estimated signals in controlling the MMC. The proposed MMC controller succeeds

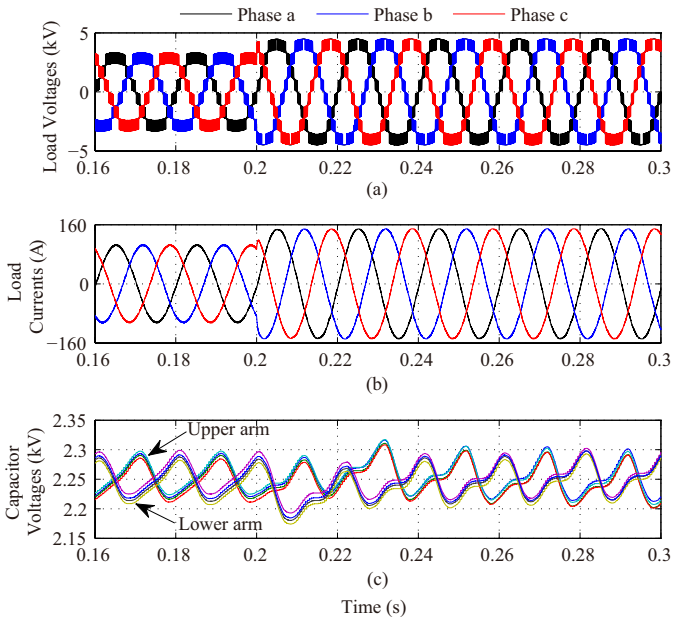

Fig. 9. Disabling the proposed estimation unit. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

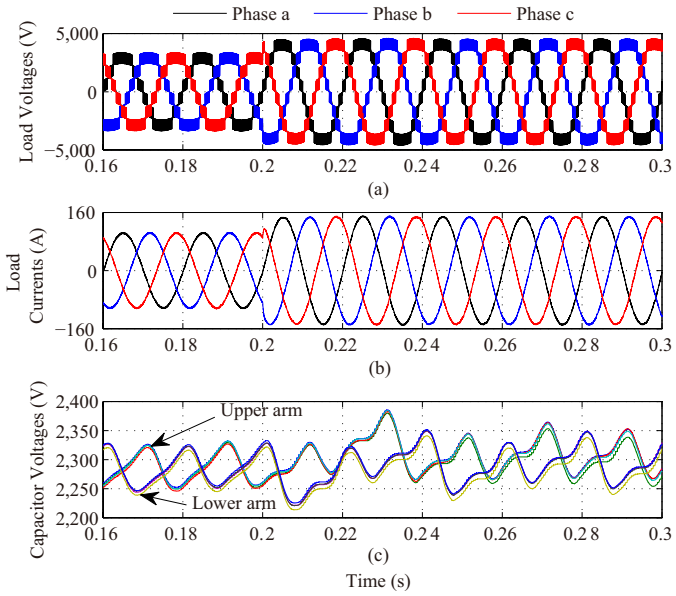

Fig. 10. Enabling the proposed estimation unit. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

in balancing the capacitor voltages at their reference value of 2.25 kV. Moreover, the estimated capacitor voltages and their corresponding actual measurements for the upper and lower arms are presented in Fig. 11 and Fig. 12, respectively.

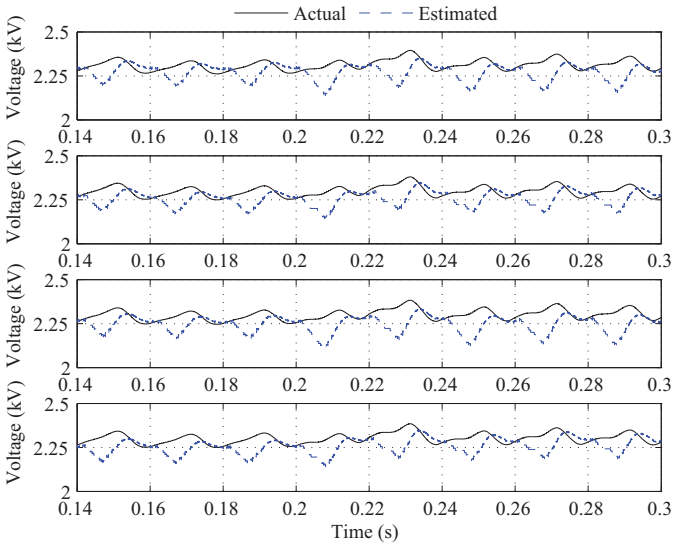

Fig. 11. Actual and estimated voltages of the upper arm sub-modules of phase a.

Fast tracking with accurate performance of the proposed ADALINE algorithm for estimating the sub-module capacitor voltages are evident. Furthermore, the circulating current is tightly tracking its reference signal, as demonstrated in Fig. 13(a). Fig. 13(b) and Fig. 13(c) illustrate the actions of the averaging controller in Fig. 6 and the balancing controller in Fig. 7 for the first sub-module at the upper arm $v^*_{\mathrm{cu1\,bal}}$, respectively. These results reveal efficient utilization of the proposed capacitor voltage estimation techniques for the MMC's control algorithm.

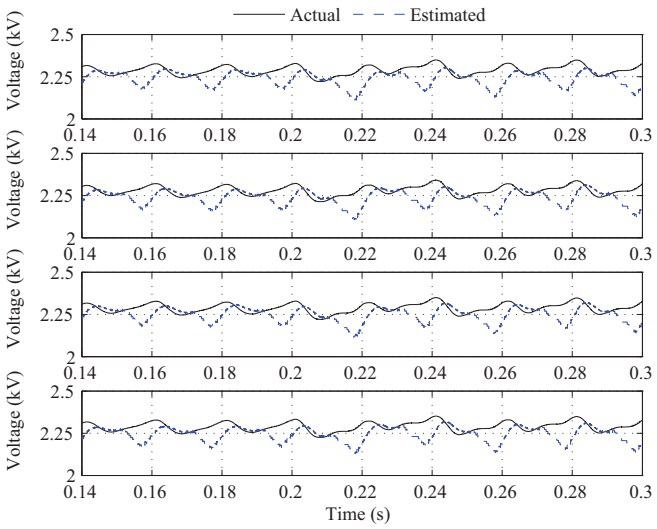

Fig. 12. Actual and estimated voltages of the lower arm sub-modules of phase a.

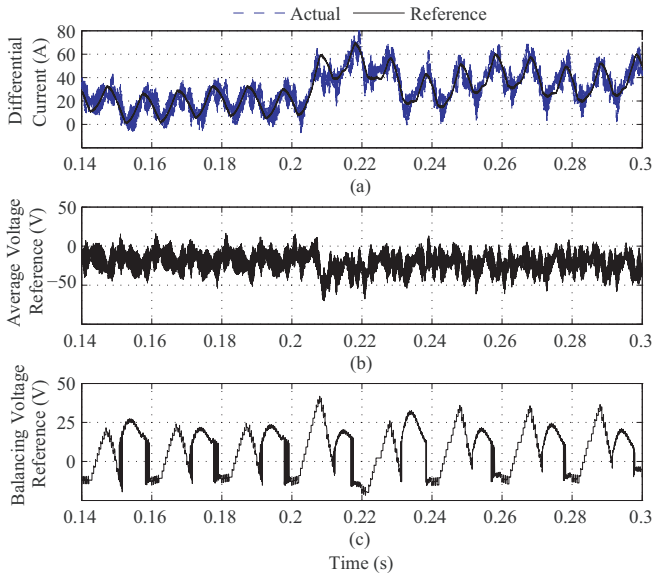

Fig. 13. Different controllers action for leg a. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

B. Dynamic Performance During Boost Operation of MMC

In this test scenario, the reference phase voltage signal v^*_{o} is kept at 1 p.u., and the capacitor reference voltage command is increased from 2.25 kV to 2.5 kV at $t = 0.4$ s. Setting v^*_{c} at values higher than v_{dc}/N results in boost operation of the MMC, which is useful in compensating for the load voltage during sub-module faults.

Fig. 14(a) indicates increase in output three-phase voltages from the MMC at $t = 0.4$ s when the proposed controller succeeds in boosting and balancing the capacitor voltages at the new set value of 2.5 kV, as illustrated in Fig. 14(c). Yet again, the fast dynamics that tolerates error of the proposed capacitor voltage estimation units are revealed in Fig. 15 and Fig. 16 for the sub-modules at both upper and lower arms, respectively. Boosting the capacitor voltages increases the circulating current, and hence the balancing voltage signal escalates, as demonstrated in Fig. 17.

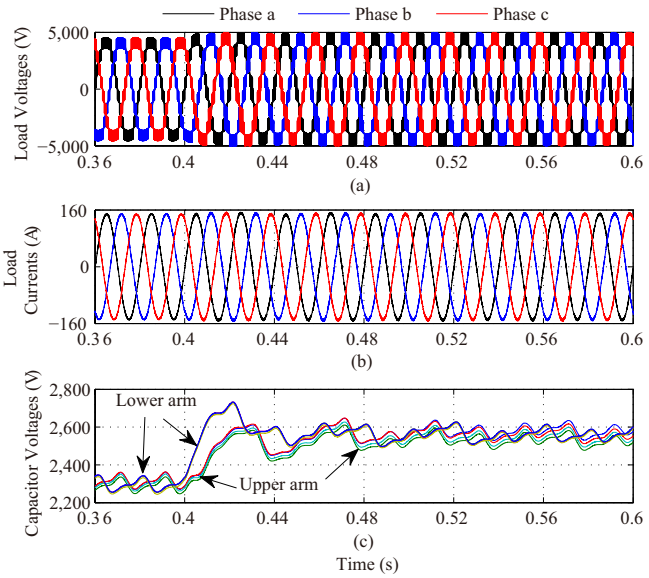

Fig. 14. Boost operation of the MMC. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

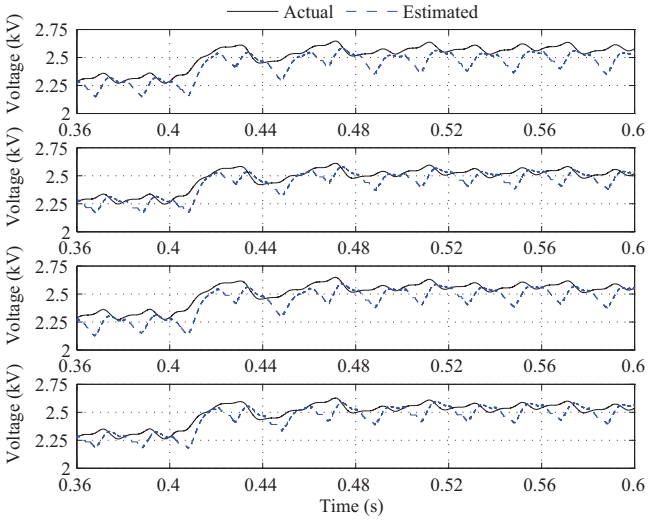

Fig. 15. Actual and estimated voltages of the upper arm sub-modules of phase a during the boost operation.

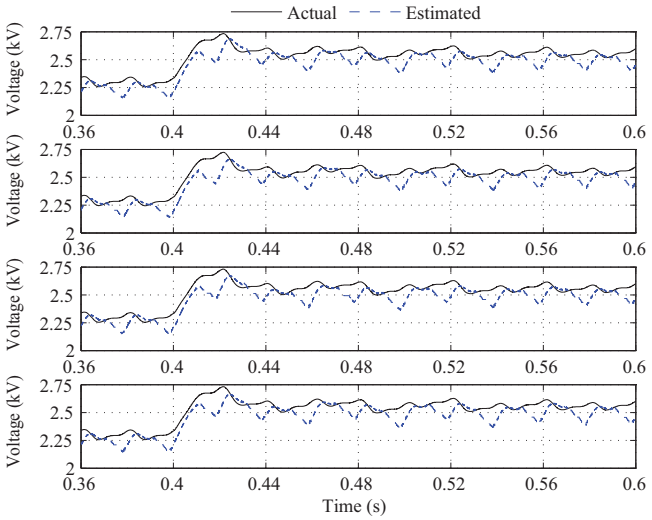

Fig. 16. Actual and estimated voltages of the lower arm sub-modules of phase a during boost operations.

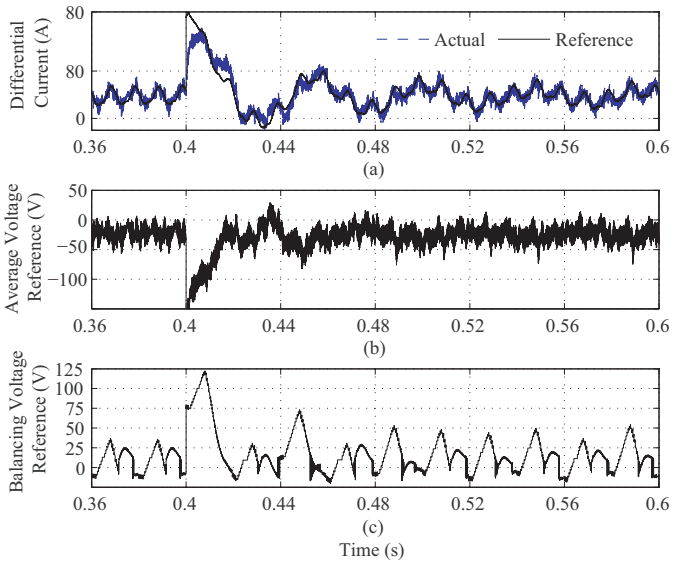

Fig. 17. Different controller actions for leg a during the boost operation. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

C. Performance Under Sub-module Fault

This task is devoted to assessing the capabilities of the proposed strategy for estimating capacitor voltages under fault conditions in a sub-module. A short-circuit fault is programmed to strike the upper switch of the third sub-module in the upper arm of phase a at $t = 0.8$ s. As a result, the voltage and current of phase a are distorted, as shown in Fig. 18(a) and Fig. 18(b), respectively. Fig. 18(c) indicates the collapse of the DC voltage of the faulty sub-module to zero at the fault instance. Consequently, the voltages of the

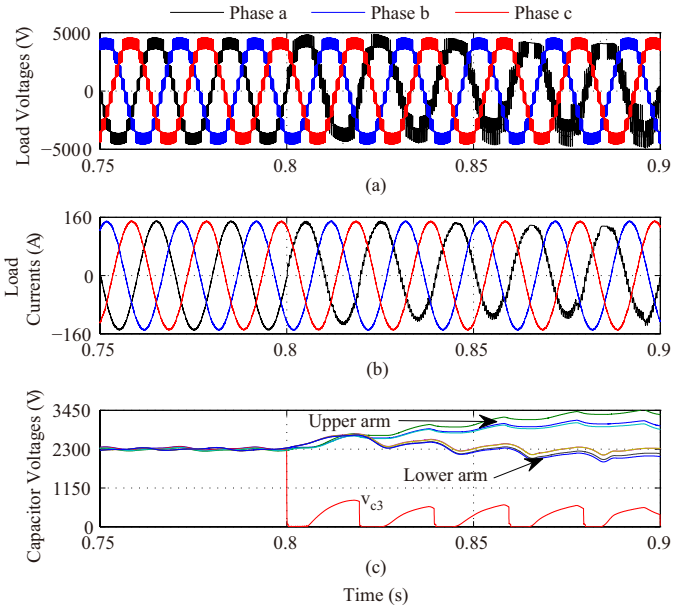

Fig. 18. Operation during a fault on the third sub-module of the upper arm. (a) Three-phase voltages. (b) Three-phase load currents. (c) Voltages of leg a sub-modules.

upper arm capacitors increase due to voltage drop in the faulty sub-module, while the voltages of the lower arm capacitors oscillate around the set value.

Fig. 19 and Fig. 20 demonstrate the fast dynamic response of the proposed ADALINE algorithm for estimating the DC voltages of different sub-modules. This result reveals that the proposed ADALINE algorithm succeeds in determining the faulty sub-module where the greatest deviation of the estimated capacitor voltage occurs. As a result, the proposed estimation unit is a candidate for sub-module fault detection and localization, which are essential tasks for fault-tolerant control of the MMC. During the fault, the circulating current, averaging, and balancing control signals oscillate with the power frequency component, as illustrated in Fig. 21.

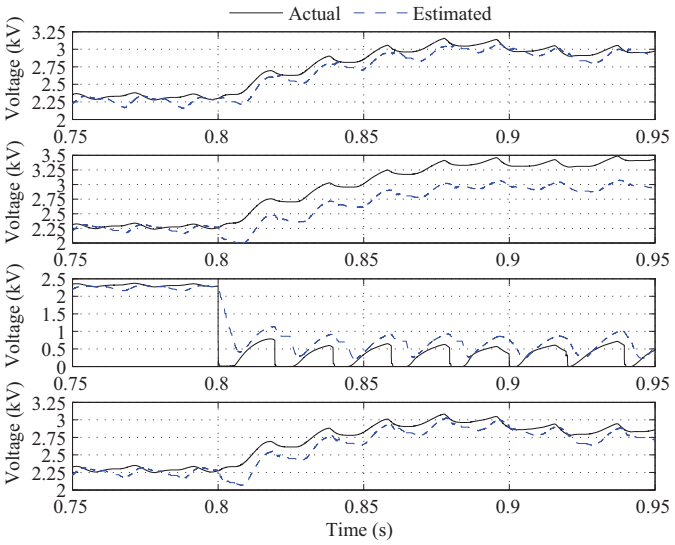

Fig. 19. Actual and estimated voltages of the upper arm sub-modules of phase a during a fault on the third sub-module of the upper arm.

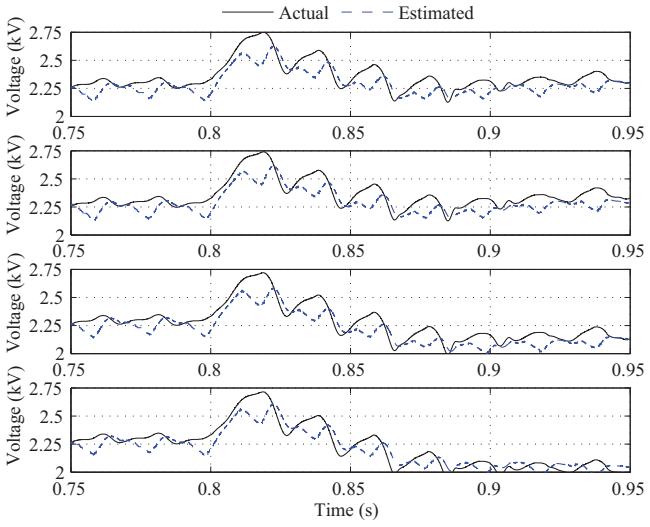

Fig. 20. Actual and estimated voltages of the lower arm sub-modules of phase a during a fault on the third sub-module of the upper arm.

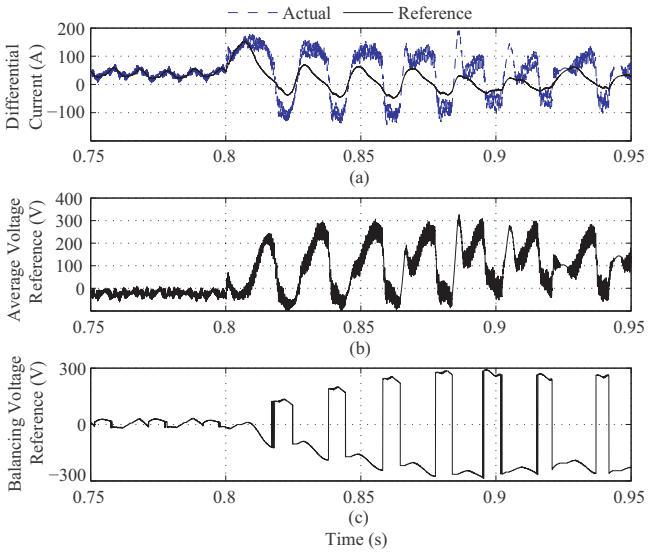

Fig. 21. Different controller actions for leg a during the faulty sub-module. (a) Actual and reference waveform of the circulating current. (b) Averaging voltage reference. (c) Balancing voltage reference for the first sub-module of the upper arm.

V. Conclusion

This paper presents an estimation unit based on the ADALINE algorithm for the sub-module DC voltages of the MMC. For each leg of the MMC, the proposed estimation unit requires only three sensors: one for the phase voltage and the other two for the voltages across the arm reactors. The proposed estimation unit is then integrated into a control strategy to balance the voltages across the sub-modules of the MMC. The proposed technique eliminates the need for direct measurement of capacitor voltages and associated communication systems, which renders it suitable for implementing a low-cost centralized controller for the MMC with a large number of sub-modules. The fast response and accurate tracking of the estimation unit under different dynamic conditions are validated in simulation results. Furthermore, the proposed MMC controller successfully balances the capacitor voltages at their set values even in boost operation mode. Finally, the circulating current is able to tightly track its reference signal, and the results demonstrate that the proposed ADALINE algorithm is able to successfully determine the faulty sub-module, which is required for implementing fault-tolerant control of the MMC.

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