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MOS based Nanocapacitor using C-AFM

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ABSTRACT

Nanocapacitors are integral devices of nanoscale MOS based integrated circuits and have not yet been realised. We report in this article our results to date on the realisation of such a nanocapacitor through the use of Atomic Force Microscopy (AFM) anodic oxidation to isolate nano-sized squares of poly-silicon, titanium and aluminium on Si/SiO_2. The focus of this work is on the Conductive AFM performed topographical and electrical characterization.

Keywords: Nanofabrication, SPM, AFM, Nanodevices

1. INTRODUCTION

AFM anodic oxidation[1] is a very powerful technique in nanotechnology that enables the growth of oxides with a minimal thickness of about 1nm and a lateral resolution of a few tens of nanometers. These oxides can be used as gate oxides, as etching masks[2] in wafer processing or as isolating dielectrics[3]. Topographical[4] and electrical characterisation[5] of the oxides can follow directly by conductive AFM.

The fabrication of metal-oxide-semiconductor (MOS) structures with AFM anodic oxidation grown SiO_2, as a gate dielectric, and their subsequent integration into a standard microelectronic process has already been seen[6]. However, nanocapacitors, integral features of nanoscale MOS based integrated circuits (ICs) have not yet been realised.

AFM anodic oxidation of titanium[7] and aluminium[8] amongst other conductive materials[9,10] has already been reported and therefore in order to realise the nanocapacitor we deposited titanium, aluminium, and polysilicon, on Si/SiO_2 and then proceeded to isolate nano-sized squares in them by this oxidation method. To define our structures as nanocapacitors we performed topographical and electrical measurements to confirm their size and electrical isolation or resistance to breakdown.

2. EXPERIMENTAL SET UP

All experimental work was done in ambient air with anodic oxidation and, topographic and electrical characterisation performed by a conductive atomic force microscope in contact mode, fitted with Pt-Ir, Co-Cr and Ti coated (20nm thick) n-type silicon cantilevers. A probe station connected to a Semiconductor Parameter Analyser was used to carry out additional electrical measurements.

Each sample consisted of a Phosphorus doped (10^{19} cm^{-3}) n-type Si(100) substrate, covered with a 6nm thermally grown SiO_2 layer and topped by a 3-5nm thick conductor (poly-silicon, titanium or aluminium) deposited by sputtering. The thickness of the conductors were chosen to be small enough as to be anodically oxidisable by AFM without the dielectric first breaking down[11,12,13] and big enough to not be completely consumed by natural oxidation[7,14]. The SiO_2 dielectric was chosen as 6nm to avoid quantum tunnelling effects and for the capacitor to be chargeable to a readable level (I_{min}=1pA for AFM and I_{min}=0.1pA for the probe station) without breaking down first (E_{BD}~1Vnm^{-1}) and to yield a low capacitance (~10fF) when the conductive layer was suitably oxidised to isolate conductive plates. Samples preparation of cleaning and passivation consisted of dipping the samples for 2 minutes at a time in each of the following: acetone, ethanol and then de-whetting the surface in dry nitrogen.

Anodic oxidation was performed under various voltage bias conditions but at a constant oxidation speed. All voltages referred to in AFM I-V measurements are those applied to the back-plane of the sample and not the tip.

To overcome problems with these simply structured samples we later designed and had fabricated at the CNM (Centro Nacional de Microelectronica, Barcelona, Spain) a series of structures (Figs 1,2,3) consisting of a ~3nm Ti finger on 6nm of SiO_2, each located in a pit which was formed by a standard MOS SiO_2 wet etch into a 200nm deep field oxide. The fingers are connected to a Ti bond pad, which allows direct probing by a semiconductor parameter analyser (SPA).

AFM anodic oxidation was also performed upon these Ti fingers to reduce their in-plane dimensions towards the nanoscale. The oxidation was done in squares, formed by growing parallel lines with a constant interlinear spacing and length. To confirm the existence of a nanocapacitor topographical and electrical measurements were then done on and around them.

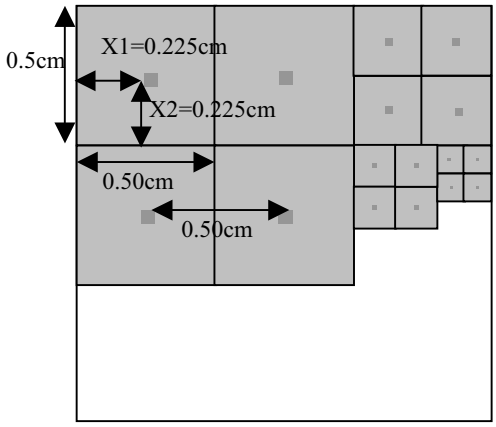

Fig.1. Schematic of 1.5cm x 1.5cm die of 4x4 different sized devices, proportional in dimensions. Devices consist of all combinations of finger dimensions (2x4µm, 1.5x3µm, 1x2µm, 0.5x1µm) and pad dimensions (500 x500µm, 250x250µm, 150x150µm, 100x100µm).

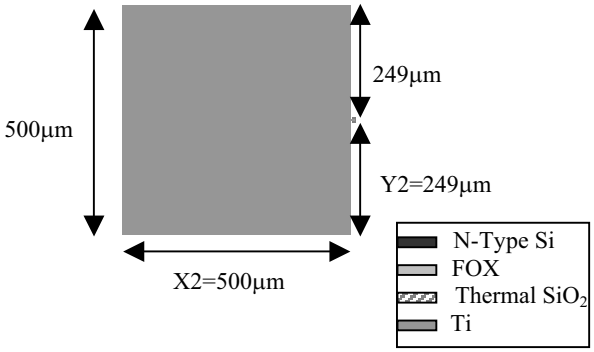

Fig.2. 500x500µm contact pad with Ti finger, 2x4µm to right hand side in etched oxide pit, shown to scale.

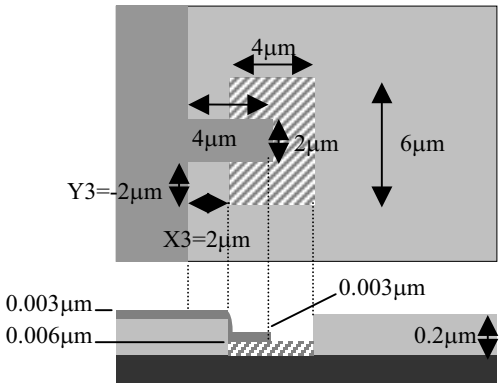

Fig.3. Plan view and cross-section close up of a Ti pad-finger intersection with the finger extending down into the pit formed from etched field oxide. Layer key as of Fig 2. Pit width is equal to the length of the finger and its length to three times the finger width.

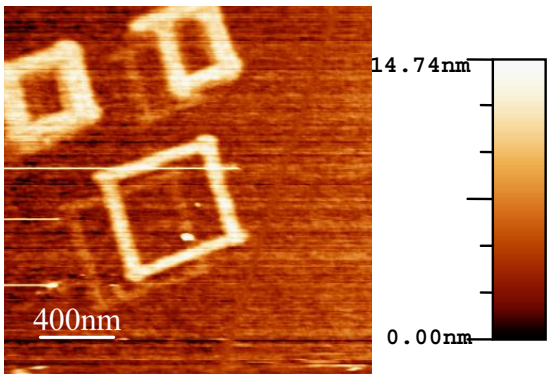

Fig.4. 0V tip bias topographic image of three squares anodically oxidised by AFM at 6V on a titanium surface.

3. RESULTS

Initial measurements (not presented here) found Poly-silicon to be too rough to oxidise. We focused our studies on the $Si/SiO_2/Ti$ structure as the Ti has a thinner natural oxide than the 2-3nm of Al[14] in its $Si/SiO_2/Al$ structure.

Initial IV measurements, with the top surface shorted to the back where the negative voltage was applied, taken inside of the titanium-oxide squares (Fig 4) suggest isolation (Fig 5 and 6) although later degradation can be seen (Fig 7). This is through Fowler-Nordheim tunnelling[15] that suggests that in measuring, the voltage stresses broke down the device.

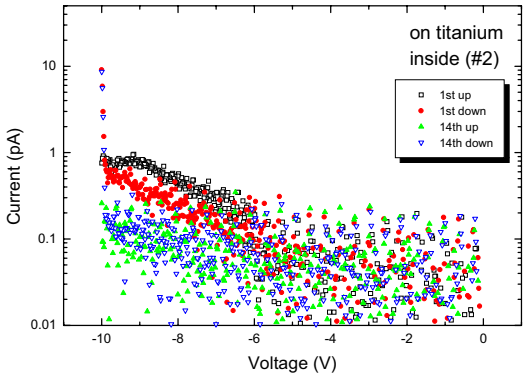

Fig.5. Current-voltage (I-V) ramps with the AFM tip inside the titanium oxide squares of Fig 4 after oxidation. Degradation occurs only at very high biases.

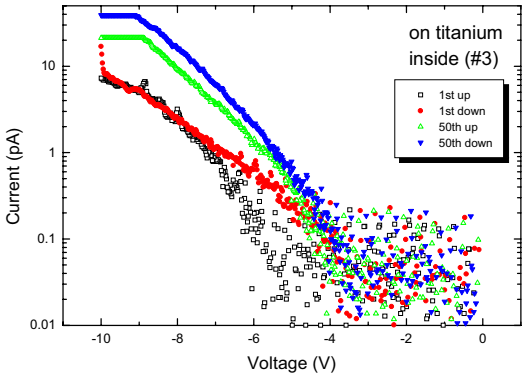

Fig.6. Subsequent I-V ramps with the tip inside the titanium oxide squares of Fig 4 show degradation, probably direct tunnelling above 4V.

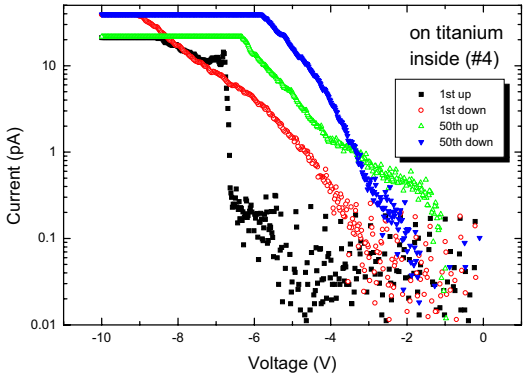

Fig.7. Further I-V ramps with the AFM tip inside the titanium oxide squares of Fig 4 show degradation at all biases, possibly via Fowler-Nordheim tunnelling.

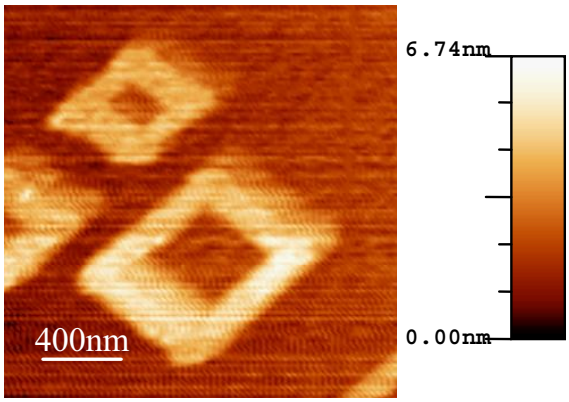

Fig.8. 0V tip bias topographic image of three squares anodically oxidised by AFM at 4V on a titanium surface

Other measurements showed inconsistencies such as negative current flow on the titanium-oxide squares when scanned at –9V. In addition two sets of 3 squares were oxidized at 4V and after one set (see Fig. 8) was scanned at voltages between –3 and –8V a subsequent zero voltage scan shows (see Fig. 9) that charge had been stored on the surface or on the Pt-Ir tip after the –3 to –8V scanning. Subsequent zero voltage scans show (see Fig. 10,11) that

through negative current tunnelling to the tip, plus possibly other ways, the surface current density decreases with time.

The other set of squares (see Fig. 12) were then scanned at 0V (see Fig. 13) and, although separated by some microns from where the other set had been charged whilst being scanned, a negative current flow (to tip) is also seen.

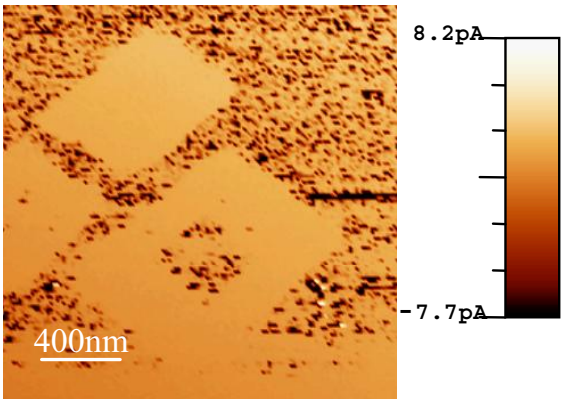

Fig.9. 0V bias current map of squares in Fig 8 at t=0.

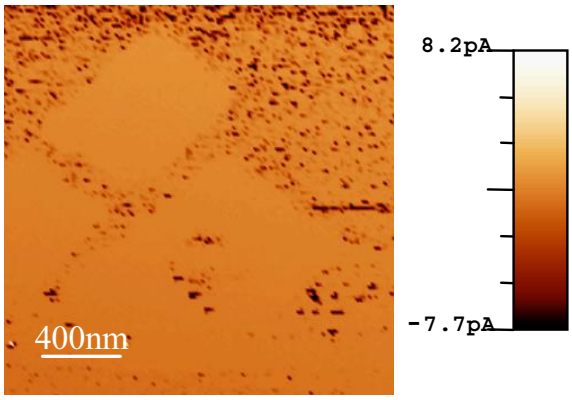

Fig.10. 0V bias current map of Fig 8 squares at t=4min.

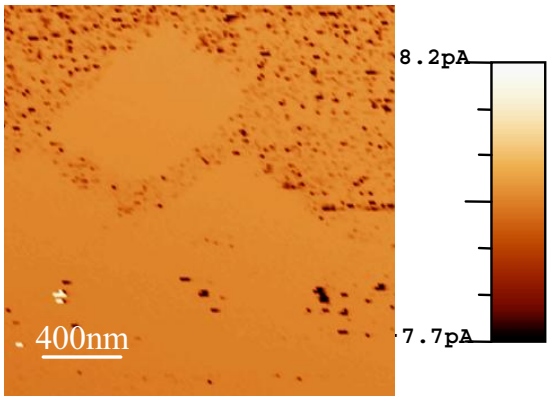

Fig.11. 0V bias current map of squares in Fig 8 at t=20min.

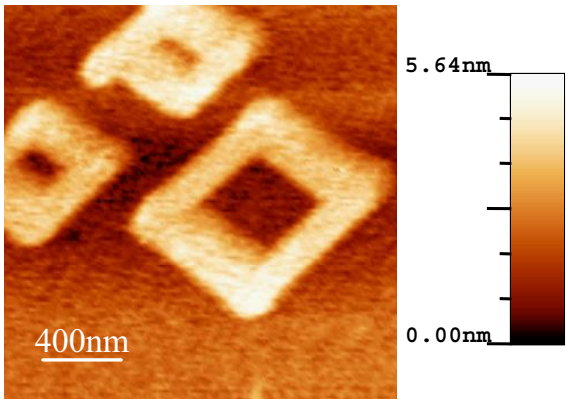

Fig.12. 0V tip bias topographic image of three squares anodically oxidised by AFM at 4V on a titanium surface.

This suggests charge transportation on the surface as well as supporting the idea of charge storage on the surface or tip as seen in the measurements of the previous set. The charge storage could occur in the great density of oxygen vacancies that makes TiO_2 an n-type semiconductor[16] and as such for a large enough negative substrate voltage a current will flow to the tip[17]. The barrier height of the native titanium oxide[16] was also thought to be contributing to C-AFM measurement inconsistencies.

We now present the results of the samples designed with a Ti finger. Initial AFM topographical images suggested that the Ti film was not deposited continually (see Fig. 14) in the second smallest sized pit (3x4μm) and not at all for the smallest sized pit (see Fig. 15).

All probe station current voltage ramps (I-V) measurements on various devices showed, after subtracting displacement and offset current from that measured, that the residual current appeared to be dominantly ohmic (see Fig 16). This ohmic behaviour appeared from at least 10mV upwards which is too low an applied voltage for the 6nm of gate oxide to have broken down (breakdown field for SiO_2 is ~$1Vnm^{-1}$). It is not understood why ohmic current is seen without breakdown characteristics being observed.

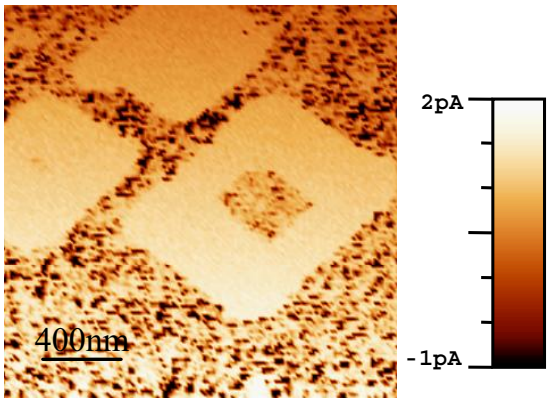

Fig.13. 0V tip bias current map of three squares anodically oxidised by AFM at 4V on a titanium surface.

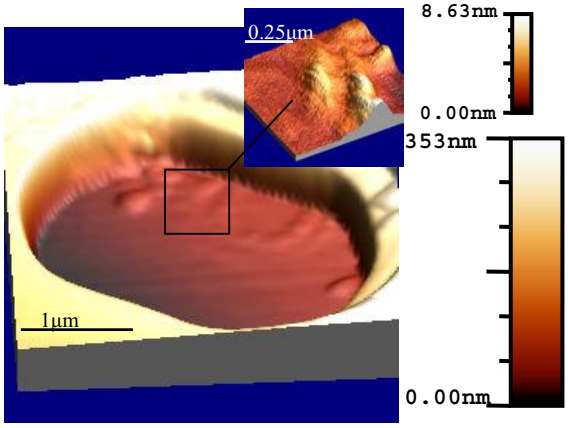

Fig.14. 3D topographical image of a 3x4µm etch pit with discontinuous Ti finger (1x2µm) extending down and from edge of right hand long side of pit. See Fig.3 for schematic.

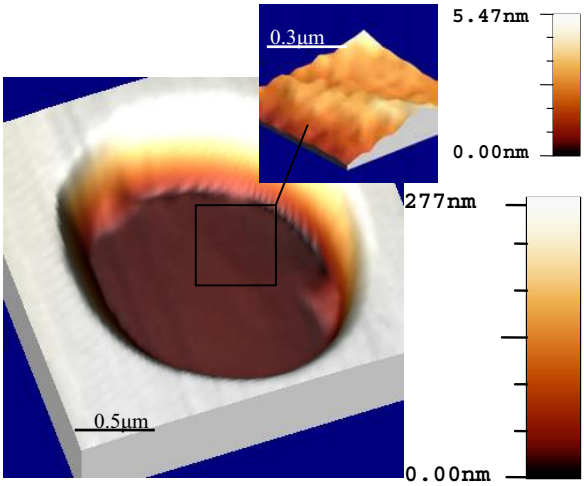

Fig.15. 3D topographical image of a 1.5x2µm etch pit with discontinuous Ti finger (0.5x1µm) extending into it from edge of right hand long side.

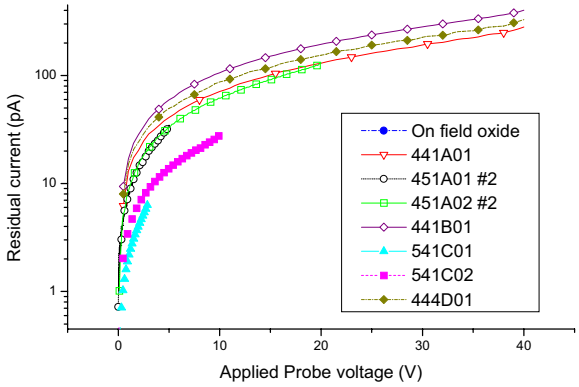

Fig.16. Probe station IV ramps measurements of various. Curves are labelled: die number (11-88) / pad size (1-4 with 1 being the largest) / finger size (A-D with A being the largest) and measurement number for that device.

TiO_2 has been reported[18] to have a resistivity of ~10^{10}Ωcm which for a 1nm thick layer and a ~1µm^2 area of probe station tip results in a resistance of ~10^{11}Ω, which is of the same order as seen in all probe station measurements. The oxide has a slightly inferior dielectric breakdown to SiO_2 at 0.6-1 Vnm^{-1} so there could be a significant oxide barrier in the path to the Ti finger/gate oxide/Si structure. In order to determine whether this barrier was actually in this structure or between it and the bond pad, various C-AFM measurements were carried out on one of the die. A device with the largest pit and finger was chosen, i.e. one with a good Ti film continuity (see Fig. 17).

Various I-V ramps were performed on the SiO_2 (see Fig. 18) surrounding the Ti finger inside the pit (see Fig. 17) and then on the finger before (see Fig. 19) and after (see Fig. 20) repetitive anodic oxidation was attempted on 90% of its surface area i.e. our attempt to reduce the Ti to 100nm x 100nm. The pre-oxidation measurements (see Fig 19) show that the finger undergoes degradation and therefore there is no substantial oxide barrier on the structure to explain the probe station IV measurements. The IV data also shows that although the 12V ramps for Ti (see Fig 19) differs to that for SiO_2 (see Fig 18), after anodic oxidation (see Fig. 21) they are similar (see Fig. 20). Although this suggests

oxidation has successfully taken place, roughness and height profile measurements (not presented here) from figure 21 are indistinguishable from those of pre-oxidation. However, as the height of the fingers is measured at only ~0.8nm, it is uncertain as to whether a topographical change would be noticeable.

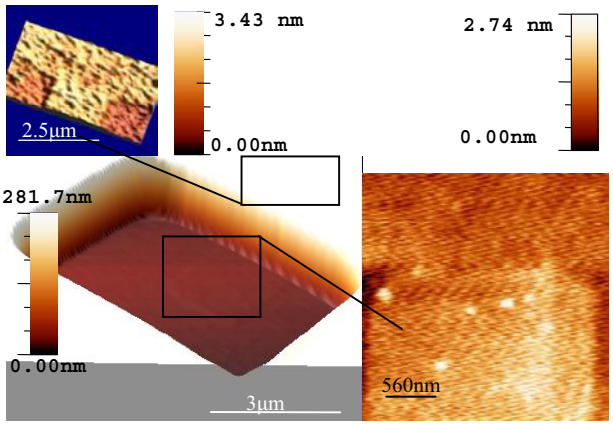

Fig.17. Main image: AFM topographical representation of '251A'. Upper right image: the intersection of the Ti finger and Ti bond pad. Lower right image: The Ti finger inside the etch pit - breakdown spots can be seen on the finger. Pit edge along bottom of image.

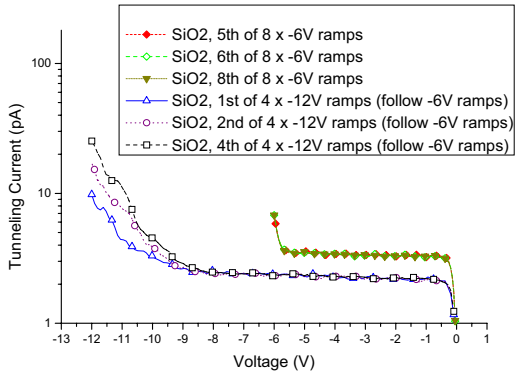

Fig.18. C-AFM I-V ramps on SiO2 at bottom of etch pit, near Ti finger. Voltage is applied to the back-plane of the wafer.

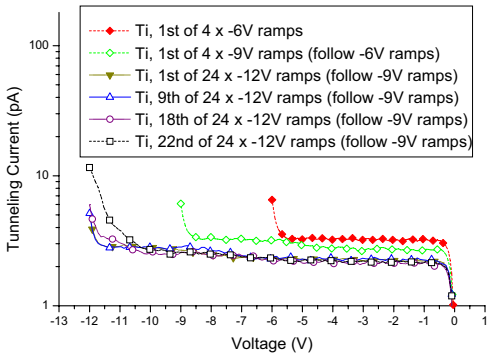

Fig.19. C-AFM I-V ramps on Ti finger at bottom of etch pit. Voltage is applied to the back-plane of the wafer.

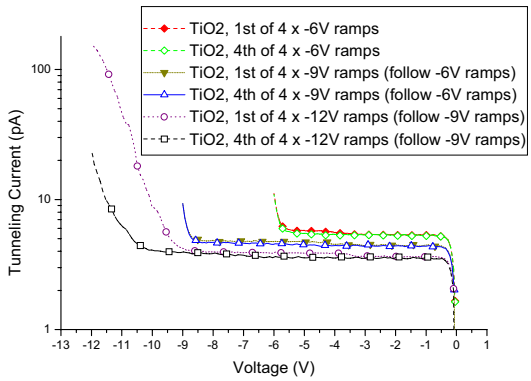

Fig.20. C-AFM I-V ramps on Ti finger, after repeated oxidation, at bottom of etch pit. Voltage is applied to the back-plane of the wafer.

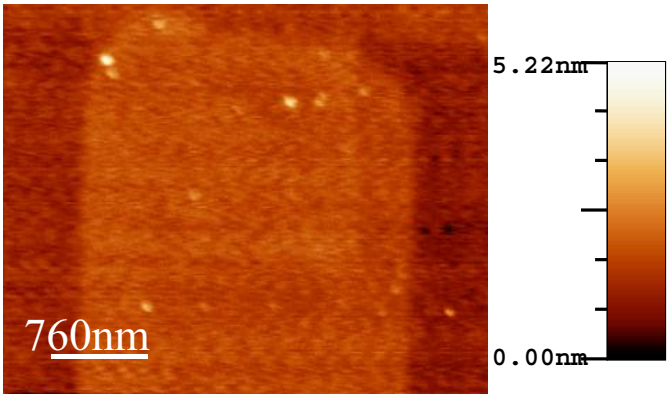

Fig.21. AFM topographical representation of the Ti finger inside the etch pit after 90% area oxidation. Breakdown spots can be seen on the finger and SiO_2 near the finger.

Subsequent repetitive I-V ramp measurements (not presented here) up to 11V (tip voltage) on the junction between the pad and finger could not breakdown the finger and so further reduction was seen as irrelevant. In other words, either the Ti had not flowed well in deposition and so the pad and finger in the pit were not physically connected or the interlayer was so thin that it had completely oxidised. This was confirmed after approaching the MOS fabrication facility[19].

4. CONCLUSION

In our contribution to realising a nanocapacitor we have used C-AFM to successfully reduce a Ti on SiO2/Si based structure down to linear dimensions of 10s of nm. Due to the native oxide of Ti and its barrier height, however, the electrical confirmation of its dielectric capability as a capacitor has proven difficult. MOS processing of further structures connected to bond pads for easier electrical characterisation has encountered a technology problem with critical thinning of the Ti in the interconnect. A focused ion beam measurement would confirm this.

5. ACKNOWLEDGEMENTS

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