

## Research Article

# An Analytical Gate-All-Around MOSFET Model for Circuit Simulation

Kuan-Chou Lin,<sup>1</sup> Wei-Wen Ding,<sup>2</sup> and Meng-Hsueh Chiang<sup>1</sup>

<sup>1</sup>MS Degree Program on Nano-IC Engineering, Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan

<sup>2</sup>Department of Electronic Engineering, National Ilan University, I-Lan 260, Taiwan

Correspondence should be addressed to Meng-Hsueh Chiang; mhchiang@mail.ncku.edu.tw

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A generic charge-based compact model for undoped (lightly doped) quadruple-gate (QG) and cylindrical-gate MOSFETs using Verilog-A is developed. This model is based on the exact solution of Poisson's equation with scale length. The fundamental DC and charging currents of QG MOSFETs are physically and analytically calculated. In addition, as the Verilog-A modeling is portable for different circuit simulators, the modeling scheme provides a useful tool for circuit designers.

## 1. Introduction

According to Moore's law, CMOS transistors continue to scale. The transistor size scaling provides for increased packing density, improves circuit speed, and lowers power consumption. However, many small-geometry effects have surfaced such as short-channel effects, limiting the device performance. In order to overcome these issues, improving device gate controllability is necessary. Multigate transistor architecture is regarded as one of the most effective ways to improve the short-channel effects and to enhance the gate controllability [1–3]. The gate-all-around (GAA) MOSFETs have drawn much attention for ultimate device scaling. To expedite further VLSI development using GAA devices, we use Verilog-A to develop the SPICE device model which can be used by circuit/device designers with a simple set of physical parameters.

## 2. Potential Model and *I-V* Model Based on Scale Length

We propose a scale-length based GAA MOSFET model. The schematic diagram of the QG MOSFET for modeling is shown in Figure 1. The model is based on an undoped n-channel multigate MOSFET.

Unlike most models limited to a certain specific type of the gate, the proposed model is highly scalable and is generic to both quadruple-gate (QG) and cylindrical-gate structures. Poisson's equation for potential can be written as [4]

$$\frac{1}{\gamma} \frac{\partial}{\partial y} \left( \gamma \frac{\partial}{\partial y} \phi(r, y) \right) + \frac{\partial^2}{\partial z^2} \phi(r, y) = \frac{qN_a}{\epsilon_{si}}, \quad (1)$$

where  $N_a$  is the channel doping (assumed to be uniform in the model) and  $r$  represents any position in the channel [4], which is equivalent to  $(W \times H)/(W + H)$  for any specific location  $(W, H)$  in  $x$ - $z$  plane [5]. The solution for  $\phi(r, y)$  is

$$\phi(r, y) = \phi_c(y) - \left( \frac{(2\epsilon_{ox} r^2 (\phi_c(y) - \phi_{gs}))}{(\epsilon_{si} t_{si}^2 \ln(1 + 2t_{ox}/t_{si}) + \epsilon_{ox} t_{si}^2/2)} \right), \quad (2)$$

where  $\phi_{gs} = V_{GS} - V_{FB}$ ,  $t_{si} = 2 \times (W_{si} \times H_{si})/(W_{si} + H_{si})$ , and  $\phi_c(y)$  is the channel center potential, which can be solved at  $r = 0$  as

$$\frac{\partial^2}{\partial y^2} \phi_c(y) - \frac{((\phi_c(y) - \phi_{gs}))}{\lambda^2} = \frac{qN_a}{\epsilon_{si}}, \quad (3)$$

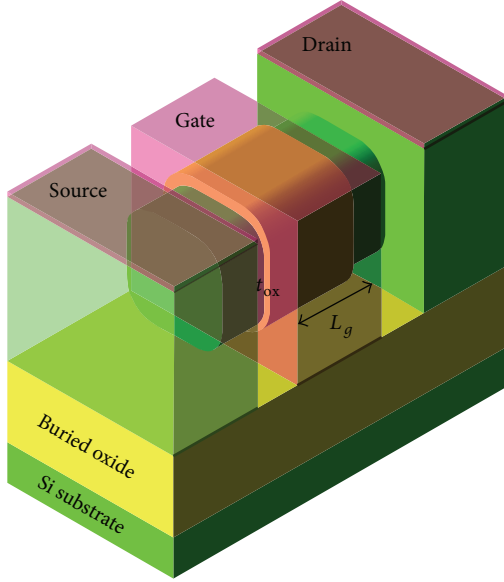


FIGURE 1: The schematic diagram of the QG MOSFET.

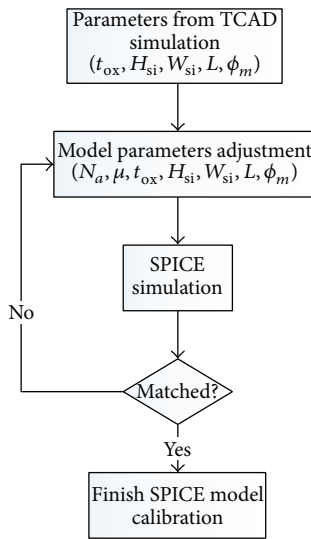


FIGURE 2: The calibration flow for model parameters.

where  $\lambda$  is defined as the scale length:

$$\lambda = \sqrt{\frac{(2\epsilon_{si}t_{si}^2 \ln(1 + 2t_{ox}/t_{si}) + \epsilon_{ox}t_{si}^2)}{(16\epsilon_{ox})}}. \quad (4)$$

The scale length gives a measure of the short-channel effects inherent in a device structure. To ensure our model accuracy, we use TCAD simulation for calibration. Figure 2 shows the calibration flow for SPICE model parameters. Due to the physical nature of the model, the calibration process is straightforward. To demonstrate the predictability of the model, it is applied to a case with model parameters  $H_{si} = 10$  nm,  $W_{si} = 10$  nm,  $L = 10$  nm, and  $t_{ox} = 0.62$  nm. Figure 3 shows the predicted  $I$ - $V$  characteristics where near ideal subthreshold slope and drain-induced barrier lowering (DIBL) of 79.68 mV/V are predicted.

### 3. Charge Model

The terminal charges are based on previous potential equation. The boundary conditions used for (1) are  $C_{ox}(V_G - V_{FB} - \phi_s) = -\epsilon_{si}E_s = Q_{si}$  for  $r = R$  and  $d\phi/dr = 0$  for  $r = 0$ , where  $C_{ox}$  is the oxide capacitance,  $V_{FB}$  is the flat band voltage,  $\phi_s = \phi(r = R)$  is the surface potential,  $E_s$  is the surface electric field, and  $Q_{si}$  is silicon charge density per unit gate area [6, 7]. From them, we can obtain the mobile charge density ( $q_m$ ) as a function of the difference between surface and center potentials ( $\alpha = \phi_s - \phi_c$ ):

$$q_m = \sqrt{\frac{4q_p\epsilon_{si}}{C_{ox}}}\sqrt{\alpha}\sqrt{0.5 + \left[\frac{1 - 1/\alpha + (1/\alpha)e^{-\alpha}}{\alpha}\right]}e^{q(\phi_s - V - 2\phi_F)/kT} - q_p, \quad (5)$$

where  $q_p = qN_aR/2$  is the fixed charge density,  $V$  is the quasi-Fermi potential in the channel, and  $\phi_F$  is the Fermi potential.  $q_m$  takes the value of  $q_s$  at the source ( $V = 0$ ) and  $q_d$  at the drain ( $V = V_{ds}$ ). Figure 4 shows the charge density (per unit area) at the source end ( $V = 0$ ) in logarithmic and linear scale.

We then use  $q_s$  and  $q_d$  to calculate charge current as

$$I_{ds} = \mu WC_{ox} \left(\frac{kT}{q}\right)^2 \left\{ \frac{(1/2)(q_s^2 - q_d^2) + [2(q_s - q_d) + q_p \ln((q_d + 2q_p)/(q_s + 2q_p))]^{SS}}{L - \Delta L} \right\}, \quad (6)$$

where  $\mu$  is short-channel effect mobility,  $W$  is the channel width, SS is the subthreshold slope degradation, and  $\Delta L$  is the channel length modulation.

Figure 5 shows the charging current network. Based on the charging current network, we can obtain total inversion capacitance by measuring gate charging current from AC simulation, as shown in Figure 6.

### 4. VLSI Application

To ensure the validity of the model for IC simulation, different types of circuit simulation including inverters and static random access memory (SRAM) are used for verification [8]. Inverters are the basic circuit block for assessing CMOS technology. Figures 7 and 8 show the inverter DC and transient

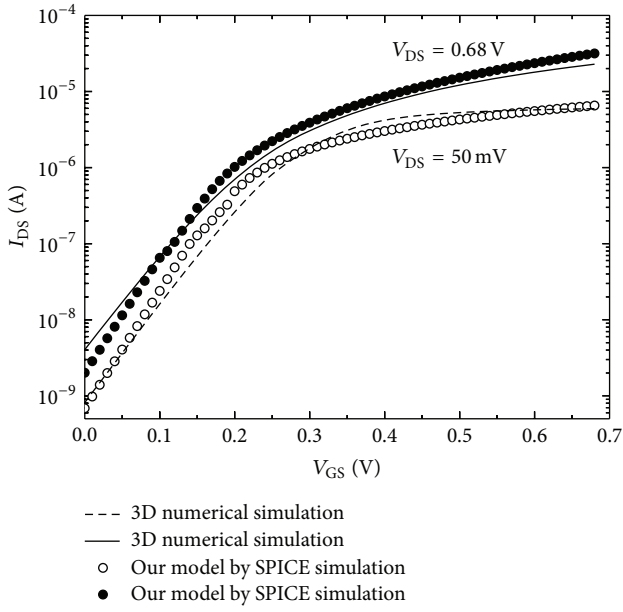


FIGURE 3: Simulated drain current as a function of gate voltage at low and high drain biases.

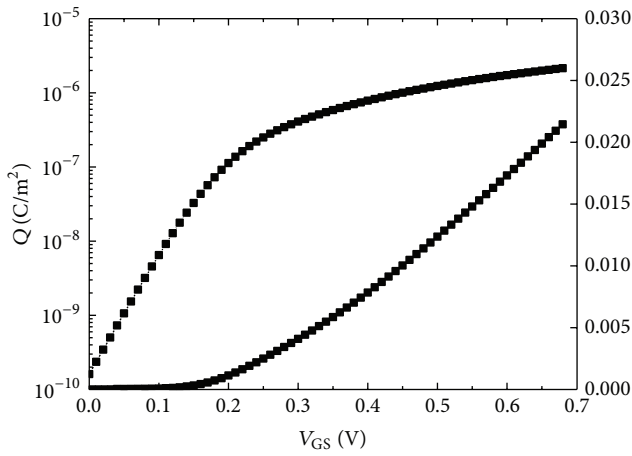


FIGURE 4: Channel charge density (per unit area) at the source end ( $V = 0$ ) in logarithmic and linear scale.

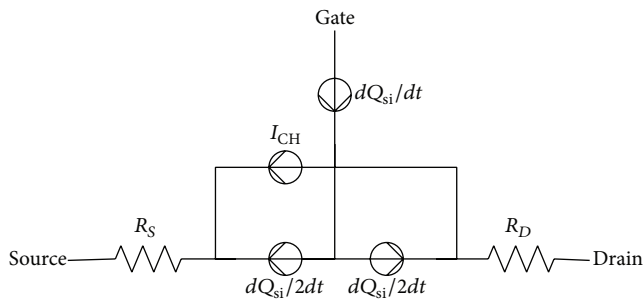


FIGURE 5: Charging current network diagram.

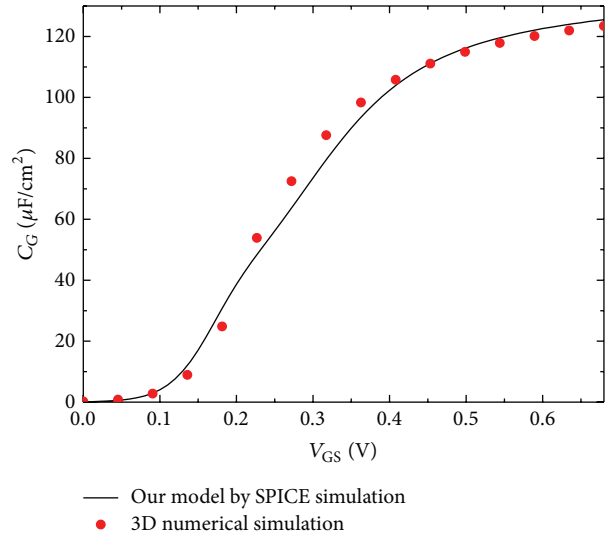


FIGURE 6: Total gate capacitance as a function of gate voltage extracted from AC simulation.

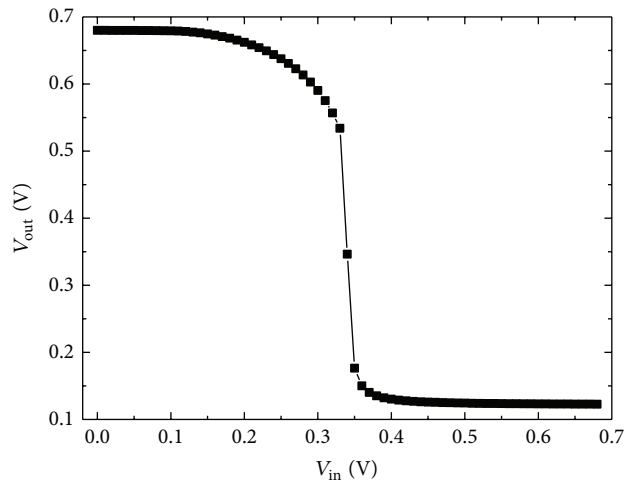


FIGURE 7: DC simulated inverter transfer curve.

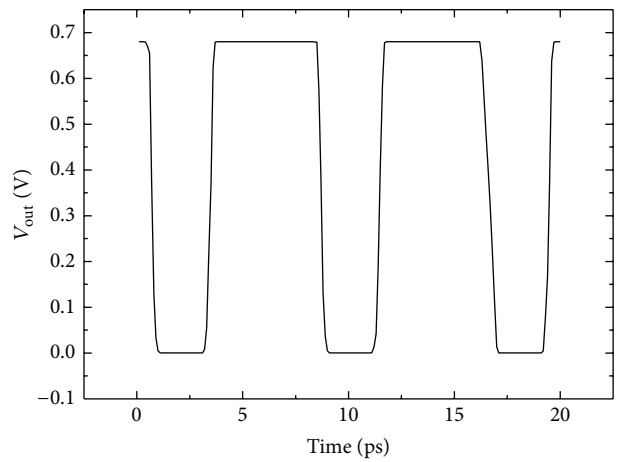


FIGURE 8: Transient simulated inverter response.

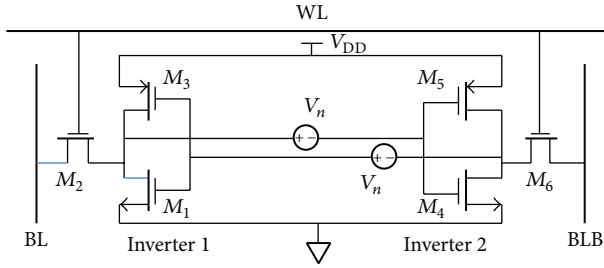


FIGURE 9: Conventional 6T SRAM.

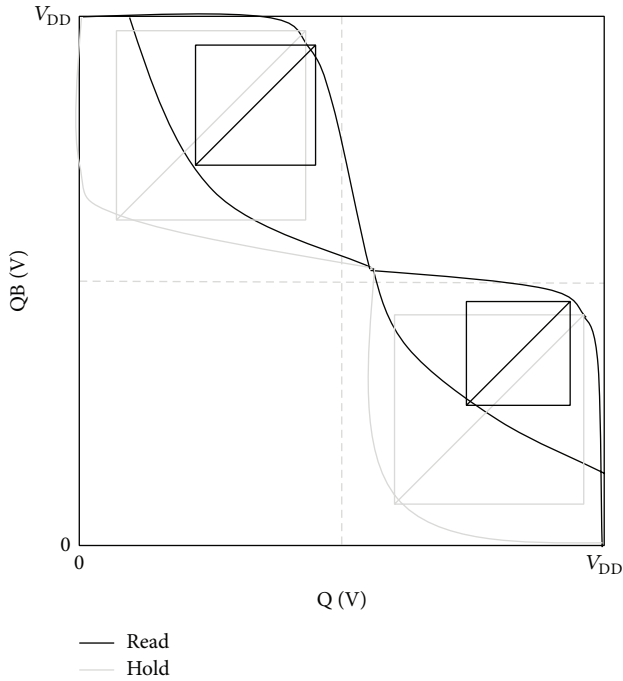


FIGURE 10: Read and hold SNMs [9].

simulation using the GAA model, from which the intrinsic inverter speed can be extracted. The circuit simulation gives an insight to device performance very efficiently based on the physical DC  $I$ - $V$  and charge models.

Figure 9 shows the circuit schematic of a 6-T SRAM. To analyze the hold static noise margin (SNM), the bit line (BL) and bit line bar (BLB) are biased at a high voltage (usually  $V_{DD}$ ) and word line (WL) is biased at low voltage. One may measure the difference in voltage between point Q and point QB. Because the word line is in the low voltage condition, the two pass-gate transistors on the sides are kept at off condition. The potential changes in BL and BLB do not influence the potentials at point Q and point QB. When analyzing the read static noise margin, a high voltage was given to WL to keep two transistors on two sides on. The BL and the BLB are also biased at a high voltage. One can measure the difference in voltage between point Q and point QB. An example of read and hold SNMs is shown in Figure 10 [9].

Figure 11 shows the simulated static noise margin of the 6-T SRAM using the proposed GAA model. In the hold mode, two transistors on two sides are off, so the inputs in BL and

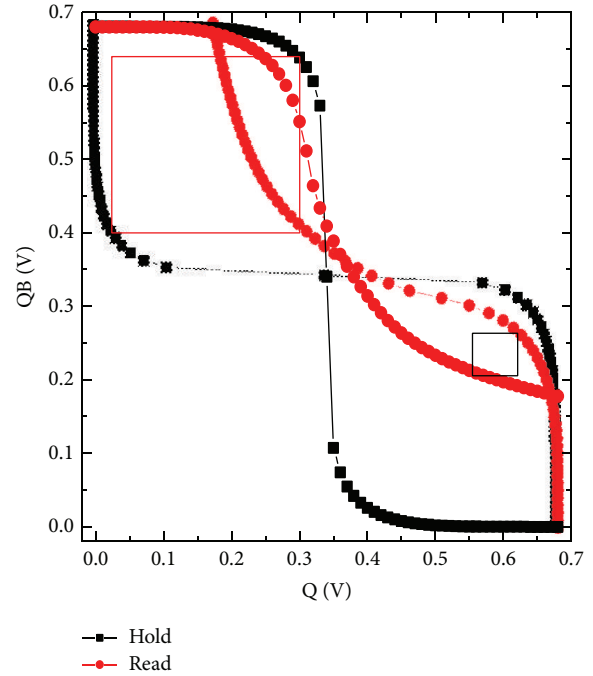


FIGURE 11: Predicted SRAM hold and read SNM curves.

BLB do not influence the potentials at point Q and point QB. Such SNM reflects the ideal voltage transfer characteristics of the inverter. However, in the read mode, two transistors on the sides conduct, so BL and BLB will influence the conditions at point Q and point QB. As can be seen, the read SNM region is much smaller than that of the read SNM region.

## 5. Conclusion

A generic and charge-based compact modeling approach applicable to both quadruple-gate and cylindrical-gate structures was proposed. The model can be used straightforwardly with physical parameters such as gate work function and structural parameters. The model is analytical and efficient enough for circuit applications.

## Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

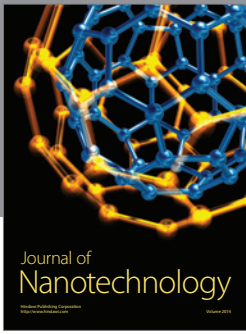
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