FABRICATION AND CHARACTERIZATION OF AL / ALO_X / AL JOSEPHSON JUNCTIONS

A Thesis

by

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ABSTRACT

This thesis works deals with the fabrication and characterization of Josephson Junctions. An upgrade over the existing fabricating process with the aim of integrating Josephson Junctions with hetero-structure based HEMT devices was the main aim of this research work. In order to achieve this, new fabrication technique with aim of fabricating small area overlap junction is presented. Josephson Junctions are a Metal-Insulator-Metal capacitor, with both of its electrodes as superconductor metals having femto Farad capacitance and low resistance.

The current transfer mechanism across very thin junctions was discussed and the related tunneling current equations were deduced after extracting the equations from the Wentzel-Kramers-Brillouin (WKB) approximation. These junctions are prone to various kinds of tunneling current phenomenon. A relationship between the room temperature tunneling current for a Metal-Insulator-Metal (MIM) capacitor and that to the resistance of the Josephson Junctions above its critical temperature was derived. A new fabrication method consists of a side-wall overlap area was presented in order to fabricate these Josephson Junctions. The dielectric / insulator layer was also deposited using a relatively new approach of Atomic Layer Deposition technique.

Using this new fabrication approach, Josephson Junctions with the small area overlap, lower capacitance and resistance values were obtained. Capacitances for

these devices were measured using an E4980 Agilent Precision LSR meter system with a 2 point probe setup. The same setup was used in order to obtain Current (I) vs. Voltage (V) sweep values for the Josephson Junctions, in order to identify the tunneling mechanism occurring in the junctions. Barrier height and effective mass of the dielectric were calculated from these tunneling plots.

It was observed that these junctions had an area overlap of ~ 0.75 μm^2 with capacitance ~ 100 fF and resistance ~ 150 $\Omega\ \mu m^2$. These values where in the same range to the value from literature which utilized the dolan bridge fabrication technique. Hence, this concluded that the step-edge technique is better approach towards fabrication of small overlap Josephson Junctions with the aim of integrating them with HEMT based devices.

DEDICATION

To my parents, Savita and Rajkumar Sharma and brother Karan …

Your love and support will always be remembered.

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1. INTRODUCTION

1.1 Why Josephson Junctions

Josephson Junctions are similar to Metal-Insulator-Metal capacitor devices but with the metal replaced by a superconductor metal. Josephson Junctions are the most basic building blocks of the present day Quantum circuits [1]. They are basis of the superconducting devices such as qubits, SQUIDS and amplifiers [2, 3]. With the current development trend in the field of superconductors and quantum devices, it places an even more pressure on the development of smaller and large operational frequency Josephson Junctions which can be integrated with other hetero-structure devices such as High Electron Mobility Transistors fabricated on a GaN / AlGaN hetero-structure.

The most common technique used in the fabrication of Josephson Junctions uses the Dolan Bridge fabrication process [4], this process suffers from many critical issues, such as junction alignment, material selectivity and integration issues to existing devices. Therefore, an improved fabrication process is put forward through this research work, which can be transferred to various materials and used to integrated quantum based devices with existing RF or CMOS devices.

1.2 Thesis Structure

Section 2 of thesis provides a theoretical approach to the conduction mechanism in Metal-Insulator-Metal capacitors and Josephson Junctions. Various tunneling condition mechanism were discussed and the required equations were identified in order to understand a clear relationship between the parameters controlling the tunneling

across the dielectric. Equivalent models for MIM and Josephson Junctions were created and their combined electric equation is presented. Section 2 also goes over the Josephson Effect and the equations governing the flow of electrons through the barrier.

Section 3 presents the current fabrication processes used in the fabrication of Josephson Junctions and presents the new approach towards the fabrication of Josephson Junctions with aim of integrating junction devices with other exists CMOS devices. Section 4 consists of all the electrical characterization carried out on the newly fabricated junction devices. It consists of I-V, C-V, G-V plots and all the tunneling mechanism plots discussed in section 2.

Section 5 is a summary of section 3 and 4 and provides the future applications of the research work presented in this thesis.

2. THEORETICAL BACKGROUND: MIM CAPACITORS AND JOSEPHSON JUNCTIONS

2.1 Fundamentals of Metal-Insulator-Metal (MIM) capacitors (diodes)

Metal-Insulator-Metal capacitors (or diodes) consist of a thin dielectric / insulator layer which is sandwiched between two similar to dissimilar metal electrodes. When both the metal electrodes across the insulator are same, the device is referred to as Symmetric MIM capacitors (or diodes), whereas when the two metal electrodes are different, the device is then referred to as Asymmetric MIM capacitors (or diodes). MIM devices have been fabricated for a long time, with applications in the field of high frequency range devices and solar cell industry.

MIM devices are ideally supposed to be perfect insulator to the current flow across the dielectric barrier. However, when the dielectric is in lower range of nanometers, electrons are capable of tunneling across the barrier of the dielectric into the conduction band of the other metal electrode. When an electron travels through a potential barrier (a barrier formed when a metal and dielectric layer are brought together), instead of overcoming it, the electron is referred to have undergone Quantum-mechanical tunneling [5]. There is no loss of energy during this quantum mechanical tunneling process. From classical particle physics, an electron is supposed to observe a net repulsive force leading to a state of complete rest, when placed under an electric field. However, from the wave theory of physics, it is observed that the electron interacts in a similar way to electric field, when considered as a particle under electric field.

However, it differs from the particle theory by stating that, though it is very less, but the electron under wave condition, has a finite probability of tunneling through thin dielectric layers [5]. This phenomenon of electron going through a dielectric is referred to as the Tunnel Effect and leads to buildup of tunnel current across the barrier, when bias in the small ranges is applied across the junction barrier.

When the two metal electrodes are of different type or same but deposited through different techniques, asymmetric behavior can be noticed in their I-V characteristic, especially, when the work function difference between the two electrodes is extremely large. Tunneling occurs across if the barrier is extremely thin, something in the order of just a few nano-meters. As the thickness of the dielectric / insulator layer increases, it allows far less electrons to tunnel through the barrier, thereby increasing the overall resistance of the junction.

The barrier height for a MIM diode with similar and different metal electrodes arrange differently on the energy band diagram. It also shows how the barrier changes with application of electric field on the bias applied metal electrode. For tunneling to occur in MIM diodes with similar metal on both sides, a bias needs to be required. However, if the work functions in the case of different metal MIM diodes, is different in huge orders of magnitude, small amount of tunneling current can be observed in the device without application of an additional electric field.

2.2 Characteristics of a MIM device

MIM devices, especially MIM diodes are characterized by using the current–voltage plots obtained from their electric characterization. Capacitance-Voltage and

Conductance-Voltage plots at various frequency range are also carried out in order to attain more technical aspects of the fabricated device. The current-voltage plot data can be used in identifying any asymmetric behavior across the junction. The differential resistance is also obtained from the current-voltage curve, and is obtained by differentiating the tunneling current across the junction to the voltage applied. As mentioned earlier, the resistance of the device is expected to increase with increasing the thickness of the dielectric layer, as the probability of the electron tunneling through the barrier decreases.

The data obtained from the current-voltage plots of the MIM diodes with and without similar metal electrodes is used in order to identify the tunneling mechanism occurring across the junction. This is carried out by using the raw data and plotting the plots with relationship between the Current Density, J and the applied Electric field. Various plots need to be plotted in order to understand the tunneling behavior for the junction devices at different voltage ranges.

The equivalent circuit of a Metal-Insulator-Metal diode can be described by a junction capacitance C in parallel with a non-linear voltage-dependent resistance R (V). This parallel combination is in series with a resistance r, which represents the metal-lead and/or the spreading resistance [6]. Figure 1 represents the equivalent circuit of a MIM diode.

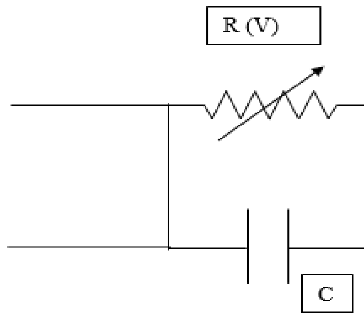


Figure 1 An equivalent electric circuit for a Metal-Insulator-Metal capacitor

The RC time constant for this circuit is equivalent to the product of the of voltage dependent Resistor R (V) and the capacitance of the circuit C. This also gives us that the cut of frequency of the circuit, f_c is given as follows [6]:

$$f_c = 1 / (2 * \pi * R(V) * C) \quad (1)$$

The capacitance of the circuit is calculated by using the parallel plate capacitor setup, and is given by the following equation:

$$C = (\varepsilon_0 * \varepsilon_r * A) / d \quad (2)$$

where ε_0 is the permittivity of free space, ε_r is the relative permittivity of the dielectric material, A is the overlap area and d is the dielectric thickness. As the aim is have a large frequency of operation, the capacitance needs to keep to very low orders, in femto-farads especially for the Josephson Junctions devices.

The C-V and G-V plots of the MIM capacitors are carried out at different frequencies in order to understand the behavior of the conductance and capacitance as the frequency is swept from a few hertz to megahertz, both above and below the pole frequency of the circuit.

2.3 Conduction mechanism in Metal-Insulator-Metal capacitors

Ideally, a Metal-Insulator-Metal capacitor is supposed to be resistant to current flow across the barrier. However, when the dielectric film is in the low order of nanometer, current is able to flow through the dielectric to the other metal side. Dielectric film quality and pin hole density can also be responsible for current flow across the barrier. This current is referred to as the Tunneling current or the Leakage current. There are a number of methods associated with the tunneling of electrons through the barrier. A few of these tunneling behaviors which are of at most significance, such as Fowler-Nordheim Tunneling (FNT), Direct Tunneling (DT), Poole-Frenkel Tunneling (PFT), Trap Assisted Tunneling (TAT), in regard to conduction mechanism in a Metal-Insulator-Metal capacitors are discussed in this sub section [7].

Various models have been used in order to put forward an easily understandable equation for various kinds of tunneling mechanisms. The transmission coefficient of a dielectric layer, the probability of an electron able to tunnel through a dielectric requires solving the Schrodinger's equation. The Wentzel-Kramers-Brillouin (WKB) approximation is used in order to identify an approximate solution to a system of linear differential equations with spatially varying coefficients [8]. The first work in regard to tunneling through insulators foe low voltages was done by 'Sommerfield and Bethe'. They provided an equation for the tunneling current at low temperature, which was related to the barrier height at the junction. Simmon also presented an equation for electric tunnel effect through a barrier of any arbitrary shape [8]. Equation 3 [8] accounts

for the effective mass of the electron in the dielectric film along with the barrier height at the junction.

$$J = \frac{1.1\,q^2}{4\pi h}\frac{1}{\varphi_b}(\frac{V+\Delta\varphi_b}{S})^2 \times \exp(\frac{-23\pi\sqrt{qm}}{6h}\varphi_b^{\frac{3}{2}}\left(\frac{S}{V+\Delta\varphi_b}\right)) \qquad (3)$$

where q is the electronic charge, V is applied voltage bias, ϕ is the barrier height, m is the effective electron mass in the dielectric and h is Plank's constant [8].

Image Force Effects the oxide barrier in the case of symmetric Metal-Insulator-Metal capacitors, these are the capacitors with same metal electrode on both sides of the dielectric layer. Electrons polarize the metal surface, thereby causing the metal surface to create a net attractive force on the electrons. As a result, there is huge electron accumulation near the barrier, causing barrier potential to restructure by rounding off the corners and narrowing the barrier width. Image Force Effects are observed in Metal-Insulator-Metal capacitors with both metals as same. Figure 2 shows some of the tunneling phenomena occurring in a MIM device.

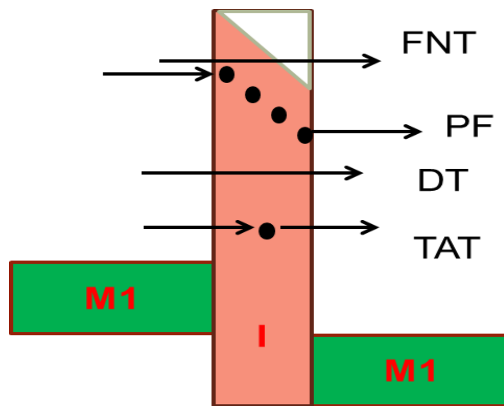


Figure 2 Various tunneling models in a MIM device

2.3.1 Direct Tunneling

Direct Tunneling is the most common type of tunneling across a dielectric film, especially if the dielectric thickness is the order of just a few nano-meters. Direct Tunneling is also referred to as the Trapezoidal based barrier tunneling, this is because the electrons pass through the entire thickness of the dielectric, which is like a rectangle but with the top of it tapered in order to form a trapezoidal structure. The electrons do not possess higher order of energies; hence tunnel through the rectangular region of the trapezoidal structure rather than the tip / triangular structure of the trapezoidal barrier.

It is observed that for the case of Direct Tunneling equation, current through the barrier is proportional to the voltage applied across the barrier. The Direct Tunneling is valid when the potential applied across the insulator is lower than the barrier height of the junction. It also requires the dielectric to be very thin, less than 2 nm. Direct tunneling can be observed by a logarithmic growth on a plot of ln (I/V^2) vs. ($1/V$) or ln (J/E^2) vs. ($1/E$) in the lower regions of the applied bias. The Direct Tunneling is given by the following set of equations 4, 5, 6 [10]:

$$I = V\, exp^{\frac{-4\pi d\sqrt{2m\phi}}{h}} \qquad (4)$$

$$\ln\frac{I}{V^2} = \ln\left(\frac{I}{V}\right)\frac{-4\pi d\sqrt{2m\phi}}{h} \qquad (5)$$

$$J = AE_{ox}^{2}\exp\left(\frac{-B\left(1-(1-\frac{V_{ox}}{\phi_b})^{3/2}\right)}{E_{ox}}\right) \quad (6)$$

where ϕ is the barrier height, h is Planks constant, V is the applied bias across the junction, I is the current measured, A and B are pre-defined Richardson constants and m* is the effective electron mass within the dielectric layer. Direct Tunneling and Fowler-Nordheim Tunneling are generally observed from a similar plot, but at different regions of the applied voltage (or electric field) bias.

2.3.2 Fowler-Nordheim Tunneling

Fowler-Nordheim Tunneling or FN Tunneling as it is commonly known as occurs when the bias applied across the junction is greater than the barrier height of the junction. Due to this, the Fermi level on the bias applied side is pushed so up high that the barrier seen by the electrons now transforms from a trapezoidal shaped barrier to a triangular shaped barrier. Thus, the electrons need to travel a lesser net distance through the barrier before reaching the conduction band of the metal on the other side of the barrier. Electron goes through the part of the dielectric wall through a quantum mechanical process. No energy is lost in this tunneling process FN Tunneling is independent of the temperature influence. A higher bias needs to be applied across the junction in order to create a barrier shape change; this is achieved by having a higher bias, leading to the requirement of a higher electric field in the regions of 8 MV/cm. Current density for FN Tunneling is given by equation 7 [11],

$$J_{FN} = \frac{q^2}{8\pi h \phi_s} E_{Al2O3}^2 \exp[-\frac{8\pi\sqrt{2m^* q}}{3hE_{Al2O3}} \phi_B^{3/2})] \quad (7)$$

where m^* is the effective mass of the tunneling electron in the dielectric, ϕ_B is the barrier height at the junction, E is the applied electric field across the junction. As mentioned earlier, FN Tunneling graph is plotted with ln (I/E_{ox}^2) vs ($1/E_{ox}$) and / or ln (J/E_{ox}^2) vs ($1/E_{ox}$) and /or ln(I/V^2) vs ($1/V$). A linear region on the ln (J/E_{ox}^2) vs ($1/E_{ox}$) plot represents a FN Tunneling dominant region [10]. For the case of FN Tunneling, the current is proportional to the square of the applied voltage across the junction. It can be seen from the equations 8, 9, 10 [11]; that the current depends on the thickness of the dielectric - d, the effective mass of the electron – m* and the barrier height – ϕ.

$$I = V^2 \; exp^{\frac{-8\pi d\sqrt{2m\phi^3}}{3hqV}} \quad (8)$$

$$\ln(\frac{I}{V^2}) = \frac{-1}{V}(\frac{-8\pi d\sqrt{2m\ \phi^3}}{3hq}) \quad (9)$$

FN Tunneling can also be represented by equations 10, 11 and 12, which are as follows [11]:

$$J = A{E_{ox}}^2 \; exp^{\frac{-B}{E_{ox}}} \quad (10)$$

where the two constants A and B are given by:

$$A = \frac{q^3}{8 \pi h m \phi} \qquad (11)$$

$$B = \frac{4 \sqrt{2 m \phi^3}}{3 q h} \qquad (12)$$

where h is the Plank's constant, h bar is the reduced Plank's constant and other variables are similar to as described for other FN Tunneling equations [11]. Under strong FN Tunneling regime, one can use the above equations to solve for the barrier height and the effective mass of the electron in the dielectric.

$$\alpha = 1.54 \times 10^{-6}/m^* \Phi_B \qquad (13)$$

$$\beta = 6.83 \times 10^7 (m^*)^{1/2} (\Phi_B)^{3/2} \qquad (14)$$

In equations 13, 14 α – represents the intercept point on the ln (J/ E_{ox}^2) vs (1/ E_{ox}) and β represents the slope of the linear region on the same curve [12].

2.3.3 Poole – Frenkle (PF) Emission

In Poole – Frenkle emission, a slight fluctuation of thermal energy or rise in temperature, causes a thermal emission of the electron to occur from the columbic trap levels in the metal electrode into the conduction or the valence band of the dielectric. This happens due to slight fluctuations of the net temperature and the small electric field, which provides part of the energy for electron to push through into the barrier. The electric field increases the probability of the electron to tunnel through by decreasing the barrier height on one side of the trap potential well. The traps in the dielectric are

considered as positively charged by default due to the absence of an electron. This positive charge attracts the negatively charged electrons towards through columbic force of attraction and the applied electric field. The tunnel current due to the Poole – Frenkle emission mechanism is given by equation 15 [12]:

$$J_{PF} \propto E_{Al2O3} \exp[-\frac{q}{kT}(\phi_t - \sqrt{qE_{Al2O3} / \pi\varepsilon_0\varepsilon_{Al2O3}})] \quad (15)$$

where E is the electric field across the barrier, T is the temperature, ϕ is the barrier height, ε_0 is the free space permittivity and ε is the permittivity of the dielectric material. The linear region on the plot of ln (I / E_{AlOx}) vs $(E_{AlOx})^{1/2}$ gives the region of a dominating Poole – Frenkle emission. The slope of the plot can be used in determining the relative permittivity constant of the dielectric layer. The slope for the Poole - Frenkle plot is given by the equation 16 [12]:

$$PF_{Slope} = \frac{q}{kT}\sqrt{qE_{AlGaN} / \pi\varepsilon_0\varepsilon_{AlGaN}} \quad (16)$$

2.3.4 Trap Assisted Tunneling (TAT)

Trap Assisted Tunneling or TAT is a two-step tunneling process, similar to the tunneling process of the Poole-Frenkle (PF) tunneling. Trap Assisted Tunneling also occurs through the entire width of the dielectric layer but in a two-step process. In the first step, the electron from the metal junction side tunnels into the traps / defects inside the dielectric layer when a positive bias is applied across it. The electron then tunnels from the trap location into the conduction band of the 2nd metal electrode, thereby leaving the trap site empty. Trap assisted tunneling was initially referred to as the Stress

Induced Leakage current; this is because the stress applied on the dielectric causes the tunneling to happen.

The Trap Assisted Tunneling current obtained across the barrier is found to be proportional to m* - the effective mass of the electron in the dielectric, ϕ - the trap state energy (or the barrier height), and inversely proportional to the electric field across the junction, equation 17 provides the relationship [12].

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm_{Al2O3}}}{3hE_{Al2O3}}\phi_t^{3/2}\right) \tag{17}$$

The linear region in the plot of ln (I) vs (1/ E_{ox}) indicates the region of dominant Trap Assisted Tunneling (TAT). Trap assisted tunneling are very common in dielectrics of poor or bad quality. This is because this dielectric has pin holes or defects in them, which act as a valuable site for the electrons to be attracted to get trapped in them.

These are some of the important electron tunneling observed in Metal-Insulator-Metal capacitors with thinner dielectric in the range of less than 2 nm. To summaries, Direct Tunneling is independent of the temperature but requires electric field in order of just few MV/cm and voltage bias less than the barrier height. FN Tunneling requires high electric field, greater than atleast 10 MV/cm and applied bias greater than the barrier height of the junction. Poole-Frenkle (PF) emission is a temperature dependent process, it requires temperature fluctuations with low orders of electric field of tunnel the electron through the barrier in a two-step process. The last tunneling discussed is the TAT, which is also a two-step process and requires electric field in the orders of 5 – 7 MV/cm.

2.4 Josephson Junctions

A Metal-Insulator-Metal device when fabricated using superconductor materials as the electrode rather than normal metal, are referred to as a Josephson Junctions. A very thin dielectric / insulator is used to sandwich the two superconducting electrodes. Josephson Junctions are also referred to as Superconductor-Insulator-Superconductor (SIS) devices. When the devices are placed at temperature less than the critical temperature of the electrode used, there is a probability of tunneling to occur across the dielectric barrier. The tunneling depends on the thickness of the dielectric, if the dielectric is thin enough, the two wave functions of the two superconductors can overlap in the dielectric, leading to transfer of electrons between the two terminals in the form of copper pairs (pair of electrons tunneling together). Figure 3 shows a schematic of a junction with Cooper pairs tunneling across barrier [13].

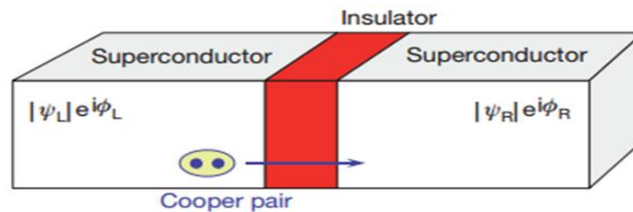


Figure 3 Cooper pair tunneling across a Josephson Junctions, figure taken from [13]

Kamerlingh Onnes in 1911 observed the realtionship between the electical resistance of some metals decreased to zero as the metal was cooled down to absolute zero temperature (0 K). This temperature at which a metal loses all of its electrical

resistance is refered to as the Critical Temperature (T_C). At this cricitcal temperature, a metal goes from its normal state of exihibiting electrical resistance to a superconducting state of zero electical resistance. Metals below its cricital temperature behave as a superconductor; a perfect conductor, thus there is no loss in current or magnetic field produced by the current in the superconductor itself.

Metals above the crictical temperature have a net repulsive interaction between two electrons, whereas below the cricitcal temperature, the overall interaction between two electrons becomes slightly attractive due to the iteraction of the electron – phonon coupling. At temperatures below critical temperature, an electron can attract the positive ions in a superconducting materials towards itself, thereby creating a postive charge localization. As a result, another electron is drawn to this region, in order to balance the net positive charge. The slight attraction between two eletrons causes the creation of a Copper pair under certain spin and momentum configurations. Due to this very slight attraction force between the two electrons, these electrons are now able to drop into a lower energy state, energy loweer than the fermi energy, thus creating an energy gap in the system. Due to existance of a Copper pair with lower energy and an energy gap, Copper pairs can move along the structure, thereby having a net flow of electric current without any dissiaption or loss in the overall current.

2.4.1 Josephson Equations

Brian D. Josephson established the two basic equations that describe the Josephson Effect, in his paper in 1962. The first equation provides a relationship between the voltage V (t) at time t across the junction and to that of the phase difference

φ (t) between the two superconductor electrodes [14]. This equation is referred to as the superconducting phase evolution equation. ($\hbar / 2e$) is referred to as $\varphi_{0,}$ the magnetic flux quantum.

$$V(t) = \frac{\hbar}{2e} \frac{\partial \phi(t)}{\partial t} \qquad (18)$$

The second Josephson equation provides a relationship between the maximum possible Josephson supercurrent I_s (t) at any time to the phase difference φ (t) between the two electrodes at any time (t) [14]. I_c is the maximum possible current through the junction at any time and is referred to as the critical current of the Josephson Junctions. This current is time independent and is affected by fluctuations in the temperature. Φ (t) is given by the difference of the two φ_1 (t) and φ_2 (t) obtained from the 2 electrodes, known as the phase difference.

$$I_s(t) = I_c \sin(\phi(t)) \qquad (19)$$

Under an external biased current, Josephson Junctions will carry this applied current as the supercurrent, without any voltage drop, to the max possible value of the critical current. Once it reaches the max possible current value, the junction will now switch over to a resistive network by producing single electrons, thereby giving rise to voltage drop across the junction.

Current across the junction at a critical temperature is generated due to tunneling of electron pairs know as Cooper Pairs across the junction. Cooper pairs at critical temperature move to a lower energy state, thereby creating a superconducting band gap.

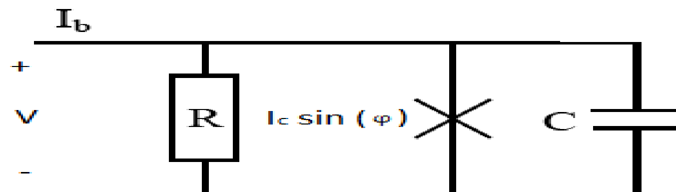
For Cooper pairs to be separated, a bias equal to the binding energy of ~ 1 mV needs to be applied across the junction.

The relationship between the critical current I_c and the temperature is given by the Ambegakor-Baratoff equation [15]. R_n is referred to as the tunnel resistance of the junction at normal state; Δ (T) is the energy gap in the material. As R_n is inversely proportional to the area of the junction, smaller area junctions have a lower critical current value [14].

$$I_c = \frac{\pi \Delta (T)}{2\, e\, R_n} \tanh\left(\frac{\Delta (T)}{2\, k\, T}\right) \tag{20}$$

2.4.2 Josephson Junctions equivalent circuit

Similar to the equaivalent circuit model of a MIM diode, the Josephson Junction also have a equvialent ciruict model. The simple equivalent electrical cirucit model for a Josephson Junction is called the 'Resistively and Capaitively Shunted Junction Mode' or RCSJ [16, 17]. Figure 4 shows the schematic of the equivalent Josephson Junction circuit.



Firgure 4 Equivalent model of a Josephson Junction

It consists of the junction, which is like a non-linear inducatnace, paraller capacitor and resistor. The resistance of the resistor will be close to the normal resistance R_n at crictical temperature. Josepshon Junctions are by default considered as parallel plate capacitors with capcitance C. Therfore, the total current in the equivalent model can be given as follows:

$$I_b = I_s + I_d + I_n \quad (21)$$

$$I_b = I_c \sin(\varphi) + C\,(dV / dt) + (V/R) \quad (22)$$

2.4.3 Application

Josephson junctions or SIS (superconductor – insulator – superconductor) are extrememly small and sensitive devices. They have a were small junctions overlap, thereby having extremely small capacitances in the order of few femto Farads. It is due to this reasons that Josephson junctions find themselves as the best suitable candidates for the construction of quantum bits (qubits) and superonducting quantum interference deviec (SQUID) for application in the core of a quantum computer. One of the very first application of Josephson jucntions was in the defination of the term 'volt'.

Currently, one of the most important application of a Josephson junction device is as a Superconductive QUantum Interference Device or (SQUID). A SQUID is a closed circuit loop consiststing of a pair of parrallel Josephson junctions, which is very senstitive to the total amount of magnetic field that can penetrate the closed loop area. As a result, it can be used to measure the activity of the brain and heart by measuring theirvery low orders of magnetic field. SQUIDs can measure magnetic fields on the

order of 5 x 10^{-11} G/Hz $^{-1/2}$ [18]. As a SQUID consists of 2 Josephson junctions, it is represented by 2 X's placed in a closed loop pattern as shown in figure 5 [19].

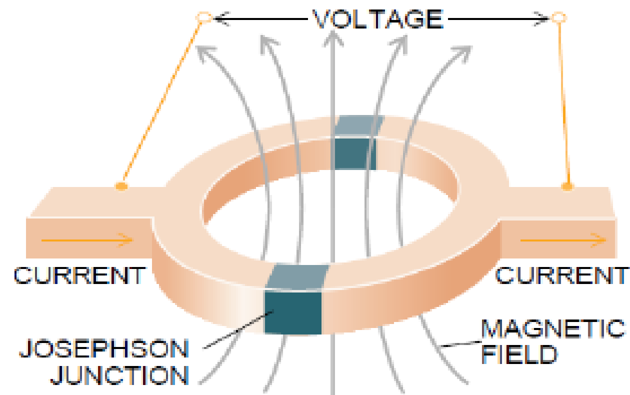


Figure 5 A schematic representation of a SQUID, figure taken from [19]

Current research on Josephson junctions is being done with the focus towards the field of quantum computing. The flux qubit (a special type of quantum bit), consisting of small loops of superconductors (SQUIDs) separated by a number of Josephson junctions.

3. FABRICATION OF JOSEPHSON JUNCTIONS (MIM CAPACITORS)

3.1 Literature survey of Josephson Junctions fabrication process

This section of the thesis summarizes the challenges and approach towards the fabrication of the Josephson Junctions or thin film MIM (Metal-Insulator-Metal) capacitors that were used in this research. Josephson Junctions are fabricated by using by sandwiching two superconducting thin film metals (Aluminum or Niobium) with a thin insulator (Aluminum Oxide (Al_2O_3) generally less than 2 nm in thickness) or a non-superconducting metal (of thickness generally greater than 1 μm) [20].

From literature, it was found that most of Josephson junction fabricated to date, consists of Aluminum (Al) or Niobium (Nb) as the superconducting metal electrodes. Bulk Aluminum (Al) has a critical temperature, $T_c = 1.2$ K and bulk Niobium (Nb) has a critical temperature, $T_c = 9.3$ K. The structure for the most common Josephson Junctions is as follows: Aluminum (Al) / Aluminum Oxide (Al_2O_3) / Aluminum (Al) and Niobium (Nb) / Aluminum Oxide (Al_2O_3) – Aluminum (Al) / Niobium. Junctions that are fabricated using Niobium (Nb) as the superconducting require a very thin layer of Aluminum (Al) to be deposited on it, in order to support growth and deposition of the Aluminum Oxide (Al_2O_3) insulator layer. In literature, the Aluminum Oxide (Al_2O_3) insulator layer is grown using thermal oxidation of Aluminum (Al) thin film in air or Oxygen ambience. As a result, the Niobium (Nb) based Josephson Junctions require a thin Aluminum (Al) layer to act as the source for the growth or as the wetting layer for the deposition / growth of Aluminum Oxide (Al_2O_3) [20]. Niobium based Josephson

Junctions are easier to test when compared to the Aluminum (Al) based Josephson Junctions due to their higher critical temperature (T_C). At atmospheric pressure, the boiling temperature of Nitrogen (N_2) is 77.3 K, Helium 4 is 4.21 K and that of Helium 3 is 3.2 K [21]. As Helium 3 is much cheaper than Helium 4, it is easier to test Niobium based Josephson Junctions than the Aluminum (Al) based Josephson Junctions. However, it has be found that the critical temperature and superconducting property of Niobium are adversely affected, if the Oxygen (O_2) content in the Niobium (Nb) thin film is increased [22].

Another important finding from the literature survey was that the most common insulator layer used in the Josephson Junctions fabrication was Aluminum Oxide (Al_2O_3). Aluminum Oxide (Al_2O_3) was found to be grown / deposited only by using the thermal oxidation of Aluminum in air or in Oxygen (O_2). Since, the required thickness of the Aluminum Oxide (Al_2O_3) is just in the range of 2 nm, it is quite necessary to have very conformal, controlled and high quality of oxide growth. The thermal oxidation of Aluminum (Al) in order to grow Aluminum Oxide (Al_2O_3) is a hit-miss kind-off approach when thickness of the oxide is the major concern. Secondly, it becomes very difficult to have very conformal film at such lower thickness. Since, conformity of the insulator film is of huge importance for the performance of the device, it was decide to approach with another technique, Atomic Layer Deposition (ALD), to deposit the Aluminum Oxide (Al_2O_3) insulator thin film as the insulator film for the junction devices used in this research work. The importance and advantages of the using Atomic Layer Deposited Aluminum Oxide (Al_2O_3) will be discussed in later in this section.

After considering the above mentioned strength and concerns of the two most common Josephson Junctions, it was decided to base this research work on Aluminum (Al) based Josephson Junctions. The device structure for the Josephson Junctions used in this research work is as follows: Aluminum (Al) / Atomic Layer Deposited (ALD) - Aluminum Oxide (Al_2O_3) / Aluminum (Al).

3.2 Fabrication of Al / ALD - Al_2O_3 / Al based Josephson Junctions

This sub-section of the thesis explores the various process steps carried out during the fabrication of Aluminum (Al) / Atomic Layer Deposited (ALD) - Aluminum Oxide (Al_2O_3) / Aluminum (Al) Josephson Junctions. It was found from literature that the most common approach towards the fabrication of Josephson Junctions either used a photolithography based Dolan Bridge technique or Electron Beam Lithography. All the previous literature work was considered in order to decide the process flow for the devices fabricated in this research.

3.2.1 Patterning technique – Dolan Bridge, Electron Beam Lithography, Step – Edge

The most common patterning technique found from literature review was based on patterning through Photolithography or Electron Beam Lithography (EBL) using the Dolan Bridge technique. Step–edge based patterning technique was the other common patterning method in the earlier days of Josephson Junctions fabrication. The Dolan Bridge technique is based on the phenomenon of using a shadow mask or a mask generated after a photolithography step and then using two different angles of thin film deposition to control the overlap area.

The basic phenomenon that is observed in the fabrication of a MIM device acting

as a Josephson Junctions through the Dolan Bridge / shadow mask technique is shown in figure 6 below. The Dolan Bridge patterning process takes place in the following manner. The substrate (Silicon wafer) undergoes the standard clean process and is dehydrated. Next, a photoresist of desired thickness is deposited on the wafer and soft baked. The mask pattern is transferred on the photoresist by using a mask aligner with the required energy time product for the photomask. The mask pattern is developed and hard baked so to make the hanging bridge resist structure more stable. The sample is now placed inside a regular Physical Vapor Deposition (PVD) to deposit the thin film of the required superconducting material like Aluminum (Al) or Niobium (Nb). The important thing to note is that either of the source / target or the substrate needs to be placed on a rotating setup [23]. Either of the source metal or the substrate stage needs to be having the ability to be rotated by few degrees of angle. Let us assume, the first metal layer is deposited by rotating the source to an angle of θ (theta) to the right of the perpendicular line of the substrate. The deposited metal is then thermal oxidized to obtain the required amount of insulator thickness. Once the requires oxide / insulator layer is grown, the sample is placed back in to the Physical Vapor Deposition (PVD) system with the same orientation, but the metal source this time is rotated to the left with a new angle theta-1 (θ_1) [23]. The overlap area of the Josephson Junctions is determined by the angles at which the source is rotated during the two deposition steps. Greater the difference between the two angles, smaller is overlap area of the junction.

The photolithography based Dolan Bridge / shadow mask technique when carried out effectively can provide an area overlap in the region of sub nanometer squares.

However, the yield in this process is towards the lower end as it is a bit difficult to control the angle of the source during deposition to the fine control.

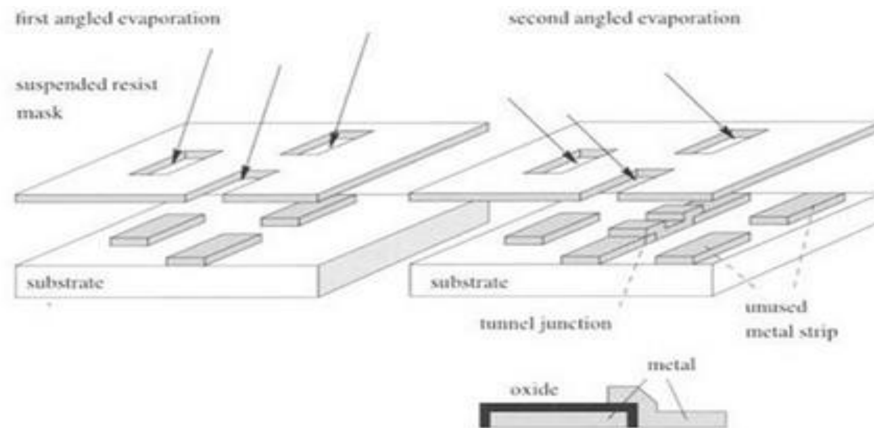


Figure 6 Schemicatic representing Dolan Bridge fabrication technique, figure taken from [23]

The same Dolan Bridge approach can be used with the Electron Beam Lithography (EBL) system. In order to use the Dolan Bridge technique with Electron Beam Lithography (EBL) system, it uses a two resist procedure instead of just one resist based photolithography. The two common resists used in this process are Poly methyl methacrylate (PMMA) and Methyl methacrylate (MMA) and differ from each other in term of their thickness and resist density [24]. Using a very confined electron beam setup, the undercut in the process can be controlled to very fine margin and junctions of the order to 40 nm * 40 nm can be easily fabricated [24]. Once the Electron Beam lithography step is completed, the same procedure of angled Physical Vapor Deposition

(PVD) as mentioned earlier in this section is used in the junction deposition. The only issue with the fabrication of Josephson Junctions with Electron Beam based lithography is the low yield and large time required for transferring patterns. However, for the point of research, this is a good approach. Figure 7 shows the Dolan Bridge fabrication using the Electron Beam lithography system. The same method used in photolithography can be used in fabricating devices using EBL but requires two resist technique [24].

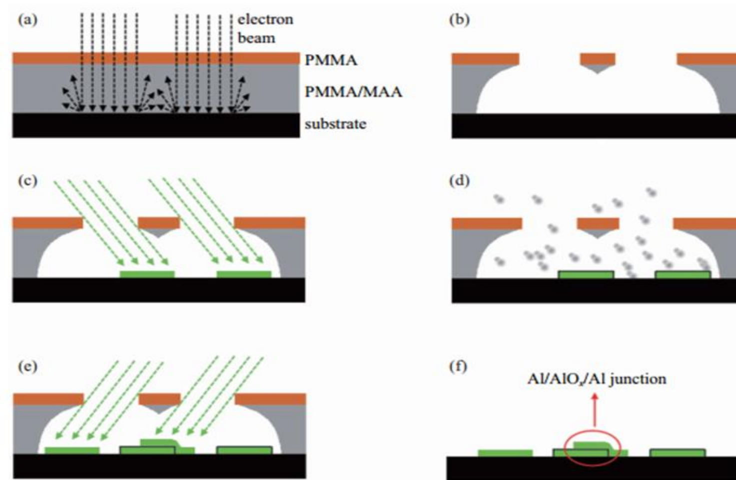


Figure 7 Dolan brdige fabrication for E Beam lithography, figure taken from [24]

The final method in the approach towards fabrication of Josephson Junctions is using a Step-Edge fabrication technique. In this method, the junction area is defined by the thickness of the superconducting film rather than the width or the length of the deposited film. The junction is formed on the outer edge of the superconducting film rather than being formed an overlap structure. In this process, the junction is formed

vertically rather than horizontally. It was found from the literature survey that the initial Josephson Junctions were fabricated using this process as it was reliable and much easier to form, however due to its in-ability to form junctions with smaller area overlap, this fabrication technique was soon replaced with the onset of the Dolan Bridge technique. The Step-Edge Josephson Junctions also use the same intermediate step of thin film metal deposition as described earlier in the Dolan Bridge approach.

However, in this research work, the Step-Edge technique was used in order to fabricate Josephson Junctions with an area overlap of less the 1 μm^2 using standard contact photolithography technique. The entire process for the fabrication of Step-Edge Aluminum (Al) / Atomic Layer Deposited (ALD)-Aluminum Oxide (Al_2O_3) / Aluminum (Al) Josephson Junctions (MIM) will be described in detail in rest of this section.

3.2.2 Initial Josephson Junctions device structure

The initial structure of the Josephson Junctions fabricated in this research consists of a multiple layer of thin film metal and insulators. The first step in the fabrication of the Josephson Junctions is cleaning of the Silicon (Si) wafers. A 2" Silicon (Si) single side polished un-doped wafer is used in this fabrication. The wafer under goes a 10 min 7:1 - DI water: Hydrofluoric Acid, Buffer oxide etches (BOE) in order to remove any organic and native Silicon dioxide (SiO_2). It is next cleaned by sonicating for 10 min each in Acetone / Isopropyl alcohol (IPA) / DI water (di-ionized water). The wafer is the dehydrated in an oven at 135 °C for 5 min.

A thick layer of 500 nm of SiO_2 is next deposited through Plasma Enhanced Chemical Vapor Deposition (PECVD). An Oxford Plasmlab 80 PECVD system is used

for the deposition of the insulator buffer layer. The deposition conditions for the oxide are as follows:

Table Temperature: 350 °C   Chamber Pressure: 1 mTorr

Gases: 355 sccm N_2O , 425 sccm 1% SiH_4 in N_2

⇨ which gives a ratio of N_2O / SiH_4 = 83.05

Deposition Rate = 50 nm/min   Measured Refractive Index = 1.4554

The refractive index of the deposited SiO_2 is measured to be 1.4554 which is similar to the refractive index of the best quality of thermally grown SiO_2. It is of utmost importance to have the buffer dielectric SiO_2 layer of the best quality in order to prevent interlayer diffusion between subsequently deposited thin films. Figure 8 shows the graph of an Ocean Optics spectroscopy scan indicating the measured refractive index for a thin film of ~ 250 nm.

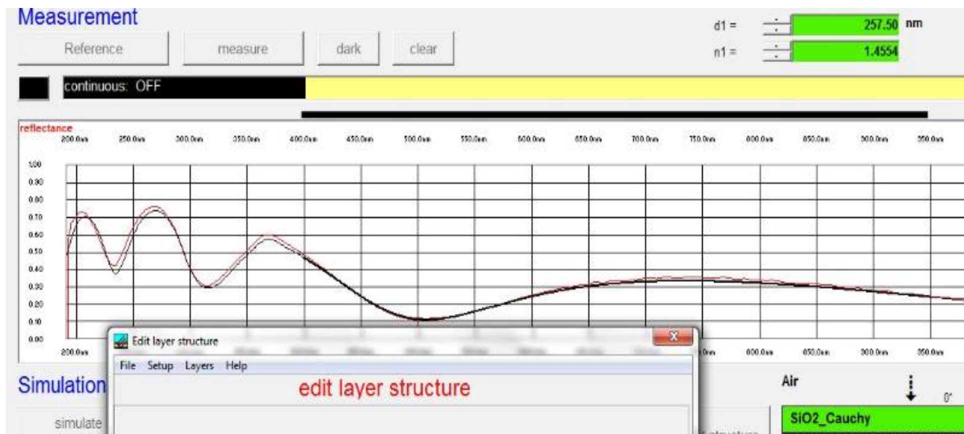


Figure 8 Ocean Optics scan of PECVD deposited SiO_2

The sample is now paced inside a Kurt J Lesker PVD 75 Electron Beam Evaporator in order to deposit the thin metal film that will work as the bottom superconducting layer. The Kurt J Lesker PVD 75 Electron Beam Evaporator consists of a 2 step vacuum system consists of a roughing pump connected to a turbo pump using a backing valve. A Tungsten coil is heated up by passing current to it, which produces a beam of electrons. The electron beams is then molded and shaped by using electro-magnets in order to make the beam strike the crucible containing the source material. The required deposition rate for each material can be obtained by altering the power of the electron beam gun. The system is first pumped down to a base pressure of 5 μTorr (5E-6 Torr). A very thin layer (~ 3 nm) of Chromium (Cr) is deposited in order to act as a diffusion barrier between the superconducting layer and the buffer insulator deposited on the 2" Silicon wafer. The next layer deposited is the superconducting Aluminum layer of 150 nm in thickness. This layer is going to act as the bottom electrode of the Step-Edge Josephson Junctions fabricated in this research work. Another Chromium (Cr) layer of 20 nm is deposited on the Aluminum (Al) layer. Aluminum (Al) forms a native oxide when exposed to the moisture in the air. In order to avoid this native oxide formation, the 20 nm Chromium (Cr) layer acts as a cap layer to the bottom Aluminum (Al) electrode. After the deposition of the 3 metal layers, the sample is removed from the PVD 75 Electron Beam Evaporator and placed back into the Plasma Enhanced Chemical Vapor Deposition (PECVD) system in order to deposit a thick 500 nm insulator layer of SiO_2. This insulator layer will help us in creating the step edge junction and at the same time help in decreasing the overall parasitic component of the junction device. This SiO_2

insulator layer is also deposited using the same Plasma Enhanced Chemical Vapor Deposition (PECVD) recipe discussed earlier in this same sub section.

A final layer of 75 nm Chromium (Cr) thin film is deposited using the Kurt J Lesker PVD Electron Beam Evaporator. This Chromium (Cr) layer will be used as a Hard Mask layer during rest of the fabrication process. This Chromium (Cr) layer will help used in defining and preserving the mesa throughout the fabrication process. The final structure at this point after the deposition of the above mentioned multiple layers is as shown in figure 9.

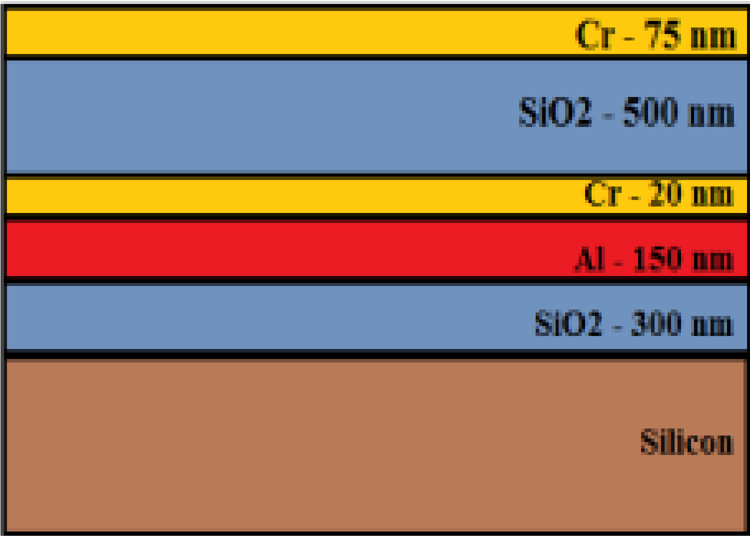


Figure 9 Complete structure of the bottom electrode

3.2.3 Mesa fabrication and etch profiling of bottom Aluminum (Al) electrode

The next step in the fabrication process of Aluminum (Al) based Josephson Junctions is the patterning of the bottom electrode. A mesa mask is patterned on to the

multilayer thin film structure shown in the above figure 09. Mask 1 is a light field mask and consists of rectangular mesa patters of various areas ranging from 110 µm x 110 µm 135 µm * 110 µm. The mesa mask used in the process can be seen in figure 10.

After the required mask has been selected, the photolithography step is next carried out using a Karl Suss MA 6 Contact Mask Aligner. An adhesive Hexamethyldisilazane (HDMS) and a positive photoresist AZ 5214 is used in this lithography process. The current structure consisting of the multilayered thin films is degreased by performing a 5 min sonication with each Acetone / Isopropyl alcohol (IPA) / Di-ionized water and then dehydrated in an oven at 135 °C for 5 mins.

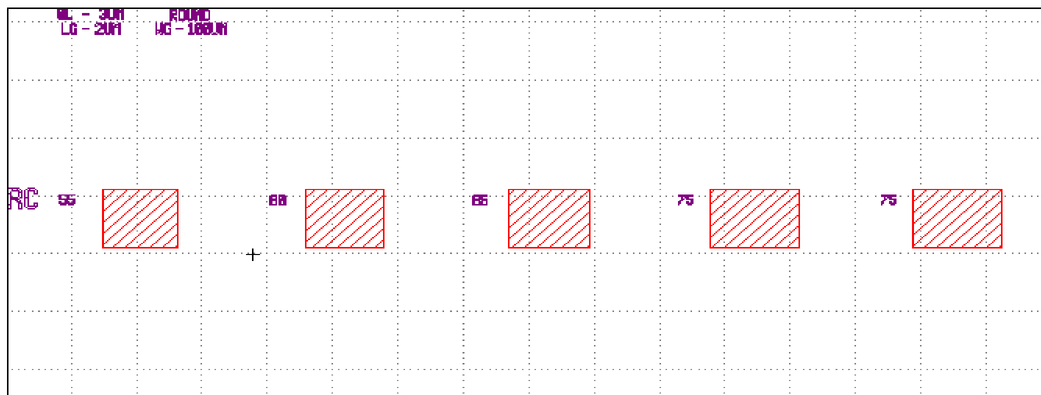


Figure 10 Mask pattern used in lithography step 1

A bake plate is turned on and set to 120 °C. Next using a dropper the Hexamethyldisilazane (HDMS) solution is poured on the Silicon wafer after it being placed on the chuck of photoresists spin coater. The spin coater is now set and ran to 4000 RPM for 40 sec. After the completion of the run, the AZ 5214 positive photoresists

is now poured on the wafer using another dropper. The wafer is again spun at 4000 rpm for 40 sec, which gives a conformal photoresist film of approximately 1.5 µm. After the completion of the spin run, the wafer is now placed on the 120 °C bake plate for 2 min. This step is known as the soft bake step, it slight hardens the photoresist, making it easier for mask patterns to not lose their structure / shape till the hard bake step. After the wafer has been soft baked, the wafer is now placed on the chuck of the Karl Suss MA 6 Mask aligner for UV light exposure to transfer the mask pattern on to the wafer. The mask used in this research work are of 100 mJ of energy, hence with an average exposure of 8 mJ/sec, the wafer and mask under contact were exposed for ~ 12 sec. The wafer after exposure is developed using an AZ 1:1 developer for 40 secs. The wafer is dried using N_2 gun and then seen under a microscope to see if the patterns came out to be as required.

Once the desired patterns have been transferred to the photoresist on the wafer, the wafer is than hard baked for 5 min in a 135 °C oven. The hard photoresist, will not act as the mask, and help in transferring the patters to the Chromium layer below it. The wafer is placed into a Chromium etchant for ~ 1 min. The lithography patterns have now been transferred to the top 75 nm Chromium (Cr) layer which will be used as a hard mask for rest of the process and for defining the structure of the Josephson Junctions. The hardened photoresist is now washed away by sonicating for 2-3 min with acetone.

3.2.4 Etch profiling by Reactive Ion Etching (RIE)

The initial etch profiling was carried by using by using a collaboration of three wet etch steps. This included etching the top thick SiO_2 using a 7:1 Buffer oxide etch at

an etch rate of 200 nm/min, followed by a quick dip in Chromium etchant with an etch rate of 100 nm/min. The next wet etch step is done using an Aluminum etchant to etch the bottom electrode to the required size. Aluminum etchant has an etch rate of about 50 nm/min. The last wet etch is done using the same 7:1 Buffer oxide etch in order to make a suitable edge profile. However, as wet etching is highly isotropic in nature, it was found not to be an ideal way towards the edge profiling of the Josephson Junctions fabricated in this research work. Due to a large isotropic nature of the wet etch profile [25]; it was found that the contact distance between the bottom and top electrode will increase in a significant amount, thereby limiting the current flow between the two superconducting electrodes and increasing the overall resistance in the junction. Figure 11 shows the difference between an isotropic wet etch and anisotropic dry etch profile. The ideal edge-profile for the Edge-Step Josephson Junctions needs to be as anisotropic as possible. This can be achieved by etching the sample using a Reactive Ion Etching (RIE), when performed using perfect gas chemistry.

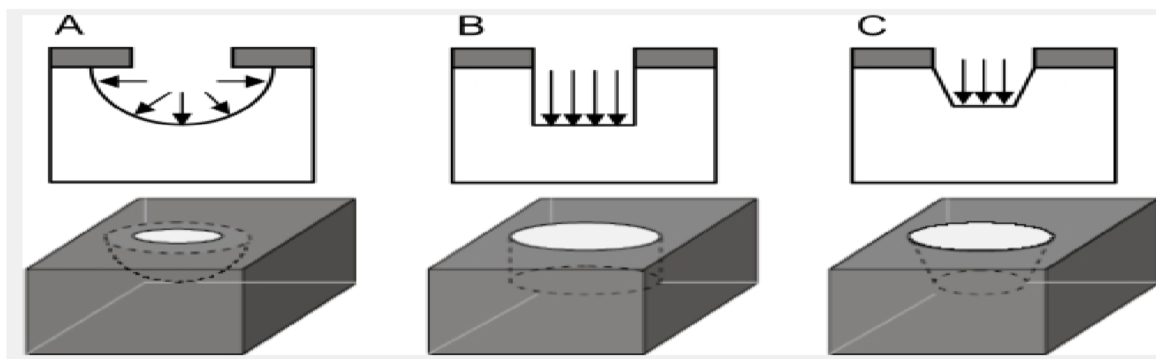


Figure 11 Various types of semiconductor etch profiles, figure taken from [25]

An Oxford Plasmalab 100 ICP etch system is used in this research work in order to carry out the anisotropic etching at the step-edge of each junctions. The system consists of a load lock, with a 2 pump system, a roughing and turbo pump. It is also connected to a liquid Nitrogen dewar which provides cooling to the sample substrate stage, in order to have a very vertical etch profile. It also consists of two types of power sources: Radio Frequency (RF) Power and Inductive Coupled Plasma (ICP) power and gases such as Oxygen (O_2), Trifluoromethane (CHF_3), Sulfur hexafluoride (SF_6), Argon (Ar). The Radio Frequency power is responsible for building / creating the plasma (ion density) in the chamber, whereas the Inductively Coupled Plasma (ICP) power is responsible for directing the formed ions on to the substrate / target wafer.

The first step in the Reactive Ion Etching (RIE) cycle is the etching of the top SiO_2, followed by an etch recipe for etching Chromium (Cr) and Aluminum (Al). The last step in the dry etching run is to carry out the etching of the buffer SiO_2 layer. This is carried out by using a slightly modified SiO_2 etching recipe. This etching step is a very critical in the fabrication process of the Josephson Junctions. The three recipes used in the etching of the 4 thin film layers are as follows:

<u>Etching of top SiO_2:</u> (Vertical etch)

Pressure = 10 mTorr   Process Temperature = 20 °C   Etch Rate: 60 nm/min

Argon (Ar) = 10 sccm   Trifluoromethane (CHF_3) = 25 sccm

RF Power = 100 W   ICP Power = 200 W

<u>Etching of Chromium (Cr) and Aluminum (Al) layers:</u> (Vertical etch)

Pressure = 10 mTorr   Process Temperature = 30 °C   Etch Rate: 20 nm/min

Argon (Ar) = 40 sccm Trifluoromethane (CHF_3) = 10 sccm Oxygen (O_2) = 5 sccm

RF Power = 250 W ICP Power = 150 W

Etching of bottom SiO_2: (more lateral etch required than vertical)

Pressure = 10 mTorr Process Temperature = 20 °C Etch Rate: 60 nm/min

Argon (Ar) = 10 sccm Trifluoromethane (CHF_3) = 25 sccm

RF Power = 100 W ICP Power = 200 W

Figure 12 provides a rough estimation of how the step-edge of the junction gets etched through all the different dry etching recipe stages. At the end of the dry etching step, a quick 30 secs Chromium etch is carried out in order to remove the top Chromium cap layer. Figure 13 provides a SEM picture of the step-edge at the end of the fabrication process of the Josephson Junctions devices.

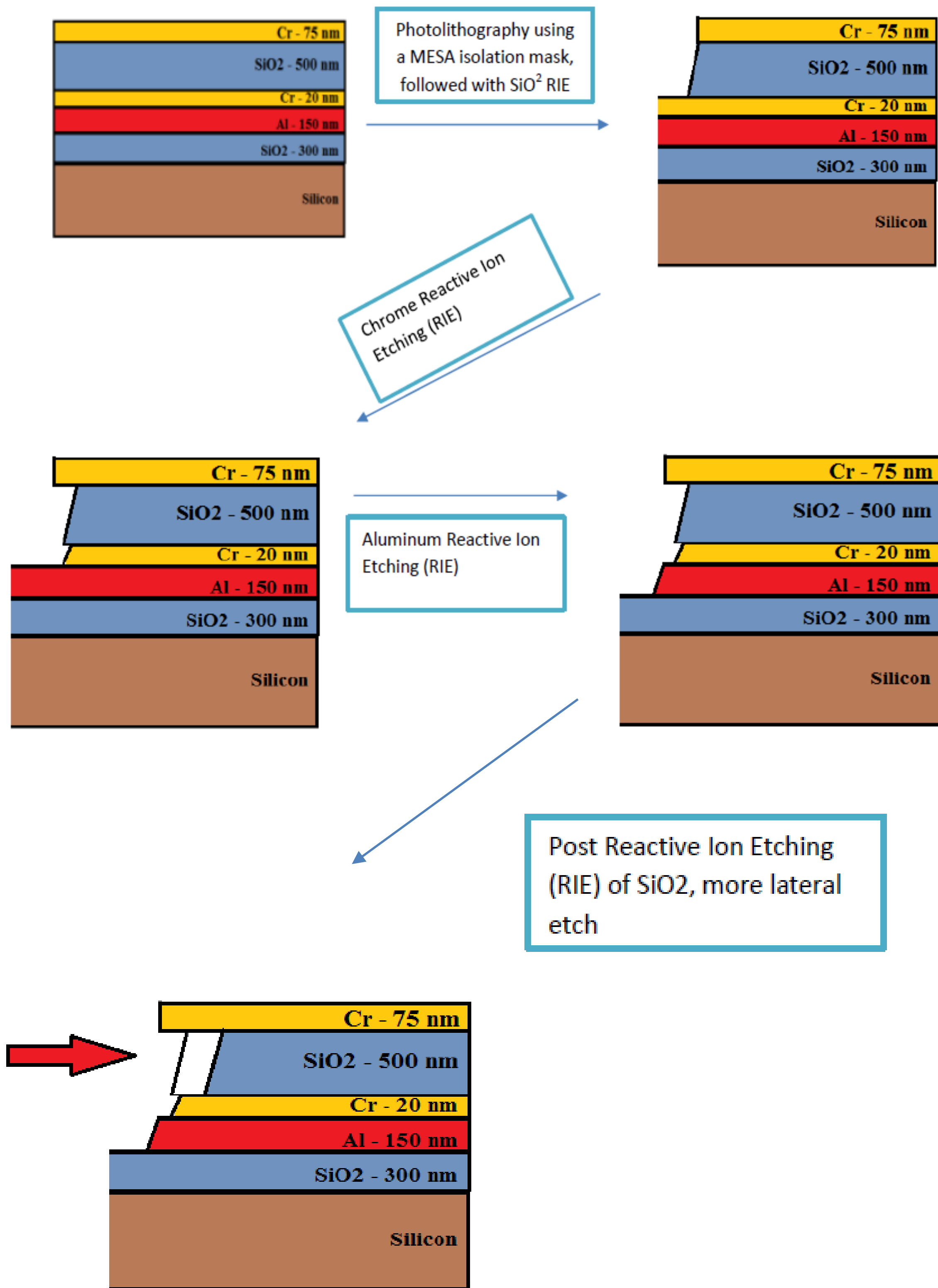


Figure 12 Entire fabrication process for creation of the step edge profile

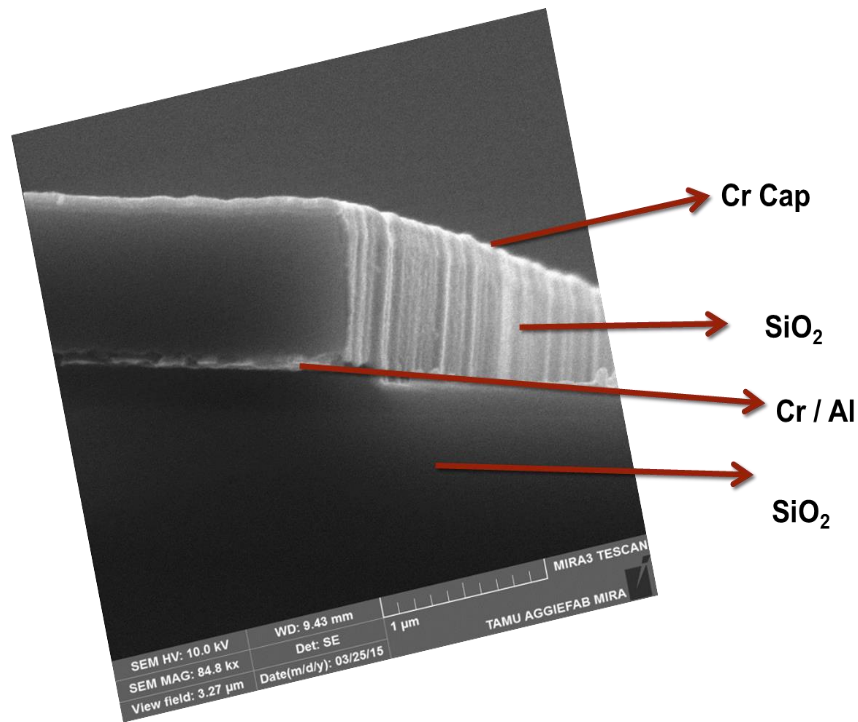


Figure 13 Scanning Electron Micrograph (SEM) indicating the cross section of the step-edge

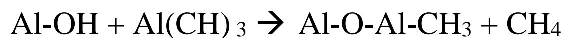
3.2.5 Aluminum Oxide (Al_2O_3) insulator deposition by Atomic Layer Deposition (ALD)

It was found from the literature review that the Aluminum Oxide (Al_2O_3) insulator used in Josephson Junctions is generally grown by thermal oxidation of Aluminum (Al) thin film layer in air or in Oxygen (O_2). The required thickness of the Aluminum Oxide (Al_2O_3) is just in the range of 2 nm, it is becomes quite necessary to have very conformal, controlled and high quality of oxide growth. The thermal oxidation of Aluminum (Al) in order to grow Aluminum Oxide (Al_2O_3) is a hit-miss kind-off approach when the required film thickness is in the extremely low nanometer range. Secondly, it becomes very difficult to have a conformal film at such lower thickness from the thermal oxidation process. As a result, there is a possibility of having low yield

and process variations when the Josephson Junctions are fabricated by a Step-Edge technique.

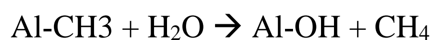
As a result, Aluminum Oxide (Al_2O_3) was deposited by using an Atomic Layer Deposition (ALD) system. The Atomic Layer Deposition (ALD) system is a chemical vapor deposition (CVD) similar to the Plasma Enhanced Chemical Vapor Deposition System (PECVD) used for the deposition of SiO_2. The film is deposited in single monolayer steps, thereby providing the ability to deposit films less than 10 nm in thickness to a very good control and conformity. The Atomic Layer Deposition (ALD) system consists of 2 precursor sources: Trimethylaluminum (TMAl) and Water (H_2O). The entire deposition of Aluminum Oxide (Al_2O_3) is carried out in 5 steps [26, 27]:

1.) In the first step of the cycle, the Water (H_2O) precursor is pulsed into the system. This step is referred to as the conditioning step or the surface wetting step. The OH group in the water attaches to the top layer on the substrate surface, thereby providing the suitable surface of the Aluminum (Al) precursor to attach too in the next cycle. This leads to formation of Al-OH link on the top layer of the surface.
2.) Now the second precursor, Trimethylaluminum (TMAl), is pulsed into the chamber. The following reaction takes places:



$$\text{Al-OH} + \text{Al(CH)}_3 \rightarrow \text{Al-O-Al-CH}_3 + \text{CH}_4$$

3.) Next is a purge cycle to remove all the byproducts created from the above reaction, out of the deposition chamber.
4.) Another, Water (H_2O) cycle is pulsed in order to form the Aluminum Oxide dielectric. The reaction that takes place is as follows:



$$Al\text{-}CH3 + H_2O \rightarrow Al\text{-}OH + CH_4$$

5.) Another purge cycle similar to step 3 is carried out in order to remove the byproducts of the above reaction.

These 5 steps are carried out in a cycle for depositing the required thickness of thin insulator film. The deposition rate per cycle for the system used in this research work was found to be ~ 0.670 Å/cycle. Figure 14 provides a cartoon depicting the deposition of Aluminum Oxide (Al_2O_3) on a Silicon (Si) wafer. Figure 15 a, b, c and d summaries the 4 main step involved in the ALD deposition technique.

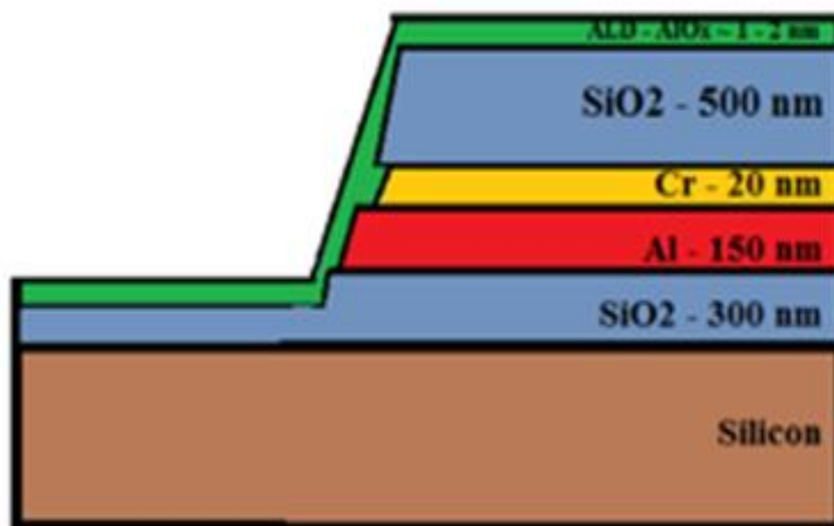


Figure 14 Cross-sectional of the junction after ALD oxide deposition

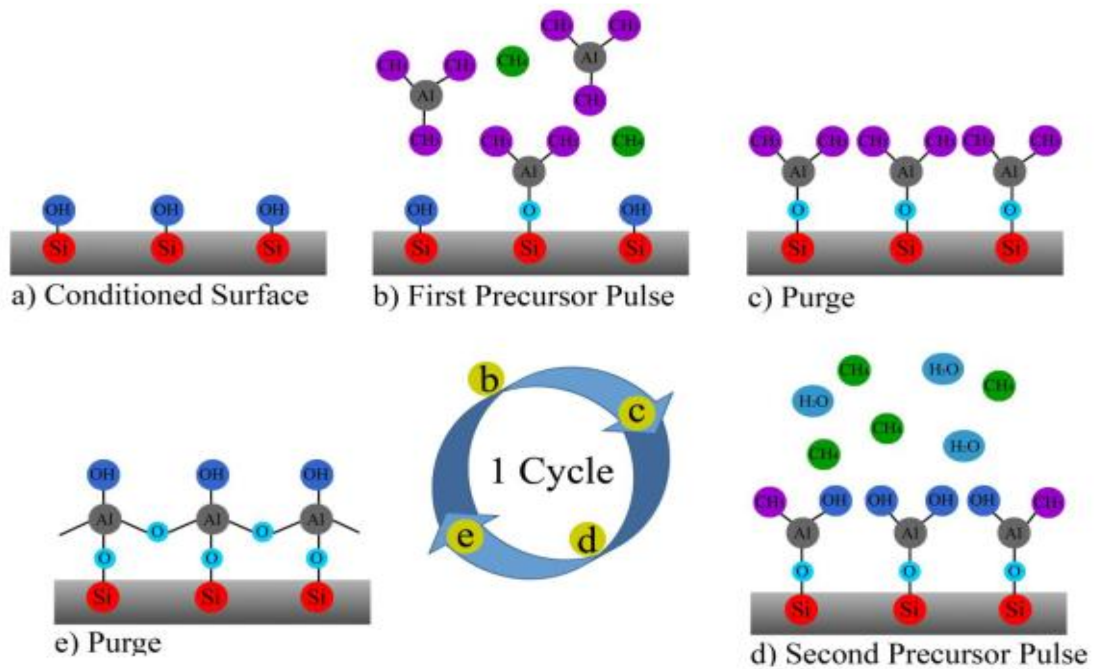


Figure 15 Intermediate steps in the process of ALD Al_2O_3 deposition, figure taken from [26, 27]

3.2.6 Second superconducting metal deposition

Once the required thickness of dielectric / insulator film has been deposited by using the Atomic Layer Deposition (ALD) system, the sample is then placed in to a Kurt J Lesker PVD 75 DC Sputter system. As the sample is no longer a planar, since it has a mesa and edge profile, the 2nd superconducting layer is deposited using the DC Sputter system because it will provide more conformal deposition at the step-edge than the Electron Beam Evaporator. This is because; the atoms produced during the metal deposition using DC sputter system have far more kinetic energy than the ones created by the Electron Beam Evaporator. More kinetic energy is directly related to the ability of the atoms to move in lateral direction and thereby causing a conformal deposition on the

step-edge of the junction, the most important area for the devices fabricated in this research work.

The Kurt J Lesker DC Sputter system also consists of double pump systems, a roughing and a turbo pump. The system is initially pumped down to a base pressure of $5x10^{-6}$ Torr, and then process is carried out a process pressure of $3x10^{-3}$ Torr with DC power as 450 W. The deposition rate for Aluminum (Al) at the above mentioned conditions is 1.82 Å/sec. An Aluminum layer of 150 nm is deposited on top of the sample consisting of the ALD - Aluminum Oxide (Al_2O_3).

3.2.7 Final photolithography step for patterning the top superconducting electrode

In the last step of the fabrication process, a similar photolithography process as discussed in sub section 3.2.3 is carried out. A different mask, shown in figure 16 is used in order to pattern the 2nd (top) superconductor layer. As this is an overlap lithography step, it is important to align the 2nd masks with the best alignment in order to have a low overlap area and to have a low overall capacitance for the Josephson Junctions device. Once the pattern has been developed, it is hard baked and placed in an Aluminum etchant to etch away the non-required Aluminum (Al) and transfer the pattern on to the Aluminum (Al) thin film.

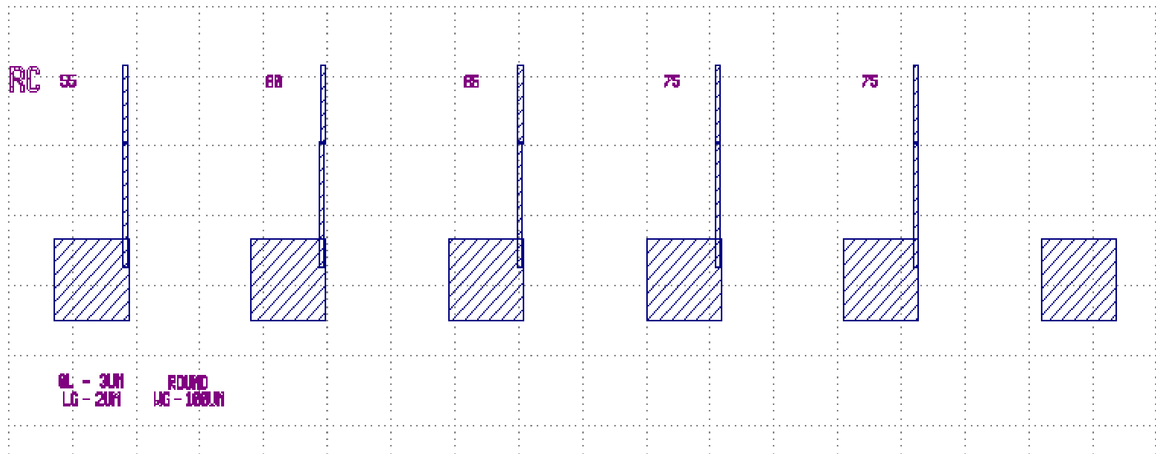


Figure 16 Mask pattern used in lithography step 2

Another quick dry etching is carried out using the Reactive Ion Etching (RIE) to etch away the thin Aluminum Oxide (Al2O3) thin film and any remaining SiO2 layer covering the bottom electrode. This needs to done in order to make the bottom electrode free from any dielectric so that it can be probed for electrical characterization. Figures 17, 18 and 19 show the final completely processed device which is ready for electrical testing and characterization.

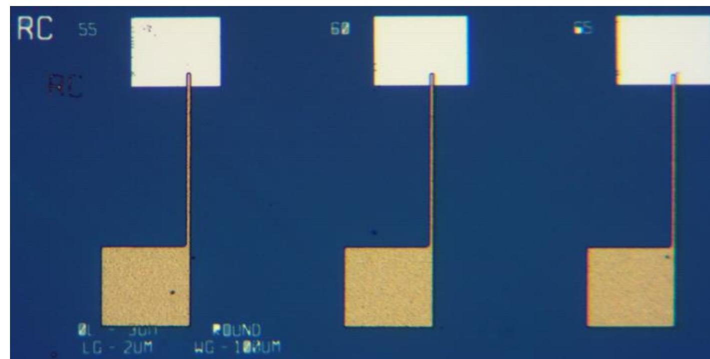


Figure 17 Device at end of fabrication process

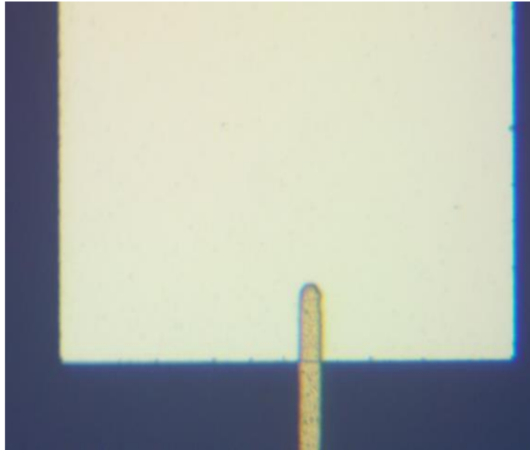


Figure 18 Junction at end of fabrication process

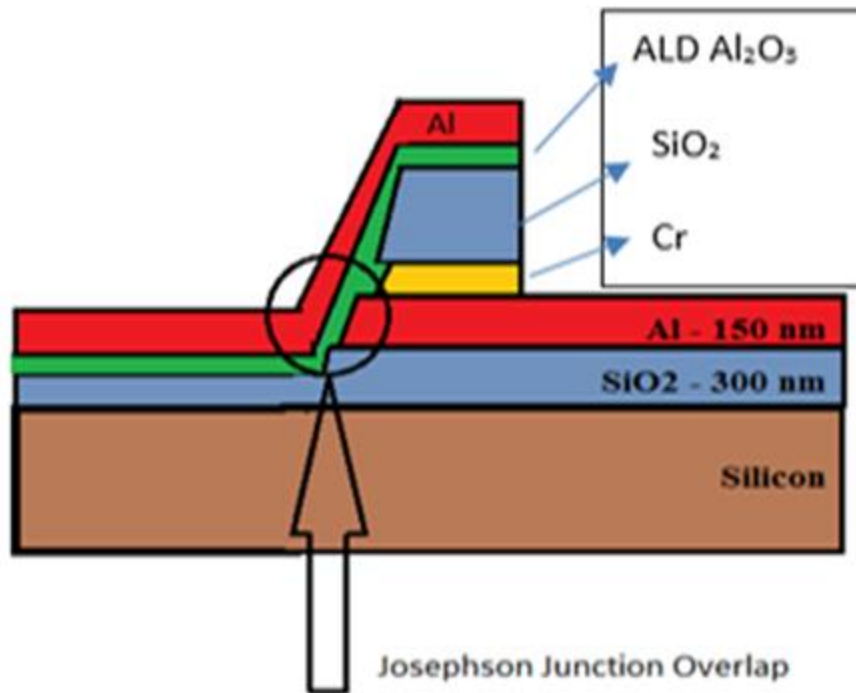


Figure 19 Final cross-sectional structure of the device

4. RESULT AND ELECTRICAL CHARACTERIZATION

4.1 Electrical characterization of Josephson Junctions (MIM)

In this section of the thesis, DC characterization of newly fabricated Josephson Junctions is presented. The DC characterization of the Josephson Junctions / Metal Insulator Metal (MIM) capacitors is carried out room temperature using an HP 4145B Parametric Analyzer and Keysight Technologies LCR E4980A. The HP 4145B Parametric Analyzer is used in obtaining the current (I) vs voltage (V) characteristics. Using the Current (I) –Voltage (V) characteristics, different parameters; such as differential resistance, tunneling characteristics and responsivity of the Josephson Junctions devices have been obtained.

The LCR E4980 Agilent meter is used in obtaining the Capacitance (C) vs Voltage (V) and Conductance (G) vs Voltage (V) characteristics at various frequencies. Capacitance (C) measured from the LCR meter was compared to the theoretical expected values as a cross check for confirmation of a successful fabrication process. As discussed earlier, various tunneling phenomenon, such as Fowler-Nordheim Tunneling (FNT), Direct Tunneling (DT), Poole-Frenkel Tunneling (PFT), Trap Assisted Tunneling (TAT) can be observed when the dielectric thickness is towards the lower order of tens of nanometer. Analysis of the Current (I) vs Voltage (V) curves under various plot relationships helped in obtaining clear clarification in regard to the possible tunneling cases observed by the junction devices fabricated in this research.

The testing setup used in order to perform the IV measurement in this research work is shown. The HP 4145B parametric analyzer is used through a LABVIEW software by linking the parametric analyzer to a computer using a GPIB interface. The parametric analyzer allows for voltage sweep from negative to positive range. Using the LABVIEW module, a two point or a four point probe IV measurement is performed. The 4 point probe IV measurement is performed in order to attain the resistance of the junctions without the contact pad resistance. But due to smaller contact pad size, probing using a 4 point probe system was difficult, so 2 point probe IV curve measurement was performed and a correction factor was used in order to attain the actual active area junction resistance. Figure 20 shows the analyzers used during the electrical analysis.

Figure 20 HP 4145B and LCR 4980 Meter used for electrical analysis [picture from research lab]

Another setup similar to the above mentioned setup was used for the measurement of the C-V and G-V curves through an Agilent LCR E4980 meter. This meter was also connect to the computer by a GPIB and interacted with the computer through a LABVIEW code. The LCR meter has a frequency range of 20 Hz to 2 MHz

and was used to measure the capacitance and conductance for s DC voltage applied across the junction. A constant AC Bias of the order of mV is also applied during the measurement process.

The first set of samples that were processed consisted of the Josephson Junctions fabricated through the Wet Etch process. Based on the electrical characterization results obtained for the wet etch sample, the next set of samples were fabricated using the dry etch fabrication process as mentioned in the above section. Table 1 shows the different set of devices that were fabricated and electrically characterized.

Sample Description	ALD Thickness	Etch Process
Al / ALD Al_2O_3 / SiO_2 / Al / SiO_2 / Si	0.00 nm	Dry Etch
Al / ALD Al_2O_3 / SiO_2 / Al / SiO_2 / Si	0.30 nm	Dry Etch
Al / ALD Al_2O_3 / SiO_2 / Al / SiO_2 / Si	0.60 nm	Dry Etch
Al / ALD Al_2O_3 / SiO_2 / Al / SiO_2 / Si	1.50 nm	Dry Etch
Al / ALD Al_2O_3 / SiO_2 / Al / SiO_2 / Si	2.50 nm	Wet Etch

Table 1 Sample description with ALD dielectric thickness and etch process

4.2 Capacitance (C) vs Voltage (V) characteristics

The Capacitance-Voltage (C-V) characterization of MIM capacitors or Josephson Junctions was carried out using the LCR meter. It uses the following equation in order perform the measurement:

$$Q = C\ V \tag{23}$$

The expected capacitances values for all the fabricated devices were calculated using the following formula:

$$C = (\varepsilon * k * A) / d \tag{24}$$

where ε: is the permittivity of free space, k: the relative permittivity of the material, A: junction overlap area, d: dielectric / insulator thickness.

Both junction and parasitic capacitance components were extracted theoretically. These two capacitances have different overlap area and different dielectrics (Al_2O_3 and SiO_2) connected in parallel to each other. The overall capacitance for the junction is found by using the following formula:

$$C_{parallel} = C_{Al2O3} + C_{SiO2} \tag{25}$$

Table 2 shows the theoretical expected and measured capacitance for various Josephson Junctions in the units of (fF). Figure 21 shows the location of the capacitances.

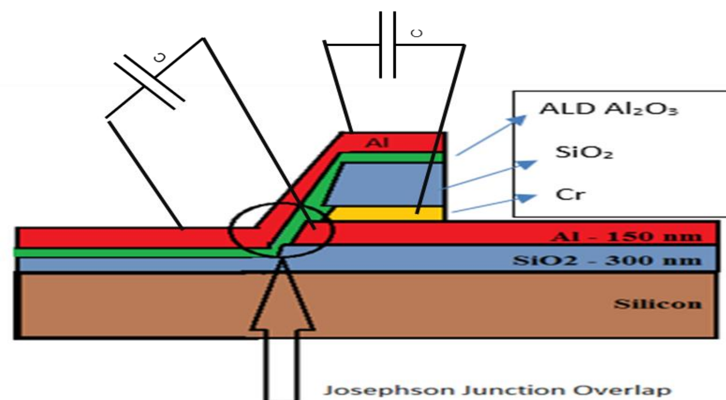


Figure 21 Cross section of the junction with junction and parasitic capacitances

Sample	Expected Capacitance (fF)	Measured Avg. Capacitance (fF)
ALD 0.3 nm	151.39 fF	171.612 fF
ALD 0.6 nm	134.82 fF	147.848 fF
ALD 1.0 nm	94.930 fF	111.799 fF
ALD 1.5 nm	58.051 fF	48.6768 fF

Table 2 Expected and measured capacitance values for dry etched sample

Both expected and measured readings are found to be within close vicinity of each other, one being the actual capacitance and other being a normal capacitance per unit area. Table 3 provides the summary of capacitance per unit area for these devices.

Sample	Expected Capacitance (fF / µm^2)	Measured Avg. Capacitance (fF / µm^2)
ALD 0.0 nm	1.1463	1.2454
ALD 0.3 nm	1.0814	1.2032
ALD 0.6 nm	0.9631	1.0618
ALD 1.0 nm	0.6781	0.7604
ALD 1.5 nm	0.4147	0.3402

Table 3 Expected and measured capacitance per unit area for etched samples

Figure 22 shows the Capacitance (C) vs Voltage (V) plot for the samples fabricated through the wet etch sample. The C-V values were in the region of about 12-23 femto Farad (fF) which was similar to the theoretical expected values. The wet etched Josephson Junctions consisted of an Al_2O_3 layer in the order to 3.0 – 3.5 nm. All the samples measured were adjacent to each other on one die on a single substrate. No process variation between the wet etched samples was observed. The junction area overlap of these devices was in the order of ~ 0.700 μm^2. The measurement was carried out at an AC bias of 5mV with a frequency of 1MHz.

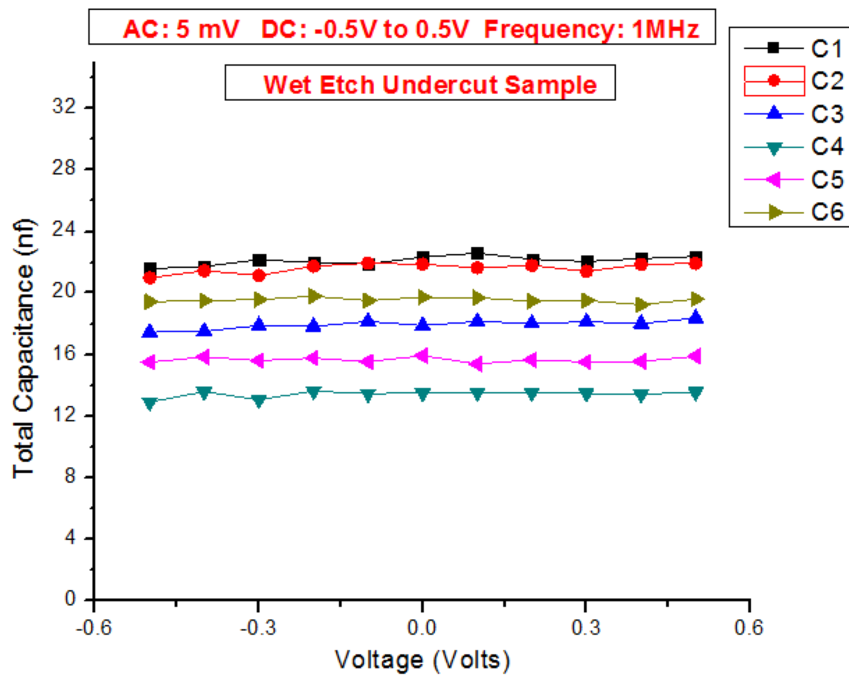


Figure 22 Capacitance vs Voltage for wet etch samples

Next set of sample that were measured were the dry etched Step-Edge Josephson Junctions samples with various thickness of ALD Al_2O_3 such as 0.00 nm, 0.30 nm, 0.60 nm, 1.0 nm and 1.5 nm. The capacitance was measured in the units of fF and fF / μm^2. The capacitance values were plotted over a unit to account for the small change in the overlap area of the Josephson Junctions. As capacitance is inversely related to the thickness of the dielectric, a similar expected trend was observed during the measurement process. The capacitance values showed a decrease with increasing thickness of the ALD dielectric. Figure 23 shows the plot of capacitance per unit area vs the applied voltage for all the dry etched processed devices with various ALD thicknesses.

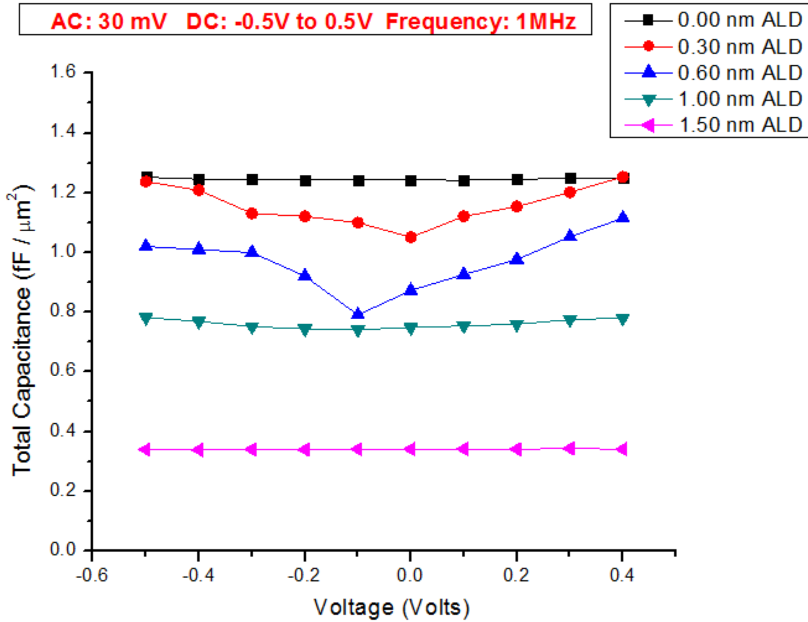
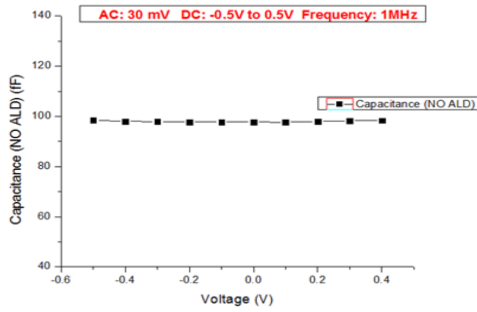
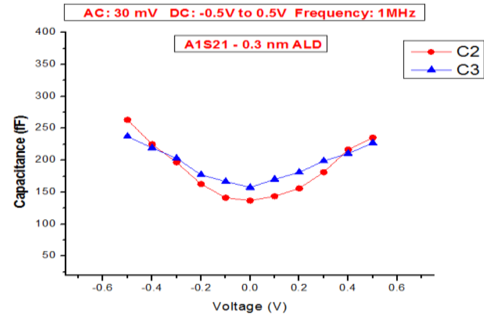


Figure 23 Capacitance per unit area vs Voltage for dry etch samples

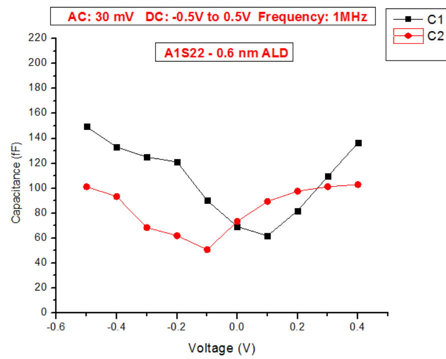
The next set of figures, figure 24 a-e, show the C-V plot for thickness 0.00 nm, 0.30 nm, 0.60 nm, 1.00 nm and 1.5 nm Al_2O_3 ALD dielectric/insulator thickness.



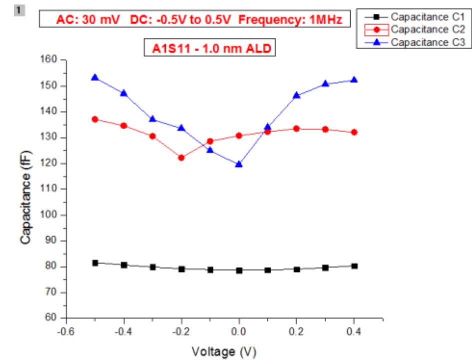
(a)



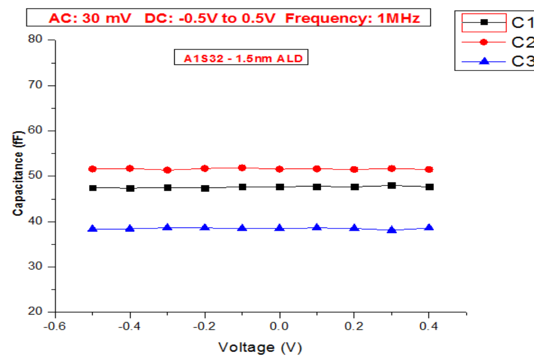
(b)



(c)



(d)



(e)

Figure 24 C-V plot for dry etched samples, a) 0.00, b) 0.30, c) 0.60, d) 1.00 and e) 1.50 nm ALD

It is important to be careful when measuring capacitances in the range of femto-Farad (fF). Various correction factors, such as, Short, Open and Wire length were taken into account in order to eliminate the noise from the LCR monitor and test setup, as the capacitances measured in this research work are in the very low magnitude. Figure 25 shows the relation between the expected and measured capacitance values for the dry etched sample.

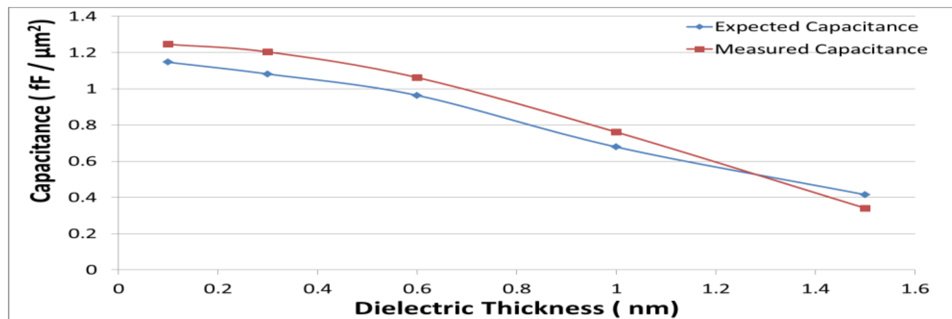


Figure 25 Plot of expected and measured capacitances per unit area vs dielectric thickness

4.3 Conductance (G) vs Voltage (V)

The conductance (G) measurements were also carried out using the same LCR Agilent 4980 meter through the entire frequency range supported by the LCR meter ~ 20 Hz to 2MHz. The first sample for the G-V measurement was the Josephson Junctions fabricated by using the wet etch fabrication process for ALD Al_2O_3 with a thickness of 3 nm. The conductance measured was orders of magnitude lower than the expected / target values. This was attributed to a couple of possible reasons, a quite thick ALD Al_2O_3 dielectric / insulator layer and to the possibility of having a very severe isotropic wet

etch of the bottom metal electrode. Thereby increasing the gap between the two metal electrodes to a severe margin, and hence decreasing the ability of electron / current transfer between the two electrodes. Figure 26 shows the plot of G-V for wet etched sample. It was due to these low conductance values that the process of Josephson Junctions fabrication was changed to a Dry Etch based – Anisotropic etch process, with much thinner ALD Al_2O_3.

The new samples fabricated by the dry etched technique and with thickness as mentioned in table 4 were fabricated and measured. The conductance values measured for the dry etch samples was much better and in the same range as target and expected values. The combined plot for all dry etch samples describing the G-V measurement can be seen in figure 27.

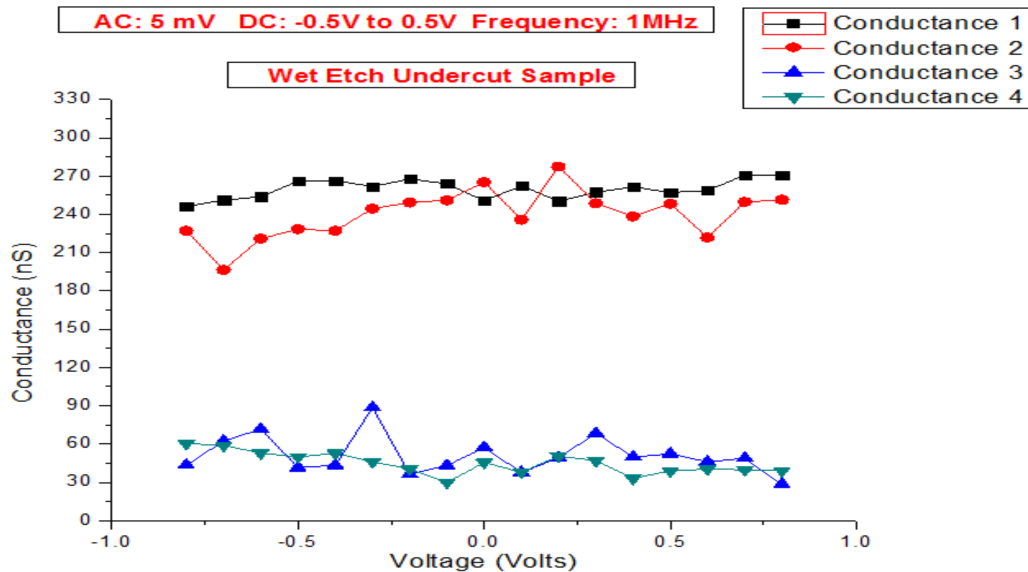


Figure 26 Wet etch undercut sample G-V curve

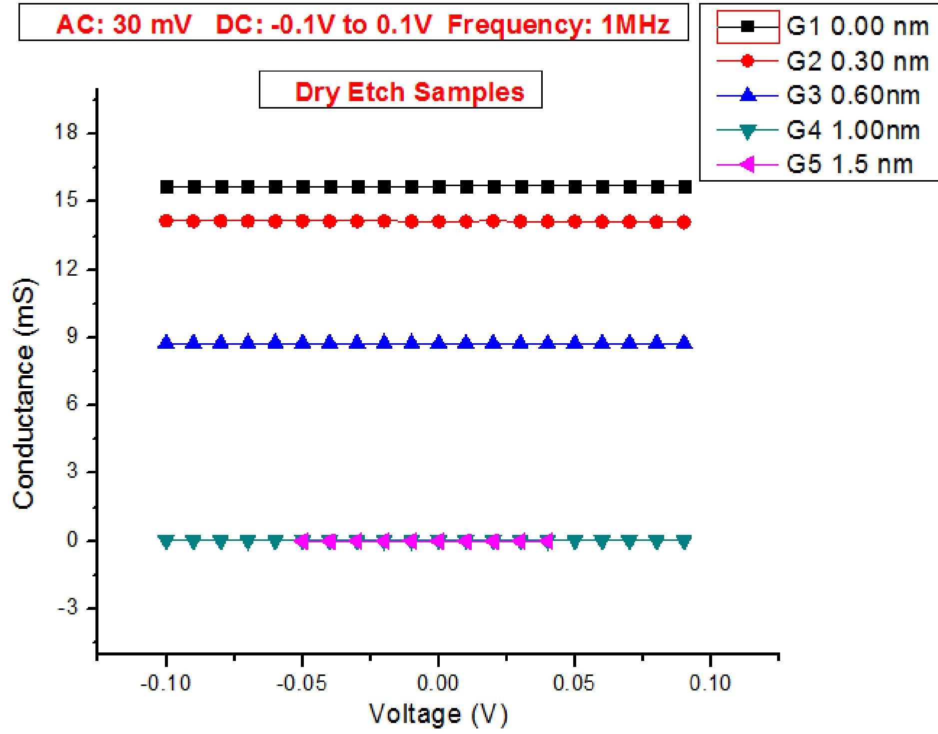


Figure 27 Dry etched samples G-V curve

Sample	Conductance (mS)
Wet Etch (3nm ALD Al_2O_3)	210 E-9
Dry Etch (0.00 nm ALD Al_2O_3)	15.703
Dry Etch (0.30 nm ALD Al_2O_3)	14.145
Dry Etch (0.60 nm ALD Al_2O_3)	8.7511
Dry Etch (1.00 nm ALD Al_2O_3)	0.0201
Dry Etch (1.50 nm ALD Al_2O_3)	74.72 E-5

Table 4 Measured value of conductance from the LCR meter

Table 4 gives a summary of the conductance value measured for the dry and wet etch samples. Figure 28 plots the relation between conductance and dielectric samples.

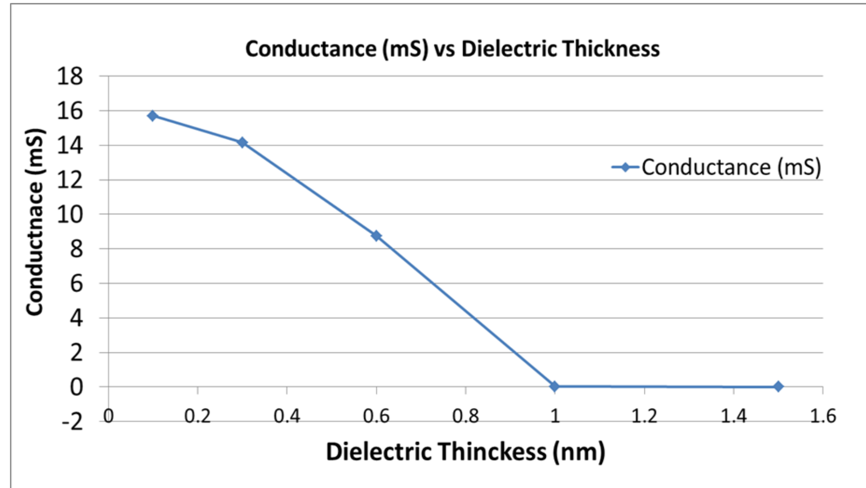


Figure 28 Conductance (G) vs Dielectric Thickness

4.4 Current – Voltage curve and tunneling mechanism

The next set of measurements that were carried out was the I-V curve measurement using the HP 4145B parametric analyzer. As mentioned earlier, the parametric analyzer is accessed using a LABVIEW code through a GPIB. I-V measurements were carried out by sweeping the DC bias from -0.1 to 0.1 V. The value of the sweep was kept in this lower end range in order to avoid device breakdown for devices with very small dielectric / insulator film. Once valuable data was obtained about the I-V behavior for all the dry etches devices, a further high voltage sweeps were carried out in order to identify the entire set of possible current tunneling phenomenon. Figure 29, 30 and 31 show the plot for the I vs V, ln (I) vs V and Current Density (J) vs

V for all of the dry etched samples. As expected from the model, total tunneling / leakage current collected across the junction is found to decrease with increasing thickness of the dielectric insulator layer.

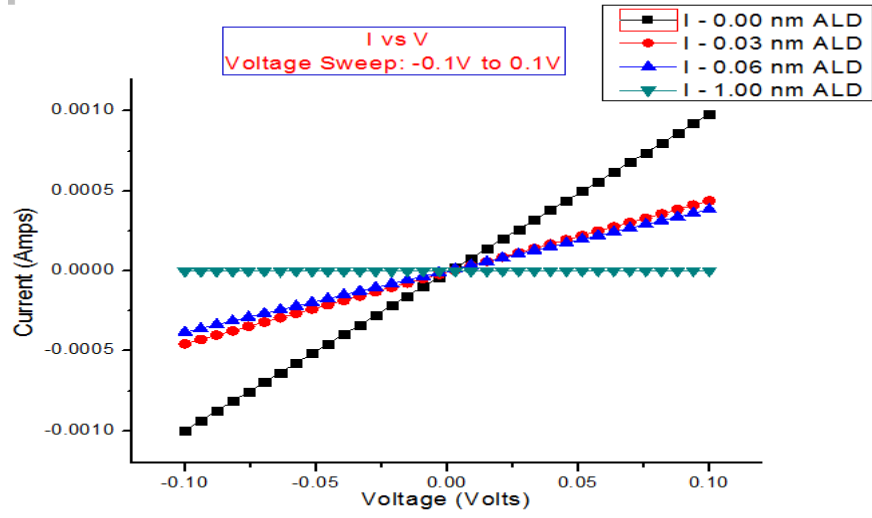


Figure 29 I-V curve for dry etched sample

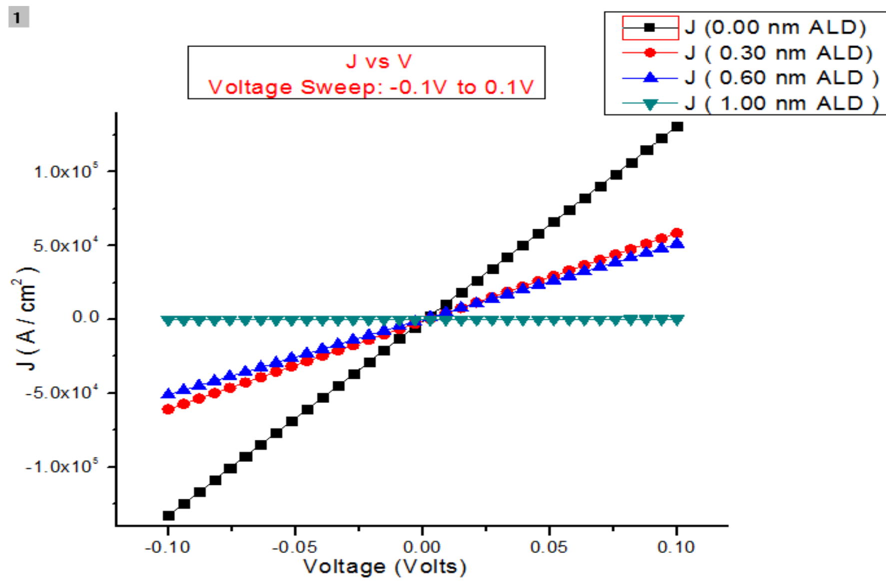


Figure 30 J-V curve for the dry etched samples

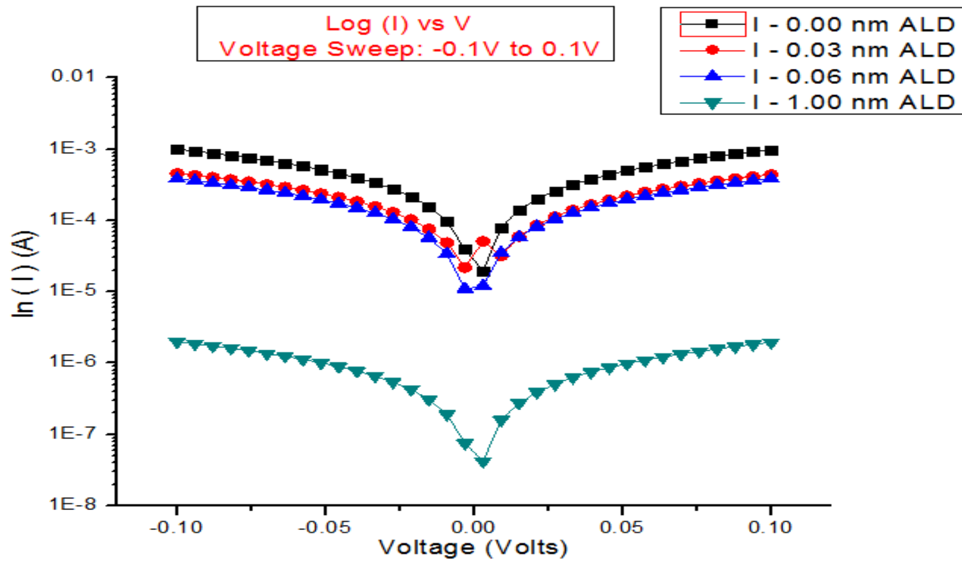


Figure 31 ln (I) - V curve for the dry etched samples

A similar plot for all devices with a higher voltage sweep was also carried out. Figures 32 and 33 represent the I-V curve plot obtained for all the dry etched devices for higher DC bias sweep.

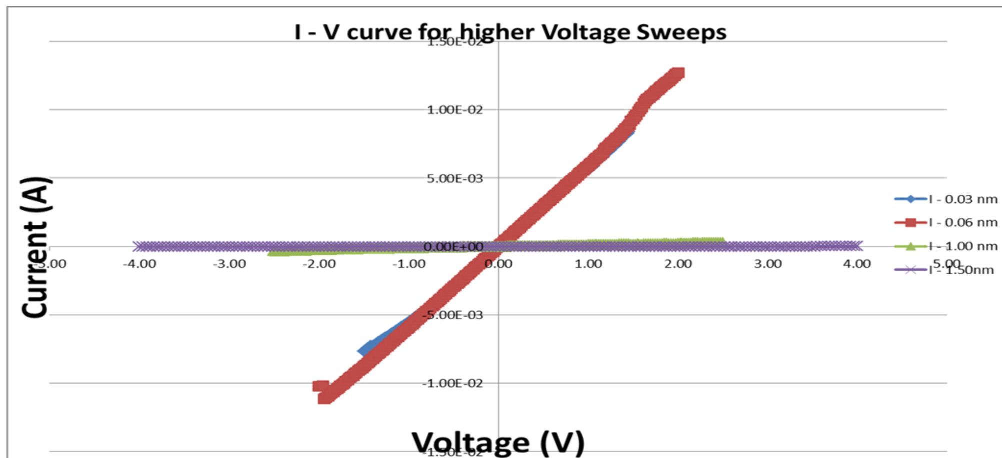


Figure 32 I - V curve for the dry etched samples, for voltage sweeps of high bias

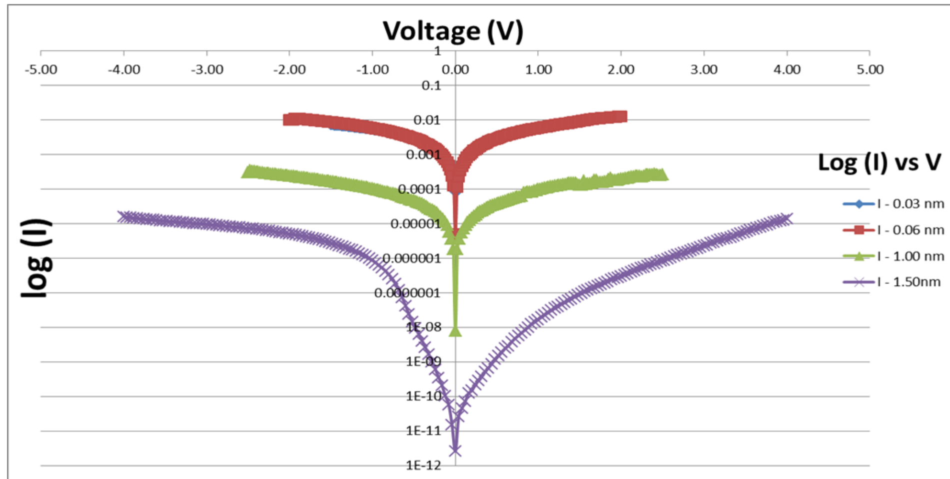


Figure 33 log(I) - V curve for the dry etched samples, for voltage sweeps of high bias

4.4.1 Differential resistance

Using the data collected from the I-V curve measurement setup, the resistance for the Josephson Junction device is extracted by using the differential resistance formula. The differential resistance is given as follows:

$$R_{diff} = (dV / dI) \qquad (21)$$

Table 5 summarizes the values obtained for the differential resistance near to 0 V bias.

Sample	Average Differential Resistance, R (Ω)	Differential Resistance near 0 V, R (Ω)
Dry Etch (0.00 nm ALD Al_2O_3)	101 Ω	102 Ω
Dry Etch (0.30 nm ALD Al_2O_3)	223 Ω	225 Ω
Dry Etch (0.60 nm ALD Al_2O_3)	261 Ω	264 Ω
Dry Etch (1.00 nm ALD Al_2O_3)	51 KΩ	51.6 KΩ
Dry Etch (1.50 nm ALD Al_2O_3)	247 KΩ	-

Table 5: Average differential resistance at ~ 0V for dry etched samples

The plots obtained for the differential resistances for all of the dry etched ALD samples are shown in figure 34, 35 and 36.

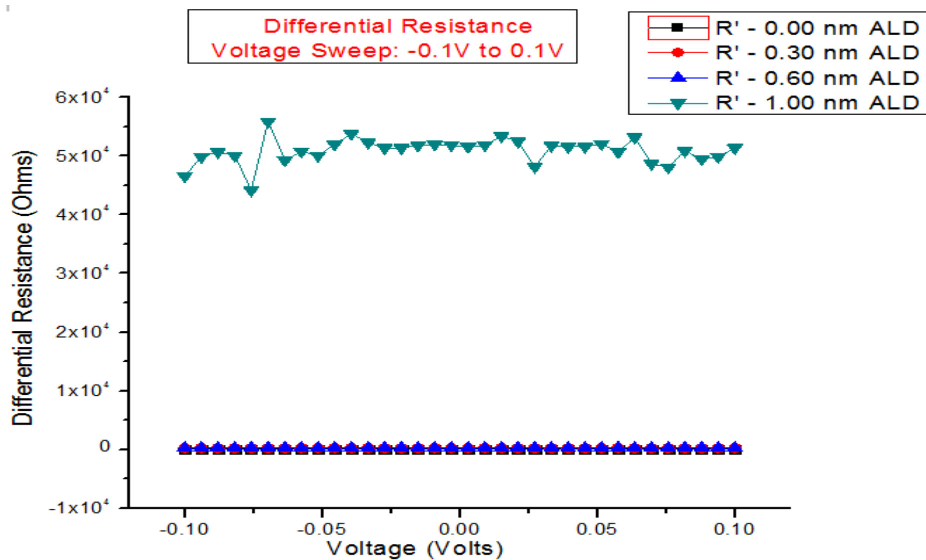


Figure 34 Differential Resistance for dry etched samples

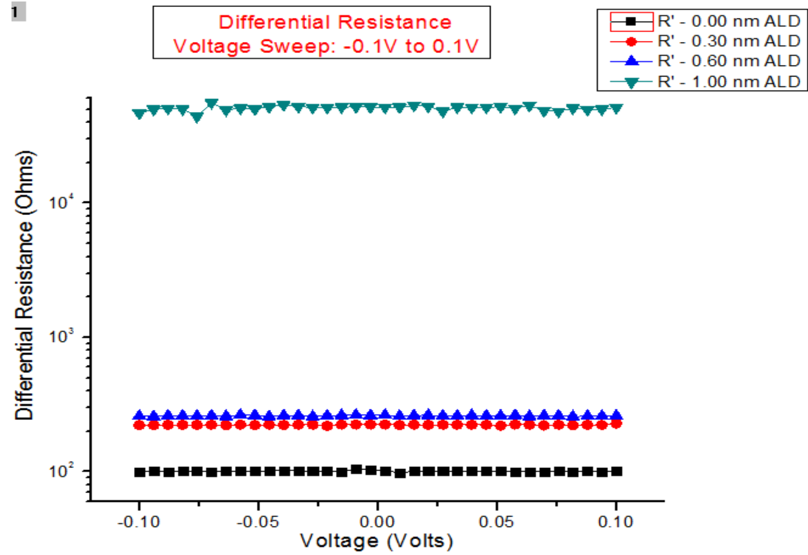


Figure 35 Differenital Resistnce for dry etched sample on semi-log plot

Plots for the differential resistances for the dry etched junctions can be seen in figure 34, 35, 36. Figure 37 shows relation between resistance and dielectric thickness.

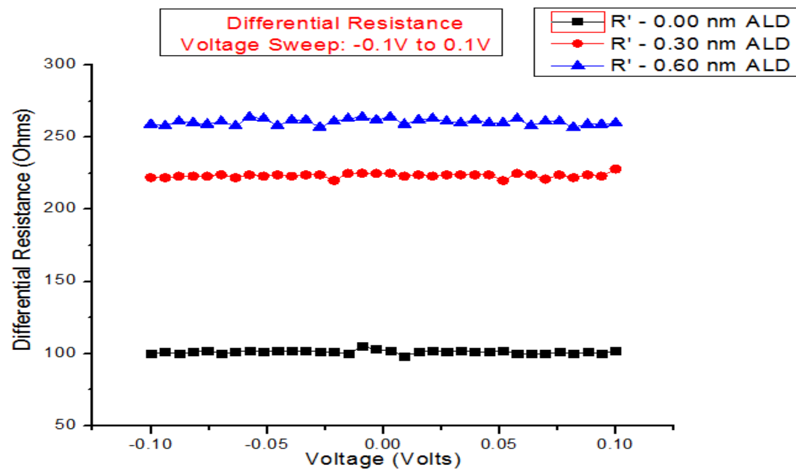


Figure 36 Differenital Resistnce for dry etched sample 0.00, 0.30 and 0.60 nm ALD

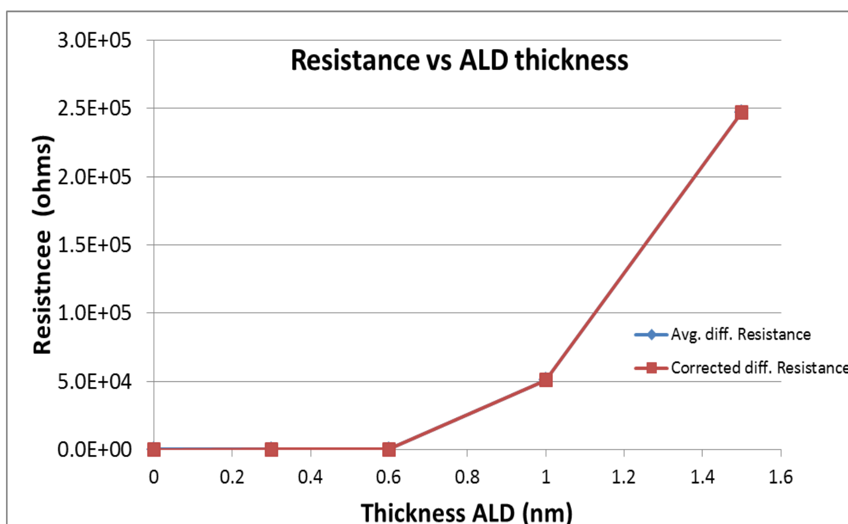


Figure 37 Resistance across junction vs Dielectric thickness

4.4.2 Current Tunneling

As discussed in earlier section of this thesis, Metal-Insulator-Metal (MIM) capacitors or Josephson Junctions are theoretically ideal insulators and must avoid flow of current across the barrier. However, as the thickness of the dielectric / insulator film is in the extreme lower order of nanometer, these devices allow current transfer between the 2 electrodes. The current that gets passed through the junction is referred to as the leakage or tunneling current.

There are various types of tunneling that the Metal-Insulator-Metal (MIM) devices under go, such as: such as Fowler-Nordheim Tunneling (FNT), Direct Tunneling (DT), Poole-Frenkel Tunneling (PFT), Trap Assisted Tunneling (TAT) can be observed when the dielectric thickness is towards the lower order just a few nanometer [12].

Direct Tunneling is most common type of tunneling occurring in these devices, occurring with the application of even a very small amount of bias – in the region of -0.5 V to 0.5 V. As the dielectric thickness is in the range of 0.00 nm to 1.50 nm, the electric field setup across it is still in the range of 1 mega-volts / centi-meter (1 MV/cm) with the application of DC bias as low as 0.1 V, therefore, with application of higher DC bias, of the order to 1 ~ 1.5 V, the electric field reaches a max value of 3.33 – 5.00 MV/cm for the 0.30 nm ALD sample, which leads to shorting the device. Hence, most of the devices were tested in the lower voltage bias range. Devices with thicker ALD, 1.0 and 1.5 nm, were capable of handling higher voltage bias, upto 2.5 and 4.0 V respectively. All devices were able to show Direct Tunneling, however, only 1.5 nm ALD device was clearly able to show Fowler-Nordheim tunneling (FNT). The 0.0 nm ALD devices also marginally showed evidence of Fowler-Nordheim tunneling. Though the dielectric is deposited using the Atomic Layer Deposition method, it is prone to Trap Assisted Tunneling (TAT) when the thickness of the dielectric is in the orders of just a few monolayers. As a result, Trap Assisted Tunneling (TAT) could be clearly observed for all of the dry etched processed samples. Different type of tunneling have different kind of relationship between current (I) and voltage (V), as a result, various set of plots were plotted in order to determine the most appropriate tunneling behavior for each set of device.

Direct and Fowler-Nordheim tunneling can be observed in plots such as; ln (I/E_{ox}^2) vs $(1/E_{ox})$ and / or ln (J/E_{ox}^2) vs $(1/E_{ox})$ and /or ln (I/V^2) vs $(1/V)$ [11, 12], where I is current across barrier, J is current density across barrier, E_{ox} is external electric field

applied across the dielectric and V is the bias voltage. For any of the above 3 mentioned plots, a logarithmic decrease represents a Direct Tunneling behavior and a parabolic increase represents the region of Fowler-Nordheim Tunneling. The region where the Direct Tunneling switches over to the Fowler-Nordheim Tunneling is referred to as the region of transfer, and the voltage applied at this region is referred as the transfer voltage, V_{trans}. Trap Assisted Tunneling is observed as linear line under an ln (I) vs (1/ E_{ox}) and / or ln (J) vs (1/ E_{ox}) [12]. The findings from the data analysis using the above mentioned plots helped in understanding the tunneling behavior occurring in the devices fabricated in this research work.

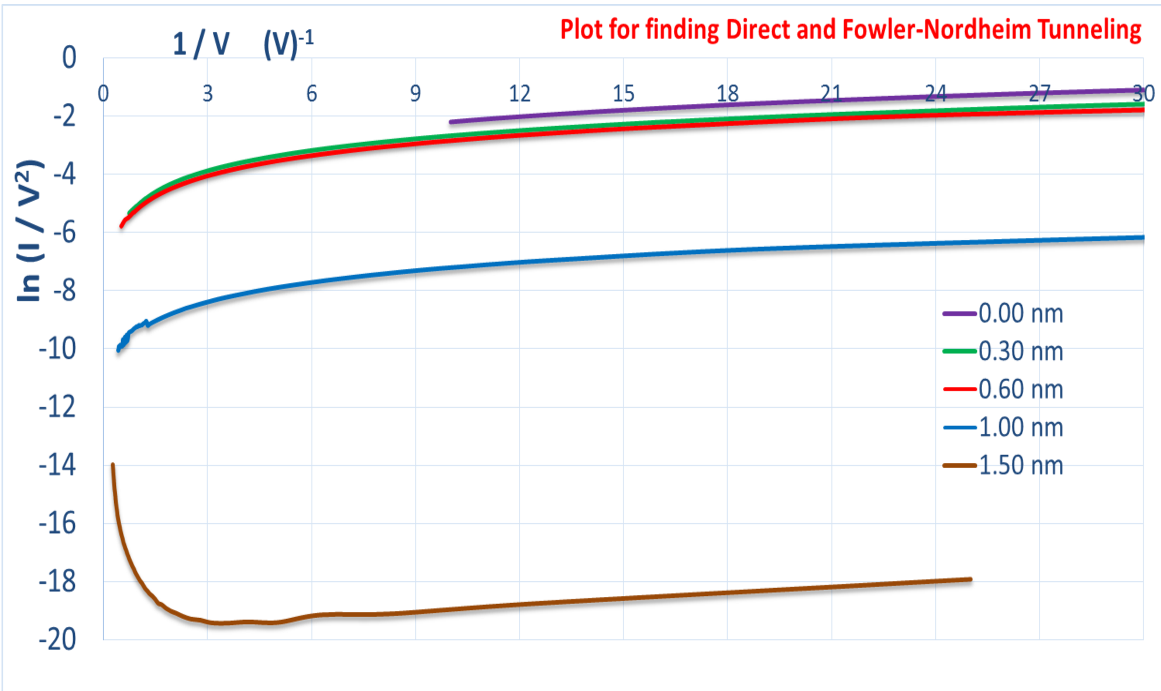


Figure 38 Plot of ln (I / V^2) vs (1/V) for dry etched samples, to identify Direct and FN tunneling regions

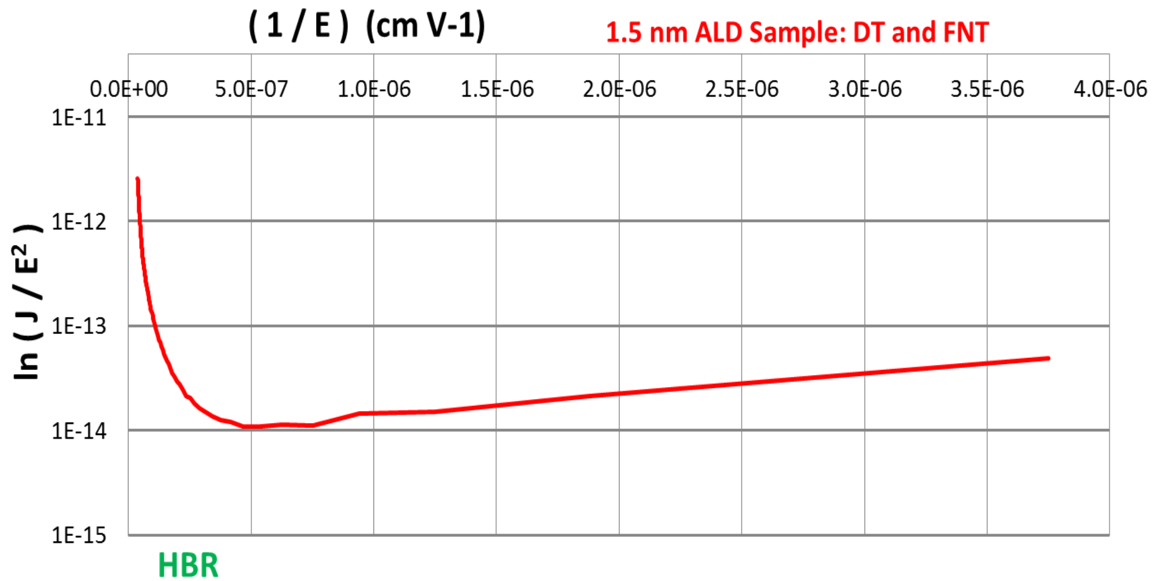


Figure 39 Plot of ln (J/ E^2) vs (1/E) for dry etched samples, to identify FN tunneling regions

It was observed from figure 38 that only the 1.50 nm ALD sample was able to undergo Fowler-Nordheim Tunneling, whereas rest of all the samples just exhibited Direct Tunneling. It was found from figure 38, using the slope of the 1.50 nm sample in the high electric field region, that the barrier height between Al-ALD Al_2O_3 is 1.74 eV and effective mass of the electrons in the oxide is 0.26

Using the slope and the intercept from the FN Tunneling region from figure 39, and the equations for the slope and the intercept, the barrier height obtained was 1.75 eV along with an effective mass of electron in the ALD dielectric as $0.26m_0$. These values are well within the range of the values obtained from the literature survey.

Using the model setup, various parameters concerning to the dielectric and the junction such as the barrier height and the effective electron mass were extracted from

the plots. It was also found that the dry etched devices conduct only due to the Direct Tunneling mechanism for most of the voltages that they can withstand without being blown apart. It is only the 1.5 nm ALD dry etched sample which can withstand high bias voltage and thus is able to undergo Fowler-Nordheim Tunneling when electric field is in the range of 26.66 MV /cm.

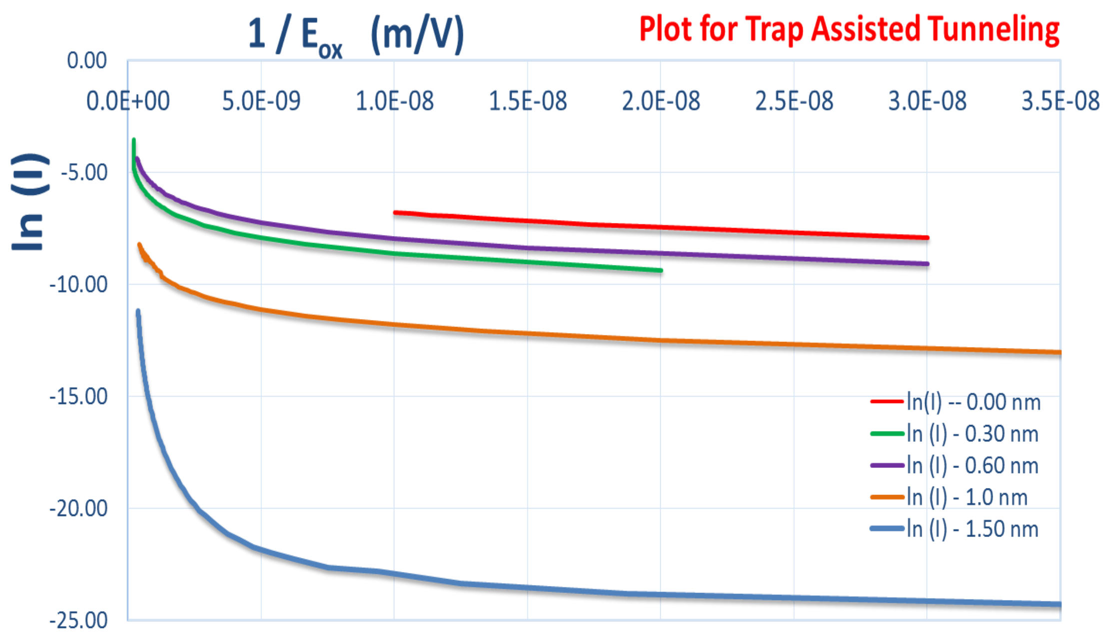


Figure 40 Plot of ln (I) vs 1/ E for the dry etched samples, to identify TAT

In regard to the Trap Assisted Tunneling, figure 40 it was observed that as the electric field across the junction increased, there was a much Trap Assisted Tunneling occurring in the region. Trap assisted tunneling is noted by a linear line on the plot of ln (I) vs $1/E_{on}$ [12]. It is observed from the plot that, the 1.5 nm sample shows the highest

degree of Trap Assisted Tunneling, closely followed with the 1.00 nm sample. Sample of thickness less than 1.00 nm ALD show just about little sign of Trap Assisted Tunneling.

From model discussed earlier, resistance in the junction is found to decrease as we near the critical temperature of the superconducting metal electrode. As Josephson Junctions are measured at critical temperature with a very low bias, in the order to 1 to 10mV, only Direct Tunneling through the dielectric is observed. At low temperatures, the dielectric is found to freeze out, thereby increasing the resistance to the flow of electrons; however, as the overall resistance of the metal is now zero, electrons pair up and tunnel across the barrier in the form of Copper pairs. Thus, only Direct Tunneling will be observed at such low temperatures. Figure 41 shows the relationship between the current voltage ration to the square root of the voltage for Poole Frenkel Emission.

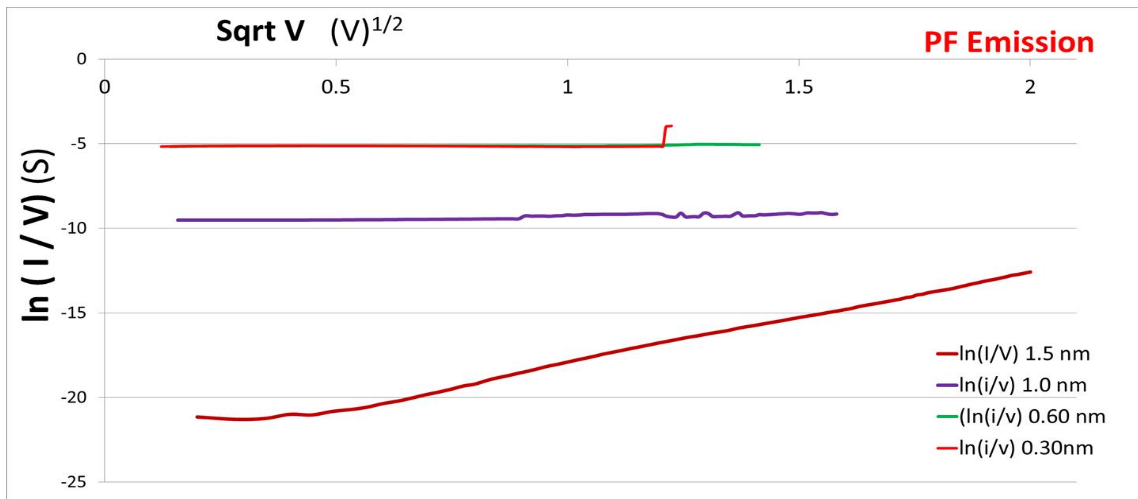


Figure 41 Plot of ln (I/V) vs sort (V) for the dry etched sample, to identify Poole-Frenkel Emission at 300 K.

5. CONCLUSION AND FUTURE WORKS

5.1 Conclusion

A new process flow for the fabrication of Metal-Insulator-Metal electrode with the application as Josephson Junctions was presented in this research work. A new approach to Josephson Junctions fabrication was required in order to integrate the Josephson Junctions fabricated devices along with Gann / Alga based hetero-structures devices, such as the High Electron Mobility Devices. The current fabrication process, using the Dolan Bridge (or Shadow Mask) is the most commonly process when it comes to the fabrication of the Josephson Junctions. However, this fabrication process suffers from the critical limits placed on the accuracy of the resist thickness along with the angle of superconductor metal deposition [29]. A slight error in the process, will lead to no overlap or very large overlap of the junction area, thereby decreasing our yield. This process also suffers from the mechanical and thermal stability limit imposed on it due to the stability of the free standing structure. As the future of quantum based circuits requires fabrication of even smaller devices, even smaller shadow mask / Dolan Bridge set will be required, thereby increasing the difficulty of the process to an even higher level. There are also issues with what materials can be deposited using the Dolan bridge method, this is because of the reaction chemistry between the resist and some of the superconducting materials. Hence, integrating Josephson Junctions devices with other CMOS based devices such as HEMTs using the Dolan Bridge technique is not a viable approach, resulting in a lower yield.

The deposition of the insulator / dielectric film was also carried out through a different process. Generally, the insulator in all Josephson Junctions is grown using thermal oxidation of Aluminum, however, when the required thickness of dielectric / insulator layer is less than 1 nm, there are difficulties associated with conformal growth and getting the exact thickness. Hence, a relatively new method of dielectric deposition, Atomic Layer Deposition (ALD), was used along with the Step-Edge deposition technique. ALD provides very controlled and conformal film deposition even to lower thickness of less than 1 nm.

Therefore, a new approach based on Step-Edge fabrication technique is presented in this research work. The target values for the device fabricated using the Step-Edge fabrication technique included, small overlap area, junction capacitance in the order of low femto-farads, dielectric / insulator layer in the order of less than 2 nm, resistance of the junction less than 100 Ω μm^2 at room temperature. At the end of the fabrication process, it was found after testing and characterization that the dry etched process based devices with thickness 0.00 nm, 0.30 nm and 0.60 nm ALD Al_2O_3 achieved our pre-defined target values. These devices had a junction overlap area in the range of 0.750 μm^2, capacitance in the range of 80 – 130 fF, dielectric layer thickness less than 0.60 nm and resistances in the range of 80 – 160 Ω μm^2.

All possible tunneling phenomenon were studied and equations providing the relationship between current (me) and voltage (V) for each of these tunneling conditions was deduced in order to identify the type of tunneling that is observed from their respective plots. These plots helped in identifying the most relevant method of tunneling

occurring at room temperature. It was found that all the dry etched samples exhibited Direct Tunneling from very small bias voltages of 0.1 V. As the bias was increased, direct tunneling current increased through the barrier, however, as the electric field became significantly huge with increasing bias, all dry etched devices except the 1.50 nm ALD Al_2O_3 device were blown up, leading to a short. However, the 1.50 nm dry etched ALD device was able to cross the trans-over region from the Direct Tunneling side to the Fowler-Nordhein Tunneling. The slope of the Fowler-Nordhein Tunneling side was used in order to extract the parameters such as the barrier height of the device structure and the effective mass of the electron in the oxide. A very small evidence of Trap Assisted Tunneling was also observed for samples with ALD thickness as 0.00 nm, 0.30 nm, and 0.60 nm. However, significant Trap Assisted Tunneling was observed for the thicker ALD samples, 1.00 and 1.50 nm.

After the characterization of all the devices, it was concluded that the dry etched device samples with ALD thickness as 0.00 nm, 0.30 nm and 0.60 nm are best suited to perform as Josephson Junctions at their critical temperature. Hence, these samples were shipped out to an external research facility for low temperature measurements. The results are still to be received from the research facility at the point of this thesis defense.

5.2 Future work

Low temperature characterization and data evaluation of the samples that hit the target values at room temperature needs to be carried out. Any changes to the Step-Edge Junction process will be carried out according to the results observed from the low temperature measurement. Similar devices with Niobium as the superconducting metal

electrode must be fabricated. Niobium based junctions are an advantage over the Aluminum based junctions as they can function at a higher critical temperature in the range of 8 – 9 K, when compared to that of ~ 1 K for Aluminum once.

Another investigation carried out during this research was measurement of GaN / AlGaN hetero-structure based High Electron Mobility Transistors (HEMT) at low temperatures. It was found that the 2 DEG layer in the hetero-structure did not freeze out at such low temperatures, instead the performance of the device was found to improve. A similar based hetero-structure based Josephson Junctions devices if fabricated using the Step-Edge fabrication process will provide even further performance at low / critical temperatures for applications related to RF and Quantum circuits. GaN / AlGaN thin films can be deposited using a Metal Organic Chemical Vapor Deposition Technique (MOCVD).

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