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Single-Flux-Quantum Bipolar Digital-to-Analog Converter Comprising Polarity-Switchable Double-Flux-Quantum Amplifier

Single-Flux-Quantum Bipolar Digital-to-Analog Converter Comprising Polarity-Switchable Double-Flux-Quantum Amplifier

Yoshinao Mizugaki, Tomoki Watanabe, and Hiroshi Shimada

Abstract—We present a single-flux-quantum (SFQ)-based digital-to-analog converter (DAC) generating bipolar output voltages, in which the key component is a polarity-switchable double-flux-quantum amplifier (PS-DFQA). The DAC comprised a dc/SFQ converter, an 8-bit variable pulse-number-multiplier (PNM), and a ± 8-fold PS-DFQA integrated on a single chip. SFQ pulse-frequency modulation was employed to realize variable output voltage amplitude, for which the multiplication factor of the variable-PNM was controlled by a commercial data generator situated at room temperature. The variable-PNM realized 8-bit resolution with a multiplication factor between 0 and 255. Bias currents fed to the ± 8-fold PS-DFQA were polarity-switched in synchronization with the digital code for the variable-PNM. The whole circuits including I/O elements were designed using SFQ cell libraries, and fabricated using a niobium integration process. Sinusoidal bipolar voltage waveform of 0.38 mV$_{\text{pp}}$ was demonstrated using a reference signal source of 43.94 MHz.

Index Terms—Superconducting integrated circuits, Josephson effect, Digital-analog conversion.

I. INTRODUCTION

PRECISE voltage generation is a unique feature of single-flux-quantum (SFQ) circuits, which may eventually realize future AC voltage standards [1]. We developed several SFQ-based digital-to-analog converters (DACs) where SFQ pulse-frequency modulation (PFM) [2] was employed for variable voltage generation [3]–[5]. The largest circuit so far was a 9-bit DAC with the maximum output voltage of 2.54 mV [5]. The output voltages of our previous SFQ-based DACs, however, were of single polarity, which was less advanced than bipolar programmable binary-weighted arrays of Josephson junctions (JJs) [6], [7] or pulse-driven JJ arrays [8], [9].

Since our previous SFQ-based DACs were driven by unipolar bias sources, their output voltages became of single polarity. One idea for realizing bipolar output voltage was adoption of the differential voltage between two output ports [10], which was similar to Josephson circuits designed for Johnson noise thermometry [11], [12] Although we demonstrated that the differential output voltage was bipolar, it was required to use a conventional differential amplifier whose amplification was not of quantum accuracy. The second idea was the

dual double-flux-quantum amplifier (dual-DFQA) where two DFQAs for positive and negative voltage multiplication were integrated [13]. The circuit operated correctly, while double amount of hardware was necessary for the dual-DFQA.

In this paper, we present another SFQ-based DAC generating bipolar output voltages. The key component for realization of bipolar output voltage is a polarity-switchable double-flux-quantum amplifier (PS-DFQA) [14]. A PS-DSQA is a stack of DFQA cells biased using a bipolar current source. The polarity of its output voltage is changed by switching the bias current polarity.

II. CIRCUIT DESIGN

A. Configuration of bipolar digital-to-analog converter

In SFQ circuitry, the average voltage $\langle V \rangle$ across a JJ is expressed as $\langle V \rangle = \Phi_0 f$, where Φ_0 and f are the flux quantum and the number of flux quanta passing through the JJ per unit time, respectively. SFQ-PFM DACs change their analog output voltage by changing f, i.e., the repetition frequency of an SFQ pulse train.

The whole configuration of the bipolar SFQ-PFM-based DAC designed in this work is shown in Fig. 1(a). A reference signal of frequency f_{Ref} is converted into an SFQ pulse train of repetition frequency f_{Ref}. Each SFQ pulse is then multiplied by $m(t)$ at the 8-bit variable pulse-number-multiplier (V-PNM). Here, $m(t)$ is an integer between 0 and 255, which is controlled by an 8-bit digital input code (t).

The modulated SFQ pulse train is forwarded to both a ± 8-fold and a ± 500-fold PS-DFQA. We have prepared two PS-DFQAs: the ± 500-fold PS-DFQA is our main target, whereas the ± 8-fold PS-DFQA is an alternative circuit.

For testing the V-PNM and PS-DFQAs separately, we have implemented two additional circuit elements. One is a "1/256 scaler" comprising 8 toggle flip-flops (TFFs), which is used for checking the multiplication factor of the V-PNM. The other is a JJ labeled as "JJ (over-bias)" that is used for feeding SFQ pulses to the PS-DFQAs and checking their input–output characteristics.

B. Variable Pulse Number Multiplier (V-PNM)

The 8-bit V-PNM comprises a ring oscillator (RO) with an 8-bit counter, which is similar to our previous design [3]–[5]. Two modifications have been made. The first one is that the oscillation frequency of the RO has been detuned from 12.3 to 11.16 GHz to increase timing margins in the V-PNM.
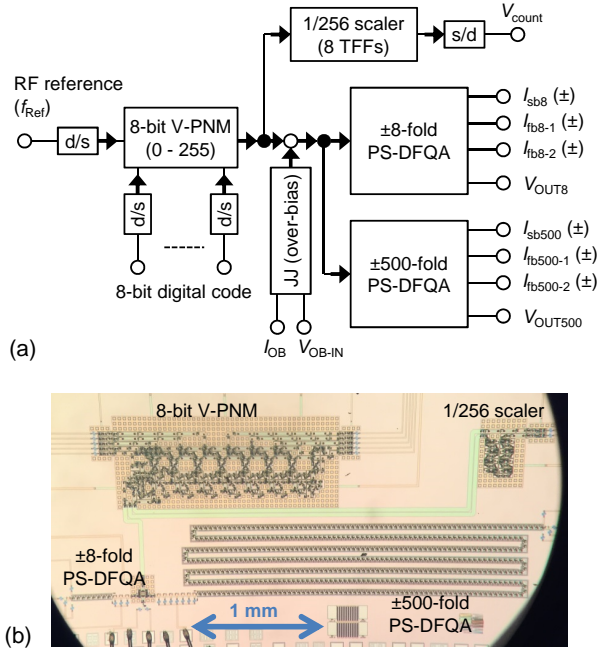
Fig. 1.　(a) Circuit configuration of the SFQ-based bipolar DAC. "d/s," "TFF," "s/d," and "JJ (over-bias)" denote the dc-to-SFQ converter, toggle flip-flop, SFQ-to-dc converter, and Josephson junction used for over-biasing measurement of the PS-DFQAs. (b) Photomicrograph of the measured chip.
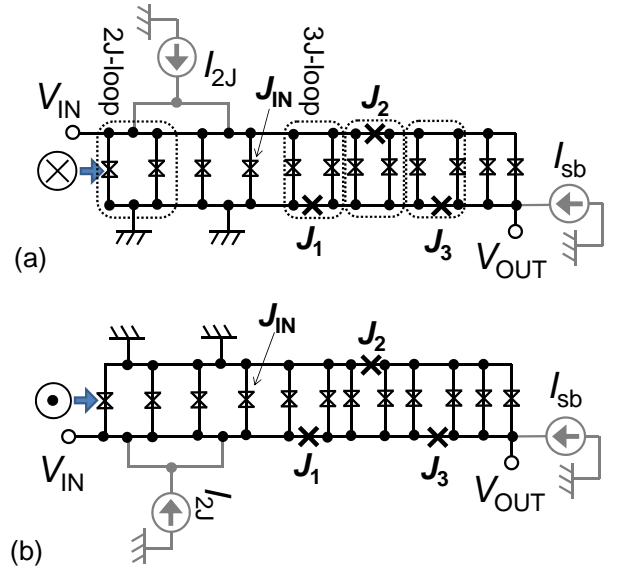

Fig. 2.　Configuration of (a) a conventional DFQA and (b) a PS-DFQA. Cross marks are under-damped junctions without shunt resistors. Hourglass marks are over-damped junctions. Flux bias lines are not shown.

The second one is that the multiplication factor is varied between "0" and "255," of which the range is different from our previous design between "1" and "256." This is because the polarity of bias currents to PS-DFQAs is assumed to be switched during the zero multiplication (zero output voltage) period, as described subsequently.

C. Polarity-Switchable Double-Flux-Quantum Amplifier (PS-DFQA)

A DFQA is a quantum voltage multiplier composed of stacked three-junction loops (3JLs) [15]–[17]. Fig. 2(a) shows its configuration including three 3JLs. One junction in a 3JL is under-damped, where 4π phase leap occurs for every input SFQ pulse. Although they are not shown in Fig. 2(a), two bias lines are magnetically coupled to 3JLs for adjustment of junction phases. In a DFQA comprising N 3JLs, the average output voltage becomes $+(N+1)V_{\mathrm{IN}}$ for the average input voltage V_{IN}. (For a DFQA integrated in an SFQ-PFM DAC, V_{IN} is expressed as $\Phi_0 m(t) f_{\mathrm{Ref}}$.) This is the positive voltage multiplication. When the polarity of biasing currents to the DFQA is inverted, negative voltage multiplication is realized with a different multiplication factor of $-(N-1)$, not $-(N+1)$. It means that the voltage amplitudes for positive and negative output are not identical.

To realize bipolar voltage multiplication of identical scales, we have developed a PS-DFQA [14]. It is presented in Fig. 2(b), where two flux bias lines are not shown. Its multiplication factors are $+NV_{\mathrm{IN}}$ and $-NV_{\mathrm{IN}}$ for positive and negative voltage multiplication, respectively. Modifications from the original DFQA are as follows. (i) The polarity of input SFQ pulses is inverted. (ii) The positions of the bias source

TABLE I
COMPARISON OF JUNCTION PHASE LEAPS FOR ONE INPUT SFQ PULSE IN A CONVENTIONAL DFQA AND A PS-DFQA.

	Conventional DFQA		PS-DFQA	
	Posi.	Nega.	Posi.	Nega.
J_{IN}	$+2\pi$	$+2\pi$	$+2\pi$	$+2\pi$
J_1	$+4\pi$	0	0	-4π
J_2	$+4\pi$	-4π	$+4\pi$	-4π
J_3	$+4\pi$	-4π	$+4\pi$	-4π
Total	$+8\pi$	-4π	$+6\pi$	-6π
		$(J_1 + J_3)$	$(J_{\mathrm{IN}} + J_1 + J_3)$	

and the ground for the input two-junction loop (2JL) stages are swapped. Combination of these modifications compensates the imbalance of junction phase leaps for positive and negative voltage multiplication. Table I summarizes the junction phase leaps in a conventional DFQA and a PS-DFQA. (Detailed operation is described in [14].)

D. Design, Fabrication, and Measurement

We have implemented the 8-bit bipolar SFQ-PFM DAC using both an SFQ digital cell library, which is referred to as the CONNECT library [18], and our DFQA library.

Test circuits were fabricated using the standard (25-μA/μm^2) Nb/AlO$_x$/Nb Josephson integration process of the National Institute of Advanced Industrial Science and Technology (AIST), Japan, referred to as the AIST-STP2. Fig. 1(b) shows a photomicrograph of a measured circuit. The total number of JJs is 2,710.

In measurements, a test chip was cooled at 4.2 K in liquid helium. A two-layer magnetic shield of highly permeable cans reduced the residual magnetic field on the chip. The input signals were generated using signal generators located at room temperature. An analog signal generator and a data pattern

generator were used for generating the reference signal and an 8-bit digital code, respectively. Bipolar bias sources for the PS-DFQAs were also used in synchronization with the 8-bit digital code. Waveforms were monitored on a digital oscilloscope via conventional 40-dB preamplifiers. We did not evaluate the absolute accuracy of the output voltage.

III. RESULTS AND DISCUSSION

A. Functional test of V-PNM

We first executed controllability test on the multiplication factor of the 8-bit V-PNM with low speed I/O signals. The reference signal of 256 kHz was applied to the reference input terminal, while the 8-bit code to the V-PNM was updated at every 1 ms.

Fig. 3(a) shows an example of V_{count} waveforms from the SFQ-to-dc converter. The number of V_{count} transitions in each 1-ms period provides the multiplication factor of the V-PNM. The code was programmed to realize a half period of a sinusoidal waveform with 256 voltage steps of 130 levels (3, 6, 9, 13, 16, 19, 22, 25, $\cdots$, 253, 254, 254, 254, 255, 255, 255, 255, 255, 255, 255, 255, 255, 255, 254, 254, 254, 253, $\cdots$, 25, 22, 19, 16, 13, 9, 6, 3, 0). The numbers of V_{count} transitions in 1 ms are indicated in Fig. 3(a), which correspond to the multiplication factors.

A sequence of the multiplication factors is shown in Fig. 3(b). Correct operation was confirmed except for one error per one half period, where the multiplication factor was not the correct value of 208 but 209. (The errors are not recognizable in Fig. 3(b).) The origin of this error has not been determined.

B. Functional test of PS-DFQA

Input–output characteristics of the PS-DFQAs were checked independently using SFQ pulses fed from an over-biased JJ.

Fig. 4 shows the input voltage–output voltage ($V_{\text{OB-IN}}$–V_{OUT8}) characteristics of the $\pm$8-fold PS-DFQA. $\pm$8-fold multiplication is confirmed for $V_{\text{OB-IN}}$ beyond 100 μV. The corresponding input SFQ repetition frequency $V_{\text{OB-IN}}/\Phi_0$ is 48 GHz, sufficiently higher than the maximum oscillation frequency of the RO in the 8-bit V-PNM (11.16 GHz).

We also measured the input–output ($V_{\text{OB-IN}}$–V_{OUT500}) characteristics of the $\pm$500-fold PS-DFQA. Although we found biasing conditions realizing $\pm$500-fold operation, the maximum $V_{\text{OB-IN}}$ was 28 μV at maximum, for which $V_{\text{OB-IN}}/\Phi_0$ is calculated to be 13.5 GHz. In addition, the bias margins for $\pm$500-fold operation were as small as a few percent.

Because of tight operation margins of the $\pm$500-fold DFQA, we tested the bipolar DAC operation using the $\pm$8-fold PS-DFQA.

C. Bipolar DAC operation

By programming the 8-bit digital code for the V-PNM as well as the synchronization signals to the biasing sources for the $\pm$8-fold PS-DFQA, the DAC synthesized a bipolar sinusoidal voltage waveform shown in Fig. 5. The frequency of the reference signal was set to 43.94 MHz, while the digital
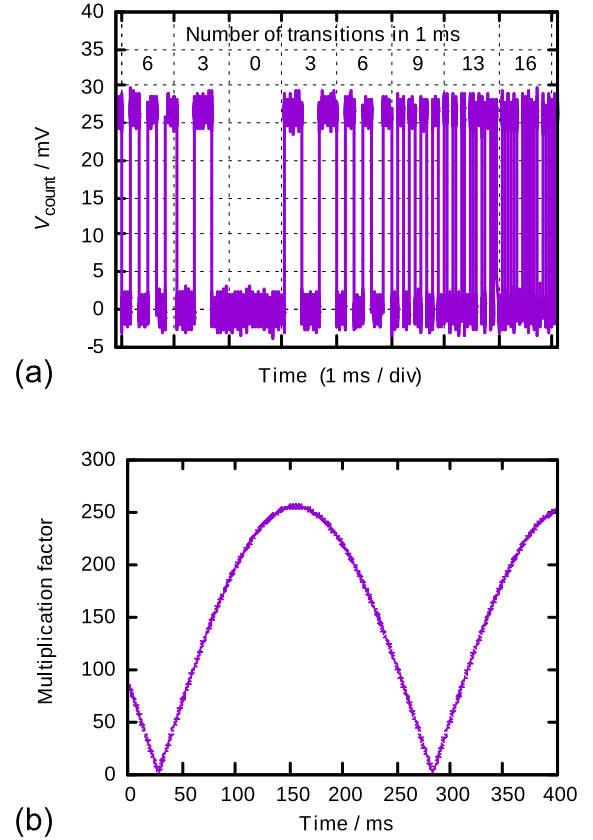

(a)

(b)

Fig. 3. (a) Example of V_{count} transitions representing the multiplication factor of the 8-bit V-PNM. (b) Sequence of the multiplication factor of the 8-bit V-PNM programmed for positive half period of a sinusoidal waveform.
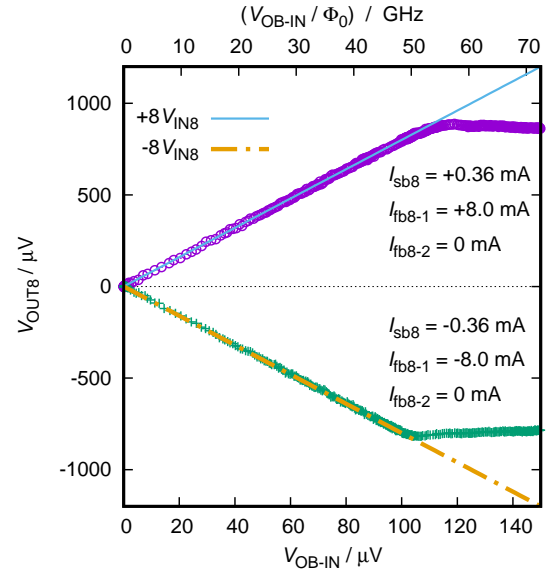

Fig. 4. Input–output characteristics of the $\pm$8-fold PS-DFQA measured using the over-biasing method. Two straight lines represented the ideal $V_{\text{OUT8}} = \pm 8 V_{\text{OB-IN}}$ relationships. In this measurement, one of two flux biases ($I_{\text{fb8-2}}$) was unused, because it had empirically been confirmed that DFQAs with multiplication factors less than twenty could be operated only with one flux bias.
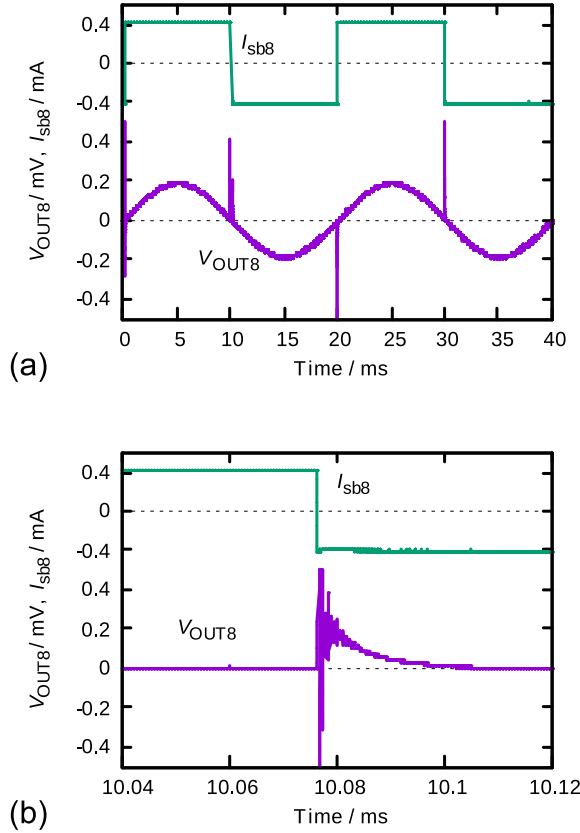
Fig. 5. (a) Sinusoidal voltage waveform synthesized by the 8-bit bipolar SFQ-PFM DAC. The bias current to the ± 8-fold PS-DFQA (I_{sb8}) is also plotted, whereas the digital input signals and flux bias currents are not shown. (b) Spike noise induced by polarity switching of the bias current.

input code was updated at every 39.1 μs ($= 1/25.6$ kHz). The polarity of the output voltage V_{OUT8} was correctly switched. The maximum and minimum output voltage were ± 0.19 mV, which agreed with the calculated value of $\pm 8 \cdot 255 \cdot 2.1 \times 10^{15}$ Wb $\cdot$ 43.94 MHz. That is, we succeeded to demonstrate bipolar output voltages of an SFQ-PFM DAC implemented with a PS-DFQA.

Unfortunately, although we programmed the code to switch the polarity during zero output periods, we confirmed spike noises at every polarity switching as shown in Fig. 5(b). Since spike noises were reduced by broadening rising/falling time of bias currents, this was likely due to limited bandwidths of our measurement set-up. Although coaxial cables were equipped between the probe head and the cold stage, only low-frequency connections were arranged from the coaxial cables to the chip through spring electrodes, a chip carrier, and bonding wires.

IV. CONCLUSION

We demonstrated an SFQ-based DAC generating bipolar output voltages. The key component was a PS-DFQA. Although the conventional DFQA generates bipolar output voltages by switching the bias polarity, its voltage multiplication factors for the positive and negative voltages were not identical. To solve this problem, we modified its circuit configuration and realized identical multiplication factors for

both positive and negative output voltages. The SFQ-PFM bipolar DAC comprised a dc/SFQ converter, an 8-bit V-PNM, and a ± 8-fold PS-DFQA integrated on a single chip. The output voltage was changed by the multiplication factor of the V-PNM, which was controlled by a data generator situated at room temperature. Sinusoidal bipolar voltage waveform of 0.38 mV$_{pp}$ was demonstrated using a reference signal source of 43.94 MHz, although spike noises were generated at the timing of polarity switching. Appropriate RF design should be implemented into the measurement set-up to eliminate spike noises.

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