Organic Ring Oscillators with Sub-200 ns Stage Delay Based on a Solution-Processed p-type Semiconductor Blend

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Organic Ring Oscillators with Sub-200 ns Stage Delay Based on a Solution-Processed p-type Semiconductor Blend

*Colin P. Watson, Beverley A. Brown, Julian Carter, John Morgan, and D. Martin Taylor**

High-frequency ring oscillators with sub-microsecond stage delay fabricated from spin-coated films of a specially formulated small-molecule/host-polymer blend are reported. Contacts and interconnects are patterned by photolithography with plasma etching used for creating vias and removing excess material to reduce parasitic effects. The characteristics of transistors with 4.6 µm channel length scale linearly with channel width over the range 60–2160 µm. Model device parameters extracted using Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model yield values of hole mobility increasing from 1.9 to 2.6 $cm^2 Vs^{-1}$ as gate voltage increased. Simulated and fabricated $V_{gs} = 0$ inverters predict that the technology is capable of fabricating 5-stage ring oscillators operating above 100 kHz. Initial designs operated mainly at frequencies in the range 250–300 kHz, due to smaller parasitic gate overlap capacitances and higher supply voltages than assumed in the simulations. A design incorporating graded inverter sizes operates at frequencies above 400 kHz with the best reaching 529 kHz. The corresponding stage delay of 189 ns is the shortest reported to date for a solution-processed p-type semiconductor and compares favorably with similar circuits based on evaporated small molecules. Significant further improvements are identified which could lead to the fabrication of digital circuits that operate at much higher bit rates than previously reported.

1. Introduction

Integrated circuits based on organic thin film transistors (OTFTs) were first reported over 15 years ago. The Philips team demonstrated a solution-processed 15-bit code generator[1] and Crone et al.[2] a vacuum-evaporated complementary technology for decoders and shift registers. Since then steady progress has been made in increasing both the speed and complexity of organic integrated circuits.[3–6] As seen in the original reports, the manufacturing processes divide naturally into two general approaches i.e., solution-processing and vacuum processing. In the former approach some or all transistor and circuit elements are deposited from solution and holds out the promise of low-cost, high-volume roll-to-roll (R2R) manufacture of circuits using, for example, inkjet[7] or gravure printing.[8] On the other hand, processes requiring vacuum evaporation of one or more component, or photolithography and dry-etching are more suited to batch-processing.

Progress has been, and continues to be made, in applying mass-printing R2R processes[9] with a range of logic circuits being demonstrated[10] albeit based on single-walled carbon nanotubes as the active material. High-speed metal patterning and barrier layer deposition are commercially used processes. R2R circuit fabrication based entirely on vacuum evaporation is, therefore, feasible.[11] For example, saturated-load unipolar ring oscillators (ROs) were produced in a R2R-compatible environment.[12] Although a stage delay of 46 µs was achieved at a high supply voltage, circuit performance was compromised by a nonoptimal design purposely limited to the resolution and registration capability of a high-speed metal printing process. Nevertheless, the stage delay achieved was much shorter than previously reported for ROs produced using *all-solution* mass-printing processes (**Table 1**).[13–15] This reflects the generally higher mobilities of vacuum-evaporated small-molecules[12] compared with solution-processed small-molecules.[16,17]

Other performance-degrading features of solution R2R-processes include a relatively thick dielectric layer and relatively poor resolution. The former leads to high operating voltages. The latter reduces operating speed by restricting the source–drain gap, i.e., the channel length, *L*, of the OTFTs to a minimum of about 30–40 µm. Achieving a resolution below ≈10 µm to improve device speed poses a significant near-term challenge for mass-printing processes. Relatively poor registration between different patterned layers is a further problem leading to undesirable parasitic effects.[12] It is not surprising, therefore, that the significant improvements in organic circuit performances have been demonstrated using the higher resolution approaches derived from silicon technology. At the most basic level, this is confined to patterning source–drain electrodes by photolithography to achieve channel lengths of 5 µm

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Table 1. Comparison of ring oscillator frequencies, f, and corresponding stage delays, t_D, achieved using both solution-processing and vacuum evaporation of the organic semiconductor.

Technology	Semiconductor	RO stages	L [μm]	f [kHz]	t_D [μs]	Reference
Mass-printed R2R unipolar	F8T2	7	100	0.004	17,900	[13]
Mass-printed R2R unipolar	F8T2	5	45	0.006	16,700	[14]
Mass-printed R2R unipolar	Arylamine copolymer	5	40	0.3	333	[15]
Vacuum R2R unipolar	DNTT	5	40	2.16	46.3	[12]
Spin-coated ambipolar	Ni dithiolene	5	5	0.35	286	[16]
Spin-coated ambipolar	PSeDPPBT	3	5	182	0.91	[18]
Spin-coated ambipolar	PDPP3T	5	5	42	2.38	[19]
Spin-coated unipolar	TIPS-pentacene/PS blend	11	4	31.4	1.45	[20]
Spin-coated unipolar	diF-TESADT	7	5	22	3.3	[21]
Spin-coated unipolar	diF-TESADT: polytriarylamine blend	7	1.5	100	0.712	[22]
Spin-coated unipolar	C_{16}IDT-BT	7	2.5	45	1.6	[23]
Inkjet complementary	PC12TV12T/P(ND12OD-T2)	5	5	80	1.25	[24]
Solution processed	Polymer	7	5	2.9	24.6	[5]
Evaporated unipolar	Pentacene	5	5	0.59	170	[25]
Evaporated unipolar	Pentacene	19	2	≈66	0.400	[4]
Evaporated unipolar	C10-DNTT	11	1	≈150	0.300	[26]
Evaporated unipolar	Pentacene	5	2	≈440[a)]	≈0.23[b)]	[27]
Evaporated complementary	Pentacene/C_{60}	5	2	200	0.500	[28]
Evaporated complementary	DPh-DNTT/ActivInk N1100	11	1	14.7	3.1	[29]
Evaporated complementary	Ph-PXX/ActivInk N3004	19	3	13.9	1.89	[30]
Inkjet unipolar	TIPS-pentacene	19	5	0.5	52.6	[17]
Inkjet complementary	SWCNT/ZTO	5	20	714	0.140	[31]
Spin-coated unipolar	*tru*-FLEX	5	4.6	529	0.189	Present work

[a)]This value is estimated from Figure 5 in reference[27] and is slightly higher than reported by the authors; [b)]calculated from the estimated frequency using $t_D = 1/2Nf$.

or less. In more advanced processes, minimization of parasitic effects and creation of vias for interconnects are achieved using dry (plasma) etching to pattern semiconductor and dielectric layers.[32] Such an approach benefits from good process control and significantly better device/circuit performance. It has been used, for example, for the fabrication of application-specific gate arrays[5] and even customized microprocessors[6] using inkjet printing to interconnect individual OTFTs or circuit elements.

Utilizing photolithography to fabricate TFTs based on 1–5 μm technology, especially when coupled with plasma processing, also allows the performance limits of organic circuits and constituent materials to be explored more fully. The main test circuit is usually the ubiquitous ring oscillator, comprising from 5 to as many as 19 inverter stages connected in series. While MHz operation[33] has been reported for single OTFTs, there are relatively few reports of organic ring oscillators showing stable operation above 100 kHz with stage delays less than 1 μs. Table 1 provides examples of values reported during the last 12 years for a range of technologies and materials.[4,5,12–31] From this list, only six reports[18,22,26–28,31] appear to meet the above benchmark and in two of these cases [18,22] the high frequency/short stage delay criterion was only achieved with supply voltages ≥50 V.

Myny et al.[4] have shown that a frequency even as low as 66 kHz from a 19-stage RO, corresponding to a stage delay of 400 ns, is sufficiently fast to enable an 8-bit RFID transponder to operate at 50 kb s^{-1}. Higher frequencies arising from shorter stage delays would allow even higher bit rates to be achieved.

Apart from the special case of the hybrid, complementary SWCNT/ZTO ring oscillator,[31] there are no reports of ROs incorporating *solution-processed* organic semiconductors operating above 200 kHz. This is surprising considering the numerous reports in the literature of solution-processable organic semiconductors, e.g., TIPS-pentacene,[34] C_{10}-DNTT,[35] blends of small molecules in host polymers,[22,36,37] and semiconducting co-polymers[23] with significantly greater mobilities than that of evaporated pentacene (typically ≈0.5 cm^2 Vs^{-1}[4]).

In the following, we present results showing, for the first time, that unipolar, 5-stage ROs produced from a spin-coated organic semiconductor blend comprising a small molecule in a semiconducting binder[38] (*tru*-FLEX, SmartKem Ltd.) can routinely operate in the 250–350 kHz range with the best operating at >500 kHz. These frequencies correspond to stage delays ranging from 400 to below 200 ns, matching the best achieved with evaporated organic semiconductors (see Table 1).

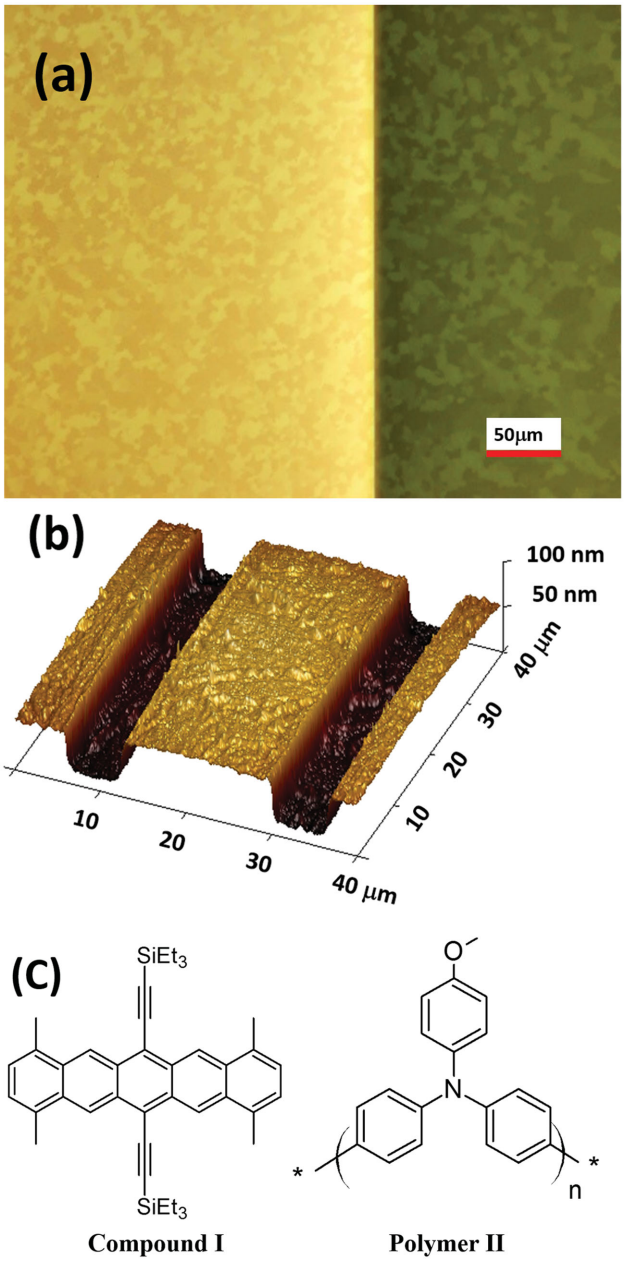

Figure 1. a) Optical micrograph through crossed polarizers showing similar blend morphology on both the gold electrode (bright region) and the substrate (darker region). b) AFM topographical image of the blend over a section of interdigitated source and drain electrodes (elevated regions), and channel confirm the similar morphology. c) Chemical structures of the small molecule 1,4,8,11-tetramethyl-6,13-bis-triethylsilyl ethynyl pentacene (compound I), and the amorphous polytriarylamine host polymer (polymer II).

2. Results and Discussion

2.1. Organic Semiconductor Blend

Previous reports on semiconducting, small molecule/host polymer blends[36,39] suggest that, when spin coated from solution, the small molecule phase separates to the air interface of the film. The cross-polar microscope image in **Figure 1**a shows this also to be the case in the present work. The small molecule forms a mosaic of randomly orientated polycrystalline domains/platelets ranging in size up to 10 s of microns on both the gold electrode and SU8-coated substrate. Reproducing consistently such morphology from substrate to substrate was achieved by careful tuning of the chemical structures of the small molecule, 1,4,8,11-tetramethyl-6,13-bis-triethylsilyl ethynyl pentacene (compound I), and the amorphous polytriarylamine host polymer (polymer II), combined with substrate pre-treatment, choice of solvent, and optimized spin conditions. With platelet dimensions generally larger than transistor channel length, in our case 4.6 μm, the influence of grain boundaries is minimized resulting in consistent transistor performance.

The atomic force microscope (AFM) topographical image in Figure 1b confirms the similar morphologies both on the gold electrode and in the channel region of the device. The root-mean-square (RMS) roughness of the organic semiconductor (OSC) layer was ≈1.47 nm over an area of 646 μm^2 when on gold and ≈2.23 nm over an area of 201 μm^2 in the channel.

2.2. Five Mask Fabrication Process

After optimizing the spin-coating conditions, TFTs, inverters and 5-stage ROs based on the bottom-contact/top-gate transistor configuration were produced using a 5-mask process. The process flow diagram is shown in **Figure 2** with full fabrication details given in Section 4. Photolithography was used to define electrode geometries; for the results presented here, the channel length, L, was 4.6 μm. The source/drain electrodes were plasma cleaned and treated with a self-assembled monolayer (SAM) prior to spin coating a 20 nm thick layer of the semiconducting ink. The organic gate insulator (OGI) was a 300 nm thick, spin-coated film of Cytop giving a capacitance per unit area of 6.2 nF cm^{-2}. Patterning of the semiconductor and insulator layers to (a) reduce parasitic effects and (b) create vias was achieved using photolithography and an oxygen plasma etch.

2.3. TFT Characteristics

For initial screening of materials and process conditions, the standard equation for describing the electrical characteristics of a thin film transistor in the linear regime was used, i.e.

$$I_D = \frac{W}{L}\mu C_i (V_G - V_T) V_D \quad (1)$$

where I_D is the source–drain current, W and L are the channel width and length respectively, μ is the carrier mobility, C_i is the capacitance per unit area of the gate dielectric, and with V_G, V_D, and V_T are the gate, drain, and threshold voltages respectively. **Figure 3**a shows the width-normalized transfer plots obtained in the linear regime (V_D = –2 V) for 12 OTFTs with channel widths, W, ranging from 60 to 2160 μm. As expected, all the characteristics superimpose showing that devices are linear in W but also, more importantly, follow similar and reproducible

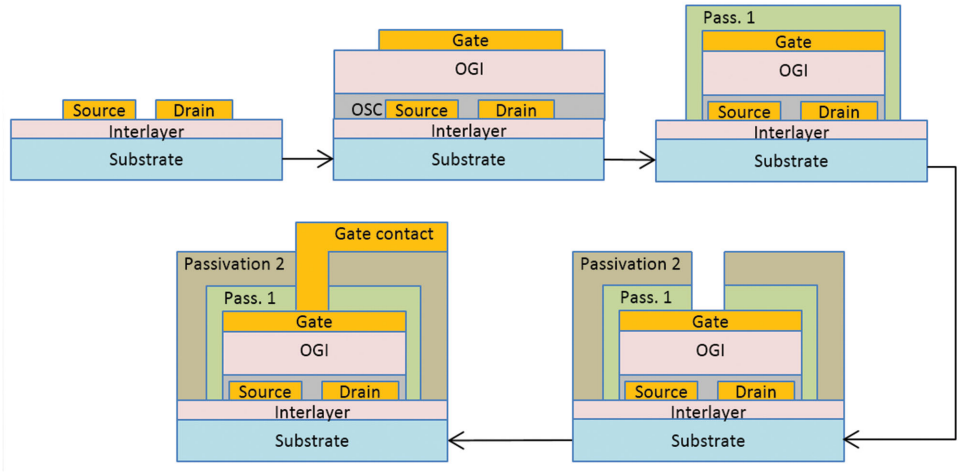

Figure 2. Flow diagram for the 5-mask process used to fabricate TFTs, inverters and ring oscillators based on the bottom-contact-top-gate structure. All electrodes and interconnects were defined photolithographically in gold. Both the organic semiconductor blend and the gate insulator (Cytop) were spin-coated layers and an oxygen plasma used to remove excess material and for creating vias.

behavior over a wide range of sizes. For all devices, the V_G-dependent mobility calculated from

$$\mu = \frac{L}{WC_i V_D} \times \frac{\partial I_D}{\partial V_G} \tag{2}$$

rises to almost 3 $cm^2\ Vs^{-1}$. The subthreshold slope is ≈1.5 V $decade^{-1}$ and the on–off current ratio $\approx 10^8$ but falling to $\approx 10^7$ in the smaller devices: the true off currents in the smaller devices are below the 1 pA detection limit of our measurement system.

2.4. TFT Parameter Extraction

For subsequent circuit design, Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model (Level = 37)[40] was used for parameter extraction. The model operates within a framework based on variable range hopping and percolation concepts leading to an effective mobility, μ_{FET}, given by

$$\mu_{FET} = \mu_{ACC}\left[\frac{V_G - V_T}{V_{ACC}}\right]^{\gamma} = \mu_{FET_0}\left[V_G - V_T\right]^{\gamma} \tag{3}$$

where μ_{ACC} defines the mobility at the onset of strong channel accumulation, generally assumed to be the band mobility. As this is not necessarily the case, a fitting parameter V_{ACC} is introduced to adjust the mobility to a value μ_{FET0}, the effective low-field mobility of the device. (In our simulations V_{ACC} is assumed equal to unity so that the values extracted for μ_{ACC} here give directly the low-field mobility). The power–law dependence, represented by γ, reflects the dependence of mobility on trap state occupancy in the channel. For ideal device behavior $\gamma = 0$. Other key parameters extracted using the UOTFT model are listed in **Table 2**. V_0 is the characteristic voltage of the carrier density of states including the effects of interface states and λ a measure of the output conductance in saturation. M_{SAT} and A_{SAT} are essentially shaping parameters, the former providing a smooth transition between the linear and saturation regions, the latter modulating the behavior of the output characteristic at the onset of saturation. I_O is the parasitic source–drain leakage saturation current and σ_0 the minimum bulk conductance, both of which contribute to the transistor off current. R_S and R_D represent series resistances, which may include both contact and bulk semiconductor resistances at the source/drain contacts respectively.

Figure 3b,c respectively show the fits obtained to the width-normalized output and transfer characteristics for three different devices for which $W = 720$ (device 4.10), 360, and 120 µm. The key parameter values are given in Table 2. (The full parameter set is given in Table S1 in the Supporting Information). The fit to all three devices provided by the optimized model for device 4.10 is excellent over a wide range of operating voltage and device size. Of particular interest, is that the low-field hole mobility $\mu_{ACC} \approx 1.9\ cm^2\ Vs^{-1}$ with the actual mobility rising to $\approx 2.6\ cm^2\ Vs^{-1}$ at higher voltages owing to the nonzero value of γ. In the software version used here, σ_0 automatically scaled linearly with W for the different device sizes. However, it was found necessary to scale manually the values of R_S and R_D to reflect their inverse dependence on W. We attribute their nonzero values to edge injection into the semiconductor layer owing to the particular geometry of the devices, i.e., the OSC layer (≈20 nm thick) was thinner than the ≈50 nm gold electrodes onto which it was deposited (Figure 1b). The width normalized off currents in the smallest device were higher than predicted by simulation and suggest that the true off currents in these devices were an order of magnitude lower than the 1 pA detection limit of the measurement system.

2.5. $V_{gs} = 0$ Inverters

The high positive turn-on voltages (≈15 V) seen in the transfer plots in Figure 3 result in "normally on" transistors suitable for use in inverters operating in $V_{gs} = 0$ mode,

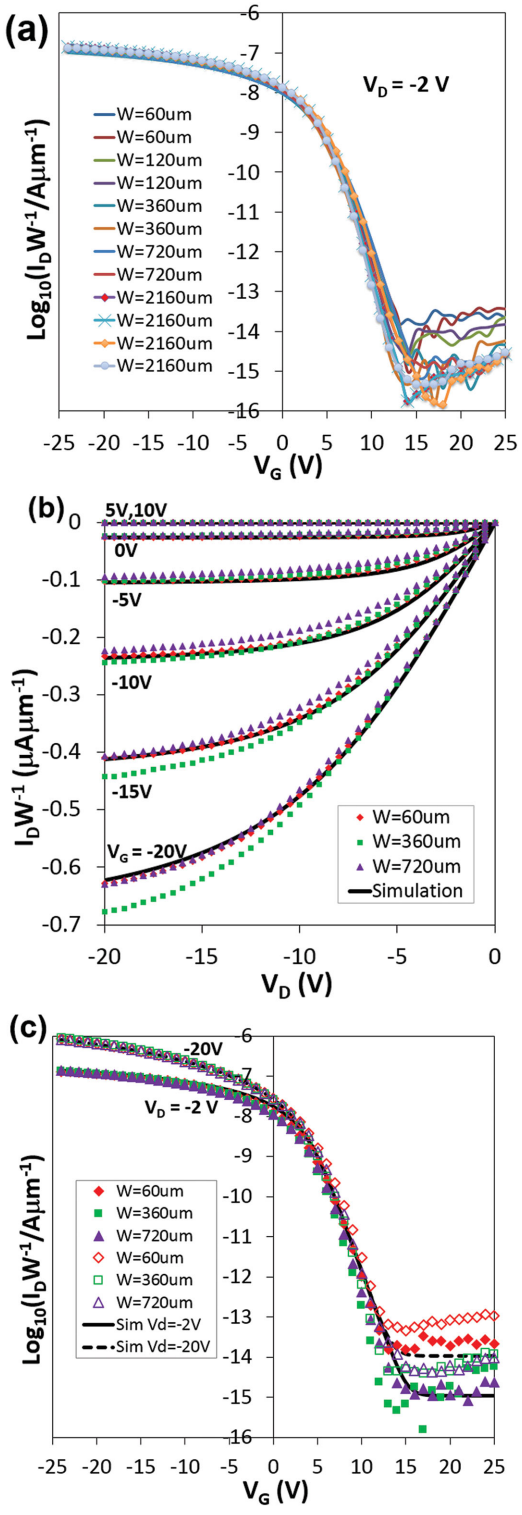

Figure 3. a) Width-normalized transfer characteristics obtained in the linear regime ($V_D = -2$ V) for 12 OTFTs with a range of channel widths, W. b) Output and c) transfer characteristics obtained from a subset of the OTFTs with $W = 60$, 360, and 720 µm. The transfer data was obtained for both the linear ($V_D = -2$ V, filled points) and saturation ($V_D = -20$ V, hollow points) regimes. The simulated characteristics were based on the model card (Table 2 and S1, Supporting Information) developed for device 4.10 (W = 720 µm). For all devices $L = 4.6$ µm.

Table 2. Key parameter values (given to three significant figures) in the model card used to derive the simulated plots for Device 4.10. The same card with R_S and R_D adjusted for different device widths was also used to fit devices for which W = 360 µm and 120 µm (see text for details). The full model card is given in Table S1 in the Supporting Information.

Parameter	Value	Parameter	Value
W [µm]	720	γ	0.100
L [µm]	4.6	λ [S]	0
C_i [nF cm^{-2}]	6.20	M_{SAT}	2.01
V_T [V]	4.37	A_{SAT}	0.892
V_O [V]	0.783	σ_0 [fS]	2.40
V_{ACC} [V]	1	R_S [kΩ]	4.17
μ_{ACC} [cm^2 V^{-1}s^{-1}]	1.89	R_D [kΩ]	1.37

i.e., inverters in which the gate of the load TFT is connected to the source electrode (see inset **Figure 4**a). To aid circuit design prior to fabrication, the response of such an inverter was simulated using the model card derived above for device 4.10 but with R_S and R_D scaled appropriately. Simulated voltage transfer and gain plots for an inverter in which W(load)/W(driver) = (2160 µm)/(360 µm) = 6 and operating from a −20 V supply rail is given in Figure 4a. The simulations show good switching behavior, high gain (≈7) and a noise margin ≈2.9 V.

Measurements made on four nominally identical inverters in which W(load)/W(driver) = (360 µm)/(90 µm) are given in Figure 4b. Although in this case the inverters were powered from a +20 V supply, as can be seen from the inset diagrams, both circuit configurations are identical. In the circuit in Figure 4b, all voltages are simply shifted 20 V to more positive values than those in Figure 4a. To confirm this, simulations were undertaken for the second case with V_{DD} = +20 V. These were again based on model card 4.10 and show reasonable agreement with measurements. The trip point in all cases was ≈5 V below the supply voltage (Figure 4b). In the best case (inverter 1) the noise margin is close to prediction i.e., ≈2 V, (see Figure S1 in the Supporting Information) and in the worst case (inverter 4) only falls to ≈1.3 V. However, the simulated gain is overestimated significantly. This is not surprising since the TFTs used for parameter extraction were made on different substrates and at different times to the inverter. Until the process flow is fully optimized and highly controlled, differences may be expected in OTFT characteristics and circuit performance. We have shown in separate simulations that relatively minor statistical variations in TFT characteristics can lead to the differences observed here. For example, when using a driver transistor from a different batch of inverters for the parameter extraction and subsequently using the new model card (Table S2, Supporting Information) to simulate the inverters, much better agreement was possible (see Figures S2 and S3 in the Supporting Information).

Although the inverter simulation in Figure 4a suggested lower gain than in Figure 4b, in view of its higher noise margin, subsequent simulations and measurement of dynamic responses focused on the former design. For the simulations, parasitic gate–source (C_{gs}) and gate–drain (C_{gd}) overlap capacitances (assumed equal) were included in the model. All

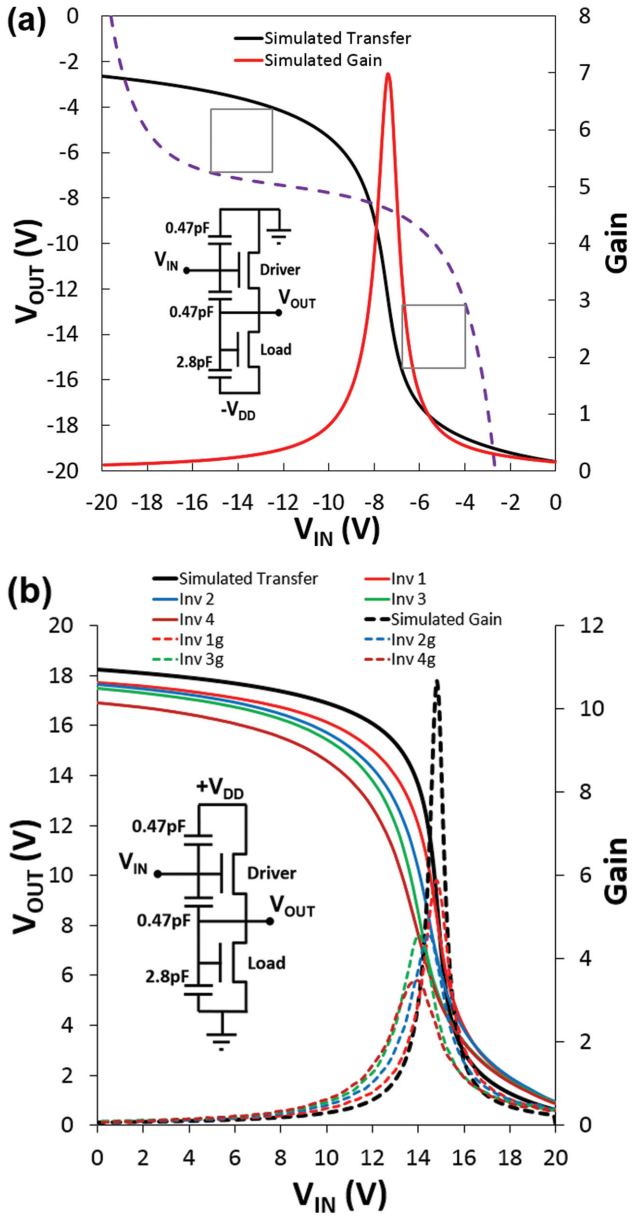

Figure 4. a) Simulated voltage transfer characteristic and gain of the V_{gs} = 0 inverter shown in the inset in which W(load) = 2160 µm and W(driver) = 360 µm. The expected noise margin is ≈2.7 V. b) Measured transfer characteristics (solid curves) and gain (dotted curves) of four V_{gs} = 0 inverters in which W(load) = 360 µm, W(driver) = 90 µm. The heavier black curves are the simulated plots. In all the simulations, TFTs were described using transistor model 4.10 (Table 2 and S1, Supporting Information) but with R_S and R_D scaled inversely with W. In all cases L = 4.6 µm and $|V_{DD}|$ = 20 V.

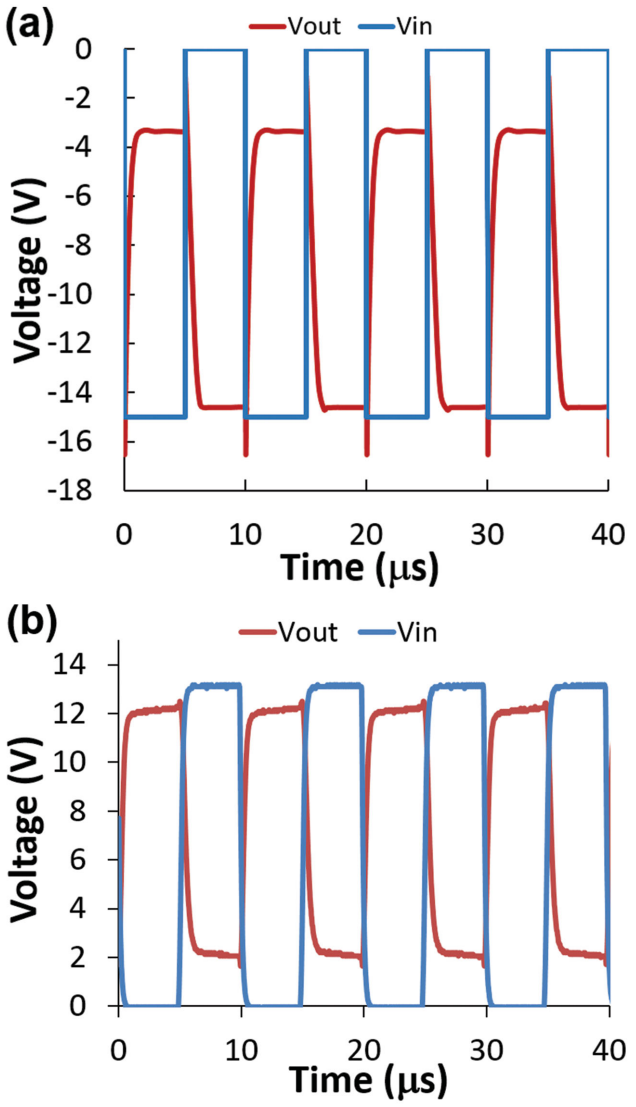

Figure 5. a) Simulated and b) measured response of a V_{gs} = 0 inverter to a 100 kHz square wave. The simulation used TFT model 4.10 (Table 2 and S1, Supporting Information). In both cases W(driver) = 360 µm, W(load) = 2160 µm and $|V_{DD}|$ = 15 V. Capacitances 2.8 and 0.47 pF were also included as shown in the inset of Figure 4 to simulate the effect of parasitic gate–source and gate–drain overlap capacitances.The function generator used for the measurements had a maximum square-wave amplitude of 13 V at 100 kHz.

transistors fabricated for this study had gate electrodes overlapping completely the interdigitated source and drain electrodes (see Figure 2). The parasitic overlap capacitances were assumed, therefore, to have areas equal to that of the source (C_{gs}) and drain (C_{gd}) electrode areas. Based on the transistor arrays used for the measurements in Section 2.3, values of 0.47 and 2.8 pF were believed to be reasonable initial estimates for the drive and load transistors respectively.

The simulated and measured responses to a 100 kHz input square wave are shown in **Figure 5** for a supply voltage $|V_{DD}|$ = 15 V. For the simulation, the amplitude of the input square wave was also 15 V. Although simulations were based on a negative supply rail, for the measurements, a positive supply voltage was more suited to the picoprobe used in the measurement. However, the maximum amplitude of the input voltage from the function generator at 100 kHz was only 13 V. Nevertheless, the similarity between the simulated and measured responses is obvious. Simulated and measured stage delays, t_D = (0.5t (rise) + 0.5t (fall)) ≈1 µs, show that the inverter is capable of MHz operation.

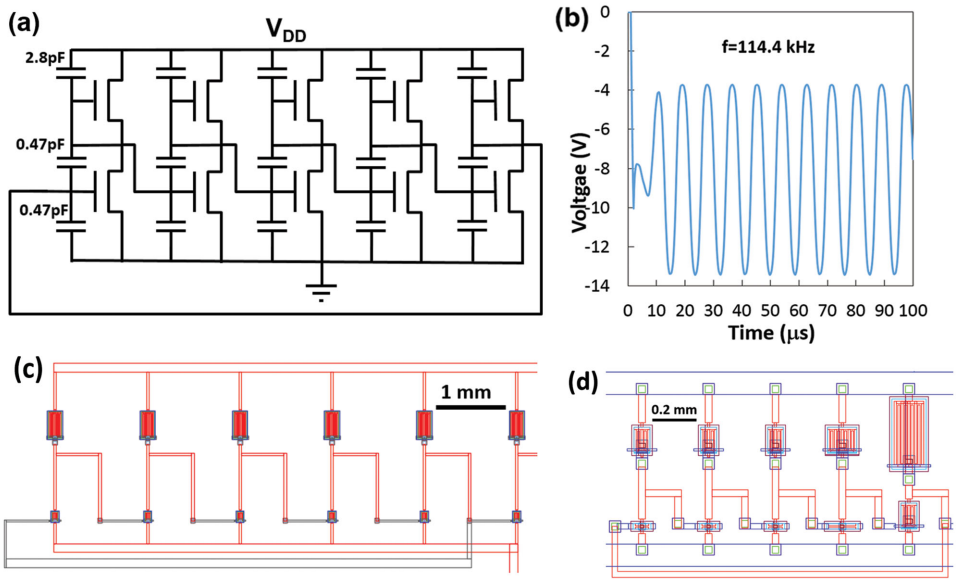

Figure 6. a) 5-stage ring oscillator circuit, including parasitic capacitances, in which L = 4.6 μm, W(driver) = 360 μm and W(load) = 2160 μm. b) The simulated output using TFT model 4.10 and V_{DD} = –15 V. Also shown are the CAD diagrams for c) uniform and d) graded oscillators.

2.6. Ring Oscillators

Both the simulations and measurements in the previous section, suggest that a 5-stage ring oscillator (**Figure 6**a) built using the same inverter design should oscillate at frequencies, f, in excess of 100 kHz (from simulation, $f = 1/2\ Nt_D$ = 108.7 kHz, where N is the number of stages). This is confirmed in the simulation in Figure 6b which shows an oscillation frequency of 114.4 kHz for $|V_{DD}|$ = 15 V and close to prediction from the inverter response.

To compare directly with simulation, a batch of thirty ROs was fabricated in which W(load) = 2160 μm and W(driver) = 360 μm. An additional batch of thirty ROs was prepared in which W(driver) was reduced to 270 μm. The CAD diagram showing the circuit layout is shown in Figure 6c. Each batch was divided equally into two groups; one in which the source/drain electrodes were simply plasma-cleaned while in the other, the plasma clean was followed by treatment with a self-assembled monolayer (SAM). The overall yield was ≈80%. To minimize possible loading effects on the ROs from the measurement probe, an additional OTFT inverter stage, identical to those forming the oscillator, was added in series to act as a buffer between the feedback loop and the measurement probe. Nevertheless, it was found necessary to increase $|V_{DD}|$ to at least 20 V to initiate stable oscillations with 25–30 V being typical.

As seen in the histogram in **Figure 7**a, the output frequencies were also significantly higher than predicted by simulation, but with little dependence on the size of the driver TFT. Most ROs oscillated at a frequency between 225 and 300 kHz with 12 (≈24%) operating at higher frequencies. The highest frequency observed, 414 kHz, is plotted in Figure 7b. (Figure S4 in the Supporting Information is a screen shot of the actual signal). Although the circuits with SAM-treated source/drain electrodes showed a marginally tighter frequency distribution (see Figure S5 in the Supporting Information), the highest frequencies were observed in circuits which had undergone only an additional plasma clean. This suggests that one contribution to the spread of oscillation frequencies may lie in the "state" of the source–drain electrodes, and especially of the electrode edges where charge injection and collection mainly occurs. Other contributions are likely to arise from process variations within and between substrates, including gate registration errors and their effects on parasitic capacitance. For example, a previous simulation study[12] showed that gate–drain parasitic capacitance degraded RO frequency more than gate–source capacitance.

That the observed operating frequencies were so much higher than suggested by simulation may, to some extent, be explained by the higher supply voltage required for stable operation. The main reason, though, was traced to the values assumed for the parasitic gate capacitances. A study of the gate overlap areas in the CAD drawings prepared for circuit fabrication, e.g., Figure 6c,d, suggested that, based on a 10 μm finger width for the source/drain electrodes, more realistic values for the associated parasitic capacitances would be 1.41 and 0.369 pF for the load and driver TFTs respectively. These values are much lower, therefore, than those assumed (2.8 and 0.47 pF).

The inverter used for the measurements in Figure 5b had the same dimensions as those in the ring oscillators. Accordingly, parasitic capacitances in the actual device would have been lower than assumed in the simulation in Figure 5a. The good agreement between simulation and measurement in Figure 5 is now seen to be a coincidence. The output rise and fall times estimated from measurement do not represent the true inverter performance but are compromised by the rise and fall times of the function generator which, as noted above, was operating at its limit.

To reduce the footprint of the oscillators, 5-stage ROs were also fabricated in which the fifth inverter stage also acted

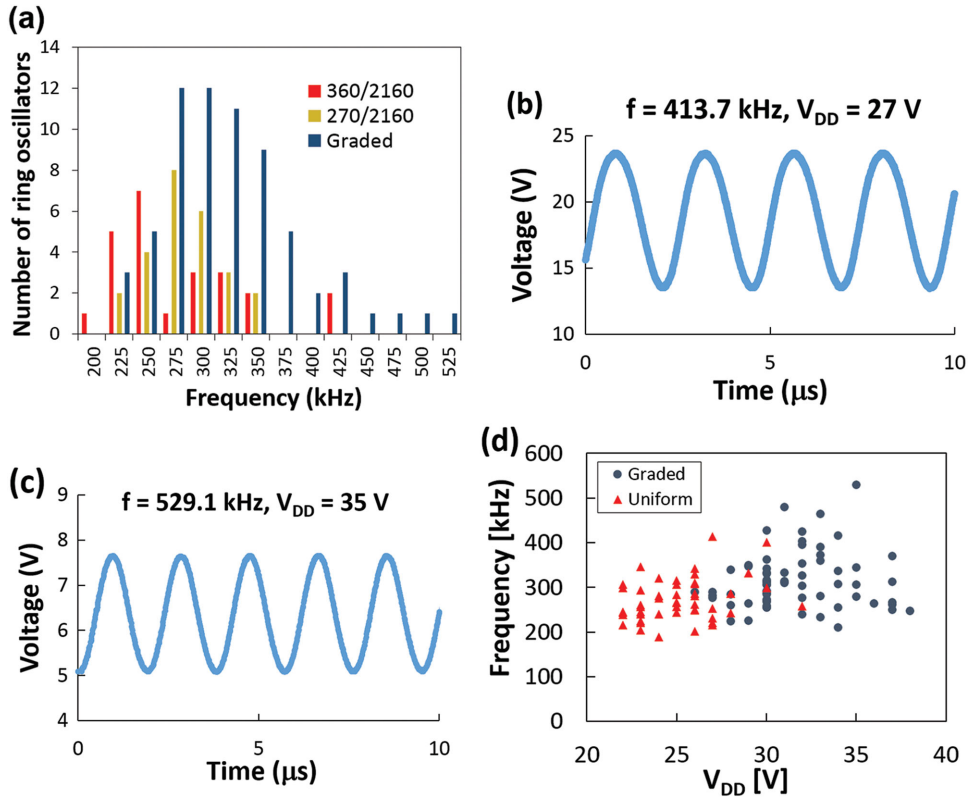

Figure 7. a) Histogram showing the number of fabricated oscillators with output frequencies in the 25 kHz band up to the indicated frequency. For two sets of oscillators W(load) = 2160 µm but with different driver sizes (W(driver) = 270 or 360 µm). For comparison are the results from 5-stage graded oscillators (see Figure 6d). Also shown are the highest frequency signals measured from b) uniform and c) graded ring oscillators. d) RO frequency versus the minimum supply voltage, V_{DD}, required for stable operation.

as the buffer. These oscillators were again based on OTFTs with a channel length of 4.6 µm but this time, inverter stages with graded sizes were used as seen in Figure 6d. In the first three stages, W(load) = 360 µm and W(driver) = 60 µm. In the fourth stage the respective values were 720 and 120 µm and in the final stage 2160 and 360 µm i.e., identical to the inverters in Figure 6c. The opportunity was taken also to reduce the inter-stage separation thus reducing the circuit footprint to ≈1.4 mm^2 in contrast to ≈20 mm^2 for the "uniform" oscillators. The "graded" ROs, however, required supply voltages in excess of ≈25 V to achieve stable oscillation. The operating frequencies of sixty-six such oscillators are also plotted in the histogram in Figure 7a. In general, the "graded" ROs oscillate at higher frequencies than our initial design; more than 50% oscillated above 300 kHz. The highest signal frequency observed from the graded oscillators was 529 kHz and is plotted in Figure 7c with the screenshot of the actual signal given in Figure S6 in the Supporting Information.

The shorter, average stage delay (now down to 189 ns) compared with the initial, uniform RO designs is probably due to the higher supply voltage required to sustain oscillation. Despite the large scatter in operating frequencies, Figure 7d suggests a general increase in frequency with V_{DD}, at least up to ≈35 V, consistent with the dependence of intrinsic cut-off frequency, f_i, of ideal transistors on source–drain voltage, V_D,[41] i.e., $f_i = \mu V_D/2\pi L^2$ if operating in the linear regime. However, transistors generally operate in, or close to saturation in which case they operate as constant current sources dependent on V_G but independent of V_D so that $f_i = \mu(V_G - V_T)/2\pi L^2$. While V_G may be expected to increase with increasing supply voltage, V_{DD}, the exact relationship will depend on many factors. For $V_{gs} = 0$ inverters a particular limitation arises in that $V_G = 0$ V for the load transistor and operation is only weakly dependent on V_D, as seen in the transfer curves in Figure 3c. It is also well recognized that other factors e.g., parasitic gate overlap capacitances and contact resistances can significantly degrade transistor frequency response.[42] Although f_i is an important factor, inverter stage delays also depend on the relative conductances of driver and load transistors, on parasitic interconnect capacitances and load impedance of any following stage. In the graded RO, there will be a reduction in parasitic capacitance resulting from shorter interconnect lengths and a reduced capacitive loading experienced by the feedback loop. Connecting the picoprobe directly to the feedback loop presented a much lower capacitance (0.1 pF) than the buffer inverter in Figure 6b.

Interestingly, in Figure 7d, where data points overlap, the performance of uniform and graded oscillators is indistinguishable suggesting that capacitances have scaled proportionally with decreasing device size. For V_{DD} greater than ≈35 V there is a tendency for operating frequency to saturate, and even

decrease, indicative of the increasing influence of contact resistance at higher device currents which leads to a decrease in the effective hole mobility.[42,43]

Nevertheless, the present study reports the highest frequencies observed for unipolar ring oscillators based on a spin-coated organic semiconductor. Furthermore, the stage delays are comparable with the shortest reported[27] for evaporated pentacene ROs based on 2 μm channel lengths (4.6 μm in the present work) and 2 μm wide source/drain interdigitated electrode fingers to reduce parasitic gate capacitances. In our case, reducing the source–drain finger widths from the present 10 to 2 μm, would result in at least a factor 2 reduction in stage delay[27] to well below 100 ns. Thus, frequencies well above 1 MHz should be readily achievable.

3. Conclusion

We have demonstrated a 5-stage ring oscillator with stage delay >200 ns operating above 0.5 MHz, the highest frequency reported to date for unipolar ROs based on a solution-processed organic semiconductor. This was achieved by synthesizing an organic small molecule and a host polymer which, when formulated as a blend (*tru*-FLEX) in tetralin, produced a high performance p-type semiconductor ink. Following detailed morphological studies, appropriate spin coating and substrate conditions were identified which resulted in thin films with reproducibly good electrical properties. In the deposited films the small molecule phase-separated to the air/film interface forming a spatially uniform "mosaic" of small crystal platelets.

Thin film transistors with 4.6 μm channel length and channel widths ranging from 60 to 2160 μm made from the blend were modeled using Silvaco's UOTFT software yielding a low-field mobility of 1.89 $cm^2\ Vs^{-1}$ which increased to ≈2.6 $cm^2\ Vs^{-1}$ at higher gate voltages. A model card based on the extracted parameters was used to model both the static and dynamic performances of $V_{gs} = 0$ inverters with reasonable accuracy. Based on these results, a ring oscillator was designed with predicted operational frequency >100 kHz. Fabricated ring oscillators with identically sized inverter stages and an additional buffer stage operated at much higher frequencies, mainly in the range 250–300 kHz but with ≈25% operating at even higher frequencies in the range up to 414 kHz. The higher operating frequencies achieved in practice compared with simulations is attributed to smaller parasitic gate capacitances in the fabricated devices and the higher supply voltages needed for stable operation of the oscillators. ROs with graded inverter sizes and integral buffer stage operated at slightly higher frequencies; more than 50% oscillated above 400 kHz with the highest measured at 529 kHz, corresponding to an average stage delay of 189 ns. These higher operating frequencies are attributed to the higher operating voltages.

Other semiconductor blends under development have shown mobilities that are significantly higher than reported here. Further design improvements are also possible, e.g., reducing channel length and gate overlap capacitances as well as further optimizing interconnect layout. With such improvements, ring oscillators operating well above 1 MHz are clearly attainable using the 5-mask process and the *tru*-FLEX series of inks. The resulting reduction in stage delay suggests that the technology developed has the potential to produce digital circuits operating at much higher bit rates than hitherto reported for organic semiconductors.

4. Experimental Section

The organic semiconductor ink used in this study (*tru*-FLEX, SmartKem Ltd., UK)[38] was a high mobility small molecule, 1,4,8,11-tetramethyl-6,13-bis-triethylsilyl ethynyl pentacene (compound I), formulated with a matched amorphous, polytriarylamine homopolymer (polymer II). The polycrystalline small molecule and semiconducting binder were dissolved in tetralin at a total solids loading of 1.7% weight:weight.

TFTs, inverters and 5-stage ROs based on the bottom-contact-top-gate transistor configuration were produced on 100 mm × 100 mm substrates using a 5-mask process. The process flow diagram is shown in Figure 2. The source/drain electrodes and connecting tracks were patterned photolithographically to yield a channel length of 4.6 μm in a 50 nm thick gold film (including a thin titanium keying layer) evaporated onto SU8-planarized Corning Eagle glass substrates. The "graded" ring oscillators were fabricated on SU8-planarized polyethylene naphthalate films.

Following a plasma clean, the source–drain electrodes were functionalized with a pentafluorobenzenethiol (PFBT) self-assembled monolayer. A 20 nm thick film of the semiconductor was immediately deposited over the substrate by spin coating at 1750 rpm, followed by a 300 nm thick, spin-coated film of Cytop (Asahi Glass Chemicals, Japan) to act as the gate dielectric. Gold gate electrodes were then evaporated and photo-patterned. These electrodes acted as etch masks for the O_2 plasma removal of excess areas of semiconductor and insulator from the substrates in order to reduce parasitic effects in the final devices. Then, two passivation layers were deposited from orthogonal solvents and patterned photolithographically to form vias. Following the deposition of another gold film, gate layer interconnects were defined in a final photolithographic step.

The morphology of spin-coated films was studied with a Nikon Eclipse Me-600 optical microscope fitted with cross polarizers and a Nanoman V atomic force microscope operating in tapping mode. Electrical characterization was undertaken in a Wentworth semi-automatic probe-station housed in an earthed metal enclosure which reduced the noise floor for measurements down to ≈1 pA. OTFT and static inverter characteristics were measured with a Keithley model 4200 SCS parameter analyzer. Dynamic measurements were made using a Picoprobe (Model 12C or 34A, GBB Industries Inc.) connected to a digital oscilloscope. OTFT parameter extraction and generation of a TFT model card was undertaken using Silvaco's UOTFT software, Level = 37. The extracted model card was then used in Silvaco Smartspice for circuit simulations.

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[1] a) C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, D. M. de Leeuw, *Appl. Phys. Lett.* **1998**, *73*, 108; b) G. H. Gelinck, T. C. T. Geuns, D. M. de Leeuw, *Appl. Phys. Lett.* **2000**, *77*, 1487.

[2] B. Crone, A. Dodabalapur, Y.-Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, W. Li, *Nature* **2000**, *403*, 521.
[3] a) G. H. Gelinck, H. Edzer, A. Huitema, E. van Veenendaal, E. Cantatore, L. Schrijnemakers, J. B. P. H. van der Putten, T. C. T. Geuns, M. Beenhakkers, J. B. Giesbers, B.-H. Huisman, E. J. Meijer, E. M. Benito, F. J. Touwslager, A. W. Marsman, B. J. E. van Rens, D. M. de Leeuw, *Nat. Mater.* **2004**, *3*, 106; b) P. F. Baude, D. A. Ender, M. A. Haase, T. W. Kelley, D. V. Muyres, S. D. Theiss, *Appl. Phys. Lett.* **2003**, *82*, 3964; c) M.-J. Spijkman, K. Myny, E. C. P. Smits, P. Heremans, P. W. M. Blom, D. M. de Leeuw, *Adv. Mater.* **2011**, *23*, 3231; d) K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, *IEEE J. Solid-State Circuits* **2012**, *47*, 284.
[4] K. Myny, S. Steudel, S. Smout, P. Vicca, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, J. Genoe, W. Dehaene, P. Heremans, *Org. Electron.* **2010**, *11*, 1176.
[5] A. Sou, S. Jung, E. Gili, V. Pecunia, J. Joimel, G. Fichet, H. Sirringhaus, *Org. Electron.* **2014**, *15*, 3111.
[6] K. Myny, S. Smout, M. Rockele, A. Bho olokam, T. H. Ke, S. Steudel, B. Cobb, A. Gulati, F. G. Rodriguez, K. Obata, M. Marinkovic, D. V. Pham, A. Hoppe, G. H. Gelinck, J. Genoe, W. Dehaen, P. Heremans, *Scientific Rep.* **2014**, *4*, 7398.
[7] a) H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, E. P. Woo, *Science* **2000**, *290*, 2123; b) T. Kawase, H. Sirringhaus, R. H. Friend, T. Shimoda, *Adv. Mater.* **2001**, *13*, 1601; c) B. K. C. Kjellander, W. T. T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans, G. H. Gelinck, *Org. Electron.* **2013**, *14*, 768; d) D. Tobjörk, N. J. Kaihovirta, T. Mälelä, F. S. Pettersson, R. Österbacka, *Org. Electron.* **2008**, *9*, 931; e) S. Chung, S. O. Kim, S.-K. Kwon, C. Lee, Y. Hong, *IEEE Electron Device Lett.* **2011**, *32*, 1134.
[8] A. de la F. Vornbrock, D. Sung, H. Kang, R. Kitsomboolloha, V. Subramanian, *Org. Electron.* **2010**, *11*, 2037.
[9] R. R. Søndergaard, M. Hösel, F. C. Krebs, *J. Poly. Sci. B: Poly. Phys.* **2013**, *51*, 16.
[10] a) J. Noh, S. Kim, K. Jung, J. Kim, S. Cho, G. Cho, *IEEE Electron Device Lett.* **2011**, *32*, 1555; b) J. Noh, K. Jung, J. Kim, S. Cho, G. Cho, *IEEE Electron Device Lett.* **2012**, *33*, 1574; c) J. Noh, M. Jung, K. Jung, J. Lee, J. Kim, S. Lim, D. Kim, Y. Choi, Y. Kim, V. Subramanian, G. Cho, *IEEE Electron Device Lett.* **2011**, *32*, 638.
[11] D. M. Taylor, *Semicond. Sci. Technol.* **2015**, *30*, 054002.
[12] E. R. Patchett, A. Williams, Z. Ding, G. Abbas, H. E. Assender, J. J. Morrison, S. G. Yeates, D. M. Taylor, *Org. Electron.* **2014**, *15*, 1493.
[13] A. C. Huebler, F. Doetz, H. Kempa, H. E. Katz, M. Bartzsch, N. Brandt, I. Hennig, U. Fuegmann, S. Vaidyanathan, J. Granstrom, S. Liu, A. Sydorenko, T. Zillger, G. Schmidt, K. Preissler, E. Reichmanis, P. Eckerle, F. Richter, T. Fischer, U. Hahn, *Org. Electron.* **2007**, *8*, 480.
[14] A. C. Hübler, G. C. Schmidt, H. Kempa, K. Reuter, M. Hambsch, M. Bellmann, *Org. Electron.* **2011**, *12*, 419.
[15] J.-M. Verilhac, M. Benwadih, A.-L. Seiler, S. Jacob, C. Bory, J. Bablet, M. Heitzman, J. Tallal, L. Barbut, P. Frère, G. Sicard, R. Gwoziecki, I. Chartier, R. Coppard, C. Serbutoviez, *Org. Electron.* **2010**, *11*, 456.
[16] T. D. Anthopoulos, S. Setayesh, E. Smits, M. Cölle, E. Cantatore, B. de Boer, P. W. M. Blom, D. M. de Leeuw, *Adv. Mater.* **2006**, *18*, 1900.
[17] B. K. C. Kjellander, W. T. T. Smaal, K. Myny, J. Genoe, W. Dehaene, P. Heremans, G. H. Gelinck, *Org. Electron.* **2013**, *14*, 768.
[18] A. J. Kronemeijer, E. Gili, M. Shahid, J. Rivnay, A. Salleo, M. Heeney, H. Sirringhaus, *Adv. Mater.* **2012**, *24*, 1558.
[19] W. S. C. Roelofs, S. G. J. Mathijssen, J. C. Bijleveld, D. Raiteri, T. C. T. Geuns, M. Kemerink, E. Cantatore, R. A. J. Janssen, D. M. de Leeuw, *Appl. Phys. Lett.* **2011**, *98*, 203301.
[20] M. H. Choi, B. S. Kim, J. Jang, *IEEE Electron Dev. Lett.* **2012**, *33*, 1571.
[21] a) D. J. Gundlach, J. E. Royer, S. K. Park, S. Subramanian, O. D. Jurchescu, B. H. Hamadani, A. J. Moad, R. J. Kline, L. C. Teague, O. Kirillov, C. A. Richter, J. G. Kushmerick, L. J. Richter, S. R. Parkin, T. N. Jackson, J. E. Anthony, *Nat. Mater.* **2008**, *7*, 216; b) S. K. Park, D. A. Mourey, S. Subramanian, J. E. Anthony, T. N. Jackson, *IEEE Electron Dev. Lett.* **2008**, *29*, 1004.
[22] J. Smith, R. Hamilton, M. Heeney, D. M. de Leeuw, E. Cantatore, J. E. Anthony, I. McCulloch, D. D. C. Bradley, T. D. Anthopoulos, *Appl. Phys. Lett.* **2008**, *93*, 253301.
[23] X. Zhang, H. Bronstein, A. K. Kronemeijer, J. Smith, Y. Kim, R. J. Kline, L. J. Richter, T. D. Anthopoulos, H. Sirringhaus, K. Song, M. Heeney, W. Zhang, I. McCulloch, D. M. DeLongchamp, *Nat. Comms.* **2013**, *4*, 1.
[24] K.-J. Baeg, S.-W. Jung, D. Khim, J. Kim, D.-Y. Kim, J. B. Koo, J. R. Quinn, A. Facchetti, I.-K. You, Y.-Y. Noh, *Org. Electron.* **2013**, *14*, 1407.
[25] U. Zschieschang, H. Klauk, M. Halik, G. Schmid, C. Dehm, *Adv. Mater.* **2003**, *15*, 1147.
[26] U. Zschieschang, R. Hofmockel, R. Rödel, U. Kraft, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. Butschke, H. Richter, J. N. Burghartz, H. Klauk, *Org. Electron.* **2013**, *14*, 1516.
[27] P. Heremans, J. Genoe, S. Steudel, K. Myny, P. Vicca, C. Grillberger, O. R. Hild, F. Furthner, B. van der Putten, A. K. Tripathi, G. H. Gelinck, *IEEE Book Series: International Electron Devices Meeting*, p. 343–346, IEEE, Piscataway, NJ, **2009**.
[28] M. Kitamura, Y. Kuzumoto, S. Aomori, Y. Arakawa, *Appl. Phys. Express.* **2011**, *4*, 051601.
[29] U. Kraft, M. Sejfić, M. J. Kang, K. Takimiya, T. Zaki, F. Letzkus, J. N. Burghartz, E. Weber, H. Klauk, *Adv. Mater.* **2015**, *27*, 207.
[30] T.-H. Ke, R. Müller, B. Kama, M. Rockele, A. Chasin, K. Myny, S. Steudel, W. D. Oosterbaan, L. Lutsen, J. Genoe, L. van Leuken, B. van der Putten, P. Heremans, *Org. Electron.* **2014**, *15*, 1229.
[31] B. Kim, S. Jang, M. L. Geier, P. L. Prabhumirashi, M. C. Hersam, A. Dodabalapur, *Nano Lett.* **2014**, *14*, 3683.
[32] S. Steudel, K. Myny, S. De Vusser, J. Genoe, P. Heremans, *Appl. Phys. Lett.* **2006**, *89*, 183503.
[33] M. Kitamura, Y. Arakawa, *Appl. Phys.Lett.* **2009**, *95*, 023503.
[34] S. K. Park, T. N. Jackson, J. E. Anthony, D. A. Mourey, *Appl. Phys. Lett.* **2007**, *91*, 063514.
[35] U. Zschieschang, M. J. Kang, K. Takimiya, T. Sekitani, T. Someya, T. W. Canzler, A. Werner, J. Blochwitz-Nimoth, H. Klauk, *J. Mater. Chem.* **2012**, *22*, 4273.
[36] M.-B. Madoc, D. Crouch, G. R. Llorente, T. J. Whittle, M. Geoghegan, S. G. Yeates, *J. Mater. Chem.* **2008**, *18*, 3230.
[37] J. Smith, W. Zhang, R. Sougrat, K. Zhao, R. Li, D. Cha, A. Amassian, M. Heeney, I. McCulloch, T. D. Anthopoulos, *Adv. Mater.* **2012**, *24*, 2441.
[38] SmartKem Limited patent family for tru-FLEX™ OSC inks, WO2012/164282; WO2013/124682 to WO2013/124688; WO2014/083328.
[39] G. Rincon-Llorente, M.-B. Madec, D. J. Crouch, S. G. Yeates, in *Proc. MRS Fall Meeting*, Boston MRS/Cambridge University Press, UK, **2008**, Paper 1114-G06-05.
[40] *Atlas User's Manual: Device Simulation Software*, Silvaco Inc, Santa Clara, CA April **2010**, Ch. no.15.
[41] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed., Wiley-Interscience, New York, **1981**, p. 454.
[42] H. Gold, A. Haase, A. Fian, C. Prietl, B. Striedinger, F. Zanella, N. Marjanović, R. Ferrini, J. Ring, K.-D. Lee, R. Jiawook, A. Drost, M. König, R. Müller, K. Myny, J. Genoe, U. Kleb, H. Hirshy, R. Prétôt, J. Kraxner, R. Schmied, B. Stadlober, *Org. Electron.* **2015**, *22*, 140.
[43] M. M. Ibrahim, A. C. Maciel, C. P. Watson, M.-B. Madec, S. G. Yeates, D. M. Taylor, *Org. Electron.* **2010**, *11*, 1234.