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Vacuum Production of OTFTs by Vapour Jet Deposition of Dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) on a Lauryl Acrylate Functionalised Dielectric Surface

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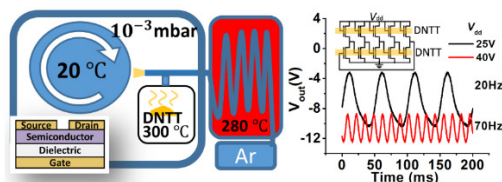
Abstract

Roll-to-roll (R2R) production of organic transistors and circuits require patterned deposition of organic layers at high deposition rate. Here we demonstrate a vapour-jet process for the rapid deposition of the organic semiconductor dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT). The deposition rate achieved, equivalent to ~200 nm/s onto a stationary substrate, was several orders of magnitude faster than ordinary thermal evaporation. Nevertheless, transistor yield was 100% with an average mobility of 0.4 cm^2/Vs in a single pass deposition onto a substrate moving at 0.15 m/min. We also demonstrate a vacuum, high rate R2R-compatible process for surface-functionalising a gate dielectric layer with lauryl acrylate which enabled an all-vacuum route to the fabrication of a five-stage ring oscillator.

Introduction

To fabricate low-cost flexible electronic circuits requires that the various patterned layers comprising an organic thin film transistor (OTFT), which is the basic building block of any circuit, are deposited at high speed in, preferably, a roll-to-roll (R2R) process. To this end, we have been developing a vacuum-evaporation route for the R2R production of organic-based circuits [1-3]. Already high-speed R2R equipment is available commercially for the vacuum-evaporation of metal patterns onto fast moving plastic webs [4] and could be adapted for TFT and circuit production. In our recent publications [2,3], we have shown that flash-evaporation technology used for depositing polymer coatings onto fast moving webs can be used to produce high-integrity, insulating films of poly(tripropyleneglycol diacrylate) (TPGDA). In this contribution, we focus on the fast deposition of the remaining layer i.e. the organic semiconductor.

To date, most attention has been focused on solution-processing, including spin-coating, ink-jet printing and gravure printing [5, 6]. With the solution-processing route material selection is limited by solubility and wetting. Initial studies concentrated on semiconducting polymers such as poly(3-hexylthiophene) [7,8], which usually has a lower mobility than found in evaporated films of small molecules such as, for example, pentacene or DNTT [9, 10]. However, the generally higher mobility of small molecules is now being harnessed by incorporation into blends [11-13] and by modification with solubilising side-groups as in, for example, TIPS-pentacene and C10-DNTT [14, 15]. However, device uniformity is still difficult to control owing to the need for reproducible phase separation in blends and, more generally, overcoming drying effects such as the coffee ring phenomenon [16]. Solution processing can also be wasteful of material and care is required in maintaining solution purity, solvent handling and equipment cleaning.

By contrast, the related issues of material solubility and solvent handling are not relevant for vacuum processing. This enables a much cleaner process with a wider material selection. However, the highest mobility in films of evaporated small molecules is achieved by slow evaporation with deposition rate usually less than 1nm/s [17]. Material usage is also relatively high as patterning is normally achieved using shadow masks.

Organic vapour jet (OVJ) deposition has been used successfully for the production of organic light emitting diodes (OLEDs) for many years [18]. OTFT production using OVJ printing has also been successfully demonstrated [19-21]. In this method the semiconductor is vaporised in a source cell and carried in an inert gas flow to the orifice of a narrow bore tube to produce a vapour jet that can be directed at relatively small localised areas of the substrate. This approach can be used for patterning and is essentially the vapour analogue of inkjet printing and results, therefore, in reduced material usage. Since our preliminary report [3] on TFT production using OVJ deposition of the semiconductor DNTT in a R2R environment, we have undertaken a more detailed investigation in which local deposition rates as high as 200 nm/s have been achieved at a substrate speed of 0.15 m/min.

Optimum OTFT characteristics are generally obtained by buffering the surface of high-k dielectrics with a low polarity film e.g. thin aluminium oxide films treated with a self-assembled monolayer of phosphonic acid [22]. In our case, it was found to be beneficial to buffer the polar TPGDA dielectric with a thin, spin-coated film of polystyrene to produce a low polarity surface [23]. As an alternative to spin-coated polystyrene and in keeping with the aim of developing an all-vacuum, R2R-compatible process, we also report here the vacuum-flash evaporation and curing of a thin film of lauryl acrylate as a buffer layer on TPGDA. Using this approach we have

fabricated, at high yield, both OTFTs and ring oscillators in an all-vacuum R2R compatible process.

Experimental
Sample preparation

Bottom-gate top-contact transistors were fabricated based on surface-buffered TPGDA as the gate dielectric and DNTT as the active semiconductor. The substrates were 125 µm thick polyethylene naphthalate film (PEN) (DuPont Teijin Films), patterned with a thermally evaporated Al gate metallisation layer. TPGDA (purchased from Sigma-Aldrich) was vacuum-flash evaporated onto the substrates, which were taped to the coating drum of the Oxford vacuum web-coater (Aerre Machines), and the acrylate monomers were polymerised *in situ* by exposure to an Ar plasma . The polymerized TPGDA layer was ~450 nm thick with a capacitance per unit area ~13 nF/cm^2. The full procedure for flash evaporation of TPGDA can be found in our previous papers [1-3].

To optimize carrier mobility, the TPGDA dielectric layer in some devices was buffered with a ~40 nm thick film of polystyrene (Sigma-Aldrich) spin-coated from 0.6 wt% toluene solution at 3000 RPM prior to evaporation of highly pure DNTT (synthesized in Manchester University). In other devices, and as part of the same integrated process, the TPGDA layer was buffered *in-situ* with a flash-evaporated and polymerised thin film composed of a mixture of lauryl acrylate (Sigma Aldrich) and 1,6-hexanediol diacrylate (HDDA) (Sigma Aldrich) (5:1 volume). In this case, the buffer layer was electron-beam cured (2.6 kV, 90 mA), so as to reduce the possible effect of O incorporation due to the plasma, in a second station in the web-coater while maintaining a drum speed of 5 m/min immediately after the main acrylate insulator layer deposition. Multiple pass deposition and curing was used for processing convenience but a single

pass R2R process would be feasible as long as curing power is adequate, as R2R curing of acrylate layers (at web speeds of up to 5m/s) has routinely been achieved using this equipment.

DNTT semiconductor layers were deposited either onto stationary substrates by thermal evaporation (0.05-0.1 nm/s) in an Edwards 306 thermal evaporator at ~5 x 10^{-4} mbar, or onto moving substrates by OVJ deposition in a purpose-built, medium-vacuum (10^{-2}-10^{-3} mbar) evaporation system. In both cases, the substrates were held at ambient temperature. For OVJ deposition, ~20 mg of DNTT powder was contained in a copper vessel held at 300ºC. Pre-heated Ar gas was fed at 6 sccm into the vessel after passing through 10 meters of copper pipe held at 260-280 ºC (see Graphical Abstract). A jet of the DNTT-loaded Ar vapour was directed to the substrate via a copper pipe fitted with nozzles of different size held close to the rotating coating drum. The substrates were attached to a rotating drum controlled by a DC motor.

The transistors and five-stage ring-oscillators were completed by depositing a 50 nm thick gold source-drain metallisation layer through a shadow mask. The aspect ratio, *W/L*, where *W* is the channel width and *L* the channel length, of a single OTFTs was (2 mm)/(100 µm). For the unipolar, saturated-load ring oscillator the aspect ratios of the driver and load TFTs were identical to those used previously [2] i.e. *W/L* (driver) = (4 mm)/(50 µm) and *W/L* (load) = (0.4 mm)/(50 µm). After a few trial runs, it became possible to routinely fabricate batches of 21 transistors with 100% yield.

Characterisation

Spin-coated buffer layer thicknesses were measured by coating directly onto microscope slides for measurement with a MicroXAM 5000B 3d ADE phase shift interference contrast optical profiler. The edge steps were created by scratching part of the film. It was not possible to

measure the thickness of the evaporated buffer layer – the underlying TPGDA layer was too soft to create a clear boundary and on glass the adhesion was very poor, presumably owing to a lack of cross-linking sites.

The semiconductor layers were characterised using a Siemens D5000 θ-2θ X-ray diffraction analyser employing copper Kα radiation (λ=0.15406 nm) and a secondary monochromator. The samples were scanned over the range $4° \leq 2\theta \leq 30°$ using a step size of 0.04° and a count time of 18 seconds per step.

XPS was performed in an ion pumped VG Microtech CLAM 4 MCD analyser system. 200 Watt unmonochromated Mg X-ray excitation was used. The analyser was operated at constant pass energy of 100 eV for wide scans and 20 eV for detailed scans. Data was obtained using SPECTRA version 8 operating system. Data processing was performed using CASAXPS.

Transistor characteristics were measured in air using two source-measure units (Keithley, Model 2400). The calculation of charge carrier mobility, μ, was based on the conventional square-law equation applicable when the device is in saturation i.e.

$$I_{dsat} = \mu \frac{W}{2L} C_i \left(V_g - V_t\right)^2 \qquad (1)$$

where I_{dsat} is the saturation source-drain current, C_i the capacitance per unit area of the dielectric layer, V_g the gate voltage and V_t the threshold voltage. Mobility was calculated from the slope of the linear section of $\sqrt{I_{dsat}}$ versus V_g plots while V_t was obtained from the intercept on the voltage axis.

Results and Discussion

The process parameters used for the OVJ-deposition of DNTT are listed in Table 1. The first set of samples used a nozzle of diameter = 2 mm, the local DNTT deposition rate onto a substrate moving at 1.5 cm/s was ~10 nm/s. This deposition rate is more than two orders of magnitude faster than previously used during thermal evaporation onto stationary substrates.

Figure 1 shows the transfer characteristics of a batch of 21 OVJ-fabricated TFTs on PS-buffered TPGDA fabricated using the 2mm nozzle. Also shown in Figure 1 are the distributions in the values of transistor characteristics extracted from the plots. Compared with our previously reported values [23] for transistors made from thermally evaporated DNTT onto stationary substrates (see Table 1), the mobility and on/off ratio have decreased from ~1.0 cm^2/Vs to ~ 0.2 cm^2/Vs and from 10^6 to 10^5 respectively. The turn-on voltages (Figure 1) were between 0 V and 6 V. Threshold voltages, however, were scattered between -1.8 V and -14 V. Similarly scattered threshold voltages were found in pentacene devices formed on a PS surface [23] which was probably caused by different concentrations of trap states near the pentacene/dielectric interface. In the present case, the scatter in mobility and threshold voltage may have arisen from the poorer registration between the OVJ nozzle and some of the devices – the centre of the vapour jet was not always located over the channel region. As described below, the lower mobility measured in these more rapidly deposited films may well have arisen from their poorer crystalline structure.

Figure 2 gives the XRD traces obtained from OVJ-deposited (rate 10 nm/s) DNTT films on a silicon wafer ((100) face) and on a PS-buffered silicon wafer, both substrates moving at 1.5 cm/s during the deposition. Also shown is the XRD trace from DNTT films thermally evaporated onto a stationary, PS-buffered silicon wafer. The stationary thermally evaporated DNTT displayed 2θ peaks at 5.5°, 11.0 ° and 16.4° corresponding respectively to the in-plane (001), (002) and (003) lattice planes of DNTT. The OVJ films deposited onto moving PS and silicon

substrates showed the same in-plane lattice plane peaks at the same positions, but also three additional peaks at 18.0°, 22.7° and 27.2° corresponding to "out-of-plane" (110), (020) and (120) lattice planes [24]. These additional peaks indicate the presence of a significant amount of out-of-plane oriented crystallites in these films, which was not significantly affected by the different substrates. The presence of these out-of-plane crystallites is indicative of a less ordered film and likely, therefore, to be the main cause of the reduced mobility in the OVJ-deposited DNTT compared with films thermally evaporated onto stationary substrates.

To increase deposition speed and reduce vapour jet area we reduced the nozzle size from 2 mm to 0.4 mm. Simultaneously, the distance to the substrate was reduced from 10 mm to ~2 mm (Table 1). The local deposition rate onto the substrate immediately under the nozzle now increased from 10 nm/s to 200 nm/s, i.e. a factor ~10^4 higher than normally used for thermal evaporation. With this setup, single pass evaporation was achieved at a drum speed of 15 cm/min. Three substrates, each with 7 transistors in a row, were aligned along the drum rotation direction in the path of the vapour jet, i.e. 21 transistors in a row. Since registration is difficult for the small nozzle, a slight off-set of 0.5 mm was applied to each substrate in the drum width direction, in order to ensure that at least one row of transistors was well registered with the jet. For the substrate with correct DNTT alignment, 100% yield of 7 working transistors was achieved. The transfer characteristics and distributions of device performance parameters are shown in Figure 6 a) Transfer curves of transistors with OVJ (2 mm nozzle) deposited DNTT on vacuum evaporated LA buffer layer; device distribution (shown in red – total of 19 devices) based on b) threshold voltage; c) turn on voltage; c) hole mobility; d) on on/off ratio. For comparison, the distribution data for the 2mm nozzle samples deposited onto spin-coated PS are reproduced from Figure 1 in grey (21 devices).. Interestingly, the DNTT carrier mobility did not decrease with increased deposition speed – on the contrary, in three transistors within the group of seven the mobility reached ~0.6

cm^2/Vs, with the spread in values grouped around a greater mobility. The transistors showed low off-currents and high on/off ratio and a reasonably narrow distribution of all parameters when measured in air in the dark. As in the lower speed batch of transistors, the devices had high negative threshold voltages. The greater scatter in mobility values were probably due to imperfect registration. That some devices showed mobilities as high as 0.6 cm^2/Vs is encouraging and suggests that optimization of the process would be beneficial. The negative turn on voltage could result from absorbed water near the semiconductor/dielectric interface that act as hole traps reported previously [25].

Equally important for device performance is the dielectric surface layer. In previous work, a polystyrene buffer layer spin-coated onto TPGDA was used to improve the hole mobility in DNTT. In order to achieve an all-evaporated process, we have investigated a R2R-compatible process for vacuum deposition of the buffer layer. This involved the flash-evaporation of lauryl acrylate, a monomer with long, non-polar section mixed in the ratio 5:1 with HDDA followed by e-beam curing. After coating the TPGDA surface with the buffer layer the water contact angle increased from 60° to 90°, suggesting a significant reduction in surface polarity.

The bare and functionalised TPGDA surfaces were characterised by XPS, in particular concentrating on the high-resolution C1s spectral features (Figure 4). These were fitted with three curves, the minimum number necessary to get a good fitting (standard deviation of the residual peak close to unity). The main peak at around 288 eV is from carbon in C-C and C-H bonds. The side peaks at 289 eV and 292 eV are from C-O and O-C=O bonds respectively. The percentage contribution from each bond type is listed in the figure. After buffering, the carbonyl contribution decreased to half its original value, possibly correlating with a lower carboxyl concentration in lauryl acrylate (1 carboxyl bond per 15 carbon atoms) compared to TPGDA (1

carboxyl bond per 7.5 carbon atoms). However, we cannot eliminate the possible additional effect of using e-beam curing rather than the plasma-cure used for TPGDA, where residual oxygen could be ionised by the plasma then react with TPGDA.

To compare the effectiveness of the lauryl acrylate buffer, three batches of transistors were prepared on bare TPGDA, PS buffered TPGDA, and lauryl acrylate buffered TPGDA. For this investigation, DNTT was deposited by thermal evaporation onto stationary substrates. Figure 5 shows the transfer curves of one typical transistor from each group which reflects the general trend of the three. Their performances are also summarised in table 2. Both buffered transistor groups showed equally good on/off ratio of about ~10^5 and mobility of ~0.6 cm^2/Vs which is significantly higher than the ~ 0.05 cm^2/Vs obtained from devices made on bare TPGDA. The lauryl acrylate buffered sample showed slightly more negative turn-on and threshold voltages than for the PS buffer, likely due to its slightly higher surface polarity and hence affinity for water. It is known that absorbed atmospheric moisture can be a source of hole traps which is reflected in transfer curves as a more negative turn-on voltage and eventually lower mobility [25]. The un-buffered transistor in this work showed carrier mobility of ~0.05 cm^2/Vs, on/off ratio of 10^4 and turn-on voltage close to 0 V. The low mobility was likely due to the undesirable surface energy which is prone to yielding poor crystallinity at the very near surface in deposited films of small molecule semiconductors as discussed in our recent paper [23].

We have also deposited DNTT by OVJ onto the lauryl acrylate functionalised surface, using the 2 mm nozzle at a substrate speed of 1.5 cm/min. Three substrates of 7 transistor arrays were processed. Two devices were damaged by mishandling during source/drain contact evaporation. The remaining 19 devices were fully functional. The transfer characteristics are shown in Figure 6 with the distributions of key transistor characteristics. Compared with the PS-

buffered OVJ-deposited samples with the same nozzle size, the distributions in threshold voltage and on/off ratio with the lauryl acrylate buffer are in a narrower range, with a comparable spread in mobility. The high yield is encouraging for further development of this in-line deposition option.

Having established that we could fabricate OTFTs with moderately good performance in an all-vacuum process, we proceeded to make and test a unipolar, saturated load, five-stage ring oscillator of the same geometry as used previously [2]. Here, though, the DNTT was deposited by OVJ in two stripes on the lauryl acrylate-buffered TPGDA, one each over the load and driver transistors as illustrated in the inset in Figure 7. The oscillator frequency was measured two weeks after fabrication. The low output frequencies 20 Hz and 70 Hz for rail voltages, V_{dd}, of 15 V and 40 V respectively, suggest a lower mobility as a result of misalignment of the vapour jet and/or deterioration in performance after storage in uncontrolled conditions between fabrication and measurement. These low frequencies contrast with ring oscillators made on PS-buffered TPGDA where shelf life greatly exceeded 1 month, presumably a consequence of the lower polarity dielectric surface and reduced propensity to degrade when exposed to atmospheric moisture in the case of the PS.

Conclusions

We have demonstrated the feasibility of using vapour jet deposition of small organic molecules to make transistors and simple circuits. Deposition rates using the technique, up to 200 nm/s, were some four orders of magnitude greater than used in traditional thermal evaporation. On polystyrene-buffered TPGDA, this resulted in only ~50% reduction in mobility even on substrates moving at 15 cm/min. By replacing the spin-coated polystyrene buffer layer with flash-evaporated lauryl acrylate, we have also demonstrated an all-vacuum, R2R compatible deposition process for the fabrication of thin-film transistors and circuits. Future developments will include improved surface functionalization to reduce further the surface polarity of the gate insulator and high-resolution patterning of both the insulator and semiconductor layers.

References

[1] Abbas, G., Ding, Z., Mallik, K., Assender, H., & Taylor, D. M. "Hysteresis-Free Vacuum-Processed Acrylate—Pentacene Thin-Film Transistors." IEEE electron device letters 34.2 (2013): 268-270. DOI:10.1109/LED.2012.2234434

[2] Patchett, E. R., Williams, A., Ding, Z., Abbas, G., Assender, H. E., Morrison, J. J., Yeates, S.G. & Taylor, D. M. "A high-yield vacuum-evaporation-based R2R-compatible fabrication route for organic electronic circuits." Organic Electronics15.7 (2014): 1493-1502. DOI:10.1016/j.orgel.2014.03.043

[3] Abbas, G. A., Ding, Z., Assender, H. E., Morrison, J. J., Yeates, S. G., Patchett, E. R., & Taylor, D. M. "A high-yielding evaporation-based process for organic transistors based on the semiconductor DNTT." Organic Electronics 15.9 (2014): 1998-2006. DOI:10.1016/j.orgel.2014.05.029

[4] Copeland N, Jack A and Harland L 2009 In-register in-vacuum pattern printing - From wish to reality *Proc Annual Techn Conf – Soc Vac Coaters* **52** 712-715

[5] Fukuda, K., Takeda, Y., Mizukami, M., Kumaki, D., & Tokito, S. "Fully solution-processed flexible organic thin film transistor arrays with high mobility and exceptional uniformity." *Scientific reports* 4 (2014). DOI:10.1038/srep03947

[6] Noh, J., Jung, K., Kim, J., Kim, S., Cho, S., & Cho, G. "Fully gravure-printed flexible full adder using swnt-based tfts." *Electron Device Letters, IEEE* 33.11 (2012): 1574-1576. DOI:10.1109/LED.2012.2214757

[7] Bao, Z., Dodabalapur, A., & Lovinger, A. J. "Soluble and processable regioregular poly (3‐hexylthiophene) for thin film field‐effect transistor applications with high mobility." *Applied Physics Letters* 69.26 (1996): 4108-4110. DOI:10.1063/1.117834

[8] Klauk, H. "Organic thin-film transistors." *Chemical Society Reviews* 39.7 (2010): 2643-2666. DOI: 10.1039/B909902F

[9] Klauk, H., Halik, M., Zschieschang, U., Schmid, G., Radlik, W., & Weber, W. "High-mobility polymer gate dielectric pentacene thin film transistors." *Journal of Applied Physics* 92.9 (2002): 5259-5263. DOI: 10.1063/1.1511826

[10] Yamamoto, T., & Takimiya, K. "FET characteristics of dinaphthothienothiophene (DNTT) on Si/SiO2 substrates with various surface-modifications." *Journal of Photopolymer Science and Technology* 20.1 (2007): 57-59. DOI:10.2494/photopolymer.20.57

[11] Abu-Sen, L., Morrison, J. J., Horn, A. B., & Yeates, S. G. "Concentration‐and Solvent‐Dependent Photochemical Instability of 6, 13‐Bis (triisopropysilylethynyl) pentacene." *Advanced Optical Materials* 2.7 (2014): 636-640. DOI: 10.1002/adom.201400003

[12] Coppo, Paolo, and Stephen G. Yeates. "Shining light on a pentacene derivative: The role of photoinduced cycloadditions." *Advanced Materials* 17.24 (2005): 3001-3005. DOI: 10.1002/adma.200501471

[13] Hunter, S., Chen, J., & Anthopoulos, T. D. "Microstructural Control of Charge Transport in Organic Blend Thin‐Film Transistors." *Advanced Functional Materials* 24.38 (2014): 5969-5976. DOI: 10.1002/adfm.201401087

[14] Park, S. K., Jackson, T. N., Anthony, J. E., & Mourey, D. A. "High mobility solution processed 6, 13-bis (triisopropyl-silylethynyl) pentacene organic thin film transistors." *Applied Physics Letters* 91.6 (2007): 063514-063514. DOI: 10.1063/1.2768934

[15] Zschieschang, U., Kang, M. J., Takimiya, K., Sekitani, T., Someya, T., Canzler, T. W., Werner, A. Blochwitz-Nimoth, J. & Klauk, H. "Flexible low-voltage organic thin-film transistors and circuits based on C 10-DNTT." *Journal of Materials Chemistry* 22.10 (2012): 4273-4277. DOI: 10.1039/C1JM14917B

[16] Deegan, R. D., Bakajin, O., Dupont, T. F., Huber, G., Nagel, S. R., & Witten, T. A. "Capillary flow as the cause of ring stains from dried liquid drops." *Nature* 389.6653 (1997): 827-829. DOI:10.1038/39827

[17] Ruiz, R., Choudhary, D., Nickel, B., Toccoli, T., Chang, K. C., Mayer, A. C., Clancy, P. & Malliaras, G. G."Pentacene thin film growth." *Chemistry of Materials* 16.23 (2004): 4497-4508. DOI: 10.1021/cm049563q

[18] Forrest, S. R. "The path to ubiquitous and low-cost organic electronic appliances on plastic." *Nature* 428.6986 (2004): 911-918. DOI:10.1038/nature02498

[19] Rolin, C., Vasseur, K., Genoe, J., & Heremans, P. "Growth of pentacene thin films by in-line organic vapor phase deposition." *Organic electronics* 11.1 (2010): 100-108. DOI:10.1016/j.orgel.2009.10.005

[20] Shtein, M., Peumans, P., Benziger, J. B., & Forrest, S. R. "Direct mask-free patterning of molecular organic semiconductors using organic vapor jet printing." *Journal of applied physics* 96.8 (2004): 4500-4507. DOI:10.1063/1.1791760

[21] Yun, C., Moon, H., Kang, H. W., Kim, M., Sung, H. J., & Yoo, S. "High-Performance Pentacene Thin-Film Transistors Fabricated by Organic Vapor-Jet Printing." *Electron Device Letters, IEEE* 31.11 (2010): 1305-1307. DOI:10.1109/LED.2010.2064752

[22] Jedaa, A., Burkhardt, M., Zschieschang, U., Klauk, H., Habich, D., Schmid, G., & Halik, M. "The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors." *Organic Electronics* 10.8 (2009): 1442-1447. DOI: 10.1016/j.orgel.2009.08.006

[23] Ding, Z., Abbas, G. A., Assender, H. E., Morrison, J. J., Sanchez-Romaguera, V., Yeates, S. G., & Taylor, D. M. "Improving the performance of organic thin film transistors formed on a vacuum flash-evaporated acrylate insulator." *Applied Physics Letters* 103.23 (2013): 233301. DOI: 10.1063/1.4839275

[24] Kuribara, K., Wang, H., Uchiyama, N., Fukuda, K., Yokota, T., Zschieschang, U., ... & Someya, T. "Organic transistors with high thermal stability for medical applications." *Nature communications* 3 (2012): 723. DOI:10.1038/ncomms1721

[25] Ding, Z., Abbas, G., Assender, H. E., Morrison, J. J., Yeates, S. G., Patchett, E. R., & Taylor, D. M. "Effect of oxygen, moisture and ill umination on the stability and reliability of

dinaphtho [2, 3-b: 2′, 3′-f] thieno [3, 2-b] thiophene (DNTT) OTFTs during operation and storage." *ACS applied materials & interfaces* 6.17 (2014): 15224-15231.
DOI: 10.1021/am503560d

Table 1 Summary of substrate speed, Ar flow rate, DNTT deposition rate, device mobility, and on/off ratio at different vapour jet nozzle size.

	Nozzle/Sub. Distance	Substrate speed	Ar feeding rate	Deposition rate	Mobility (cm^2/Vs)	On/off ratio
2mm diameter nozzle	10mm	1.5cm/min	6 sccm	~10nm/s	0.20±0.07 (PS*)	10^5
					0.18±0.06 (LA*)	10^4
0.4mm diameter nozzle	2-3mm	15cm/min	6 sccm	~200nm/s	0.43±0.16 (PS*)	10^5
Stationary[23]	200mm	0	N/A	0.02nm/s	1 (PS*)	10^{6-7}

*PS denotes polystyrene buffered devices, LA denotes lauryl acrylate buffered devices.

Table 2 Summary of transistor performance: without dielectric buffer, with PS buffer and with LA buffer
The DNTT were stationary thermally evaporated at rate of 0.05-0.1nm/s

	Mobility (cm^2/Vs)	Threshold voltage	Turn-on voltage	On/off ratio	SS (V)
No buffer	0.05	-2	0	4.3x10^4	2.22
PS buffer	0.6	-2	-1	1.5x10^5	1.33
LA buffer	0.6	-5	-2.5	4.7x10^4	1.72
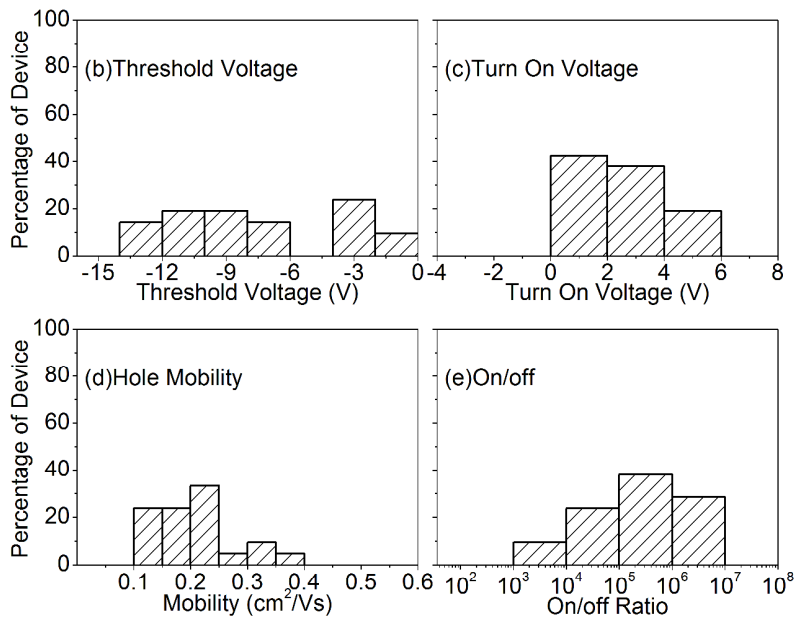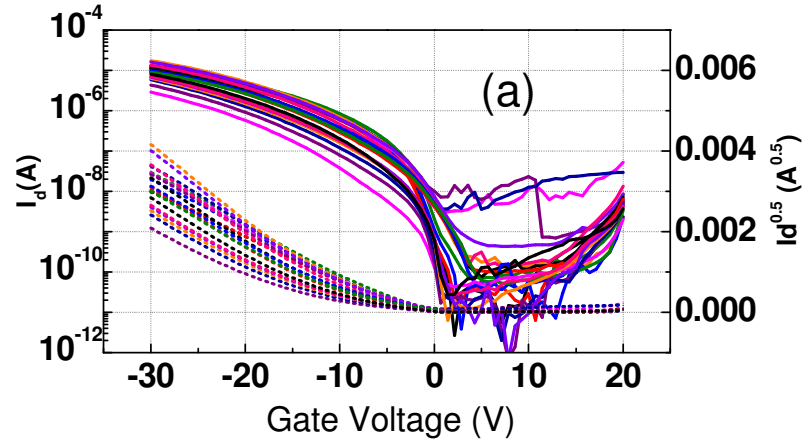
Figure 1. a) Transfer curves of transistors with OVJ (2mm nozzle) deposited DNTT onto the spin-coated PS buffer layer; device distribution (21 devices in total) based on b) threshold voltage; c) turn-on voltage; c) hole mobility; d) on/off ratio.
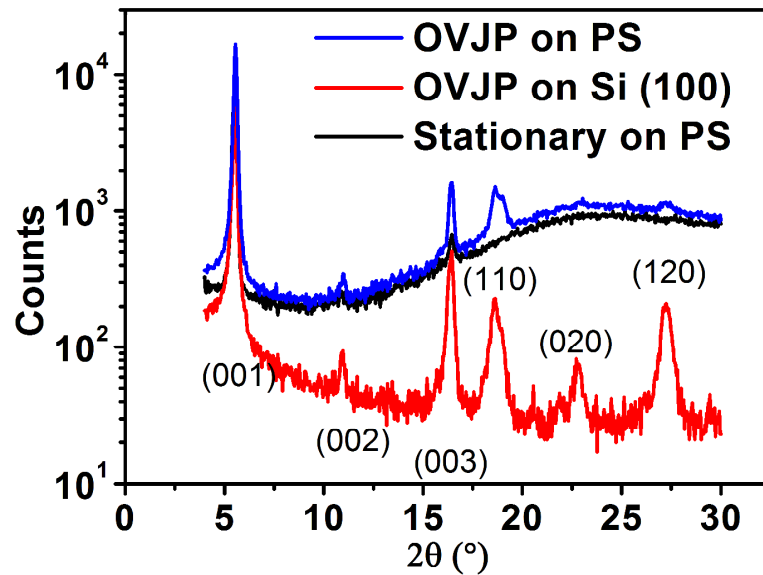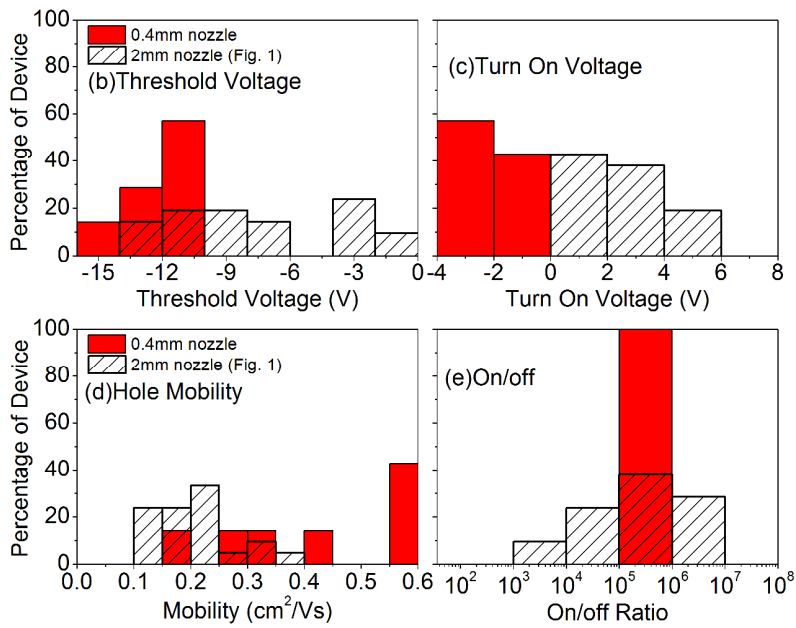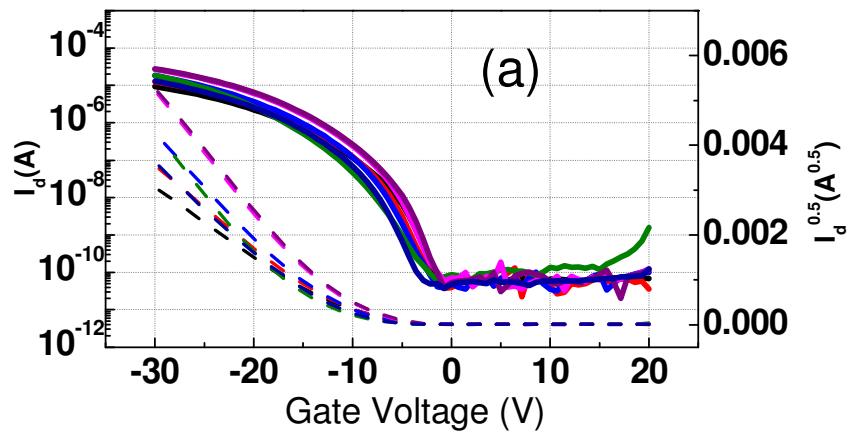
Figure 2. XRD traces of OVJ deposited DNTT on spin-coated PS and Si wafer at rate of about 10 nm/s; stationary evaporated DNTT on spin-coated PS at rate of 0.2 /s. The difference in baseline can be accounted for by scattering from the underlying amorphous PS.

Figure 3 a) Transfer curves of transistors with OVJ (0.4 mm nozzle) deposited DNTT on spin-coated PS buffer layer; device distribution (shown in red – total of 7 devices) based on b) threshold voltage; c) turn on voltage; c) hole mobility; d) on on/off ratio. For comparison, the distribution data for the 2mm nozzle are reproduced from Figure 1 in grey (21 devices).
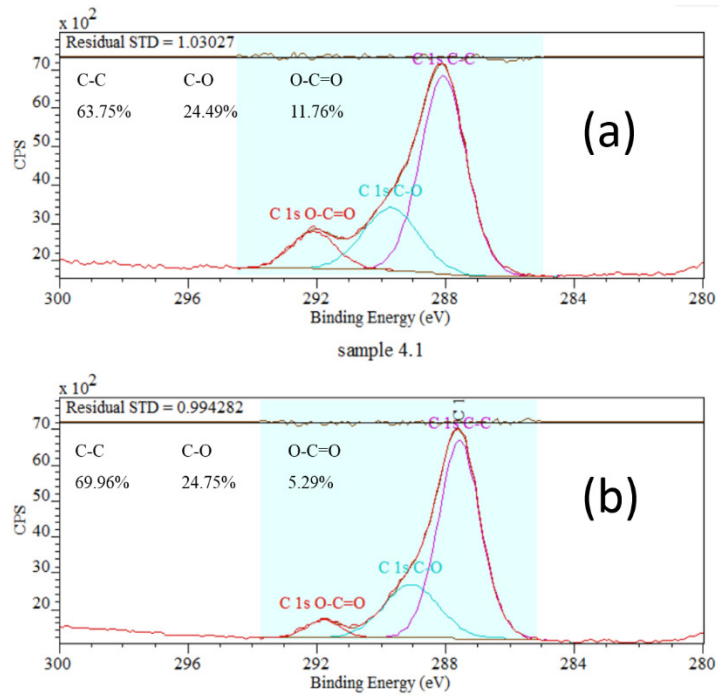
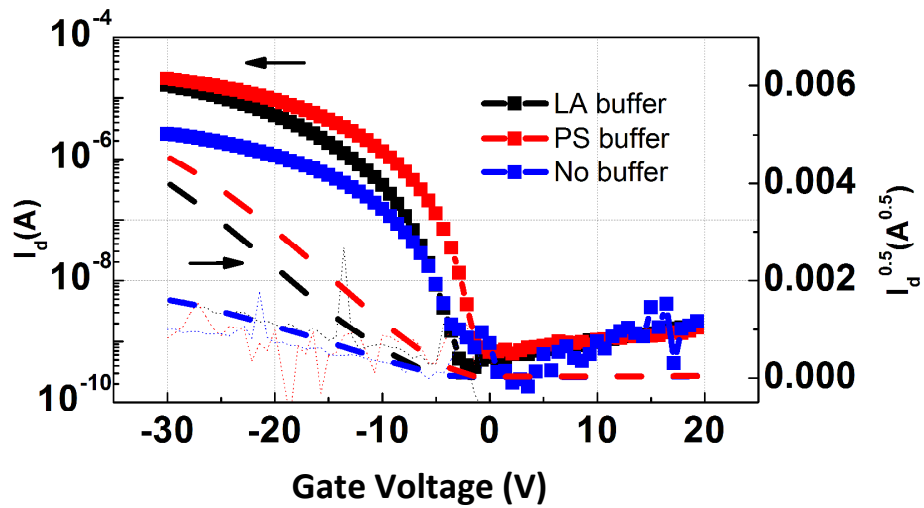Figure 4 XPS spectra of carbon 1s peaks for the TPGDA dielectric surface (a) before and (b) after buffering with lauryl acrylate.

Figure 5 Transfer curves of transistors with dielectric layer surface treated by no buffer layer, LA buffer and spin-coated PS buffer layer (stationary evaporated DNTT).
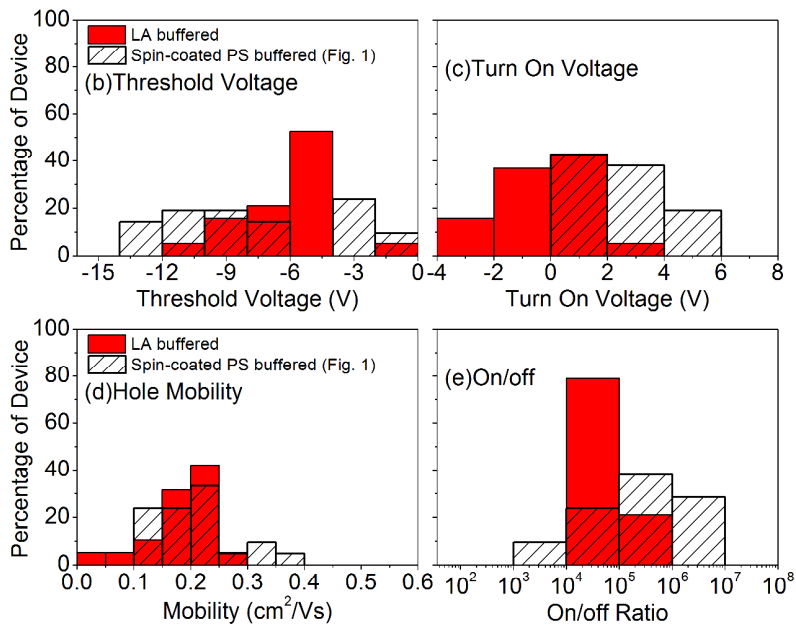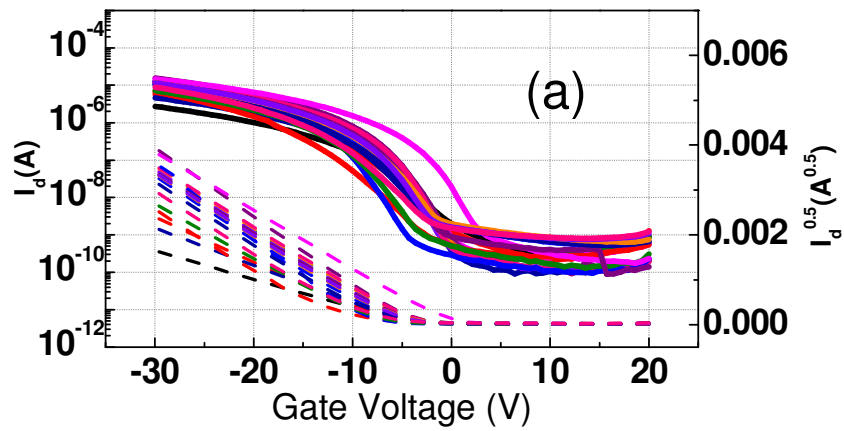
Figure 6 a) Transfer curves of transistors with OVJ (2 mm nozzle) deposited DNTT on vacuum evaporated LA buffer layer; device distribution (shown in red – total of 19 devices) based on b) threshold voltage; c) turn on voltage; c) hole mobility; d) on on/off ratio. For comparison, the distribution data for the 2mm nozzle samples deposited onto spin-coated PS are reproduced from Figure 1 in grey (21 devices).
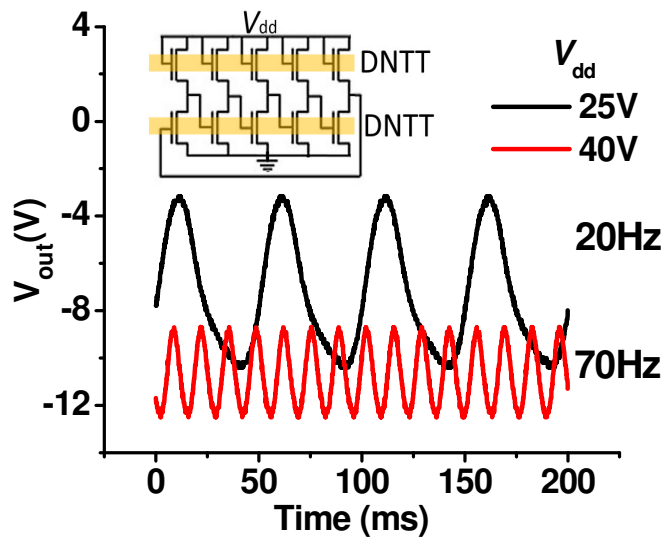
Figure 7 Voltage output of a five-stage ring oscillator made using OVJ deposited DNTT on LA buffered acrylate. Depsition rate = 10 nm/s, substrate speed = 1.5 cm/s.