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# Organic Digital Logic and Analog Circuits Fabricated in a Roll-to-Roll Compatible Vacuum-Evaporation Process

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***Abstract*— We report the fabrication of a range of organic circuits produced by a high-yielding, vacuum-based process compatible with roll-to-roll production. The circuits include inverters, NAND and NOR logic gates, a simple memory element (set–reset latch), and a modified Wilson current mirror circuit. The measured circuit responses are presented together with simulated responses based on a previously reported transistor model of organic transistors produced using our fabrication process. Circuit simulations replicated all the key features of the experimentally observed circuit performance. The logic gates were capable of operating at frequencies in excess of 1 kHz while the current mirror circuit produced currents up to 18 $\mu$A.**

***Index Terms*— Analog circuits, circuit simulation, digital circuits, logic circuits, organic electronics, thin film transistors (TFTs).**

## I. Introduction

OVER the last decade or so, there has been increasing interest in developing low-cost processes for printing organic thin film transistors (OTFTs) and circuits onto flexible substrates. Initial efforts were based around ink-jet printing [1], [2] and are still being actively developed [3]–[5] for OTFT fabrication. Recently, significant progress has been made in developing roll-to-roll (R2R) fabrication utilizing other printing technologies including offset, gravure and flexographic printing [6]–[12], and combinations thereof.

While some success has been achieved with a hybrid of Si and printing technologies [13], there are still many problems to overcome in all-solution-printing approaches. The resulting thin film transistors (TFTs) tend to suffer from low yield, poor device-to-device reproducibility, and low mobility, often a consequence of ink formulation, layer morphology, and poor interfaces. When coupled with the thick gate insulators needed to minimize pinhole defects and the long channels resulting from poor printing resolution, high operating voltages (50–100 V) are necessary to effect even modest circuit performance.

In [14]–[18], we have demonstrated that OTFT and circuit fabrication based on thermal evaporation of the various layers is a feasible proposition for low-cost R2R device and circuit fabrication. Commercial vacuum equipment is already available for applying metal patterns onto plastic packaging [19]. Using a combination of metal evaporation with oil printing in a lift-off-type process [20], [21] a resolution of 30–50 $\mu$m is possible at web speeds up to $\sim$200 m/min. Low-cost, high-speed processes [14], [22] are also available commercially for applying thin, polymer barrier layers to plastic packaging, providing an established route for the formation of pinhole-free, electrically robust insulating layers.

Vacuum processing removes many solvent related issues, e.g., solvent drying times and recovery, solvent-induced layer interdiffusion, pinhole defects, and surface roughness, which can lead to poor device performance and low yield, thus negating the suggested cost advantage of solution-based processes.

We have already demonstrated [18] that using vacuum-based methods compatible with R2R manufacture, 90-transistor arrays with high mobility, $\sim$1 cm$^2$/Vs, can be produced routinely with high yield $\geq$ 90%. Furthermore, the bottom-gate, top-contact devices, based on polymerized, flash-evaporated tripropyleneglycol diacrylate (TPGDA) monomer as the gate insulator and dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) [23] as the active semiconductor, displayed good operational and environmental stability. In [18], we focused attention on the fabrication and characterization of transistors, inverters, and ring oscillators. Here, we extend this novel, vacuum-based fabrication approach to the manufacture of digital logic circuits [NAND/NOR logic gates and set–reset (S–R) latch] and an analog circuit (current mirror). We also show that a previously derived transistor model [18], when used to simulate the response of the fabricated circuits, replicates well the observed experimental performance.

## II. Experiment

Arrays of NAND, NOR, S–R latches, and current mirrors were fabricated with high yield on precleaned,

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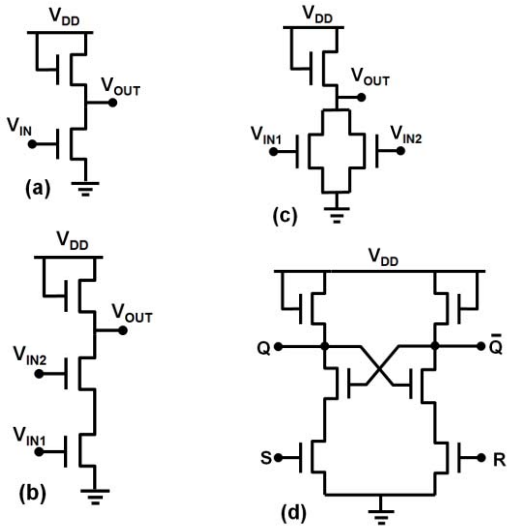


Fig. 1. Digital logic circuits fabricated, tested, and simulated in this paper. (a) Inverter. (b) NAND gate. (c) NOR gate. (d) S–R latch.

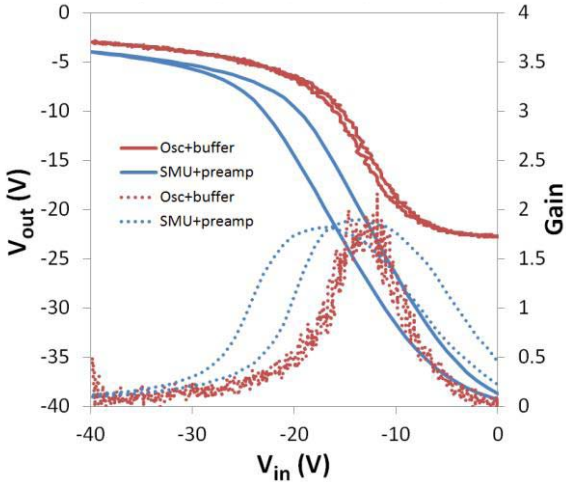


Fig. 2. Inverter transfer characteristics (solid lines) and gain (dotted lines) for two different probe systems (see text for details). $V_{DD} = -40$ V.

50 mm × 50 mm square, 125-$\mu$m-thick polyethylene naphthalate (PEN) (Dupont–Teijin) substrates using our previously described protocols [14]–[18]. Briefly, the gate-level metallization was achieved by thermally evaporating aluminum through appropriate Kapton shadow masks (Laser Micromachining Ltd) onto the PEN substrates. These were then fixed onto the water-cooled drum of a webcoater (Aerre Machines) equipped with a Sigma polymer coating system (Sigma Technologies) and rotated at a linear speed of 25 m/min. TPGDA vapor was directed through Kapton shadow masks onto the metalized substrate where it condensed. The liquid film passed immediately under an Ar plasma source where it cross linked to form a robust insulating layer ∼400–500-nm thick. As the samples were directly attached to the coating drum for experimental convenience, the film was built up over several passes under the deposition/curing source.

To minimize the deleterious effects of polymer polar groups on carrier mobility [24], a polystyrene ($M_W = 350\,000$) buffer layer [18] was spin coated from 3 wt% solution in toluene at 1000 r/min onto the TPGDA in a nitrogen glove box and heated on a hot plate at 100 °C for 10 min, thus forming a two-layer gate dielectric with capacitance 4.38 nF/cm$^2$. The substrates were then transferred into an integrated evaporator (Minispectros, Kurt Lesker) for the vacuum deposition (2.4 nm/min) onto the insulator of highly pure, recrystallized DNTT [18], [23], a high-mobility, air-stable organic semiconductor [25], [26]. Without exposing the substrates to ambient air, the source/drain metallization layer was deposited in the same evaporator by thermal evaporation of gold through a Kapton shadow mask. The aspect ratio $W/L$ (where $W$ and $L$ are the channel width and length, respectively) of the unipolar saturated load transistors in the inverter, NAND, and NOR circuits was 625 $\mu$m/100 $\mu$m. For the driver (input) transistors and all four transistors in the mirror circuit, $W/L$ was 2500 $\mu$m/50 $\mu$m.

OTFT characteristics, inverter transfer characteristics, and current-mirror functionality were measured using a Keithley model 4200 semiconductor characterization system in ambient dark conditions. Owing to the poor frequency response of the Keithley system, the time responses of inverters, NAND and NOR logic gates, and the S–R latch were recorded by connecting the output of each circuit to a digital oscilloscope (Agilent DSO-X 2014A) via a buffer amplifier to minimize oscilloscope loading effects. The input signals were provided from a TTi TGA1242 Waveform Generator connected to a high voltage amplifier (Falco Systems Model WMA01). The source follower buffer amplifier design (based on the OPA445 op-amp) was a compromise between high voltage capability, high frequency response (2 MHz), and low bias current (10 pA). This last results in a much lower effective input resistance than presented by the preamplifier input to the Keithley source measure unit (SMU) (∼$10^{16}$ Ω). For comparison, therefore, static inverter transfer characteristics were also obtained using the oscilloscope-buffer amplifier combination. Device parameter extraction and circuit simulations were undertaken using Silvaco's universal OTFT (UOTFT) model (Level = 37) and Gateway SmartSpice Circuit Simulator.

## III. Results and Discussion

The four logic gates fabricated and characterized in this paper are shown in Fig. 1. The inverter function was achieved by grounding the connection between the two input OTFTs of the NAND circuit. The current-mirror circuit is shown in the inset in Fig. 7. In the following sections, both the experimentally measured circuit performances and their simulations are presented. In all cases, the simulations were based on a representative model card for our transistors that was derived using Silvaco's UOTFT software and presented in [18].

### A. Inverter

The static transfer characteristic of the inverter section of a NAND gate (Fig. 2), not surprisingly, is seen to depend on the input impedance of the measurement system. Using the Keithley system, the output voltage swing is ∼35 V with $V_{DD} = -40$ V but shows strong hysteresis. Since the

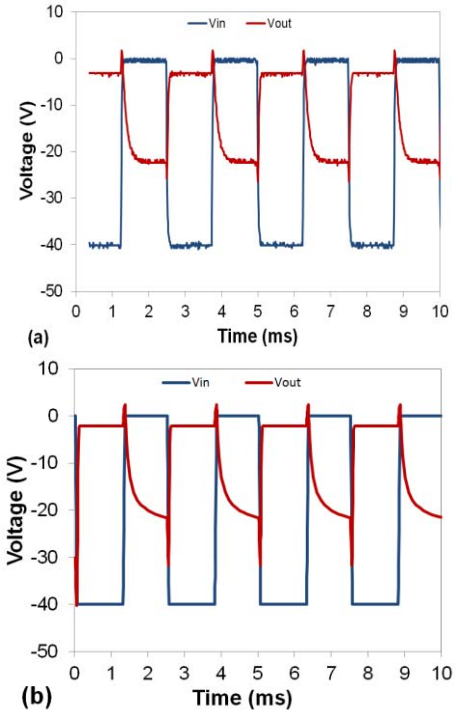


Fig. 3. (a) Experimental and (b) simulated inverter response. The frequency of the input square wave is 400 Hz and $V_{DD} = -40$ V.

measurement took around ∼6 min, this may have resulted from threshold voltage shifts in the OTFTs. However, using the oscilloscope/buffer amplifier approach over an even longer timescale, there was negligible hysteresis but a lower output swing, ∼20 V. The reduced output swing is due to the 10-pA bias current of the buffer amplifier shunting the drive transistor while the significantly higher input resistance of the Keithley preamplifier leads to the hysteresis. Both measurements indicate an inverter gain approaching two. In terms of noise margin, the buffer amplifier will provide conditions closer to those prevailing in circuit operation, i.e., high and low noise margins $NM_H$ ∼4.7 V and $NM_L$ ∼4.4 V [27]. This is more than sufficient for ensuring continuous operation of a seven-stage ring oscillator for 8 h, as reported previously [18] and the robust performance of S–R logic gates as described below.

In Fig. 3(a) is shown the response of the same inverter to a 400 Hz, 40 V input square wave ($V_{DD} = -40$ V). Whilst the driver transistor is able to pull down the output to −3.1 V, the load transistor pulls up the output only to −22.5 V. Since the latter operates in saturation at all times the current $I_D$(load), it can supply to the load capacitance $C_L$ is given by

$$I_D(\text{load}) = \frac{W}{2L}\mu C_i\,[(V_{DD} - V_{TL}) - V_{OUT}]^2 \qquad (1)$$

where $C_i$ is the capacitance per unit area of the gate dielectric, $V_{OUT}$ the inverter output voltage, and $V_{TL}$ the threshold voltage of the load transistor. If the driver transistor is fully turned OFF when the input voltage $V_{IN} = 0$, then $I_D$(load) will also be close to zero. This would correspond to the condition $V_{DD} - V_{OUT} - V_{TL} = 0$, which suggests that $V_{TL} = -17.5$ V. This is close to that previously reported ($-18.15 \pm 0.25$ V) and obtained using the Silvaco's UOTFT software to extract device parameters from the characteristics of OTFTs produced using the same fabrication procedures [18]. However, in the present case, since $V_{OUT}$ is determined by the bias current of the buffer amplifier, $V_{TL}$ will be lower.

Equation (1) may also be used to determine the rate at which $V_{OUT}$ rises to high when the driver OTFT is turned ON since

$$\frac{dV_{OUT}}{dt} = \frac{I_D(\text{load})}{C_L} = \frac{\beta}{2C_L}[(V_{DD} - V_{TL}) - V_{OUT}]^2 \qquad (2)$$

where $\beta = (W/L)\mu C_i$. Separating the variables in (2) and integrating subject to the boundary condition that at $t = 0$, $V_{OUT} = 0$ yields the relation

$$\frac{V_{OUT}}{(V_{DD} - V_{TL})} = \frac{(\beta/2C_L)(V_{DD} - V_{TL})t}{1 + (\beta/2C_L)(V_{DD} - V_{TL})t} \qquad (3)$$

from which it is seen that $V_{OUT}$ reaches 50% of its final value when $(\beta/2C_L)(V_{DD} - V_{TL})t = 1$. Inserting the relevant values of $W$, $L$, and $C_i$ for the load transistor and assuming that $\mu = 1$ cm$^2$/Vs, then $\beta = 2.74 \times 10^{-8}\Omega^{-1}V^{-1}$. $C_L$ comprises the capacitance of the buffer amplifier and connecting cables (48 pF) and the gate capacitance (40 pF) of the driver transistor that is dominated by the parasitic gate–drain overlap capacitance (our transistors were designed to reflect the registration ability of a high-speed R2R process [18]). Noting that $|V_{DD} - V_{TL}| \geq 22.5$ V, then the time taken for $V_{OUT}$ to reach 50% of its final value $t_{50}(R)$ is estimated to be less than ∼260 $\mu$s. This is significantly longer than measured experimentally, $t_{50}(R) \sim 135\mu$s, suggesting that parasitic gate capacitance or $V_{TL}$ (or both) have been over-estimated.

In Fig. 3(b), we show the simulated inverter performance. As in the calculation above, the simulated circuit model included the capacitive load presented by the gate of the driver transistor plus the buffer amplifier and cable. The simulated response closely resembles the measured inverter output as it switches between low (−3.1 V) and high (−22.5 V) even reproducing the spikes arising from capacitive breakthrough. From the simulations, $t_{50}(R)$ is estimated to be ∼130 $\mu$s and close to that measured experimentally. In the later stages of the transition to high, the fabricated circuit performs better than predicted by simulation. This suggests that, as $V_{OUT}$ increases toward $V_{DD}$, the measured $I_D$(load) falls more slowly than simulation predicts. While this may arise from a parasitic source–drain current, which significantly increases the conductance of the smaller load OTFT [18], the sharper cutoff is probably caused by the buffer amplifier.

A similar analysis to that above can be undertaken for the transition from high to low, i.e., when the driver transistor is turned ON. Now, to a first approximation, with $V_{IN} = -40$ V we may assume that the driver acts as a constant current source, $I_D$ (driver), discharging $C_L$ at a constant rate so that the time to switch to low is given by

$$t = \frac{C_L \cdot \Delta V_{OUT}}{I_D(\text{driver})} = \frac{2C_L \cdot \Delta V_{OUT}}{\beta(V_{IN} - V_{TD})^2} \qquad (4)$$

where $V_{TD}$ is the threshold voltage of the driver transistor, assumed equal to $V_{TL}$, and $\beta = 2.19 \times 10^{-7}\Omega^{-1}\text{V}^{-1}$ reflecting the larger aspect ratio $W/L$ of this device. For $\Delta V_{OUT} = 19.4$ V, the time taken to reach 50% of the output

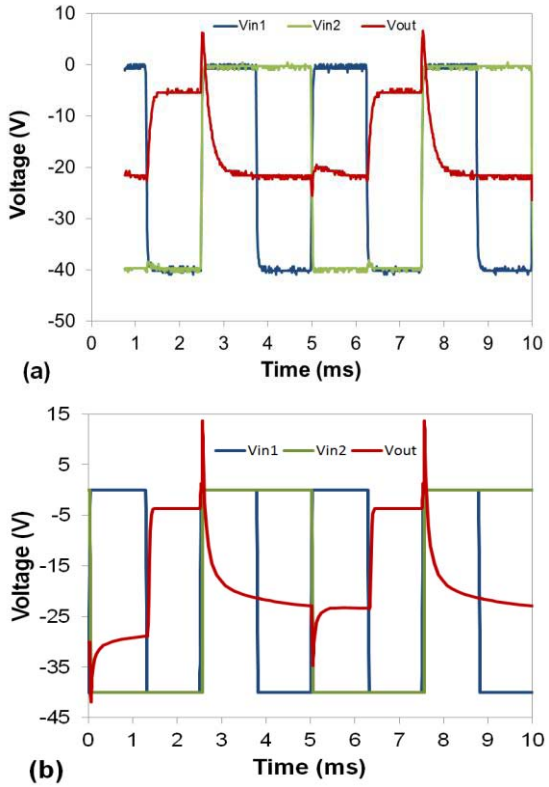


Fig. 4. (a) Experimental and (b) simulated responses of a NAND logic gate. Input square wave frequencies are 400 Hz ($V_{\text{in1}}$) and 200 Hz ($V_{\text{in2}}$).

swing $t_{50}(F)$ is 15 $\mu$s. From the measured and simulated responses, the transition times $t_{50}(F)$ to fall by $\Delta V_{\text{OUT}}/2$ are estimated to be ~25 and ~40 $\mu$s, respectively. This is significantly faster than from low to high reflecting the higher transconductance of the driver transistor; that (4) predicts a shorter switching time than these is not surprising. As $V_{\text{OUT}}$ falls toward zero, $I_D$(load) increases and should be subtracted from $I_D$ (driver) in (4). Nevertheless, it may be concluded that with a propagation delay, $[t_{50}(R) + t_{50}(F)]$, of ~160 $\mu$s at $V_{\text{DD}} = -40$ V, the inverter is well-capable of operating at frequencies >1 kHz.

### *B.* NAND *and* NOR *Gates*

The measured response of the NAND gate [Fig. 1(b)] to square wave input signals $V_{\text{IN1}}$ (400 Hz) and $V_{\text{IN2}}$ (200 Hz) is shown in Fig. 4(a). As expected, $V_{\text{OUT}}$ follows the truth table for a NAND gate (Table I), i.e., remains high (−21.5 V) except when both inputs are high (−40 V). The simulated response in Fig. 4(b) resembles closely that measured experimentally. The larger capacitive spikes in the simulation result from the sharper edges of the simulated input signals compared with those used experimentally. This also explains why the small feature observed in the measured response between 5 and 6 ms is not reproduced. The shallower edges of the input signals applied experimentally allow both transistors to conduct partially during the transition, thus leading to a tendency for the output to go lower.

The experimental and simulated responses of the NOR gate [Fig. 1(c)] to input square waves of 400 and 200 Hz are given

TABLE I
TRUTH TABLES FOR NAND AND NOR LOGIC GATES

| NAND GATE | | | NOR GATE | | |
|---|---|---|---|---|---|
| $V_{\text{IN1}}$ | $V_{\text{IN2}}$ | $V_{\text{OUT}}$ | $V_{\text{IN1}}$ | $V_{\text{IN2}}$ | $V_{\text{OUT}}$ |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 |

TABLE II
TRUTH TABLE FOR THE S–R LATCH

| S | R | Q | $\overline{\text{Q}}$ |
|---|---|---|---|
| 0 | 0 | Invalid | Invalid |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | No change | No change |

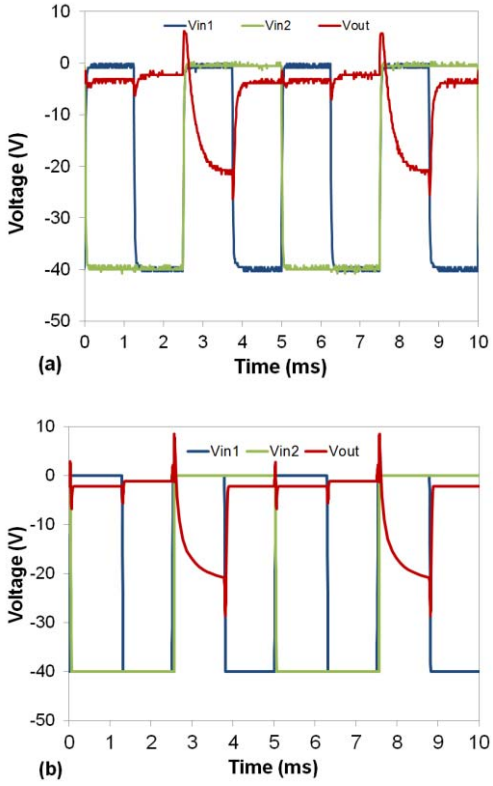


Fig. 5. (a) Experimental and (b) simulated output of a NOR logic gate. Input square wave frequencies are 400 Hz ($V_{\text{in1}}$) and 200 Hz ($V_{\text{in2}}$).

in Fig. 5(a) and (b), respectively. The simulation again predicts with some accuracy the features observed in the measured response, with both following the NOR truth table (Table I).

The successful demonstration of NAND and NOR gates fabricated using a R2R compatible vacuum-evaporation process opens a route to the fabrication of more complex logic circuits. In the following section, we show that the technology can be extended to the fabrication of a simple static memory element, the so-called S–R latch.

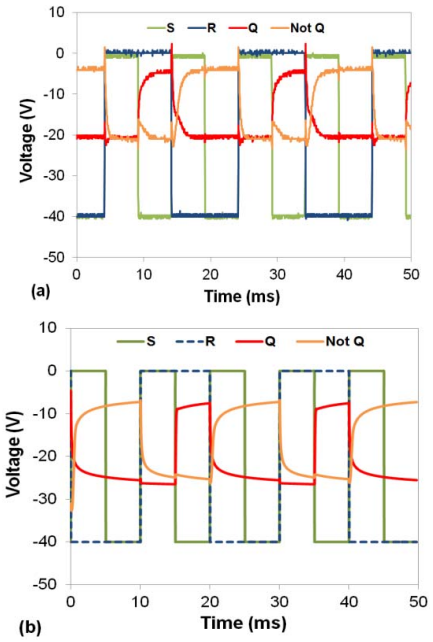


Fig. 6. (a) Experimental and (b) simulated response of an S–R latch.

### C. NAND-*Based S–R Latch*

S–R latches may be implemented using either NAND or NOR logic gates. Here, we present results obtained from a S–R latch based on cross-coupled NAND gates [Fig. 1(d)]. The truth table for the latch (Table II) shows that the outputs, i.e., the next states of Q and $\bar{Q}$, depend not just on the inputs S and R but also on the current state of the output. For example, if either input is 0 (low) and the other 1 (high), the outputs will be defined by the inputs. However, if both inputs are 1, the outputs will remain in their current state 0, 1 or 1, 0. When used in logic operations, two low inputs, i.e., 0, 0 are avoided for two reasons: 1) the memory state is lost—both outputs go high so one output is no longer the complement of the other and 2) the circuit may go unstable.

The various states may be observed in Fig. 6 for both the experimental and simulated S–R latch circuits. Starting at 10 ms in the experimental plots [Fig. 6(a)], S = 1 and R = 0 and results in Q = 0, $\bar{Q}$ = 1. Reversing the inputs to 0, 1 changes the outputs to 1, 0. At ∼20 ms, both inputs go high (1,1) but the outputs remain unchanged. When both inputs go low (0,0), both outputs go high, i.e., the invalid state. Simulations were undertaken [Fig. 6(b)] for this same input sequence, albeit time-shifted by 10 ms, and using the same OTFT model card as above for the inverter, NAND, and NOR gates. As can be seen, the simulation is in reasonable agreement with the measured response of the circuit.

### D. *Current Mirror*

A current mirror is a basic integrated circuit element serving to provide controlled bias currents or acting as a dynamic load for other circuits. The inset in Fig. 7 shows a modified Wilson mirror circuit that was fabricated and tested as part of the present program. Here, the reference current source $I_{\mathrm{REF}}$ will force the same current through transistor $T_1$ establishing a gate–source voltage $V_{\mathrm{GS}}$ also common to $T_2$, which then

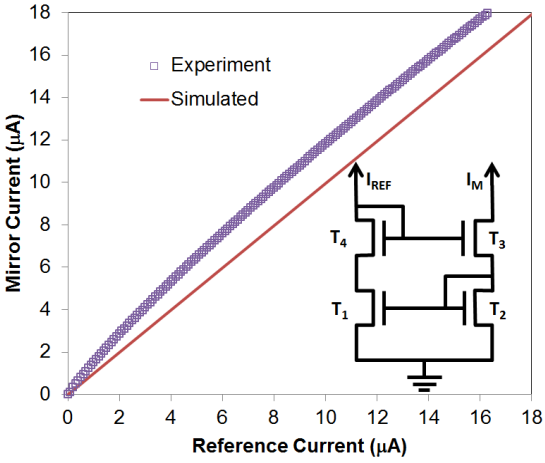


Fig. 7. Comparison of experimental and simulated performance of the current mirror circuit shown in the inset. The transistors were nominally identical with $W = 2500\ \mu$m and $L = 50\mu$m.

produces a current $I_M$ in the right branch. If $T_1$ and $T_2$ are exactly identical, then $I_M = I_{\mathrm{REF}}$. The actual circuit performance is shown in Fig. 7 together with the simulation.

Although all four TFTs were nominally identical, the departure from the ideal response as represented by the simulation, suggests that minor differences exist in the characteristics of transistors $T_1$ and $T_2$. It is readily shown [28] that, the difference in current $(I_{\mathrm{REF}}–I_M) = (I_{T1}–I_{T2}) = \Delta I_D$ is given by

$$\frac{\Delta I_D}{I_{\mathrm{REF}}} = \frac{2\Delta V_T}{(V_{GS} - V_{T1})} - \frac{\Delta\beta}{\beta_1} \tag{5}$$

where $V_{T1}$ and $\beta_1$ refer to $T_1$, $\Delta V_T = (V_{T1} - V_{T2})$ and $\Delta\beta = (\beta_1 - \beta_2)$.

The analysis shows that threshold voltage difference is more important at low $V_{\mathrm{GS}}$ with its effect diminishing at higher values. In crystalline silicon devices, carrier mobility is constant under normal operating conditions so that $\Delta\beta/\beta_1$ reduces to the fractional error in the aspect ratio, i.e., to $\Delta(W/L)/(W/L)_1$. However, at the current state of development of organic transistors, there will also be incremental differences in mobility between devices, with the further complication that the mobility is gate-voltage dependent, leading to a more complex dependence on $V_{\mathrm{GS}}$ than initially expected from (5).

Nevertheless, a controlled constant current source delivering up to 18 $\mu$A is more than sufficient for most analog circuit applications.

## IV. Conclusion

We have shown for the first time that logic devices ranging from simple inverters to the more complex S–R latch can be fabricated using a novel, vacuum-based, R2R compatible OTFT process. Propagation delay in the inverter is <200 $\mu$s enabling the operation of logic circuits at frequencies above 1 kHz. This frequency would be significantly enhanced by reducing gate–drain overlap capacitances in optimized devices. The fabrication process has also been used to produce a simple analog circuit, namely the modified Wilson current

mirror circuit. Although not showing ideal behavior, the circuit delivers a controlled output current up to 18 $\mu$A that changes linearly over most of the input current range albeit shifted by $\sim$2 $\mu$A to higher values. The reproducibly high yield of stable transistors produced by our process will readily allow expansion to more complex digital and analog circuits.

## ACKNOWLEDGMENT

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